Design of a Kind of Optimized Time-Lapse Macro VR Movie Recording System

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Abstract. With the popularization of VR head mounted displays (HMD), the demands for VR movies are rising rapidly. Traditionally, time lapse movies are usually used for educational purpose, but they can be significantly more vivid if they can be viewed in VR ways. The authors designed a kind of automatic control system targeted to record VR movies showing the slow process of change such as plant growing, astronomical phenomena, etc. The system is mainly consist of hardware module and software part. The system hardware includes five parts consisting of the main-control chip using FPGA, dual H-bridge motor drive circuit using L298N drive chip, two channels relay circuit with isolation using optical coupler, the three channels DC output switched-mode power supply, a slide track with a two phase four wire step motor as mechanical parts, which are used to support the camera controlled by a cable release. For the software part, Quartus II and Verilog HDL were used to program and control. It has many advantages, including adjustable micro spur, simple design, unattended operation for a long time, safe and convenient operations.

Keywords: Time-lapse Macro VR movies · FPGA · Step motor
Liner slide rail

1 Introduction

The fast development of VR glass meet people's new demand of pursuing stereo content because of more realistic feelings. However, there are many stereo natural phenomenon in the domain of science, whose states change very slowly so that people can't notice the change. The authors usually use time-lapse videos to amplify the change, and need to shoot them in a relatively close distance as in Macro Photography.

There are three methods used by this kind of photography at present. However, traditional stereo camera has big spacing between two lens, and the spacing is not adjustable. Existing macro stereo lens usually lead to poor image quality [2], and imaging size will be reduced by a half [3]. Using two cameras synchronously to take photos results in a bigger spacing between the two lens on two cameras than when using the camera with a single stereo lens. Hence, using two cameras is not a good option to take macro effect photo. Currently, there is still no ideal solution for this kind of requirement.

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Because object of time-lapse video changes very slowly, the authors then used a single camera by moving it on a liner slider rail. However, because the delay period may be for many days, the authors can't finish this kind of photography continuously by manual method. So the authors design an automatic control system based on FPGA [1], which can work automatically for a long time and has extra advantages of adjustable micro-interval, simple design, stable and convenient.

2 System Design

The hardware modules of automatic control system is designed based on FPGA as main-control chip, a power module, a liner slide rail, a step motor running on the liner slide rail, a L298N motor drive module, a two channels relay circuit module, the control principle of cable release, system machinery and power supply module. A camera was mounted on the liner slide rail, the shutter of the camera will be triggered by the cable release and the camera will move according to the step motor.

System logic was realized by software modules using Verilog HDL programming language in Quartus II software to drive and operate the whole system.

Figure 1 shows hardware modules diagram of the system.

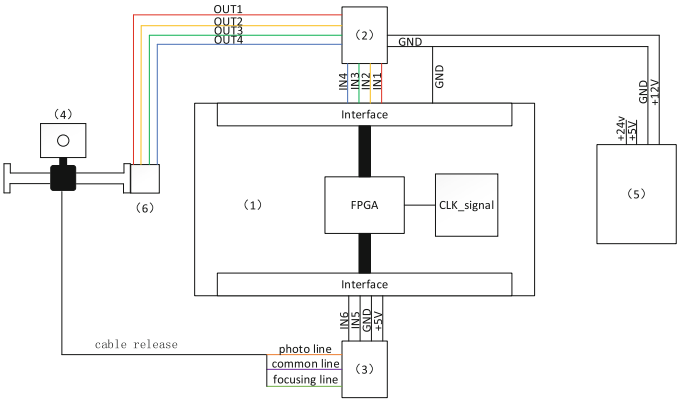

Fig. 1. System hardware modules block diagram (Color figure online)

2.1 Two Phase Four Wire Step Motor Timing Sequence

As the component (6) in Fig. 1, the system use a 42 series two phase four wire step motor, which contains four wires in red, yellow, green and blue corresponding to A+, B+, A−, B−. When FPGA pin sends a pulse to the motor, it will run 1.8°, and when FPGA sends pulses according to certain timing sequence, the motor will run incessantly. Here the authors use eight beats working mode because this mode can improve the system stability relative to four beats working mode [4]. The result is displayed in Table 1.

Table 1. Eight beats working mode timing sequence

	A	B	C	D	E	F	G	H
A+	1	1	0	0	0	0	0	1
B+	0	1	1	1	0	0	0	0
A−	0	0	0	1	1	1	0	0
B−	0	0	0	0	0	1	1	1

0 and 1 in table expresses given low and high level by FPGA relevant pins.

2.2 Main-Control Chip FPGA Module

Compared with the traditional design of step motor control, Altera ® FPGA has strong adaptive ability, adjustable DSP precision and effective electrical characteristics [5]. So the authors chose an Altera Cyclone EP1C3T144C8 FPGA mounted on a development board with 144 pins. In this part of work, as the component (1) in Fig. 1, the authors use totally 8 pins in FPGA, and their functions are given in Table 2.

Table 2. Pin numbers to name and corresponding function

Pin No. to name	Function
82 to IN1	Be used to link A+ wire of two phase four wire step motor
84 to IN2	Be used to link B+ wire of two phase four wire step motor
91 to IN3	Be used to link A− wire of two phase four wire step motor
96 to IN4	Be used to link B− wire of two phase four wire step motor
78 to IN5	Be used to link relay circuit module and finish auto-focusing function
98 to IN6	Be used to link relay circuit module and finish auto-photo function
100 to 5 V	Be used to act as power supply of relay circuit module
GND	Be used to form loop

The development board is equipped with a 48 MHz crystal oscillator in order to provide clock or pulse signal. In order to avoid resonance of step motor and slide rail [6], the system needs an appropriate step motor speed, so the authors used a 2400 Hz crossover module through instancing in the FPGA. This pulse frequency can avoid resonance effect after repeated experiments.

2.3 L298N Motor Drive Module

Step motor can be derived by relay or power transistor [7]. In the system, in order to adapt to the control requirement, for example, drive voltage, current, power, the authors design a dual H-bridge motor drive circuit based on L298N drive chip showed in the component (2) of Fig. 1, the module circuit is showed in Fig. 2.

L298N drive chip embeds dual H-bridge motor circuit, DriveOut(3) to DriveOut(0) respectively corresponds with 82, 84, 91, 96 pin of FPGA showed in Table 2, the four

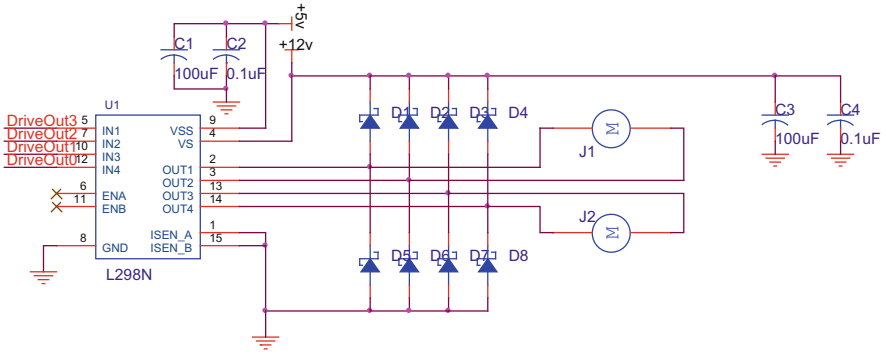

Fig. 2. L298N motor drive module circuit

wires can give same timing sequence as it in Table 1 to L298N so that the step motor will move without a break unless L298N receives a stop instruct (DriveOut(3) to DriveOut(0) is 4'b0) from FPGA.

C1, C2, C3, C4 are filter capacitors. In order to protect the step motor, the authors use eight freewheeling diode D1 to D8. J1, J2 are the load step motor symbols, and relevant motor control code will be stated in system software module part.

2.4 Two Channels Relay Circuit Module

In order to realize take photo and focusing automatically, the authors must accomplish communication automatically from FPGA to camera.

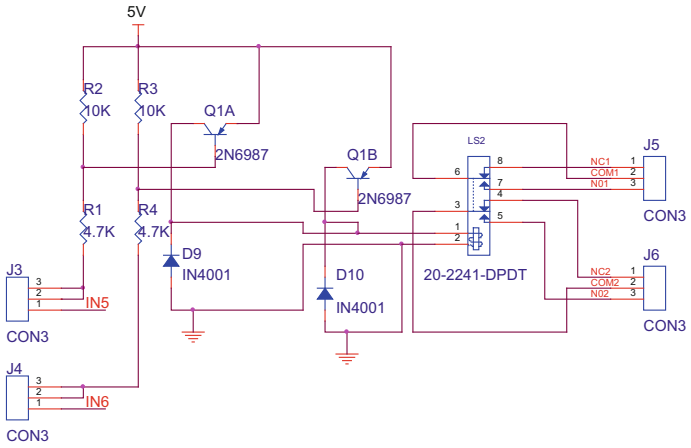

Fig. 3. Two channels relay module circuit

Two channels relay circuit and cable release are showed in the component (3) of Fig. 1. Figure 3 shows the detailed module circuit.

On the figure, IN5 and IN6 connect to FPGA number 78 and 98 pin and receive instruction from FPGA. The number 78 pin is for automatic focusing and the 98 pin for taking photo automatically. It can realize function switch on and off in fact when using the saturation conduction and cut-off character of transistor, but the load power of transistor is limited, so there should be a relay circuit amplification current from transistor [8]. The circuit uses low level to export from collector. R2 and R3 is pull-up resistor, the base will be high level when it is not offered pulse or voltage and now ungated because it is inverse transistor. It can be conductive when IN6 and IN5 offers low level to base, so when NO1 and NO2 is closed, NC1 and NC2 is opened with common port.

2.5 The Control Principle of Cable Release

In order to finish communication between relay module and camera, the authors use a strip of cable release to transmit signal. Its sketch map is showed in Fig. 4.

Fig. 4. Cable release sketch map (Color figure online)

The cable release consists totally of an interface and three lines [9]. The interface is used for inserting in camera. The purple line between is common. The orange line above used for taking photo, when the above and between line connect together, camera will open its shutter rapidly during a short time and take photo. Besides, camera will be focusing when the between lines and under dark green line connect together. But camera will open Blub gate when three lines connect together, this means that the camera will be exposed for a long time.

Figure 5 shows the interface of camera and relay module through cable release. The authors use FPGA number 98 pin to control J1 by first relay channel through IN5 pin of J3 and 78 pin to control J2 by second relay channel through IN6 pin of J4 in Fig. 3. When 98 pin gives low level to IN5 pin, the photo and common line will connect and camera will take photo.

Similarly, when 78 pin gives low level focusing and, the common line will be connected and the camera will be focusing.

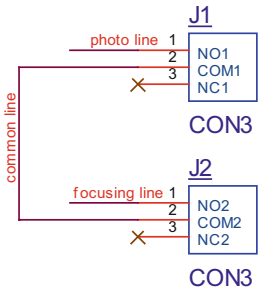

Fig. 5. The interface of camera and relay module

2.6 System Machinery and Power Supply Module

The camera can move and stop on the slide track that is about 220 mm long and has 8 mm screw pitch. System includes a three channels DC output Switch power supply represented by the component (5) of Fig. 1, it can offer +5 V, +12 V, +24 V power for our system, each channel maximal output current corresponding to 8 A, 2.5 A, 2 A respectively, so the power supply is enough for our L298N drive current. Figure 6 shows system setup.

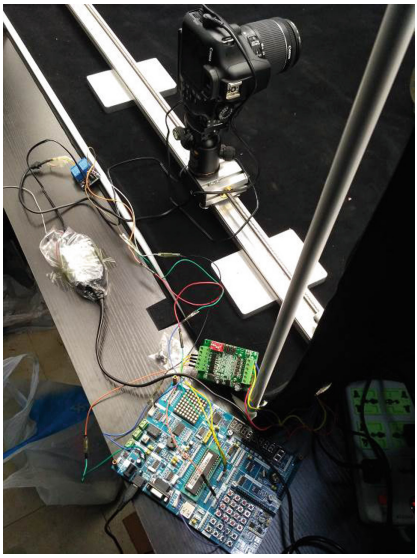

Fig. 6. System field entity

2.7 Software Modules and System Logic

System uses Verilog HDL programming language to implement function in Quartus II software. Figure 7 gives flow chart for achieving the requirement.

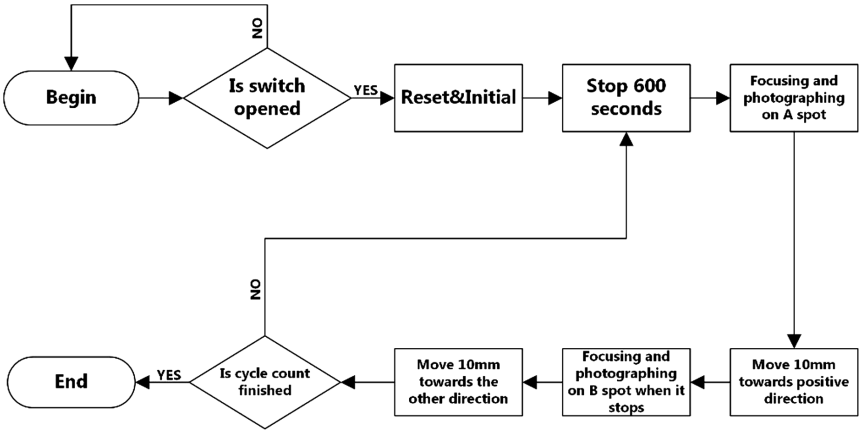

Fig. 7. Program flow chart.

3 Program Functionality Design and Application

In the basic logic of the time-lapse VR video recording, users could set spot A and spot B in the liner slide rail. The interval between A and B is adjustable freely so that system can reach micro spur target.

Usually the recorded objects change very slowly, in order to increase the production efficiency, the authors array a serials of objects in a line parallel to the liner slide rail, then record the objects one by one.

Another consideration is, in some situation, time-lapse VR videos might be displayed on naked eye stereoscopic displays, rather than a two-picture image pairs for traditional VR HMDs. Naked eye stereoscopic displays usually require four-picture image pairs, based on the above consideration, the recording method is designed as below (Fig. 8):

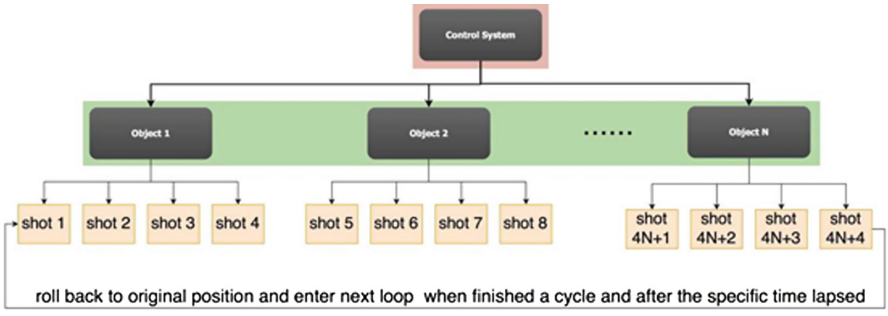

Fig. 8. Program functionality design

Four objects were arrayed parallel to the liner slide rail. For each object, four pictures were recorded in each loop. There is a gap of 5 mm between 2 adjacent shots for each object, and there is a 10-min interval between two loops, thus slightly changes could be recorded in detail.

4 Result Analysis

Three groups of pictures were selected to analyze the system, shown as Fig. 9.

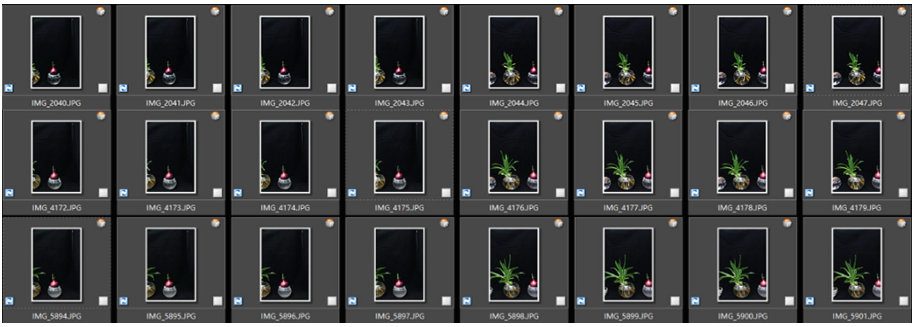

Fig. 9. Selected recorded image groups

The first group were recorded from 2017/04/16/13:26 to 13:28, the second group were recorded from 2017/04/19/10:53 to 10:56, the third group were recorded from 2017/04/21/18:51 to 18:53, it lasted for 5 days and 5 and a half hours, 3872 pictures were recorded, there are 968 shots for each object, and 242 shots at each fixed position.

To check the stability of this system, we compare two pictures recorded at the same position at 2017/04/16/13:26 and 2017/04/21/18:51, as shown in Fig. 10. From the obtained results, it could be easily seen that the still objects in two pictures match perfectly in both horizontal and vertical directions, as shown in Fig. 11.

Fig. 10. Two pictures recorded at the same position at 2017/04/16/13:26 and 2017/04/21/18:51

Fig. 11. Two pictures match perfectly in both horizontal and vertical directions

Fig. 12. Four-picture stereo pairs for naked eye stereoscopic display

Also any two pictures from a four-picture stereo (Fig. 12) pairs could form very comfort stereo effects. When displaying the four-picture stereo pairs on a naked eye stereoscopic display, users could see very comfortable stereo effects from more than one angles.

The only one unexpected thing is that there is too large difference between the change speeds of the 4 objects. Actually, they are 4 kinds of plants, only one of them changes in the first 5 days and it changes too fast, while the other 3 plants almost didn't change a little, one of the 3 even have root rot.

5 Conclusion

By using a liner slide rail, FPGA board, step motor and its drive circuit using L298N IC, machinery system, and a program wrote by Verilog HDL, the authors developed a kind of system that could record stable time-lapse VR video contents automatically for long period. The users could define the numbers of pictures in an image pairs, gap between shots, the time gap between loops to realize a flexible time-lapse VR contents recording.

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