Chapter 4
Schottky Rectifiers

A Schottky rectifier is formed by making a nonlinear contact between a metal and the semiconductor drift region. The Schottky rectifier is an attractive unipolar device for power electronics applications due to its relatively low on-state voltage drop and its fast switching behavior. It has been widely used in power supply circuits with low operating voltages due to the availability of excellent devices based upon silicon technology. In the case of silicon, the maximum breakdown voltage of Schottky rectifiers has been limited by the increase in the resistance of the drift region. Commercially available devices are generally rated at breakdown voltages of less than 100 V. Novel silicon structures that utilize the charge-coupling concept have allowed extending the breakdown voltage to the 200 V range [1, 2].

Many applications described in Chap. 1 require fast switching rectifiers with low on-state voltage drop that can also support over 500 V. The much lower resistance of the drift region for silicon carbide enables the development of such Schottky rectifiers with very high breakdown voltages [3]. These devices not only offer fast switching speed but also eliminate the large reverse recovery current observed in high-voltage silicon P-i-N rectifiers. This reduces switching losses not only in the rectifier but also in the IGBTs used within the power circuits [4].

In this chapter, the basic structure of the power Schottky rectifier is first introduced to define its constituent elements. The chapter then provides a discussion of the basic principles of operation of the metal-semiconductor contact. The current transport mechanisms that are pertinent to power devices are elucidated for both the forward and reverse mode of operation. In the first quadrant of operation, the thermionic emission process is dominant for power Schottky rectifiers. In the third quadrant of operation, the influence of Schottky barrier lowering has a strong impact on the leakage current for silicon devices. In the case of silicon carbide devices, the influence of tunneling current must also be taken into account when performing the analysis of the reverse leakage current.

The trade-off between reducing power dissipation in the on-state and the off-state for Schottky rectifiers is also analyzed in this chapter. This trade-off requires taking

© Springer International Publishing AG, part of Springer Nature 2019

B. J. Baliga, *Fundamentals of Power Semiconductor Devices*,
https://doi.org/10.1007/978-3-319-93988-9_4

into account the maximum operating temperature for the application. The power dissipation in the Schottky rectifier is shown to depend upon the barrier height as well as the duty cycle.

4.1 Power Schottky Rectifier Structure

The basic one-dimensional structure of the metal-semiconductor or Schottky rectifier structure is shown in Fig. 4.1 together with electric field profile under reverse bias operation. The applied voltage is supported by the drift region with a triangular electric field distribution if the drift region doping is uniform. The maximum electric field occurs at the metal contact. The device undergoes breakdown when this field becomes equal to the critical electric field for the semiconductor.

When a negative bias is applied to the cathode, current flow occurs in the Schottky rectifier by the transport of electrons over the metal-semiconductor contact and through the drift region as well as the substrate. The on-state voltage drop is determined by the voltage drop across the metal-semiconductor interface and the ohmic voltage drop in the resistance of the drift region, the substrate, and its ohmic contact.

At typical on-state operating current density levels, the current transport is dominated by majority carriers. Consequently, there is insignificant minority carrier stored charge within the drift region in the power Schottky rectifier. This enables switching the Schottky rectifier from the on-state to the reverse blocking off-state in

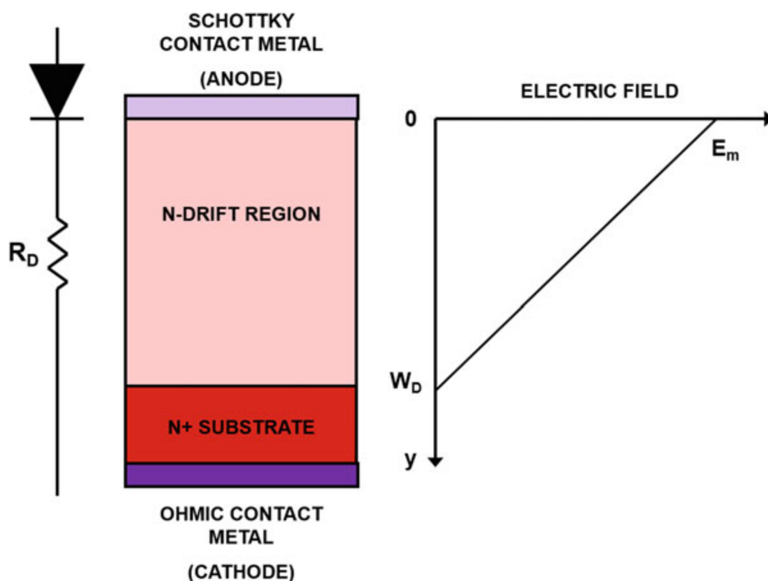

Fig. 4.1 Electric field distribution in a Schottky rectifier

a rapid manner by establishing a depletion region within the drift region. The fast switching capability of the Schottky rectifier enables operation at high frequencies with low power losses making this device popular for high-frequency switch-mode power supply applications. With the advent of high-voltage Schottky rectifiers based upon silicon carbide, they are being utilized in motor control and solar inverter applications as well.

4.2 Metal-Semiconductor Contact

Nonlinear current transport across a metal-semiconductor contact has been known for a long time. The potential barrier responsible for this behavior was ascribed to the presence of a stable space-charge layer by Walter Schottky in 1938. In this section, the principles for the formation of a rectifying contact between a metal and an N-type semiconductor region are described. This enables relating the Schottky barrier height between the metal and the semiconductor to their fundamental properties.

The energy band diagram for a metal and an N-type semiconductor are shown in Fig. 4.2 when they are isolated from each other. In general, the position of the Fermi level in the metal and the semiconductor will have different energy values. In the example shown in the figure, the Fermi level in the semiconductor lies above the Fermi level for the metal. The work function for the metal (ϕ_M) is defined as the energy required to move an electron from the Fermi level position in the metal (E_{FM}) to a state of rest in free space outside the surface of the metal. In the same manner, the work function for the semiconductor (ϕ_S) is defined as the energy required to move an electron from the Fermi level position in the semiconductor (E_{FS}) to a state of rest in free space outside the surface of the semiconductor. Since no electrons are located at the Fermi level position in the semiconductor, it is useful to define an electron affinity for the semiconductor (χ_S) as the energy required to move an electron from

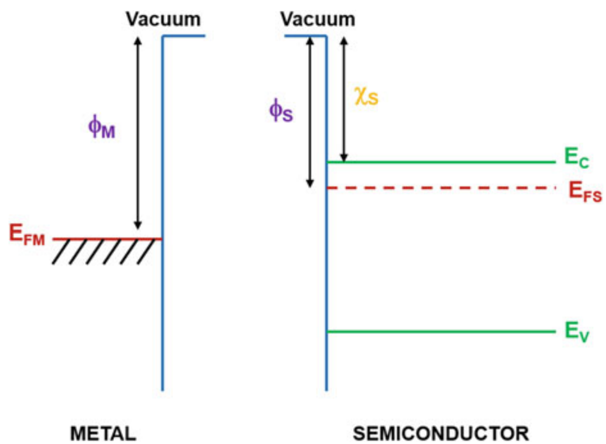

Fig. 4.2 Energy band diagram for a metal and a semiconductor in isolation

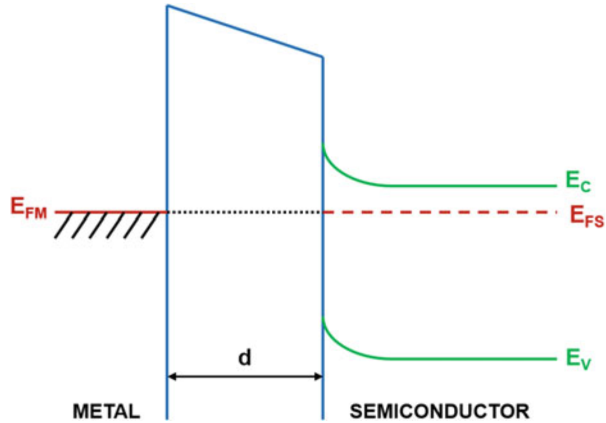

Fig. 4.3 Energy band diagram for the metal and semiconductor after making an electrical connection between them

the bottom of the conduction band in the semiconductor (E_C) to a state of rest in free space outside the surface of the semiconductor. The work function and electron affinity for the semiconductor are related by:

$$\Phi_S = \chi_S + (E_C - E_{FS}) \tag{4.1}$$

The potential difference between the Fermi level in the semiconductor and the Fermi level in the metal is called the *contact potential* (V_{CP}) which is given by:

$$qV_{CP} = (E_{FS} - E_{FM}) = \Phi_M - \Phi_S = \Phi_M - (\chi_S + E_C - E_{FS}) \tag{4.2}$$

The contact potential is also the built-in voltage for a Schottky barrier diode.

When an electrical connection is provided between the metal and the semiconductor, electrons are transferred from the semiconductor to the metal due to their greater energy until thermal equilibrium is established. This transfer of electrons creates a negative charge in the metal and a positive charge within a depletion region formed at the semiconductor surface. The resulting band structure is illustrated in Fig. 4.3 for the case of a separation "*d*" between the metal and the semiconductor surfaces. When the metal and the semiconductor surfaces are brought into contact by reducing the separation "*d*" to zero, the band structure for the metal-semiconductor contact is obtained as illustrated in Fig. 4.4. The entire contact potential is now supported within the depletion region formed at the surface of the semiconductor. This voltage is therefore also referred to as the *built-in potential* (V_{bi}) of the metal-semiconductor contact.

The Schottky barrier height (ϕ_{BN}) is related to the built-in potential by:

$$\Phi_{BN} = qV_{bi} + (E_C - E_{FS}) \tag{4.3}$$

Another useful relationship for obtaining the Schottky barrier height is:

$$\Phi_{BN} = \Phi_M - \chi_S \tag{4.4}$$

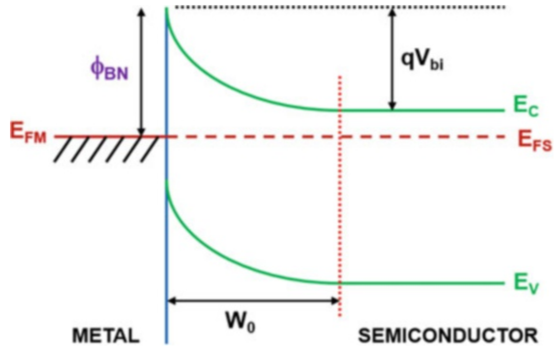

Fig. 4.4 Energy band diagram for the metal-semiconductor junction after making an intimate contact of their surfaces

because these properties for the materials can be measured. The built-in potential creates a depletion region within the semiconductor whose width is given by:

$$W_0 = \sqrt{\frac{2\varepsilon_S V_{bi}}{qN_D}} \tag{4.5}$$

4.3 Forward Conduction

Current flow across the metal-semiconductor junction can be produced by the application of a negative bias to the N-type semiconductor region. This produces a shift in the energy band structure as illustrated in Fig. 4.5. Current flow across the interface then occurs mainly due to majority carriers – electrons for the case of an N-type semiconductor. The current transport across the contact can take place via four basic processes [5] that are schematically shown in the figure:

(a) The transport of electrons from the semiconductor into the metal over the potential barrier – referred to as *thermionic emission current*
(b) The transport of electrons by quantum mechanical tunneling through the potential barrier – referred to as *tunneling current*
(c) The transport of electrons and holes into the depletion region followed by their recombination – referred to as *recombination current*
(d) The transport of holes from the metal into the neutral region of the semiconductor followed by recombination – referred to as the *minority carrier current*

In the case of power rectifiers, the doping concentration in the semiconductor must be relatively low in order to support the reverse bias (or blocking) voltage. This spreads the depletion region over a substantial distance. Consequently, the potential barrier is not sharp enough to allow substantial current via the tunneling process. The recombination current in the space-charge region is observable only at very low on-state current levels. The current transport due to the injection of holes is usually

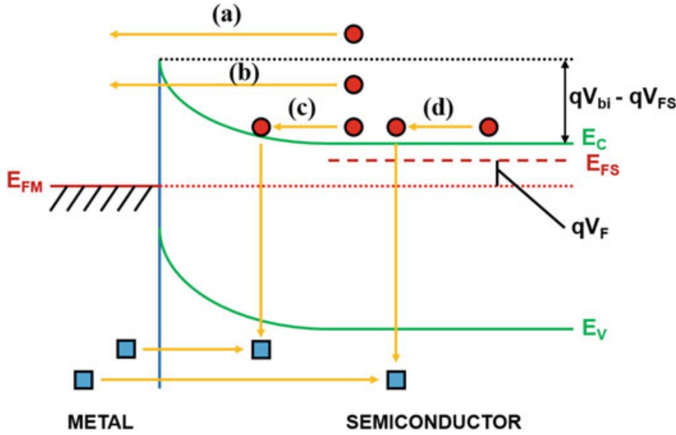

Fig. 4.5 Energy band diagram for a metal-semiconductor junction after the application of a forward bias voltage (electrons are shown as *red circles* and holes as *blue squares*)

negligible unless the Schottky barrier height is large. In power Schottky rectifiers, the barrier height is intentionally reduced to lower the on-state voltage drop making the minority carrier current small. Consequently, the current flow via the thermionic emission process is the dominant current transport mechanism in silicon and silicon carbide Schottky power rectifiers.

In the case of high-mobility semiconductors, such as silicon, gallium arsenide, and silicon carbide, and for power rectifiers with low doping concentrations in the semiconductor, the thermionic emission theory can be used to describe the current flow across the Schottky barrier interface [6]:

$$J = AT^2 e^{-(q\Phi_{\mathrm{BN}}/kT)}\left[e^{(qV/kT)} - 1\right] \tag{4.6}$$

where A is the effective Richardson's constant, T is the absolute temperature, k is Boltzmann's constant, and V is the applied bias. An effective Richardson's constant of 110, 140, and 146 A/cm^2-^{o}K^2 can be used for N-type silicon [6], gallium arsenide [6], and 4H silicon carbide [3], respectively. This expression, based upon the superimposition of the current flux from the metal and the semiconductor [7] which balance out at zero bias, holds true for both positive and negative voltages applied to the metal contact.

When a forward bias is applied (positive values for V in Eq. (4.6)), the first term in the square brackets of the equation becomes dominant allowing calculation of the forward current density using:

$$J_{\mathrm{F}} = AT^2 e^{-(q\Phi_{\mathrm{BN}}/kT)} e^{(qV_{\mathrm{FS}}/kT)} \tag{4.7}$$

where V_{FS} is the forward voltage drop across the Schottky contact.

In the case of power Schottky rectifiers, a thick lightly doped drift region must be placed below the Schottky contact as illustrated in Fig. 4.1 to allow supporting the reverse blocking voltage. A resistive voltage drop (V_R) occurs across this drift region which increases the on-state voltage drop of the power Schottky rectifier beyond V_{FS}. In case of current transport by the thermionic emission process, there is no modulation of the resistance of the drift region because minority carrier injection is neglected. Due to the small thickness (typically less than 50 μm) of the drift region for power Schottky diodes, it is grown on top of a heavily doped N^+ substrate as a handle during processing and packaging of the devices. The resistance contributed by the substrate (R_{SUB}) must be included in the analysis because it can be comparable to that of the drift region especially for silicon carbide devices. In addition, the resistance of the ohmic contact (R_{CONT}) to the cathode may make a substantial contribution to the on-state voltage drop.

The on-state voltage drop (V_F) for the power Schottky rectifier, after including the resistive voltage drop, is given by:

$$V_F = V_{FS} + V_R = \frac{kT}{q} \ln\left(\frac{J_F}{J_S}\right) + R_{S,SP} J_F \quad (4.8)$$

where J_F is the forward (on-state) current density, J_S is the saturation current density, and $R_{S,SP}$ is the total series-specific resistance. In this expression, the saturation current is given by:

$$J_S = AT^2 e^{-(q\Phi_{BN}/kT)} \quad (4.9)$$

and the total series-specific resistance is given by:

$$R_{S,SP} = R_{D,SP} + R_{SUB} + R_{CONT} \quad (4.10)$$

The saturation current is a strong function of the Schottky barrier height and the temperature as shown in Fig. 4.6 for silicon devices. (A corresponding plot for 4H-SiC is provided in Ref. [3] for the range of barrier heights typical for this material.) The barrier heights chosen for this plot are in the range for typical metal contacts with silicon. The saturation current density increases with increasing temperature and reduction of the barrier height. This has an influence not only on the on-state voltage drop but an even greater impact on the reverse leakage current as discussed in the next section.

As discussed in Chap. 1, the specific on-resistance of the drift region is given by:

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \quad (4.11)$$

The specific on-resistance of the drift region for 4H-SiC is approximately 2000 times smaller than for silicon devices for the same breakdown voltage (around 1000 V) as shown earlier in Fig. 3.6. Their values are given by:

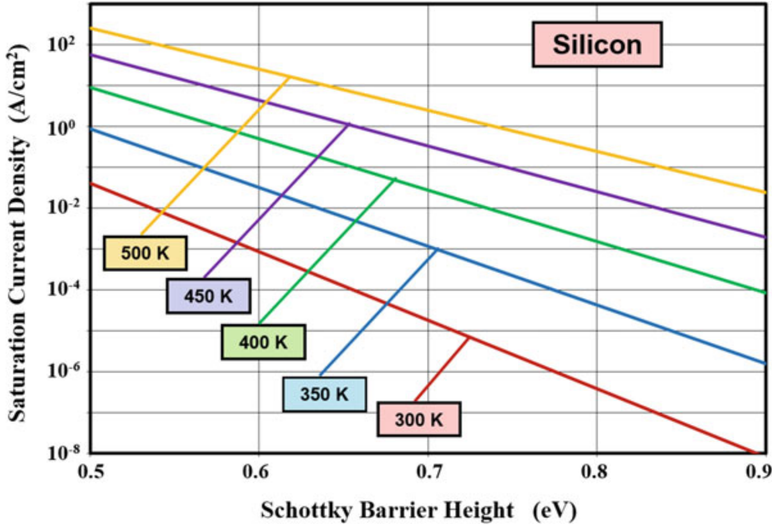

Fig. 4.6 Saturation current density for silicon Schottky barrier rectifiers

$$R_{D,SP} = R_{on\text{-}ideal}(\mathrm{Si}) = 8.4 \times 10^{-9}\mathrm{BV}^{2.5} \tag{4.12}$$

and

$$R_{D,SP} = R_{on\text{-}ideal}(4\mathrm{H}-\mathrm{SiC}) = 2.07 \times 10^{-12}\mathrm{BV}^{2.5} \tag{4.13}$$

if a constant mobility of 1360 cm^2/V-s is used for silicon and 1140 cm^2/V-s for 4H-SiC. This approximation works well for silicon but not for 4H-SiC because the doping levels are much larger resulting in reduced mobility.

In addition, it is important to include the resistance associated with the thick, highly doped N^+ substrate because this is comparable to that for the drift region in some instances. The specific resistance of the N^+ substrate can be determined by taking the product of its resistivity and thickness. For silicon, N^+ substrates with resistivity of 1 mΩ-cm are available. If the thickness of the substrate is 200 μm, the specific resistance contributed by the N^+ substrate is 2×10^{-5} Ω-cm^2. For silicon carbide, the available resistivity of the N^+ substrates is substantially larger. For the available substrates with a typical resistivity of 0.02 Ω-cm and thickness of 200 μm, the substrate contribution is 4×10^{-4} Ω-cm^2. The specific resistance of the ohmic contact to the N^+ substrate can be reduced to less than 1×10^{-6} Ω-cm^2 with adequate attention to increasing the doping concentration at the contact and by using ohmic contact metals with low barrier heights as discussed in Sect. 2.4.

The calculated forward conduction characteristics for silicon Schottky rectifiers are shown in Fig. 4.7 for various breakdown voltages. For this figure, a Schottky barrier height of 0.7 eV was chosen because this is a typical value used in actual power devices. It can be seen that the series resistance of the drift region does not

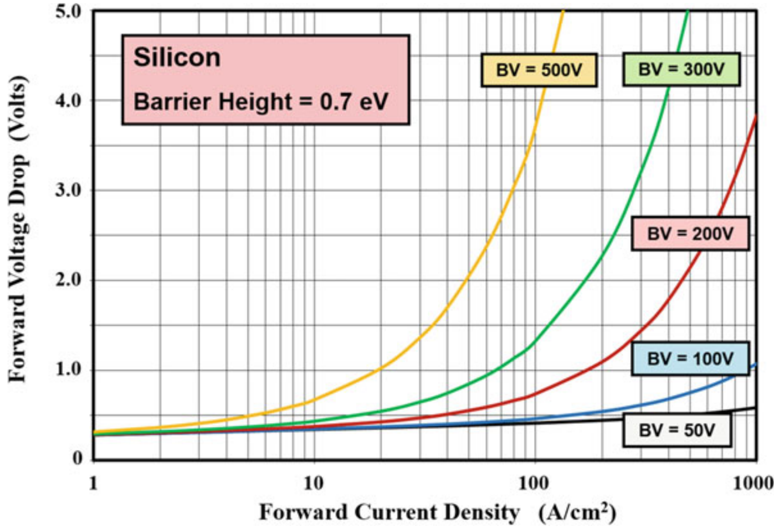

Fig. 4.7 Forward characteristics of silicon Schottky rectifiers

adversely impact the on-state voltage drop for the device with a breakdown voltage of 50 V at a nominal on-state current density of 100 A/cm^2. However, this resistance becomes significant when the breakdown voltage exceeds 100 V, limiting the application of silicon Schottky rectifiers to systems, such as switch-mode power supply circuits, operating at voltages below 100 V.

The significantly smaller resistance of the drift region enables scaling of the breakdown voltage of silicon carbide Schottky rectifiers to much larger voltages typical of medium and high power electronic systems, such as those used for motor control. The forward characteristics of high-voltage 4H-SiC Schottky rectifiers are shown in Fig. 4.8 for the case of a Schottky barrier height of 1.1 eV. The N$^+$ substrate resistance used for these calculations was 4×10^{-4} Ω-cm^2. It can be seen that the drift region resistance does not produce a significant increase in on-state voltage drop until the breakdown voltage exceeds 3000 V. From these results, it can be concluded that silicon carbide Schottky rectifiers are excellent companion diodes for medium and high power electronic systems that utilize insulated gate bipolar transistors (IGBTs). Their fast switching speed and absence of reverse recovery current can reduce power losses and improve the efficiency in motor control applications [4].

The choice of the Schottky barrier height has an impact on the on-state voltage drop. In order to illustrate this, the calculated forward conduction characteristics for silicon Schottky rectifiers are shown in Fig. 4.9 for various Schottky barrier heights. For this figure, a breakdown voltage of 50 V was chosen because this is a typical value for power devices. It can be seen that an increase in the on-state voltage drop occurs in proportion to the magnitude of the Schottky barrier height. It is therefore attractive to use a low Schottky barrier height for power rectifiers in order to reduce the on-state voltage drop.

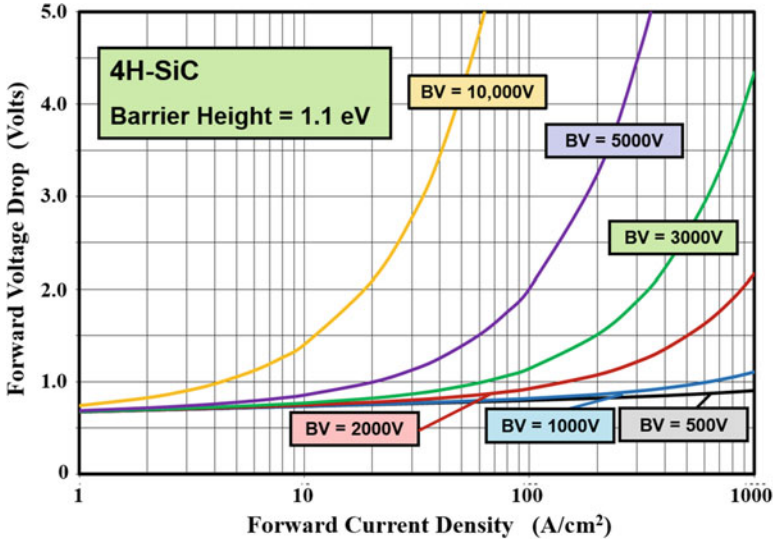

Fig. 4.8 Forward characteristics of 4H-SiC Schottky rectifiers

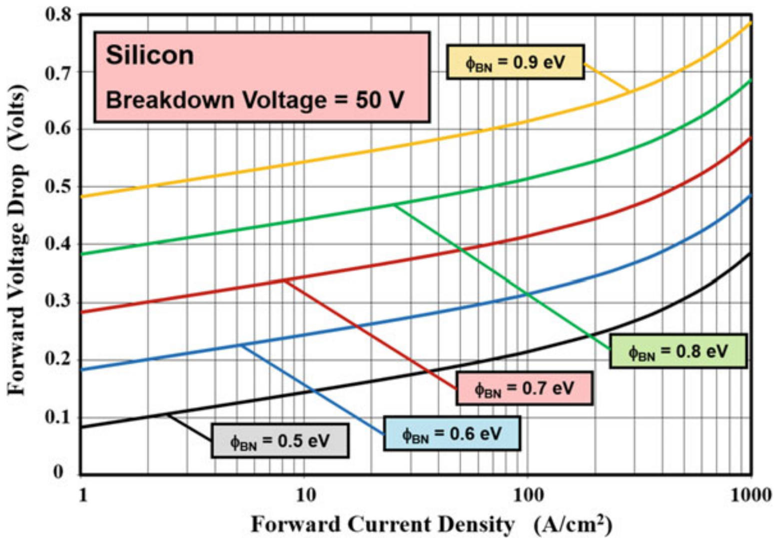

Fig. 4.9 Forward characteristics of silicon Schottky rectifiers

As discussed above, the on-state voltage drop for silicon Schottky power rectifiers designed to support low voltages is determined mainly by the voltage drop across the metal-semiconductor contact. By using Eqs. (4.8 and 4.9) and neglecting the resistive voltage drop, the on-state voltage drop is given by:

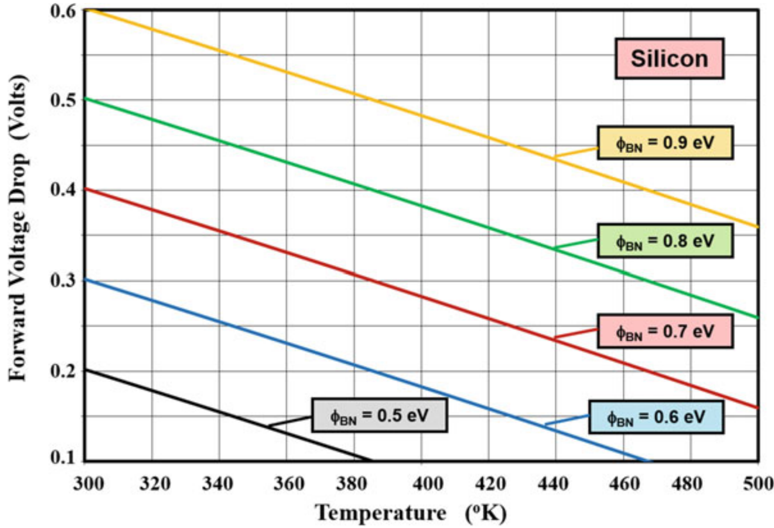

Fig. 4.10 Temperature dependence of the on-state voltage drop for silicon Schottky rectifiers

$$V_F = \Phi_{BN} + \frac{kT}{q} \ln\left(\frac{J_F}{AT^2}\right) \tag{4.14}$$

Since the logarithmic term in this expression has a negative value, the forward voltage drop for the Schottky diode decreases with increasing temperature. Examples of the variation of the on-state voltage drop for Schottky rectifiers with temperature are shown in Fig. 4.10 for various cases of the Schottky barrier height. The observed decrease in the on-state voltage drop with temperature is favorable for reducing power losses but can cause current localization within devices.

Simulation Example

The results of one-dimensional numerical simulations are provided in this section for the case of a device with a breakdown voltage of 50 V to gain further insight into the physics of operation for the Schottky rectifier. This is a typical breakdown voltage for commercially available silicon power Schottky rectifiers. This breakdown voltage was obtained with a drift region with doping concentration of 8×10^{15} cm^{-3} and thickness of 3 μm. The forward conduction characteristics were obtained by sweeping the cathode voltage in the negative direction. Simulations were performed for various values for the Schottky barrier height to examine the impact on the injection of minority carriers (holes) into the drift region. The minority carrier lifetimes (τ_{p0} and τ_{n0}) were assigned a value of 10 μs during these simulations.

The forward characteristics obtained with the simulations for these Schottky rectifiers are shown in Fig. 4.11 for various Schottky barrier heights. These characteristics are in excellent agreement with those shown in Fig. 4.9 based upon the analytical model. For example, the on-state voltage drop obtained at a current

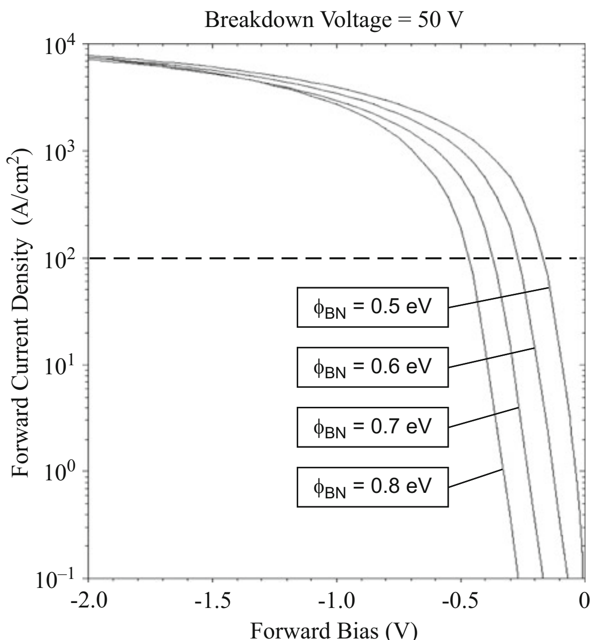

Fig. 4.11 Forward conduction characteristics for silicon Schottky rectifiers with breakdown voltage of 50 V

density of 100 A/cm^2 is 0.41 V for both the simulation and the analytical case when the barrier height is 0.7 eV. The analytical model is therefore sufficient for the analysis of the silicon Schottky rectifier.

The on-state current flow in the Schottky rectifier was discussed earlier with the aid of Fig. 4.5. It was pointed out that one of the current flow mechanisms is by minority carrier injection into the drift region. The simulations allow analysis of this contribution by examination of the hole concentration in the drift region. Since the injection process is known to be sensitive to the barrier height [8], the hole concentration in the drift region is shown in Fig. 4.12 for various barrier heights. In all cases, the on-state voltage drop was chosen as 0.5 V, which is the typical operating value for silicon rectifiers because it produces an on-state current density of about 100 A/cm^2. It can be observed that the injected hole concentration increases with increasing barrier height as expected. However, even for the largest barrier height of 0.8 eV, the injected hole density is less than 10^{13} cm^{-3} in the drift region, which is 1000 times smaller than the doping concentration. This confirms that the on-state operation of the silicon Schottky rectifier can be performed while neglecting the injection of minority carriers. It also confirms that the stored charge in the silicon Schottky rectifier is small allowing rapid switching from the on-state to the off-state during circuit operation.

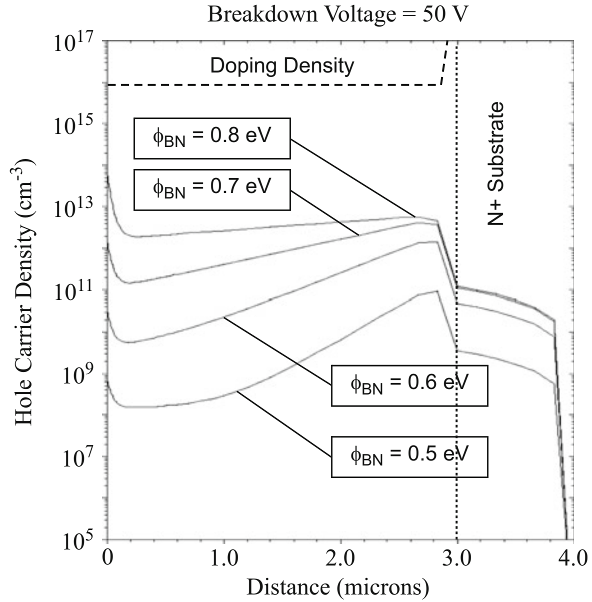

Fig. 4.12 Injected hole concentration for silicon Schottky rectifiers at an on-state voltage drop of 0.5 V

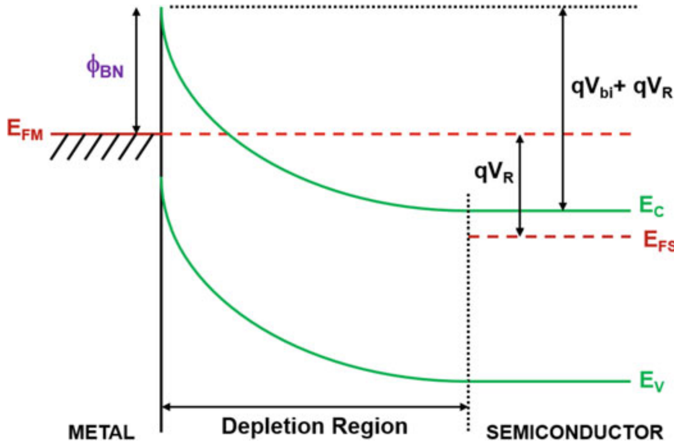

Fig. 4.13 Energy band diagram for a metal-semiconductor junction after the application of a reverse bias voltage

4.4 Reverse Blocking

When a reverse bias is applied to the Schottky rectifier, the voltage is supported across the drift region with the maximum electric field located at the metal-semiconductor contact as shown in Fig. 4.1. The energy band diagram corresponding to this condition is illustrated in Fig. 4.13. Since no voltage can be

supported within the metal, the reverse blocking capability of the Schottky rectifier is governed by the physics for the abrupt P-N junction that was discussed in Chap. 3. If a parallel-plane breakdown voltage is assumed, the drift region doping and width for a silicon device are given by:

$$N_D = 1.577 \times 10^{18} (BV_{PP})^{-4/3} \quad (4.15)$$

and

$$W_D = 2.87 \times 10^{-6} (BV_{PP})^{7/6} \quad (4.16)$$

In the case of actual power Schottky rectifiers, the breakdown voltage is constrained by breakdown at the edges. Edge terminations that have been used to raise the breakdown voltage of Schottky rectifiers close to the parallel-plane value are discussed in a later section of the chapter.

4.4.1 Leakage Current

The leakage current for Schottky rectifiers is comprised of three components:

(a) Space-charge generation current arising from the depletion region
(b) Diffusion current arising from carrier generation in the neutral region
(c) Thermionic emission current across the metal-semiconductor contact

Due to the relatively small barrier height utilized in silicon Schottky rectifiers, the thermionic emission component is dominant. The leakage current for the Schottky rectifier can be obtained by using Eq. (4.6) and substituting a negative bias of magnitude V_R applied to the diode:

$$J_L = AT^2 e^{-(q\Phi_{BN}/kT)} \left[e^{-(qV_R/kT)} - 1 \right] \quad (4.17)$$

Since the typical reverse bias voltages (V_R) are much greater than the thermal energy (kT/q), the exponential term in the square brackets becomes very small under reverse blocking conditions. Consequently, the leakage current is determined by the saturation current:

$$J_L = -AT^2 e^{-(q\Phi_{BN}/kT)} = -J_S \quad (4.18)$$

As previously discussed with reference to Fig. 4.6 for the saturation current, the leakage current due to the thermionic emission process is a strong function of the Schottky barrier height and the temperature. In order to reduce the leakage current and minimize power dissipation in the blocking state, a large Schottky barrier height is required. Further, a very rapid increase in leakage current occurs with increasing temperature, as shown in Fig. 4.14. If the power dissipation due to the leakage

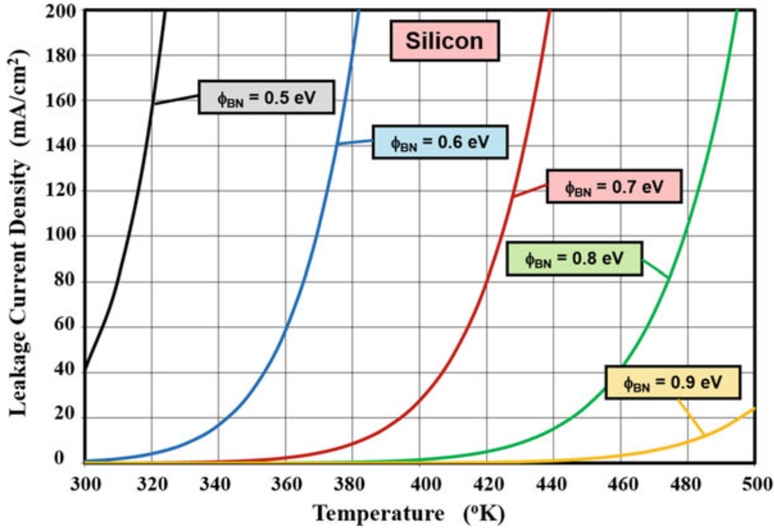

Fig. 4.14 Temperature dependence of the leakage current for silicon Schottky rectifiers

current becomes dominant, the resulting increase in the device temperature produces a positive feedback mechanism which can lead to unstable operation of the Schottky rectifier due to thermal runaway. This destructive failure mechanism for power Schottky rectifiers must be avoided by sufficiently increasing the Schottky barrier height even though this increases the on-state voltage drop. A larger Schottky barrier height is warranted for power Schottky rectifiers that must operate at higher ambient temperatures. This trade-off is discussed in more detail later in the chapter.

4.4.2 Schottky Barrier Lowering

Based upon the above analysis, the leakage current of the Schottky rectifier should be independent of the magnitude of the applied reverse bias voltage. However, actual power Schottky rectifiers exhibit a significant increase in the leakage current with increasing reverse bias voltage. This increase in the leakage current is far greater than the space-charge generation current within the expanding depletion region with increasing reverse bias voltage.

Under reverse blocking operation, it has been found that there is a reduction of the Schottky barrier height due the image force lowering phenomenon [9]. In order to analyze this phenomenon, consider the energy band diagram for the metal-semiconductor contact shown in Fig. 4.15. When an electron in the semiconductor approaches the metal at a distance x from the interface, a positive mirror image charge of the same magnitude occurs in the metal at a distance $-x$ from the interface. This produces an electrostatic force on the electron given by:

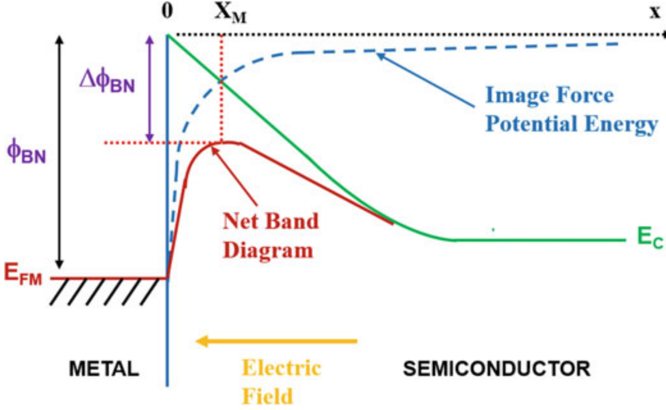

Fig. 4.15 Band diagram illustrating the image force lowering of the Schottky barrier height

$$F(x) = \frac{q^2}{4\pi\varepsilon_S (2x)^2} \tag{4.19}$$

This attractive force between the particles creates a negative potential energy for the electron inside the semiconductor, which is the work done to move the electron from position x to infinity. The corresponding image force potential (V_I) is given by:

$$qV_I = \int_x^{\infty} F(x)dx = -\frac{q^2}{16\pi\varepsilon_S}\int_x^{\infty}\frac{dx}{x^2} = -\frac{q^2}{16\pi\varepsilon_S x} \tag{4.20}$$

The negative image force potential combines with the positive potential due to the Schottky barrier producing a maximum at a distance X_M from the interface. At this location, the image force potential is equal to the potential drop across the depletion region due to the prevailing electric field indicated by the arrow in the figure. Since the maximum is located close to the interface, it can be assumed that the electric field at this location is approximately equal to the maximum electric field (E_M) at the Schottky contact. The illustration exaggerates the change in barrier height and the distance X_M to clarify the physics. Equating the image force potential (V_I) at location X_M to the potential drop ($E_M.X_M$) in the depletion region:

$$\frac{q}{16\pi\varepsilon_S X_M} = E_M X_M \tag{4.21}$$

The reduction of the barrier height due to the image force lowering phenomenon, indicated as $\Delta\Phi_{BN}$ in Fig. 4.15, is then given by:

$$\Delta\varphi_{BN} = 2E_M X_M \tag{4.22}$$

Using Eq. (4.21) to eliminate X_M, the barrier lowering is found to be determined by the maximum electric field (E_M) at the metal-semiconductor interface:

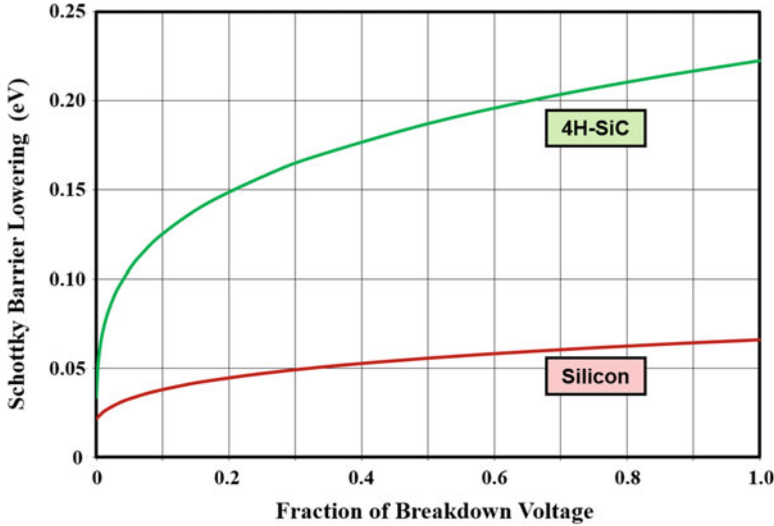

Fig. 4.16 Schottky barrier lowering for silicon and 4H-SiC Schottky rectifiers

$$\Delta\varphi_{\mathrm{BN}} = \sqrt{\frac{qE_{\mathrm{M}}}{4\pi\varepsilon_{\mathrm{S}}}} \tag{4.23}$$

For a one-dimensional structure, the maximum electric field is related to the applied reverse bias voltage (V_{R}) by:

$$E_{\mathrm{M}} = \sqrt{\frac{2qN_{\mathrm{D}}}{\varepsilon_{\mathrm{S}}}(V_{\mathrm{R}} + V_{\mathrm{CP}})} \tag{4.24}$$

where V_{R} is the reverse bias voltage and V_{CP} is the contact potential.

As an example, the reduction of the barrier height for a 60-V silicon Schottky rectifier is shown in Fig. 4.16. The reduction of the Schottky barrier height is 0.065 eV at the maximum reverse bias voltage. Although this change in barrier height may appear to be small, it can lead to a substantial increase in the leakage current with increasing reverse bias voltage.

The leakage current for the Schottky rectifier including the effect of Schottky barrier lowering is given by:

$$J_{\mathrm{L}} = -\mathrm{AT}^2 e^{-q(\varphi_{\mathrm{BN}} - \Delta\varphi_{\mathrm{BN}})/kT} \tag{4.25}$$

The leakage currents calculated with and without the Schottky barrier lowering effect are compared for the case of a silicon device with a breakdown voltage of 60 V in Fig. 4.17. In making these plots, the leakage current due to space-charge generation was neglected because it is much smaller than the leakage current across the metal-semiconductor contact. It can be seen that the leakage current is enhanced by a factor of five times due to the barrier lowering phenomenon as the reverse voltage increases and approaches the breakdown voltage.

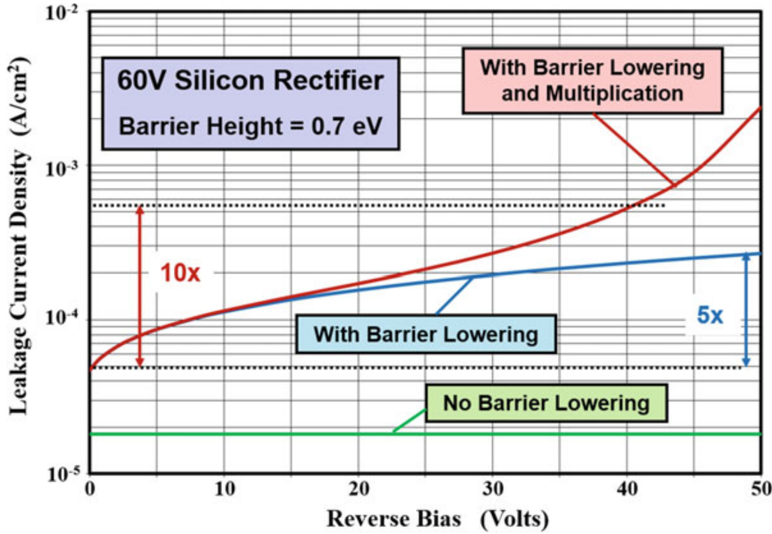

Fig. 4.17 Leakage current density for a 60V silicon Schottky rectifier

4.4.3 Pre-breakdown Avalanche Multiplication

The actual reverse leakage current for silicon Schottky rectifiers has been found to increase by an even greater degree than predicted by the Schottky barrier lowering phenomenon. This increase in leakage current can be accounted for by including the effect of pre-breakdown avalanche multiplication of the large number of free carriers being transported through the Schottky rectifier structure at the high electric fields associated with reverse bias voltages close to the breakdown voltage [10]. This impact ionization process can be treated as a purely electron initiated process due to the relatively large thermionic emission current across the metal-semiconductor contact. The total number of electrons that reach the edge of the depletion region will be larger than those crossing the metal-semiconductor contact by a factor M_n, which is the electron multiplication factor. An analytical expression for the electron multiplication factor can be derived by using a power series approximation for the impact ionization coefficients α_n and α_p:

$$\alpha_n = 6.6 \times 10^{-24} E^{4.93} \tag{4.26}$$

and

$$\alpha_p = 2.3 \times 10^{-24} E^{4.93} = 0.344\alpha_n \tag{4.27}$$

It has been assumed that the ratio of the impact ionization coefficients for electrons and holes remains independent of the electric field. The multiplication coefficient

(M_n) is then determined from the maximum electric field (E_M) at the metal-semiconductor contact:

$$M_n = \left\{1 - 1.52\left[1 - \exp\left(-7.22 \times 10^{-25} E_m^{4.93} W_D\right)\right]\right\}^{-1} \quad (4.28)$$

where W_D is the depletion layer width. The leakage current density for a silicon Schottky rectifier with drift region doping concentration of 1×10^{16} cm^{-3} is shown in Fig. 4.15 after including the influence of the pre-breakdown multiplication coefficient. The effect of including the multiplication coefficient is apparent at high voltages when the electric field approaches the critical electric field for breakdown. The leakage currents obtained, after including the effects of Schottky barrier lowering and pre-breakdown multiplication, are consistent with the characteristics of commercially available silicon devices, which exhibit an order of magnitude increase in leakage current from low reverse bias voltages to the rated voltage (about 80% of the breakdown voltage).

4.4.4 Silicon Carbide Rectifiers

Since the low specific on-resistance of the drift region in silicon carbide devices is associated with the much larger electric field in the material before the onset of impact ionization, the Schottky barrier lowering in silicon carbide rectifiers can be expected to be significantly larger than in silicon devices. For the case of a drift region doping level of 1×10^{16} cm^{-3}, the barrier lowering is found to be three times larger in silicon carbide at the corresponding breakdown voltage as shown in Fig. 4.14. In preparing this graph, the reverse voltage was normalized to the breakdown voltage because of the different breakdown voltages for the silicon (50 V) and silicon carbide devices (3000 V).

The enhanced Schottky barrier lowering in silicon carbide devices leads to a more rapid increase in leakage current with increasing reverse bias as shown in Fig. 4.18. The leakage current is predicted by this model to increase by about three orders of magnitude when the reverse voltage approaches the breakdown voltage. The observed increase in leakage current with applied reverse bias voltage for high-voltage silicon carbide Schottky rectifiers is much greater than can be accounted for with the Schottky barrier lowering model [11–13] despite the much larger barrier lowering effect. The experimentally observed increase in leakage current is about six orders of magnitude with increase in reverse bias voltage.

Tunneling Current

In order to explain the more rapid increase in leakage current observed in silicon carbide Schottky rectifiers, it is necessary to include the field emission (or tunneling) component of the leakage current [14]. The thermionic field emission model for the tunneling current leads to a barrier lowering effect proportional to the square of the

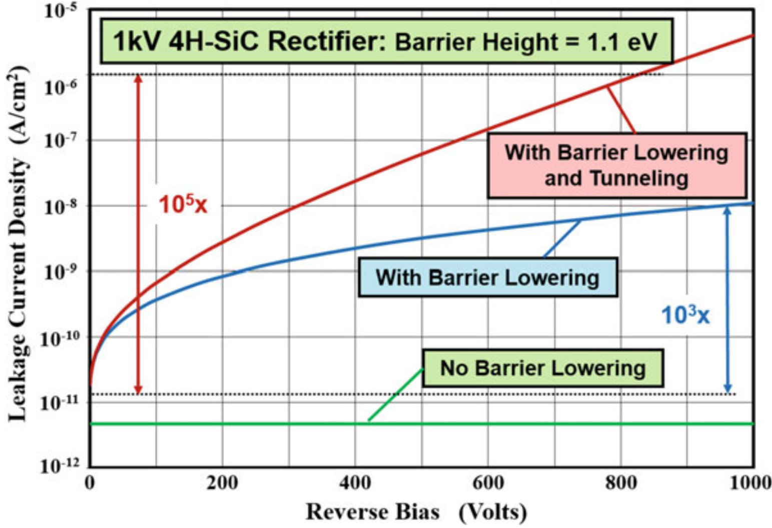

Fig. 4.18 Leakage current density for a 3 kV 4H-SiC Schottky rectifier

electric field at the metal-semiconductor interface. When combined with the thermionic emission model, the leakage current density can be written as:

$$J_S = AT^2 \exp\left(-\frac{q\varphi_{BN}}{kT}\right).\exp\left(\frac{q\Delta\varphi_{BN}}{kT}\right).\exp\left(C_T E_M^2\right) \tag{4.29}$$

where C_T is a tunneling coefficient. A tunneling coefficient of 8×10^{-13} cm^2/V^2 was found to yield an increase in leakage current by six orders of magnitude as shown in Fig. 4.18 consistent with the experimental observations. Thus, the inclusion of the tunneling model enhances the leakage current by another three orders of magnitude beyond that due to the Schottky barrier lowering phenomenon.

As discussed above, the leakage current in silicon carbide Schottky rectifiers increases much more rapidly with reverse voltage than in silicon devices. Fortunately, larger barrier heights can be utilized in silicon carbide devices when compared with silicon devices to reduce the absolute magnitude of the leakage current density because an on-state voltage drop of 1–1.5 V is acceptable for such high-voltage structures. This enables maintaining an acceptable level of power dissipation in the reverse blocking mode. For example, in the case of the 3 kV 4H-SiC Schottky diode discussed above, the reverse power dissipation at room temperature is less than 1 W/cm^2 compared with an on-state power dissipation of 100 W/cm^2. The expected increase in leakage current with temperature must of course be taken into account in order to ensure that the reverse power dissipation remains below the on-state power dissipation for stable operation. The leakage current can be suppressed by shielding the Schottky contact [3] using the JBS rectifier structure [15] originally proposed for silicon devices.

4.5 Device Capacitance

The reverse blocking voltage is supported across a depletion region in the power Schottky rectifier as shown in Fig. 4.11. The thickness of the depletion region (W_D) is related to the applied reverse bias voltage (V_R) by:

$$W_D = \sqrt{\frac{2\varepsilon_S}{qN_D}(V_R + V_{CP})} \tag{4.30}$$

where V_{CP} is the contact potential. The specific capacitance (capacitance per unit area) associated with this depletion region is given by:

$$C_{SBD,SP} = \frac{\varepsilon_S}{W_D} \tag{4.31}$$

where ε_S is the dielectric constant of the semiconductor.

The specific capacitance calculated using the above relationships is plotted in Fig. 4.19 for silicon Schottky rectifiers with breakdown voltages of 30, 50, and 100 V. For these plots, the contact potential was assumed to be 0.7 V. The specific capacitance decreases with increasing reverse bias voltage due to the expansion of the depletion region into the drift region. At any given reverse bias voltage, the specific capacitance is smaller for the higher breakdown voltage structure due to the smaller doping concentration in the drift region. A typical value for the specific capacitance for silicon Schottky rectifiers is 10^{-8} F/cm^2.

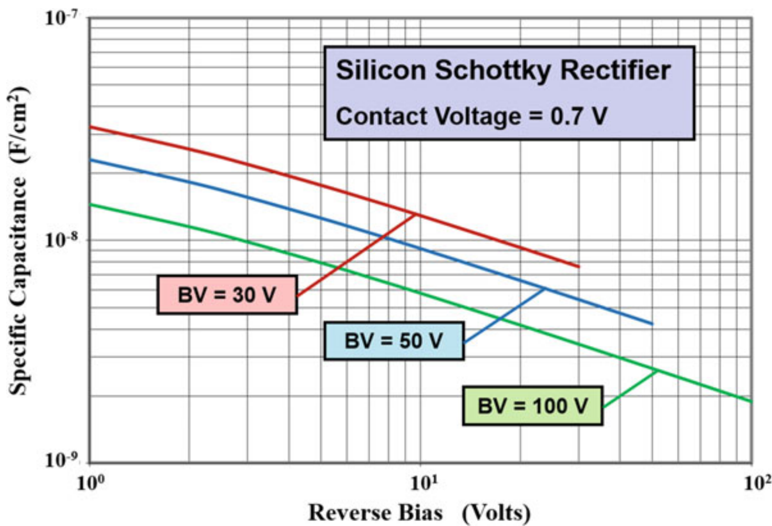

Fig. 4.19 Specific capacitance for silicon Schottky rectifiers

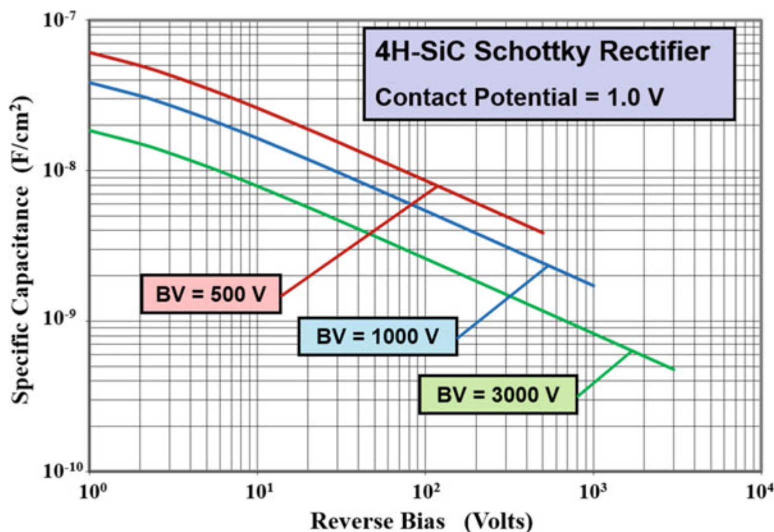

Fig. 4.20 Specific capacitance for 4H-SiC Schottky rectifiers

The specific capacitance for the 4H-SiC Schottky rectifiers calculated using the above relationships is plotted in Fig. 4.20. In this case, a slightly larger contact potential of 1.0 V was used due to the larger Schottky barrier heights utilized in silicon carbide devices. Larger values for the breakdown voltages for the silicon carbide Schottky diodes, of interest for their applications, were selected for this figure. The behavior of the specific capacitance is similar to that for silicon devices. A typical value for the specific capacitance for these higher breakdown voltage 4H-SiC Schottky rectifiers is also 10^{-8} F/cm^2.

4.6 Thermal Considerations

The Schottky power rectifier is used to control the direction of current flow in power circuits, such as switch-mode power supplies, operating at high frequencies. The device operates for a part of the cycle in the on-state and in the off-state for the rest of the cycle with rapid switching transients between these modes. A typical set of current-voltage waveforms for the Schottky rectifier are shown in Fig. 4.21 under the assumption that the switching intervals can be neglected. As discussed earlier in the chapter, the minority carrier stored charge is very small in the silicon Schottky rectifier allowing the device to rapidly switch between the on-state and the off-state. In practical circuit boards, care must be taken to ensure that current ringing due to the stray inductance of the board and the diode capacitance is minimized.

The power dissipation incurred in the power Schottky rectifier can be calculated by adding the power loss during the on-state with the power dissipated in the

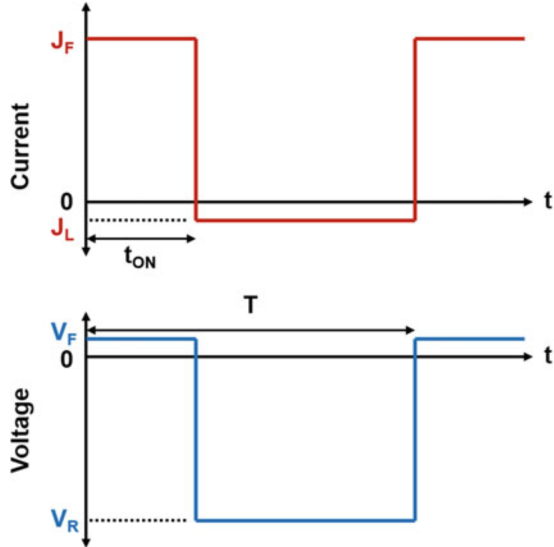

Fig. 4.21 Typical switching waveforms for a Schottky rectifier

off-state [16]. Unlike most power devices, the off-state power loss in the Schottky rectifier becomes significant, especially at elevated temperatures, due to the relatively large leakage current. If the power loss due to the leakage current becomes greater than the power loss due to the on-state current flow, the Schottky rectifier can undergo thermal runaway leading to destructive failure.

As shown in Fig. 4.21, typical Schottky rectifiers exhibit a voltage drop (V_F) during current conduction in the forward direction. This results in power dissipation per unit area in the on-state given by:

$$P_L(\text{on}) = \delta J_F V_F \tag{4.32}$$

where J_F is the on-state current density. In this expression, δ is referred to as the duty cycle given by:

$$\delta = t_{ON}/T \tag{4.33}$$

where t_{ON} is the on-state duration and T is the time period (the reciprocal of the operating frequency). The on-state power dissipation decreases with increasing temperature because the on-state voltage drop decreases as shown in Fig. 4.10.

The power dissipation per unit area in the off-state is given by:

$$P_L(\text{off}) = (1 - \delta) J_L V_R \tag{4.34}$$

where J_L is the leakage current exhibited by the device in its off-state due to supporting a reverse bias (V_R). The power dissipation in the off-state increases rapidly with temperature due to an increase in the leakage current as shown in Fig. 4.14.

The total power dissipation incurred in the diode is obtained by combining these terms:

$$P_{\mathrm{L}}(\mathrm{total}) = P_{\mathrm{L}}(\mathrm{on}) + P_{\mathrm{L}}(\mathrm{off}) \tag{4.35}$$

As the temperature of the diode is increased from room temperature, the on-state power dissipation decreases resulting in a reduction of the total power dissipation because the leakage current is small. However, the leakage current increases rapidly at high temperatures resulting in an increase in the power dissipation with temperature. Consequently, the power dissipation in the Schottky rectifier goes through a minimum with increasing temperature as illustrated in Fig. 4.22 for the case of a device with breakdown voltage of 50 V. A duty cycle of 50%, a Schottky barrier height of 0.7 eV, a reverse bias voltage of 30 V, and an on-state current density of 100 A/cm^2 were chosen for this example.

The maximum stable operating temperature for the Schottky rectifier is limited by the thermal impedance of the package and heat sink. If a tangent is drawn from the ambient temperature to the power dissipation curve as shown in Fig. 4.22, the maximum stable operating temperature is obtained as shown in the figure. Although stable operation is theoretically predicted below this temperature point, it is prudent to keep the maximum operating temperature below the point of minimum power dissipation indicated in the figure.

The Schottky barrier height has a strong influence on the maximum operating temperature and the minimum power dissipation. This is illustrated in Fig. 4.23 for the case of a silicon Schottky rectifier with a breakdown voltage of 50 V. Here, a duty cycle of 50% was chosen with a reverse bias voltage of 30 V and an on-state current density of 100 A/cm^2 for these diodes. As the barrier height is increased from

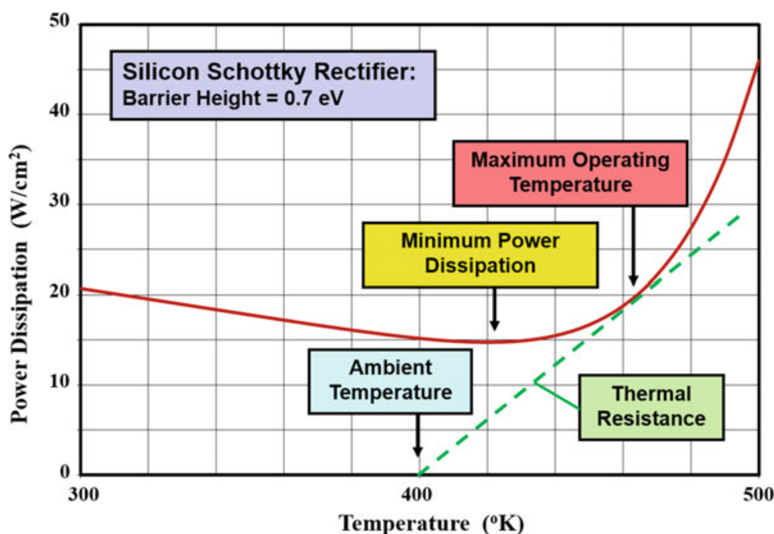

Fig. 4.22 Typical power dissipation for a silicon Schottky rectifier

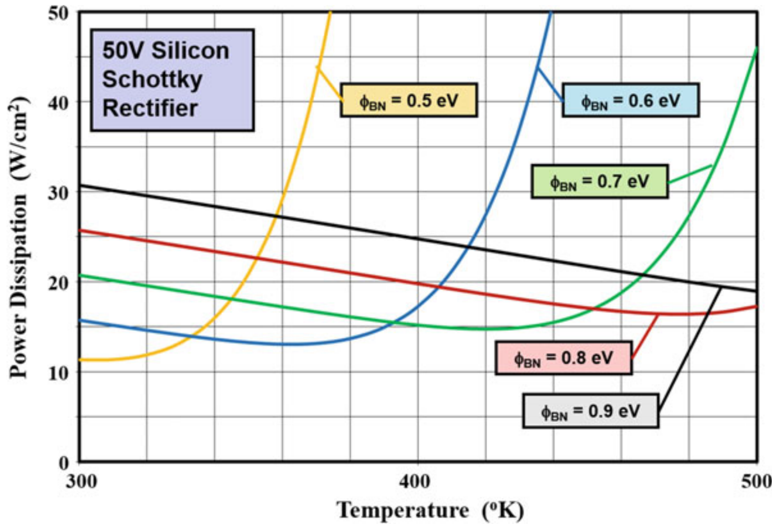

Fig. 4.23 Power dissipation for silicon Schottky rectifiers

0.5 to 0.9 eV, the temperature at which the minimum power dissipation occurs shifts from 300 °K to above 500 °K. Thus, it becomes necessary to use a larger Schottky barrier height when designing silicon Schottky rectifiers for high temperature operation. It can be observed from the figure that this is accompanied by an increase in the power dissipation within the rectifier.

The maximum operating temperature is also dependent on the duty cycle. This is illustrated in Fig. 4.24 for the case of 50 V silicon Schottky rectifiers with a barrier height of 0.7 eV. Here, a reverse bias voltage of 30 V and an on-state current density of 100 A/cm^2 were assumed for these diodes. It can be seen that at room temperature, the power dissipation is reduced for smaller duty cycles because the on-state power dissipation is dominant. However, the temperature at which the minimum power dissipation occurs, indicated by the red arrows in the figure, is also smaller for smaller duty cycles. It becomes necessary to raise the barrier for low duty cycle operation to enable operation at high temperatures leading to an increase in the power dissipation.

It is worth pointing out that all the power dissipation curves cross one another at the same temperature. This implies that there is a temperature at which the power dissipation becomes independent of the duty cycle. This temperature can be determined by using Eq. (4.35) with:

$$\frac{dP_{\mathrm{L}}}{d\delta} = 0 \tag{4.36}$$

By using Eqs. (4.14 and 4.17) for the on-state voltage drop and the leakage current, this condition is defined by:

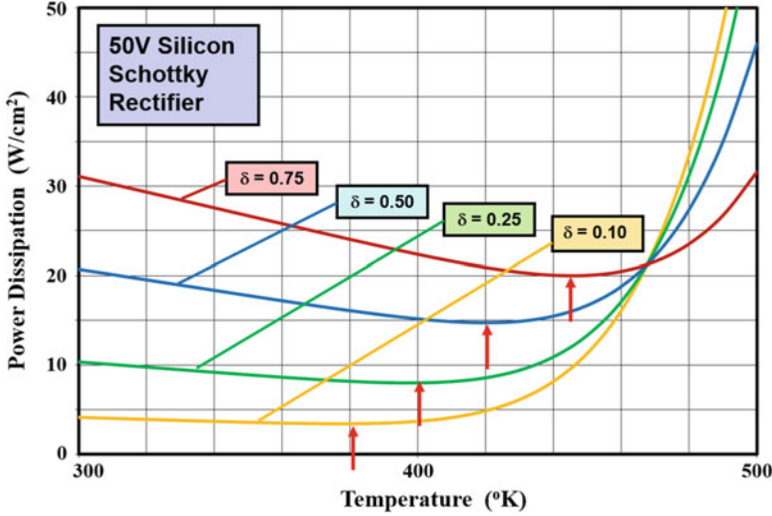

Fig. 4.24 Power dissipation for silicon Schottky rectifiers

$$J_{\mathrm{F}}\left[\varphi_{\mathrm{BN}}+\frac{kT}{q}\ln\left(\frac{J_{\mathrm{F}}}{\mathrm{AT}^2}\right)\right]-AT^2e^{-(q\phi_{\mathrm{BN}}/kT)}V_{\mathrm{R}}=0 \tag{4.37}$$

Iterative solution of this equation with the previously defined device parameters yields a temperature of 466 °K, which is in agreement with the plots in Fig. 4.24.

4.7 Fundamental Trade-Off Analysis

As demonstrated in the previous section, it is necessary to adjust the barrier height in order to minimize the power losses for applications. Low barrier heights should be chosen for power Schottky rectifiers that are intended for applications with large duty cycles where the power losses due to forward conduction are dominant. However, the leakage current increases resulting in a low maximum operating temperature if a small Schottky barrier height is chosen. Similarly, large barrier heights are required for Schottky rectifiers used in applications with high reverse bias stress and elevated ambient temperatures. It is therefore necessary to make a trade-off between reducing the forward voltage drop and minimizing the leakage current by appropriate choice of the barrier height.

In the case of low voltage (< 50 V) Schottky rectifiers, it is possible to neglect the influence of the series resistance on the on-state voltage drop. In this case, the on-state voltage drop is given by:

$$V_F = \Phi_{BN} + \frac{kT}{q} \ln\left(\frac{J_F}{AT^2}\right) \tag{4.38}$$

If the impact of Schottky barrier lowering and pre-breakdown avalanche multiplication is neglected, then the leakage current for the Schottky rectifier is equal to the saturation current density:

$$J_L = J_S = AT^2 e^{-(q\Phi_{BN}/kT)} \tag{4.39}$$

A fundamental trade-off relationship that is useful during the design of Schottky power rectifiers can be derived by combining the above equations with the elimination of the barrier height:

$$J_L = J_F e^{-(qV_F/kT)} \tag{4.40}$$

The calculated trade-off curves for Schottky rectifiers operating at various junction temperatures are shown in Fig. 4.25. It is worth pointing out that these trade-off curves are fundamental in nature because they are independent of the semiconductor material (not accounting for the small difference in the Richardson's constant). This implies that the performance of silicon Schottky rectifiers with low breakdown voltages cannot be improved by replacement with other semiconductors, such as gallium arsenide or silicon carbide. Thus, the plots in Fig. 4.25 establish the minimum expected leakage current in Schottky rectifiers for any given on-state voltage drop and operating temperature. For example, the trade-off curve for 400 °K indicates that the minimum leakage current for a Schottky rectifier will be

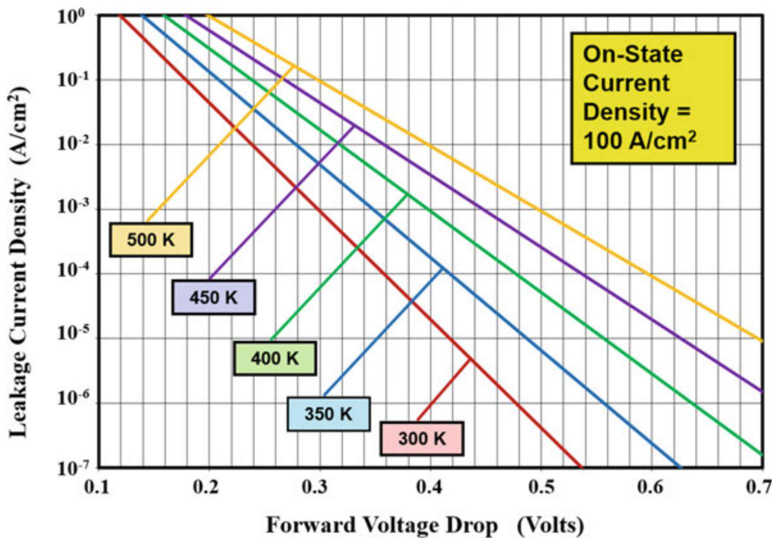

Fig. 4.25 Fundamental trade-off curves for Schottky rectifiers

1 mA/cm^2 if the barrier height is chosen to obtain an on-state voltage drop of 0.4 V. The performance of actual devices can be expected to be worse than this due to the impact of the series resistance on increasing the on-state voltage drop and the influence of Schottky barrier lowering and pre-breakdown avalanche multiplication on increasing the leakage current.

4.8 Device Technology

A variety of metals have been used to manufacture silicon Schottky barrier rectifiers. As previously pointed out, it is necessary to use a metal with low barrier height to reduce the power dissipation. This is satisfactory if the operating ambient temperature for the diode is low. As the ambient temperature increases, it becomes necessary to use metals with larger barrier heights to suppress the leakage current. The Schottky barrier height depends upon the work function of the metal. The work functions and corresponding barrier heights [17] are tabulated in Fig. 4.26 for cleaved silicon surfaces with metal deposited in an ultrahigh vacuum environment. As expected, the barrier height increases with increasing work function for the metal. These values for the barrier height are consistent with an electron affinity of about 4.0 eV for silicon.

When the metal-silicon interface is subjected to an anneal process at elevated temperatures, the metal reacts with the silicon producing a metal silicide which has a different work function. The measured barrier heights for various metal silicides on N-type silicon are provided in Fig. 4.27. Platinum silicide is commonly used for power Schottky rectifiers that must be designed to operate at high temperatures.

Metal	Cr	W	Mo	Pt
Work Function (eV)	4.50	4.60	4.60	5.30
Barrier Height (eV)	0.57	0.61	0.59	0.81

Fig. 4.26 Work functions and Schottky barrier heights for metals on silicon

Fig. 4.27 Schottky barrier heights for metal silicides on silicon

Metal-Silicide	$CrSi_2$	WSi_2	$MoSi_2$	$PtSi_2$
Barrier Height (eV)	0.57	0.65	0.55	0.78

4.9 Barrier Height Adjustment

The barrier height is usually decided by the choice of the metal when manufacturing power Schottky rectifiers. An alternative approach to adjusting the barrier height is by employing a shallow ion implant at the surface of the semiconductor. The addition of a surface layer, whose thickness is less than the electron mean free path of about 100 angstroms, with a carefully controlled dose, can change the effective barrier height between the metal and the semiconductor [18]. For an N-type drift region, the addition of an N-type surface layer will reduce the effective barrier height, while it will be increased by the incorporation of a P-type surface layer. This method is attractive because it allows the selection of the metal based upon the metallurgical properties of the interface with the semiconductor for stable operation while simultaneously tailoring the barrier height using the ion-implanted layer for the intended application. The optimization of the barrier height for power Schottky rectifiers can be achieved by starting with a large barrier height and then reducing the barrier by ion implantation of an N-type surface layer into the N-type drift region.

In order to analyze the reduction of the barrier height, the doping profile for this case is shown in Fig. 4.28 under the assumption of a uniform concentration in the surface layer and the drift region. The electric field profile for this doping profile is also shown in the figure. The slope of the electric field profile in the zone from $x = 0$ to $x = a$ is determined by the larger doping concentration of the surface layer while that in the drift region from $x = a$ to $x = W$ is determined by its lower doping concentration. It can be seen from the band diagram in Fig. 4.28 that a narrow

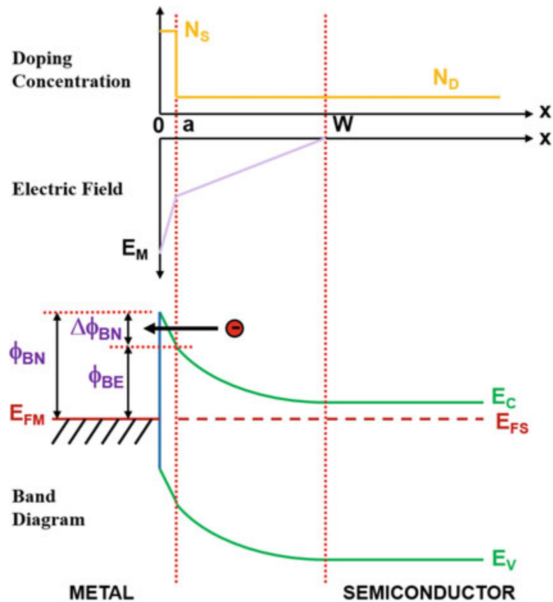

Fig. 4.28 Metal-semiconductor contact with a thin, highly doped, n-type surface layer

potential barrier is formed at the metal-semiconductor interface. As indicated in the figure, electrons can pass through this barrier creating a tunneling current. This additional current component can be analyzed as a reduction in the barrier height producing an enhancement of the thermionic emission current.

The electric field profile obtained by solving Poisson's equation with the doping profile shown in Fig. 4.28 is given by the following equations:

$$E(x) = -E_{\mathrm{M}} + \frac{qN_{\mathrm{S}}x}{\varepsilon_{\mathrm{S}}} \tag{4.41}$$

from $x = 0$ to $x = a$ and

$$E(x) = -\frac{qN_{\mathrm{D}}}{\varepsilon_{\mathrm{S}}}(W - x) \tag{4.42}$$

from $x = a$ to $x = W$. The maximum electric field (E_{M}) at the metal-semiconductor contact is given by:

$$E_{\mathrm{M}} = \frac{q}{\varepsilon_{\mathrm{S}}}[N_{\mathrm{S}}a + N_{\mathrm{D}}(W - a)] \tag{4.43}$$

The reduction of the Schottky barrier height can be obtained by substitution of this expression into Eq. (4.23). If the dose ($N_{\mathrm{S}}.a$) of the ion implant to create the N-type surface layer is much greater than the charge in the depletion region at zero bias, the reduction of the barrier height is given by:

$$\Delta\varphi_{\mathrm{BN}} = \frac{q}{\varepsilon_{\mathrm{S}}}\sqrt{\frac{aN_{\mathrm{S}}}{4\pi}} \tag{4.44}$$

The effective barrier height (ϕ_{BE}) can be calculated by subtracting this barrier reduction from the metal-semiconductor barrier height (ϕ_{BN}).

The reduction of the Schottky barrier height that can be achieved with a shallow N-type ion implant is shown in Fig. 4.29. It is possible to obtain a barrier reduction in the range of 0.05–0.15 eV by using a dose of between 10^{12} and 10^{13} cm^{-2}. This has been experimentally confirmed by using antimony implanted into an N-type drift region [19]. Antimony was chosen as the N-type dopant because of its large mass and low diffusion coefficient in silicon. The large atomic mass for antimony ensures that the dopant is located close to the silicon surface for ion implant energies of 5–10 keV, the lowest energies available in commercial ion implanters. Its low diffusion coefficient ensures that the dopant does not get redistributed during the post-implant annealing step to activate the dopant and remove the implant damage. It has been found that the damage from ion implantation can also alter the barrier height as well as contribute to leakage current by the generation of current at the metal-semiconductor interface via deep levels in the bandgap. Consequently, appropriate annealing steps are required after the ion implant to produce good Schottky diode characteristics.

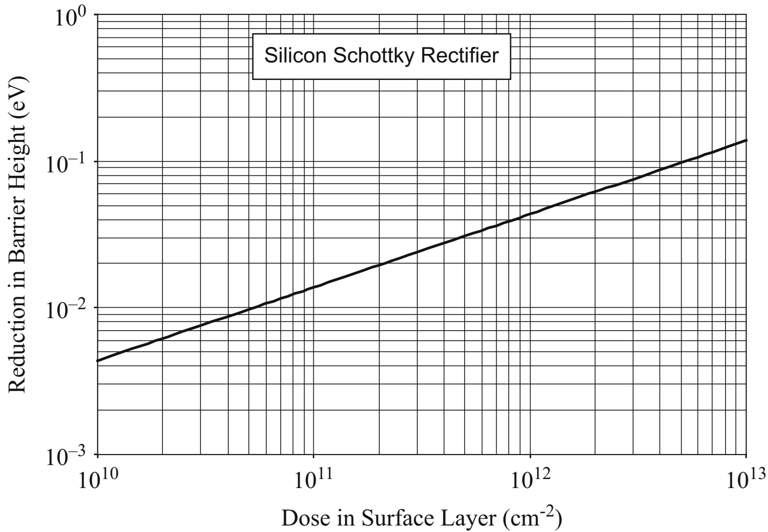

Fig. 4.29 Reduction of the Schottky barrier height with a thin, highly doped, N-type surface layer

4.10 Edge Terminations

The power Schottky barrier rectifier can be fabricated without the need for the additional processing steps that are required for creating P-N junctions. A Schottky rectifier with a metal field plate structure is illustrated in Fig. 4.30(a) with thermally grown silicon dioxide as the passivation at the edges. With this edge termination, a high electric field develops at the edges of metal (at point A). This not only degrades the breakdown voltage but contributes to the enhancement of the leakage current due to Schottky barrier lowering. The extension of Schottky contact metal over the oxide reduces the electric field at point A as discussed for field plates in Chap. 3. Care must be taken to design the field plate termination so that premature breakdown is not initiated at point B.

An improved field plate structure, illustrated in Fig. 4.30(b), can be created by using the LOCOS (Local Oxidation of Silicon) process. In the LOCOS process, a tapered field oxide is grown at the edges by utilizing a silicon nitride mask in the active area of the diode. This produces a tapered oxide at the edges due to formation of the "birds-beak" effect, as illustrated in the figure, which assists in reducing the electric field at Schottky metal contact.

A more commonly used approach for providing the edge termination for silicon Schottky power rectifiers is by incorporation of a P^+ guard ring, as illustrated in Fig. 4.30(c), even though this entails extra processing steps. The guard rings overlap the edges of the Schottky contact metal completely screening it from high electric fields. The breakdown voltage of this edge termination is the same as that of the cylindrical junction discussed in Chap. 3 if the corners of the diode are sufficiently

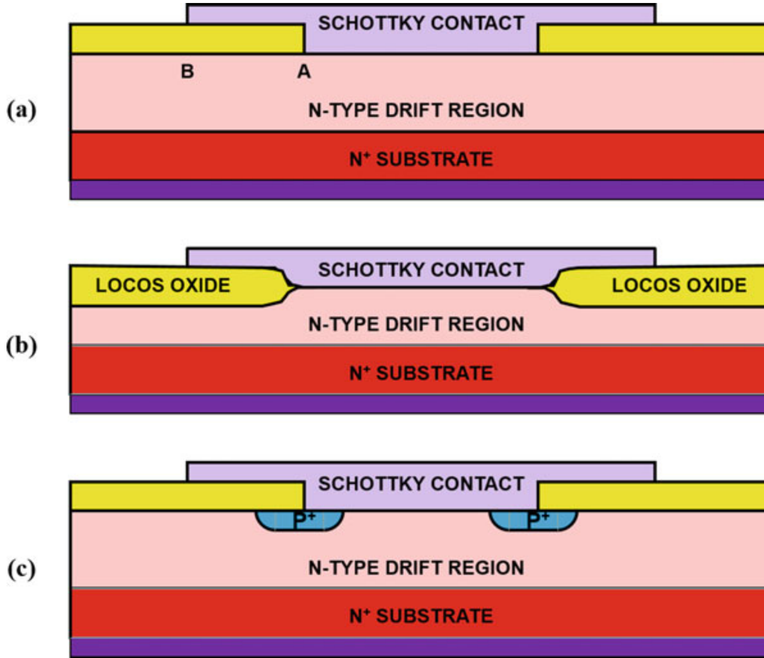

Fig. 4.30 Edge terminations for Schottky barrier rectifiers

rounded to avoid formation of spherical junctions. The presence of the P^+ guard ring creates a P-N junction in parallel with the Schottky diode. If the Schottky rectifier is designed to operate with an on-state voltage drop below 0.6 V, as is typical for silicon Schottky rectifiers with low breakdown voltages, the P-N junction does not get sufficiently forward biased to inject minority carriers into the drift region under normal operating conditions. This preserves the fast switching properties of the Schottky rectifiers essential for their application in high-frequency power circuits. Under surge current levels, where the diode is subjected to a very high on-state current density, the injection from the P-N junction is beneficial for reducing the on-state voltage drop and power dissipation.

4.11 Reverse Recovery Current

It will be shown in Chap. 5 that P-i-N rectifiers exhibit a large reverse recovery current flow due to stored charge inside the drift region produced by the on-state current flow. There is no stored charge in Schottky rectifiers due to majority carrier transport in the on-state. Despite this, a reverse recovery current is observed in Schottky rectifiers due to the capacitance of the device.

Consider the case of a Schottky rectifier which undergoes switching from the on-state to the off-state with a constant rate of change (δ) of the anode voltage. The reverse voltage across the device is then given by:

$$V_R(t) = (V_{bi} + \delta t) \tag{4.45}$$

where V_{bi} is the built-in voltage of the Schottky contact. The reverse current produced by this [*dV*/*dt*] applied to the Schottky diode can be obtained using its capacitance $C(V)$:

$$J_R(t) = C(V)\left[\frac{dV}{dt}\right] = \frac{\varepsilon_S}{W_D(V)}\delta \tag{4.46}$$

where $W_D(V)$ is the width of the depletion region. The width of the depletion region is given by:

$$W_D(t) = \sqrt{\frac{2\varepsilon_S[V_R(t) + V_{bi}]}{qN_D}} = \sqrt{\frac{2\varepsilon_S(\delta t + V_{bi})}{qN_D}} \tag{4.47}$$

where N_D is the doping concentration of the drift region. Using this expression in Eq. (4.46):

$$J_R(t) = \sqrt{\frac{qN_D\varepsilon_S\delta^2}{2(\delta t + V_{bi})}} \tag{4.48}$$

As an example, the reverse recovery current density is shown in Fig. 4.31 for case of a drift region doping concentration of 1×10^{16} cm^{-3} corresponding to a Schottky diode with breakdown voltage of about 50 V. A reverse voltage ramp rate of 1×10^7 V/s was assumed here with the resulting waveform shown in Fig. 4.31. The largest reverse current density occurs at zero crossing because of the largest capacitance with a maximum value of about 0.3 A/cm^2. This is a relatively small reverse recovery current when compared with P-i-N rectifiers.

4.12 Summary

The physics of operation of the Schottky rectifier has been described in this chapter. For power devices with relatively high breakdown voltages, the dominant current conduction mechanism is by the thermionic emission process. This process governs the fundamental relationship between the on-state voltage drop and the leakage current for power Schottky rectifiers. For power Schottky rectifiers, it is necessary to include the impact of the series resistance of the drift region on the on-state voltage drop. This series resistance limits the performance of silicon rectifiers to a breakdown voltage of less than 200 V. In addition, the Schottky barrier lowering and

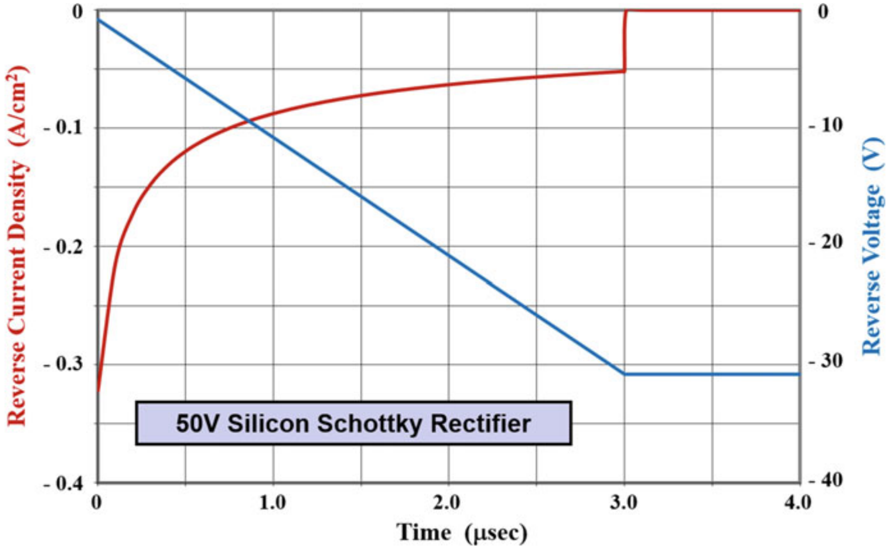

Fig. 4.31 Reverse recovery waveforms for Schottky barrier rectifiers

pre-breakdown avalanche multiplication must be taken into consideration when analyzing the leakage current for silicon devices because they can enhance the leakage current by an order of magnitude for high reverse bias voltages. In the case of silicon carbide Schottky rectifiers, it is possible to extend the breakdown voltage to at least 3000 V due to the much smaller resistance in the drift region. However, the reverse leakage current in silicon carbide devices is significantly enhanced by the tunneling current at high reverse bias voltages.

The leakage current in silicon and silicon carbide Schottky rectifiers can be suppressed by using the junction-barrier controlled Schottky (JBS) rectifier structure [1–3]. A detailed analysis of these structures is beyond the scope of this textbook due to space limitations. In addition, the performance of silicon Schottky rectifiers has been greatly improved by using the Trench MOS Barrier Schottky (TMBS) charge-coupling concept. The JBS and TMBS structures are discussed in detail in other recently published books [20, 21].

Problems

4.1 Calculate the barrier height for a Schottky contact to silicon made using a metal with a work function of 4.6 eV.

4.2 Calculate the specific resistance for the ideal drift region for a silicon Schottky barrier rectifier designed to block 100 V.

4.3 Calculate the on-state voltage drop for a Silicon Schottky barrier rectifier designed to block 100 V under the following assumptions: (a) parallel-plane breakdown voltage, (b) on-state current density of 100 A/cm^2, (c) barrier height of 0.8 eV, (d) operation at room temperature (300 °K), and (e) zero

substrate and ohmic contact resistance. Provide the voltage drop across the Schottky barrier and the drift region.

4.4 Calculate the specific resistance for the ideal drift region for a silicon Schottky barrier rectifier designed to block 1000 V.

4.5 Calculate the on-state voltage drop for a silicon Schottky barrier rectifier designed to block 1000 V under the following assumptions: (a) parallel-plane breakdown voltage, (b) on-state current density of 100 A/cm^2, (c) barrier height of 0.8 eV, (d) operation at room temperature (300 °K), and (e) zero substrate and ohmic contact resistance. Provide the voltage drop across the Schottky barrier and the drift region.

4.6 Calculate the specific resistance for the ideal drift region for a 4H-SiC Schottky barrier rectifier designed to block 1000 V.

4.7 Calculate the on-state voltage drop for a 4H-SiC Schottky barrier rectifier designed to block 1000 V under the following assumptions: (a) parallel-plane breakdown voltage, (b) on-state current density of 100 A/cm^2, (c) barrier height of 1.1 eV, (d) operation at room temperature (300 °K), and (e) zero substrate and ohmic contact resistance. Provide the voltage drop across the Schottky barrier and the drift region.

4.8 A Silicon Schottky barrier rectifier is designed to block 100 V.

(a) Calculate the leakage current density without Schottky barrier lowering.
(b) Calculate the leakage current density with Schottky barrier lowering.
(c) What is the barrier reduction in eV due to the image force?

Use the following assumptions: (a) parallel-plane breakdown voltage, (b) reverse bias voltage of 80 V, (c) barrier height of 0.8 eV, (d) no impact ionization, and (e) no generation or diffusion current.

4.9 A 4H-SiC Schottky barrier rectifier is designed to block 1000 V.

(a) Calculate the leakage current density without Schottky barrier lowering and tunneling.
(b) Calculate the leakage current density with Schottky barrier lowering but without tunneling.
(c) Calculate the leakage current density with Schottky barrier lowering and tunneling.
(d) What is the barrier reduction in eV due to the image force?

Use the following assumptions: (a) parallel-plane breakdown voltage, (b) reverse bias voltage of 800 V, (c) barrier height of 1.1 eV, (d) no impact ionization, and (e) no generation or diffusion current.

4.10 Calculate the specific capacitance for a silicon Schottky barrier rectifier designed to block 100 V at reverse bias voltages of 10, 20, 40, and 80 V.

4.11 Calculate the specific capacitance for a 4H-SiC Schottky barrier rectifier designed to block 1000 V at reverse bias voltages of 100, 200, 400, and 800 V.

4.12 Calculate the power dissipation for a silicon Schottky barrier rectifier designed to block 100 V at 300, 350, 400, 450, and 500 °K. Use the following assumptions: (a) parallel-plane breakdown voltage, (b) reverse bias voltage

of 80 V, (c) barrier height of 0.8 eV, (d) duty cycle of 50%, and (e) on-state current density of 100 A/cm^2. Estimate the temperature at which minimum power dissipation is observed.

References

1. Baliga BJ, “Schottky barrier rectifiers and methods of forming the same”, U.S. Patent 5,612,567, 18 Mar 1997
2. Baliga BJ (2001) The future of power semiconductor technology. Proc IEEE 89:822–832
3. Baliga BJ (2005) Silicon carbide power devices. World Scientific Publishing Company, Singapore
4. Baliga BJ (1994) Power semiconductor devices for variable frequency drives. Proc IEEE 82:1112–1122
5. Crowell CR, Sze SM (1966) Current transport in metal-semiconductor barriers. Solid State Electron 9:1035–1048
6. Sze SM (1981) Physics of semiconductor devices, 2nd edn. Wiley, New York, pp 254–258
7. Bethe HA (1942) Theory of the boundary layer of crystal rectifiers. MIT Radiat Lab Rep 43:12
8. Sze SM (1981) Physics of semiconductor devices, 2nd edn. Wiley, New York, pp 265–270
9. Rhoderick EH, Williams RH (1988) Metal-semiconductor contacts, 2nd edn. Science Publications, Oxford, pp 35–38
10. Tu SL, Baliga BJ (1992) On the reverse blocking characteristics of Schottky power diodes. IEEE Trans Electron Devices 39:2813–2814
11. Bhatnagar M, McLarty PK, Baliga BJ (1992) Silicon carbide high voltage (400V) Schottky barrier diodes. IEEE Electron Device Lett 13:501–503
12. Dahlquist F et al (2000) A 2.8kV, forward drop JBS diode with low leakage. Silicon Carbide and Related Materials – 1999, Material Science Forum 338–342:1179–1182
13. Sugawara Y, Asano K, Saito R (2000) 3.6kV 4H-SiC JBS diodes with Low Ron. Silicon Carbide and Related Materials – 1999, Material Science Forum 338–342:1183–1186
14. Hatakeyama T, Shinohe T (2002) Reverse characteristics of a 4H-SiC Schottky barrier diode. Silicon Carbide and Related Materials – 2001, Material Science Forum 389–393:1169–1172
15. Baliga BJ (1984) The pinch-rectifier: a low forward drop, high speed power diode. IEEE Electron Device Lett EDL-5:194–196
16. Page DJ (1972) Theoretical performance of the Schottky barrier power rectifier. Solid State Electron 15:505–515
17. Rhoderick EH, Williams RH (1988) Metal-semiconductor contacts, 2nd edn. Science Publications, Oxford, pp 48–55
18. Shannon JM (1974) Reducing the effective height of a Schottky barrier using low energy ion implantation. Appl Phys Lett 24:369–371
19. Ashok S, Baliga BJ (1984) Effect of antimony ion implantation on Al-Silicon Schottky diode characteristics. J Appl Phys 56:1237–1239
20. Baliga BJ (2009) Advanced power rectifier concepts. Springer-Science, New York
21. Baliga BJ (2017) Gallium nitride and silicon carbide power devices. World Scientific Publishers, Singapore