Chapter 7
Spin-Based Majority Computation

Odysseas Zografos, Adrien Vaysset, Bart Sorée, and Praveen Raghavan

7.1 Introduction

The exploration and study of novel non-charge-based logic devices has been a main research focus in the past decade [1]. The purpose is to identify concepts that can extend the semiconductor industry roadmap beyond the complementary metal oxide semiconductor (CMOS) technology [1]. Since CMOS scaling, dictated by Moore's Law [2], will reach its limits in the following decade [3], there is a need for logic components that can operate at high frequencies, be extremely compact, and also consume ultralow power [4]. A variety of magnetic devices have been benchmarked as promising candidates for low-power applications [4–8].

The goal of this chapter is to introduce, analyze, and discuss two spin-based logic concepts that utilize majority-based computation. Namely, the Spin Wave Device (SWD) and Spin Torque Majority Gate (STMG) concepts, which were first proposed by Khitun et al. in [9] and Nikonov et al. in [6] respectively. This section introduces some terms and concepts which are useful for establishing the framework of this chapter. More specifically, Sect. 7.1.1 introduces basic physics terminology. Important spin-based logic concepts, different from SWD and STMG, are described in Sect. 7.1.2. Finally, Sect. 7.1.3 introduces majority-based logic, which is used extensively by SWD and STMG logic as elaborated in Sects. 7.2 and 7.3.

O. Zografos (✉) · A. Vaysset · P. Raghavan
imec, Leuven, Belgium
e-mail: odysseas.zografos@imec.be

B. Sorée
KU Leuven, ESAT, Leuven, Belgium
imec, Leuven, Belgium
Universiteit Antwerpen, Physics Department, Condensed Matter Theory, Antwerpen, Belgium

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7.1.1 Spin and Magnetism Basics

In this part, we will introduce the most important physics terms required to understand the rest of the chapter. This introduction is by no means exhaustive and we invite the interested reader to look for further information and insight at the referenced manuscripts.

7.1.1.1 From Angular Momentum to Ferromagnetism

The angular momentum ($\mathbf{L}$) of a particle is generally defined as the cross-product of the particle's position ($\mathbf{r}$) and momentum ($\mathbf{p}$) [10]:

$$\mathbf{L} = \mathbf{r} \times \mathbf{p}, \tag{7.1}$$

where $\mathbf{p} = m\mathbf{v}$ is the linear momentum of the particle. When the particle carries a charge q and is flowing in a circular loop with radius R and area $A = \pi R^2$, carrying a current $I = qv/2\pi R$ where v is the velocity of the charged particle, the magnitude of the orbital angular momentum $|\mathbf{L}| = mvR$, while the associated magnetic moment is

$$\boldsymbol{\mu}_{\mathrm{L}} = IA\mathbf{e}_n = \frac{qv}{2\pi R}\pi R^2\mathbf{e}_n = \frac{qvR}{2}\mathbf{e}_n = \frac{q}{2m}\mathbf{L} = \gamma_{\mathrm{L}}\mathbf{L}, \tag{7.2}$$

where $\gamma_{\mathrm{L}} = q/2m$ is the gyromagnetic ratio.

In classical mechanics, a rigid object admits two kinds of angular momentum: *orbital* (see Eq. (7.1)), associated with the motion of the center of mass, and *spin*, associated with motion about the center of mass [10]. Similarly, in quantum mechanics there is also another kind (other than the orbital) of angular momentum occurring called spin angular momentum [11]. However, the spin angular momentum of a particle cannot be decomposed into orbital angular momenta of constituent parts [10] and should not be pictured as due to some internal motion of the particle. In that sense the description of a particle's spin angular momentum is completely different from the one of a rigid object (in classical mechanics) and hence it is considered a purely quantum mechanical phenomenon.

As a quantum mechanical entity, the spin of a particle is described by a set of complete Hermitian operators corresponding to the magnitude of the spin $\hat{S}$ and one component of the spin vector conventionally along the z-direction, that is, $\hat{S}_z$. The spin state is then completely described by a state vector $|sm_s\rangle$ being the eigenstate of the aforementioned Hermitian operators, that is

$$\hat{S}^2|sm_s\rangle = \hbar^2 s(s+1)|sm_s\rangle \tag{7.3}$$

$$\hat{S}_z|sm_s\rangle = \hbar m_s|sm_s\rangle, \tag{7.4}$$

where the eigenvalue s assumes an integer value for Bosons and half integer number for Fermions, while the eigenvalue can assume the following values $m_s = -s, -s+1, \ldots, s-1, s$ (e.g., for electrons $s = 1/2$, $m_s = +1/2, -1/2$). The eigenvalues s and m_s are the possible quantized outcomes of a measurement with a probability given by the modulus squared of the corresponding amplitudes. For a spin $1/2$ system, if the spin state is given by

$$|\Psi\rangle = \alpha|1/2, 1/2\rangle + \beta|1/2, -1/2\rangle, \tag{7.5}$$

where $|\alpha|^2 + |\beta|^2 = 1$ due to normalization, the probability of measuring the spin $s = 1/2$ with spin along the $+z$-direction (spin-up), that is, $S_z = \hbar/2$, is given by $|\alpha|^2$, while for spin down, that is, $S_z = -\hbar/2$, the corresponding probability is $|\beta|^2$.

According to Pauli's exclusion principle [12], no two fermions in an atom can have all their quantum numbers equal [13]. This means that in order for two electrons to fill the same orbital in an atom they have to have opposite spins (one will occupy the quantum state of spin-up and the other of spin down).

A charged particle with spin angular momentum constitutes a *magnetic dipole* [10], meaning that an electron acts also as a tiny magnet. The magnetic dipole moment associated with spin, $\boldsymbol{\mu}_{\mathrm{S}}$ is proportional to its spin angular momentum $\mathbf{S}$. The proportionality is defined by a constant called **gyromagnetic ratio** γ_{S} [14], that is

$$\boldsymbol{\mu}_{\mathrm{S}} = \gamma_{\mathrm{S}}\mathbf{S}. \tag{7.6}$$

Both the intrinsic spin as well as the orbital angular momentum will contribute to the total magnetic moment of an electron. The total angular momentum $\mathbf{J} = \mathbf{L} + \mathbf{S}$ is related to the total magnetic moment $\boldsymbol{\mu}$ as follows:

$$\boldsymbol{\mu} = \gamma\mathbf{J}. \tag{7.7}$$

where γ is the gyromagnetic ratio relating the total magnetic moment and total angular momentum. Two magnetic dipoles can interact in two different ways: by exchange interaction, when the dipoles are close together or by dipole–dipole interaction (i.e., dipolar coupling), when the dipoles are far from each other. The exchange interaction arises from the overlap of the two particles' wave functions combined with the Coulomb interaction and the Pauli exclusion principle. If these two particles are at a fixed close distance then the interaction tends to change their spin eigenstates so that they either have the same or parallel orientation (both spin-up or spin down) or an opposite or antiparallel orientation. On the other hand, dipolar coupling tends to align spins of far-away magnetic moments in an antiparallel fashion. The competition between the long-range dipolar interaction and the short-range exchange interaction gives rise to magnetic configurations that strongly depend on the size of the magnet. For submicron sizes, exchange interaction dominates, which leads to uniform magnetization distribution at equilibrium. For larger magnets, the dipolar interaction favors multidomain states.

Table 7.1 Ferromagnetic crystals [13]

Substance	Curie temperature in K
Fe	1043
Co	1388
Ni	627
Gd	292
Dy	88
MnAs	318
CrO_2	386
EuO	69
$Y_3Fe_5O_{12}$	560

Ferromagnetism is the basic mechanism by which certain materials (see Table 7.1) form permanent magnets due to the aforementioned exchange interaction, which means that they can be magnetized in the absence of an external magnetic field. Ferromagnetism involves the magnetic dipoles associated with the spins of unpaired electrons [10] (electrons that partially fill the outer shell of the atoms). The magnetic dipoles of neighboring atoms interact via exchange interaction and are strongly aligned to the same orientation. So ferromagnetism is one of the macroscopic expressions of the quantum mechanical spin and exchange phenomena. Other possible long-range magnetic ordering driven by the exchange interaction are antiferromagnetism and ferrimagnetism which are not considered here as they are out of scope and for the purpose of this chapter we will refrain for elaborating furthermore. The reader is encouraged to look into [14] and [15] for more insights.

Ferromagnetism is found in the binary and ternary alloys of Fe, Co, and Ni with one another, in alloys of Fe, Co, and Ni with other elements, and in a relatively few alloys which do not contain any ferromagnetic elements [15]. Table 7.1 enumerates a few examples of known ferromagnetic materials, along with their Curie temperature.[1]

A phenomenon occurring to ferromagnetic materials, which is important for the introduction of this chapter, is magnetostriction. Magnetostriction is the phenomenon whereby the shape of a ferromagnetic specimen changes during the process of magnetization [16]. In other words, the dimensions and magnetic properties of magnetostrictive materials are intertwined. This class of materials is significant to any spin-based technology and their integrated application because in combination with piezoelectric materials they offer a way of voltage-induced magnetic control. Table 7.2 enumerates a few examples of magnetostrictive materials along with their respective magnetostriction constants.[2]

[1] Curie temperature of a ferromagnetic material is the temperature over which the material loses its magnetic ordering [14].

[2] Magnetostriction constants define how much the material deforms [16].

Table 7.2 Magnetostrictive ferrites [16]

Substance	λ_{100}	λ_{111}
$MnFe_2O_4$	−31	6.5
Fe_3O_4	−20	78
$Co_{0.8}Fe_{2.2}O_4$	−590	120
$NiFe_2O_4$	−42	−14
$CuFe_2O_4$	−57.5	4.7
$MgFe_2O_4$	−10.5	1.7

7.1.1.2 Magnetization Dynamics and the Landau–Lifshitz–Gilbert Equation

A magnetic moment $\boldsymbol{\mu}$ subjected to an effective magnetic induction field $\mathbf{B}_{\text{eff}}$ experiences a torque $\boldsymbol{\tau} = \boldsymbol{\mu} \times \mathbf{B}_{\text{eff}}$. Due to $\boldsymbol{\mu} = \gamma \mathbf{J}$, where γ is the gyromagnetic ratio, the equation of motion for the magnetic moment is

$$\frac{d\mathbf{J}}{dt} = \boldsymbol{\tau} = \boldsymbol{\mu} \times \mathbf{B}_{\text{eff}} \Rightarrow \frac{d\boldsymbol{\mu}}{dt} = \gamma \boldsymbol{\mu} \times \mathbf{B}_{\text{eff}}. \tag{7.8}$$

When the magnetic moment $\boldsymbol{\mu}$ is at an angle φ with the effective magnetic induction field $\mathbf{B}_{\text{eff}}$, it will make a precessional motion around the $\mathbf{B}_{\text{eff}}$ field vector. The effective magnetic induction field accounts for all external applied fields as well as internal fields due to exchange and anisotropy and is related to the magnetic field by $\mathbf{B}_{\text{eff}} = \mu_0 \mathbf{H}_{\text{eff}}$. The magnetization or magnetic moment per unit volume of a magnetic material is given by $\mathbf{M} = N\boldsymbol{\mu}$ where N is the number of magnetic moments per unit volume. As a result, the equation of motion for the magnetization is

$$\frac{d\mathbf{M}}{dt} = -\gamma \mu_0 \mathbf{M} \times \mathbf{H}_{\text{eff}}. \tag{7.9}$$

This equation is known as the dampless Landau equation for the magnetization and does not take into account the presence of damping processes that occur in real magnetic materials. In order to account for such damping, an additional phenomenological term is added to the equation of motion which tends to pull the magnetization in the direction of the effective magnetic field:

$$\frac{d\mathbf{M}}{dt} = -\gamma \mu_0 \mathbf{M} \times \mathbf{H}_{\text{eff}} + \frac{\alpha}{M_s} \times \left(\mathbf{M} \times \frac{d\mathbf{M}}{dt} \right). \tag{7.10}$$

This equation is known as the Landau–Lifshitz–Gilbert equation. The strength of the damping is quantified by the damping parameter α and M_s is the saturation magnetization.

7.1.1.3 Anisotropy

Crystal symmetries can induce preferred magnetization directions. This phenomenon is called *magnetocrystalline anisotropy*, and the preferred directions are referred to as *easy axes*. In the common case of uniaxial anisotropy, the magnetization tends to align along one particular axis. The anisotropy energy is then expressed as

$$E_{\text{anis}} = K_u V \sin^2 \theta, \tag{7.11}$$

where K_u is the anisotropy constant in J/m^3 and θ is angle between the magnetization and the easy axis.

Magnetocrystalline anisotropy is a bulk effect. However, in thin films, some interface effects can dominate over bulk. For example, the interfaces MgO–CoFeB and Co–Ni induce a perpendicular anisotropy. The energy of this interface anisotropy is expressed as

$$E_{\text{anis}} = \frac{K_s}{t} V \left(1 - \cos^2 \theta\right), \tag{7.12}$$

where K_s is the surface anisotropy coefficient in J/m^2, t is the thickness, and θ is the out-of-plane angle.

In thin films, the aforementioned dipolar interaction favors in-plane magnetization. It is therefore opposite to the interface anisotropy. As a consequence, an effective anisotropy coefficient can be expressed as

$$K_{\text{eff}} = \frac{K_s}{t} - \frac{1}{2}\mu_0 M_s^2. \tag{7.13}$$

At equilibrium, the magnetization is perpendicular to the plane if $K_{\text{eff}} > 0$ (out-of-plane easy axis) and in-plane if $K_{\text{eff}} < 0$ (in-plane easy axis).

7.1.1.4 Spin Transfer Torque

The Spin Transfer Torque (STT) [17] is the effect induced by a spin polarized current on the magnetization. The spin polarization is created by a thick ferromagnetic layer called *polarizer*, or *reference layer*. The torque is exerted on the magnetization of the *free layer*, bringing it along the direction of the spin polarization. In simulations, the spin torque is modeled as an additional term in the Landau–Lifshitz–Gilbert equation (7.10).

In a Magnetic Tunnel Junction (MTJ), a thin oxide layer is sandwiched between the free layer and the polarizer. The tunneling of the current through the oxide barrier is spin-dependent [18], leading to enhanced spin torque efficiency, in particular for coherent tunneling through crystallized MgO barrier [19–21].

7.1.1.5 Tunnel Magnetoresistance

The magnetic state of the free layer can be detected via Tunnel Magnetoresistance (TMR). If the free layer magnetization is parallel to the magnetization of the reference layer, a low-resistance state is detected. In contrast, antiparallel alignment leads to a high-resistance state. The TMR ratio is defined as

$$\mathrm{TMR} = \frac{R_{\mathrm{AP}} - R_{\mathrm{P}}}{R_{\mathrm{P}}}, \tag{7.14}$$

where R_{P} and R_{AP} are the resistances of the parallel and antiparallel states.

7.1.2 Spin-Based Logic Concepts

As shown in [5] and [4], there exists a variety of novel spin-based devices and components. Three of the most important concepts, as potential IC applications, are presented here below.

7.1.2.1 SpinFET

The SpinFET was first proposed by Datta and Das in [22]. It consists of a quasi-one-dimensional semiconductor channel with ferromagnetic source and drain contacts Fig. 7.1a. The concept makes use of the Rashba spin–orbit interaction [23], where spin polarized electrons are injected from the source to the channel and then detected at the drain. The electron transmission probability depends on the relative alignment of its spin with the fixed magnetization of the drain. This alignment is controlled by the gate voltage and the induced Rashba interaction, meaning that also the source–drain current is controlled. This first proposal had several impediments toward experimental demonstration, such as low spin-injection efficiency due to resistance mismatch [24], spin relaxation and the spread of spin precession angles, which resulted in alternative proposals such as [25] (see Fig. 7.1b, c). Recently, Chuang et al. in [26] have shown experimentally an all-electric and all-semiconductor spin field-effect transistor in which aforementioned obstacles are overcome by using two quantum point contacts as spin injectors and detectors.

7.1.2.2 Nanomagnetic Logic

Among the most prominent concepts investigated for beyond-CMOS applications is the NanoMagnetic Logic (NML) (also known as Magnetic Quantum Cellular Automata) that was first introduced by Cowburn et al. [27] and Csaba et al. [28]. In NML, the information is encoded in the perpendicular magnetization (along

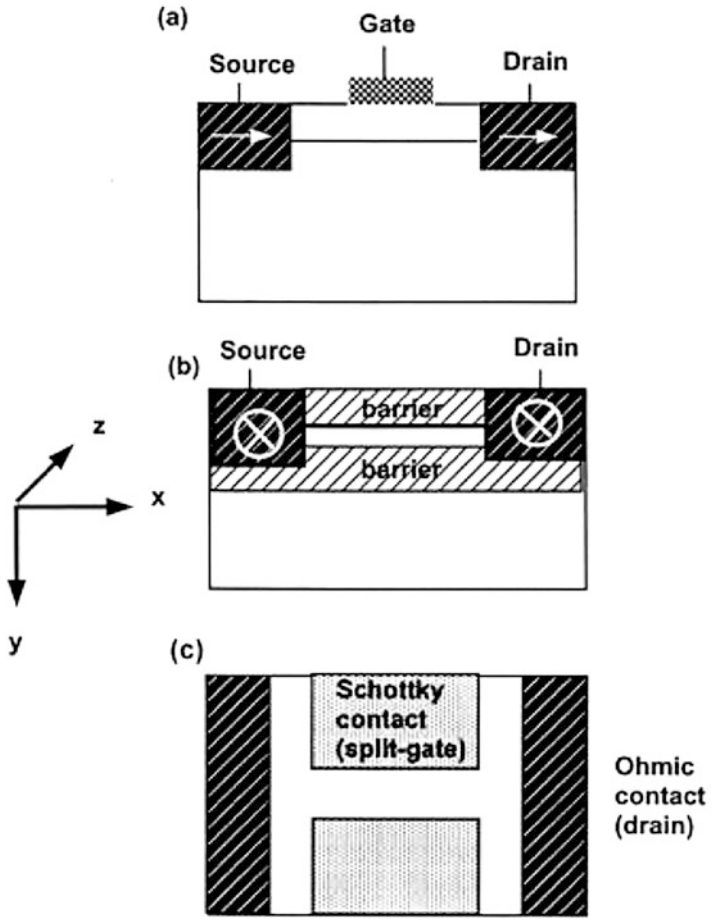

Fig. 7.1 Schematic of the spintronic modulator of [22]. (**b**) Side view of the spintronic modulator proposed in [25]. (**c**) Top view showing the split gates [25]

$+\hat{\mathbf{z}}$ or $-\hat{\mathbf{z}}$) of ferromagnetic dots. The computation is mediated through dipolar coupling between nanomagnets. Although NML devices can be beneficial in terms of power consumption and non-volatility [4], they have an operating frequency limited to about 3 MHz and an area around 200 nm $\times$ 200 nm [29], limitations which are imposed by the nanomagnet material properties. However, a functional 1-bit full adder based on NML majority gates has been shown experimentally in [29] and a schematic is depicted in Fig. 7.2.

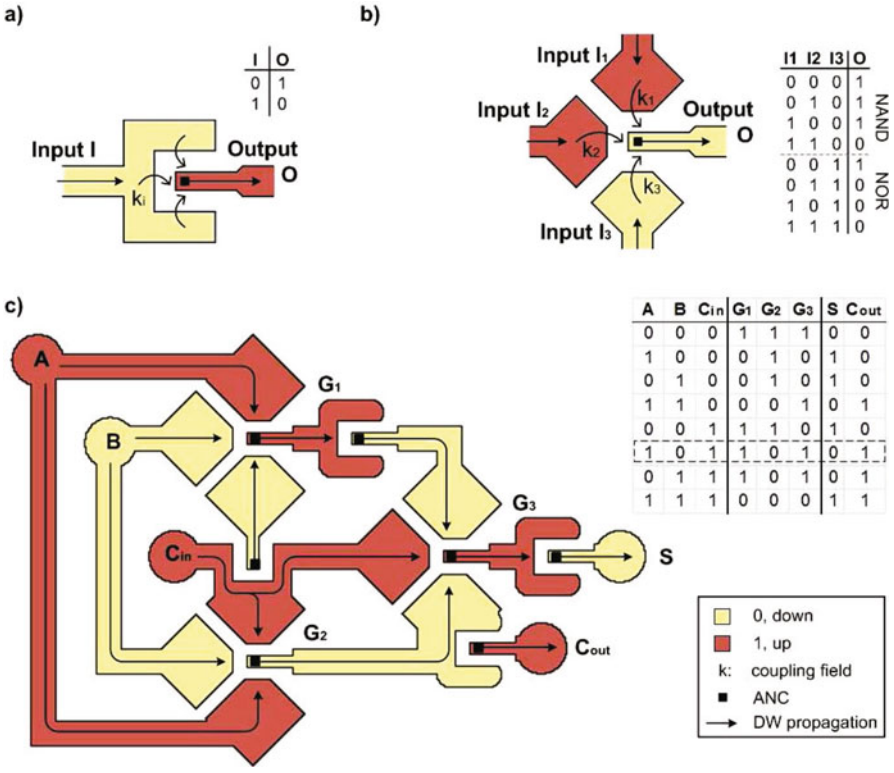

Fig. 7.2 Inverter (**a**) and majority gate (**b**) as basic building blocks for perpendicular NML. A 1-bit full adder (**c**) with inputs A, B and carry-in C_{in} and outputs sum S and carry-out C_{out} is realized by three majority gates and four inverter structures connected by wires [29]

7.1.2.3 All-Spin Logic

Proposed by Behin-Aein et al. in [30] as a logic device with built-in memory, All-Spin Logic (ASL) is a concept that combines magnetization states of nanomagnets and spin injection through spin-coherent channels. A schematic of the device is shown in Fig. 7.3. The input logic bit controls the state of the corresponding output logic bit with the energy coming from an independent source. Information is stored in the bistable states of magnets. Corresponding inputs and outputs communicate with each other via spin currents through a spin-coherent channel, and the state of the magnets is determined by the spin-torque phenomenon. The aforementioned challenges of SpinFET and NML are also present in the ASL concept. Existing nanomagnet material properties and spin-transfer channel properties fall short of the energy and delay targets [31] dictated by modern advanced CMOS devices [32].

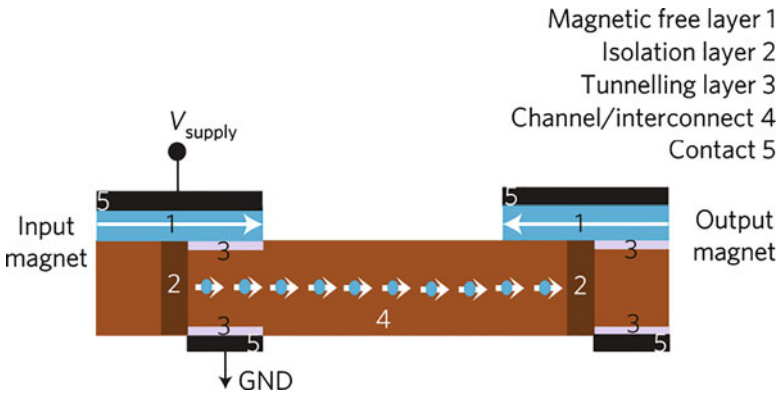

Fig. 7.3 Schematic of the all-spin logic device [30]

However, a scaling path of ASL material targets has been outlined in [31] which if achieved can enable radical improvements in computing throughput and energy efficiency.

7.1.3 Majority Logic Synthesis

New logic synthesis methods are required to both evaluate emerging technologies and to achieve the best results in terms of area, power, and performance [33]. Majority gates enhance logic power of a design since they can emulate both AND and OR operation and are one of the basis for basic operation of binary arithmetic [34]. In order to build complete circuits composed from MAJ gates, we need to employ specific synthesis methodologies. In the results shown in this chapter, the principle of synthesis is based on Majority-Inverter Graph (MIG) [35]. A novel logic representation structure for efficient optimization of Boolean functions, consisting of three-input majority nodes and regular/complemented edges. This means that only two logic components are required for this representation, a MAJ gate and inverter (INV). In this way, it's possible to reduce the total chip area by utilizing functional scaling [36]. Meaning that instead of scaling down single gates and devices, these single blocks gain functionality.

Also, MIG has proven to be an efficient synthesis methodology for CMOS design optimization [35] and can be further exploited for SWD technology, as shown in [37]. Other novel synthesis tools for majority logic exist, such as [38] but it's specific to a certain technology (QCA), while MIG representation and optimization that is technology-agnostic can be straightforwardly used to evaluate circuit perspectives for any majority-based technology.

7.2 Spin Wave Device Circuits

Introduced in 2011 [9], a Spin Wave Device (SWD) is a concept logic device that is based on the propagation and interference of spin waves in a ferromagnetic medium. As a concept that employs wave computing, a SWD circuit consists of (a) wave generators; (b) propagation buses; and (c) wave detectors. One of the most compelling properties of SWDs is the potential of using the same voltage-controlled element for spin wave generation and detection, called Magnetoelectric (ME) Cell. Both spin waves and ME cells are described in Sect. 7.2.1. An overview of experimental results, that can lead to the complete implementation of the SWD circuit concept, is given in Sect. 7.2.2. The potential benefits of such SWD circuits are presented and discussed in Sects. 7.2.3 and 7.2.4.

7.2.1 Concept Definition

7.2.1.1 Spin Waves

Spin waves are usually known as the low-energy dynamic eigen-excitations of a magnetic system [39]. The spin-wave quasi-particle, the magnon, is a boson which carries a quantum of energy $\hbar\omega$ and possesses a spin $\hbar$. Incoherent thermal magnons exist in any magnetically ordered system with a temperature above absolute zero. Here, in the context of spin wave devices the spin waves are rather classical wave excitations of the macroscopic magnetization in a magnetized ferromagnet. In the context of spin-based applications (like SWD), thus, the main interest is not in thermal excitations, but externally excited spin-wave signals: coherent magnetization waves which propagate in ferromagnets over distances which are large in comparison with their characteristic wavelength [40].

Spin wave propagation depends on the nonlinear dispersion relation of the excitation $\omega(k)$, which is strongly affected by the dimensions and geometry of the magnetic medium [40]. This dispersion can be characterized into three distinct regimes, depending on which spin interaction mechanism dominates (dipolar or exchange). These regimes are the magnetostatic (dipolar-dominated) regime [41], exchange regime [42], and an intermediate regime of dipole-exchange waves, where excitations are affected by both contributions [43].

As wave entities, spin waves (or magnons) have a specific wavelength and amplitude. The SWD concept exploits the interference of spin waves, where the logic information is encoded in one of the spin wave properties and two or more waves are combined into an interfered result. Consider two waves Ψ_A and Ψ_B with the same frequency and amplitude and a certain phase shift ϕ relative to each other. Interference of these two waves can be elaborated as follows:

$$\Psi_{\text{tot}}(\mathbf{r}, t) = \Psi_A + \Psi_B = A \cdot e^{i(\mathbf{kr}-\omega t)} + B \cdot e^{i(\mathbf{kr}-\omega t+\phi)}. \tag{7.15}$$

If we assume that the two waves have equal amplitude ($A = B$):

$$\text{for } \phi = 0: \qquad \Psi_{\text{tot}}(\mathbf{r}, t) = 2A \cdot e^{i(\mathbf{kr} - \omega t)} \tag{7.16a}$$

$$\text{for } \phi = \pi: \qquad \Psi_{\text{tot}}(\mathbf{r}, t) = 0 \tag{7.16b}$$

Equation (7.16) show that in a spin wave concept we can define a logic '0' as a spin wave with phase $\phi = 0$ and a logic '1' as a spin wave with phase $\phi = \pi$. This choice is arbitrary but serves as an example of how spin wave (or wave, in general) interference can be used in a logic application, with the information being encoded into the phase of the waves.

7.2.1.2 Magnetoelectric Cell

Aside from the propagation of spin waves, in order for the SWD concept to be integrated as an IC technology, there has to be a way to generate and detect spin waves that is amenable to scaling and is preferably voltage-driven [4]. One of the most prominent concepts that seem to satisfy the above criteria is the Magnetoelectric (ME) cell [44].

The magnetoelectric effect has been studied [45] and applied in several concepts as an interface between the electric and the spin domains [8, 9, 44]. An example of an ME cell is shown in Fig. 7.4. It usually consists of a stack with a magnetostrictive layer at the bottom, a piezoelectric layer above it, and a metal contact on top. When voltage is applied across the stack, the piezoelectric layer is strained and the strain is transferred to the magnetostrictive layer, which modifies its magnetic anisotropy. By modifying the anisotropy, the easy axis goes from out-of-plane to in-plane, which rotates the magnetization and a spin wave is generated and can be propagated through adjacent spin waveguide (stripe of ferromagnetic material). The spin wave detection exploits the inverse phenomenon.

Bistable Magnetization

Basic spin wave generation and detection can be achieved by the aforementioned magnetostrictive/piezoelectric interaction. However, in order to enable SWDs as a complete logic concept, the generators and detectors used need to offer information-

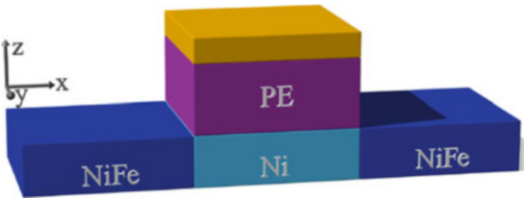

Fig. 7.4 Schematic view of ME cell stack connected to spin wave ferromagnetic bus [46]

encoding controllability. This means that it should be possible to controllably generate/detect spin waves with phase $\phi = 0$ or $\phi = \pi$. To realize this feature, the ME stacks proposed [8, 44] always include a magnetostrictive material with two stable magnetization states. Each magnetization state is associated with one of the spin wave phases (and also with a logic '0' or '1'). With a bistable magnetization, when a specific (e.g., positive) voltage is applied on the ME cell the magnetostrictive layer's magnetization switches on the associated state (e.g., '0') which generates a spin wave with the equivalent phase (e.g., $\phi = 0$). When an opposite voltage is applied (e.g., negative), then magnetostrictive layer's state will become '1' and a spin wave with phase $\phi = \pi$ will be generated. Hence, bistable magnetization is required to enable the controllable operation of information-encoded spin waves and ME cells. Two options have been proposed for the implementation of bistable magnetization of the magnetostrictive layer each coming with their inherited advantages and disadvantages.

In [9, 37, 46, 47] the bistability of the ME cell magnetization was assumed to be in canted magnetization states, as shown in Fig. 7.5a. Since the two stable states are separated by a relatively small angle (from $\theta_{\text{me}} \simeq 1°$ [9] to $\theta_{\text{me}} \simeq 5°$ [48]), energy required to switch between these states is also small leading to an ultralow-power device [48]. On the other hand, the small state separation indicates that this configuration will be very sensitive to thermal noise.

In [8], the bistability of the ME cell was implemented in in-plane magnetization ($\pm\hat{x}$—Fig. 7.5b). The magnetostrictive layer of the ME cell has two low-energy stable in-plane magnetization states along the $\pm\hat{x}$ direction, favored by the shape anisotropy of the structure. In order for the magnetization to switch, it first has to be put in a meta-stable state (i.e., along $+\hat{z}$). Since this proposal employs two in-plane magnetization states which are well separated, the result is a thermally stable and nonvolatile ME cell. However, the ME cell operation becomes slightly more complicated (compared to the canted state ME cell) since putting the magnetization to the meta-stable state (along $+\hat{z}$) requires an extra "step" before spin wave generation or detection.

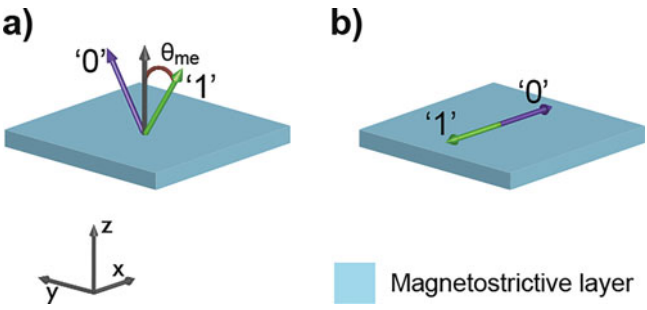

Fig. 7.5 Proposed bistability of the magnetostrictive layer. (**a**) Canted magnetization states as shown in [9] where θ_{me} is the canting angle between a stable magnetization state and $\hat{z}$. (**b**) In-plane bistable magnetization as proposed in [8]

Table 7.3 Overview of propagation characteristics of different spin wave regimes

Regime	Propagation length	Waveguide	Reference
Magnetostatic	6 mm	YIG	[49]
Magnetostatic	7 mm	YIG thin film	[50]
Dipole-exchange	5 μm	Py—2.5 μm wide	[51]
Dipole-exchange	10 μm	CoFeB—0.5 μm wide	[52]
Dipole-exchange	Up to 4 μm	Py—500 nm wide	[53]
Dipole-exchange	12 μm	Py—2.5 μm wide	[54]

7.2.2 Experimental Demonstrations

There has been no experimental proof for the complete SWD concept, containing all necessary parts of excitation, propagation, logic computation, and detection. However, these parts have been separately studied and experimentally shown. Here we give a brief overview of the most relevant experimental work done in spin waves, that is closely related to the realization of SWD circuits. As aforementioned in Sect. 7.2.1, spin waves can be observed in three different regimes, each having different propagation characteristics. Table 7.3 presents a comprehensive overview of these propagation characteristics shown in literature.

Magnetostatic spin waves can propagate for long distances but cannot be confined in nanometer scale structures due to their long wavelengths. Dipole-exchange spin waves have shorter wavelengths and thus can be more confined but also have much shorter propagation lengths. Spin waves in the exchange regime have the shortest wavelengths from the three regimes and that is why it is not possible yet to experimentally observe them.[3] However, the propagation lengths of either dipole-exchange or exchange spin waves do not guarantee signal integrity over more than several circuit stages [46]. This means that in a realistic SWD circuit concept spin wave amplification or regeneration has to be included to enable cascading of SWD gates.

As described in Sect. 7.2.1, ME cells can serve as a generator and a detector, which means they can be used for regeneration of spin waves to ensure propagation. Despite the importance of ME cells to the SWD concept and to spin-based technologies in general, to our knowledge the only experimental work showing spin waves generated by ME material was done by Cherepov et al. in 2014. Where voltage-induced strain-mediated generation and detection of propagating spin waves using multi-ferroic magnetoelectric cells was experimentally demonstrated by fabricating 5 μm wide Ni/NiFe waveguides on top of a piezoelectric substrate, Fig. 7.6.

Although the spin waves amplitudes measured in [55] are rather small, the fact that the ME cell functionality was experimentally proven is significant. However,

[3]Either with an optical measurement setup or with an electrical one, the exchange spin waves would be lower than the resolution of a state-of-the-art measurement setup.

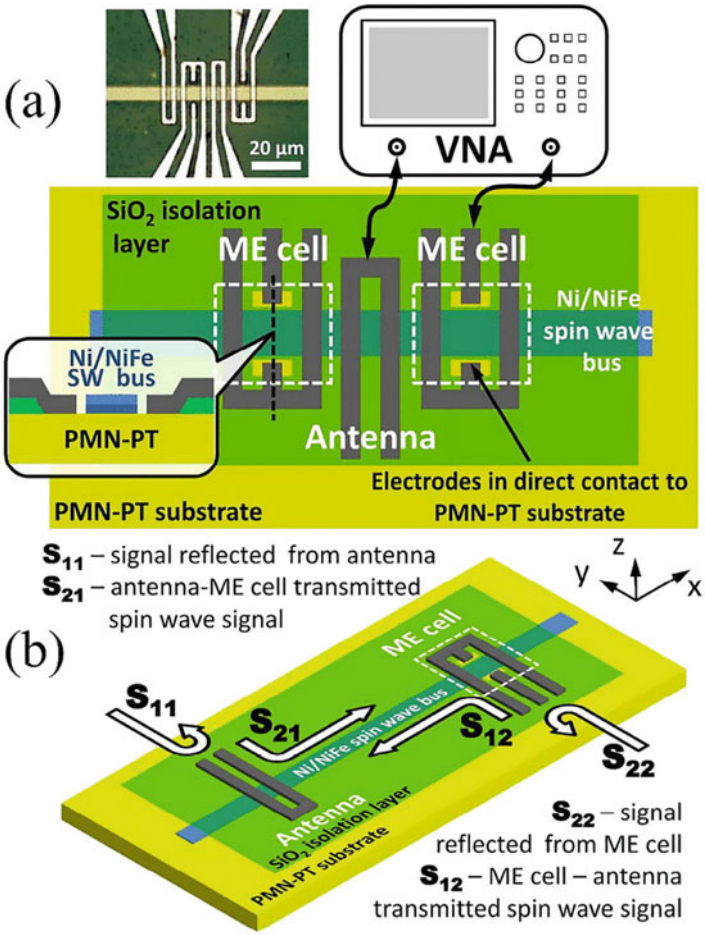

Fig. 7.6 (**a**) Schematic of the studied device: Spin wave generation and propagation measurements using a vector network analyzer were performed on the 5 μm wide Ni/NiFe bus lithographically defined on a PMN-PT piezoelectric substrate. Inset shows cross-sectional view of the ME cell. (**b**) The schematic of two-port measurements of transmission (S21 and S12) and reflection (S11 and S22) measurements between conventional loop antennas and voltage-driven magnetoelectric cells [55]

the cross section shown in Fig. 7.6a is quite different from the ME cell concept depicted in Fig. 7.4 which means that the ME cell field has to take major strides in order to reach a functional but also IC integrable stack.

The dynamic behavior and propagation is strongly dependent on the geometry of the spin wave structure. In the same way, spin wave interference behavior has a high geometry and material dependence. Several experimental and simulation studies have explored the behavior of spin wave interference [56–59] but are all in the order of microns. More specifically, the work presented in [57, 58] shows

simulation of two spin wave Majority gate structures, which can be realistically fabricated. Meaning that the spin waves are generated and detected by micron-sized antennas (or coplanar waveguides) and propagated in micron-sized ferromagnetic waveguides. The field of spin wave devices and spin wave majority gates includes a variety of simulation and experimental proof of concepts. In many publications [8, 9, 37, 44, 46, 47, 60], the feature sizes of the assumed and studied concepts are in the order of nanometers. However, the whole spin wave computation concept (meaning spin wave generation, propagation, and detection) has not yet been shown experimentally in these dimensions.

7.2.3 SWD Circuit Benchmarking

One important aspect of exploring novel technologies (especially non-charge-based) is the projection and evaluation of a complete logic circuit of each technology and how it compares with the current CMOS technology. This evaluation serves as a useful guideline toward how much effort should be put in and in which aspects of an emerging technology. Such evaluations and benchmarking have been presented in [4] and [5], and are based in several assumptions for each emerging technology. Obviously, studies like these cannot foresee the exact designs and layouts of all novel technologies but help in painting a picture of where each technology stands with respect to the others. The following section is a circuit evaluation of spin wave devices making use of the canted state ME cells [9, 47].

7.2.3.1 Assumptions

Since all experimental proof necessary for a complete nanometer-scaled SWD circuit do not exist yet, we need to consider several assumptions in order to evaluate the circuit benefits of SWD. These assumptions include the interface between the spin and electric domains, the geometry of SWD gates, and their cascadability. The block diagram, depicted in Fig. 7.7, provides a frame in which SWD can be integrated with CMOS devices in a realistic IC environment.

We assume that the spin wave domain of the block diagram shown in Fig. 7.7 consists of ME cell gates, presented in Fig. 7.8, and spin wave amplifiers [61]. However, since spin wave amplification is a complex issue, we will ignore the impact of amplifiers for the rest of this evaluation.

In Fig. 7.8a, we present the INV component which is a simple wave bus, with a magnetically pinned layer on top, that inverts the phase of the propagating signal. The MAJ gate (Fig. 7.8b) is the merging of three wave buses. For the gates presented in Fig. 7.8, we assume minimum propagation length equal to one wavelength of the spin wave which in our study is assumed at 48 nm, since the wavelength is defined/confined by the width of the spin wave bus. As aforementioned in

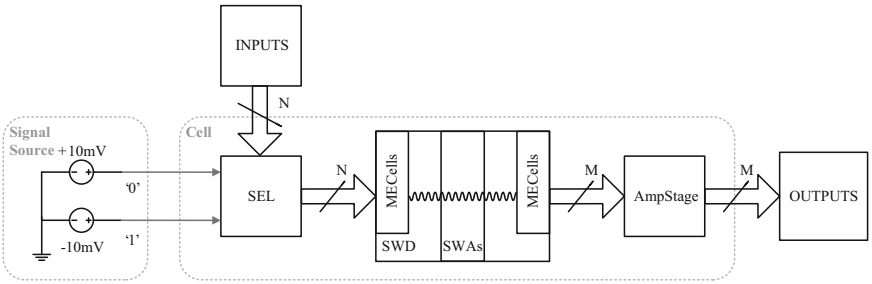

Fig. 7.7 Block Diagram that integrates SWD with CMOS and digital interfaces [47]

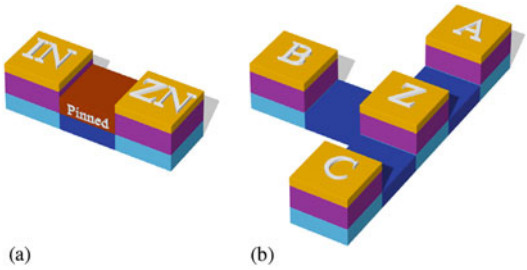

Fig. 7.8 Gate primitives used for SWD circuits. (**a**) INV. (**b**) MAJ

Sect. 7.1.3, with an inverter and a majority gate as the only primitive components, one can re-create any possible logic circuit that is traditionally (with CMOS technology) composed with NAND/NOR or other gates.

In [9, 47], the operational voltage levels of an ME cell were considered to be ± 10 mV. This was because the angle of the canted magnetization was assumed to be $\theta_{\text{me}} \simeq 1°$. However, in [48] a larger and more feasible canted magnetization was calculated and according to that study we assume that the operational voltage level of an ME cell is 119 mV. This means that the *minimum* energy needed to actuate an inverter or a majority operation (Fig. 7.8) is given by

$$E_{\text{INV}} = C_{\text{ME}} \cdot V_{\text{ME}}^2 = 14.4\,\text{aJ} \tag{7.17a}$$

$$E_{\text{MAJ}} = 3 \cdot C_{\text{ME}} \cdot V_{\text{ME}}^2 = 43.3\,\text{aJ}, \tag{7.17b}$$

where C_{ME} is assumed at 1 fF [48].

For this assumption of ME cell output voltage, the final output stage of the spin wave domain (Fig. 7.7) to the electric domain, a sense amplifier (SA) was designed and used in [48] to accommodate a peak-to-peak input signal of 119 mV with a yield above $1–10^{-5}$, assuming a Pelgrom constant $A_{\Delta \text{VT}} = 1.25\,\text{mV}\,\mu\text{m}$. The amplifier consists of two stages. The first stage consists of a PMOS differential pair, with one PMOS gate connected to the input signal and the other PMOS gate connected to a 0 mV reference voltage. This first stage operates in a pulsed mode: The current source is activated during only 3 ps. During this time, an amplified version of the

Table 7.4 Specifications of SWD circuit components, mostly from [48]

Component	Area (μm^2)	Delay (ns)	Energy (fJ)
INV	0.006912	0.42	1.44×10^{-2}
MAJ	0.03456	0.42	4.33×10^{-2}
SA	0.050688	0.03	2.7

input signal is developed on the output nodes of the first stage. The second stage is a drain-input latch-type SA that acts as a latch, amplifying the signals from the first stage to full logic levels. This signal is buffered by two minimal-size inverters to drive amplifier's outputs. Better options might be possible with calibration or offset compensation. The sensing circuitry and the core SWDs of the circuit are considered to be integrated side by side.

The specifications of the components (INV, MAJ, SA) described above are given in Table 7.4.

7.2.3.2 Benchmarks

The benchmarks used for the SWD circuit evaluation are selected from a set of relatively large combinational designs. All designs have been synthesized with MIG [35] for a straightforward mapping with the gate primitives shown in Fig. 7.8. The ten benchmarks selected are shown in Table 7.5. These benchmarks have varying input and output number of bits (I/O bits), which is critical in order to quantify the impact of the CMOS peripheral circuitry that enables digital I/O to the SWD circuits. The list includes three 64-bit adders (BKA264, HCA464, CSA464), three 32- and 64-bit multipliers (DTM32, WTM32, DTM64—Dadda tree and Wallace tree), a Galois-Field multiplier (GFMUL), a 32-bit MAC module (MAC32), a 32-bit divider (DIV32), and a cyclic redundancy check XOR tree (CRC32). All benchmarks (except DIV32 and CRC32) were generated using the *Arithmetic module generator* [62].

7.2.3.3 Circuit Estimations

The specifications in Table 7.4 are used to calculate the results presented in Table 7.6. It's important to note that in these results energy and power metrics of SWD are calculated including the interconnection capacitances for each benchmark. This means that contrary to [48], here a more **realistic** sum of capacitances is accounted to calculate the minimum energy and power consumption of the SWD circuits. To quantify the benefits of SWD circuits, the same benchmarks were executed using a state-of-the-art CMOS technology of 10 nm feature size (hereafter named N10) [63]. All N10 reference results are provided post-synthesis by *Synopsys Design Compiler*. Table 7.6 includes the area metric for both technologies, the energy calculated to be consumed in the SWD circuits, the delay metric, and the power consumption metric.

Table 7.5 Benchmark designs with I/O bits and MIG synthesis results ordered by size [48]

Codename	Input bits	Output bits	MIG size	MIG depth
CRC32	64	32	786	12
BKA264	128	65	1030	12
GFMUL	34	17	1269	17
CSA464	256	66	2218	18
HCA464	256	66	2342	19
WTM32	64	64	7654	49
MAC32	96	65	8524	58
DTM32	64	64	9429	35
DIV32	64	128	26,001	279
DTM64	128	128	34,485	43

First, we observe that for all benchmarks the SWD circuits give smaller area (on average 3.5× smaller). This is based on two main factors: (1) the Majority synthesis in conjunction with the MAJ SWD gate yield great results, and (2) the output voltage assumed doesn't require bulky output SAs. Second, we note that for all benchmarks the SWD circuits are much slower than the reference circuits (on average 12× slower). This is due to the large ME cell switching delay (0.42 ns for INV/MAJ operation—Table 7.4) which is accumulated according to the longest path of the MIG netlists. However, due to the low energy consumption of both the SWD gates and the SA design, the power consumption metrics are in large favor of the SWD circuits for all the benchmarks (on average 51× lower).

Table 7.7 contains two important product metrics which help compare the two technologies, one is the product of area and energy (A·E—divided by 1000 for ease of presentation) and the other is the area, delay, and energy product (A·D·E—again divided by 1000). A·E serves as an indicator of the low-power application benefits of this technology, where the performance (delay) is the critical metric. The second product metric A·D·E combines all aspects of circuit evaluation. The energy consumption of the N10 reference benchmarks is not directly given by the synthesis tool, so it's calculated as the product of delay and power (from Table 7.6).

Figure 7.9 depicts the results of Table 7.7. On average in both product metrics, the SWD circuits outperform the N10 counterparts. Consider the A·E product, except one benchmark (BKA264), SWD technology produces smaller and less energy-consuming designs. However, when accounting for the long SWD delays with the A·D·E product, the benefits of the SWD technologies hold only for the two deepest benchmarks (CSA464 and DIV32). This means that SWD circuits outperform N10 ones only in the cases of large and complex benchmarks where CMOS circuit performance is not easily optimized (note the quite large delays of 1.78 ns and 14 ns for CSA464 and DIV32, respectively—Table 7.6).

These results compel us to characterize SWD (with CMOS overhead circuitry) as a technology extremely adept for ultralow-power applications, where latency is a secondary objective. SWD circuits perform in a way that CMOS circuits are not

Table 7.6 Summary of benchmarking results

	Area (μm^2)				Energy (fJ)			Delay (ns)		Power (μW)	
Name	SWD core	CMOS SA	SWD total	N10	SWD core	CMOS SA	SWD total	SWD	N10	SWD	N10
CRC32	27.61	1.54	29.14	95.88	45.73	86.40	132.13	5.07	0.22	26.06	304.30
BKA264	36.48	3.12	39.60	118.55	63.32	175.50	238.82	5.07	0.21	47.10	133.92
GFMUL	44.09	0.82	44.91	162.98	76.31	45.90	122.21	7.17	0.16	17.04	433.92
CSA464	78.42	3.17	81.59	240.26	152.55	178.20	330.75	7.59	1.78	43.58	663.17
HCA464	82.71	3.17	85.88	262.63	162.06	178.20	340.26	8.01	0.29	42.48	594.28
WTM32	264.96	3.07	268.04	1163.37	635.03	172.80	807.83	20.61	0.58	39.20	3571.90
MAC32	295.25	3.12	298.37	1372.83	727.32	175.50	902.82	24.39	0.66	37.02	3872.10
DTM32	326.31	3.07	329.38	1183.64	822.32	172.80	995.12	14.73	0.52	67.56	3667.50
DIV32	899.04	6.14	905.18	3347.73	3009.03	345.60	3354.63	117.21	14.00	28.62	5346.10
DTM64	1192.69	6.14	1198.83	3459.32	4373.85	345.60	4719.45	18.09	0.63	260.89	12,793.10
Averages	324.76	3.34	328.09	1140.72	1006.75	187.65	1194.40	22.79	1.91	60.95	3138.03

Table 7.7 Summary of benchmarking products

Name	A·E (/1000)			A·D·E (/1000)		
	SWD	N10	Impr. (×)	SWD	N10	Impr. (×)
CRC32	3.9	6.4	1.7	6.8	1.4	0.2
BKA264	9.5	3.3	0.4	12.7	0.7	0.1
GFMUL	5.5	11.3	2.1	24.6	1.8	0.1
CSA464	27.0	283.6	10.5	94.5	504.8	5.3
HCA464	29.2	45.3	1.5	111.5	13.1	0.1
WTM32	216.5	2410.2	11.1	3508.0	1397.9	0.4
MAC32	269.4	3508.4	13.0	5292.9	2315.5	0.4
DTM32	327.8	2257.3	6.9	3989.7	1173.8	0.3
DIV32	3036.5	250,562.2	82.5	319,246.9	3,507,871.1	11.0
DTM64	5657.8	27,880.9	4.9	94,854.9	17,565.0	0.2
Averages	958.3	28,696.9	**13.5**	42,714.3	353,084.5	**1.8**

able to even if their optimized only for power consumption. Just their innate leakage power would be enough in large designs to exceed the power consumption of their SWD equivalents.

7.2.4 Discussion

In Sect. 7.2.2, we presented several experimental advancements toward the realization of the SWD concept, and in Sect. 7.2.3 we showcased the potential of the SWD with circuit evaluations. In order for these projections to become a reality, there should be several more steps implemented at the experimental level. The two main benefits the SWD concept has to offer are smaller area and lower energy than CMOS. In order for the first to be realized, more experimental work is needed for studying the behavior of exchange spin waves, which due to their short wavelength would have the ability to propagate in narrow and short waveguides (less than 100 nm wide). For SWD to deliver their low energy potential, the most crucial component to be experimentally verified is the ME cell spin wave generation and detection. Having experimental proof that the operational ME cell stack consisting of thin layers (not bulk piezoelectric as in [55]) can be integrated next to (or on top of) a ferromagnetic waveguide *and* that this cell would produce (and detect) well-controlled spin waves would be ideal. However, there are many challenges remaining for an ME cell realization. Such challenges include (but are not limited to) stacking a piezoelectric layer with other layers, maintaining its piezoelectric properties. Additionally, an ME cell should be optimized for spin wave detection, so that the read-out voltage is more than a few mV [9].

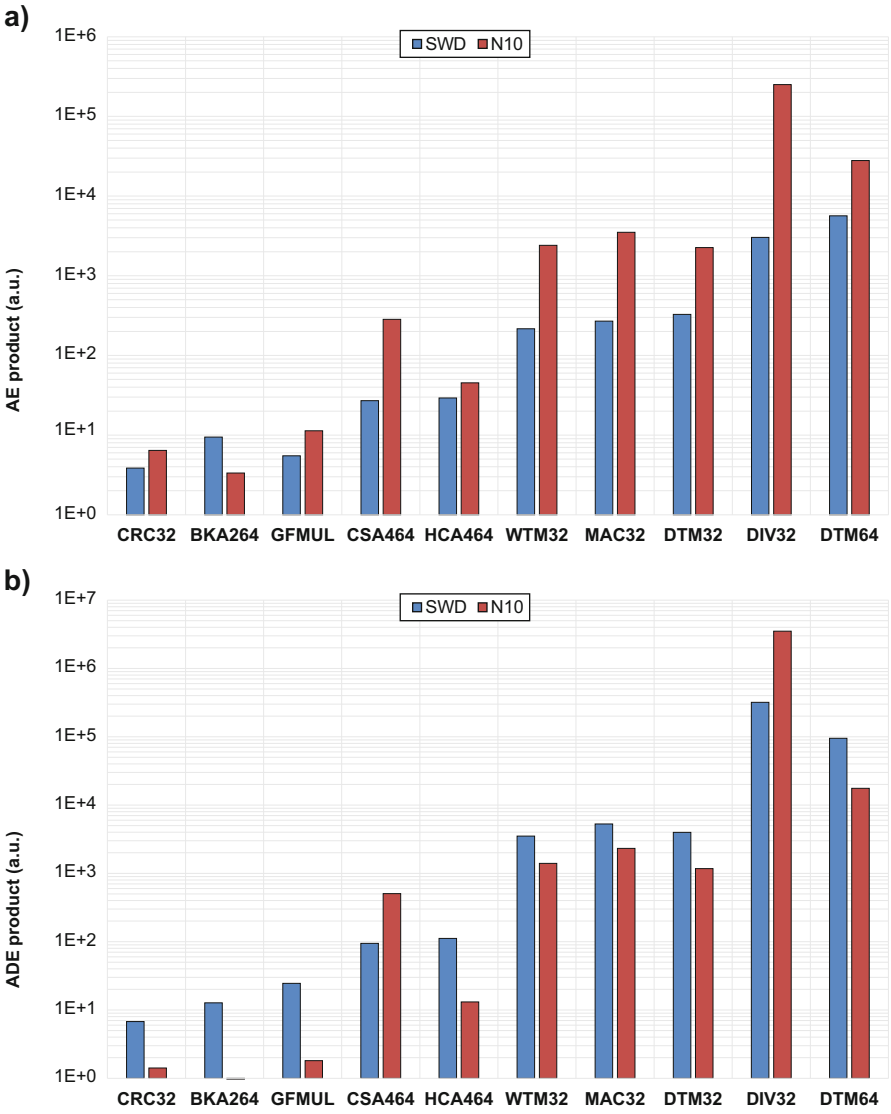

Fig. 7.9 Product metrics for all benchmarks, ordered according to benchmark size. (**a**) Area-Energy product. (**b**) Area-Delay-Energy product

In conclusion, the SWD circuit can be promising and be very useful as CMOS technology is reaching its limits, especially for low-power applications. Paving the way for the realization of this concept has started but there is a lot for improvement and necessary advancements.

7.3 Spin Torque Majority Gate

The concept of Spin Torque Majority Gate (STMG) was introduced by Nikonov et al. in 2011 [6]. Before introducing the working principle of STMG, two key spintronics notions will be explained: the Spin Transfer Torque and the Tunnel Magnetoresistance, which are the write and read mechanisms of STMG.

7.3.1 Working Principle of STMG

7.3.1.1 Device Description

The STMG consists of a perpendicularly magnetized free layer shared by four Magnetic Tunnel Junctions. The logic state ('0' or '1') is represented by the orientation of the free layer magnetization ('UP' or 'DOWN'), as illustrated in Fig. 7.10. The input magnetic states are written by STT via the three input Magnetic Tunnel Junctions. The output magnetization state is detected by the fourth MTJ via Tunnel Magnetoresistance (TMR). The cross shape of the free layer has a main advantage: It should allow for easy cascading by utilizing the output arm of the cross as an input arm for the next gate. Several types of cross were simulated [64]. However, the "simple cross" remained the most reliable.

It is important to note that the current is perpendicular to the plane of the free layer. In practice, a voltage is applied between the top and the bottom electrodes.

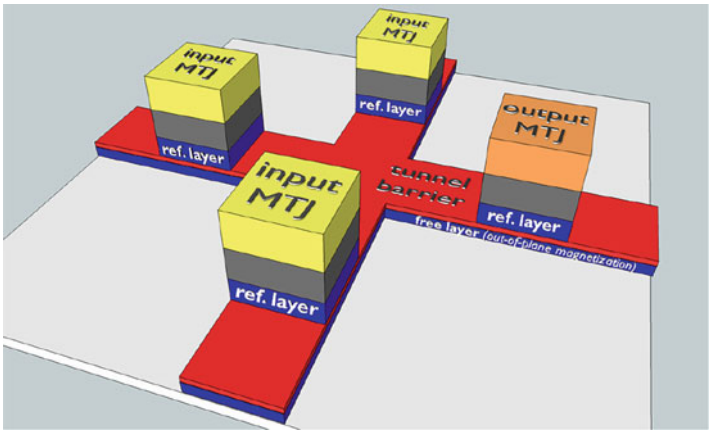

Fig. 7.10 Schematic view of a Spin Torque Majority Gate. The red layer is the oxide tunnel barrier. The reference layer and the free layer (both in blue) have perpendicular magnetic anisotropy. The reference layer induces the spin polarization, and the free layer carries information. The input MTJs convert information from charge to spin while the output MTJ converts it from spin to charge

Depending on the voltage polarity, the current flows either downward or upward, creating a torque that pushes the magnetization either up or down, representing a '1' or a '0'. Contrary to other concepts of DW logic [65–67], here, no current is injected in-plane. The vertical current flows in the areas defined by the input MTJs. Thus, the spin torque is exerted only at the inputs, while the rest of the free layer is mainly driven by the exchange interaction. Since exchange is a short-range interaction, the MTJs have to be close enough to each other for correct STMG operation. How close? This question will be addressed in the following section.

7.3.1.2 Micromagnetic Simulations and Analytical Model

Extensive micromagnetic simulations were performed to simulate the magnetization dynamics of the free layer [68]. The size and the main material parameters were varied for every possible input combination. The device is a functional majority gate if the majority of inputs is '1' lead to an output state UP (i.e., '1'), and if the majority is '0' lead to an output state DOWN (i.e., '0').

An example of simulation is shown in Fig. 7.11. The initial state is pointing UP (red). A negative voltage (i.e., '0') is applied to two input MTJs, pushing the magnetization down. A positive voltage (i.e., '1') is applied to the third MTJ, holding the magnetization up. These input signals, sent for 2 ns, are followed by relaxation time of 4 ns. At the end of the simulation, the magnetization under the output MTJ has switched to a down state (blue), as expected.

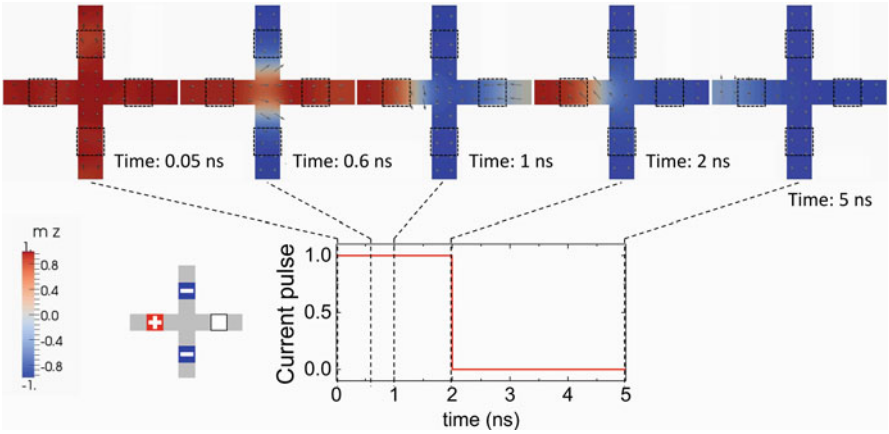

Fig. 7.11 Micromagnetic simulation of a Spin Torque Majority Gate having a strip width of 10 nm and typical material parameters of CoFeB. At the top: simulation snapshots. The color represents the magnetization orientation; red: up; blue: down. Here, the combination of inputs induces a down state in the top and bottom arms of the cross and an up state in the left arm. At the end of the pulse, the majority state down has been transferred to the output arm. This output state remains stable after turning off the current

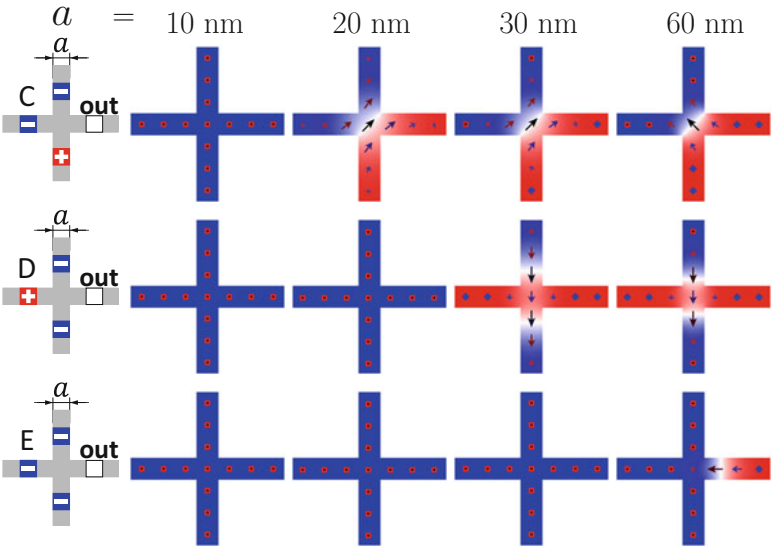

Fig. 7.12 From [68]. Final magnetic states of the STMG free layer for four different sizes, for three combinations of inputs that are supposed to switch the output arm. For a strip width of 10 nm, no failure is observed

For simplicity, all the simulations were started from an initial UP state. Therefore, it is expected that, for a majority of '1', the output does not switch, and that it switches for majority '0'. The expected behavior has been confirmed by simulation for all the trivial combinations that do not induce any switching. However, several failures have been observed when output switching is expected. In some cases, the failure can be easily explained by a current density being too small or a pulse duration being too short. However, in other cases, failure is observed even at large pulse duration and amplitude. This is illustrated in Fig. 7.12 for the combinations "C", "D" and "E" that are supposed to switch the output. Interestingly, the failures always disappear below a critical size, confirming the essential role of the short-range exchange interaction. "E" (last line of Fig. 7.12) has the largest critical size, while "C" (first line of Fig. 7.12) is the most critical input combination. In the latter, a domain wall (shown in white) is pinned at the center of the cross, along the diagonal. In magnetism, "domain wall" refers to the transition region between two magnetic domains. Here the two magnetic domains are pointing up (in red) and down (in blue), while the domain wall is in-plane (in white).

The results of the micromagnetic simulations for the input combination "C" have been summarized in the phase diagram of Fig. 7.13. The failure region corresponds to a final state with a domain wall pinned at the center of the cross. The working region corresponds to a switched output. In the simulations, the width a of the cross has been varied, as well as the exchange parameter A_{ex} and the anisotropy constant K_{eff}. For a given size, it was found that $\sqrt{A_{ex}/K_{eff}}$ is a relevant parameter

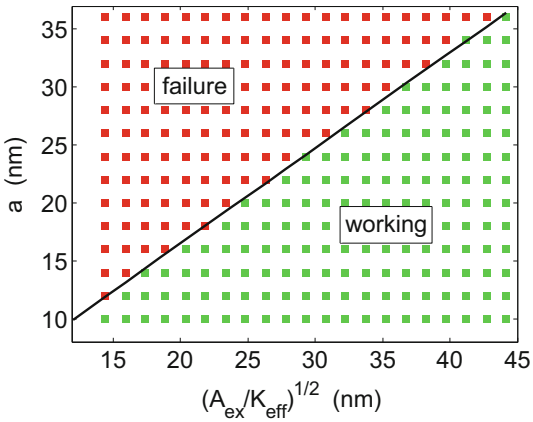

Fig. 7.13 From [68]. Phase diagram of a STMG of aspect ratio $k = 5$ obtained from micromagnetic simulations. Switched (*working*) and non-switched (*failure*) output states are given as a function of the strip width a and $\sqrt{A_{\text{ex}}/K_{\text{eff}}}$

that discriminates between failure and success. This parameter is known as being proportional to the domain wall width. Therefore, Fig. 7.13 reveals that majority operation is determined by a particular relation between the size of the device and the width of the domain wall. More specifically, for an aspect ratio $k = 7$, STMG is functional if $\sqrt{A_{\text{ex}}/K_{\text{eff}}} < 1.21a$.

Further investigation showed that STMG is very likely to fail when the domain wall is energetically stable at the center of the cross. In contrast, if the domain wall is unstable, the device exhibits majority operation, provided that the pulse of current is sufficiently large and long. Thus, STMG functionality is determined by the energy landscape.

Based on this conclusion, an analytical model was developed to derive the magnetic energy of the domain wall state [69] along the diagonal of the cross. Describing the domain wall as a function of two parameters, its position x_0 and its width Δ, the total energy was obtained.

$$E = 2t\,\zeta\,\left(A_{\text{ex}} + K_{\text{eff}}\Delta^2\right) + cst, \tag{7.18}$$

where t is the thickness of the free layer, cst is a constant, and ζ is given by

$$\zeta = \frac{3d}{\Delta} + \ln\left(\frac{1+e^{\frac{2x_0}{\Delta}}}{e^{\frac{d}{\Delta}}+e^{\frac{2x_0}{\Delta}}}\right) + \ln\left(\frac{1+e^{-\frac{2x_0}{\Delta}}}{e^{\frac{d}{\Delta}}+e^{-\frac{2x_0}{\Delta}}}\right) - \frac{2d}{\Delta}\left(\frac{e^{\frac{2x_0}{\Delta}}}{e^{\frac{L}{\Delta}}+e^{\frac{2x_0}{\Delta}}} + \frac{e^{-\frac{2x_0}{\Delta}}}{e^{\frac{L}{\Delta}}+e^{-\frac{2x_0}{\Delta}}}\right) \tag{7.19}$$

where $d = \sqrt{2}a$ and $L = ka/\sqrt{2}$. The function ζ reveals the major differences with the common 1D model of domain wall. Here, the center of the cross acts like a pinning site. Moreover, the effect of the finite length L is included in the last term.

The dependence of the energy with respect to the domain wall position x_0 is directly given by ζ. Figure 7.14 shows ζ as a function of x_0 for several domain wall widths Δ. For $\Delta = 10\,\text{nm}$, the domain wall is clearly a minimum of the energy in

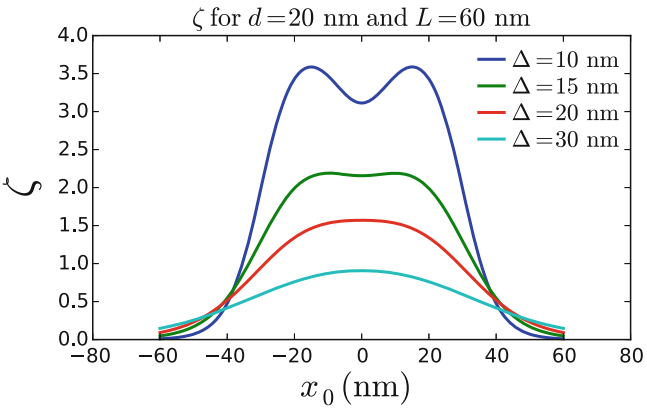

Fig. 7.14 ζ as a function of the domain wall position for several domain wall widths. The lateral length L and the distance d correspond to a cross of aspect ratio $k = 6$ and arm width $a = 14\,\text{nm}$

Table 7.8 The operating condition expressed as a function of a (arm width) and, equivalently, as a function of ka (total length of the cross)

	$k = 5$	$k = 7$	$k = 9$
$\sqrt{\frac{A_{ex}}{K_{eff}}} >$	$0.95\,a$	$1.27\,a$	$1.57\,a$
$\sqrt{\frac{A_{ex}}{K_{eff}}} >$	$0.190\,ka$	$0.181\,ka$	$0.174\,ka$

$x_0 = 0$. In other words, it is pinned at the center of the cross, along its diagonal, which leads to STMG failure. In contrast, for $\Delta = 20$ and 30 nm, the domain wall state is not in a minimum, which means that it cannot be pinned at the center. As mentioned previously, in that case, a pulse of current sufficiently large and long leads to the expected output. The case of $\Delta = 15\,\text{nm}$ is uncertain: The domain wall is in a shallow energy minimum in $x_0 = 0$, but it can be overcome when the STT is applied. For reliable STMG, this state should also be avoided.

The analytical model is valid for any aspect ratio k. The condition for the domain wall not being an energy minimum has been solved numerically at several values of k. The results are summarized in Table 7.8. These results are in very good agreement with the micromagnetic simulations at $k = 7$, confirming the validity of the analytical model. Interestingly, the ratio of the total length ka and the domain width determines the operating condition. In summary, the domain wall width should be larger than about $0.2\,ka$ to be unstable at the center, leading to functional STMG.

7.3.2 *Circuit Outlook of STMGs*

As mentioned in Sect. 7.2.3, it is important to evaluate each emerging technology and identify potential advantages and drawbacks of their circuit implementation. The following section introduces the results of such benchmarking calculations

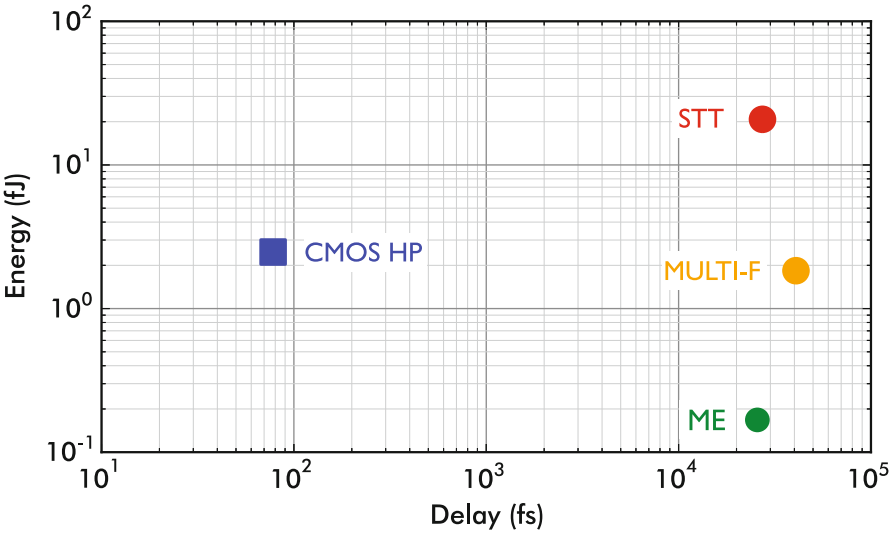

Fig. 7.15 Energy over delay, for a 32-bit adder, all data from [4, 70]. CMOS HP is the CMOS High-Performance implementation, STT [4] is the original proposal of STMG implementation, MULTI-F [4] assumes use of multi-ferroic input and output elements, ME [70] assumes use of magnetoelectric input and output elements

along with the requirements STMG technology has to fill in order to fully exploit its potential.

7.3.2.1 Benchmarking

STMGs have been benchmarked several times [4, 5, 70] versus CMOS and other beyond-CMOS technologies. A summary of the benchmarking results presented over the years is shown in Fig. 7.15. Energy and delay of a 32-bit full adder are used as metrics to compare CMOS High-Performance (CMOS HP) implementations to different flavors of STMG.

The first version of STMG shown in Fig. 7.15 (STT) is the one that uses MTJs and STT for generating the inputs. This version has been the original proposal [6] and the one studied in this chapter so far. We can clearly see that the circuit modeling of this version produces a result which is inferior to CMOS by one order of magnitude in energy and two orders of magnitude in delay. However, in [4], an alternative version of STMGs was modeled, which used voltage-controlled multi-ferroic elements for signal generation (Fig. 7.15 (MULTI-F)). These elements consume less energy and produce an 11× more energy-efficient result.

Lastly, Nikonov and Young presented in [70] a model of an STMG technology that utilizes Magnetoelectric cells (ME) as inputs and outputs. Taking this into account, the targeted 32-bit full adder can be implemented with an order of

magnitude improvement in energy compared to CMOS HP. From the results in Fig. 7.15, two statements can be made: (a) the appropriate application of STMGs is on designs that target low-energy operation and not high-performance, and (b) the input/output elements of STMG circuit should be voltage-controlled and as energy-efficient as possible to maximize the benefits of the technology.

7.3.2.2 Discussion

With the aforementioned results in mind, we can define a set of requirements for efficient implementation of STMGs from a circuit perspective. To be a serious contender to CMOS, STMG-based circuits should be reliable and consume less energy, but they should also meet the need of an application that exploits its intrinsic non-volatility. More specifically, the following points should be addressed.

1. **Energy-efficient generation and detection of domains**
   In the original concept, proposed in [6], MTJs are used to generate the input domains by STT and detect the output domain by TMR. These two mechanisms require current to flow through a tunnel barrier, which leads to a substantial energy consumption, especially at the inputs where the current density is larger. Instead, domains could be nucleated using Voltage-Controlled Magnetic Anisotropy, magnetoelectric effect or Spin-Orbit Torques, for instance. These effects have been actively studied in recent years as they are promising alternatives to STT.
2. **Energy-efficient domain propagation**
   The majority domain should propagate as fast as possible between the inputs and the output. This is critical for delay but also for energy, as the input signal must be activated until the end of the operation. In the present concept of STMG, the domains are switched via the exchange interaction that couples the STT-driven spins to their neighbors. The efficiency of this method is not very well known but it could certainly be increased by a more direct coupling between the input signal and the magnetization to switch. Improving the domain propagation would also enable easier cascading of the gates. All in all, the STMG could be operated with two independent mechanisms: One that would switch the inputs and another one that would assist the propagation of the majority domain. Thus, both could be optimized independently without trade-off.
3. **Wider operating range**
   The STMG can operate only when a domain wall is not stable inside the cross. This is a restrictive condition that implies small anisotropy and small size, hence small thermal stability. A device that would allow a domain wall could have a much wider operating range and would give much more flexibility for circuit design.
4. **Use of non-volatility**
   Having a magnetic domain as the information carrier lends itself to inherit non-volatility at each gate output. In order to maximize the benefits of STMG,

this non-volatility has to be exploited by the circuit design. A common way of doing this is to utilize non-volatility to reduce static/leakage energy consumption [71]. This aspect of STMG has not been addressed yet but should yield significant advantages compared to CMOS and other volatile emerging technologies.

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