Chapter 1
Nanopackaging: Nanotechnologies and Electronics Packaging

James E. Morris

1.1 Introduction

Level one electronics packaging is traditionally defined as the design and production of the encapsulating structure that provides mechanical support, environmental protection, electrical signal and power I/O, and a means of heat dissipation for the Si chip, whether digital or analog, processor, or memory. Level two packaging is then the integration of these packaged chips into a board-level system that similarly provides mechanical support, power and signal delivery and interconnections, and thermal dissipation. Of course, nowadays the chip is often mounted directly on the board (chip-on-board, direct chip attach, flip chip), and the packaging process actually begins with the chip fabrication (wafer-level packaging), e.g., with solder bumping. The underlying principles of the field are covered in textbooks [1–3], and a multitude of others, e.g. [4], are more research focused. The field is inherently multidisciplinary with electrical, mechanical, and thermal design at its core, with all of these subject to reliability studies and material selection. Figure 1.1 shows the history of the electronics package from the vacuum tube to a multi-chip "system in a package" (SiP). The package has always been the limiting factor to system performance, i.e., the Si chip can operate at higher frequencies than the package.

Current issues facing the electronics package designers include:

- Thermal dissipation
- High temperature and power applications. (This is driving transient liquid-phase soldering/sintering (TLPS) joining, which enables high-temperature intermetallic compound (IMC) alloy joints from low-temperature processing of low melting point materials.)

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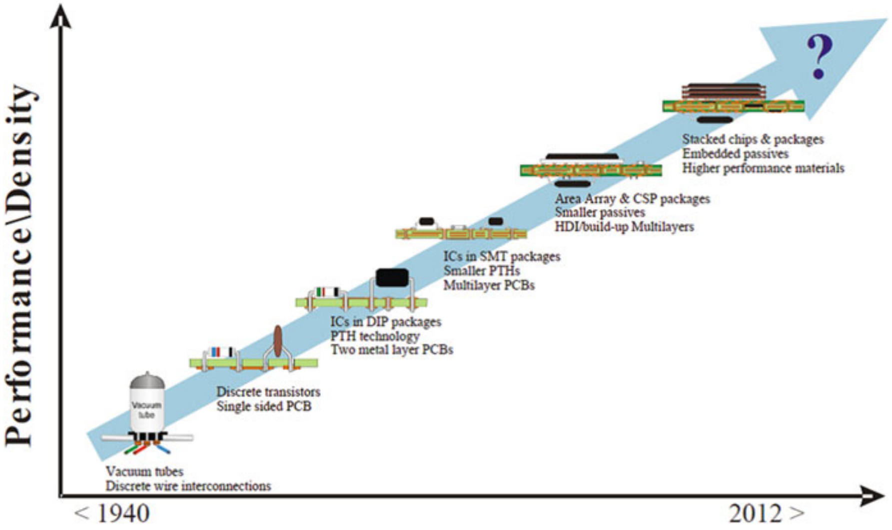

Fig. 1.1 The evolution of electronic assembly. (Joe Fjelstad, with permission)

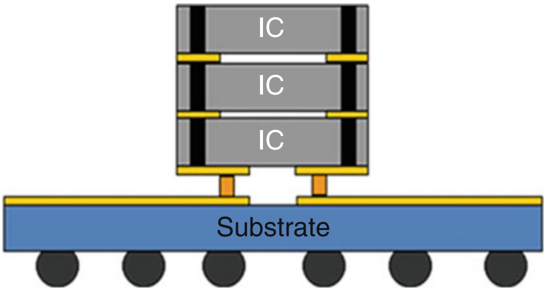

Fig. 1.2 The concept of TSVs for 3D chip stacking

- Embedded passives. (Traditionally, most of the printed wiring board (PWB) surface is taken up by many passive components. Embedding them inside the PWB would release surface area for more active Si-integrated circuits (ICs).)
- 3D system integration. (Chip stacking drives through silicon via (TSV) technology (Fig. 1.2).)
- Heterogeneous system integration. (More than Moore implies the integration of unlike technologies, e.g., random logic, memory, microelectromechanical systems, optical and RF communications, etc., in a SiP enabled by chip stacking.)
- Flexible electronics includes both wearable and robotic systems.
- No-Pb solder. (The prevalent no-Pb solder is Sn-Ag-Cu (SAC), which melts at higher temperatures than traditional eutectic Sn-Pb solder, exacerbating electromechanical stresses in the package and failures, creating interest in lower-temperature solders and sintering.)

It often seems that the promise of nanotechnology's impact on everyone's quality of life is as over-hyped as past promises of endless cheap energy from cold fusion and high-temperature superconductivity. But there are two major differences. While the term "nanotechnology" has caught the attention of industry, legislators, and research funding agencies, in most cases the technologies in question are rooted in steady research progress in the field in question, as fabrication and characterization techniques have steadily conquered ever smaller dimensions, with the parallel development of theory to explain and model the new phenomena exposed. Furthermore, nanotechnologies have already yielded everyday consumer benefits beyond stain-resistant clothing and transparent sunblock. So it is hardly surprising to discover active research and development programs in nanotechnology applications to electronics packaging, with special nanotechnology sessions at electronics packaging research conferences and research journal papers demonstrating the range and progress of these applications.

The definition of nanotechnology is usually taken to be where the size of the functional element falls below 100 nm or 0.1 μm, and with 10 nm node CMOS devices upon us, we are already well into the nanoelectronics era. Furthermore, with metallic grain sizes typically below this limit, one might also argue that solder has always qualified as a nanotechnology, along with many thin-film applications. So, the requirement that the specific function depends upon this nanoscale dimension is conventionally added to the definition. According to this *caveat*, MOSFET technology, for example, would not qualify by simple device shrink but would at dimensions permitting ballistic charge transport.

New nanoscale characterization techniques will be applied wherever they can provide useful information, and the atomic force microscope (AFM), for example, is relatively commonly used to correlate adhesion to surface feature measurements. More recently, confocal microscopy has been applied to packaging research [5], but it is especially interesting to note the development of a new instrument, such as the atomic force acoustic microscope [6], which adapts the AFM to the well-known technique for package failure detection.

1.2 Computer Modeling

The use of composite materials is well established for many applications, but while overall effective macroscopic properties are satisfactory for computer modeling of automotive body parts, for example, they are clearly inadequate for structures of dimensions similar to the particulate sizes in the composite. The modeling of such microelectronics (or nanoelectronics) packages must include two-phase models of the composite structure, and this general principle of inclusion of the nanoscale structural detail in expanded material models must be extended to all aspects of package modeling [7]. The extended computer models can be based on either the known properties of the constituent materials (and hopefully known at appropriate dimensions) or the measured nanoscale properties (e.g., by a nano-indenter [8, 9] or

AFM [10]). Molecular dynamics modeling software has been particularly useful in the prediction of macroscale effects from the understanding of nanoscale interactions [11]. Computer modeling is covered in more detail in Chaps. 2, 3, 4, and 5.

1.3 Nanoparticles

1.3.1 Nanoparticles: Introduction

Nanotechnology drivers are the varied ways in which material properties change at low dimensions. Electron transport mechanisms at small dimensions include ballistic transport, severe mean free path restrictions in very small nanoparticles, various forms of electron tunneling, electron hopping mechanisms, and more. Other physical property changes going from the bulk to nanoparticles include:

- Melting point depression, i.e., the reduction of metal nanoparticle melting points at small sizes [12], although this is unlikely to be a factor in packaging applications with even 10% reductions typically requiring dimensions under 5 nm [13]
- Sintering by surface self-diffusion, which is thermally activated, with net diffusion away from convex surfaces of high curvature [14]
- The Coulomb blockade effect, which requires an external field or thermal source of electrostatic energy to charge an individual nanoparticle and is the basis of single-electron transistor operation [15]
- Theoretical maximum mechanical strengths in single grain material structures [16]
- Unique optical scattering properties by nanoparticles one to two orders smaller than the wavelength of visible light [17]
- The enhanced chemical activities of nanoparticles, which make them effective as catalysts, and other effects of the high surface-to-volume ratio

Chapter 6 considers nanoparticle properties in more detail.

1.3.2 Nanoparticles: Fabrication

Noble metal nanoparticles have been fabricated by an ultrasonic processing technique [18] and Ag/Cu with “polyol” [19]. Alternatively, a precursor may be used, e.g., $AgNO_3$ for Ag nanoparticles, and there are techniques to control the particle shapes, e.g., spherical, cubic, or wires [20]. Good dispersion and smaller nanoparticles are achievable with ~60 MHz ultrasonic agitation [21]. Nanoparticle fabrication is reviewed in Chap. 7 and specifically Ag nanoparticle fabrication in [22].

1.3.3 Nanoparticles: Embedded Capacitors

For a planar capacitor of dimensions L_x, w_y, and t_z in the x, y, and z directions, respectively, the capacitance, C, between metal contact plates of area L_x x w_y at $z = 0$ and $z = t_z$ (for $t_z << L_x, w_y$) is $C = \varepsilon(L_x \text{ x } w_y)/t_z$ where ε is the dielectric constant. In microelectronic systems, substrate area is precious, even when one can move passive components from the PWB surface. To increase C for a given area (l_x x w_y), one must shrink the thickness t_z. As t_z approaches the nanoscale, any particles in a composite dielectric must be smaller still.

The move toward embedded passive components at both on-chip and PWB levels has also prompted a search for high dielectric constant materials for low area capacitors. High dielectric constants can be achieved by the inclusion of high dielectric constant particulates and minimal thickness. The latter requirement pushes one toward nanoscale particulates, with examples of the former covering ceramic [23–26], silicon [27], and metal [28–32]. The ceramic particles are generally barium titanate, e.g., applied to organic FETs with composite k around 35 [24]; in such materials, the particle surface energy must be reduced to avoid aggregation [25].

The target *k* is 50–200, and while *k*~150 has been achieved, it is at the expense of high leakage (dielectric loss.) Similar structures have been studied in the past as "cermets," (ceramic-metal composites,) for high-resistivity materials for on-chip resistors [33], which conduct by electron tunneling between particles. At low fields, the nanoparticles can act as Coulomb blocks to minimize DC leakage if they are sufficiently small [27], but still do not eliminate it at finite temperature [34]. It is the AC performance which is more important, however, and inter-particle capacitance will bypass the block unless pseudo-inductive effects develop at capacitor thicknesses which permit even short nanoparticle chains [35].

An alternative approach to leakage is to use aluminum particles, to take advantage of the native oxide coating [30], with *k*~160 achieved [31]. Ag/Al mixtures have also been studied [32].

Design, fabrication, and testing of commercial $BaTiO_3$-based embedded capacitors are described in [36], while [37, 38] describe two alternative techniques for embedding the $BaTiO_3$ particles in the polymer. In [37] hyperbranched polymer shells are formed around the nanoparticles with methyl methacrylate added to enhance cross-linking between them, and in [38] the composite is formed by electrospinning polymer fibers containing the $BaTiO_3$. (Electrospinning is described in Chaps. 12 and 21). In [39] the $BaTiO_3$ is in the form of nanorods. Smaller $BaTiO_3$ nanoparticles (~6 nm) exhibit higher breakdown strengths and lower loss factors than larger ones (~90 nm) but with lower dielectric constants [40].

See also Chap. 8.

1.3.4 Nanoparticles: Embedded Resistors

See also Chap. 9.

For the same dimensions as specified for the capacitor above, the resistance, R, of an embedded resistor is $R = \rho.L_x/(w_y \text{ x } t_z)$, where ρ is the resistivity, often written $R = (\rho/t_z) \text{ x}.(L_x/w_y)$, where ρ/t_z is termed the surface resistivity in Ω/square and L_x/w_y is the number of "squares" along the length L_x of the resistor. Again, to minimize the x-y area, the thickness t_z is driven down to the nanoscale for high surface resistivities with a low (ideally zero) temperature coefficient of resistivity (TCR) being also required. Thin-film resistor materials include alloys (e.g., Ni/Cr, Ni/P), polymer or ceramic/metal composites (cermets) (e.g., C/epoxy, Cr/SiO_2), conducting polymers (e.g., coating various filler nanoparticles [41]), and others such as TaN [42, 43]. The ratio of TaN to Ta_3N_5 can be controlled by the N_2 in the sputter deposition chamber, affording some control of the TCR <0. Most cermet films balance the positive TCR of a continuous metallic percolating cluster phase against the negative TCR of an electrostatically activated tunneling process between isolated nanoparticles. In a Ag/Ta_3O_5 cermet [44], a large negative Ta_3O_5 TCR is transformed into a near-zero positive TCR by the Ag content, apparently even as isolated nanoparticles.

Note that thermally conductive materials have very similar structural requirements to the passive components, with metallic or SiC nanoparticles as fillers [45].

1.3.5 Electrically Conductive Adhesives

The addition of smaller μm diameter silver powder to 10 μm silver flakes in isotropic conductive adhesives (ICAs) reduces resistance by inserting bridging particles between the flakes. The simple addition of nanoparticles does not improve conductance, due to mean free path restrictions and added interface resistances, and the same principles limit the performance of alumina-loaded thermal composites [46]. The addition of silver nanoparticles does achieve dramatic reductions, however, by sintering wide area contacts between flakes [47], a principle also applicable to via fill [48, 49]. Filler nanoparticle sintering can also improve anisotropic conductive adhesive performance [50], aided by contact conductance enhancement by the addition of self-assembly molecular surface treatments [47, 51, 52]. Sintering effects have also been shown to improve contacts in materials with sufficiently low filler content as to be regarded as non-conductive adhesives [53]. When silica nanoparticles are added to a Cu-powder/Cu-epoxy ICA [54], they can inhibit crack propagation and improve adhesive strength. Ink-jet printable adhesives [55] would be another significant step forward, possibly achievable with nanoscale fillers that are less likely than micro-flakes to clog nozzles.

Nanoparticles in ICAs and anisotropic conductive adhesives (ACAs) are considered further in Chaps. 11 and 12.

1.3.6 Nanoparticles: Sintered Interconnect

Surface electrical interconnect for board and package levels can be achieved by screen printing and sintering nanoscale metal colloids in suspension [56–58], and now ink-jet-printed conductors are relatively routine, especially for flexible polymer substrates [59–61]. Electrical continuity is established by sintering, e.g., of 5–10 nm silver particles [62–65], and sintering may be accomplished at room temperature [66–68], by laser [69] microwave [60] or oven heating, or by plasma immersion [59]. Resistivities as low as around 4–6 μΩ.cm are achievable by annealing at 200–300 °C [70, 71]. Lower-temperature processing is important for polymer/flex substrates [72, 73] but results in higher porosity [74, 75], which translates to higher resistivities [61]. The changing electrical and mechanical properties as the sintered material is aged or stressed have been correlated with changing pore sizes and shapes [76–79].

Stretchable circuits are more than just flexible and are directed more to wearable applications but can still find applications in packaging. Ag nano-ink can be stamped on a stretchable substrate in conductive horseshoe chain patterns that can stretch like a concertina [80] with less than 10% resistance increase at 50% strain. The traditional bimodal Ag flakes and nanoparticle filler are compared with nanowire and dendrite fillers in polyurethane in [81].

Sintered Ag nanoparticles can also be used for die-attach [82] or thermal interfaces [83–85]. In the last example, 10 nm Ag nanoparticles nucleate on the surface of Ag-oxalate microparticles and bond by sintering, achieving thermal conductivity of 100 W/mK [85]. As a variation, magnetic composite films (e.g., of Co/SiO_2 in BCB and Ni/ferrite in epoxy) have been screen-printed for antennas [86]. Sn/Ni bumps have also been grown on Sn from a nanometer Ni slurry [87]. Ag nano-ink deposited on a stepped via [88] has proven to be more resistant to shrinkage and cracking than in a simple barrel via [89].

With maturity of the nano-Ag technologies, attention has switched to the possibility of sintered copper interconnects, which offer a cheaper alternative to Ag, but with the problem of oxidation, since unlike the silver oxides, the copper oxides are insulating. Again, the emphasis is on flexible polymer substrates [72, 73], and the research extends, for example, to Ag-coated Cu nanoparticles [71]. Generally, the oxide problem is avoided by nanoparticle fabrication in solution and processing in controlled inert atmospheres [90, 91] or by using the surface oxide as a temporary protective coating [92]. In other cases, e.g. [93], the solution chemistry can provide a protective organic coating automatically. As with ICAs, a bimodal distribution of copper nanoparticles and microparticles can yield lower resistivities than either alone [94, 95].

With copper interconnect prevalent on-chip, and growing interest in 3D chip stacking, copper nanoparticles are finding application in direct Cu-Cu bonding, with sintered nanoparticles bonding to each face [96–100]. Silver nanoparticles have also been used for Cu-Cu bonding [101, 102] but of course run the risk of Kirkendall voids.

An innovative interconnection technology based on nanoporous materials is described in [103, 104]. In these papers, the Ag is etched out of an Au/Ag alloy leaving a porous sponge-like structure of Au behind. Two such porous contacts can bond at low pressure (10 MPa) and low temperature (200 °C) with "a similar characteristic as sintering processes" [103]. More recently, the concept has been extended to nanoporous Cu contacts synthesized from a Cu/Si alloy which is sintered in a N_2 atmosphere [105].

The field of sintered nanoparticle interconnect has been reviewed recently in [106] and in Chaps. 13 and 14.

1.3.7 Nanosolder

Often, "nanosolder" papers turn out to be about sintered interconnects, but there are examples on nanosolder in the literature, based on true melting point (MP) depression. Second-order effects include shape dependence of the decreased and increased coefficient of thermal expansion (CTE) at smaller nanoparticle sizes [107, 108]. For the case of a disk-like nanoparticle of radius r_d and thickness t of equal volume to a sphere of radius r_s, the shape factor, defined as the ratio of the projected surface areas of the disk and sphere (to normalize the ratio = 1 for the sphere), is $r_s/3$ t. Clearly, the minimum particle dimension controls the MP reduction because of the disordered surface layer thickness. For a disk of thickness $t \sim r_s/5 \sim 5$ nm, the disk MP reduction is 25% rather than 10% for a 5 nm radius spherical particle. For similar reasons, the CTE of a 2.5 nm diameter spherical Fe particle increases by about 60% with further increases for shape factors >1.

The MP depressions of solder alloys follow the same trends as for metals [109]. Solder alloy nanoparticles have been fabricated and the MP and other properties determined [110–113], generally agreeing with theory at 5 nm and 20 nm radii. Interestingly, the solidification temperature for a nanoparticle of given size is less than the MP, and the variation with size is less marked [114]. In a dynamic nanosoldering operation though, with a paste containing multiple nanosolder particles, coalescence increases both the solidification and melting temperatures as the particles increase in size. Koppesa et al. [115] demonstrates the process as the temperature is raised in steps. It is not clear that there is any MP depression advantage in this case or in [116]. Ideally, one should be able to take advantage of the shape factor MP depression to use solder nanowires as a low-temperature solder source [117, 118], but at 50 nm diameter [119], there is still unlikely to be much MP depression advantage. However, in this case the temperature was raised by Joule heating, which could provide a different advantage for solder nanowires.

As an alternative to soldering, transient liquid-phase sintering/soldering (TLPS) has been demonstrated for joining Si wafers for 3D integration by a Cu nanorod/Sn/Cu structure [120–122] with a fundamental process study in [123]. In this process, solid-state diffusion leads to a high-temperature Sn/Cu IMC. Ag-nanowire bonding has been demonstrated by solid-state wetting and subsequent atomic diffusion between the nanowires [124].

1.3.8 Nanoparticles in Solder

The addition of Pt, Ni, or Co nanoparticles to no-Pb Sn-Ag-based solders [125, 126] eliminates Kirkendall voids, reduces intermetallic compound (IMC) growth, and reduces IMC grain sizes, significantly improving drop-test performance [127]. Similarly, Ni or Mo nanoparticles promote finer grain growth, increased creep resistance, and better contact wetting [128]. Nanoparticles in the grain boundaries also inhibit grain boundary sliding and thermomechanical fatigue, but a similar function can be provided by 1.5 nm $SiO_{1.5}$ polyhedral oligomeric silsesquioxane structures with surface-active Si-OH groups [129]. One hundred nanometer Zn nanoparticles were added to non-conductive films employed in Sn-Ag soldering of Cu pillars to lower intermetallic compound (IMC) formation [130], but note that Amagai found no IMC reduction with Zn addition to solders [127, Chap. 15].

Other nanoparticles added to solder include Ag and TiO_2 for improved substrate wettability and adhesion [131–133], alumina [134], silica, diamond, $Bi_2Te_{3,}$ and La_2O_3 for mechanical strength [135–138]. The TiO_2, diamond, and Bi_2Te_3 also inhibited IMC formation, while the La_2O_3 also improved wettability and thermomechanical reliability, as demonstrated by resistance to thermal shock. The silica was bound to the solder matrix with POSS trisilanol [135]. Ag nanoparticles can precipitate out of the solder matrix, degrading the solder joint over time [139]. The effects of nanoparticles in solder have been reviewed in [140].

1.3.9 Nanoparticles: Nanocomposites

The key advantage of nanoscale silica particles in flip-chip underfill formulations is that they resist settling [141]. They also scatter light less than the larger traditional fillers, permitting UV optical curing and providing a dual photoresist function from a single material [142] and other advantages of optical transparency [143]. The higher viscosity of the nano-filled material can be reduced by silane surface treatments [144]. Further improvement is possible with a subsequent second layer [145]. Mesoporous silica, where the μm scale aggregates are characterized by a high nanoscale surface-to-volume ratio, has also been shown to be better than similarly sized solid particles [146]. One hundred nanometer silica particles have also been incorporated into a non-conductive film, which effectively serves as an underfill [147]. Underfills also serve as thermally conductive paths, and the thermal conductivity can be raised an order of magnitude by the addition of 10 nm Ag nanoparticles to underfill with 10–40 μm silica, BN, or diamond fillers to provide enhanced thermal contact between the larger particles [148]. Fabrication involves nanoparticle self-assembly to create the inter-particulate necks.

Nanoparticle-filled composites can be used as encapsulants. The addition of a bimodal dispersion of 8–10 μm bentonite with 12 nm SiO_2 to epoxy slows moisture absorption in a humid environment significantly [149]. Two to six nm nanoparticles of TiO_2 in a silicone LED encapsulant increase the refractive index and reduce the internal reflection light at the GaN/encapsulation interface [150]. A silica bimodal distribution of 1 μm SiO_2 powder and ≤50 nm nanoparticles has been laminated with a resin film to form circuit boards that outperform the traditional FR-4 in CTE, storage, and flexural moduli and warpage [151].

1.4 Carbon Nanotubes (CNTs)

1.4.1 CNTs: Fabrication

CNT growth can be accomplished for both electrical and thermal applications by chemical vapor deposition [152], with satisfactory solder wetting of the CNTs for electrical contacts. One usually requires bundles of aligned CNTs, whether large or small diameter SWCNTs (single-wall CNTs) or MWCNTs (multiwall CNTs.) The bundles morph from SWCNTs to MWCNTs as one increases the catalytic particle sizes to grow larger diameter SWCNTs, and small diameter SWCNTs need low growth rates [153]. Similarly, bundle densities are limited at the low end by alignment limitations and at the high end by achievable catalytic particle densities [153]. 950 °C is usually quoted as the minimum growth temperature for SWCNTs, with lower values quoted for MWCNTs. In fact, SWCNTs can be grown at lower temperatures (down to 365 °C [154]) but at the expense of greater defect densities.

One approach to minimizing CNT bundle resistance and maximizing current density, given the practical constraints above, is to densify the bundles post-growth. This is usually accomplished by some sort of organic liquid/vapor [155–158], but deposited solid-phase materials have been demonstrated too [159].

Most fabrication techniques yield vertical z-axis interconnect bundles, but for horizontal (x- or y-axis) interconnects, one can either realign a vertical bundle by liquid surface tension [160] or grow the bundle in a horizontal electric field at the outset [161].

CNT synthesis and characterization are covered in Chaps. 17 and 18.

1.4.2 CNTs: Composites

CNT/polymer composites have potential electrical, mechanical, and thermal applications in electronics packaging [162]. The key to achieving the target properties in such composites is effective random CNT dispersion, requiring a suitable choice of liquid agent [163], ultra-sonication [164], MHz sonication with an AC electric field [165], or similar techniques. The primary result of such composites is an improvement in Young's modulus [164] and other mechanical properties [166], but the combination of CNTs with carbon microfibers can be much more effective [167].

For electrical applications of randomly dispersed CNT/polymer composites, one needs good electrical contacts between the cylindrical CNT surfaces [168]. Modeling can include CNT volume fraction, diameters, and lengths to determine the percolation threshold [169], but it has been shown that CNT flexibility must be taken into account [170]. Also, the CNT-CNT contact resistance is typically unknown in such simulations. Experimentally, the CNTs can be coated with Ag, for example, to reduce this resistance [171]. When CNTs are added to a conventional Ag-loaded ICA, electrical and thermal conductivities and reliability lifetime can all improve [172]. Acid etching the CNTs to introduce surface defects before mixing to form a CNT/alumina composite further improves the mechanical properties [173], and the same effect is expected with polymers with the defects improving CNT-matrix bonding.

CNTs have also been mixed with carbon black in PDMS to provide low-resistance flexible electrodes (up to ~80% strain) for wearable microsystems [174].

If an aligned CNT/polymer composite is required, the polymer would have to be infiltrated around the CNTs of a previously grown bundle. Studies have shown that capillary forces can buckle the CNTs if the bundle is too long, or the CNTs are too close together, or the (MWCNT) walls are too thin [175].

There is growing interest in CNT/metal composites for a variety of applications [176, 177]. These include random CNT distribution within, for example, copper interconnects for increased resistance to electromigration [178], which should work for solder too. Another source of interest lies in the possibility of reducing the coefficient of thermal expansion (CTE) of metals in the package, especially of electrical interconnections of various types [179]. A major cause of package failures is due to the thermal mismatch between the silicon chip and both metals and polymers. CNTs (and graphene) have negative CTEs around 300 K, depending on chirality and diameter, with different figures for axial and radial CTEs [180]. The inclusion of randomly dispersed or aligned CNTs within a polymer, or more likely at higher densities within a metal conductor, has the potential to reduce the CTE mismatch to Si significantly, possibly even achieving a match.

Most of the interest in CNT/metal composites is for copper, but Ag/CNT composites have been made for interconnects on highly flexible substrates by the heterogeneous nucleation of Ag nanoparticles on CNTs [181]. Further growth of the Ag bonds the CNTs together, retaining the flexibility to survive longer flex cycling at lower resistances than conventionally deposited Ag films. Similar processes, e.g., electroless deposition, have been used to metallize CNTs to form hybrid CNT/Cu nanowires [182–184]. Printed Ag/CNT composites (Ag flakes-/Ag nanoparticle-decorated CNTs) have been demonstrated for conformally coated contacts and TSV fillers [185].

In CNT/Cu composites, the mechanical properties are regularly improved [186–189], but both decreases [187] and increases [188, 189] in electrical and thermal resistivities have been reported.

The addition of carbon nanotubes (CNTs) to solder can also have beneficial effects, e.g., 30–50% improvements in tensile strength [126, 190] and a 40%

increase in reliability lifetime with an aligned CNT structure [191]. Both increased [192] and decreased [132] wettabilities have been observed.

Aligned CNT/Cu composites are attracting interest for 3D TSV interconnections for chip stacking; this topic is explored below.

1.4.3 CNTs: Thermal

The high thermal conductivity of CNTs is being exploited for microelectronics chip cooling both directly in conductive cooling and indirectly in convective cooling systems [193, 194]. It appears that aligned CNTs offer the best hope for an order of magnitude improvement over current thermally conductive materials [195]. The thermal properties of vertically aligned CNT systems are being studied [196–198]. For conductive systems, the key is to establish CNT alignment [190], since the thermal conductivities of random arrays (of CNTs and carbon fibers alike) fall far short of expectation, showing no advantages over conventional materials, often also because of CNT fracture at the substrate [199]. In one of the most advanced techniques, vertical CNTs are first grown on both the aluminum heat sink and silicon chip surfaces, which are then positioned ~μm apart in a CVD furnace, enabling the CNTs from the two surfaces to grow further and connect with each other [190]. Composites incorporating CNTs have also been studied for thermal interface materials, e.g., CNT/carbon-black mixtures in epoxy resin [200]. The use of a liquid crystal resin matrix can impose structural order on the CNT alignment to yield a sevenfold improvement in thermal conductivity [201]. Electrospun polymer fibers filled with CNTs, or with SiC or metallic nanoparticles, have shown advances in both mechanical and thermal properties [202, 203].

So far, convective CNT cooling has been limited to the use of μm-scale clusters of vertically grown nanotubes [204–206]. These clusters define micro-channels for coolant flow which look very much like the metal or silicon cooling fins they aim to replace (Fig. 7 in Chap. 24) with similar thermal performances. The problem is that the flowing coolant is only in contact with the outermost CNTs of the clusters, and the internal CNTs are separated from each other. The system has been modeled [193], and one solution is to spread the CNTs apart to permit coolant contact with each one [204], but another is to thermally connect the CNTs by secondary lateral CNTs [207] or graphitization [208]. The problem then is whether individual CNTs can withstand the coolant flow pressure without detaching from the substrate. There is also a high thermal resistance between the CNT and the epoxy used for the CNT transfer process [209, 210]. The choice of the cooling thermo-fluid is also important, with suspensions of CuO [211], alumina [212], CNTs [213, 214; Cheng Z, SMIT Center, Shanghai University, 2008, Personal communication], and plasma-treated CNTs [215] in water all being tried. In the last case, the plasma treatment promotes a hydrophilic CNT surface. [211] analyzes CNT fin geometries. An air-jet-cooled CNT fin array is described in [216] with the mechanical reliability of the CNTs in this structure examined in [217].

A potentially revolutionary cooling system is described in [218], requiring three closed-end CNTs aligned end-to-end. Hot electrons, e.g., above the Fermi level, tunnel across a gap from the heated CNT to the "barrier" CNT where they lose energy before tunneling again to the third CNT which acts as a heat sink. In this way, energy is transferred from the heated CNT to the heat sink CNT via the barrier CNT. The principle is described in [219] and [220], and an alternative setup is proposed in [221]. The practical challenge would be the precise alignment and support of the CNTs.

1.4.4 Carbon Nanotubes: Electrical

The fundamental concepts of quantum conduction in CNTs are reviewed in [222].

An important development has been the ability to open CNTs after growth [168, 223, 224], since the open ends permit better wetting by Sn/Pb (and presumably other metals) for improved electrical contact. Au and Ag incorporation into CNTs and fullerenes has also been studied for electrical contacts with minimal galvanic corrosion [225]. Metal- and carbon-loaded polymers have long been used for high-frequency conductors in electromagnetic shielding, and both carbon fibers [226] and multi-walled CNTs have been studied in polymer matrices for the purpose [227–229], but CNT replacement of metal filler in isotropic conductive adhesives [230–232] does not even match the electrical conductivity of standard materials [232, 233]. However, 10–50 μm long Ag/Co nanowires of 200 nm diameter can be maintained in a parallel vertical orientation by a magnetic field, while polymer resin flows around them [234], to form an anisotropic conductive film for z-axis contacts [235–237]. CNT interconnection schemes are also under intense study [238–241], with μm-scale CNT bundles successfully developed as flip-chip "nanobumps" [242–244]. The expectation is that CNT bumps will outperform solder by being stress-free with no reflow step, by the absence of electromigration and by being more flexible. The mechanical reliability of CNTs as bumps and other forms of interconnect has been studied [217]. A "Velcro" form of CNT-to-CNT interconnect has been demonstrated [207], between CNT bundles on a flip chip and corresponding bundles on the circuit board, resistivities of 0.05–0.1125 Ω.cm having been achieved. Further in the future, RF wireless interconnect has been proposed using CNT antennas [245].

In a modeling paper [246], it has been shown that the increase in MWCNT conduction channels with temperature can offset the increased electron scattering to yield a negative temperature coefficient of resistance (TCR) for shorter MWCNTs up to ~1 to 10 μm long, depending on diameter.

A number of performance comparisons of CNT interconnects with Cu (and graphene) [247] have been made. The broad conclusion is that CNT interconnects, either MWCNTs or tight bundles of SWCNTs, are only competitive with Cu conductivity at longer lengths where the CNT ballistic length exceeds the electron mean free path in Cu [238, 248, 249] and for signal delay at ≥50–100 μm. These conductivity comparisons are typically made at DC, and it is the high-frequency performance that is more important for signal transmission.

Due to the high kinetic inductance, there is negligible redistribution of current at high frequencies, i.e., negligible skin effect, and the CNT bundle resistance does not increase at high frequencies as it does for Cu [250–252]. High-frequency CNT (and graphene) modeling is reviewed in [253] and [254] which also describe CNT implementations of capacitors and inductors.

A continuing problem with CNT interconnects, e.g., in TSVs, is the interfacial resistance to metallic conductors, which may make up 80% of the total interconnection resistance [255, 256]. The basic problem is that even a metallic CNT forms a Schottky barrier with the metal [168, 257] which may still provide an acceptable contact between high work function metals to p-type CNTs or low work function metals to n-type CNTs. Other techniques include deposition of graphene on the CNT as a graphitic interfacial layer [258] or rapid thermal annealing, possibly by Joule heating [259]. An AuPd alloy reportedly matches the CNT work function to achieve a low interface resistance [260]. A high resistance to Ti is attributed to oxidation, which is avoided by substituting TiN, achieving 0.59 Ω, but the deposition of Ti between the CNT and Cu apparently presents no problem as a top contact [261]. Ti/TiN is also used in [262] with an Al top contact. Ag, Au, and Pt contact resistances are reported in [263], which states that Ti, Cr, and Fe are better than Au, Pd, or Pt because of the work functions. In another work, Cr/Ni/Cu is sputtered on to the CNT ends, which then form a strong thermocompression bond to a Cu substrate [264]. The CNT resistance to Au can be reduced by about 11% by the electron beam-induced deposition of W [265], and the CNT can be welded on to a favorable metal for wetting the CNT, e.g., Ni, with the metal wetting the CNT, so C atoms are effectively embedded in the metal [266].

Most of the CNT interconnect studies above have been on free-standing vertical bundles, but these can also be encased in deposited silicon oxide or nitride with no ill effects [267]. There are also obvious benefits to encasing a vertically aligned CNT bundle in a metal, e.g., Cu, but also possibly Ni, Co, Fe, or Ag. After conformal deposition of pyrolytic graphite to stabilize the bundle, it is infused with a metal salt, which is reduced with H_2 [268].

With the current focus on packaging for 3D integration and chip stacking, it is a short hop from vertical CNT bundles for electrical connections to the more specific application in TSVs [269–272]. CNT TSVs (Fig. 1.3) [273] have been fabricated by various techniques [273–280]. The process generally follows a sequence of ion etching a blind via in the Si substrate with the subsequent deposition of a seed layer, usually of Fe nanoparticles, on the bottom of the via. The CNT bundle then grows on the seed nanoparticles by CVD from a suitable hydrocarbon gas. For SWCNTs, the diameter is controlled by the nanoparticle size. The top surface is then typically metallized or planarized, while the Si substrate is thinned from the back to provide access to the bottom of the CNTs. One of the most dramatic pictures in the literature is of a single 15 nm diameter MWCNT in a 35 nm via [281].

To compete with Cu TSVs' electrical properties, the CNT bundles need to be densified to provide as many CNTs per unit area as possible. In addition, CNT

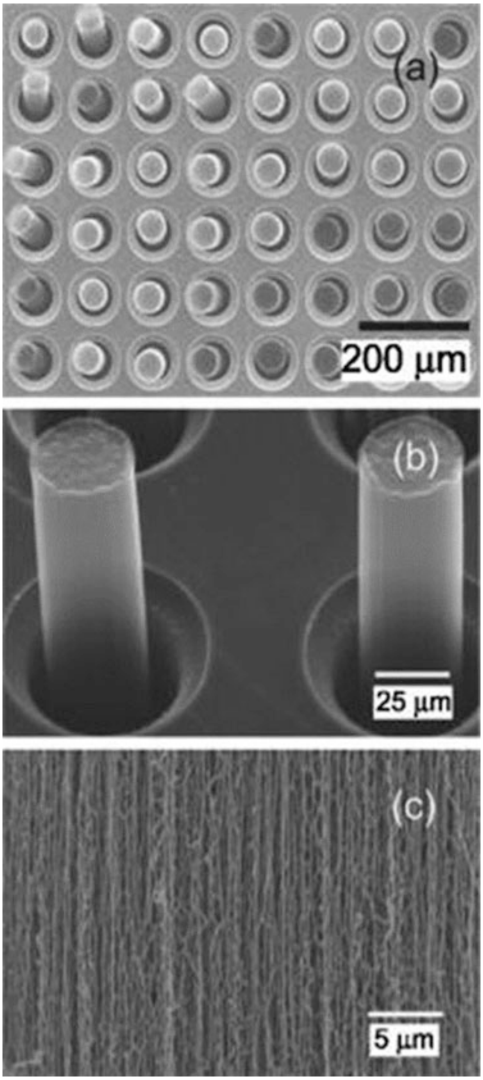

Fig. 1.3 CNT vias at various magnifications. (**a**) and (**b**) show CNT bundles in the vias, while (**c**) shows the CNTs in a bundle. (Reproduced from Xu et al. [273], with the permission of AIP Publishing)

growth in the blind via as described above limits the growth temperature and introduces unwanted defects into the CNTs. To combat both of these problems, CNTs have been grown as free-standing bundles, which were then densified and transferred to the target wafer by inserting them into the pre-etched vias [157, 158, 282–285].

There is no lack of electrical modeling of CNT TSVs [250, 286–293]. Some model a TSV pair as a transmission line [288–290], some present results in terms of scattering parameters [287, 291–293] while others focus on delay time and frequency response [290], but only a few address skin effect in the CNT TSV context [250, 287]. As mentioned above, the absence in CNTs of the high-frequency

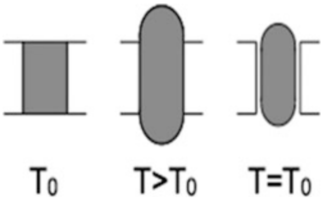

Fig. 1.4 Copper "pumping" in a TSV: as fabricated at temperature T_0; copper extrudes from the TSV at temperature $T > T_0$ due to the Si-Cu CTE mismatch; gap appears between the copper and silicon when the temperature returns to T_0 [294]

resistance increase in metals due to skin effect is a major advantage, besides which CNTs have demonstrated high current stability [154] due to the absence of electromigration. Electrically, the CNT TSV may not perform much differently than Cu- or W-filled TSVs, but there are further advantages from higher thermal conductivity and thermal stability [289]. This latter point comes from the issue in metal-filled TSVs of metal "pumping" (Fig. 1.4 [294]) which can open the via to moisture or fracture metal contacts at the ends, a problem due to the extreme CTE mismatch between Si and metals, and mitigated by CNTs' closer match to Si. It has been shown that stress at the surface of Cu TSVs is the result of this CTE mismatch and is largely absent in CNT TSVs [295].

The Cu-CNT composite TSV seems to be a logical step to combine the advantages with a vertically aligned CNT bundle embedded in Cu. The two main fabrication approaches, both by electroplating the Cu into pre-grown CNT bundles, are represented by [296] and [297]. In [296], the CNTs are grown in a blind via, and an electroplating solution is added after CNT densification, which promotes accessibility of the solution to the CNTs. In [297], the CNTs are grown and the TSVs etched separately; the CNT bundles are sputtered with Ti (10 nm) and Au (20 nm) before being threaded into the TSVs for electroplating. There was no densification step in order to preserve the CNTs' pristine state for the sputter deposition and Cu nucleation. In the first case [296], the TSV resistances were all greater than for the equivalent Cu TSV, possibly indicating incomplete Cu plating along the entire length of the via, although the Cu seemed to be as intended at both ends. In the second case, [297], the resistance was as calculated, with the Cu reducing the CNT bundle resistance.

In theoretical modeling of the high-frequency performance, the Cu still provides a skin effect, which is reduced by increasing CNT content [298]. The TCR is reduced in comparison with a Cu TSV, as expected, as is the CTE [297], with an order of magnitude less stress in the silicon. It has been shown that the axial CTE can exactly match silicon's, for zero Cu pumping, at 29% CNT content by volume [294]. At 29%, the radial CTE is also reduced to about 2/3 of the Si CTE. It has also been shown that for a similar Cu/CNT structure, but in thin-film form, the current-carrying capacity is increased by the CNTs to 100x the Cu value [299].

A slightly different Cu/CNT TSV was used in [300] to model its mechanical properties, namely, with a Cu cylinder surrounding a separate CNT bundle, under bending and thermal cycling. Another variation in the form of a tapered via has been proposed as more effective in the Cu electroplating step [301] and has been shown to provide a reduced delay over the cylindrical geometry, presumably due to the lower average capacitance, although the delays are slightly different depending on signal direction.

The electrical properties of CNTs (and graphene) are covered extensively in Chap. 27, and further coverage can be found in [302–310].

1.4.5 Nanowires

Nanowires are covered in Chap. 21 and in Chap. 22, which focus on anisotropic conductive film (ACF) applications and carbon nanofibers (CNFs) in [311]. CNFs cannot compete with CNT properties but have the advantage of lower synthesis temperatures. Applications include as ICA fillers [236, 237, 312–314] and for z-axis connections within ACFs [234, 315].

Ni nanowires have also been employed in a reusable test probe system [214] where a nanowire bundle is shown to have less contact resistance than a simple planar pad.

1.5 Graphene

1.5.1 Graphene: Introduction

Graphite has long been used as a lubricant, an electrical conductor (e.g., for the carbon arc in old movie projectors) and as a thermal conductor (e.g., in pastes) as well as in the ubiquitous “lead” pencils, and children learn in grade school that it lubricates because the single layers of carbon atoms can slide over each other. It was the painstaking exfoliation of those 2D planes of C atoms down to a single atomic layer that spawned the still expanding area of graphene research. In nanopackaging, there are three main application areas that exploit three main attributes: mechanical strength (mainly in composites) and high thermal and electrical conductivities. In addition, its impermeability provides possible applications as a diffusion barrier, e.g., to prevent the galvanic corrosion of Cu in contact with Ag-ICA [316].

Once graphene had opened up the concept of 2D atomic monolayers, the search began for others, most noticeably 2D Si (silicene), Ge (germanene), P (phosphorene), hexagonal-BN (h-BN), MoS_2, and (recently) Si_2BN [317]. Some of these are truly 2D, while others are buckled, i.e., the monolayer atoms are not actually coplanar.

See Chaps. 24 and 25 for more on graphene synthesis and characterization.

1.5.2 Graphene: Nanocomposites

The properties of graphene/polymer composites are reviewed in [318] and compared with CNT and silica nanoparticle (and nanoclay) polymer composites in [166] which are focused on mechanical properties. An intriguing concept is the application of dilute-functionalized graphene nanosheets as "self-healing" agents in a graphene/polymer composite to repair cracks and other defects under infrared laser irradiation [319].

1.5.3 Graphene: Thermal

The thermal properties of graphene are compared with those of other carbon allotropes in [320], which highlights the wide range of data in the literature. The paper notes that pyrolytic graphite challenges single crystal diamond's thermal conductivity at room temperature and above and leads one to conclude that graphite should not be ignored as a lower-tech lower-cost candidate for efficient electronics cooling. At 4000–6000 W/mK, graphene seems to display the most impressive potential, but these results, obtained for a single suspended sheet, are not maintained in contact with another material, even other graphene sheets. The results for suspended few-layer graphene (FLG) degrade to high-quality graphite's values (~2000 W/mK) at between three and four monolayers and to standard graphite values (~1000 W/mK) at eight monolayers, which is not surprising given that graphite is multilayer graphene. Single and FLG values range ~50 W/mK at 0.7 nm thickness to 1000 W/mK at 8 nm when sandwiched between dielectric layers as they would be in an on-chip or SiP heat-spreading scenario, i.e., less than graphite's 2000 W/mK.

It is noted in passing that the thermal conductivity of graphene with a reduced content of the ^{13}C allotrope (0.1% vs. the natural 1%) is increased by ~35% [321].

The conventional thermal dissipation pathways are metal, e.g., lead, tracks, vias, heat sinks, and thermal ladders, so it would be logical to try to improve their performance by adding graphene. The effects of oriented lamellar and randomly oriented single-layer graphene (SLG) and multilayer graphene (MLG) in Cu have been calculated, for both along and perpendicular to the graphene sheets in the lamellar case [322]. The effects are positive only for the lamellar SLG case along the graphene layer direction and for oriented SLG and MLG particulates. The mechanical properties and contact angle are improved by the addition of graphene sheets (decorated with Ni nanoparticles) to solder [323], as for CNT additives [Chap. 20, 132, 192].

Graphene sheets decorated with Ag nanoparticles have been added to Ag/epoxy ICAs with Ag flake/powder fillers to enhance the ICA thermal conductivity, reaching ~8 W/mK at 12wt.% graphene/Ag [324] and 3 wt.% graphene [325].

Porous heterostructures have also been developed. In one, conducting graphene and insulating h-BN foams are compared [326]. The foam is seated between the chip and circuit board and compressed to 1–2 μm thickness. The advantage of the nanoscale porous features and the compression is that excellent contact is possible at both surfaces, accommodating asperities and achieving thermal conductivities ~80 W/mK. In another approach, graphene is deposited on the surfaces of porous Cu, yielding ~210 W/mK [327] to ~230 W/mK [328].

Most predictions of graphene's function in chip/package cooling assume it will be in 2D heat spreaders for hotspot mitigation [329, 330]. In [331] and [332], silane-functionalized graphene oxide is inserted between the package hotspot and the graphene-based film to improve thermal contact. Graphene and h-BN heat spreaders are compared in [333]. The reader is referred to Chap. 27 for more details.

Graphene can be controlled as p-type or n-type depending on the polarity of a back-gate bias, so an effective PN junction can be created. With a PN junction, the possibility of thermoelectric cooling by the Seebeck effects becomes possible, as proposed in [334]. The thermoelectric figure of merit, ZT, is given by:

$$ZT = \frac{S^2 T}{\rho K_t},$$

where S is the thermoelectric power, T is the absolute temperature, ρ is the electrical resistivity, and K_t is the thermal conductivity. The problem is that K_t is high in graphene and also that ρ can be high due to surface scattering, both reducing ZT. It turns out that $ZT.K_t$ is greater in graphene on h-BN (e.g., on a 10 nm h-BN spacer) than on SiO_2, and the feasibility of Peltier cooling has been demonstrated [335]. The active cooling boosts the passive cooling of the structure by 10%.

Porous heterostructures have also been developed. In one, conducting graphene and insulating h-BN foams are compared [326]. The foam is seated between the chip and/or circuit board and compressed to 1–2 μm thickness. The advantage of the nanoscale porous features and the compression is that excellent contact is possible at both surfaces, accommodating asperities and achieving thermal conductivities ~80 W/mK. In another approach, graphene is deposited on the surfaces of porous Cu, yielding ~210 W/mK [325] to ~230 W/mK [328].

Chapter 27 covers the application of graphene in microelectronics cooling in more detail.

1.5.4 Graphene: Electrical

The theory behind the electrical properties of both CNT and graphene nanoribbon (GNR) interconnects is reviewed in [253] and [336, 337]. Theoretically the mean free path (ballistic length) of a GNR is $\lambda_{GNR} \approx 450w$, where w is the GNR width, but in practice λ_{GNR} ~1 μm due to defect scattering, but even for λ_{GNR} ~5 μm, single-layer GNRs could not compete with Cu interconnect. Moving on to multilayer GNRs (MLGNRs), there is the problem that they degrade to graphite for more than few layers. The solution is that the graphene layers must be kept apart in an intercalated structure. AsF_5 [253, 336, 337] and $FeCl_3$ [158, 338, 339] are mentioned. The in-plane resistivity of AsF_5-intercalated graphite is quoted as 1.6μΩ.cm, or a little less than Cu's with $\lambda_{GNR} = 1.03$ μm [253], with 21.45μΩ.cm for $FeCl_3$ [339] (or 20 Ω/square as a transparent electrode) [338]. The arguments pertaining to the kinetic inductance and skin effect mimic those for CNTs.

Graphene-wrapped Cu interconnects have been proposed with tri-layer graphene deposited on one, two, and all four sides of a square Cu conductor [340]. The current flows mainly in the central Cu at the ends due to higher graphene-Cu contact resistance than Cu-Cu but mainly in the graphene along most of the interconnect length, reducing the current density in the Cu and reducing the chances of electromigration failure. The graphene also conducts heat away from the Cu, further increasing reliability.

There are proposals in the literature for all carbon interconnects with MLGNR x-y plane tracks and CNT vias [158, 341]. Such a system would require making reliable low-resistance contacts from the CNTs to the graphene sheet, possibly by introducing defects into the graphene surface, e.g., by removing C atoms or depositing seed nanoparticles, and growing the CNTs from there. The electrical and thermal performances of such a MLG/CNT via system are simulated in [341] and compared with Cu.

At the "low-tech" application end, surface resistivities as low as 80 Ω/□ have been obtained by direct writing MLG flakes in quick-drying isooctane [342].

The electrical properties of graphene (and CNTs) are covered extensively in Chap. 27.

1.6 Nanoscale Structures

The incorporation of nano-diamond particles into an electroless Ni film coating on an electrothermal actuator [343] can improve cantilever performance by changing the thermal and mechanical properties. Sometimes one can get to the nanoscale by just continually shrinking existing technology, and in a truly impressive development, the micro-spring contacts originally developed at PARC-Xerox have been downsized to 10-nm-wide cantilevers, still 1 μm long, for biological sensing [344] (Fig. 28.14 in Chap. 28). Nano-imprinting technology is also being used to fabricate optical interconnect waveguides in organic PCBs [345].

1.7 Nano-interconnects

The "nano-interconnect" terminology is applied to interconnect structures which are clearly μm-scaled [346–353]. The ITRS Roadmap called for 20–100 μm pitch interconnects for nanoelectronics systems of feature size under 100 nm [349], which has prompted studies of nano-grain solders [346] or copper [348], nanocrystalline copper and nickel [349], and nanoscale via fillers [347], all for applications at around 30–35 μm pitch [346, 348]. Some nano-interconnect options are reviewed in reference [351]. Other technologies can be included in this group, too, e.g., metal-coated polymer posts on a similar scale [351] and embedded micro- or nano-electrodes for biological flow sensing [353]. Control of the interfacial surface charge on the nano-electrode in contact with the fluid can be used to control the flow [353]. Since the ITRS roadmapping program ceased, the IEEE Electronics Packaging Society (EPS, formerly CPMT) has undertaken responsibility for the electronics packaging roadmap with the Heterogeneous Integration Roadmap:

https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

There are many ways to fabricate metallic nanowires for interconnections, but one of the newest is to utilize DNA as a framework. The DNA is activated by metallic cations, and metallic nanoparticles are added by electroless deposition to form conducting Cu or Au nanowires of ~20 nm diameter [354, 355].

Skin effects are canceled for high-frequency interconnects by balancing ferromagnetic and non-ferromagnetic conductors within the contact [356]. A polymer doped with ferromagnetic material (e.g., Co, Ni, etc.) is electrospun onto a substrate seeded with Cu, and after suitable lithographic patterning, Cu is electroplated into the structure to form a porous contact.

1.8 Plasmonic Interconnects

As nano-CMOS circuits and devices shrink on-chip, so do the metal interconnection lines, increasing the resistance, R, and the RC_{gate} time constant becomes the limiting factor in circuit speeds rather than the transmission line delay. As a result, surface plasmon polariton transmission is being studied as an alternative to electronic conduction interconnects [357–359], since the wave rides on the metal surface (or at the metal-insulator interface) [360]. Even though interconnect cross section areas are greater at the package level than on-chip, the same problem is developing due to longer line lengths. Of course, with transmission lengths on the order of 10 μm before the signal needs a boost, the need for pumping/amplification [361] will be greater at the package level than on-chip. Nevertheless, if the technology is adopted on-chip, it will likely migrate to the package when mature. It is interesting to note that surface plasmon currents have been stimulated and observed in discontinuous nanoparticle films [362].

Plasmon/nanoparticle interactions are already being employed in electronics packaging [363]. If one of a number of fine-pitch pads or solder joints must be re-worked, it is decorated with Au nanoparticles on a graphene sheet carrier. These nanoparticles will be heated by the surface plasmons excited by laser irradiation, heating that specific pad/joint but leaving the neighbors unaffected.

1.9 Miscellaneous

A relatively new development is the application of biotechnologies to electronics packaging. Nanocellulose has been shown to be a suitable electronics substrate material, especially for flexible applications or where transparency is required [364]. The substrates have a smoother surface than the competitors', and the material assists in recycling components by being biodegradable, combustible, and readily disintegrates in water. Biosynthesis of Ag nanoparticles from $AgNO_3$, for example, can be accomplished by bacterial, fungal, or plant extract interactions, possibly assisted by microwaves, sonication, or heating [365]. In a third example, Ag^+ ions on polyimide are nucleated into nanoparticles by laser-assisted reduction in a mineral extract from spinach leaves in ethanol [366].

The Internet of Things (IoT) is projected to be the primary source of massive growth of the microelectronics industry in the near future. By and large, the system packaging technologies that will be employed here will be the same as those that are used in other applications, whether in the home, automobile, aircraft, industrial, or others. However, the IoT will push the development of nano-sensors which will have unique packaging challenges. But one of the recognized IoT challenges will be the proliferation of radio signals for reporting and control with an attendant risk of interference. So many system packages will need protection from electromagnetic interference by unwanted frequencies, e.g., by an array of ink-jet-printed and sintered nano-Ag band-reject antennas [367].

1.10 EHS: Environment, Health, and Safety

Much of the material being used in nanopackaging is nano-Ag, which has been used in various antibacterial and medical applications for centuries [365, 368], but the argument that therefore there should be no concerns about its growing use in other areas has been challenged [369]. Concerns are focused on the demonstrated toxicity to aquatic life and especially to embryonic fish and others at the bottom of the food chain [22, 370–372] although there is also concern about cellular effects in humans [373]. An industry perspective is found in [374]. Ag is not the only source of concern; a broader range is covered in [372], and nano-TiO_2 liver damage has been reported in [375].

CNTs have also been the subject of much study, again with concerns on cellular effects and the impact on aquatic life [376]. In this case, however, the similarities to asbestos mesothelioma are too obvious to be ignored, and pulmonary effects are the most studied [377], and following that analogy, distinctions must be drawn between the microphage ability to enclose and mitigate short CNTs or compact CNT bundles and the longer CNTs which cannot be surrounded [378].

See also Chap. 32.

1.11 Conclusion

The importance of nanoelectronics and "electro-nanotechnologies" in the future is sufficiently well recognized to have become the subject of industrial and government policy roadmaps [379]. Similarly, the academic world is responding with both undergraduate and graduate level courses and with textbooks. As for electronics packaging, the field requires students to be "subject multilingual" [380].

One of the surprising observations to come out of this survey, in full agreement with prior comment [381], has been that there is almost no work reported on the development of packaging for next-generation nanoelectronics technologies. The "nano-interconnect" work is directed toward continued Moore's law shrinkage of silicon (More Moore) or heterogeneous integration (More than Moore.) Candidate next-generation nanoelectronics technologies (e.g., single-electron transistors, quantum automata, molecular electronics, etc.) are generally hypersensitive to dimensional change, if based on quantum-mechanical electron tunneling, and this is just one example of how appropriate packaging will be essential to the success or failure of these technologies [382]. Packaging strategies must therefore be developed in parallel with the basic nanoelectronics device technologies in order to make informed decisions as to their commercial viabilities.

There has been a veritable explosion of research in the nanopackaging area since the first edition of this book appeared, and it is impossible to include it all here. Hopefully, the interested researcher can move backward and forward in time on a specific topic from the references in a specific paper and its later citations. There was a brief update to the first edition published [383], so most of its content has not been duplicated here. For future information in the field, the annual *IEEE Electronic Components and Technology Conference* (ECTC) and the nanopackaging sessions in the *IEEE International Conference on Nanotechnology* (NANO) and the *IEEE Nanomaterials and Devices Conference* (NMDC) are recommended.

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