James E. Morris *Editor*

Nanopackaging

Nanotechnologies and Electronics Packaging

Second Edition



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Foreword to the First Edition

Semiconductors entered the nanotechnology era when they went below the 100 nm technology node a few years ago. Today the industry is shipping 65 nm technology wafers in high volume, 45 nm is in production, with 32 nm working at the development stage. While the predictions that Moore's law has reached its practical limits have been heard for years, they have proven to be premature. And it is expected that the technology will continue to move forward unabated for some years before it comes close to the basic physical limits to CMOS scaling.

Consumers are becoming the dominant force for electronic products. The industry has learnt that the consumer market is driven by many factors other than CMOS scaling alone. Functional diversification, accomplished through integration of multiple circuit types, and different device types such as MEMs, optoelectronics, chemical and biological sensors, and others provide electronic product designers with different functional capabilities meeting the needs, wants, and tastes of consumers. This functional diversification together with cost, weight, size, fashion and appearance, and time to market are critical differentiators in the market place. These two technology directions are often described as "More Moore" and "More than Moore."

Packaging is the final manufacturing process transforming semiconductor devices into functional products for the end user. Packaging provides electrical connections for signal transmission, power input, and voltage control. It also provides for thermal dissipation and the physical protection required for reliability. Packaging governs the size, weight, and shape of the end product and is the enabler for functional diversification through package architecture and package design. In the new landscape of advancing device technology nodes and a dynamic consumer market place, packaging can become either the enabling or limiting factor. This market force has resulted in an unprecedented acceleration of innovation. Design concepts, packaging architecture, material, manufacturing process, equipment, and system integration technologies are all changing rapidly. Materials are at the heart of packaging technology. Packaging material contributes significantly to the packaged device performance, reliability, and workability as well as to the total cost of the package. With the driving forces from "More Moore" and "More than Moore," the challenges for packaging materials have broadened from traditional package requirements for future generation devices to include those for new package types, such as the system in package (SiP) families, wafer level packaging, integrated passive device (IPD), through silicon vias (TSV), die & wafer stacking, 3D packaging, and RF, MEMs, physical, chemical, and biological sensors, and optoelectronics applications. It is believed that materials in use today cannot meet the requirements of future packaging requirements. This is particularly true for complex SiP structures where hot spots, high currents, mechanical stresses for very thin die and ever shrinking geometries would require electrical, thermal, and mechanical properties that are beyond those of existing materials and manufacturing processes.

Nanomaterials and nanotechnologies promise to offer significant solutions toward packaging technology challenges in coming years. Carbon nanotubes (CNTs), nanowires, and nanoparticles have shown unique electrical, thermal, and mechanical properties orders of magnitude superior to current packaging materials used today. They have fired up the imaginations of engineers and scientists alike. How to design the next generation packaging materials and develop materials processing and application methodologies utilizing the nanomaterials' unique physical properties is an important question for the electronic packaging community.

Do CNTs have a place in future generation low dimensional thermal interface materials (TIM), smoothing out the hot spots and taking higher levels of thermal energy away from the die? How do we utilize the CNT electrical properties for future generation high density packages? What role will nanoparticles play in the new generation passives? How would macromolecules be designed into polymer materials to provide specific electrical, thermal, and mechanical properties required for the package function? With advances on the science and technology of nanomaterials, one envisions that whole new classes of materials will be introduced into the package features such as embedded and integrated passives, stacked and thinned dies, wafer level process, TSVs, MEMS, sensors, and medical and biochip applications.

This book is a compendium of in depth reviews written by some of the leading practitioners in the field. They cover the broad aspects of the field from materials preparations, materials properties, surface modifications, engineering applications, mathematical simulations, and "More than Moore" technical issues. It is a timely and important contribution to the technical literature for practitioners and researchers in the electronic industry field.

The editor of this book is a member of the IEEE Nanotechnology Council. Many of the contributors are from the IEEE/CPMT Society membership. They are to be

congratulated for bringing this very important topic forth in the timely manner for the benefit of the electronic packaging and materials community.

ASE Group, Santa Clara, CA, USA

William T. Chen

President, IEEE Components, Packaging, & Manufacturing Technology Society, Piscataway, NJ, USA October, 2007

Foreword to the Second Edition

Many technologically complex products today (e.g., smartphones, tablet computers, airplanes, etc.) already benefit from nanotechnology. There are also many "non-high tech" industries, such as plastics, textiles, plaster, lubricants, and athletic equipments, which have incorporated nanotechnology, including familiar products such as beer bottles and bandages. (Miller Brewing uses clay nanoparticles, which keep oxygen out and hold carbon dioxide in, to bottle its beer in plastic containers that prevent the brewed beverage from spoiling. Z-Medica uses aluminosilicate nanoparticles, which are inorganic specks derived from kaolin clay, to trigger the body's natural clotting process in order to stop nose-bleeds very quickly). Nanotechnology encompasses nanoscale devices, nanoparticles, nanocomposites, nanomagnetics, etc., which have already proliferated across applications such as medical diagnosis, healthcare, energy, integrated circuit technology, etc., and have benefited end-users from the electronics, pharmaceutical, biotechnology, and textile industries. It has been reported that the global nanotechnology market revenue is forecast to grow at 16.9% CAGR to reach \$12.83 billion by 2021.¹ In fact, the adaptation of nanotechnology into manufacturing has been compared to the advent of prior technologies that have transformed modern society, such as electricity, semiconductors, and plastics. By now, it is clear that nanotechnology will bring life-changing improvements in the performance of materials, electronics, displays, medicine, energy, machine tools, clothing, and many other areas in the near future.

Nanotechnology is likely to make discernable contributions to the semiconductor industry by transforming semiconductor devices themselves in terms of materials and fabrication processes. It is well known that we cannot shrink device dimensions ad infinitum. Once the device size approaches that of single atoms, quantum physics comes into play, i.e., a transistor may or may not switch, depending on the prevailing

¹"Nanotechnology Market – By Type (Nanocomposites, Nanofibers, Nanoceramics, Nanomagnetics); By Application (Medical diagnosis, Energy, ICT, Nano-EHS); By End – Users (Electronics, Pharmaceuticals, Biotechnology, Textile, Military) – Forecast (2016–2021)", report published by IndustryARC, May 18, 2016.

statistics, and thus, building traditional logic gates out of such devices is not sensible. Currently, for solid state memories, an important metric for the device material is the ratio of change between the 1 and 0 states. In a well-designed and fabricated flash memory, the ratio will be around 10,000. By exploiting phase change in graphene, it is theoretically possible to obtain ratios of conductivity over 1 million, which would result in a fivefold increase in storage capacity over today's memory devices.² Therefore, graphene is a potential nanomaterial to replace silicon and lead the semiconductor industry to long-term growth after the "End of Moore's Law."

As expressed by Dr. William T. Chen, who wrote the Foreword to the first edition of this book, packaging is the final manufacturing process transforming semiconductor devices into functional products for the end user. Packaging provides electrical connections for signal transmission, power input, and voltage control. It also provides for thermal dissipation and the physical protection required for reliability. Packaging governs the size, weight, and shape of the end practical device and is the enabler for functional diversification through package architecture and package design. Nanotechnologies have already offered significant solutions toward packaging technology challenges in the past decade. Carbon nanotubes (CNTs), nanowires, and nanoparticles have already shown unique electrical, thermal, and mechanical properties orders of magnitude superior to current packaging materials in laboratories worldwide. Activities to engineer and mass-manufacture nanomaterials with unique electrical, thermal, and mechanical properties for packaging applications will continue to proliferate among both the academic and practitioner communities in the field of electronics packaging in future decades.

In the near term, the most likely application of nanotechnology in the semiconductor industry is in the area of interconnects. CNTs and metallic nanowires have been found to have high electrical current density, with some nanowires theoretically possessing 1000 times greater current density than those of metals such as copper. On the other hand, graphene has been shown to have a resistivity of approximately $10^{-6} \Omega$.cm, which is lower than the resistivities of gold, copper, and silver. One of the major causes of power consumption and propagation delay in semiconductor circuits is the *RC* time constant of interconnects, i.e., the time required to charge a capacitor with capacitance *C* through a resistor with resistance *R*. Therefore, reducing the resistivities of materials will provide significant benefits to conventional semiconductors by reducing propagation delay.

This book is a compendium of in depth reviews written by some of the leading practitioners in nano-packaging, as Dr. Chen has pointed out in the first edition. This book covers broad aspects of the nano-packaging field from nanomaterials preparation, nanomaterials properties, surface modifications, engineering applications, and modeling and simulations. Since its first publication in 2008, this book is still a very important contribution to the technical literature for practitioners and researchers in the electronics industry today.

²http://electroiq.com/blog/2011/03/nanotechnology-for-semiconductors/ ("Nanotechnology for semiconductors", Giles Humpston, Tessera Inc., May 2011).

This book has some significant additions since the first edition, including several new chapters related to graphene, a nano-material that was not discussed in the original version. Graphene is one of the newest 2D materials that has brought scientists and engineers much excitement in the past decade (especially after A. Geim and K. Novoselov won their Nobel Prize in 2011.) Graphene is certainly as important to future nanoscale devices and packaging materials as CNTs, perhaps even more so. Specifically, this new edition includes 11 new chapters, including those on graphene, and other novel advanced packaging technologies such as "Applications of Bio-Nanotechnology to Electronics Packaging." This book has also updated 16 chapters from its first edition, including four completely rewritten.

Dr. James E. Morris, the editor of this book, who has been a key contributor to the IEEE Nanotechnology Council (NTC) in the past decade, should be congratulated for bringing so many world experts in the research and development of nano-packaging technologies to share their knowledge and expertise in this wide-ranging book on nano-packaging. Many of the contributors are also members of the NTC Technical Committee (TC) on Nanopacking and the IEEE Components, Packaging, and Manufacturing Technology Society (CPMT) TC on Nanotechnology, which serve as nano-packaging program committee members for the IEEE NANO and NMDC conferences. They should all be commended for pushing the frontiers of research and development of nano-packaging and for updating the contents of this book for the benefit of electronics and sensing materials and packaging communities.

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President, IEEE Nanotechnology Council, Piscataway NJ, USA May, 2017

Preface

This is the second edition of the Springer book of the same name published in 2008. It has been significantly updated with new material and expanded from 23 chapters to 32. A table identifying the new chapters, those updated and those remaining unchanged, is included at the end of the Preface.

The Preface to the first edition began with the comments that:

"Moore's Law has been remarkably effective over 40 years or so in predicting the march of CMOS technology, as device dimensions shrank to mils, to microns, to nanometers. With continued CMOS shrinkage projected to 20 nm, there is clearly continued life in the technology, despite past predictions of its demise which turn out to be, like Mark Twain's, greatly exaggerated. However, the day will clearly come when the physical device structure cannot be supported at near atomic dimensions, but despite concerted research, no obvious successor technology has yet emerged as a clear winner. One of the factors in identifying that technology must be consideration of packaging techniques and design for reliability. However, package design depends on the nature of the basic device technology, and the decision process goes in circles.

However, the rapid development of nanotechnologies in almost every branch of science and engineering is already yielding new approaches to packaging materials and techniques, and these should be well developed and compatible for the next generation of devices, whether they be single electron transistors, spintronics, carbon nanotube transistors, molecular electronic devices, or something not yet envisaged."

Most of these comments still remain valid, but nearly 10 years later the 20 nm CMOS node has come and gone, 10 nm nears mass production, 7 nm manufacturing issues are being debated, 5 nm is in research labs, and TSMC has announced the construction of a 3 nm fab! There was a flurry of news reports that Moore's law, actually a law of economics, had finally died with the 14 nm node with conjecture that the cost per transistor would not come down to less than for the preceding node and hence would find no mass market driver. However, Intel has assured us that all is well, and the transistor cost for the next node(s) will continue to drop (see figure below.)



But despite expectations, there is still no obvious consensus as to the technology which will take over from CMOS when the latter finally runs into its limits. So, there is still negligible attention being paid to the packaging reliability issues which would accompany any of the candidate technologies. However, while the packaging of novel nanoelectronic devices still receives scant interest, the application of nanotechnologies to current microelectronic system packaging problems is thriving. At the same time, many nanotechnology experts are still unaware of its possible applications in electronics packaging and system integration, and conversely, many packaging engineers are unfamiliar with the potential of nanoscale materials and devices. This book is intended to bridge that gap, with Chap. 1 introducing the scope of the field with a literature survey.

Then four chapters deal with computer modeling in nanopackaging. Bailey et al. take a high level approach to the modeling process in Chap. 2, backed up with multiple examples of nanoscale modeling in packaging, present and future, including nano-imprinting, solder paste printing and reflow, microwave heating, FIB milling, underfill, thermal interface materials, and anisotropic conductive film. Chaps. 3 and 4 from van der Sluis et al. deal with interfacial delamination, first by continuum modeling and then at the atomistic level by molecular dynamics, but also include other examples, e.g., sintering. Chap. 5 from Zhong et al. similarly applies both molecular dynamics and finite element modeling to nanoimprinting. The intention in each case is to understand macroscale package properties by modeling at nanoscale dimensions, with emphasis on the need to be able to transfer modeling results between software at different length scales.

The bulk of the book from here on splits naturally into five sections: nanoparticles, carbon nanotubes (CNTs), graphene, miscellaneous, and industrial.

Morris covers fundamental metal nanoparticle properties in Chap. 6, with introductions to melting point depression, the Coulomb block, interfacial diffusion effects, optical absorption, sintering, novel fabrication, etc. The references in this chapter intentionally include many from the earliest days on nanotechnology research, to make the point that much work was done before the current decade's surge of interest and funding. Nanoparticle fabrication is covered in Chap. 6 by Inoue et al., with emphasis on an ecologically friendly sono-chemical technique. Other fabrication methods are touched on in other chapters, including Chaps. 8 and 14.

The next three chapters consider nanotechnologies for passive devices, which are moving into the substrate as embedded components. The development of nanoparticle-based high-*k* dielectrics is covered by Lu et al. in Chap. 8, with consideration of the effects of both metallic and ferroelectric nanoparticles on material performance and a survey of commercial state of the art. At higher metal loading levels, the cermet (ceramic-metal or polymer-metal) materials become resistive, and cermets have been used as resistors in various applications for decades. The basic principle of operation balances the nanoscale effects of activated tunneling and percolation, as explained by Wu et al. in Chap. 9, which also includes a survey of commercial state of the art. Nanoparticle applications in passive components are rounded out by the Jha et al. Chap. 10 on inductors and antennas, which are essential to portable wireless systems. These are generally micron-sized devices with nanoscale features, e.g., size effects, surface roughness, and nano-granular materials (for which classical theory does not match the properties.)

Nanoscale engineering of isotropic conductive adhesives (ICAs) in Chap. 11, by Lu et al., covers both nanoparticle additives, low temperature nanoparticle sintering, CNT additives, etc., and enhancements by surface treatments. In Chap. 12, Paik and Suk describe an innovative technique to stabilize the conducting particles in anisotropic conductive adhesives with electrospun polymer nanofibers, and Chap. 13 by Das and Egitto deals with printed wiring board (PWB) microvias, and especially nanoparticle loaded fillers. Completing this group of four chapters, Felba covers nanoparticle-based PWB interconnect developments in Chap. 14, including progress toward printable and flexible electronics. This chapter emphasizes the role of nano-Ag sintering in this technology.

Soldering is the core technology of circuit assembly, so it is not surprising that researchers would explore the possible benefits of nanoparticle or CNT additives. As it turns out, Co, Ni, or Pt nanoparticles have some dramatic effects in limiting intermetallic compound (IMC) growth and hence mechanical failure by brittle fracture. These effects and others are covered by Amagai in Chap. 15.

Lall et al. describe the use of ceramic nanoparticle additives to lower the coefficient of thermal expansion in underfill in Chap. 16, the final chapter on nanoparticles. To model this effect, they also consider the problems of random distributions, viscoelasticity, etc. The work is extended to studies of encapsulated PWB reliability with and without the underfill.

The cluster of CNT chapters is introduced by two from the same authors. Various CNT fabrication techniques are reviewed in Chap. 17 by Shanmugam and Prasad who then follow-up with a review of basic CNT properties and applications in

Chap. 18, which provides a primer on some device research which parallels the work described in this book.

High CNT conductance suggests CNT-polymer composites for light weight electromagnetic shielding, and Cheng et al. present their work on the effectiveness of this technique in Chap. 19. Chap. 20 provides the CNT parallel to Chap. 15, with the account by Kumar et al. of the results of adding CNTs to both eutectic Sn-Pb and Pb-free solders, with the verdict that essentially every parameter of interest can be improved.

The subject moves from CNTs to nanowires in Chaps. 21 by Fiedler et al. and 22 by Razeeb et al. Chap. 21 includes both applications and fundamental problems, with an extensive bibliographic review. Chap. 22 returns to the area of electrically conductive adhesives (Chaps. 11 and 12) with the development of nanowire-based anisotropic conductive film.

In Chap. 23, Maffucci considers the potential use of both graphene and CNTs for electrical interconnect, and finally, in the CNT section, Chap. 24 by Liu and Wang turns to thermal applications with high thermal conductance CNT microchannel cooling and the thermal conductance of CNT bumps, with also a description of a novel thermal interface material.

Chap. 25 by Chung et al. and Chap. 26 by Chen et al. deal, respectively, with the fabrication and characterization and with the properties and applications of graphene. The primary interest in graphene for packaging in the near term is for its thermal properties, and Chap. 27 by Malekpour and Balandin focuses on graphene laminates and composites and on anisotropic heat spreaders.

Then Ma et al. introduce a novel stress-engineered cantilever technique to form free-standing interconnect wires (or springs) in Chap. 28. Micron-scale structures are described first, before demonstrating their reduction to the nanoscale. The concept of on-chip or in-package prognostics is becoming accepted, but requires appropriate sensors. Two of these are described by Morris in Chap. 29, the second in the "miscellaneous" category which is completed in Chap. 30 by Varga who introduces the concept of applying nano-bio-technology to electronics packaging.

Most of the work described in the book is still in the research stage, but it concludes with two chapters from an industrial perspective. With CMOS technology well into the nanoscale, current packaging problems are already nano-CMOS packaging problems. Chap. 31 by Mallik et al. presents an overview of these challenges in the context of continuing device shrinkage. Then, Trybula et al. close the book with Chap. 32 on the environmental impact and health and safety issues in nanomanufacturing.

Most chapters include a focus on the authors' own research in each respective field, but all end with extensive reference listings. The intentions of the book are to present an overview of each topic area, usually with the deeper treatment of one particular aspect, and especially to provide the reader with a resource for future study of those of interest. Hopefully, the book will pique such interest.

Second edition chapter	First edition chapter	Status
1	1	Expanded
2	2	Updated
3	4	New
4		
5	3	New
6	5	Updated
7	6	Updated
8	7	Expanded
9	8	Expanded
10	9	Updated
11	10	Updated
12	N/A	New
13	11	Unchanged
14	12	Revised
15	13	Unchanged
16	14	Expanded
17	15	Revised
18	16	Expanded
19	18	Updated
20	19	Unchanged
21	20	Unchanged
22	N/A	New
23	N/A	New
24	17	Unchanged
25	N/A	New
26	N/A	New
27	N/A	New
28	21	Unchanged
29	N/A	New
30	N/A	New
31	22	Revised
32	N/A	New

Portland, OR, USA

James E. Morris

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Chapter 1 Nanopackaging: Nanotechnologies and Electronics Packaging



James E. Morris

1.1 Introduction

Level one electronics packaging is traditionally defined as the design and production of the encapsulating structure that provides mechanical support, environmental protection, electrical signal and power I/O, and a means of heat dissipation for the Si chip, whether digital or analog, processor, or memory. Level two packaging is then the integration of these packaged chips into a board-level system that similarly provides mechanical support, power and signal delivery and interconnections, and thermal dissipation. Of course, nowadays the chip is often mounted directly on the board (chip-on-board, direct chip attach, flip chip), and the packaging process actually begins with the chip fabrication (wafer-level packaging), e.g., with solder bumping. The underlying principles of the field are covered in textbooks [1-3], and a multitude of others, e.g. [4], are more research focused. The field is inherently multidisciplinary with electrical, mechanical, and thermal design at its core, with all of these subject to reliability studies and material selection. Figure 1.1 shows the history of the electronics package from the vacuum tube to a multi-chip "system in a package" (SiP). The package has always been the limiting factor to system performance, i.e., the Si chip can operate at higher frequencies than the package.

Current issues facing the electronics package designers include:

- Thermal dissipation
- High temperature and power applications. (This is driving transient liquid-phase soldering/sintering (TLPS) joining, which enables high-temperature intermetallic compound (IMC) alloy joints from low-temperature processing of low melting point materials.)

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Fig. 1.1 The evolution of electronic assembly. (Joe Fjelstad, with permission)



- Embedded passives. (Traditionally, most of the printed wiring board (PWB) surface is taken up by many passive components. Embedding them inside the PWB would release surface area for more active Si-integrated circuits (ICs).)
- 3D system integration. (Chip stacking drives through silicon via (TSV) technology (Fig. 1.2).)
- Heterogeneous system integration. (More than Moore implies the integration of unlike technologies, e.g., random logic, memory, microelectromechanical systems, optical and RF communications, etc., in a SiP enabled by chip stacking.)
- Flexible electronics includes both wearable and robotic systems.
- No-Pb solder. (The prevalent no-Pb solder is Sn-Ag-Cu (SAC), which melts at higher temperatures than traditional eutectic Sn-Pb solder, exacerbating electromechanical stresses in the package and failures, creating interest in lowertemperature solders and sintering.)

It often seems that the promise of nanotechnology's impact on everyone's quality of life is as over-hyped as past promises of endless cheap energy from cold fusion and high-temperature superconductivity. But there are two major differences. While the term "nanotechnology" has caught the attention of industry, legislators, and research funding agencies, in most cases the technologies in question are rooted in steady research progress in the field in question, as fabrication and characterization techniques have steadily conquered ever smaller dimensions, with the parallel development of theory to explain and model the new phenomena exposed. Furthermore, nanotechnologies have already yielded everyday consumer benefits beyond stain-resistant clothing and transparent sunblock. So it is hardly surprising to discover active research and development programs in nanotechnology applications to electronics packaging, with special nanotechnology sessions at electronics packaging research conferences and research journal papers demonstrating the range and progress of these applications.

The definition of nanotechnology is usually taken to be where the size of the functional element falls below 100 nm or 0.1 μ m, and with 10 nm node CMOS devices upon us, we are already well into the nanoelectronics era. Furthermore, with metallic grain sizes typically below this limit, one might also argue that solder has always qualified as a nanotechnology, along with many thin-film applications. So, the requirement that the specific function depends upon this nanoscale dimension is conventionally added to the definition. According to this *caveat*, MOSFET technology, for example, would not qualify by simple device shrink but would at dimensions permitting ballistic charge transport.

New nanoscale characterization techniques will be applied wherever they can provide useful information, and the atomic force microscope (AFM), for example, is relatively commonly used to correlate adhesion to surface feature measurements. More recently, confocal microscopy has been applied to packaging research [5], but it is especially interesting to note the development of a new instrument, such as the atomic force acoustic microscope [6], which adapts the AFM to the well-known technique for package failure detection.

1.2 Computer Modeling

The use of composite materials is well established for many applications, but while overall effective macroscopic properties are satisfactory for computer modeling of automotive body parts, for example, they are clearly inadequate for structures of dimensions similar to the particulate sizes in the composite. The modeling of such microelectronics (or nanoelectronics) packages must include two-phase models of the composite structure, and this general principle of inclusion of the nanoscale structural detail in expanded material models must be extended to all aspects of package modeling [7]. The extended computer models can be based on either the known properties of the constituent materials (and hopefully known at appropriate dimensions) or the measured nanoscale properties (e.g., by a nano-indenter [8, 9] or

AFM [10]). Molecular dynamics modeling software has been particularly useful in the prediction of macroscale effects from the understanding of nanoscale interactions [11]. Computer modeling is covered in more detail in Chaps. 2, 3, 4, and 5.

1.3 Nanoparticles

1.3.1 Nanoparticles: Introduction

Nanotechnology drivers are the varied ways in which material properties change at low dimensions. Electron transport mechanisms at small dimensions include ballistic transport, severe mean free path restrictions in very small nanoparticles, various forms of electron tunneling, electron hopping mechanisms, and more. Other physical property changes going from the bulk to nanoparticles include:

- Melting point depression, i.e., the reduction of metal nanoparticle melting points at small sizes [12], although this is unlikely to be a factor in packaging applications with even 10% reductions typically requiring dimensions under 5 nm [13]
- Sintering by surface self-diffusion, which is thermally activated, with net diffusion away from convex surfaces of high curvature [14]
- The Coulomb blockade effect, which requires an external field or thermal source of electrostatic energy to charge an individual nanoparticle and is the basis of single-electron transistor operation [15]
- Theoretical maximum mechanical strengths in single grain material structures [16]
- Unique optical scattering properties by nanoparticles one to two orders smaller than the wavelength of visible light [17]
- The enhanced chemical activities of nanoparticles, which make them effective as catalysts, and other effects of the high surface-to-volume ratio

Chapter 6 considers nanoparticle properties in more detail.

1.3.2 Nanoparticles: Fabrication

Noble metal nanoparticles have been fabricated by an ultrasonic processing technique [18] and Ag/Cu with "polyol" [19]. Alternatively, a precursor may be used, e.g., AgNO₃ for Ag nanoparticles, and there are techniques to control the particle shapes, e.g., spherical, cubic, or wires [20]. Good dispersion and smaller nanoparticles are achievable with ~60 MHz ultrasonic agitation [21]. Nanoparticle fabrication is reviewed in Chap. 7 and specifically Ag nanoparticle fabrication in [22].

1.3.3 Nanoparticles: Embedded Capacitors

For a planar capacitor of dimensions L_x , w_y , and t_z in the x, y, and z directions, respectively, the capacitance, C, between metal contact plates of area $L_x x w_y$ at z = 0 and $z = t_z$ (for $t_z \ll L_x$, w_y) is $C = \varepsilon(L_x x w_y)/t_z$ where ε is the dielectric constant. In microelectronic systems, substrate area is precious, even when one can move passive components from the PWB surface. To increase C for a given area ($l_x x w_y$), one must shrink the thickness t_z . As t_z approaches the nanoscale, any particles in a composite dielectric must be smaller still.

The move toward embedded passive components at both on-chip and PWB levels has also prompted a search for high dielectric constant materials for low area capacitors. High dielectric constants can be achieved by the inclusion of high dielectric constant particulates and minimal thickness. The latter requirement pushes one toward nanoscale particulates, with examples of the former covering ceramic [23–26], silicon [27], and metal [28–32]. The ceramic particles are generally barium titanate, e.g., applied to organic FETs with composite k around 35 [24]; in such materials, the particle surface energy must be reduced to avoid aggregation [25].

The target *k* is 50–200, and while k~150 has been achieved, it is at the expense of high leakage (dielectric loss.) Similar structures have been studied in the past as "cermets," (ceramic-metal composites,) for high-resistivity materials for on-chip resistors [33], which conduct by electron tunneling between particles. At low fields, the nanoparticles can act as Coulomb blocks to minimize DC leakage if they are sufficiently small [27], but still do not eliminate it at finite temperature [34]. It is the AC performance which is more important, however, and inter-particle capacitance will bypass the block unless pseudo-inductive effects develop at capacitor thicknesses which permit even short nanoparticle chains [35].

An alternative approach to leakage is to use aluminum particles, to take advantage of the native oxide coating [30], with $k\sim$ 160 achieved [31]. Ag/Al mixtures have also been studied [32].

Design, fabrication, and testing of commercial BaTiO₃-based embedded capacitors are described in [36], while [37, 38] describe two alternative techniques for embedding the BaTiO₃ particles in the polymer. In [37] hyperbranched polymer shells are formed around the nanoparticles with methyl methacrylate added to enhance cross-linking between them, and in [38] the composite is formed by electrospinning polymer fibers containing the BaTiO₃. (Electrospinning is described in Chaps. 12 and 21). In [39] the BaTiO₃ is in the form of nanorods. Smaller BaTiO₃ nanoparticles (~6 nm) exhibit higher breakdown strengths and lower loss factors than larger ones (~90 nm) but with lower dielectric constants [40].

See also Chap. 8.

1.3.4 Nanoparticles: Embedded Resistors

See also Chap. 9.

For the same dimensions as specified for the capacitor above, the resistance, R, of an embedded resistor is $R = \rho L_x /(w_y x t_z)$, where ρ is the resistivity, often written $R = (\rho/t_z) x (L_x/w_y)$, where ρ/t_z is termed the surface resistivity in Ω /square and L_x/z w_v is the number of "squares" along the length L_x of the resistor. Again, to minimize the x-y area, the thickness t_z is driven down to the nanoscale for high surface resistivities with a low (ideally zero) temperature coefficient of resistivity (TCR) being also required. Thin-film resistor materials include alloys (e.g., Ni/Cr, Ni/P), polymer or ceramic/metal composites (cermets) (e.g., C/epoxy, Cr/SiO₂), conducting polymers (e.g., coating various filler nanoparticles [41]), and others such as TaN [42, 43]. The ratio of TaN to Ta_3N_5 can be controlled by the N_2 in the sputter deposition chamber, affording some control of the TCR <0. Most cermet films balance the positive TCR of a continuous metallic percolating cluster phase against the negative TCR of an electrostatically activated tunneling process between isolated nanoparticles. In a Ag/Ta₃O₅ cermet [44], a large negative Ta₃O₅ TCR is transformed into a near-zero positive TCR by the Ag content, apparently even as isolated nanoparticles.

Note that thermally conductive materials have very similar structural requirements to the passive components, with metallic or SiC nanoparticles as fillers [45].

1.3.5 Electrically Conductive Adhesives

The addition of smaller µm diameter silver powder to 10 µm silver flakes in isotropic conductive adhesives (ICAs) reduces resistance by inserting bridging particles between the flakes. The simple addition of nanoparticles does not improve conductance, due to mean free path restrictions and added interface resistances, and the same principles limit the performance of alumina-loaded thermal composites [46]. The addition of silver nanoparticles does achieve dramatic reductions, however, by sintering wide area contacts between flakes [47], a principle also applicable to via fill [48, 49]. Filler nanoparticle sintering can also improve anisotropic conductive adhesive performance [50], aided by contact conductance enhancement by the addition of self-assembly molecular surface treatments [47, 51, 52]. Sintering effects have also been shown to improve contacts in materials with sufficiently low filler content as to be regarded as non-conductive adhesives [53]. When silica nanoparticles are added to a Cu-powder/Cu-epoxy ICA [54], they can inhibit crack propagation and improve adhesive strength. Ink-jet printable adhesives [55] would be another significant step forward, possibly achievable with nanoscale fillers that are less likely than micro-flakes to clog nozzles.

Nanoparticles in ICAs and anisotropic conductive adhesives (ACAs) are considered further in Chaps. 11 and 12.

1.3.6 Nanoparticles: Sintered Interconnect

Surface electrical interconnect for board and package levels can be achieved by screen printing and sintering nanoscale metal colloids in suspension [56–58], and now ink-jet-printed conductors are relatively routine, especially for flexible polymer substrates [59–61]. Electrical continuity is established by sintering, e.g., of 5–10 nm silver particles [62–65], and sintering may be accomplished at room temperature [66–68], by laser [69] microwave [60] or oven heating, or by plasma immersion [59]. Resistivities as low as around 4–6 $\mu\Omega$.cm are achievable by annealing at 200–300 °C [70, 71]. Lower-temperature processing is important for polymer/flex substrates [72, 73] but results in higher porosity [74, 75], which translates to higher resistivities [61]. The changing electrical and mechanical properties as the sintered material is aged or stressed have been correlated with changing pore sizes and shapes [76–79].

Stretchable circuits are more than just flexible and are directed more to wearable applications but can still find applications in packaging. Ag nano-ink can be stamped on a stretchable substrate in conductive horseshoe chain patterns that can stretch like a concertina [80] with less than 10% resistance increase at 50% strain. The traditional bimodal Ag flakes and nanoparticle filler are compared with nanowire and dendrite fillers in polyurethane in [81].

Sintered Ag nanoparticles can also be used for die-attach [82] or thermal interfaces [83–85]. In the last example, 10 nm Ag nanoparticles nucleate on the surface of Ag-oxalate microparticles and bond by sintering, achieving thermal conductivity of 100 W/mK [85]. As a variation, magnetic composite films (e.g., of Co/SiO₂ in BCB and Ni/ferrite in epoxy) have been screen-printed for antennas [86]. Sn/Ni bumps have also been grown on Sn from a nanometer Ni slurry [87]. Ag nano-ink deposited on a stepped via [88] has proven to be more resistant to shrinkage and cracking than in a simple barrel via [89].

With maturity of the nano-Ag technologies, attention has switched to the possibility of sintered copper interconnects, which offer a cheaper alternative to Ag, but with the problem of oxidation, since unlike the silver oxides, the copper oxides are insulating. Again, the emphasis is on flexible polymer substrates [72, 73], and the research extends, for example, to Ag-coated Cu nanoparticles [71]. Generally, the oxide problem is avoided by nanoparticle fabrication in solution and processing in controlled inert atmospheres [90, 91] or by using the surface oxide as a temporary protective coating [92]. In other cases, e.g. [93], the solution chemistry can provide a protective organic coating automatically. As with ICAs, a bimodal distribution of copper nanoparticles and microparticles can yield lower resistivities than either alone [94, 95].

With copper interconnect prevalent on-chip, and growing interest in 3D chip stacking, copper nanoparticles are finding application in direct Cu-Cu bonding, with sintered nanoparticles bonding to each face [96–100]. Silver nanoparticles have also been used for Cu-Cu bonding [101, 102] but of course run the risk of Kirkendall voids.

An innovative interconnection technology based on nanoporous materials is described in [103, 104]. In these papers, the Ag is etched out of an Au/Ag alloy leaving a porous sponge-like structure of Au behind. Two such porous contacts can bond at low pressure (10 MPa) and low temperature (200 °C) with "a similar characteristic as sintering processes" [103]. More recently, the concept has been extended to nanoporous Cu contacts synthesized from a Cu/Si alloy which is sintered in a N₂ atmosphere [105].

The field of sintered nanoparticle interconnect has been reviewed recently in [106] and in Chaps. 13 and 14.

1.3.7 Nanosolder

Often, "nanosolder" papers turn out to be about sintered interconnects, but there are examples on nanosolder in the literature, based on true melting point (MP) depression. Second-order effects include shape dependence of the decreased and increased coefficient of thermal expansion (CTE) at smaller nanoparticle sizes [107, 108]. For the case of a disk-like nanoparticle of radius r_d and thickness t of equal volume to a sphere of radius r_s , the shape factor, defined as the ratio of the projected surface areas of the disk and sphere (to normalize the ratio = 1 for the sphere), is $r_s/3$ t. Clearly, the minimum particle dimension controls the MP reduction because of the disordered surface layer thickness. For a disk of thickness t ~ $r_s/$ 5~5 nm, the disk MP reduction is 25% rather than 10% for a 5 nm radius spherical particle. For similar reasons, the CTE of a 2.5 nm diameter spherical Fe particle increases by about 60% with further increases for shape factors >1.

The MP depressions of solder alloys follow the same trends as for metals [109]. Solder alloy nanoparticles have been fabricated and the MP and other properties determined [110–113], generally agreeing with theory at 5 nm and 20 nm radii. Interestingly, the solidification temperature for a nanoparticle of given size is less than the MP, and the variation with size is less marked [114]. In a dynamic nanosoldering operation though, with a paste containing multiple nanosolder particles, coalescence increases both the solidification and melting temperatures as the particles increase in size. Koppesa et al. [115] demonstrates the process as the temperature is raised in steps. It is not clear that there is any MP depression advantage in this case or in [116]. Ideally, one should be able to take advantage of the shape factor MP depression to use solder nanowires as a low-temperature solder source [117, 118], but at 50 nm diameter [119], there is still unlikely to be much MP depression advantage. However, in this case the temperature was raised by Joule heating, which could provide a different advantage for solder nanowires.

As an alternative to soldering, transient liquid-phase sintering/soldering (TLPS) has been demonstrated for joining Si wafers for 3D integration by a Cu nanorod/Sn/Cu structure [120–122] with a fundamental process study in [123]. In this process, solid-state diffusion leads to a high-temperature Sn/Cu IMC. Ag-nanowire bonding has been demonstrated by solid-state wetting and subsequent atomic diffusion between the nanowires [124].

1.3.8 Nanoparticles in Solder

The addition of Pt, Ni, or Co nanoparticles to no-Pb Sn-Ag-based solders [125, 126] eliminates Kirkendall voids, reduces intermetallic compound (IMC) growth, and reduces IMC grain sizes, significantly improving drop-test performance [127]. Similarly, Ni or Mo nanoparticles promote finer grain growth, increased creep resistance, and better contact wetting [128]. Nanoparticles in the grain boundaries also inhibit grain boundary sliding and thermomechanical fatigue, but a similar function can be provided by 1.5 nm SiO_{1.5} polyhedral oligomeric silsesquioxane structures with surface-active Si-OH groups [129]. One hundred nanometer Zn nanoparticles were added to non-conductive films employed in Sn-Ag soldering of Cu pillars to lower intermetallic compound (IMC) formation [130], but note that Amagai found no IMC reduction with Zn addition to solders [127, Chap. 15].

Other nanoparticles added to solder include Ag and TiO₂ for improved substrate wettability and adhesion [131–133], alumina [134], silica, diamond, Bi₂Te₃, and La₂O₃ for mechanical strength [135–138]. The TiO₂, diamond, and Bi₂Te₃ also inhibited IMC formation, while the La₂O₃ also improved wettability and thermomechanical reliability, as demonstrated by resistance to thermal shock. The silica was bound to the solder matrix with POSS trisilanol [135]. Ag nanoparticles can precipitate out of the solder matrix, degrading the solder joint over time [139]. The effects of nanoparticles in solder have been reviewed in [140].

1.3.9 Nanoparticles: Nanocomposites

The key advantage of nanoscale silica particles in flip-chip underfill formulations is that they resist settling [141]. They also scatter light less than the larger traditional fillers, permitting UV optical curing and providing a dual photoresist function from a single material [142] and other advantages of optical transparency [143]. The higher viscosity of the nano-filled material can be reduced by silane surface treatments [144]. Further improvement is possible with a subsequent second layer [145]. Mesoporous silica, where the μ m scale aggregates are characterized by a high nanoscale surface-to-volume ratio, has also been shown to be better than similarly sized solid particles [146]. One hundred nanometer silica particles have also been incorporated into a non-conductive film, which effectively serves as an underfill [147]. Underfills also serve as thermally conductive paths, and the thermal conductivity can be raised an order of magnitude by the addition of 10 nm Ag nanoparticles to underfill with 10–40 µm silica, BN, or diamond fillers to provide enhanced thermal contact between the larger particles [148]. Fabrication involves nanoparticle self-assembly to create the inter-particulate necks.

Nanoparticle-filled composites can be used as encapsulants. The addition of a bimodal dispersion of $8-10 \,\mu\text{m}$ bentonite with 12 nm SiO₂ to epoxy slows moisture absorption in a humid environment significantly [149]. Two to six nm nanoparticles

of TiO₂ in a silicone LED encapsulant increase the refractive index and reduce the internal reflection light at the GaN/encapsulation interface [150]. A silica bimodal distribution of 1 μ m SiO₂ powder and \leq 50 nm nanoparticles has been laminated with a resin film to form circuit boards that outperform the traditional FR-4 in CTE, storage, and flexural moduli and warpage [151].

1.4 Carbon Nanotubes (CNTs)

1.4.1 CNTs: Fabrication

CNT growth can be accomplished for both electrical and thermal applications by chemical vapor deposition [152], with satisfactory solder wetting of the CNTs for electrical contacts. One usually requires bundles of aligned CNTs, whether large or small diameter SWCNTs (single-wall CNTs) or MWCNTs (multiwall CNTs.) The bundles morph from SWCNTs to MWCNTs as one increases the catalytic particle sizes to grow larger diameter SWCNTs, and small diameter SWCNTs need low growth rates [153]. Similarly, bundle densities are limited at the low end by alignment limitations and at the high end by achievable catalytic particle densities [153]. 950 °C is usually quoted as the minimum growth temperature for SWCNTs, with lower values quoted for MWCNTs. In fact, SWCNTs can be grown at lower temperatures (down to $365 \,^{\circ}C$ [154]) but at the expense of greater defect densities.

One approach to minimizing CNT bundle resistance and maximizing current density, given the practical constraints above, is to densify the bundles post-growth. This is usually accomplished by some sort of organic liquid/vapor [155–158], but deposited solid-phase materials have been demonstrated too [159].

Most fabrication techniques yield vertical z-axis interconnect bundles, but for horizontal (x- or y-axis) interconnects, one can either realign a vertical bundle by liquid surface tension [160] or grow the bundle in a horizontal electric field at the outset [161].

CNT synthesis and characterization are covered in Chaps. 17 and 18.

1.4.2 CNTs: Composites

CNT/polymer composites have potential electrical, mechanical, and thermal applications in electronics packaging [162]. The key to achieving the target properties in such composites is effective random CNT dispersion, requiring a suitable choice of liquid agent [163], ultra-sonication [164], MHz sonication with an AC electric field [165], or similar techniques. The primary result of such composites is an improvement in Young's modulus [164] and other mechanical properties [166], but the combination of CNTs with carbon microfibers can be much more effective [167]. For electrical applications of randomly dispersed CNT/polymer composites, one needs good electrical contacts between the cylindrical CNT surfaces [168]. Modeling can include CNT volume fraction, diameters, and lengths to determine the percolation threshold [169], but it has been shown that CNT flexibility must be taken into account [170]. Also, the CNT-CNT contact resistance is typically unknown in such simulations. Experimentally, the CNTs can be coated with Ag, for example, to reduce this resistance [171]. When CNTs are added to a conventional Ag-loaded ICA, electrical and thermal conductivities and reliability lifetime can all improve [172]. Acid etching the CNTs to introduce surface defects before mixing to form a CNT/alumina composite further improves the mechanical properties [173], and the same effect is expected with polymers with the defects improving CNT-matrix bonding.

CNTs have also been mixed with carbon black in PDMS to provide low-resistance flexible electrodes (up to ~80% strain) for wearable microsystems [174].

If an aligned CNT/polymer composite is required, the polymer would have to be infiltrated around the CNTs of a previously grown bundle. Studies have shown that capillary forces can buckle the CNTs if the bundle is too long, or the CNTs are too close together, or the (MWCNT) walls are too thin [175].

There is growing interest in CNT/metal composites for a variety of applications [176, 177]. These include random CNT distribution within, for example, copper interconnects for increased resistance to electromigration [178], which should work for solder too. Another source of interest lies in the possibility of reducing the coefficient of thermal expansion (CTE) of metals in the package, especially of electrical interconnections of various types [179]. A major cause of package failures is due to the thermal mismatch between the silicon chip and both metals and polymers. CNTs (and graphene) have negative CTEs around 300 K, depending on chirality and diameter, with different figures for axial and radial CTEs [180]. The inclusion of randomly dispersed or aligned CNTs within a polymer, or more likely at higher densities within a metal conductor, has the potential to reduce the CTE mismatch to Si significantly, possibly even achieving a match.

Most of the interest in CNT/metal composites is for copper, but Ag/CNT composites have been made for interconnects on highly flexible substrates by the heterogeneous nucleation of Ag nanoparticles on CNTs [181]. Further growth of the Ag bonds the CNTs together, retaining the flexibility to survive longer flex cycling at lower resistances than conventionally deposited Ag films. Similar processes, e.g., electroless deposition, have been used to metallize CNTs to form hybrid CNT/Cu nanowires [182–184]. Printed Ag/CNT composites (Ag flakes-/Ag nanoparticle-decorated CNTs) have been demonstrated for conformally coated contacts and TSV fillers [185].

In CNT/Cu composites, the mechanical properties are regularly improved [186–189], but both decreases [187] and increases [188, 189] in electrical and thermal resistivities have been reported.

The addition of carbon nanotubes (CNTs) to solder can also have beneficial effects, e.g., 30–50% improvements in tensile strength [126, 190] and a 40%

increase in reliability lifetime with an aligned CNT structure [191]. Both increased [192] and decreased [132] wettabilities have been observed.

Aligned CNT/Cu composites are attracting interest for 3D TSV interconnections for chip stacking; this topic is explored below.

1.4.3 CNTs: Thermal

The high thermal conductivity of CNTs is being exploited for microelectronics chip cooling both directly in conductive cooling and indirectly in convective cooling systems [193, 194]. It appears that aligned CNTs offer the best hope for an order of magnitude improvement over current thermally conductive materials [195]. The thermal properties of vertically aligned CNT systems are being studied [196-198]. For conductive systems, the key is to establish CNT alignment [190], since the thermal conductivities of random arrays (of CNTs and carbon fibers alike) fall far short of expectation, showing no advantages over conventional materials, often also because of CNT fracture at the substrate [199]. In one of the most advanced techniques, vertical CNTs are first grown on both the aluminum heat sink and silicon chip surfaces, which are then positioned ~µm apart in a CVD furnace, enabling the CNTs from the two surfaces to grow further and connect with each other [190]. Composites incorporating CNTs have also been studied for thermal interface materials, e.g., CNT/carbon-black mixtures in epoxy resin [200]. The use of a liquid crystal resin matrix can impose structural order on the CNT alignment to yield a sevenfold improvement in thermal conductivity [201]. Electrospun polymer fibers filled with CNTs, or with SiC or metallic nanoparticles, have shown advances in both mechanical and thermal properties [202, 203].

So far, convective CNT cooling has been limited to the use of µm-scale clusters of vertically grown nanotubes [204-206]. These clusters define micro-channels for coolant flow which look very much like the metal or silicon cooling fins they aim to replace (Fig. 7 in Chap. 24) with similar thermal performances. The problem is that the flowing coolant is only in contact with the outermost CNTs of the clusters, and the internal CNTs are separated from each other. The system has been modeled [193], and one solution is to spread the CNTs apart to permit coolant contact with each one [204], but another is to thermally connect the CNTs by secondary lateral CNTs [207] or graphitization [208]. The problem then is whether individual CNTs can withstand the coolant flow pressure without detaching from the substrate. There is also a high thermal resistance between the CNT and the epoxy used for the CNT transfer process [209, 210]. The choice of the cooling thermo-fluid is also important, with suspensions of CuO [211], alumina [212], CNTs [213, 214; Cheng Z, SMIT Center, Shanghai University, 2008, Personal communication], and plasma-treated CNTs [215] in water all being tried. In the last case, the plasma treatment promotes a hydrophilic CNT surface. [211] analyzes CNT fin geometries. An air-jet-cooled CNT fin array is described in [216] with the mechanical reliability of the CNTs in this structure examined in [217].
A potentially revolutionary cooling system is described in [218], requiring three closed-end CNTs aligned end-to-end. Hot electrons, e.g., above the Fermi level, tunnel across a gap from the heated CNT to the "barrier" CNT where they lose energy before tunneling again to the third CNT which acts as a heat sink. In this way, energy is transferred from the heated CNT to the heat sink CNT via the barrier CNT. The principle is described in [219] and [220], and an alternative setup is proposed in [221]. The practical challenge would be the precise alignment and support of the CNTs.

1.4.4 Carbon Nanotubes: Electrical

The fundamental concepts of quantum conduction in CNTs are reviewed in [222].

An important development has been the ability to open CNTs after growth [168, 223, 224], since the open ends permit better wetting by Sn/Pb (and presumably other metals) for improved electrical contact. Au and Ag incorporation into CNTs and fullerenes has also been studied for electrical contacts with minimal galvanic corrosion [225]. Metal- and carbon-loaded polymers have long been used for highfrequency conductors in electromagnetic shielding, and both carbon fibers [226] and multi-walled CNTs have been studied in polymer matrices for the purpose [227– 229], but CNT replacement of metal filler in isotropic conductive adhesives [230– 232] does not even match the electrical conductivity of standard materials [232, 233]. However, 10–50 µm long Ag/Co nanowires of 200 nm diameter can be maintained in a parallel vertical orientation by a magnetic field, while polymer resin flows around them [234], to form an anisotropic conductive film for z-axis contacts [235–237]. CNT interconnection schemes are also under intense study [238-241], with µm-scale CNT bundles successfully developed as flip-chip "nanobumps" [242–244]. The expectation is that CNT bumps will outperform solder by being stress-free with no reflow step, by the absence of electromigration and by being more flexible. The mechanical reliability of CNTs as bumps and other forms of interconnect has been studied [217]. A "Velcro" form of CNT-to-CNT interconnect has been demonstrated [207], between CNT bundles on a flip chip and corresponding bundles on the circuit board, resistivities of $0.05-0.1125 \ \Omega$.cm having been achieved. Further in the future, RF wireless interconnect has been proposed using CNT antennas [245].

In a modeling paper [246], it has been shown that the increase in MWCNT conduction channels with temperature can offset the increased electron scattering to yield a negative temperature coefficient of resistance (TCR) for shorter MWCNTs up to ~ 1 to $10 \ \mu m$ long, depending on diameter.

A number of performance comparisons of CNT interconnects with Cu (and graphene) [247] have been made. The broad conclusion is that CNT interconnects, either MWCNTs or tight bundles of SWCNTs, are only competitive with Cu conductivity at longer lengths where the CNT ballistic length exceeds the electron mean free path in Cu [238, 248, 249] and for signal delay at \geq 50–100 µm. These

conductivity comparisons are typically made at DC, and it is the high-frequency performance that is more important for signal transmission.

Due to the high kinetic inductance, there is negligible redistribution of current at high frequencies, i.e., negligible skin effect, and the CNT bundle resistance does not increase at high frequencies as it does for Cu [250–252]. High-frequency CNT (and graphene) modeling is reviewed in [253] and [254] which also describe CNT implementations of capacitors and inductors.

A continuing problem with CNT interconnects, e.g., in TSVs, is the interfacial resistance to metallic conductors, which may make up 80% of the total interconnection resistance [255, 256]. The basic problem is that even a metallic CNT forms a Schottky barrier with the metal [168, 257] which may still provide an acceptable contact between high work function metals to p-type CNTs or low work function metals to n-type CNTs. Other techniques include deposition of graphene on the CNT as a graphitic interfacial layer [258] or rapid thermal annealing, possibly by Joule heating [259]. An AuPd alloy reportedly matches the CNT work function to achieve a low interface resistance [260]. A high resistance to Ti is attributed to oxidation, which is avoided by substituting TiN, achieving 0.59 Ω , but the deposition of Ti between the CNT and Cu apparently presents no problem as a top contact [261]. Ti/TiN is also used in [262] with an Al top contact. Ag, Au, and Pt contact resistances are reported in [263], which states that Ti, Cr, and Fe are better than Au, Pd, or Pt because of the work functions. In another work, Cr/Ni/Cu is sputtered on to the CNT ends, which then form a strong thermocompression bond to a Cu substrate [264]. The CNT resistance to Au can be reduced by about 11% by the electron beaminduced deposition of W [265], and the CNT can be welded on to a favorable metal for wetting the CNT, e.g., Ni, with the metal wetting the CNT, so C atoms are effectively embedded in the metal [266].

Most of the CNT interconnect studies above have been on free-standing vertical bundles, but these can also be encased in deposited silicon oxide or nitride with no ill effects [267]. There are also obvious benefits to encasing a vertically aligned CNT bundle in a metal, e.g., Cu, but also possibly Ni, Co, Fe, or Ag. After conformal deposition of pyrolytic graphite to stabilize the bundle, it is infused with a metal salt, which is reduced with H₂ [268].

With the current focus on packaging for 3D integration and chip stacking, it is a short hop from vertical CNT bundles for electrical connections to the more specific application in TSVs [269–272]. CNT TSVs (Fig. 1.3) [273] have been fabricated by various techniques [273–280]. The process generally follows a sequence of ion etching a blind via in the Si substrate with the subsequent deposition of a seed layer, usually of Fe nanoparticles, on the bottom of the via. The CNT bundle then grows on the seed nanoparticles by CVD from a suitable hydrocarbon gas. For SWCNTs, the diameter is controlled by the nanoparticle size. The top surface is then typically metallized or planarized, while the Si substrate is thinned from the back to provide access to the bottom of the CNTs. One of the most dramatic pictures in the literature is of a single 15 nm diameter MWCNT in a 35 nm via [281].

To compete with Cu TSVs' electrical properties, the CNT bundles need to be densified to provide as many CNTs per unit area as possible. In addition, CNT





growth in the blind via as described above limits the growth temperature and introduces unwanted defects into the CNTs. To combat both of these problems, CNTs have been grown as free-standing bundles, which were then densified and transferred to the target wafer by inserting them into the pre-etched vias [157, 158, 282–285].

There is no lack of electrical modeling of CNT TSVs [250, 286–293]. Some model a TSV pair as a transmission line [288–290], some present results in terms of scattering parameters [287, 291–293] while others focus on delay time and frequency response [290], but only a few address skin effect in the CNT TSV context [250, 287]. As mentioned above, the absence in CNTs of the high-frequency



Fig. 1.4 Copper "pumping" in a TSV: as fabricated at temperature T_0 ; copper extrudes from the TSV at temperature $T > T_0$ due to the Si-Cu CTE mismatch; gap appears between the copper and silicon when the temperature returns to T_0 [294]

resistance increase in metals due to skin effect is a major advantage, besides which CNTs have demonstrated high current stability [154] due to the absence of electromigration. Electrically, the CNT TSV may not perform much differently than Cu- or W-filled TSVs, but there are further advantages from higher thermal conductivity and thermal stability [289]. This latter point comes from the issue in metal-filled TSVs of metal "pumping" (Fig. 1.4 [294]) which can open the via to moisture or fracture metal contacts at the ends, a problem due to the extreme CTE mismatch between Si and metals, and mitigated by CNTs' closer match to Si. It has been shown that stress at the surface of Cu TSVs is the result of this CTE mismatch and is largely absent in CNT TSVs [295].

The Cu-CNT composite TSV seems to be a logical step to combine the advantages with a vertically aligned CNT bundle embedded in Cu. The two main fabrication approaches, both by electroplating the Cu into pre-grown CNT bundles, are represented by [296] and [297]. In [296], the CNTs are grown in a blind via, and an electroplating solution is added after CNT densification, which promotes accessibility of the solution to the CNTs. In [297], the CNTs are grown and the TSVs etched separately; the CNT bundles are sputtered with Ti (10 nm) and Au (20 nm) before being threaded into the TSVs for electroplating. There was no densification step in order to preserve the CNTs' pristine state for the sputter deposition and Cu nucleation. In the first case [296], the TSV resistances were all greater than for the equivalent Cu TSV, possibly indicating incomplete Cu plating along the entire length of the via, although the Cu seemed to be as intended at both ends. In the second case, [297], the resistance was as calculated, with the Cu reducing the CNT bundle resistance.

In theoretical modeling of the high-frequency performance, the Cu still provides a skin effect, which is reduced by increasing CNT content [298]. The TCR is reduced in comparison with a Cu TSV, as expected, as is the CTE [297], with an order of magnitude less stress in the silicon. It has been shown that the axial CTE can exactly match silicon's, for zero Cu pumping, at 29% CNT content by volume [294]. At 29%, the radial CTE is also reduced to about 2/3 of the Si CTE. It has also been shown that for a similar Cu/CNT structure, but in thin-film form, the current-carrying capacity is increased by the CNTs to 100x the Cu value [299].

A slightly different Cu/CNT TSV was used in [300] to model its mechanical properties, namely, with a Cu cylinder surrounding a separate CNT bundle, under

bending and thermal cycling. Another variation in the form of a tapered via has been proposed as more effective in the Cu electroplating step [301] and has been shown to provide a reduced delay over the cylindrical geometry, presumably due to the lower average capacitance, although the delays are slightly different depending on signal direction.

The electrical properties of CNTs (and graphene) are covered extensively in Chap. 27, and further coverage can be found in [302–310].

1.4.5 Nanowires

Nanowires are covered in Chap. 21 and in Chap. 22, which focus on anisotropic conductive film (ACF) applications and carbon nanofibers (CNFs) in [311]. CNFs cannot compete with CNT properties but have the advantage of lower synthesis temperatures. Applications include as ICA fillers [236, 237, 312–314] and for z-axis connections within ACFs [234, 315].

Ni nanowires have also been employed in a reusable test probe system [214] where a nanowire bundle is shown to have less contact resistance than a simple planar pad.

1.5 Graphene

1.5.1 Graphene: Introduction

Graphite has long been used as a lubricant, an electrical conductor (e.g., for the carbon arc in old movie projectors) and as a thermal conductor (e.g., in pastes) as well as in the ubiquitous "lead" pencils, and children learn in grade school that it lubricates because the single layers of carbon atoms can slide over each other. It was the painstaking exfoliation of those 2D planes of C atoms down to a single atomic layer that spawned the still expanding area of graphene research. In nanopackaging, there are three main application areas that exploit three main attributes: mechanical strength (mainly in composites) and high thermal and electrical conductivities. In addition, its impermeability provides possible applications as a diffusion barrier, e.g., to prevent the galvanic corrosion of Cu in contact with Ag-ICA [316].

Once graphene had opened up the concept of 2D atomic monolayers, the search began for others, most noticeably 2D Si (silicene), Ge (germanene), P (phosphorene), hexagonal-BN (h-BN), MoS₂, and (recently) Si₂BN [317]. Some of these are truly 2D, while others are buckled, i.e., the monolayer atoms are not actually coplanar.

See Chaps. 24 and 25 for more on graphene synthesis and characterization.

1.5.2 Graphene: Nanocomposites

The properties of graphene/polymer composites are reviewed in [318] and compared with CNT and silica nanoparticle (and nanoclay) polymer composites in [166] which are focused on mechanical properties. An intriguing concept is the application of dilute-functionalized graphene nanosheets as "self-healing" agents in a graphene/ polymer composite to repair cracks and other defects under infrared laser irradiation [319].

1.5.3 Graphene: Thermal

The thermal properties of graphene are compared with those of other carbon allotropes in [320], which highlights the wide range of data in the literature. The paper notes that pyrolytic graphite challenges single crystal diamond's thermal conductivity at room temperature and above and leads one to conclude that graphite should not be ignored as a lower-tech lower-cost candidate for efficient electronics cooling. At 4000–6000 W/mK, graphene seems to display the most impressive potential, but these results, obtained for a single suspended sheet, are not maintained in contact with another material, even other graphene sheets. The results for suspended few-layer graphene (FLG) degrade to high-quality graphite's values (~2000 W/mK) at between three and four monolayers and to standard graphite values (~1000 W/mK) at eight monolayers, which is not surprising given that graphite is multilayer graphene. Single and FLG values range ~50 W/mK at 0.7 nm thickness to 1000 W/mK at 8 nm when sandwiched between dielectric layers as they would be in an on-chip or SiP heat-spreading scenario, i.e., less than graphite's 2000 W/mK.

It is noted in passing that the thermal conductivity of graphene with a reduced content of the 13 C allotrope (0.1% vs. the natural 1%) is increased by ~35% [321].

The conventional thermal dissipation pathways are metal, e.g., lead, tracks, vias, heat sinks, and thermal ladders, so it would be logical to try to improve their performance by adding graphene. The effects of oriented lamellar and randomly oriented single-layer graphene (SLG) and multilayer graphene (MLG) in Cu have been calculated, for both along and perpendicular to the graphene sheets in the lamellar case [322]. The effects are positive only for the lamellar SLG case along the graphene layer direction and for oriented SLG and MLG particulates. The mechanical properties and contact angle are improved by the addition of graphene sheets (decorated with Ni nanoparticles) to solder [323], as for CNT additives [Chap. 20, 132, 192].

Graphene sheets decorated with Ag nanoparticles have been added to Ag/epoxy ICAs with Ag flake/powder fillers to enhance the ICA thermal conductivity, reaching ~8 W/mK at 12wt.% graphene/Ag [324] and 3 wt.% graphene [325].

Porous heterostructures have also been developed. In one, conducting graphene and insulating h-BN foams are compared [326]. The foam is seated between the chip and circuit board and compressed to $1-2 \mu m$ thickness. The advantage of the

nanoscale porous features and the compression is that excellent contact is possible at both surfaces, accommodating asperities and achieving thermal conductivities ~80 W/mK. In another approach, graphene is deposited on the surfaces of porous Cu, yielding ~210 W/mK [327] to ~230 W/mK [328].

Most predictions of graphene's function in chip/package cooling assume it will be in 2D heat spreaders for hotspot mitigation [329, 330]. In [331] and [332], silanefunctionalized graphene oxide is inserted between the package hotspot and the graphene-based film to improve thermal contact. Graphene and h-BN heat spreaders are compared in [333]. The reader is referred to Chap. 27 for more details.

Graphene can be controlled as p-type or n-type depending on the polarity of a back-gate bias, so an effective PN junction can be created. With a PN junction, the possibility of thermoelectric cooling by the Seebeck effects becomes possible, as proposed in [334]. The thermoelectric figure of merit, ZT, is given by:

$$ZT = \frac{S^2 T}{\rho K_t},$$

where S is the thermoelectric power, T is the absolute temperature, ρ is the electrical resistivity, and K_t is the thermal conductivity. The problem is that K_t is high in graphene and also that ρ can be high due to surface scattering, both reducing ZT. It turns out that ZT.K_t is greater in graphene on h-BN (e.g., on a 10 nm h-BN spacer) than on SiO₂, and the feasibility of Peltier cooling has been demonstrated [335]. The active cooling boosts the passive cooling of the structure by 10%.

Porous heterostructures have also been developed. In one, conducting graphene and insulating h-BN foams are compared [326]. The foam is seated between the chip and/or circuit board and compressed to $1-2 \mu m$ thickness. The advantage of the nanoscale porous features and the compression is that excellent contact is possible at both surfaces, accommodating asperities and achieving thermal conductivities ~80 W/mK. In another approach, graphene is deposited on the surfaces of porous Cu, yielding ~210 W/mK [325] to ~230 W/mK [328].

Chapter 27 covers the application of graphene in microelectronics cooling in more detail.

1.5.4 Graphene: Electrical

The theory behind the electrical properties of both CNT and graphene nanoribbon (GNR) interconnects is reviewed in [253] and [336, 337]. Theoretically the mean free path (ballistic length) of a GNR is $\lambda_{GNR} \approx 450w$, where *w* is the GNR width, but in practice $\lambda_{GNR} \sim 1 \ \mu\text{m}$ due to defect scattering, but even for $\lambda_{GNR} \sim 5 \ \mu\text{m}$, single-layer GNRs could not compete with Cu interconnect. Moving on to multilayer GNRs (MLGNRs), there is the problem that they degrade to graphite for more than few layers. The solution is that the graphene layers must be kept apart in an intercalated structure. AsF₅ [253, 336, 337] and FeCl₃ [158, 338, 339] are mentioned. The

in-plane resistivity of AsF₅-intercalated graphite is quoted as 1.6µ Ω .cm, or a little less than Cu's with $\lambda_{GNR} = 1.03 \ \mu m$ [253], with 21.45µ Ω .cm for FeCl₃ [339] (or 20 Ω /square as a transparent electrode) [338]. The arguments pertaining to the kinetic inductance and skin effect mimic those for CNTs.

Graphene-wrapped Cu interconnects have been proposed with tri-layer graphene deposited on one, two, and all four sides of a square Cu conductor [340]. The current flows mainly in the central Cu at the ends due to higher graphene-Cu contact resistance than Cu-Cu but mainly in the graphene along most of the interconnect length, reducing the current density in the Cu and reducing the chances of electromigration failure. The graphene also conducts heat away from the Cu, further increasing reliability.

There are proposals in the literature for all carbon interconnects with MLGNR x-y plane tracks and CNT vias [158, 341]. Such a system would require making reliable low-resistance contacts from the CNTs to the graphene sheet, possibly by introducing defects into the graphene surface, e.g., by removing C atoms or depositing seed nanoparticles, and growing the CNTs from there. The electrical and thermal performances of such a MLG/CNT via system are simulated in [341] and compared with Cu.

At the "low-tech" application end, surface resistivities as low as 80 Ω/\Box have been obtained by direct writing MLG flakes in quick-drying isooctane [342].

The electrical properties of graphene (and CNTs) are covered extensively in Chap. 27.

1.6 Nanoscale Structures

The incorporation of nano-diamond particles into an electroless Ni film coating on an electrothermal actuator [343] can improve cantilever performance by changing the thermal and mechanical properties. Sometimes one can get to the nanoscale by just continually shrinking existing technology, and in a truly impressive development, the micro-spring contacts originally developed at PARC-Xerox have been downsized to 10-nm-wide cantilevers, still 1 μ m long, for biological sensing [344] (Fig. 28.14 in Chap. 28). Nano-imprinting technology is also being used to fabricate optical interconnect waveguides in organic PCBs [345].

1.7 Nano-interconnects

The "nano-interconnect" terminology is applied to interconnect structures which are clearly μ m-scaled [346–353]. The ITRS Roadmap called for 20–100 μ m pitch interconnects for nanoelectronics systems of feature size under 100 nm [349], which has prompted studies of nano-grain solders [346] or copper [348], nanocrystalline copper and nickel [349], and nanoscale via fillers [347], all for applications at

around 30–35 µm pitch [346, 348]. Some nano-interconnect options are reviewed in reference [351]. Other technologies can be included in this group, too, e.g., metalcoated polymer posts on a similar scale [351] and embedded micro- or nanoelectrodes for biological flow sensing [353]. Control of the interfacial surface charge on the nano-electrode in contact with the fluid can be used to control the flow [353]. Since the ITRS roadmapping program ceased, the IEEE Electronics Packaging Society (EPS, formerly CPMT) has undertaken responsibility for the electronics packaging roadmap with the Heterogeneous Integration Roadmap:

https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

There are many ways to fabricate metallic nanowires for interconnections, but one of the newest is to utilize DNA as a framework. The DNA is activated by metallic cations, and metallic nanoparticles are added by electroless deposition to form conducting Cu or Au nanowires of ~20 nm diameter [354, 355].

Skin effects are canceled for high-frequency interconnects by balancing ferromagnetic and non-ferromagnetic conductors within the contact [356]. A polymer doped with ferromagnetic material (e.g., Co, Ni, etc.) is electrospun onto a substrate seeded with Cu, and after suitable lithographic patterning, Cu is electroplated into the structure to form a porous contact.

1.8 Plasmonic Interconnects

As nano-CMOS circuits and devices shrink on-chip, so do the metal interconnection lines, increasing the resistance, R, and the RC_{gate} time constant becomes the limiting factor in circuit speeds rather than the transmission line delay. As a result, surface plasmon polariton transmission is being studied as an alternative to electronic conduction interconnects [357–359], since the wave rides on the metal surface (or at the metal-insulator interface) [360]. Even though interconnect cross section areas are greater at the package level than on-chip, the same problem is developing due to longer line lengths. Of course, with transmission lengths on the order of 10 µm before the signal needs a boost, the need for pumping/amplification [361] will be greater at the package level than on-chip. Nevertheless, if the technology is adopted on-chip, it will likely migrate to the package when mature. It is interesting to note that surface plasmon currents have been stimulated and observed in discontinuous nanoparticle films [362].

Plasmon/nanoparticle interactions are already being employed in electronics packaging [363]. If one of a number of fine-pitch pads or solder joints must be re-worked, it is decorated with Au nanoparticles on a graphene sheet carrier. These nanoparticles will be heated by the surface plasmons excited by laser irradiation, heating that specific pad/joint but leaving the neighbors unaffected.

1.9 Miscellaneous

A relatively new development is the application of biotechnologies to electronics packaging. Nanocellulose has been shown to be a suitable electronics substrate material, especially for flexible applications or where transparency is required [364]. The substrates have a smoother surface than the competitors', and the material assists in recycling components by being biodegradable, combustible, and readily disintegrates in water. Biosynthesis of Ag nanoparticles from AgNO₃, for example, can be accomplished by bacterial, fungal, or plant extract interactions, possibly assisted by microwaves, sonication, or heating [365]. In a third example, Ag⁺ ions on polyimide are nucleated into nanoparticles by laser-assisted reduction in a mineral extract from spinach leaves in ethanol [366].

The Internet of Things (IoT) is projected to be the primary source of massive growth of the microelectronics industry in the near future. By and large, the system packaging technologies that will be employed here will be the same as those that are used in other applications, whether in the home, automobile, aircraft, industrial, or others. However, the IoT will push the development of nano-sensors which will have unique packaging challenges. But one of the recognized IoT challenges will be the proliferation of radio signals for reporting and control with an attendant risk of interference. So many system packages will need protection from electromagnetic interference by unwanted frequencies, e.g., by an array of ink-jet-printed and sintered nano-Ag band-reject antennas [367].

1.10 EHS: Environment, Health, and Safety

Much of the material being used in nanopackaging is nano-Ag, which has been used in various antibacterial and medical applications for centuries [365, 368], but the argument that therefore there should be no concerns about its growing use in other areas has been challenged [369]. Concerns are focused on the demonstrated toxicity to aquatic life and especially to embryonic fish and others at the bottom of the food chain [22, 370–372] although there is also concern about cellular effects in humans [373]. An industry perspective is found in [374]. Ag is not the only source of concern; a broader range is covered in [372], and nano-TiO₂ liver damage has been reported in [375].

CNTs have also been the subject of much study, again with concerns on cellular effects and the impact on aquatic life [376]. In this case, however, the similarities to asbestos mesothelioma are too obvious to be ignored, and pulmonary effects are the most studied [377], and following that analogy, distinctions must be drawn between the microphage ability to enclose and mitigate short CNTs or compact CNT bundles and the longer CNTs which cannot be surrounded [378].

See also Chap. 32.

1.11 Conclusion

The importance of nanoelectronics and "electro-nanotechnologies" in the future is sufficiently well recognized to have become the subject of industrial and government policy roadmaps [379]. Similarly, the academic world is responding with both undergraduate and graduate level courses and with textbooks. As for electronics packaging, the field requires students to be "subject multilingual" [380].

One of the surprising observations to come out of this survey, in full agreement with prior comment [381], has been that there is almost no work reported on the development of packaging for next-generation nanoelectronics technologies. The "nano-interconnect" work is directed toward continued Moore's law shrinkage of silicon (More Moore) or heterogeneous integration (More than Moore.) Candidate next-generation nanoelectronics technologies (e.g., single-electron transistors, quantum automata, molecular electronics, etc.) are generally hypersensitive to dimensional change, if based on quantum-mechanical electron tunneling, and this is just one example of how appropriate packaging will be essential to the success or failure of these technologies [382]. Packaging strategies must therefore be developed in parallel with the basic nanoelectronics device technologies in order to make informed decisions as to their commercial viabilities.

There has been a veritable explosion of research in the nanopackaging area since the first edition of this book appeared, and it is impossible to include it all here. Hopefully, the interested researcher can move backward and forward in time on a specific topic from the references in a specific paper and its later citations. There was a brief update to the first edition published [383], so most of its content has not been duplicated here. For future information in the field, the annual *IEEE Electronic Components and Technology Conference* (ECTC) and the nanopackaging sessions in the *IEEE International Conference on Nanotechnology* (NANO) and the *IEEE Nanomaterials and Devices Conference* (NMDC) are recommended.

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Chapter 2 Modelling Technologies and Applications



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2.1 Introduction

Since writing this chapter for the first edition of this book, we have seen a significant focus on modelling tools for nano-packaging in the community. Techniques based on atomistic and continuum modelling are now extensively used by the electronics packaging community to characterise material properties (e.g. nanocomposites for thermal interfaces), fabrication processes, assembly processes and performance and reliability assessments of electronic packages.

The structure of this chapter is similar to the first edition, namely, it focuses on (i) modelling tools and then modelling examples for (ii) fabrication processes, (iii) assembly processes and (iv) performance and reliability assessments. Each section has been updated to include references to recent work, and new sections on additive manufacturing and thermal interface materials have been included.

Numerical modelling technology and software is now being used to underwrite the design of many microelectronic and microsystems components. The demands for greater capability of these analysis tools are increasing dramatically, as the user community is faced with the challenge of producing reliable products in ever shorter lead times.

Modelling nano-packaging processes and materials requires modelling algorithms and software tools that can capture and predict interactions among the distinct phenomena and physics at multiple length and timescales. These multi-physics and multi-scale technologies are now being provided by a number of tool vendors. Figure 2.1 provides an overview of the key life stages in the manufacture and use of an electronic package.

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Fig. 2.1 Optimisation-driven numerical modelling for predicting reliable nano-packaging microsystems



Fig. 2.2 Modelling across the length scales

2.2 Modelling Technologies

All matter is made of atoms and molecules, and its behaviour is ultimately governed by the law of quantum physics. However, in the macroscopic world the fact that matter is a collection of discrete entities is often ignored because continuum theory can be used to describe the material behaviour reasonably well at this length scale. The use and classification of modelling tools across the length scales is detailed in Fig. 2.2.

Table 2.1 Some continuum- based modelling tools	Software	Web address
	ANSYS	www.ansys.com
	COMSOL	www.comsol.com
	FloTHERM	www.mentor.com
	MARC	www.mscsoftware.com
	Abaqus	www.3ds.com

2.2.1 Continuum Modelling

Continuum mechanics modelling tools can be classified as:

- *Computational Fluid Dynamics (CFD)* solving phenomena such as fluid flow, heat transfer, combustion, solidification, etc.
- *Computational Solid Mechanics (CSM)* solving deformation, dynamics, stress, heat transfer and failures in solid structures
- *Computational Electromagnetics (CEM)* used to solve electromagnetics, electrostatics and magnetostatics

Until recently the majority of continuum mechanics codes focused on the prediction of distinct physics, but now there has been a strong push by software vendors to develop multi-physics or co-disciplinary tools that capture the complex interactions between the governing physics such as fluidics, thermal, mechanical and electrical.

The use of these continuum methods is justified for most electronics assemblies because the feature size in these assemblies is so large compared to the size of the atoms/molecules that there are an astronomically large number of atoms in any assembly. The following table details a number of commercial continuum mechanics codes as used by the microsystems packaging community (Table 2.1).

2.2.2 Atomistic and Multi-scale Modelling

In order to model materials where understanding phenomena at nanoscale dimensions is important requires modelling methods that take into account the structure and the interactions of the atoms and molecules. This kind of modelling is called atomistic modelling, and the most frequently used atomistic modelling method is molecular dynamics (MD).

MD was first used by Alder and Wainwright to simulate a system of hard spheres [1]. The classic molecular dynamics method uses simple potential functions to describe the interactions between atoms and molecules. The average effects of the electrons are assumed to be included in the potential. In the ab initio or the first-principle MD method, the interactions between the ions as well as the interactions between the electrons and the ions are taken into account, and both the distribution of the electrons and the movements of the ions are tracked in the modelling [2]. The

Table	2.2	Some	atomistic-
based	mode	elling t	ools

Web address
lammps.sandia.gov
www.gromacs.org
accelrys.com
www.charmm.org
ambermd.org

embedded atom method (EAM) and its variants such as the modified embedded atom method (MEAM) enhance the classic MD method by including a separate potential term that can be attributed to the effects of the electrons [3]. Table 2.2 details some of the atomistic tools used by the community to calculate force fields and undertake molecular dynamics simulations.

In a classic MD simulation, the most important input is the potential function. In general, the function depends on the location of many atoms, but in many situations, the most important term is pairwise, i.e. the potential depends only on the distance between two atoms. The best known example of this type of potential function is the Lennard-Jones potential [4]. But even with the use of this simple potential, the number of atoms that can be modelled using the MD method is still very small compared to the number of atoms in any small macroscopic object. Even in a large-scale MD simulation, the number of atoms is limited to a few million, and the modelled time is in the order of picoseconds to nanoseconds. Hence there is a challenge in using MD to model processes and phenomena over longer time and spatial domains.

To bridge the length and time gaps between atomistic and continuum modelling, heterogeneous methods such as the particle-in-cell can be used [5]. This method takes into account atomic interactions in a physical phenomenon that takes place in a macroscopic system. Atomistic-continuum mechanics (ACM) is another method that combines the atomistic nature of materials with continuum mechanics [6]. In this method, the lattice structure and the interactions between atoms are taken into account. The macroscopic mechanical properties can be derived, but the dynamics of the atoms can't be studied using this method. A number of multi-scaling issues and use of MD for electronic packaging and material applications are provided in [7]. Further resources for nanoscale modelling can be obtained at nanoHUB (https://nanohub.org).

2.2.3 Optimisation and Uncertainty

Simulation-based optimisation for virtual prototyping of various electronic products and manufacturing processes has proven as an effective approach for process characterisation and product development at the early design stage [8, 9]. The complexity and variability of nanostructures and nanomaterials often makes real prototyping, experimental setups and testing difficult or expensive. Hence coupling
Table 2.3 Some optimisation-based modelling tools		
	Software	Web address
	VisualDOC	www.vrand.com
	iSight	www.3ds.com
	MATLAB	www.mathworks.com
	Ontimus	www.noesissolutions.com

physics-based modelling tools with optimisation and uncertainty analysis is a costeffective way to identify packaging designs and material properties that meet performance and reliability requirements. A number of physics-based modelling tools contain optimisation algorithms. Table 2.3 details some of the focused tools used for optimisation and uncertainty analysis within the community.

Optimal product or process design, when derived through a deterministic physicsbased model, may be far from a design solution which is safe, robust and meets the imposed design requirements. The reason for this is the presence of uncertainty which is inherent in various aspects of the nano-packaging. For example, variability can be found in the manufacturing and/or operational process parameters (e.g. operational temperature, humidity, etc.), dimensions of the manufactured structures, the physical properties of the materials, etc.

Quantifying uncertainty can be undertaken using several different concepts and methods. The most popular is probability theory which has the advantage to quantify uncertainty of a design or process parameter using probability distribution functions (PDFs). This important concept relates to the definition of the so-called limit state function (failure surface) which quantifies the reliability metric. The term 'reliability' in this context has the meaning of conforming with respective design requirements such as functionality, quality and dimensions.

Commonly used numerical techniques for uncertainty evaluation are the sampling methods such as the Monte Carlo simulation and Latin hypercube sampling where samples of random variables are generated according to the parameter probability distribution and then the reliability function is directly evaluated and checked for failure [10]. The proportion of the sample points for which failure is indicated through the limit state function approximates the failure probability. The disadvantage of these methods is the huge number of sampling point evaluations. Also each evaluation might be complex, expensive and time consuming if these are obtained through experiment or finite element type models. Reduced order models are used to overcome this limitation. These models offer fast analysis of the process or design and therefore a fast evaluation of the reliability function.

A different numerical approach to evaluate failure probability is based on the construction of approximations of the limit state function using first- or second-order Taylor series. These methods are known as first-order reliability methods (FORM) and second-order reliability methods [11].

There is an increased interest in non-probabilistic uncertainty modelling and uncertainty quantification which can potentially overcome some of the limitations of the probabilistic approach. Examples include the evidence theory [12], fuzzy sets and possibility theory [13], interval-based approaches [14] and polynomial chaos techniques [15, 16].

Numerical design optimisation is termed 'probabilistic' if it includes in the problem formulation the uncertainties of the various design variables and performs the optimisation while accounting for their propagation into variation of output design responses. A generic design problem under uncertainty can be defined as

$$\begin{array}{ll} \min_{X} F(X) & (\text{p1}) \\ subject \ to: \ P(g_{j}(X) > 0) \leq p_{j} \quad j = 1, m \quad (\text{p2}) \\ & X_{i}^{L} \leq x_{i} \leq X_{i}^{U} & i = 1, n \quad (\text{p3}) \end{array}$$

where $X = (x_1, x_2, ..., x_n)$ is the vector of design variables, F(X) denotes the objective function (aspect of the design or process we aim to improve) and p is the acceptable limit for the failure probability associated with the state limit function $g_j(X)$. The constraints under (p2) are referred to as probability of failures (POFs). One or more design variables in the defined optimisation task (p1)–(p3) are assumed to be uncertain and therefore have to be modelled with their respective known probability distribution.

There are various numerical techniques that can be used to obtain the solution of the above optimisation problem. The interested reader is referred to [17] for more details on the most common numerical optimisation techniques.

Figure 2.3 provides a visual interpretation on the main difference between a deterministic design solution and probabilistic design solution. The underlying



Fig. 2.3 Illustration of the shift from the deterministic optimal design solution when the same design problem is solved using probabilistic design optimisation

rationale is to compromise on the value of the objective function by moving the optimal design (e.g. defined with mean values of design variables) away from the critical boundary of constraints defined with the limits of the state functions. The probabilistic optimal design is found inside the feasible region of the searched design space so that the spread of designs due to the variation of design input parameters is still satisfying the respective constraints (p2).

The advantage of probabilistic numerical optimisation extends beyond the problem of achieving design goals under constraints and parameter uncertainty. This approach has been used more recently to achieve process robustness in the presence of manufacturing process variations and to make product design performance and reliability insensitive to operational and environmental variations. Examples of such application of probabilistic optimisation include the design of the quantum potential profile in a semiconductor nano-device [18], minimisation of current density overshoots in power semiconductor devices [19] and design of tri-modular redundancy (TMR) circuit systems [20].

While the focus with the six-sigma approach is mainly on the cost reduction by finding problems that occur in manufacturing and by fixing the immediate causes for these problems, the design for robustness approach is primarily about preventing the problems through product design and manufacturing process design optimisation that minimises variability of their performance aspects and characteristics.

Robustness analysis aims at providing an accurate estimation of the sensitivity of design outputs to the variability on the design inputs. The design input variability is described by formulating and considering the design input variables as being random (uncertain) variables. These variables are characterised with respective probabilistic distributions. In general, the standard deviations of design responses are used as quantitative measures for the robustness of the outputs. Smaller standard deviation of an output is associated with, and hence can be interpreted as, a more robust the design output.

Figure 2.4 illustrates the concept of robustness. Designing the process/product with input at X1 makes the response Y less sensitive to the variation of the



input X. For the same range of variation for the input, when at X2, the resulting variation for Y is substantially larger. Hence, design for robustness is primarily about the control of the variability of a response through design optimisation.

2.2.4 Future Challenges for Modelling Tools

There are a number of computational mechanics software tools now on the market. These technologies provide electronic packaging engineers with the knowledge and design rules to help deliver reliable products in time and at lower cost than could ever be achieved through physical prototyping alone.

Although computational mechanics codes are now used in the design of manufacturing processes, there are still a number of challenges. These can be classified as:

- 1. *Multi-physics*: Many packaging processes are governed by close coupling between different physical processes. Computational mechanics tools are now addressing the need for multi-physics calculations, but more work is required to capture the physics accurately in these calculations.
- 2. *Multi-discipline*: Thermal, electrical, mechanical, environmental, plus other factors are important in the design and packaging of microsystems products. Computational mechanics tools that allow design engineers from different disciplines to trade-off their requirements early in the design process will dramatically reduce lead times.
- 3. *Multi-scale*: Nano-packaging processes are governed by phenomena taking place across the length scales (nano, micro, meso, macro). Techniques that provide seamless coupling between simulation tools across the length scales are required.
- 4. *Fast Calculations*: Computational mechanics software that solves highly non-linear partial differential equations are compute intensive and slow. There is a need for reduced-order models (or compact models) for nano-fabrication and packaging processes. Although not as accurate as high-fidelity finite element or atomistic modelling techniques, they provide the design engineer with the ability to quickly eliminate many unattractive designs early in the design process.
- 5. Life Cycle Considerations: Major life cycle factors such as reliability, maintenance and end-of-life disposition receive limited visibility in computational mechanics analysis. Future models will include all life cycle considerations, such as product greenness, reliability, recycling, disassembly and disposal.
- 6. *Variation Risk Mitigation*: Current product and process models used in computational mechanics usually ignore process variation, manufacturing tolerances and uncertainty. This will be very important for nano-packaging. Future models will include these types of parameters to help provide a prediction of manufacturing risk. This can then be used by the design engineer to enable them to implement a mitigation strategy.

2.3 Modelling Applied to Fabrication Processes

Fabrication of nanostructures that can be used in nano-packaging of electronic systems is considered in this section. Techniques which illustrate a bottom-up (electrodeposition) and top-down (focused ion beam and print forming) approach to nano-fabrication are discussed. In addition to this, we also detail recent advances in additive manufacturing.

2.3.1 Modelling of Focussed Ion Beam Milling Process

Focussed ion beam (FIB) is a milling process used to remove material from a defined area or to deposit material onto it at micro- and nanoscales. The principle of operation for FIB is bombardment of a target surface through high-energy gallium Ga+ (or other) ions. As a result, small amounts of material sputter in the form of secondary ions, natural atoms and secondary electrons.

The FIB process reduces dramatically the damage on the surface being subject to ion bombardment compared to other classical methods. In the FIB process a critical variable to control is depth variation. This is essential to ensure suitable fabrication of 3D nano features, miniaturised objects, masks and moulds for various microsystems.

Modelling and simulation of FIB processes has received substantial research interest in the past years due to its potential to enable informed milling of predefined structures [21]. The advantage of using numerical modelling and simulation of FIB process has been recognised particularly for nanometre-scale manufacture of fine features, for example, in fabrication of nanoholes [22] and single line etching and deposition [23].

The mathematical model discussed here is capable to predict the etched shape or to calculate the dwell times required to achieve a predefined shape [24, 25]. This model assumes a square pixel matrix placed over the target surface. The sputtering model is then discretized over each element of the pixel matrix so that a system of linear equations that relates the dwell times t_{ij} with the sputtering depth H_{ij} at any pixel (*i*,*j*) is constructed. A brief outline of the model is given below.

If (x_i, y_j) denotes the centre of the pixel (i,j), then the sputtering at this pixel in terms of depth due to material removal at that pixel can be expressed as

$$H_{ij} = \iint \frac{\Phi(x, y)}{\eta} f_{x, y}(x_i, y_j) Y(E_0, \alpha_{x_i, y_j}) t_{x, y} \, dx \, dy \tag{2.2}$$

where H_{ij} is the sputtering depth at the point (x_i, y_j) , $\Phi(x, y)$ is the ion flux at point $(x, y) \cdots (\text{cm}^{-2}\text{s}^{-2})$, η is the atomic density of the target material (atoms/cm³), \$\$*Y* (E_0, α_{x_i, y_j}) is the sputtered yield (atoms per incident ion at point (x_i, y_j)), $t_{x,y}$ is the

dwell time of the ion beam at point (x_i, y_j) (seconds) and $f_{x, y}(x_i, y_j)$ is the ion beam density distribution function in two dimensions.

The sputtered yield in Eq. (2.4) is a function of the incident angle α_{x_i, y_j} of the ion beam at point (x_i, y_j) and the ion energy E_0 as well as the type of ion source and target material. Generally, the yield increases from perpendicular ion beam incidence to a maximum at angle 60–85° and then rapidly decreases due to the strong reflection at grazing incidence. A classical empirical formula for the angular dependence of the sputtered yield is given by Eq. (2.5) which was originally proposed by Yamamura [26]:

$$Y(E_0, \alpha) = Y(E_0, 0) \frac{e^{\left(f\left[1 - \frac{1}{\cos a}\right] \cos \alpha_{opt}\right)}}{\left(\cos \alpha\right)^f}$$
(2.3)

where $Y(E_0, \alpha)$ is the sputtering yield at ion energy E_0 and nominal angle of incidence α . The quantities *f* and α_{opt} are parameters to fit the experimental data. In addition, α_{opt} is the nominal incidence angle at maximum sputtering yield.

The ion beam geometry in terms of density distribution $f_{x, y}(x_i, y_j)$ is also taken into account in the model (2.4). If Gaussian bivariate density function is assumed then

$$f_{x,y}(x_i, y_j) = \left(\frac{1}{\sqrt{2\pi\sigma}}\right)^2 e^{-r^2/(2\sigma^2)}$$
(2.4)

where $r^2 = (x_i - x)^2 + (y_j - y)^2$ radial coordinate for an ion beam focused at (*x*,*y*).

Figure 2.5 shows an example of a FIB simulation predicting the dwell times and milling shape using the model defined above. The model is used to calculate the dwell times over each of the pixel cells so that with given ion beam parameters a cavity with prior defined parabolic shape is sputtered. The parabolic predefined shape has a maximum depth of 2 µm. In this analysis the ion beams are assumed to have normal distribution with standard deviation $\sigma = 0.075$ um, $\Phi(x, y) = 1E19$ ions/s cm², $\eta = 5E22$ atoms/cm³, and pixel grid is 20 × 20 over target area 3 × 3 µm.



Fig. 2.5 Modelling of FIB milling of a parabolic feature – milling times along the cross-sectional pixels (left) and contour depth levels (microns)

The target surface is silicon, and the sputtering yield is calculated using Eq. (2.5) and assuming 20 keV Ga ions.

The above model for FIB sputtering can be enhanced by considering redeposition. The mathematical model given in Eq. 2.7 below is constructed on the basis of assuming the amount of the sputtered atoms or ions from a source pixel cell (i,j) and then redeposited onto another target pixel cell (k,l) is dependent on the relative locations between the two cells and their own orientations [27]. The redeposited volume of material R_{ij} as function of the sputtered volume S_{ij} can be calculated as:

$$R_{ij} = \frac{F(B) - F(\gamma)}{F(180^{\circ})} S_{ij} \text{ where } F(x) = \frac{\pi r^3}{3} \left[\cos^3(x) - 3\cos(x) + 2\right]$$
(2.5)

In Eq. (2.7), β and γ are the minimum and maximum angles that are measured from the centre of the source cell (i,j) to any possible locations within the target unit cell (k,l) respectively. For a cell (k,l) the re-repositioned volume can be found as the summation of contribution from all other source cells (i,j). This model assumes that the total displacement after redeposition is normal to the surface of the unit cell.

Some recent efforts in the modelling of the FIB process have focused on simulating the non-linear dynamics of ripple formation as a result of the ion beam sputtering process [28]. Modelling and understanding the ripples formation phenomenon is gaining interest as a result of the potential to use it in various nanotechnology applications.

2.3.2 Modelling of Nanoimprint Lithography (NIL) Process

Among the most attractive and promising nano-fabrication processes is nanoimprint lithography (NIL). This method offers low-cost and high-yield nanoscale patterning using various materials at dimensions as small as 6 nm [29].

Thermal nanoimprint lithography is one of the most typical methods for nanoimprint lithography. The thermal imprint process is based on the utilisation of thermoplastic polymers and comprises several steps as outlined schematically in Fig. 2.6. A polymer and a nanofabricated master tool (mould) are preheated above the polymer glass transition temperature (Tg), and then the fine mould, patterned according to the required specification, is pressed into the polymer forming a negative relief of the master. While the mould is pressed and held down, the polymer is cooled down below the Tg and hardens, thus retaining the profile of the mould pattern. Finally, the imprinting pressure is removed and the mould is released.

Modelling and simulation of NIL has been playing an important role in developing this technology. For example, modelling and simulation techniques have been adopted in studies of the effect of various geometrical parameters on accuracy and throughput of ultraviolet nanoimprint lithography [30], solvent migration in a polydimethylsiloxane (PDMS) stamp during imprint lithography of PMMA hybrid



Fig. 2.6 Typical steps in thermal nanoimprint lithography

suspensions [31], filling process in directed self-assembly lithography of block copolymer with NIL [32] and embossing stage of an ultrasonic vibration-assisted hot glass lithography process [33].

Typical issues associated with NIL are related to the mechanical stresses and the large deformations of the polymer films and the residual thickness after imprinting. Numerical simulations of the cross-sectional profiles as functions of process parameters such as the imprinting pressure, polymer initial thickness and the nano-cavity size/aspect ratio can provide valuable knowledge on the imprint process. There are two main modelling approaches that can be utilised to model the nanoimprint lithography process.

The first method involves modelling of the mechanical deformation process using hyperelastic large strain finite element analysis [34]. For this type of analysis the polymer is modelled as a rubber elastic body above its Tg with large strain and assumed to be a non-compressive material. A suitable model to represent this behaviour is the Mooney-Rivlin model [35, 36]. According to this model, the stress is expressed as

$$\sigma_i = \lambda_i \frac{\partial W}{\partial \lambda_i} \tag{2.6}$$

where λ_i is the expansion strain rate (deviatoric strain), and W is a strain energy density function defined as

$$W = C_{10}(I_1 - 3) + C_{01}(I_2 - 3)$$

$$I_1 = \lambda_1^2 + \lambda_2^2 + \lambda_3^2$$

$$I_2 = \lambda_1^2 \lambda_2^2 + \lambda_2^2 \lambda_3^2 + \lambda_3^2 \lambda_1^2$$
(2.7)

In the equations above, C_{10} and C_{01} are the Mooney material constants characterizing the deviatoric deformation of the material.

The Money-Rivlin model for rubber elastic non-linear stress-strain behaviour is incorporated in commercially available software such as ANSYS and MARC. The other critical feature of this type of analysis is the simulation of large deformations in materials under contact boundary conditions which is required to represent the interaction between the mould and the polymer. This analysis is based on some assumptions such as that no air bubbling, trapping or absorption into the polymer occurs. This does not impose any major setback because the imprint pressure is very high compared with the air ambient pressure, hence no major impact on polymer deformation at the macro level will take place.

The above modelling approach can be applied to study in detail the imprint process sequence. As an example, Hirai's group uses this approach to undertake defect analysis in thermal nanoimprint lithography and to study the dynamics of the deformation process [37]. As part of their work the authors have found very good agreement between simulation results and the experiments. The numerical analysis has identified correctly a stress concentration site near the polymer corner due the applied pressure below Tg which subsequently led to the defect of polymer fracture during the mould release step. The simulation results for the cross-sectional profiles from the analysis of the resist deformation process [38] have been shown to agree quantitatively very well with the experimental results for various geometric and pressure conditions.

The second modelling approach is based on modelling the flow of the polymer using computational fluid dynamics analysis. The key features of this type of simulation include modelling the polymer as a non-Newtonian fluid with a free (moving) boundary. In such two-phase large free boundary deformation flow analysis, phenomena such as the polymer capillary surface with surface tension boundary condition are explicitly considered. These continuum simulations can capture the underlining physics of the nanoimprint process from 10 nm to 1 mm scale and are capable of predicting accurately the polymer deformation mode and surface dynamics. A non-dimensionalised calculation procedure that follows this modelling strategy is presented in the work by Rowland and co-authors [39].

2.3.3 Modelling of Electroforming Processes

Attempts to numerically model the electrodeposition process are challenging as they must solve a system of coupled non-linear equations with the added complication that the governing equation set changes under different physical situations, for example, as the deposition current varies from primary to secondary, tertiary or diffusion-limited regimes [40]. Additionally the representation of electrode kinetics, the driving force for deposition, is of key importance and is complicated by its influence from the electrode surface overpotential and the concentration of reacting ions in the immediate vicinity of the depositing interface. Figure 2.7 illustrates the process taking place for trench or via filling.

The governing equations may therefore include all or a combination of the momentum, heat, concentration and electric potential equations with various degrees of intercoupling by electromigration, convection and importantly through the reaction rate boundary condition at the electrode surface. Standard continuum equations for momentum, electric field and ion concentration are solved except at the thin







layers adjacent to the electrode boundaries, the electrical double layer which is of the order of $<\sim100$ nm in width. In these thin layers, the deposition current is accounted for by an electrode kinetic function, typically the Butler-Volmer equation [41]. Figure 2.8 illustrates the evolution of a deposition layer using a coupled simulation approach and a free surface tracking algorithm [42, 43].

The main goal of numerical modelling of electrodeposition (ED) processes is to determine the values of certain control parameters that would guarantee the best

Fig. 2.7 Evolving

deposition layer on a conductive surface

quality of filling, e.g. filling that is free from both overplating, i.e. crowding formed at the mouth of the via, and underplating, i.e. unacceptably thin layers at the bottom of the via. Typical control parameters include the aspect ratio, copper ion concentration and initial current density. To estimate the outcomes of the numerical predictions, various metrics can be employed to characterise the plating process [44, 45].

Two processes are mainly responsible for ion transport during basic ED: *diffusion* which is caused by the difference in concentration of cupric ions and *migration* which is caused by the electric field, i.e. positively charged cupric ions move towards the negatively charged cathode.

To solve the governing ED equations, various software tools can be used. For example, COMSOL Multiphysics provides a natural way to solve these equations. Numerical experiments with various types of vias confirm the widely accepted opinion that basic ED that uses no additives or any other form of enhancement does not guarantee an acceptable quality of filling of microvias. The crucial reason of this underperformance is that basic ED does not provide a sufficient level of ion transport in the vias.

Capturing the impact of plating bath flow conditions on electrodeposition requires a multi-scale approach. For example, such modelling techniques are required when considering controlled electrolyte flow and megasonic agitation [45, 46]. Figure 2.9 details such a multi-scale approach.

At the macro level, the numerical models predict pressure, velocity and ion concentration in any part of the plating cell, including the surfaces of the panels, which serve as input for the relevant micro models. The macro level simulations lead to recommendations on the most suitable design of a plating cell with the purpose to improve ion transport, i.e. suggestions on the positions of the panels, inlets and outlets within the cell.

Considering acoustic streaming (AS) induced by megasonic agitation as a possible form of enhancement of ED, one of the aspects associated with AS has to be taken into account. Due to megasonic agitation, an acoustic boundary layer in the model is generated along the panel surfaces. That layer is extremely thin, e.g. for a transducer's frequency of 1 MHz, and its thickness is less than 0.6 μ m [47], while the



Fig. 2.9 Relations between different levels of flow modelling

a b c d

Fig. 2.10 Deposition level for the 1:1 AR via: (a) basic ED; (b) ED enhanced by AS, and for the 2:1 AR via; (c) basic ED, ED enhanced by AS

thickness of the hydrodynamic boundary layer along a panel is much larger, e.g. $1500 \mu m$ for a flow velocity of 4 m/s [48].

Due to its small thickness, the acoustic boundary layer is responsible for maintaining a permanent level of ion concentration in the vicinity of the mouth of the via. Thus, a modified boundary condition in the micro models with AS assumes the same bulk concentration in the whole area above the mouth of a via, rather than at the far field. Due to a permanent supply of copper ions at the mouth area, the updated boundary condition has a positive effect on ion transport and eventually on the quality of filling. Figure 2.10 shows the differences between the deposition level achieved in each via for the basic ED and ED with the modified boundary conditions due to AS. The main difference is that under the conditions of the basic model, none of the vias is completely filled. By contrast, in the case with the modified concentration boundary conditions, the filling of both vias is complete, leaving no void.

While the described improvement is related to AS at the macro level, i.e. outside the via, the influence of AS on convective flow inside the vias is negligible. In the case of blind vias, this conclusion is supported by both theoretical considerations regarding AS in narrow closed channels with reflective bottom [47] and real-life experiments [49].

2.3.4 Modelling of Additive Manufacturing Processes

Printed electronics and 3D printing is seen as one of the most attractive technologies for fabrication of nano- and microelectronics. Current examples include the fabrication of electronic structures and components such as thin-film transistors, electrical circuit patterns using nano-silver inks, RFID labels, conductive and photovoltaic structures, NEMS, flexible displays, mechanical actuators and sensors [50]. Recent advances in 3D printing suggest that it has the potential to transform the traditional manufacture of electronic products into printing-based manufacture of completely integrated devices with functional capabilities [50, 51].

A number of research programmes are underway to make 3D printing a reality in producing truly 3D electronic devices and systems. One example is the EU project NextFactory [52] which is developing 3D printing, micro-assembly and curing systems that will accurately deposit and cure both functional and structural materials and place/embed components in an integrated manner within a single platform.

ASTM Standard F2792 'Standard Terminology for Additive Manufacturing Technologies' defines seven process classifications for additive manufacturing, specifically binder jetting, directed energy deposition, material extrusion, material jetting, powder bed fusion, sheet lamination and vat photopolymerisation [53].

Inkjet printing is an example of a material jetting method. It involves the ejection of continuous or drop-on demand ink droplets from a printhead nozzle and their deposition and solidification on a selected substrate.

Dimensional and shape accuracy of printed structures and achieving required specifications (e.g. resistivity of conductive lines, etc.) is a major requirement. The quality of 3D inkjet printing process is highly dependent on both material physical properties and machine operating conditions such as the droplet ejection, deposition and cure [54]. For example, inkjet printing of conductive inks and the methods of their sintering are key factors affecting the performance, quality and reliability of the manufactured electronic circuits and devices.

While current research is focused primarily on the demonstration of the technology potential for 3D printing for electronics packaging, suitability of different sintering methods [57] and printability and resulting electrical conductivity of sintered particle-filled inks [58], there is a growing interest and demand for developing design and modelling methodologies and tools for 3D printing.

Computational intelligence techniques such as artificial neural networks, fuzzy systems and genetic algorithms have been used for quality prediction in a variety of applications but so far have found limited use in relation to 3D printing processes. Work published to date is mainly in the field of rapid prototyping [55].

From the reliability point of view, risks of stress-induced defects in a final product are of great concern and have to be mitigated or, at least, understood. The majority of the research activities to date in this area have focussed on analysis of the structural stability of 3D printable designs. As an example, Stava et al. studied stress relief design solutions based on hollowing and thickening using finite element analysis [56].

Printed conductive lines are the main feature of any printed electronic device. It is very important to obtain the lowest possible resistance or to meet any user-defined requirements for resistivity. It has been shown for printing DGP 40LT-15C ink on a polyethylene terephthalate substrate that the values of resistivity vary with layer thickness during the process [57], and that the resistivity of silver-ink printed lines thinner than 500 nm is not constant because of the significant extra scattering of electrons on the surface of the lines.



Fig. 2.11 NARX five-step-ahead predictions for quality parameter (resistivity of conductive line) over discrete time steps of printing conductive lines

Using the NARX neural network [59] provides the ability to predict resistivity of printed lines as a condition-based monitoring system. For example, [60] have demonstrated such an approach where a constructed NARX model forecasts the resistivity of conductive lines that are yet to be printed (see Fig. 2.11).

Cure shrinkage is a major issue and requires optimal selection of ink materials. 3D inkjet printing involves deposition of materials which are initially in a liquid state (inks) but are subsequently cured in order to achieve a final solid state. Viscoelastic-related shrinkage is the dominant phenomenon taking place when 3D inkjet-printed structures are fabricated. This is a key factor contributing to the quality of the fabricated products in terms of their dimensional and shape accuracy. Shrinkage behaviour of polymers is not always fully characterised, and material data or models are rarely available.

Cure shrinkage in either thermal or UV cure processes can be simulated through the use of standard FEA codes which have capability for modelling thermal expansion phenomenon. This requires the calculation of the so-called effective coefficient of thermal expansion (α_{eff}). The temperature-driven thermal expansion strains (ε_T) and the chemically induced cure shrinkage strains (ε_C) are modelled, respectively, as

and $\varepsilon_T(t) = \alpha(T(t) - T_0)$ $\varepsilon_C(t) = bp_m(t)$ (2.8)

where α is the polymer coefficient of thermal expansion (CTE), T(t) is temperature as a function of time, T_0 is a reference temperature, b is the total chemical strain at the end of cure (negative value for shrinkage) and p_m is the mechanical degree of cure.

The mechanical degree of cure is a measure of the polymer mechanical integrity and is used as a representation of the degree of cure of the polymer. Given that the viscosity of the uncured material is very small, the storage modulus for uncured polymer can be effectively taken as zero. Therefore, the mechanical degree of cure can be obtained as the ratio of the storage modulus at time t during the cure polymerisation process and the maximum storage modulus achieved at the end of the cure.

The total strain (ε_{tot}) is a sum of the thermal strain and the chemical cure strain:

$$\varepsilon_{tot}(t) = \left(\alpha + \frac{bp_m(t)}{T(t) - T_0}\right)(T(t) - T_0)$$
(2.9)

This equation allows a direct input into a FEA code for the effective coefficient of thermal expansion as a function of time:

$$\alpha_{eff}(t) = \alpha + \frac{bp_m(t)}{T(t) - T_0}$$
(2.10)

Using the above methodology, predictions of evolving stress in 3D printed structures have been obtained [61] (see Fig. 2.12). This illustrates the set of



Fig. 2.12 Contour levels of normalised stress intensity in the printed layered structure (close view at the edge). Deformed shape magnified by factor f = 5

modelling results showing the state of the structure after printing each of the ten layers. The contours refer to normalised, over range 0–1, stress intensity and detail the stress pattern at the edge of the printed structure. The shape of the layers is the deformed shape illustrated with magnification factor 5. The dotted lines define the original target topology of the ten layers, with each layer thickness being 25 μ m. (total target thickness 250 μ m). Finally, the grey layer above is a schematic representation where 25 μ m of liquid ink is deposited.

The highest stress was found to develop at the edge region of the first layer (due to the assumption for perfect adhesion and pinning the area of the deposited liquid ink) but away from the edge region stress is very low and can be neglected. In terms of the cross-sectional profile at the peripheral edge of the domain of printed layers, there is a lateral offset due to cure shrinkage. This in-plane shrinkage is limited as cured layers beneath provide significant restriction for deformations in this direction. A principal conclusion is that shrinkage affects predominantly the thickness of the printed structure.

2.4 Modelling Applied to Assembly Processes

Modelling of typical assembly or packaging process is discussed in this section. The processes discussed are solder pasting and its reflow and microwave heating to cure polymer materials as used in electronic packaging.

2.4.1 Solder Paste Printing

The stencil printing process is used to deposit solder paste at precise locations on the PCB pads in order to prepare for the placement and bonding of electronic components. In this process a squeegee blade moves the solder paste over the surface of a stencil with a particular pattern of apertures. As a result of the high pressure in the solder paste, induced by the squeegee blade, the solder paste is forced to fill the stencil apertures.

The overall solder paste composition exhibits non-Newtonian rheological properties with shear-thinning behaviour, i.e. the viscosity decreases with increasing shear rate. This behaviour is what enables the paste to flow into the apertures with a low viscosity when the shear rate is high due to the action of the moving squeegee blade. After the removal of the stencil, the viscosity increases again in the absence of shearing, a phenomenon which helps the paste to remain in place.

Computational fluid dynamics (CFD) can predict the movement of solder paste across a stencil surface. For example, simulation of the paste motion of a solder material with nanoparticles and characterised bulk behaviour can be undertaken using the classical Navier-Stokes equations with the following viscosity model for solder paste [62]:



Fig. 2.13 Modelling predictions for the flow of solder material in the stencil printing

$$\frac{\eta - \eta_{\infty}}{\eta_0 - \eta_{\infty}} = \frac{1}{1 + K\lambda^m} \tag{2.11}$$

where η is the apparent viscosity; η_0 and η_∞ are the viscosity at zero and infinite shear rate, respectively; λ is the strain rate; and *K* and *m* are experimentally obtained constants. Figure 2.13 shows the schematic of the printing process and associated CFD predictions for solder flow using a classical continuum approach.

Traditional CFD simulations based on the continuum simulation approach assume homogeneous fluid and may not provide realistic answers about the transport of the individual solder nanoparticles. To understand the flow of the solder paste into the stencil apertures, coupled continuum-particle computational methods are required.

Among the most attractive discrete particle-based fluid dynamic computational techniques are Stokesian dynamics [63] and mesoscopic approaches such as Lattice-Boltzmann methods (LBM) [64] or dissipative particle dynamics (DPD) [65].

Stokesian dynamics is a method in which only forces between the particles of the solid phase are considered, and the detailed flow of the suspending fluid is not simulated. The interparticle forces are based on lubrication theory, where the drag on a particle is dependent on the position and velocity relative to that of its neighbouring particles or solid walls as well as the average local velocity of the suspending fluid [63]. Some major drawbacks of this method include the lack of detail for the flow of the suspending fluid and difficulties with mass conservation. Stokesian dynamics is also considered to be inefficient for suspension flows in comparison to mesoscopic methods.

Mesoscopic approaches are similar to molecular dynamics but replace the fluid molecules with much larger fictitious particles that can be considered to represent accumulations of the real underlying molecules. Computer memory requirements are therefore smaller, and collision timescales are closer to that of the evolution of the macroscopic flow. The properties of these fictitious particles are set so that they mimic the flow behaviour of the underlying real fluid at the macroscopic scale. These methods are therefore referred to as mesoscopic since they lie somewhere between microscopic atomistic and macroscopic continuum approaches. Dissipative particle





dynamics (DPD) methods are based on attractions and repulsions which are dependent on the relative positions and velocities of the particles relative to each other.

Hybrid models for coupled nanoscale dynamics with macroscopic continuum flow behaviour try to benefit from a multi-scale approach for simulating the solder paste printing process [66]. Figure 2.14 (left) shows simulation results for solder paste printing using a hybrid analysis approach. The velocity field of the DPD simulation region is represented by particulate region. The continuum and particle regions overlap by a narrow band A–D (Fig. 2.14, right) with two defined subregions A–B and C–D. Strip A–B of the particle domain coincides with the boundary of the continuum region. Similarly, strip C–D of the continuum domain coincides with the boundary of the particle simulation. Mass and momentum flux densities are measured and coarse-grained in band A–B of the particle field and imposed at the boundary of the continuum field.

2.4.2 Molecular Dynamics Calculation of Solder Reflow Process

In the lead-free soldering technology area, Dong et al. used the modified embedded atom method (MEAM) and the molecular dynamics method to study the collapsing and merging behaviour of tin and silver particles [67]. One of the aims of this work was to find out if the mechanical mixture of tin and silver nanoparticles can replace the SnAg alloy for low reflow temperature applications. The modelled particles were all 4 nm in diameter and contain 1257 and 1895 atoms, respectively. The total simulated time was 3 ns. It turned out that the silver sphere kept its crystalline structure, and no significant diffusion between tin and silver was observed within the simulation time.

2.4.3 Microwave Heating in Microelectronics and Nano-packaging Applications

Microwave energy fundamentally accelerates the cure kinetics of polymer materials [68], providing a route to focus heat into the polymer materials, minimizing the temperature increase and associated thermal stresses in the surrounding materials.

A number of systems using microwave energy to cure microelectronics components are in use today. The novel 'FAMOBS' [69, 70] system proposed by Sinclair et al. [71] uses an open-ended oven mounted on a pick-and-place machine which is capable of heating/curing a single component at a time, thus reducing/eliminating the issues related to generation of unnecessary thermal stresses.

In order to accurately model the process of microwave polymer, curing a holistic approach must be taken. The process cannot be considered to be a sequence of discrete steps, but must be considered as a complex coupled system combining electromagnetic and thermophysical behaviour of the whole system because each of these processes fundamentally influences the other, as illustrated in Fig. 2.15.

A significant problem in the analysis of microwave heating is the disparity in timescales between the electromagnetic and thermophysical problems. Microwave sources operate in the range of 1–30 GHz. Therefore substantial variation in the electric field distribution is apparent at sub-picosecond timescales. Significant variation in the thermophysical properties is only apparent in timescales of seconds (one trillion times the duration). A method for linking pico-scale to macro-scale analyses is critical to solution of the problem.

A number of methods have been employed to determine a suitable steady-state electric field distribution. These methods generally rely on the electric fields reaching a time-harmonic state in which the field magnitude varies rapidly but the distribution of the modal structure remains invariant. If a time-harmonic state is reached (or assumed to have been reached), the fields magnitude can be assessed through using a time-averaged or root mean square value or through the use of a (normally discrete) Fourier transform. The transformed electric field is used to determine the power absorbed by the dielectric load, and the differences between successive values of absorbed power at successive Fourier transfer analyses are used to determine if a converged time-harmonic solution has been obtained.



Fig. 2.15 Process coupling in microwave heating of polymers

2.5 Modelling Applied to Reliability Predictions

Modelling applications for final reliability prediction of an electronic package are discussed below. The impact of how nanotechnology may influence reliability and how this can be modelled is discussed for both underfills and anisotropic conductive films and thermal interface materials. The impact of very small joints and current crowding effects is also outlined.

2.5.1 The Effects of Underfills on Solder Joint Reliability

Underfills are widely used in the packaging industry to offset the damaging effects of CTE mismatch on interconnections such as solder joints between a chip and the substrate in a flip chip assembly. The effectiveness of an underfill in reducing the impact of CTE mismatch mainly depends on its thermal-mechanical properties such as the Young's modulus and the CTE. Other important properties of an underfill include the heat conductivity, the moisture absorption, the viscosity, etc. All these properties may be modified by adding filler particles such as silica into the polymer matrix. The underfill properties can be modified by changing the filler particle properties [72] or by changing the filler content.

The filler content is an important issue especially for no-flow underfills because on the one hand, it is desirable to have high filler content in order to achieve low CTE, but on the other hand, high filler content degrades the flow properties of the underfill making the process prone to defect formation in the underfill and at the solder-pad interface [38]. Figure 2.16 shows one defect developed during a no-flow underfill process.

Because of the low filler content, no-flow underfills have higher CTE than traditional capillary underfills. To investigate the effect of this on the lifetime of flip chip solder joint, Lu et al. [73] modelled the lifetime of a flip chip's fatigue



Fig. 2.16 Solder joint cross-sections. (a) Underfill trapping between solder bump and pad. (b) Good bonding between solder bump and pad



Fig. 2.17 The flip chip computer model that has been used in the study of the effects of the no-flow underfill material



Fig. 2.18 The predicted lifetime of the flip chip solder joint. (a) The traditional underfill. (b) No-flow underfill

lifetime under cyclic thermal-mechanical loading for a range of underfill properties. Figure 2.17 shows the 3D FEA model used in the modelling, and Fig. 2.18 shows the predicted lifetimes. The results show that flip chips using no-flow underfills have significantly lower lifetimes than traditional underfills. In order to achieve the highest reliability, the CTE of the underfill needs to be brought down to about 20 ppm/°C.

The solution to this problem may be the use of nanosized filler particles [74, 75] because this technology may increase the filler content without compromising the

solder joint quality. Lall et al. [76] have developed a method based on representative volume element (RVE) and modified random spatial adsorption to predict the temperature-dependent underfill properties. Their results show that when the volume fraction of the filler content is higher than 30%, the CTE is lower than 40 ppm/°C which is close to the capillary underfill's value.

Modelling the behaviour of underfills in advanced packaging application poses the challenge of capturing as accurate as possible the temperature-dependent material behaviour. Research efforts in this direction resulted in better understanding of underfill properties and development of relevant viscoelastic models. For example, work carried out by Chhanda established the viscoelastic mechanical response of a typical underfill encapsulant [77]. The behaviour in this study was characterised via rate-dependent stress-strain testing over a wide temperature range and via creep testing for a large range of applied stress levels and temperatures. The research team also investigated the effects of moisture exposure on the mechanical behaviour of flip chip underfills in microelectronic packaging [78].

2.5.2 Modelling of Anisotropic Conductive Films (ACFs)

Anisotropic conductive films (ACFs), with many distinct advantages such as extreme fine pitch capability, being lead-free and environmental friendly, are being widely used in fine pitch flip chip technologies [79]. A typical ACF flip chip is shown in Fig. 2.19. The conductive particle is a nickel gold-coated polymer ball with a diameter of 3.5 μ m. In order to improve the electrical performance of ACFs' assembly, nanoscale conductive fillers are being considered for the next generation of high-performance fine pitch packaging applications [80, 81].

Computer modelling analysis, in particular finite element analysis, is being used as a powerful tool to predict the behaviour and responses of ACF particles during the



Fig. 2.19 ACF flip chip and structure of a conductive particle



Fig. 2.20 Mesh details of the macro and micro models of an ACF assembly

bonding process and reliability testing. However, previous modelling work [82, 83] has been mostly limited to the analysis of simplified two-dimensional models. Three-dimensional models have focused on the microdomain and ignored global effects at the package level, or they have modelled the whole package and used gross assumptions at the micro interconnect level [84–86]. The recognised difficulty here is due to the vast range of length scales in an ACF flip chip assembly and the large number of conductive particles.

The diameter of the conductive particles in the ACF material is several micro metres, and the thickness of the particle metallisation is in nanoscale, which is about 50 nm. If the die is 11 mm in its length, the ratio of the two is approximately 1: 200,000. In addition, there are thousands of conducting particles in a typical ACF material used to bond a flip chip component to a substrate. This means that an 'exact' model which includes all the particles and interconnections would require millions if not billions of mesh elements to be used in a finite element model. This is simply not achievable with today's computer technology.

Therefore, a 3D macro-micro modelling technique is required in order to provide the ability to accurately model the behaviour of the conductive particles during the reliability test. Two models, one macro and one micro, with very different mesh densities were built (see Fig. 2.20). The macro model is used to predict the overall behaviour of the whole assembly during reliability testing. The displacements obtained from this macro model are then used as the boundary conditions for the micro model so that the detailed stress analysis in the region of interest could be carried out. This macro-micro modelling technique enables more detailed 3D modelling analysis of an ACF flip chip than previously.

Using this modelling technique, the moisture diffusion and induced stresses inside an ACF flip chip when subjected to autoclave test environment were predicted [87, 88]. Modelling results were consistent with the findings in the experimental work.

2.5.3 Metal Migration-Related Damages in Nano-packaging

Metal migration is a truly multi-physics and multi-scale phenomenon. It is due to atoms in the metal migrating due to thermal, electrical and stress gradients. For example, electromigration (EM) in the on-chip interconnection/metallisation of Al or Cu has been the subject of intense study over the last 40 years [89, 90]. Recently, because of the increasing trend of miniaturisation, high current density-induced damages are becoming a growing concern for off-chip interconnection where low melting point solder joints are commonly used. EM is atom transfer due to a high current density.

Unlike Al and Cu metallisation, Joule heating from the interconnect line can severely effect the damage characteristics of solder joints. Moreover, current crowding at the contact interface between the solder ball and the metal pad/underbump metallisation (UBM) increases the local current density and local resistance of the solder alloy that further increase Joule heating and yields a localised hot spot [91]. In that case, atoms migrate from the hot spot to the remaining cooler region, and this is known as thermomigration.

Thermomigration may assist EM if the hot side coincides with the cathode side [91-93].

In summary there are seven major phenomena associated with electro- and thermomigration [94]. They are (i) EM (mass transfer due electron bombardment), (ii) thermomigration (mass transfer due to thermal gradient), (iii) enhanced intermetallic compound (IMC) growth, (iv) enhanced UBM dissolution, (v) enhanced current crowding, (vi) high Joule heating and (vii) solder melting.

Multi-physics models are required to predict the combined effect of electromigration, thermomigration, current crowding, Joule heating, thermal stress and local melting phenomena. These need to capture IMC growth and UBM dissolution for solder interfaces under high current density.

Current crowding is always found to play a vital role in such a sensitive packagelevel interconnect, in particular such as a flip chip solder joint. High growth/ dissolution of IMC/UBM at the current crowding area will be encountered. This is because of typical flip chip solder joint design where a spherical solder is connected with the thin-film metallisation (see Fig. 2.21). With the shrinking trends of interconnects in nano-packages, this current crowding effect increases exponentially.

A detailed review of modelling techniques for EM and a multi-physics framework for solving the coupled electro-thermal-mechanical equations for electromigration, thermal migration and stress migration is provided in [95]. The modelling approach shows that the electric current, temperature and stress can be solved simultaneously, and the vacancy concentration can be predicted in a seamless framework. The design considerations for resisting EM are also discussed in this work, and a shunt structure for a solder joint pad is proposed, and its potential for the reduction of EM risk is demonstrated.



Fig. 2.21 Typical example of current crowding in the flip chip solder joint. (**a**) Schematic of flip chip solder joint and current crowding region; current density distribution in a slice through the line AB shown in Figure (**a**) considering 1 Amp current passing through the joint. Current density at the current crowding area is ten times higher than that of the other area for the same slice

2.5.4 Thermal Interface Materials

High-performance thermal interface materials (TIMs) with excellent thermal conductivity are needed to provide effective heat dissipation and avoid the occurrence of overheating; see Fig. 2.22a, b. This can be achieved by using polymer nanocomposites, i.e. a polymer (a matrix material) reinforced by fillers, e.g. carbon nanotubes (CNTs) or various ceramic fillers.

Recently ceramic fillers have attracted significant interest. Aluminium nitride (AlN) and boron nitride (BN) are considered ideal candidates as fillers for TIM composites because of their high thermal conductivity, low CTE and low dielectric constant and of being nontoxic [96–99].

Modelling is a useful tool for predicting specific properties of the resulting material such the effective thermal conductivity K_{eff} , where both numerical and theoretical approaches have been developed to complement experimental work [100]. However, the results of analytical predictions do not often agree well enough with experimental data, especially when the filler concentration is high [101].



Fig. 2.22 TIMs: (a) use in microelectronics, (b) heat dissipation through TIM

For most semiconductor and dielectric materials, phonons (quantised lattice vibrations) are the main energy carriers for heat conduction. One of the most important characteristics of phonon transport is the mean free path Λ , i.e. the average distance travelled by a phonon between successive collisions. If the filler particle size *L* in a composite is of the same order as the phonon mean free path Λ , then thermal transport is ballistic, and it cannot be simply captured by the Fourier heat conduction theory; see, e.g. [102]. In this case, Boltzmann's transport equation (BTE) is used to determine thermal characteristics of the composite:

$$\frac{\partial f}{\partial t} + \mathbf{v} \cdot \nabla_{\mathbf{r}} f = \left(\frac{\partial f}{\partial t}\right)_{scat},\tag{2.12}$$

where *f* is the phonon distribution function, *t* is time, **v** is the phonon group velocity vector and **r** is a position vector. The left-hand side describes the drift of the phonon, which causes the departure from an equilibrium position of an atom within a crystal lattice. The right-hand side of the equation represents the *phonon scattering* term, which restores the equilibrium. There are three principal approaches used for finding K_{eff} based on simulation of phonon transport:

- Deterministic methods; however, it is extremely difficult to find a solution of the BTE using these methods.
- Monte Carlo methods (see, e.g. [103–105]) that simulate the process of phonon transport, so that the results of that simulation can be seen as a numerical solution of BTE.
- Molecular dynamics (MD) simulations [106–108] that are limited to a very small length and timescales.

If the particle size and the size of the sample are bigger than the phonon mean free path, i.e. $L >> \Lambda$, thermal transport is diffusive, and solutions can be obtained by solving Fourier's law across the length scales. Fourier heat conduction theory is well established, and there are numerous software pieces that are able to solve the relevant equations numerically [109–111].

If the molecules of a polymer matrix are on the same size scale as the filler particles, then it is very important to handle the problem of defining the value of the thermal boundary resistance (TBR) at the filler/matrix interface since the TBR can essentially affect thermal flow [103]. No effective analytical or experimental techniques are known for determining TBR, and MD simulations can be employed.

One of the possible approaches to the numerical modelling of thermal properties of bimodal composites with ceramic fillers is presented below. The composite under consideration contains a polymer as a matrix and two filler materials: BN flakes of nano-thickness and AlN particles of micro size. The volume fractions of the two inclusions are equal, i.e. their volume concentration ratio is 1:1, and the total volume concentration of filler particles does not exceed 80%. Here, one of the challenges is to handle the large difference in length scales among filler particles, i.e. a great aspect ratio of some fillers. Moreover, the flakes of BN being of nano-thickness have widths that lie in the micrometre range, i.e. the ratios between the size parameters may exceed several thousands.

Another difficulty is that the composite, as a multiphase medium, is highly sensitive to the geometry and the spatial arrangements of the fillers. To address the multi-scale issues of the problem, it is split into three stages; see Fig. 2.23. In the first (nanoscale) stage, thermal conductivities of the BN/polymer composite in two perpendicular directions are determined to capture the anisotropic nature of thermal conductivity. It is assumed that all plates of BN are parallel to each other. The output of Stage 1 is then considered as two composite materials: Material 1, with horizontal orientation of BN flakes, and Material 2, with vertical orientation of flakes. The computational domain on this stage is randomly filled with 'squares' of Material 1 and Material 2, 20 for each side of the domain. In order to determine isotropic thermal conductivity of BN/polymer composite, 30 different domains are randomly generated. In the third stage, the isotropic values of thermal conductivity of BN/polymer composite are considered as a matrix for the bimodal composite with AlN particles as an inclusion. The final effective thermal conductivity is obtained as



Fig. 2.23 Three-stage modelling approach for determining effective thermal conductivity of the bimodal system



Fig. 2.24 Thermal conductivity of AIN/BN/polymer composite for various values of AIN diameter

an average of 30 simulations for domains with different randomly generated AlN particle distributions and with a given filler volume concentration.

The results of numerical simulations will be more realistic, provided that a numerical model includes TBR. In Stage 1 of the described methodology, the values for TBR at the BN/polymer interfaces (obtained either from MD simulations or from available literature) can be included as an additional input parameter into numerical calculations. In order to determine how thermal conductivity of the final composite depends on the sizes of the AlN particles, a parametric study has been conducted. A reasonable value of 5.e-8 Km²/W for TBR has been taken as the internal boundary condition. As can be seen from Fig. 2.24, thermal conductivity of the AlN/BN/ polymer composite increases with increasing the AlN particle diameter. The thermal conductivity rate of growth gets slower with an increase of AlN diameter.

The numerical predictions are in good agreement with the Maxwell-Eucken prediction, which can be explained by the fact that the latter formula is valid for concentrations of spherical particles (AlN) below 40%; see [100].

Good agreement can be observed even for a higher filler concentration. For example, for a mono-composite characterised by the filler thermal conductivity $k_f = 250$ W/(m·K), particle diameter D = 275 µm and the matrix thermal conductivity $k_m = 0.31$ W/(m·K), the graphs for thermal conductivity k determined by the Maxwell-Eucken formula and by the numerical approach based on the steady-state heat transfer equation, start diverting when the volume concentration of the filler exceeds 61%; see Fig. 2.25. This concentration value is actually the percolation threshold for the composite, so that for a concentration higher than 61%, thermal conductivity starts growing essentially faster, and that phenomenon is not reflected in the Maxwell-Eucken formula.

The described numerical modelling methodology provides a route to determining thermal conductivity of complex composite mixtures containing multi-scale filler



Fig. 2.25 Numerical and analytical predictions for the composite thermal conductivity

particles. This cannot be achieved using analytical methods, especially for high concentrations of fillers.

2.6 Conclusions

Modelling technology is now used extensively in industry and research institutions as a key tool to help produce reliable products and reduce cost and lead times from conceptual design to product introduction to the market.

The move towards nano-packaging poses a number of challenges for modelling tools. The multi-physics/scale challenge is being addressed by a number of software vendors although much needs to be done to validate these tools. The addition of uncertainty analysis within a physics-based modelling environment is very important as the scales of nano-packaging are not deterministic, and a risk-based approach is required to fully understand how input design variables will impact packaging assembly and reliability. Integrating modelling results within a whole life cycle analysis approach is also very important and will be a major requirement for modelling tools in the future.

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Chapter 3 Advances in Delamination Modeling of Metal/Polymer Systems: Continuum Aspects



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3.1 Introduction

Microelectronic packages are typically composed of various materials, like silicon, metals, oxides, glues, and compounds (polymers). In Fig. 3.1, cross sections of leadframe- and substrate-based packages are depicted. Due to the dissimilar nature of these materials and the inherent presence of a large number of interfaces in each component, various failure modes, such as interface delamination, chip cracking, and/or solder fatigue, will occur during processing, (qualification) testing, or usage. The occurring thermomechanically related failures in these components account for more than 65% of the total reliability issues [1].

3.1.1 Delamination-Related Failures in Microand Nano-electronics

As mentioned above, various failure modes can occur in micro- and nano-electronic devices. A division can be made between failures at the device and package levels [1]. Examples of failures at the device level are electromigration, electrostatic discharge (ESD) damage, pattern shift (or metal shift), back-end structure delamination, and Kirkendall voiding. At the package level, examples are stitch break, die

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Fig. 3.1 Cross section of two package families: leadframe- (left) and substrate-based (right). (Courtesy of W.D. van Driel)



Cu/low-k delamination

Underfill/die delamination and cracking

Cu/PDMS delamination

Fig. 3.2 Examples of delamination-related failures in microelectronic packages, flexible displays, and stretchable electronics (EMC epoxy molding compound, PDMS polydimethylsiloxane)

lifting, body cracking, solder joint fatigue, and delamination at various interfaces. Figure 3.2 shows several examples of actually observed delamination-related failures in electronic devices.

The smallest feature sizes on today's dies are already falling to 25 nm and lower, and from the packaging point of view, a similar trend is visible. Die thickness will decrease below 50 μ m, wire diameter below 10 μ m, interconnect pitch below 15 μ m, copper film thickness below 10 μ m, and via diameter in substrates below 10 μ m. However, from a materials science and engineering perspective, industrial development methods can be improved significantly as the required developments are primarily achieved by experimental "trial-and-error" methods [2]. In this context, virtual prototyping and virtual qualification provide a framework to generate optimized designs, resulting in less trial-and-error-based design cycles, thus reducing development costs and time-to-market. Reliable and efficient numerical models and advanced simulation-based optimization methods are therefore required [3, 4]. In fact, development of accurate, robust, and efficient delamination testing and
prediction methods needs our attention today. Not only those material combinations having sufficient resistance to delamination should be selected but also design choices should be made resulting in components that are able to withstand increased forces due to the occurrence of delamination.

3.1.2 Metal-Polymer Adhesion: A Multi-scale Phenomenon

Adhesion and delamination have been pervasive problems hampering the performance and reliability of microelectronic devices (see, e.g., [5]). Different types of dissimilar material interfaces are encountered in microelectronics such as polymer/ metal, metal/ceramic, and polymer/ceramic. According to the ASTM definition (D907-70), adhesion is the state in which two surfaces are held together by interfacial forces which may consist of valence forces or interlocking forces or both. These forces can be van der Waals forces, electrostatic forces, or chemical bonding across the coating/substrate interface. Delamination is the phenomenon that a layer separates from the substrate or matrix in composite materials [6]. It can be driven by mechanical or thermal stress, shock waves, corrosion, electrostatic forces, etc. The thermodynamic work of adhesion, Γ_0 , which defines the energy gained (or expended) to form an equilibrated interface from two equilibrated free surfaces is described by the Dupré equation

$$\Gamma_0 = \gamma_f + \gamma_s - \gamma_{fs} \tag{3.1}$$

where γ_f and γ_s denote the surface energies of the film and substrate, respectively, and γ_{fs} is the film-substrate interface free energy. The thermodynamic work of adhesion can be determined by contact angle measurements [7] or atomistic simulations (see, e.g., [8, 9] and Chap. 4 of this book) although contamination and surface pretreatments can affect this value. Kendall [10] argues that the value of the true work of adhesion occupies a small range from 0.1 to 10 Jm⁻².

In fact, adhesion is a multi-scale phenomenon: at the smallest scale possible, adhesion is defined by the thermodynamic work of adhesion (3.1). At a somewhat larger scale (i.e., micrometer range), adhesion is affected by surface roughness (which results in increased contact surface area and mechanical interlocking possibly resulting in interface crack deflection) [11, 12], microscale viscoelastic [13–15] and plastic deformation [10, 16], and fibrillation [17, 18]. At the macroscopic scale, these additional dissipation mechanisms such as bulk plasticity [19], viscoelasticity [11, 20–22], or friction between the contact surfaces [23–25] affect the measured apparent adhesion or work-of-separation. Evidently, the contribution of each of these mechanisms is sample and loading case specific and can result in macroscopic adhesion energy values of over 1000 Jm^{-2} (see, e.g., [11, 22]).

3.1.3 On the Meaning of the Experimentally Measured Interface Fracture Toughness

There has been considerable activity in devising ways to assess adhesion properties in the past few decades. In fact, a survey of the literature in 1995 indicated that over 350 different techniques were available [26]. The testing methods can be subdivided into pull-off tests (peel and lap shear), super-layer tests, bending tests (three-point, four-point, mixed mode), blister tests, double cantilever beam (DCB), button shear, scratch, end-notch flexure (ENF), and (cross-sectional) indentation tests. The "best" adhesion test method at the macroscopic scale should ideally match the intended application: different setups can lead to different mechanisms of interfacial failure that occur during testing at their own, perhaps different, scales and loading conditions. Nevertheless, these macroscopic characterization techniques are frequently used in academia and industry to quantify adhesion (see, e.g., [6, 27]). Due to the macroscopic approach, quantitative comparison of adhesion results obtained from different test methods is not trivial as different dissipative mechanisms across the scales can contribute differently to the macroscopic adhesion energy. A fascinating example of this difference in microscale dissipation mechanisms is found in the measured work-of-separation in a polymer-coated metal, of which values of 2 J/m² [28], 30 J/m² [29], and 194 J/m² [30] have been reported by different techniques on exactly the same material system.

What is actually measured in macroscopic adhesion tests is the practical work of adhesion, also referred to as work-of-separation [27, 31].

$$\Gamma_i = \Gamma_0 + \Gamma_D \tag{3.2}$$

where Γ_0 is the thermodynamic work of adhesion, and Γ_D contains all dissipative terms that contribute to the work-of-separation, such as plastic dissipation and friction (see above). In terms of fracture mechanics, the crack driving force *G* should be equal to the work-of-separation to propagate the (interface) crack: $G = \Gamma_i$. It is known from literature that the interface toughness Γ_i depends on the mode angle ψ [27, 32]. The mode mixity angle indicates the ratio between the fracture mode II (i.e., sliding mode) and mode I (i.e., opening mode) components and will be defined in (3.12). Consequently, the criterion for interface crack propagation when the crack tip is loaded in mixed mode can be written as

$$G = \Gamma_i(\psi) \tag{3.3}$$

It appears that the interface toughness under far-field mode I loading can be factors smaller than in mode II loading [32, 33]. In fact, the aforementioned additional dissipative mechanisms are the main reason for the mode angle dependency of the interface toughness [16, 27, 32, 34], as these mechanisms are more pronounced under mixed-mode loading conditions. This is illustrated in the buckling-driven delamination section, in particular Fig. 3.8. Experimental characterization methods

that are able to establish the mixed-mode dependency of the fracture toughness have been proposed in literature [33, 35], but will not be discussed in this chapter.

It can thus be argued that the macroscopic adhesion properties are a complex function of all dissipation mechanisms across the scales. Thorough understanding of the significance of each of these dissipative mechanisms is of utmost importance in order to establish physically correct, unambiguous values of the adhesion properties, which can only be achieved by proper multi-scale techniques.

3.1.4 Scope of the Chapter

The topic "Advances in Delamination Modeling" has been split into two separate chapters: this chapter discusses the continuum aspects of delamination, while the next chapter deals with the atomistic aspects of interface separation. The continuum models are typically implemented in a finite element (FE) framework from which the resulting thermomechanical response of a product with appropriate boundary and processing conditions can be calculated. However, due to the decreasing dimensions of the materials, the characterization of their "bulk" and interface properties becomes more critical [5]. In this respect, atomistic modeling methods provide a means to predict and understand these properties and ultimately, to develop materials, interfaces, and components with tailored properties. The basics and challenges of molecular dynamics (MD) will be discussed in the next chapter. Although MD will provide valuable information regarding these properties, the size of the models is still restricted to a very small region of the components under consideration. Hence, the actual combination of both modeling methods will provide a very powerful multi-scale framework for the virtual prototyping of micro- and nano-electronic components.

The chapter starts with a concise overview of the theory on interface fracture mechanics, followed by five "application" sections. The first application is bucklingdriven delamination in flexible displays, in which a combined numericalexperimental approach is used to establish macroscopic adhesion properties, as function of material stack and mode angle. The second application discusses a multi-scale method to identify the relevant dissipative mechanisms in fibrillating metal/elastomer interfaces that are encountered in stretchable electronics. The third application concerns the analysis and prediction of a particular microscale dissipative mechanism at patterned (roughened) interfaces, as a result of the competition between adhesive and cohesive failure. All modeling efforts rely on accurate characterization of material and interface properties, which is addressed in the fourth application. Here, the parameter identification is realized by a very recent method called integrated digital image correlation which essentially eliminates the need for calculating displacements from images prior to parameter identification. The final application of the chapter, although not purely delamination related, is the modeling of the sintering behavior of Ag particles in a thermal interconnect material. The chapter ends with conclusions, outlook, and acknowledgments.

3.2 Interface Fracture Mechanics

Fracture mechanics theory provides a way to evaluate if an already present (or assumed) crack of given geometry and location in a sample is critical. To this end, the energy release rate (ERR), also called crack driving force, as formulated in Griffith's energy balance, is calculated (e.g., [36]):

$$\frac{dW}{da} - \frac{dU}{da} = \frac{d\Gamma}{da}$$
(3.4)

Here, *W* is the external work, *U* is the elastic energy, and Γ is the energy required for crack growth, while *a* is the crack length. Dividing the left-hand side by the specimen thickness, *B*, yields the energy release rate *G* (ERR) in J/m². The right-hand side of (3.4) is called the crack resistance force (after division by *B*). The (simplified) energy balance assumes slow crack growth, absence of kinetic energy, constant temperature, and no dissipation except for the dissipated energy by the fracture process itself. The criterion for crack growth is $G \ge G_c$ where G_c is the fracture toughness in homogeneous materials and the interface toughness when applied at an interface crack. De-adhesion, or delamination, of a thin film can be described by interface fracture mechanics which is covered in great detail in [32, 37]. In the following, only a short summary is presented.

Rice [37] showed that the stresses and displacements exhibit the following typical behavior

$$\sigma_{ij} \sim r^{-1/2} \cos{(\varepsilon \ln r)}, \text{ and } u_i \sim r^{1/2} \cos{(\varepsilon \ln r)},$$
(3.5)

in which the bi-material index

$$\varepsilon = \frac{1}{2\pi} \ln \left(\frac{1 - \beta_D}{1 + \beta_D} \right) \tag{3.6}$$

with β_D the second Dundurs' parameter which is a measure of the mismatch in the in-plane bulk moduli on either side of the interface (Fig. 3.3a).

The expressions in (3.5) indicate that, although the strength of the elastic singular stress field near the tip of an interface crack has the usual \sqrt{r} -singularity, it also exhibits an oscillatory behavior near the crack tip region. This behavior is a characteristic feature of interface cracks and results in a coupling between the stress intensity factors (SIFs) $K = K_1 + iK_2$. Accordingly, the singular stress field can be denoted as follows

$$\sigma_{ij} = \frac{\Re\{Kr^{i\varepsilon}\}}{\sqrt{2\pi r}} \tilde{\sigma}_{ij}^{I}(\vartheta, \varepsilon) + \frac{\Im\{Kr^{i\varepsilon}\}}{\sqrt{2\pi r}} \tilde{\sigma}_{ij}^{II}(\vartheta, \varepsilon)$$
(3.7)

where the local polar coordinates located on the crack front in planes perpendicular to the crack front are represented by *r* and ϑ , and $r^{i\varepsilon} = \cos(\varepsilon \ln r) + i \sin(\varepsilon \ln r)$ is a so-called oscillatory singularity. The functions $\tilde{\sigma}_{ii}^{I}(\vartheta, \varepsilon)$ and $\tilde{\sigma}_{ii}^{II}(\vartheta, \varepsilon)$ describe the



Fig. 3.3 (a) Geometry and conventions for an interface crack; (b) a crack kinking out of an interface

angular distribution of the stresses around the crack tip and are provided by Rice and Sih [38]. As mentioned, a decomposition into pure mode I and mode II is impossible in interface fracture mechanics. Consequently, the SIFs K_1 and K_2 cannot be related directly to these modes. This can be illustrated when rewriting (3.7) along the interface, $\vartheta = 0$

$$\begin{pmatrix} \sigma_{yy} \\ \sigma_{xy} \end{pmatrix} = \frac{1}{\sqrt{2\pi r}} \begin{pmatrix} K_1 \cos\left(\varepsilon \ln r\right) - K_2 \sin\left(\varepsilon \ln r\right) \\ K_1 \sin\left(\varepsilon \ln r\right) + K_2 \cos\left(\varepsilon \ln r\right) \end{pmatrix}$$
(3.8)

It is directly obvious that K_1 is not only associated with the normal stress but also with the shear stress at the interface crack tip. This separation is possible only in the special case of $\varepsilon = 0$.

As can be inferred from (3.7), the stresses in the proximity of the crack tip exhibit, in addition to the singularity, an oscillatory character. This means that the stresses not only become infinitely large but also change sign with an increasing frequency while approaching the crack tip.

The expression for the ERR for an interface crack is given by

$$G_i = \frac{1 - \beta_D^2}{E_*} \left(K_1^2 + K_2^2 \right)$$
(3.9)

where $E_*^{-1} = 0.5(\bar{E}_1^{-1} + \bar{E}_2^{-1})$ and $\bar{E}_i = E_i/(1 - \nu_i^2)$, the plane strain stiffness of material *i*. Consequently, the criterion for interface crack growth is

$$G_i = \Gamma_i(\psi) \tag{3.10}$$

with Γ_i the interface fracture toughness and ψ the mode mixity angle which will be defined below. The crack tip opening displacement vector is asymptotically specified by *K* according to

$$\delta_x + i\delta_y = \frac{8}{(1+2i\varepsilon) \mathrm{cosh}\pi\varepsilon} \frac{Kr^{i\varepsilon}}{E_*} \sqrt{\frac{r}{2\pi}}$$
(3.11)



Fig. 3.4 Schematic illustration of crack tip opening vector (gray arrow) as a result of a far-field mode I loading: the left picture represents the uniform case, while the right picture represents the bi-material case with $E_1 > E_2$

The mode mixity is defined as

$$\psi = \arg(K\ell^{i\epsilon}) = \tan^{-1}\left\{\frac{\Im(K\ell^{i\epsilon})}{\Re(K\ell^{i\epsilon})}\right\}$$
(3.12)

where ℓ is a reference length. Even though in the literature the choice of the reference length has been a topic of discussion, it is rather straightforward to transform mode angles with different reference lengths according to

$$\psi_2 = \psi_1 + \varepsilon \ln \left(\ell_2 / \ell_1 \right) \tag{3.13}$$

Here, mode angle ψ_i is associated with reference length ℓ_i .

Consider an interface crack with a far-field mode I loading, i.e., $\sigma_{yy}^{\infty} \neq 0$, Fig. 3.4. On the left, the uniform case is shown ($\varepsilon = 0$). The crack tip opening vector clearly illustrates that for this case, the mode angle $\psi = 0^{\circ}$. In contrast, for a bi-material interface with $\varepsilon \neq 0$ (in this case, $E_1 > E_2$), far-field mode I loading results in a mixed-mode crack tip loading: $\psi \neq 0^{\circ}$. This example illustrates the fact that the two modes are strictly speaking inseparably connected to each other.

In the above, it was implicitly assumed that the interface crack propagates along the interface. In certain cases, however, the interface crack might kink or deflect into one of the materials. Prior to kinking, the interface crack is loaded with a complex stress intensity factor *K* and mode mixity ψ . Consider an assumed crack of length *a* kinking out of the interface at an angle ω , as depicted in Fig. 3.3b. When assuming that *a* is sufficiently small with respect to all in-plane dimensions (including the interface crack), a relation exists between the kinking SIFs K_I and K_{II} at the tip of the assumed bulk crack and the interface SIFs K_1 and K_2 acting on the interface crack tip [39]

$$K_I + iK_{II} = cKa^{i\varepsilon} + \bar{d}\,\bar{K}a^{-i\varepsilon} + b\sigma_{xx}\sqrt{a} \tag{3.14}$$

Here, $(\overline{})$ denotes complex conjugation, and *c*, *d*, and *b* are complex solution coefficients dependent on material properties and kinking angle ω . He and Hutchinson [40] tabulated solution coefficients *c*, and *d* for certain material combination, while He et al. [39] accounted for parallel normal stress σ_{xx} . Noijen et al. [41] generalized He and Hutchinson's solutions for arbitrary material combinations.

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The expression of the ERR for a kinked crack (e.g., into material "2") is

$$G_c = \frac{K_I^2 + K_{II}^2}{\bar{E}_2}$$
(3.15)

Upon denoting Γ_c as the (mode I) fracture toughness of material 2, the crack kinking condition, based on fracture mechanics theory, can be formulated as

$$\frac{G_c}{G_i} > \frac{\Gamma_c}{\Gamma_i(\psi)} \tag{3.16}$$

Within an FE framework, several methods exist that can be applied to describe (interface) crack initiation and propagation. For crack propagation analysis in linear elastic materials, the ERR can be calculated by the so-called J-integral as explained in, e.g., [36]. Several alternative methods exist to calculate the ERR, like the virtual crack extension method [42] and the virtual crack closure method [43, 44]. For the calculation of the stress intensity factors, necessary for the determination of the mode angle, several methods have been developed: the interaction integral method proposed in [45] and the crack surface displacement method by using the crack tip opening displacements [46]. Due to the scope of this chapter, these will not be discussed here. In contrast with fracture mechanics theory, cohesive zone modeling, based on the pioneering ideas of Dugdale [47] and Barenblatt [48], does not require an initial crack to be present. Instead, this technique can be used to describe both crack initiation and propagation and is versatile in the sense that it can be applied to brittle and ductile failure behavior. The idea for developing cohesive zone models is that infinite stresses at the crack tip do not exist. Instead, the crack is divided into a stress-free region and a stressed region around the crack tip, loaded by so-called cohesive stresses. Fracture is regarded as a gradual process in which failure occurs across an extended crack tip, or cohesive zone, and is resisted by cohesive tractions [49]. In an FE context, cohesive zone elements are placed between continuum elements. Hence, this method is extremely appealing when considering interface delamination issues [49, 50]. Cohesive zone modeling is applied in several sections of this chapter. Excellent in-depth overviews of computational fracture mechanics methods are provided in [51, 52].

The following sections present application examples of delamination analysis in microelectronic devices.

3.3 Buckling-Driven Delamination in Flexible Displays

Multilayered materials consisting of polymers are commonly used as a flexible substrate for flexible displays. The flexible substrate is typically coated on both sides with an inorganic/organic hybrid coating that acts as a gas barrier, increases the scratch resistance, and is called a hard coat (HC) layer. On top of the HC layer, a transparent conducting oxide layer such as indium tin oxide layer (ITO) is used [53, 54]. To achieve high reliability and integrity of the display, proper adhesion between all layers is imperative. High compressive strains in the thin layer as a result of processing and bending, in combination with initially insufficient adhesion at the interface, can cause the layer to buckle and to delaminate from the substrate. This buckling-driven delamination failure mode is caused by the coupling of buckling and interfacial delamination [32, 55] and has been identified as the dominant failure mechanism for compressed layers [56, 57].

This section discusses a macroscopic approach to quantify the effect of adding an HC layer between the substrate and the ITO layer on the adhesion properties by means of a combined experimental-numerical approach. For this purpose, samples with and without HC layer have been processed. Due to the fact that the layers in the samples are brittle, standard available experimental methods (e.g., peel testing) are not applicable. For this reason, a two-point bending setup has been applied [55]. With this method, additional to the residual strain present due to the processing of the multilayered structure, a mechanical strain is applied by bending the sample.

3.3.1 Experiments

To study the effect on adhesion of adding an HC layer between substrate and ITO layers, two material systems are considered: a two-layered ITO/AryliteTM and a four-layered ITO/HC/AryliteTM/HC structure. Firstly, 250 nm ITO layers are deposited on a 200 μ m thick polymer bare substrate (AryliteTM, Ferrania Imaging Technology). Secondly, 250 nm ITO layers are deposited on AryliteTM coated with a 3 μ m silica-acrylate hybrid coating (the HC layer). Details of the processing of the samples are provided in [57].Residual compressive strains are observed after sputtering of the ITO layers in both sample designs. These strains arise from the difference in thermal expansion coefficients of the layer and the substrate and from the difference in the temperature during deposition and subsequent cooling to room temperature. Assuming a thin layer on a thick substrate, Röll's equation [58] can be used to estimate the residual strain induced in the ITO layers

$$\varepsilon_f = \frac{h_s^2}{6h_f} \frac{\bar{E}_s}{\bar{E}_f} \left(\frac{1}{R_2} - \frac{1}{R_1} \right) \left[1 + \frac{h_f}{h_s} \left(\frac{4\bar{E}_f}{\bar{E}_s} - 1 \right) \right]$$
(3.17)

Here, the labels *s* and *f* indicate the Arylite substrate and the ITO film. R_1 and R_2 are the radii of curvature before and after layer deposition, respectively. Since both the bare substrate and the HC/substrate/HC are flat before depositioning of the ITO layer, $1/R_1 \approx 0$. Directly after depositioning, the radius of curvature R_2 is measured using eight specimens from which the residual strain can be evaluated using (3.17). A mechanical two-point bending device is used to apply a deformation with constant curvature to the samples [55], Fig. 3.5a. As the thickness of the ITO layer is much smaller than the substrate thickness, the neutral line is approximately located at the midplane of the layered structure [59]. The applied strain is then calculated from



Fig. 3.5 (a) The mechanical two-point bending device used to deform the sample. (Picture courtesy of C. van Rekum); (b) 2D buckling-driven delamination model of the two-layer system (not to scale)



Fig. 3.6 Confocal microscope images of (**a**) straight and (**b**) telephone cord buckle morphology. The bending strain is increased from (**a**) to (**b**). (Pictures are courtesy of A. Abdallah)

$$\varepsilon_{app} = \frac{h_s + h_f}{2K} \tag{3.18}$$

in which *K* is the bending radius. The total strain in the ITO layer is assumed to be the sum of the residual compressive strain and the applied compressive strain.

The buckle morphology and profiles are measured by atomic force microscopy AFM and confocal optical microscopy. As a result, the buckling morphology can be studied as a function of prescribed strain [55], as illustrated in Fig. 3.6. By increasing

the curvature, and thus the compressive strain in the sample, the straight buckles transform, under certain conditions, into the telephone cord morphology.

3.3.2 Numerical Analysis

In order to establish the adhesion properties for both samples, two-dimensional, plane strain, numerical models for both systems are applied that incorporate the transient buckling-driven delamination process, Fig. 3.5b. Cohesive zone (CZ) elements (e.g., [49, 60]) are used to describe the initiation and propagation of interface failure. Here, the cohesive tractions are calculated from a traction-separation law (TSL), providing the relation between the normal and shear components of the traction vector $\mathbf{t} = t_n \mathbf{n} + t_s \mathbf{s}$ and the separation vector $\boldsymbol{\delta} = \delta_n \mathbf{n} + \delta_s \mathbf{s}$. The effective opening δ and effective traction t are introduced according to [49]. Following [61], an exponential Smith-Ferrante TSL is adopted

$$t = t_{max} \frac{\delta}{\delta_c} \exp\left(1 - \frac{\delta}{\delta_c}\right) \tag{3.19}$$

The parameter δ_c is the effective separation at which the maximum traction, or interface strength, t_{max} is reached. To incorporate the history dependency of the Arylite substrate, a nonlinear elastoplastic model is adopted from [62]. The ITO and HC layers are assumed to deform elastically, with properties given in [57]. As the loading condition, a compressive strain is prescribed which contains the residual strain and the externally applied (bending) strain, (3.17) and (3.18). The model has been validated by solving a benchmark problem regarding buckling delamination of a thin film on a rigid substrate [57].

For the two-layered and four-layered structures, the substrate radii were measured directly after deposition using eight specimens. Applying Röll's equation (3.17), the residual strains were obtained: in the ITO/Arylite samples, $\varepsilon_f = 1.70\%$, while for the ITO/HC/Arylite/HC samples, $\varepsilon_f = 0.95\%$. However, layer buckling-driven delamination was not observed. Buckle delamination perpendicular to the bending axis occurred only when an additional compressive load was applied with the mechanical bending device. For the ITO/Arylite structure, layer buckling was observed for a total compressive strain above 2.0%, while for the ITO/HC/Arylite/HC structure, buckling occurs at a compressive strain above 1.18%; see Table 3.1 [57]. Larger buckles were found for the ITO/HC/Arylite/HC structure.

In [57], an analytical model is presented to calculate the interface toughness. However, this model does not incorporate plastic deformation in the substrate, while also the effect of a compliant substrate is approximated. For this reason, the numerical model is used to estimate the interface properties in terms of the CZ parameters Γ_i and t_{max} . For this purpose, the buckle geometries obtained from the numerical simulations with varying CZ properties will be matched with the experimentally measured dimensions. For the two-layered system, Γ_i is varied between

Sample	2b [µm]	w [µm]	ε [%]	$\Gamma_i [J/m^2]$	t _{max} [MPa]	ψ[°]
Two-layer	5.2	0.24	2.04	31.9	116	71
	3.7	0.14	2.33	63.7	106	81
Four-layer	12.0	0.97	1.18	11.8	188	64
	17.0	1.20	1.51	14.1	184	75
	20.3	1.35	1.58	15.4	196	79

 Table 3.1
 Overview of experimental and numerical results (buckle width 2b and buckle height w)

20 and 80 J/m² and t_{max} between 50 and 200 MPa. For the four-layered system, Γ_i is varied between 5 and 20 J/m² and t_{max} between 50 and 200 MPa. The dependencies of the buckle height and width on the CZ parameters are obtained by determining response surface models (RSM) [63].

In Fig. 3.7, the thus determined height and width RSMs are depicted for both systems at a given strain value. It can be observed that for the two-layered sample, the interface strength has a significant impact on the buckle geometry, while for the four-layered system, t_{max} does not significantly influence the buckle geometry. In [57], this could be explained by the occurring plastic zone in the substrate surrounding the delamination front in the two-layered sample: the larger the t_{max} , the larger the plastic zone size.

The buckle width 2*b* and height *w* were determined using AFM and confocal microscopy and are given in Table 3.1, for several measurements. By matching the experimentally determined buckle geometries with the values from the RSMs, the CZ parameters are established and are given in Table 3.1 as well. It can be observed that the interface toughness for the two-layer samples is larger than for the four-layer samples, for all cases considered. Hence, adding a HC layer effectively weakens the adhesion of the ITO layer. This is not only caused by the occurring plastic deformation at the delamination front in the two-layered system resulting in a higher toughness value but also by the change in intrinsic adhesion due to the presence of a different material attached to the ITO layer (i.e., HC instead of Arylite). It is remarked that both effects are accounted for in the numerical model in a macroscopic sense as a result of the lumping approach. As mentioned earlier, for either a plastically deforming substrate or film, $\Gamma_D \neq 0$ (3.2). Following [16], the height of the plastic zone can be approximated as

$$H_p = \frac{1}{3\pi(1-\nu^2)} \frac{\Gamma E}{\sigma_\nu^2} \tag{3.20}$$

which yields $H_p = 0.5 \,\mu\text{m}$. This corresponds to $2t_f$ implying that large-scale yielding occurs. This essentially corroborates the statement by Wei and Hutchinson that "only film/substrate systems whose interface toughness is on the order of 1 J/m² or smaller are likely to satisfy small scale yielding when the film thickness is on the order of 1 μ m" [16]. The interface strength for the two-layer samples is lower than for the four-layer samples, which suggests a more ductile interface behavior of the two-layer samples and a more brittle interface behavior of the four-layer samples.



Fig. 3.7 Buckle height and width response surface models, for (**a**, **b**) the two-layered system at $\varepsilon = 2.33\%$ and (**c**, **d**) the four-layered system at $\varepsilon = 2.50\%$

Tvergaard and Hutchinson [19] argue that mode angle-dependent interface toughness values are caused by localized plastic deformations in the process zone. In fact, the importance of mode-dependent interface toughness values on occurring buckle morphologies, such as the straight and telephone cord ones, is emphasized in [64]. The obtained work-of-separation Γ_i as function of the mode angle ψ is depicted in Fig. 3.8. The results show increasing interface toughness values as function of increasing mode angle. Furthermore, it appears that in the two-layered system, in which more plastic dissipation occurs, this dependency is more distinct. Due to the fact that only a small number of values can be obtained from the experiments, trend lines are included to illustrate the dependency more clearly. It is also concluded that for both samples, the interface is loaded predominantly in shear. The thus obtained results imply that incremental measurements of buckle geometries could be a means to determine a mode angle-dependent work-of-separation $\Gamma_i(\psi)$. A more dedicated



Fig. 3.8 The obtained work-of-separation for both systems as function of the mode angle (the gray trend lines are included for illustration purposes only)



Fig. 3.9 (a) Finite element model showing the straight-sided buckle with a circular front as a result of the prescribed biaxial residual strain; (b) coordinate system at the crack front

approach to determine interface properties covering the full range of mode mixities could be followed by using a so-called mixed-mode bending setup [33, 35].

The above mentioned results were obtained for straight-sided buckles, as illustrated in Fig. 3.6a. A different commonly observed buckling shape is the so-called telephone cord buckle [64, 65] and Fig. 3.6b. To explain the occurrence of this rather distinctly shaped buckle, a three-dimensional fracture mechanics model was used, which departs from a straight-sided buckle having a semicircular front and a buckle width of 30 μ m. The model consists of a hard coat substrate (thickness 3 μ m) and a thin Si₃N₄ film (thickness 400 nm). An assumed biaxial in-plane compressive residual strain is prescribed on the film which results in a buckled film, as illustrated in Fig. 3.9a.



Fig. 3.10 Results along the crack front of the buckle; (a) energy release rate; (b) mode angle; (c) interface toughness function; (d) normalized ERR

To calculate the driving force at the crack front as a result of the residual strain, the ERR along the curved front is calculated by means of the *J*-integral method and is given in Fig. 3.10a. To ensure accurate values of the ERR, a focused crack tip mesh is employed [66], where the size of the collapsed quarter point elements corresponds to 25 nm. It appears that at two locations, the ERR shows a maximum which implies that it is not straightforward to establish the actual direction of crack propagation of the buckle. In addition, the mode angle along the crack front is calculated from (3.12) using the film thickness as reference length, Fig. 3.10b. It can be observed that the mode angle changes significantly over the crack front. In fact, it changes from mixed mode at the front to almost pure mode II at higher θ values (i.e., the sides of the buckle). To account for the typical mode dependency of the interface toughness in a simplified way, the following toughness function is assumed [32]

$$\Gamma_i(\psi) = \Gamma_I^c \left\{ 1 + \tan^2 [(1 - \lambda)\psi] \right\}$$
(3.21)

Even though an arbitrary compressive strain is prescribed, the following values are used: $\Gamma_I^c = 5.0 \text{ J/m}^2$ and $\lambda = 0.3$. Figure 3.10c shows the resulting toughness distribution along the crack front. Due to the increased mode angle, the toughness varies significantly. Consequently, the mode dependency of the interface toughness

can be incorporated by normalizing the calculated ERR with the interface toughness function (3.21) as depicted in Fig. 3.10d. It can be concluded that the crack front is most likely to propagate at the location $\theta \approx 0.3\pi$ and not at the straight side.

This result suggests that the occurrence of telephone cord buckles could be explained by the mode-dependent behavior of the interface toughness. It also appeared that prescribing a uniaxial strain instead of a biaxial strain results in a preference for straight-sided buckles instead of telephone cord buckles. More recently, results of extensive 3D cohesive zone simulations by Faou et al. [67] appear to corroborate this observation as "the configurational instability induces a large mode mixity locally and effectively pins the front" which results in the typical telephone cord buckle shape.

3.4 Multi-scale Mechanics of High Toughness Fibrillating Interfaces in Stretchable Electronics

In stretchable electronics applications, small rigid semiconductor islands are interconnected with thin metal conductor lines on top of, or encapsulated in, a highly compliant substrate, such as a rubber material. The required stretchability of the thin interconnects can be realized by depositing serpentine-shaped interconnects on compliant substrates [68–70]. Fibrillating interfacial systems, such as large elastic-mismatch elastomer-metal interfaces that are typically used in stretchable electronics applications [71], can exhibit remarkably high values of the interface fracture toughness (i.e., $\Gamma_i > 1 \text{ kJm}^{-2}$) [22, 72–74]. The huge gap that exists between the microscopic adhesion energy and the reported macroscopic work-of-separation will be unraveled by means of experimental and numerical multi-scale analysis. This will ultimately lead to guidelines for engineering interfaces with superior macroscopic toughness values.

3.4.1 Experimental Analysis

During peeling of the copper film from the rubber substrate (Sylgard 184 PDMS, Dow Corning), rubber fibrillation is observed at the delaminating copper-rubber interface [72, 73], as illustrated in Fig. 3.11.First, adhesion properties at the macroscopic scale are extracted from 90° peel test experiments. To this end, the fibril-based mode-dependent interface model with a large displacement formulation is adopted from [75]. In this formulation, first Piola-Kirchhoff tractions are employed [76]. Consequently, the required cohesive zone element length corresponds to the initial element length and can be determined unambiguously. The opening and traction vectors are no longer decomposed with respect to a local basis but resolved globally, and thus no distinction is made between the normal and tangential



Fig. 3.11 (a) In situ SEM images of horseshoe interconnects at 100% stretch; (b) in situ ESEM image of the progressing delamination front during a 90° peel test

directions. A single exponential relation between the traction t and separation δ is formulated

$$t = \frac{\Gamma_i}{\delta_c} \left(\frac{\delta}{\delta_c}\right) \exp\left(-\frac{\delta}{\delta_c}\right) \exp\left(\alpha \frac{d}{2}\right)$$
(3.22)

in which the traction vector $\mathbf{t} = t\mathbf{e}$ and the opening displacement vector $\boldsymbol{\delta} = \delta \mathbf{e}$, where \mathbf{e} is the unit vector along the line between corresponding opposite points of the interface, Γ_i the work-of-separation, and δ_c is the separation value at which the maximum traction (interface strength) t_{max} is reached:

$$\delta_c = \frac{\Gamma_i}{\exp(1) t_{max}} \tag{3.23}$$

The parameter *d* describes the opening mode: *d* attains a value between 0 (mode l) and 2 (mode ll). Intermediate values of *d* represent a mixed-mode opening. The mode dependency of the work-of-separation is captured by the parameter α : the interface is stronger ($\alpha > 0$) or weaker ($\alpha < 0$) in mode ll than in mode l. Irreversibility is taken into account by assuming linear elastic unloading to the origin, i.e., elasticity-based damage. More details can be found in [31].

The interface identification method is based on a comparison of the forcedisplacement curves (to extract the work-of-separation) and the lift-off geometry of the rubber during peeling (to extract the interface strength) between the experiment and simulation. Additional validation in terms of strain values along the peel front confirms that the characterized model adequately describes the experiment on the macro- and mesoscale [72]. However, the cohesive zone model is applied on the mesoscale and thus effectively lumps all the relevant phenomena occurring at lower scales onto the cohesive zone model parameters. Figure 3.12 reveals the mismatch between scales: it can be observed that the identified cohesive zone model leads to





spurious tractions on the interface, i.e., non-zero tractions are present in regions where the interface has completely failed. Obviously, this is not a shortcoming of the cohesive zone model itself but a result of the mesoscopic approach employed.

The hyperelastic PDMS material suggests that no energy should be dissipated in the PDMS in the fracture process zone, which implies that the dominant energy dissipation mechanism is the release of elastically stored energy upon fibril failure. However, large stretch ratios are observed in the fibrils, and the response of PDMS in this regime may deviate from a purely elastic response. To estimate the occurrence of any significant irreversible deformations, the 3D topology of the two separated fracture surfaces is measured by means of an optical profilometer, Fig. 3.13a, b. Next, the initial location of the PDMS surface with respect to the copper surface is recovered by applying a customized digital image correlation (DIC) routine [72]. This DIC routine assumes that the PDMS surface is simply inverted with respect to the copper surface, as shown in Fig. 3.13c, implicitly assuming that the copper topology is initially fully covered by PDMS, which seems fair due to the molding process of the samples. The residual image obtained, Fig. 3.13d, serves as a measure of the mismatch between the two surface topologies after delamination. Even though it is impossible to identify each separate contribution to the residual image, it can be argued that the irreversible crack opening cannot exceed the measured residual. The mean residual amplitude is approximately 1 μ m and confirms the hypothesis that the amount of energy dissipated in the fibrils and the nearby PDMS material is negligible.

3.4.2 Numerical Analysis

In order to identify the dominant dissipative mechanisms that explain the high workof-separation values, the experimental observations described above are used to construct a micromechanical model. First, the contribution of fibril mechanics to



Fig. 3.13 (a, b) Optical surface topologies of the delaminated PDMS and copper surfaces; (c) the inverted PDMS topology; (d) the residual topology, i.e., the difference between the copper and PDMS surface topologies; (e, f) reconstructed cross sections, of which the locations are indicated with dashed lines in subfigures (a-d)

the work-of-separation is quantified by means of a micromechanical model of a single fibril, in which the growth of a nucleated fibril up to the moment of fracture is described. Given the large variation in measured stress-strain curves for rubber materials reported in the literature [77], a small-scale single fibril experiment is performed to characterize the material properties and is illustrated in Fig. 3.14.

In the experiment, hollow tips are fabricated from glass tubes (outer diameter 1 mm; inner diameter 0.58 mm). The tip is attached to an aluminum cantilever having a stiffness of 13.0 N/m. After mixing and degassing, the PDMS is poured into an aluminum container. Using a micro-precision stage, the container is moved toward the tip in order to form a capillary bridge. The PDMS is cured for 1 h at 100 °C through the use of a heating stage positioned directly underneath the PDMS container. After cooling down to room temperature, the load is applied through the reversed displacement of the PDMS container at a rate of 30 μ m/s. The experiment is visualized using a Zeiss V20 optical microscope coupled to an AxioCam HR camera, which records 3 frames per second. The tip is tracked using global digital image correlation (GDIC, [78]), which, for the present analysis, is optimized to deal



Fig. 3.14 Illustration of the single fibril experiment: the PDMS material that was initially adhering to the tip (\mathbf{a}, \mathbf{b}) debonds from the tip, resulting in a small protrusion on the fibril, as indicated by the arrow in (\mathbf{c}) . Upon further loading $(\mathbf{d}-\mathbf{f})$, material is drawn from the hollow tip into the fibril, while simultaneously the initial fibril (below the protrusion) is stretched further

with sparse patterns and rigid body displacements. The load on the fibril is calculated from the movement of the tip by using the cantilever stiffness. The approximate accuracy of the force sensor is determined as 2 μ N, which is sufficiently accurate for the present purpose [77]. The mechanical behavior of the PDMS material is described by a hyperelastic Ogden material model, which accurately captures the strain hardening typically observed at large strains. The particular form used here is taken from [79] and is a generalization of the form by Ogden ([80], p. 222). The strain energy density function *W* reads

$$W = \frac{1}{2}\kappa(J-1)^2 + \sum_{k=1}^{N} \frac{c_k}{m_k^2} \left(\lambda_1^{m_k} + \lambda_2^{m_k} + \lambda_3^{m_k} - 3 - m_k \ln J\right)$$
(3.24)

where λ_i are the principal stretches, $J = \det(\mathbf{F})$ is the volume change ratio with \mathbf{F} the deformation gradient tensor, and c_k and m_k are material parameters; κ is a penalty parameter to enforce the near incompressibility of the material. In the simulations,

N = 2. To establish the constitutive parameters, the numerically and experimentally obtained deformed geometries just before the fibril fractures are used.

From the simulations, it appears that the dissipated energy mainly consists of elastically stored energy that is lost through dynamical release upon unstable fibril failure. Consequently, the resulting work-of-separation value is calculated from the macroscopic traction-separation response

$$\Gamma_M = \int_0^{\delta_m^{max}} T_M \, \mathrm{d}\delta_m \tag{3.25}$$

in which T_M is the (homogenized) macroscopic traction and δ_m the microscopic opening [18, 81]. The maximum value of the work-of-separation from a single fibril is calculated from the model: 18 J/m² [77]. Even though this value is significantly larger than the typical values for the microscale adhesion energy (i.e., Γ_0 in (3.2)), yet it remains an order of magnitude smaller than the aforementioned values, and thus, the single fibril micromechanics model is not able to explain the aforementioned high values. For this reason, a discrete multi-fibril model has been developed to analyze the interaction between the fibrils as well as the interaction between fibrils and the adjacent bulk rubber. In this model, fibrils are assumed to fail instantaneously once the magnitude of the average first Piola-Kirchhoff stress p on the fibril's top end reaches the critical stress p_c [77].

First, it is interesting to study the influence of the loading angle on the work-ofseparation. Figure 3.15 shows the deformed geometry for several loading angles. It can be observed that for all loading angles, a volume of bulk material is highly deformed near the critical fibril [82].

From these simulations, the bulk contribution to the work-of-separation is determined, see Fig. 3.16. No significant influence of the loading angle is visible which might appear to be unexpected, as mode dependency is a commonly reported phenomenon for interface fracture toughness values [32, 33, 35]. However, peel tests on these particular metal-elastomer fibrillating interfaces reveal only a negligible mode dependency [72]. These numerical results thus provide a physical explanation for the experimental observations.

Next, the effect of the critical stress is studied. The critical stress is varied between $p_c = 0.5$ MPa and $p_c = 4$ MPa. The resulting deformed geometries are shown in Fig. 3.17. Comparison of the calculated peel front geometries with the experimentally measured shapes [72, 73] confirms the appropriateness of the applied boundary conditions. In addition, it can be observed that for $p_c = 1.0$ MPa, hardly any lift-off geometry is present, while increasing the critical stress leads to an increase in the peel front height, i.e., the fracture process zone increases.

Figure 3.18 depicts the work-of-separation as a function of the peel front height, for all considered fibril widths [82]. Remarkably, the curves almost coincide. Experimentally measured values are included in the figure from which it appears that the predicted work-of-separation values from the numerically obtained peel front height are in good agreement with the experimentally measured values. It can thus be concluded that the mechanisms identified in the discrete fibrils model



Fig. 3.15 Influence of the loading angle on the delamination mechanics, fibril width w = 0.01 mm. The colors indicate the strain energy density [N/mm²]. (a) The fibril reaches the failure criterion. (b) The geometry after instantaneous failure of the critical fibril. (c) SED after failure minus the SED before failure, projected on the geometry before failure



provide a proper mechanistic explanation for the high work-of-separation values of fibrillating metal-elastomer interfaces and emphasize the limits of modeling fibrillating interfaces with a continuum approach. In summary, the high work-of-separation values could be explained by the following phenomena: (i) the dynamic release



Fig. 3.17 Influence of the critical stress p_c on the delamination mechanics. The colors indicate the strain energy density [N/mm²]. (a) The fibril reaches the failure criterion; (b) the geometry after instantaneous failure of the critical fibril; (c) SED after failure minus the SED before failure, projected on the geometry before failure



Fig. 3.18 Work-of-separation versus the peel front height, as a result of the discrete fibrils, for several fibril widths w. Extrapolation of the results indicates a good match with the experimental data obtained for 90° peel tests of the same PDMS grade, indicated by the circles

of the stored elastic energy by fibril fracture, (ii) the spatial discreteness of multiple fibrils as well as the interaction of these fibrils with the adjacent deforming bulk elastomer material, and (iii) the highly nonlinear behavior of the elastomer.

3.5 Competition Between Adhesive and Cohesive Failure at Patterned Surfaces

It is common practice to improve adhesion by surface roughening or micropatterning [83, 84]. Next to the increase of contact surface, the competition between adhesive and cohesive fracture in the vicinity of a patterned interface, i.e., interface crack deflection, is a key mechanism that contributes significantly to the macroscopic adhesion enhancement [12, 41, 85]. To study the effect of interface patterning, contact effects on fracture resistance were considered in [23] by including friction using a (simplified) representation of a patterned interface, as a function of the applied mode mixity. In [34], patterned polymer films on SiO₂ samples with toughness enhancement were studied due to localized plastic deformation in the polymer film and increased interface surface. The effect of nano-patterned roughness profiles between two elastic solids was analyzed in [86]. Zavattieri and co-workers [87, 88] modeled adhesive failure at a sinusoidal surface pattern as a function of pattern geometry and elastic mismatch from which it was concluded that toughness increases due to the surface pattern, but "daughter cracks" that occur ahead of the main interface crack might diminish this effect. In addition, the sinusoidal patterns induced intermittent crack extension with slow (stable) crack propagation and fast (unstable) crack propagation. The effect of adhesive failure in a micro-patterned surface on macroscopic adhesion was studied in [89]. In the aforementioned references, the actual competition between cohesive and adhesive fracture was not taken into account.

In this section, first, experimental results of specifically designed polymer-metal samples that contain a simplified "two-dimensional" micro-pattern illustrate this typical crack deflection mechanism during a four-point bending test. Next, to actually understand this mechanism, a combined energy- and strength-based method is employed which is able to describe the aforementioned competition mechanism.

3.5.1 Experimental Results

The geometry of realistic roughness profiles is stochastic. To prevent any ambiguity in the model results, bi-material interface samples have been processed containing well-defined 2D patterns (Fig. 3.19a). A copper substrate of thickness 0.2 mm is patterned by using an etching process using a specifically designed mask. The Cu substrates are cleaned using a sulfuric acid dip and plasma prior to molding of an



Fig. 3.19 (a) Cross section of the patterned sample; (b) adhesive and cohesive cracking during four-point bending

epoxy molding compound (EMC) of thickness 0.5 mm. The molding is performed at 180 °C and 180 bar followed by a post-mold cure step at 175 °C during 4 h. The resulting structured bi-material is laser cut into strips suitable for four-point bending tests with dimensions $50 \times 8 \times 0.7$ mm³. As common in this particular interface test, a pre-crack in the EMC is applied. As illustrated in Fig. 3.19b, it appears that crack kinking indeed occurs: the adhesive crack propagates from left to right (the "main" interface crack from the four-point bending test), while cohesive cracks propagate into the EMC [85].

3.5.2 Numerical Results

According to the crack kinking criterion (3.16), crack deflection occurs if $G_R > \Gamma_R$ in which $G_R \equiv G_c/G_i$ and $\Gamma_R \equiv \Gamma_c/\Gamma_i(\psi)$. For common epoxies, Γ_c is in the order of 100–500 J/m², while Γ_i for typical EMC/Cu interfaces at the microscopic scale is limited to 10 J/m²; hence $\Gamma_R > 10$. In literature, G_R values beyond 5 have not been reported [40, 41], which means that for the EMC/Cu interface, crack kinking will actually not occur according to this fracture mechanics theory. Recently, a cohesive zone-based method was used to show that competing process zones exist at the moment of crack deflection, but this study was limited to the effect of the ratio of fracture toughness values [90]. It is argued that the actual occurrence of crack kinking is mainly defined by the crack initiation process, and thus, it is imperative to include the effect of the fracture strength values in the analysis. For this purpose, CZ elements are applied that are indeed able to describe crack initiation and subsequent propagation. Adhesive failure is described by the exponential TSL [91] given by

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$$t_n = \frac{\Gamma_i \delta_n}{\left(\delta_n^{max}\right)^2} \exp\left(\frac{-\delta_n}{\delta_n^{max}}\right) \exp\left(\frac{-\delta_s^2}{\left(\delta_s^{max}\right)^2}\right)$$
(3.26)

$$t_{s} = \frac{2\Gamma_{i}\delta_{s}}{\left(\delta_{s}^{max}\right)^{2}} \left(1 + \frac{\delta_{n}}{\delta_{n}^{max}}\right) \exp\left(\frac{-\delta_{n}}{\delta_{n}^{max}}\right) \exp\left(\frac{-\delta_{s}^{2}}{\left(\delta_{s}^{max}\right)^{2}}\right)$$
(3.27)

with t_n and t_s the normal and shear traction, δ_n and δ_s the current normal and shear opening, Γ_i the interface work-of-separation (assumed equal in normal and shear direction), and δ_n^{max} and δ_s^{max} denote the opening values at maximum normal and shear traction, respectively. Following the work of Xu and Needleman [92] for dynamic crack propagation, cohesive failure is modeled by placing cohesive zone elements between all inter-element boundaries. In [93], this model was adapted for quasi-static crack growth. These elements are initially rigid and activated by means of a failure law [94]. Once active, the opening of these elements is governed by an initially rigid exponentially decaying TSL [95, 96]:

$$t_n = t_{max} \exp(h_s \kappa); \quad t_s = d_{int} \exp(h_s \kappa) \delta_s$$
 (3.28)

where, again, t_{max} denotes the cohesive tensile strength, κ is a history parameter that equals the maximum value of the equivalent separation, d_{int} is the unit shear stiffness, $h_s = -t_{max}/\Gamma_c$, and Γ_c the cohesive fracture toughness. The CZ elements in the epoxy are inserted at an inter-element boundary *i* during the simulation, according to a mode I-based failure criterion: $t_n^i > t_{max}$. Here, t_n^i is the normal traction at the boundary *i*, which is obtained by averaging the stresses in the surrounding elements. By dynamically inserting these CZ elements during the simulation, the well-known mesh dependency due to the spurious compliance of initially elastic CZ models is avoided. Due to the localized nature of the cohesive failure, numerical issues may occur in the Newton-Raphson procedure. To avoid these issues, a dissipative arclength solver has been employed [97]. Clearly, this CZ-based model enriches the fracture mechanics crack kinking model in the sense that the effects of fracture toughness and fracture strength ratios are considered simultaneously.

The four-point bending test is modeled according to the dimensions and loading conditions given in Fig. 3.20. In addition, the patterned Cu surface is included (right picture in Fig. 3.20). For copper, E = 123 GPa, and $\nu = 0.33$, while for the epoxy, E = 21,240 MPa, and $\nu = 0.25$. In [85], it is shown that the results (i.e., crack paths) converge upon mesh refinement.

To establish the effect of the cohesive and adhesive failure parameters, the fracture toughness values are varied. The resulting crack paths are depicted in Fig. 3.21. First, it can be observed that the model is indeed able to capture the combined adhesive-cohesive fracture behavior, and the calculated crack paths are rather similar to the experimentally observed paths, even though the filler particles in



Fig. 3.20 Left: the four-point bending model; right: local mesh at the patterned interface



Fig. 3.21 Calculated adhesive and cohesive crack paths for different fracture toughness values: on the left, the adhesive fracture toughness is varied, while on the right, the cohesive fracture toughness is varied. The color bar denotes the damage value in the cohesive elements and ranges between 0 (undamaged) and 1 (fully damaged)

the EMC are not included in the model. Furthermore, the adhesive fracture toughness does not significantly affect the crack paths (i.e., for the applied range), while the cohesive fracture toughness influences the cracks in both shape and fully developed crack size (i.e., damage value = 1).

The initiation location of the cohesive crack can be explained by the local stress concentration in the EMC material at the proximity of the actual semicircular pattern, as shown in Fig. 3.22. Due to the mixed-mode loading from the four-point bend test, a compressive stress is present in the EMC material at the left side of the fillet. However, a tensile stress acts in the EMC at the top of the fillet which causes the cohesive crack to initiate at the moment that the local strength criterion is reached.

Currently, a parametric study is being performed to quantify the effects of strength and toughness ratios at the microscopic scale on the resulting adhesion properties at the macroscopic scale.



Fig. 3.22 Local stress concentrations around the semicircular pattern

3.6 Integrated Digital Image Correlation (IDIC) for Small-Scale Characterization of Adhesion Properties

In order to understand and predict delamination behavior in complex, dense material stacks, as commonly used in microelectronic devices, proper identification of macroscopic constitutive model parameters is essential. As already introduced in the preceding sections, CZ modeling is a versatile manner of describing the failure behavior of interfaces. Typically, as explained in more detail in the introductory section of this chapter, the CZ parameters are identified by mechanical tests at macroscopic scale that are carefully designed so that specific assumptions allow for analyzing material response from limited data (e.g., force-displacement curves). However, the restricted kinematic information may result in inaccurate parameter identification, and it typically calls for more than one test to determine the different parameters. To more rigorously identify model parameters, full-field identification methods are well suited to analyze the details of the deformation process by means of images. At the heart of such a method lies digital image correlation (DIC), which captures full-field kinematics, exhibiting more complete information about material response. Together with the tight integration of FE simulations of the conducted mechanical test, images are correlated in order to optimize the material and CZ parameters, using the method of integrated digital image correlation (IDIC). To illustrate the accuracy and robustness of this enhanced identification method, this section describes the application of IDIC to image data obtained from virtual double cantilever beam (DCB) experiments.

3.6.1 The Integrated Digital Image Correlation Technique

Various (inverse) identification approaches make use of full-field data, such as the virtual fields method [98], the equilibrium gap method [99], the reciprocity gap method [100], and the constitutive gap method [101], of which overviews are given

in the literature [102]. Undoubtedly, the most intuitive and widely used method is that of finite element model updating (FEMU) [103]. Here, constitutive model parameters are optimized by comparing displacement fields from FE simulations with displacement fields acquired through standard DIC procedures on experimental images. More recently, a novel method has been introduced [104] which closely integrates mechanical descriptions of a material with full-field measurements to identify model parameters. The method is referred to as IDIC and eliminates the need for calculating displacements from images prior to parameter identification. Instead, digital images are directly correlated by optimizing the mechanical parameters that govern the deformation of the imaged material. Thereby, the raw experimental data is used (i.e., intensity images), avoiding any processed derivatives of such data (e.g., displacement fields). Hence, the mechanical model steers the correlation procedure, which can be incorporated through either closed-form analytic solutions [104, 105] or FE simulations [106, 107]. In IDIC, the correlation and identification procedures are integrated into a one-step approach, making it distinct from the aforementioned methods, which are two-step approaches where by postprocessing of experimental data precedes the identification procedure. In IDIC, parameter identification is realized by directly integrating the FE simulation with a DIC procedure. In DIC, the residual between images is minimized, assuming conservation of brightness. This can be formulated as follows:

$$f(\mathbf{x}, t_0) \approx g(\mathbf{\Phi}(\mathbf{x}, t)) = g \circ \mathbf{\Phi}(\mathbf{x}, t)$$
(3.29)

$$\mathbf{\Phi}(\mathbf{x},t) = \mathbf{x} + \mathbf{U}(\mathbf{x},t) \tag{3.30}$$

where *f* and *g* are the scalar intensity fields of, e.g., light sensed by a camera sensor, the symbol " \circ " denotes composition of two functions according to $(b \circ a)(\mathbf{x}) = b(a (\mathbf{x}))$, and $\mathbf{\Phi}$ represents the vector function that maps the pixel coordinates \mathbf{x} of image *f*, corresponding to the reference material state, to the pixel coordinates of image *g*, corresponding to the deformed state. The mapping function $\mathbf{\Phi}(\mathbf{x}, t)$ depends on a displacement field $\mathbf{U}(\mathbf{x}, t)$, which can be approximated by FE simulation of a model of the experiment $\mathbf{U}(\mathbf{x}, t) \approx \mathbf{U}_a(\mathbf{x}, t, \theta_i)$, which depends on the constitutive model parameters θ_i . The displacement vector field is to be determined with sub-pixel accuracy, by minimizing the residual Ψ between images *f* and *g* within the spatial domain Ω

$$\Psi = \int_{\tau} \int_{\Omega} \frac{1}{2} [f(\mathbf{x}, t_0) - g \circ \mathbf{\Phi}(\mathbf{x}, t, \theta_i)]^2 d\mathbf{x} dt$$
(3.31)

which results in the following system of equations

$$M_{ij}\delta\theta_j = b_i \tag{3.32}$$



Fig. 3.23 Schematic representation of the IDIC procedure

where the degrees of freedom in the correlation process correspond to the unknown constitutive parameters θ_i . The correlation matrix M_{ij} and the right-hand side term b_i are given in [106]. Hence, optimization of the constitutive parameters θ_i is directly achieved by minimizing this image residual in an iterative Gauss-Newton scheme. A flowchart of the IDIC method is provided in Fig. 3.23.

Besides kinematic information (in the form of images), loading data is required in the identification process for certain parameters [108]. For this purpose, a load residual can be defined as

$$P_F = \int_{\tau} \left[\mathbf{F}_{exp}(t) - \mathbf{F}_{sim}(t, \theta_i) \right]^2 \mathrm{d}t$$
(3.33)

where $\mathbf{F}_{exp}(t)$ is the experimentally measured force vector and $\mathbf{F}_{sim}(t, \theta_i)$ is the numerically obtained force vector and depends on the constitutive parameters θ_i . This objective function is minimized by optimizing the parameters θ_i by means of a Gauss-Newton algorithm.

3.6.2 Virtual Double Cantilever Beam (DCB) Test Case

In [106], the IDIC procedure is employed to identify bulk material model parameters for several examples based on virtual test results. Here, the procedure is used to identify material and interface parameters simultaneously. To this end, a virtual DCB experiment is employed. Instead of taking images of an actual DCB specimen that is deformed during a mechanical test, deformed images are artificially created with the help of FE simulations. Firstly, an artificial speckle pattern is generated by adding several Gaussian gray value peaks. The resulting undeformed reference image can be



Fig. 3.24 The virtual DCB test case: (a) undeformed artificial pattern; (b) deformed artificial pattern

seen in Fig. 3.24a. The coarseness of the pattern is governed by the widths of the Gaussian peaks, which were tuned so that both fine and coarser speckle features are present in the image. This allows for resolving fine kinematics and improves the robustness of the iterative IDIC method, respectively. Displacement fields obtained from FE simulations of a DCB model were used to displace the pixels of the reference image in order to come to a deformed speckle pattern, as seen in Fig. 3.24b. The DCB model utilizes an elastic constitutive model for the two beams, characterized by a Young's modulus and a Poisson's ratio that correspond to spring steel. An exponential TSL law is employed for the glue interface between the beams and is characterized by the interface fracture toughness Γ_i and a critical opening displacement parameter δ_c .

The IDIC procedure is applied to not only identify the interface parameters but also the elastic properties of the beams. The following errors are obtained:

Parameter	
Young's modulus E	0.024
Poisson's ratio ν	
Fracture toughness Γ_i	
Critical opening δ_c	

It can be observed that for this test case, the parameters are quantified very accurately. In addition, it appears that the problem is insensitive to the Poisson's ratio. In fact, this parameter should be omitted from the identification procedure (i.e., fixed at a certain value). Furthermore, only the delamination part of the loading history is taken into account to identify the elastic and CZ parameters. This is beneficial, because the elastic regime may be left out of consideration, making the IDIC routine less expensive. Finally, even when the initial crack tip location is incorrectly assumed (a 33% error of the initial crack tip location is introduced), it appears that the values of the CZ parameters are still accurately identified, with errors well below 1% (not indicated in the table).

This example shows the ability of the IDIC method to robustly and accurately quantify material and interface parameters. Currently, the method is being extended in order to extract the material and interface parameters from actual LED devices.

3.7 Modeling of Sintering of Ag Particles by Means of Phase Fields and Finite Elements

In several chapters of this book, thermal interface and electrical interconnection materials based on Ag nanoparticles are discussed in detail. This section focuses on the modeling of the sintering process of the Ag particles. Even though this topic is not fully related to the chapter title, it has a clear connection to the book content. To model sintering, appropriate choices for the numerical scheme and material parameters are essential. Up to date, the majority of papers in the literature on the modeling of solid-state sintering [109, 110] have essentially focused on the development of numerical schemes and their qualitative analysis and have not directly been applied to a realistic material system to make quantitative predictions. In this section, a numerical model is presented that adequately captures the sintering behavior in a quantitative manner by means of a comparison with small-scale experiments reported in [111].

The process of mass transport in solid-state sintering is complex and depends on many physical mechanisms, including viscous flow, vapor transport, surface diffusion, volume diffusion, grain boundary diffusion, and plastic flow [112]. It also depends on processing conditions such as the applied pressure and temperature-time profile. In this section, only the most dominant mechanisms are considered: surface, volume, and grain boundary diffusion under isothermal conditions at different temperatures without external pressure. Given the fragile nature of microelectronic components, the sinter paste considered is assumed to be processed under atmospheric pressure.

A finite element-based phase field method is used as the numerical scheme for spatial discretization as it offers a large flexibility in capturing the complex nature of sintering. Moreover, finite elements are not restricted to geometries of rectilinear simulation domains. Finite elements have previously been employed [113] to solve well-known phase field equations, i.e., the fourth-order Cahn-Hilliard equation and the second-order Allen-Cahn equation to study spinodal decomposition and grain growth, respectively. The chemical diffusion mobilities used were constant scalars with no directional dependence. In this section, MOOSE [114] is employed to incorporate the sintering module in order to capture the three dominant diffusion mechanisms and grain boundary migration. The chemical diffusion mobilities are taken as functions of the conserved concentration field and the non-conserved order parameter. Tensorial mobility effects are included as a part of the formulation, so that diffusion occurs only along the tangential direction of the particle, thereby producing the correct neck growth between sintered particles.

3.7.1 Phase Field Model

Diffusional mass transport and grain boundary migration between sintered silver particles are described using the phase field method. For this purpose, a conserved field parameter c and a non-conserved order parameter η_{α} are introduced, where α is

the index of a particle. The conserved field *c* describes the concentration of silver, and it takes a value of 1 in the solid phase and 0 in the void phase. The morphological evolution of the particles is described by the non-conserved order parameter η_{α} , which equals 1 at the α -th particle and 0 elsewhere in the system. The microstructural evolution is driven by the minimization of the free energy function

$$F = \int_{\nu} \left\{ f(c, \eta_{\alpha}) + \frac{1}{2} \kappa_c |\nabla c|^2 + \frac{1}{2} \sum_{\alpha=1}^{N} \kappa_{\eta} |\nabla \eta_{\alpha}|^2 \right\} \mathrm{d}\nu$$
(3.34)

where $f(c, \eta_{\alpha})$ is the bulk free energy, κ_c is the gradient energy parameter for the conserved field, κ_{η} is the gradient energy parameter for the non-conserved field, and N is the total number of order parameters. The following form for the bulk free energy contribution is adopted from [109]

$$f(c,\eta_{\alpha}) = \omega c^{2} (1-c)^{2} + \zeta \left[c^{2} + 6(1-c) \sum_{\alpha=1}^{N} \eta_{\alpha}^{2} - 4(2-c) \sum_{\alpha=1}^{N} \eta_{\alpha}^{3} + 3 \left(\sum_{\alpha=1}^{N} \eta_{\alpha}^{2} \right)^{2} \right]$$
(3.35)

where ω and ζ are constants. The gradient energy parameters can be related to the grain boundary energy γ_{gb} and the surface energy γ_{sf} according to [115]

$$\kappa_{\eta} = \frac{3}{4\zeta} \gamma_{gb}^2 \tag{3.36}$$

$$\kappa_c = \frac{18}{7\zeta + \omega} \gamma_{sf}^2 - \kappa_\eta \tag{3.37}$$

To uniquely determine all parameters in the free energy function (3.34), the following relation must be satisfied [115]

$$\frac{6\zeta}{\kappa_{\eta}} = \frac{\omega + \zeta}{\kappa_c} \tag{3.38}$$

The width of the grain boundary can be denoted by

$$l_{gb} = \sqrt{\frac{4\kappa_{\eta}}{3\zeta}} \tag{3.39}$$

The evolution of the conserved field parameter c is described by the Cahn-Hilliard equation

$$\frac{\partial c}{\partial t} = \nabla \cdot \left[\mathbf{M} \cdot \nabla \left(\frac{\partial f}{\partial c} - \kappa_c \nabla^2 c \right) \right]$$
(3.40)

where M is the concentration mobility tensor and is defined as

$$\mathbf{M} = \frac{\mathbf{D}}{2(\zeta + \omega)} \tag{3.41}$$

with **D** the diffusivity tensor which is additively decomposed into the contributions from volume, surface, and grain boundary diffusion [116]:

$$\mathbf{D} = \mathbf{D}^{\nu} + \mathbf{D}^{sf}(c) + \mathbf{D}^{gb}(\eta_{\alpha}, \eta_{\beta})$$
(3.42)

Expressions in terms of diffusion coefficients can be found in [117].

The evolution of the non-conserved order parameter η_{α} is described by the Allen-Cahn equation

$$\frac{\partial \eta_{\alpha}}{\partial t} = -L \left(\frac{\partial f}{\partial \eta_{\alpha}} - \kappa_{\eta} \nabla^2 \eta_{\alpha} \right)$$
(3.43)

with *L* the order parameter scalar mobility, defined as [118]

$$L = \frac{\vartheta_{gb} \gamma_{gb}}{\kappa_{\eta}} \tag{3.44}$$

and ϑ_{gb} is the grain boundary mobility.

3.7.2 Finite Element Formulation

The evolution equations (3.40) and (3.43) are solved by means of the finite element method. To this end, the fourth-order Cahn-Hilliard equation (3.40) is written as two second-order equations upon introducing an additional field variable μ [119] and switching to index notation

$$\frac{\partial c}{\partial t} = \frac{\partial}{\partial x_i} \left(M_{ij} \frac{\partial \mu}{\partial x_j} \right)$$
(3.45)

$$\mu = \frac{\partial f}{\partial c} - \kappa_c \frac{\partial^2 c}{\partial x_i \partial x_i} \tag{3.46}$$

The second-order Allen-Cahn equation can be rewritten in index notation as

$$\frac{\partial \eta_{\alpha}}{\partial t} = -L \left(\frac{\partial f}{\partial \eta_{\alpha}} - \kappa_{\eta} \frac{\partial^2 \eta_{\alpha}}{\partial x_i \partial x_i} \right)$$
(3.47)

As commonly done in finite element theory, the weak form of these nonlinear equations is obtained upon introducing test functions and integrating by parts. The obtained system of nonlinear equations is subsequently solved in a fully coupled implicit manner using the MOOSE framework [114]. The details of this derivation are provided in [120]. All simulations were performed using nine-node quadratic elements and were solved using periodic boundary conditions. To reduce computational costs, an adaptive meshing and an adaptive time stepping scheme were adopted.

3.7.3 Results

The material parameters required to model sintering of silver particles are the surface diffusion coefficient D_{eff}^s ; the volume diffusion coefficient D_{eff}^v ; the grain boundary diffusion coefficient D_{eff}^{gb} ; as required in (3.42); the grain boundary mobility ϑ_{gb} ; the grain boundary energy γ_{gb} ; and the surface energy γ_{sf} . The reported grain boundary mobility data of silver in the literature [121–123] reveals a wide range of values with little consistency. The grain boundary mobility for silver is taken from [124], which has a similar order of magnitude compared to other FCC metals like aluminum and copper, although the grain boundary mobility is highly dependent on the grain boundary structure which can vary for different metals. The diffusion coefficient D_{eff} obeys the Arrhenius equation

$$D_{eff} = D_0 e^{-Q/k_b T} (3.48)$$

where *T* is the temperature, k_b is Boltzmann constant, D_0 is a temperature independent constant, and *Q* is the activation energy. The following values for the material parameters have been adopted: $\vartheta_{gb} = 10^{-16} \text{ m}^4 \text{ J}^{-1} \text{s}^{-1} [124]$, $\gamma_{gb} = 0.79 \text{ Jm}^{-2} [125]$, $\gamma_{sf} = 1.14 \text{ Jm}^{-2} [126]$, $Q^s = 3.84.10^{-19} \text{ J} [127]$, $Q^v = 3.15.10^{-19} \text{ J} [128]$, $D_0^s = 10^2 \text{ m}^2 \text{ s}^{-1} [127]$, and $D_0^v = 0.67.10^{-4} \text{ m}^2 \text{ s}^{-1} [128]$. The grain boundary diffusion coefficient is typically in between the surface and volume diffusion coefficient and is here taken as 0.1 times surface diffusion coefficient [109, 117]. This is valid for temperatures above 150 °C; below 150 °C the surface diffusion coefficient tends to approach the volume diffusion coefficient. The remaining parameters were determined from (3.36), (3.37), and (3.38): $\omega = 4.08.10^9 \text{ J/m}^3$, $\zeta = 3.95.10^8 \text{ J/m}^3$, $\kappa_c = 2.24.10^{-9} \text{ J/m}$, and $\kappa_\eta = 1.19.10^{-9} \text{ J/m}$.

3.7.3.1 Two Identical Particles

First, the sintering process of two identical particles is considered. The diameter is 40 nm, the grain boundary width (3.39) is taken as 2 nm, and the sintering temperature is 400 °C. The evolution of the silver particles during sintering is compared to the experimental work of [111] and is shown in Fig. 3.25 during the first 15 min. The phase field plots represent the evolution of the particles by



Fig. 3.25 The evolution of two equal-sized silver particles of 40 nm in diameter sintered at 400 $^{\circ}$ C for 15 min. The phase field concentration plots are shown in (**a**–**c**), while the experimental images are shown in (**d**–**f**) and are taken from [111]

computing $\sum_{\alpha=1}^{N} \eta_{\alpha}^2$ in every point of the domain, which takes a value of one in the particles and zero in the voids. An adequate agreement can be observed between the behavior predicted by the phase field model and the experimental observations. A difference, however, can be noticed in the dihedral angle ϕ , defined as $\gamma_{sf} = 2\gamma_{gb} \cos(\phi/2)$ [112] subtended between the particles: the experimental results show that the sintered particles produce an acute dihedral angle, whereas the phase field model predicts an obtuse dihedral angle. In [120], it is shown that by changing the γ_{sf}/γ_{gb} -ratio, the dihedral angle indeed changes. Reducing the ratio results in a better approximation of the experimentally observed sintered shapes. Furthermore, the presence of carbon impurities on the surface of the silver particle as reported in [111] is not included in the phase field model, even though this may well affect the diffusion coefficient.

The effect of temperature is illustrated next. The technologically relevant temperature range of interest to sinter silver particles is below 400 °C. Two silver particles of 15 nm size sintered at 400 °C, 300 °C, and 250 °C for 4 min are shown in Fig. 3.26. It can be seen that particles sinter faster at higher temperatures, which is in accordance with the higher diffusion values obeying the Arrhenius equation.

3.7.3.2 Size Effect

In order to demonstrate the effect of the absolute size on particle sintering, sintering of particles with a diameter 40 nm and 15 nm at 400 °C for 4 min is simulated. The sintered particles are shown in Fig. 3.27, from which the difference in sintering



Fig. 3.26 Two 15 nm particles sintered for 4 min at three different temperatures: (a) 400 $^{\circ}$ C, (b) 300 $^{\circ}$ C, and (c) 250 $^{\circ}$ C



Fig. 3.28 Sintering of multiple particles: (a) the initial structure with 50% porosity; (b) the structure as a result of 60 min sintering at 300 $^{\circ}$ C

behavior is evident and thus reveals a size effect. Clearly, this is caused by the higher surface area per unit volume for the smaller particles compared to the larger particles [129], resulting in faster sintering of nanoparticles compared to microparticles.

3.7.3.3 Multiple Particles

Simulation results of multiple particles are provided in Fig. 3.28. The size of the models is 500×500 nm², and the initial structure represents a random realization at 50% porosity. The sintering temperature is 300 °C, while the sintering time is 60 min. The differences in "neck" sizes across the structure can be observed.
The next step is to extend the simulations to realistic, irregularly shaped, particles. Ideally, from the calculated structures, the thermal effective properties could be calculated from which a structure-property relation can be established.

3.8 Discussion

In this chapter, particular attention was given to the multi-scale character of adhesion and the corresponding complexity of meaningful continuum-based modeling and characterization methods. It was argued that the common approach of performing delamination experiments at the macroscopic scale and correspondingly, assigning macroscopic model parameters and thereby lumping all dissipative processes in the vicinity of the delaminating front onto the model parameters thus determined, suffers from several limitations. Most importantly, the predictive capability of these models is limited to cases that are very similar to the testing conditions in terms of loading angle, processing history, and sample geometry. This limitation is essentially caused by the absence of the inherent multi-scale character of interface adhesion in these phenomenological models. Indeed, it is their phenomenological nature that hampers these models to be truly predictive. Hence, the challenge remains to develop a generic method for accurate quantitative determination of interface parameters at small scales in actual micro- and nano-electronic devices, as a crucial step toward quantitative prediction of delamination in these devices. Indeed, in order to characterize the interface properties from these experiments, a detailed multi-scale analysis should be pursued through which all separate dissipation contributions to the workof-separation are uniquely identified and quantified, as formulated in a generic way in (3.2).

In order to derive truly predictive adhesion models, the salient features of the underlying microstructure (or even at smaller scales) as well as the resulting dissipative mechanisms need to be accounted for in an appropriate way. In the case of fibrillating interfaces, the discreteness of the fibrils proved to be essential to provide a mechanistic understanding of the physics involved with interface delamination through fibrillation in metal-elastomer interfaces. In addition, an intrinsic shortcoming of cohesive zone formulations at the macroscopic scale was revealed. Likewise, in the case of quantitative understanding of adhesion improvement through surface patterning, the competition between cohesive and adhesive failure appeared to be the critical dissipative mechanism at the microscale.

These examples illustrate the importance of developing dedicated multi-scale methods in order to arrive at truly predictive interface failure models at macroscopic scales. Buehler [130] states: "in order to understand materials failure, it is not simply possible to average over microscopic features." In addition, "the significance of including atomistic or nanoscale mechanisms is also due to the increasing trend towards miniaturization." It is emphasized that this significance depends on the scales at which the most prominent mechanisms act, as illustrated by the examples provided in this chapter. The identification of meaningful model parameters is a

fundamental challenge of any model, either continuum- or atomistic-based [130]. These two modeling approaches treat the description of materials, and interfaces, in an entirely different manner. Continuum models do not explicitly incorporate the atomistic mechanisms at the relevant scales; instead, these are described by empirical relations that enter the constitutive equations at macroscopic scale. Evidently, the behavior of nanomaterials (e.g., nanowires, CNTs) cannot be captured by only a continuum model. Atomistic models are based on interatomic potentials which often originate from first-principle calculations but also entail limitations in their formulations and resulting accuracy and range of applicability. Clearly, atomistic models cannot be applied to describe the behavior of entire structures at the macroscopic scale and at practical time scales [131]. In fact, both approaches are complementary, and the combined use can provide much insight and understanding.

Incorporating mechanisms across the scales is achieved by multi-scale methods. The purpose, and challenge, of multi-scale methods is to extract predictive macroscopic properties by resolving the relevant geometrical and physical details of the underlying scales [132]. Two main multi-scale methods are suggested in the literature [131, 133]:

- Concurrent methods: the behavior at each distinct scale strongly depends on the behavior at the other scales and is thus simultaneously addressed in the problem domain. In general, different methodologies are applied in different regions of the domain. One of the challenges is to ensure a smooth coupling between the different scales, or regions, to avoid spurious wave reflections at the interface between the separate regions [134].
- Hierarchical, or information-passing, methods: the distinct scales are coupled in a sequential manner. Results from calculations at the smallest scale are used as input for approximate, phenomenological models at the larger scales. The coupling between the scales can be achieved through, e.g., volume averaging of the relevant state variables. The employed modeling methods at the different scales can either be equal (e.g., micromechanics) or distinct [131].

A significant number of alternative multi-scale methods have been introduced, such as quasi-continuum methods [135], and are sometimes referred to as hybrid methods as these incorporate characteristics of both methods mentioned above [132]. As a relevant quasi-continuum example for delamination analysis, the so-called multi-scale cohesive zone method is mentioned [136, 137].

Even though substantial progress in multi-scale modeling of materials and interface behavior has been achieved over the past two decades, truly predicting material and interface behavior in three dimensions in complex micro- and nano-electronic devices remains a tremendous challenge. **Acknowledgments** The authors are grateful to the following colleagues, (former) students, and funding sources:

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Chapter 4 Advances in Delamination Modeling of Metal/Polymer Systems: Atomistic Aspects



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4.1 Introduction

The preceding chapter explains the importance of the capability to truly predict adhesion properties and delamination mechanisms in micro- and nano-electronic devices, with a particular focus on the continuum mechanical aspects relevant for metal/polymer interfaces. This chapter elaborates on the pertinent atomistic aspects for metal/polymer interfaces.

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4.1.1 Atomistic Modeling

Molecular modeling has historically concentrated on chemistry and either the prediction of gas phase chemical properties or bulk physical properties. As a result there was little interest in its use in materials engineering. However, over the last several decades (and particularly over the last decade), molecular modeling has gained reputation investigating material performance issues using simulation methods based upon classical mechanics. By providing path-dependent evolution of molecular interactions in order to predict specific effects of a material in its application, it has been found to be a very reliable and flexible platform from which to study compositional connections to performance. Molecular modeling has been especially useful for electronic materials where interfacial interactions have become increasingly important as feature sizes shrink [1-3]. As argued in the preceding chapter, it is the molecular-scale understanding that forms the basis from which to identify underlying weaknesses within a specific material or material formulation and serves as a companion to traditional engineering models such as finite element methods. The downside of molecular modeling is often the small scale of the model. This means that macroscale representation of specific interactions (or molecular combinations) under investigation are not practically possible because the calculations can scale dramatically with the system size (i.e., the number of atoms involved in the model) and become computationally unwieldy. This also means that to critically understand the nature of the material under investigation, strategies for limiting the model size are needed in order to identify the most important interactions.

Fortunately, there are years of structure-property correlations that can be drawn upon within synthetic and organic chemistry in order to weed out the critical interactions for first consideration. For instance, does the material have hydrogen bonding? Is it highly dipolar or ionic in nature? Is there large aliphatic content? And for polymers: how cross-linked is it, are there crystalline or ordered regions? Each of these questions brings with it decisions on how to build and analyze the model. Interestingly, these are common themes when looking at the molecular structure, so the question of what to model sometimes is a relatively simple one of modeling the strongest interactions against the weakest. Other times the question of what to model takes a step up in complexity which includes architectural effects and effects from multifunctional content. Adding additional variables such as the type of order along the polymer backbone (including random, blocked, and stereochemical content), the architecture of the backbone, and cross-linking can increase the model difficulty but become interesting pieces of the puzzle.

Just as interesting as the architecture, there are also common themes in simulating the structural responses with the molecular-scale perspective, such as cycling issues (thermal and/or mechanical), static or equilibrium comparisons, chemical changes, and of course the combinations. While this may seem straightforward to other modeling disciplines, to the molecular modeler it should not be, as the complexity of the model can depend greatly upon the number of different compositional elements. Grouping and simplifying the model (or models) is a major aspect of molecular modeling. One way in which informed grouping of the chemical component has been shown to be invaluable is for the prediction of bulk properties. This has been the topic of many group-based and descriptor analysis methods, such as Jozef Bicerano's program Synthia [4] (available through Biovia), Codessa (Alan R. Katritzky, Mati Karelson, Ruslan Petrukhin, distributed by Semichem), and Cosmotherm (from Andreas Klamt distributed by Cosmologic).

4.1.2 Molecular Simulation Strategies

There are generally two ways to perform a typical molecular simulation: direct quantum methods or classical force field-based molecular mechanics/dynamics (including Monte Carlo methods). Quantum mechanics is the most time and computer-resource intensive model but often needed to understand the basic chemistry. It is also used when the classical force field method is not suitable for the material or property under investigation because of lack of a good representative force field. Today the most popular quantum method is density functional theory (DFT) which basically makes use of spatially dependent electron densities [5] rather than explicit Hartree-Fock calculations of the wave function or semiempirical calculations which are more approximated methods. DFT has been proven invaluable in determining most likely chemical structures, especially if formulation ingredients are the only initial known variables. DFT has also been used to modify force field-assigned atomic charges and bonding when new structures that are not necessarily known are being investigated. For instance the correct charges for ionic species can be very important to define correctly. In addition, DFT is also instrumental for issues involving electronic transitions (optical and electronic properties) and cases in which electrons are moved (such as reactions) as classical force field methods cannot be used.

Almost all of the simulation methods described will make use of classical force field molecular mechanics (MM) and molecular dynamics (MD), with a focus on developing methods or strategies that can be used for material development. Force fields which describe the bond and non-bond characteristics of the atoms are an important part of classical molecular modeling. Today many different force fields are available depending upon the software package, and new force fields are continually being developed today. In several examples in this chapter, the consistent valence force field (CVFF) [6] was applied, which is one of the older force fields, while in other examples, the polymer consistent force field (PCFF) [7] was used. All force fields will describe both the bond and non-bond character of the atoms and their linkages; see e.g. [8]. Without going into detail, the force field should contain terms which describe bond stretch, angle bend, rotational bond torsion, distortion out of

plane, longer range issues (such as one to three interactions), as well as any crossinteraction between these terms. The non-bond description will involve van der Waals (or Lennard-Jones) and Coulombic interactions. Depending upon the force field and software used, some of the parameterizations may be further edited for customization, or new force fields may be accessed. For the engineer, these force fields merely represent constitutive relationships between the atomic and molecular forces and the atomic positions, or material structure. The difficulty in using molecular modeling then becomes one of level of trust in the force field. There are also trust issues related to the definition of the structure trying to be modeled, but that may be handled by modeling ranges of structures to get an idea of the possible response range. For this reason, it is always best practice to compare the model against experiments to be sure the chosen force field is robust enough. Benchmarks or experimental validation is highly desired to ensure confidence in the modeling results and is especially needed when the results must be used in product development.

Until length-scale bridging methods are fully developed which allow transparency forward and backward from molecular to macroscale (refer to the Discussion section of the preceding chapter), one of the most effective uses of molecular modeling is through the use of relative trends. As a tactic, it is one of the fastest as validation in terms of trends to the experimental result is faster than trying to model all aspects of the explicit material. Also in many cases of commercial materials, the components themselves are not atomistically well defined. Since the molecular model is confined to small length scales, almost all molecular modeling can be considered as a nano-material perspective, and the comparative analysis is a good approach from which connections to macro-material trends may be developed.

In most of the provided examples, the strategy involved is to generate comparative molecular interactions in order to develop directional trends, with the philosophy that every property or performance metric is derived from a series of interfacial interactions that respond through the bond and non-bond forces that manifest in energy and structural changes. This philosophy serves the molecular modeler well, in that by concentrating on compositional interactions, the most important ones that contribute to the mechanical response can be identified early. The interfacial interactions may be defined as self-to-self (cohesive types), or self-to-other (adhesive types), but the general strategy is always the same: that of understanding basic pairwise interactions that serve to explain a macro-phenomenon.

Since the fastest way to obtain the family of interactions is with trend analysis (rather than a search for properties), the molecular modeler has latitude to investigate different perspectives that affect the material response within the compositions and molecular structures and architectures. But the models can also look at environmental conditions like temperature, pressure, or moisture and even the rate of change of these conditions. If different perspectives begin to converge on a similar structure or condition, then there is higher probability a root cause has been identified. An interesting example of this kind of modeling investigation for a defect found during commercial use of an IC dielectric which used a combination of techniques was reported in [9–12], but this is not covered in this chapter. In some cases, exact

properties may be derived directly from the molecular model as is the case of modulus which shows remarkable consistency regardless of scale, demonstrating that its main interaction is at a molecular structural level. However, it is always cautioned that benchmark or validation models to experimental results should be done for both trend analysis and property derivation. In cases where electronic properties are involved (and quantum mechanics is used), the philosophy is generally similar, in that no material is felt to be acting in a vacuum by itself and in some way is modified by its environment, even if that environment is represented by a simple molecular pair or a surface.

Since energies and structures are the only two basic results coming out of a molecular model, the setup and definition of the base model are of primary importance as it will provide the basis for comparison. This base model will vary depending upon the material system and the performance properties that are being developed within the application. And even in cases where the method is not quite in sync with the application, the trends found can be used for initial analysis to understand how the molecules are responding to whatever stress is applied in order to design a better model (or material). In many cases, the major material components are used with modifying agents to simplify the base model. Additional components that increase the model size may be added depending upon the time allotted to solve the issue and computer resources available. Both stoichiometric and nonstoichiometric models can be used although the danger is always whether large enough ranges have been used in order to bound the composition variable space. However, ranges can also be quickly pared down by the experimentalists' experience with similar formulations or materials or from scoping models of specific components.

4.1.3 Scope of the Chapter

Without trying to be inclusive with all of the possible simulation methodologies that can be developed, this chapter tries to show the utility that molecular modeling can bring to the material developer and to the material integrator dealing with electronic packaging issues. The different examples will demonstrate that the appeal of molecular modeling is not necessarily the methods available within a software package, but the versatility that can be accomplished with basic tools to create methods directed at specific material applications. Several sections discuss the prediction of bulk and interface properties by means of atomistic modeling. However, property predictions are just one part of molecular modeling, and for the work described here, we will discuss another less acknowledged area of simulation. The former is distinguished from the latter through the concept that often the time-dependent evolution of properties of interacting material systems is needed, so how these molecular interactions evolve is important in order to make a rational judgment of performance worthiness from the material composition perspective. Molecular modeling provides a means to simulate and judge the relationship between the chemistry (and chemical composition) and the performance of the interacting materials. Such interactions, or interfaces, will often have properties of their own that can be classified using molecular modeling simulation. Examples will be provided which will discuss how current software is being used to scale from the molecular into the nano-/microscale through the use of coarse-grained (CG) or mesoscale models (which coarse-grain parameterizes molecular models to larger particles in order to derive a scale-up in model size) in order to begin to address the small scale weaknesses of molecular modeling. Most of the modeling examples that will be discussed represent the actual materials being developed for electronic packaging.

The chapter starts with a short recap of molecular dynamics (MD) theory, after which the first example covers the prediction of thermomechanical properties of an epoxy molding compound (EMC) and the adhesion properties of an EMC/copper interface by means of MD and CG MD approaches. The second case will review the work done for die attach and via fills, covering the modeling of wetting, adhesion, and reliability cycling. The third case discusses model scaling to discrete element modeling (DEM) for understanding underfill flow. The work done using DEM is not fully molecular modeling per se, but the energy relationships were identified by molecular modeling, and the repercussions of the right energy relationships are discussed. The next example stays within the area of model scaling, reviewing work done in mesoscale (CG) modeling of an epoxy molding compound which relates to the first example. The fifth example covers the molecular modeling of some silicate layers used in planarization and encapsulant layers for flat panel displays. The next example is another mesoscale CG-related one, exploring simple diffusion of organic bases which is of concern to photoresist poisoning. As a cautionary note, any representation of the materials are for illustrative purposes only, as actual compositions cannot be shown. Although all of the molecular models and the coarse-grained models shown were done in 3D, 2D views are shown here for simplicity. The final example reports the prediction of thermomechanical properties of a low-k dielectric material, SiOC:H. The chapter ends with conclusions and acknowledgments.

4.2 Concise Overview of Molecular Dynamics

The focus of this chapter is not to provide an elaborate in-depth overview of molecular dynamics as excellent textbooks on this topic are readily available (e.g., [8, 13-15]). Here, a concise overview is given.

From quantum mechanics point of view, matters have dual natures: particle and wave. However, while the geometry of the system is large enough, the wave nature of individual components becomes unapparent and the system becomes determined. When the wave nature of the particle will be ignored or considered implicitly by the potential functions, MD exhibits high efficiency in the simulation of the molecules. MD, widely used in organic chemistry, is a framework for many particle problems and "describes the time evolution of a set of interacting atoms by integration their

equations of motion" [13]. This method assumes the atom(s) as rigid particles of which the movement is described by coordinate variables. The interactions between the particles are described by the potential functions (or force fields). MD is based on Newton's second law of motion:

$$\mathbf{F}_i = m_i \mathbf{a}_i \tag{4.1}$$

for each particle *i* in a system constituted by *N* particles. In (4.1), m_i is the mass of particle *i*, $\mathbf{a}_i = d^2 \mathbf{r}_i / dt^2$ is its acceleration, in which \mathbf{r}_i is the atomic position, and \mathbf{F}_i is the force acting on the particle. Therefore, MD is a deterministic technique: given an initial set of positions and velocities, the subsequent time evolution can be determined. The interaction force between particles, as required in (4.1), can be defined by potential functions or force fields:

$$\mathbf{F}_{i} = -\frac{\partial}{\partial \mathbf{r}_{i}} U(\mathbf{r}_{1}, \dots, \mathbf{r}_{N})$$
(4.2)

where $U(\mathbf{r})$ is the potential function. Potentials can be categorized broadly as (i) pair potentials, (ii) empirical many-body potentials and (iii) quantum mechanical potentials. Two-body potentials, such as Lennard-Jones, $U(r) = 4\varepsilon[(\sigma/r)^{12} - (\sigma/r)^6]$ (ε is the depth of the potential well, σ is the distance where energy equals zero [16]), and Morse potentials, $U(r) = D\{\exp[-\alpha(r - r_0)] - 1\}^2$ (r_0 is the equilibrium distance, α is the elastic modulus, and D is the cohesion energy [17]), are used for large-scale simulations where computational efficiency is a significant factor. Note that (4.2) indicates that the force in each particle depends on the positions of all particles in the system. A typical two-body potential is illustrated in Fig. 4.1. When the distance of the two-body system is larger than the equilibrium distance (denoted by r_0), the





attractive energy, governed by Coulomb's law, is significant. The attractive energy will fade out when the distance approaches infinity. On the contrary, when the distance of the two-body system decreases, the repulsive energy which is governed by the Pauli exclusion principle will increase. Moreover, the energy approaches infinity if the distance approaches zero.

For systems where multibody interactions are important, the Stillinger-Weber [18], Tersoff [19], and Brenner potentials are often used. Such potentials are empirical in that they are parameterized by fitting either to a set of experimental measurements or to quantum mechanical calculations. However, large local departures from the coordination or bonding used for the parameterization can take such potentials outside their domain of validity and lead to unreliable results. This has fostered efforts for deriving interatomic potentials directly from quantum mechanical principles.

Equation (4.1) represents the system at specific time *t*. To understand the interaction of the particle and the mechanical response, a method regarding the time integration should be used. The most common time integration algorithms are based on finite difference methods. Two popular integration methods for MD are the Verlet and predictor-corrector algorithms [15, 20]. The integration time step must be small enough to capture the dynamics of the vibration modes of the system, with frequencies in the order of 10^{13} s⁻¹. Each particle which is described by MD has three degrees of freedom, which can be either fixed or free. For a system with billions of particles, periodic boundary conditions (PBC) (see, e.g., [13]) can be used to reduce the computational effort.

The initial conditions of the MD simulation include the definition of initial coordinates and velocities of particles in the system. The coordinates can be obtained from stoichiochemistry, measured by experiments or ab initio computational methods. The initial velocity can be defined by the temperature, which is directly related to the kinetic energy by the equipartition formula $K = 1.5Nk_BT$ where N is the number of particles and k_B is Boltzmann's constant. The summation of the kinetic energy of each particle in the system obeys the equipartition formula. Moreover, the centroid velocity equals the given system velocity or zero if the system is at rest.

In principle, MD is based on the theory of classical mechanics while considering the interaction between atoms. MD can be applied when the wave nature can be ignored or represented implicitly. A simple test of the validity of the classical approximation is based on the de Broglie thermal wavelength:

$$\Lambda = \sqrt{\frac{2\pi\hbar^2}{Mk_BT}} \tag{4.3}$$

where *M* is the atomic mass, and *h* is Plank's constant. If $\Lambda \ll a$, where *a* is the nearest neighbor separation, the assumption of the classical approach is satisfied. However, for very light systems, like H₂, He, Li, or a system with sufficiently low temperature, the criterion is not satisfied, and hence, quantum effects will become important.

4.3 Computing Thermomechanical Properties of Cross-Linked Epoxy and Epoxy/Copper Interface

This section deals with the calculation of the thermomechanical properties of an epoxy molding compound formed by curing tri-/tetra-functionalized EPN1180 with bisphenol A, i.e., the "Delft compound" [21]. Conducting MD simulations of polymeric materials is not straightforward as, unlike in crystalline solids, the molecules in polymeric materials are more or less randomly connected, which is particularly true for polymers with cross-linked network structures. Early work mostly concentrated on the network build-up process through Monte Carlo simulations on idealized models, without considering chemical details [22]. More recently, atomistic representations of polymer networks were proposed along with realistic and validated force fields [23, 24]. More advanced methodologies involve dynamic curing of networks starting from a physical mixture of monomers. Yarovsky and Evans [25] applied a cross-linking scheme for epoxy resins. Other authors proposed multistep procedures to create covalent bonds and iteratively equilibrate the structure. For instance, Wu and Xu [26] constructed a model by repeatedly cross-linking and relaxing the system until the desired conversion rate was reached. Similarly, Varshney et al. [27] used a cyclic cross-linking algorithm including multistep topology relaxation to construct an epoxy-based polymer network. Based on the molecular models built by the afore-described approaches, MD simulation techniques were used to simulate the dynamic [28], thermal [23, 27, 28], mechanical [23, 29, 30], and diffusion [24, 25, 31] behavior of epoxies and epoxy-based composites. Alternatively, Kacar et al. [32, 33] developed a mesoscopic approach to predict properties of cross-linked epoxies and epoxy/aluminum interfaces by effectively combining dissipative particle dynamics (DPD) with MD employing the polymer consistent force field (PCFF) [7].

In this section, a cross-linking-relaxation methodology is presented which allows the construction of a highly cross-linked polymer network from a given set of monomers. By using an existing PCFF [7], several thermomechanical properties of the model epoxy are computed such as the coefficient of thermal expansion, glass transition temperature, Young's modulus, and Poisson's ratio. More details can be found in [34].

4.3.1 MD Epoxy Model Generation

The model material studied in this work is an epoxy phenol novolac (EPN). The EPN consists of EPN 1180 as epoxy and bisphenol A (BPA) as hardener [21], shown in Fig. 4.2. Using the stoichiometric mixing ratio of tri-epoxy/tetra-epoxy/BPA = 2:3:9, the theoretical full conversion can be reached, and the average epoxy functionality of 3.6 is maintained.



Fig. 4.2 Molecular structures of (a) epoxy and (b) hardener [21]

To describe the interactions between atoms in the molecular model, the PCFF [7] is applied. This PCFF has been parameterized and validated for various organic and inorganic species and consists of valence terms (bond stretching, angle bending, dihedral and improper interactions, and cross-coupling) and non-bond terms (electrostatic and van der Waals forces):

$$E_{total} = \sum_{b} \sum_{n=2}^{4} k_n (b - b_0)^n + \sum_{\theta} \sum_{n=2}^{4} H_n (\theta - \theta_0)^n + \sum_{\phi} \sum_{n=1}^{3} V_n (1 - \cos n\phi) \\ + \sum_{\chi} K_{\chi} \chi^2 + \sum_{b,b'} F_{bb'} (b - b_0) (b' - b'_0) + \sum_{b,\theta} F_{b\theta} (b - b_0) (\theta - \theta_0) \\ + \sum_{\theta,\theta'} F_{\theta\theta'} (\theta - \theta_0) (\theta' - \theta'_0) + \sum_{b,\phi} (b - b_0) \sum_{n=1}^{3} V_n \cos n\phi \\ + \sum_{\theta,\phi} (\theta - \theta_0) \sum_{n=1}^{3} V_n \cos n\phi + \sum_{b,\theta,\phi} F_{b\theta\phi} (b - b_0) (\theta - \theta_0) \cos \phi \\ + \sum_{i,j} \frac{Q_i Q_j}{r_{ij}} + \sum_{i,j} \varepsilon_{i,j} \left(\frac{A_{ij}}{r_{ij}^9} - \frac{B_{ij}}{r_{ij}^6} \right)$$
(4.4)

The parameters in this model are explained in more detail in [7, 34]. The most challenging aspect of constructing the molecular model is how to accurately describe the cross-linked network of polymers. The actual curing process of thermosetting polymers, which results in the cross-linked network, is complex and involves the formation and breakage of covalent bonds and hydrogen transfers. Depending on the temperature, the curing time required to reach full conversion may range from tens of minutes to hours, which is clearly not feasible for MD simulations. For this reason, a methodology was developed that yields the final cross-linked structure without actually simulating the details of the chemistry of the curing process [34]. In order to achieve a fully relaxed network, the cross-linked system is further equilibrated by MD simulations under the canonical (NVT) ensemble at 600 K for 1 ns, followed by NVT annealing to 300 K at a cooling rate of 10 K/10 ps. Afterward, another MD simulation is performed under the NPT ensemble for 1 ns at 300 K and atmospheric pressure to bring the system to the correct density. An example of the cross-linked structure for the studied epoxy resin is shown in Fig. 4.3, for a conversion rate of 90%.

Fig. 4.3 An example of the molecular configuration after cross-linking to a conversion rate of 90%



4.3.2 MD Epoxy Model Results

First, volume shrinkage caused by cross-linking is calculated. To this end, systems generated along the trajectory of the polymerization simulation, with conversions of 0%, 25%, 50%, 75%, and 90%, were equilibrated at 300 K. The obtained cell volume for each conversion is shown in Fig. 4.4a, including the volumetric shrinkage with respect to the uncross-linked state. For the highest cross-linked system (90% conversion), a volume shrinkage of 4.24% is predicted. It can be observed that volume shrinks consistently with cross-link density [34]. In order to study the temperature dependence of various thermodynamic quantities, a high temperature annealing protocol was followed. The temperature was first increased to 500 K and equilibrated for 500 ps using an NPT ensemble under atmospheric pressure and incrementally decreased to 200 K. At each temperature, the system was equilibrated by an NPT MD simulation at atmospheric pressure for 200 ps. For each temperature, the volume was monitored over the entire duration of the simulation. The thus obtained volume versus temperature curve is depicted in Fig. 4.4b. The discontinuity in the volume versus temperature slope corresponds to the glass transition temperature T_g . To determine T_g from volume versus temperature data, segmental linear regression was conducted and depends on the selected temperature range. Bandyopadhyay et al. [35] derived T_g as a temperature range based on five choices of temperature ranges for data fitting.

The volumetric coefficient of thermal expansion (CTE) α is defined as

$$\alpha = \frac{1}{V_0} \left(\frac{\partial V}{\partial t} \right)_P \tag{4.5}$$

with V_0 the equilibrated volume before the cooling simulation starts. From Fig. 4.4b, the CTE of the cured (90%) epoxy is calculated as 191 ppm/K in the glassy state and



Fig. 4.4 (a) Volume shrinkage as function of conversion and (b) cell volume as function of temperature (the dashed line indicates T_g)

397 ppm/K in the rubbery state, which are in good agreement with experimental values of 210 ppm/K and 570 ppm/K [21].

Calculation of mechanical properties through molecular simulations usually follows one of three methods, namely, static, dynamic, or fluctuation approaches [34]. To extract the elastic properties of the epoxy molding compound, the dynamic method is applied. To this end, a tensile loading is prescribed onto the molecular model which is a much larger model than is needed for structural and thermal analyses, for the sake of reducing noises in the engineering stress data. A model having 240 3-mers, 360 4-mers and 1080 BPAs (corresponding to 82,992 atoms) was constructed and corresponds to a cell length of ~95.50 Å. The computational cell along the loading direction was continuously elongated, while the atmospheric pressure was maintained on the lateral surfaces. Due to Poisson's effect, the simulation cell shrinks in the directions transverse to the tensile axis. The strain rate applied in the MD simulation was 1.10^9 s⁻¹. This rate is typical for MD simulations but is clearly much higher than used in quasi-static tensile tests. Figure 4.5a shows the stress-strain curve of the 90% cured system at room temperature (300 K). Observe that the lateral stress indeed remains approximately zero. The longitudinal stress exhibits a linear elastic regime up to approximately 5% strain. The Young's modulus was extracted by performing linear regression on this part of the raw stressstrain data. The uncertainty is due to the different choices of strain range used for the linear regression. In this work, the strain range used is $[0, \varepsilon_{el}]$ with ε_{el} varying from 2% to 5%, which gives Young's modulus of 2.517 \pm 0.168 GPa, which correlates well with the experimental value of 2.25 GPa [21]. The compressive lateral versus longitudinal strain relationship is plotted in Fig. 4.5b. The Poisson's ratio can then be extracted from the data by linear regression. Following the same approach used for the modulus, we found that the Poisson's ratio is 0.375 \pm 0.0048, falling in the range of 0.30-0.46 for typical glassy state thermosetting polymers. The effect of conversion rate, strain rate, and temperature on the properties is given in [34].

In spite of the extensive use of MD simulations in predicting material properties, these models suffer from severe limitations in length and time scales, which restrict their applications in describing physical processes requiring larger temporal and



Fig. 4.5 (a) Stress-strain response and (b) compressive lateral versus longitudinal strain curve for the 90% cured epoxy model at 300 K, using a strain rate of 1.10^9 s⁻¹

spatial scales to correctly capture, e.g., mechanical responses of polymers. Aside from achieving upscaling in spatial and temporal domains, describing bond rupture for the purpose of modeling material failure and possible cohesive fracture mechanisms in biomaterials is missing in most of the fully atomistic models for polymer networks. In fact, the harmonic or quartic-polynomial bond stretching term present in the consistent valence force fields, such as CVFF [6] or PCFF [7] and (4.4), inherently forbids smooth cutoff of bond energy. Furthermore, valence bond breakage at the atomistic level involves complex re-equilibration of partial charges. Coarse graining (CG) is a method of achieving upscaling by lumping a group of atoms into a "super-atom." As a result, the number of degrees of freedom is reduced, and larger time steps can be taken in the simulation, due to the softer interparticle interactions. This method consists of two steps: (1) partitioning the system into larger structural elements and (2) constructing force fields to describe the inter-bead interactions. The second step is highly material and application dependent thus does not follow a universal rule.

One of several coarse-graining approaches is to match the physical properties of the material by optimizing parameters of presumed mathematical formulations. For instance, the "Martini" force field [36] was parameterized by reproducing the partitioning free energy between polar and apolar phases of a number of chemical compounds. Shinoda et al. [37] developed a coarse-grained potential for surfactant/ water systems by fitting density and surface tension. This approach will be applied here.



Fig. 4.6 CG-based bead-connector representations of monomers: (a) EPN-3mer; (b) EPN-4mer, and (c) BPA

4.3.3 CG Epoxy Model Generation

In the CG model, the monomers are represented by beads connected by chains that preserve similar geometry as their realistic atomistic configurations. Different monomer structures are mapped onto different bead-chain structures as illustrated in Fig. 4.6 [38]. Epoxy monomers (i.e., EPN-3mer and EPN-4mer) and the hardener monomers are mapped into reactive beads. During the MD simulated cross-linking process, bonds are continuously introduced between these two types of beads.

The non-bonded interactions between beads are described by the widely used Lennard-Jones (LJ) potential:

$$U_{LJ}(r) = 4\varepsilon \left[\left(\frac{\sigma}{r} \right)^{12} - \left(\frac{\sigma}{r} \right)^{6} \right]$$
(4.6)

where σ is the finite distance at which the interparticle potential is zero, and *r* is the inter-bead distance (see Fig. 4.1). The truncation distance for U_{LJ} is set to 2.5 σ . The bonded interactions between beads are described by a quartic function of *r* and a repulsive LJ function, with a cutoff at $2^{1/6}\sigma$ [39]:

$$U_{b}(r) = U_{0} + k_{4}(r - r_{c}^{2})(r - b_{1} - r_{c})(r - r_{c})H(r_{c} - r) + 4\varepsilon \left[\left(\frac{\sigma}{r}\right)^{12} - \left(\frac{\sigma}{r}\right)^{6} + \frac{1}{4}\right]H(2^{1/6}\sigma - r)H(r_{c} - r)$$
(4.7)

where H(x) is the Heaviside step function, $k_4 = 1434.3\epsilon/\sigma^4$, $b_1 = -0.7589\sigma$, and $U_0 = 67.2234\epsilon$ [39]. The bond extension cutoff distance r_c is one of the parameters to be fitted. At r_c , the potential is smoothly truncated, and the bond is removed from the system (bond breakage). The LJ pair potential (4.6) is turned on between the afore-bonded pair. The angle bending interaction is described by a quadratic function of the bond angle:

$$U_a^i(\theta) = k_\theta^i \left(\theta - \theta_0^i\right)^2 \tag{4.8}$$

where θ_0^i is the equilibrium bond angle. The index *i* denotes the angle type: type 1 corresponds to the angle formed by the three beads in a BPA monomer, with assumed $\theta_0^1 = 100^\circ$; type 2 corresponds to the angle formed by a reactive bead in an EPN and a BPA, with $\theta_0^2 = 180^\circ$; all remaining angles formed by beads within each EPN are called type 3, with $\theta_0^3 = 180^\circ$. The assumptions on the equilibrium angles

are based on the geometry of the monomer configurations (see Fig. 4.6). All parameters in the inter-bead potentials are quantified by means of the particle swarm optimization procedure which iteratively minimizes the difference between the CG model and atomistic models. Details of the algorithm are provided in [38].

To generate the epoxy model, CG beads representing epoxy and hardener monomers are randomly seeded in a cubic simulation cell with periodic boundary conditions in all three orthogonal directions. The number of different types of monomers obeys the stoichiometric ratio 2:3:9 for 3mer:4mer:BPA. The assembly is equilibrated under NPT ensemble conditions at the temperature of 500 K with a time step of 5 fs for one million steps. Next, a dynamic cross-linking step is performed. Upon reaching the desired conversion degree, the simulation cell is quenched from 500 to 300 K at 2.2×10^{10} K/s, followed by an NPT simulation of one million steps at 300 K to reach the equilibrium density of 1.183 g/cm³. The used simulation cell contains 7,834,220 beads, with size ~85 × 85 × 85 nm³ at RT equilibrium.

4.3.4 CG Epoxy Model Results

The cross-linked epoxy material was equilibrated under NPT ensemble conditions at 610 K. Next, the material was cooled down from 610 to 150 K during four million steps, at a cooling rate of 2.3×10^{10} K/s (time step 5 fs). Figure 4.7a shows the specific volume versus temperature for different conversions. From these results, T_g for the 90% and 0% cross-linked systems is 401 K and 312 K, respectively, which is in good agreement with the values from the MD simulations [34] and Sect. 4.3.2. To verify the validity of the CG model predictions at other conversion rates, Fig. 4.7b shows the CG and MD results in which the error bars correspond to different choices



Fig. 4.7 (a) Specific volume versus temperature relationships for systems with different conversions using the optimized CG potential parameters; (b) glass transition temperature versus conversion relationships obtained from CG and full MD simulations





in temperature range in the bilinear regression. It is seen that the T_g values as function of conversion predicted by the CGMD model are very close to the values from the MD model [34].

The tensile behavior of the epoxy is simulated by subjecting the cross-linked and equilibrated polymer network to a tensile deformation at 300 K. The deformation is accomplished by elongating the simulation cell along the loading axis with a strain rate of 10^8 s^{-1} which is clearly much higher than typical strain rates used in quasistatic loading in laboratory tests. Figure 4.8 shows a stress-strain curve under the uniaxial strain condition. It is seen that at a strain level of ~7%, the material reaches its yield stress of about 300 MPa. After yielding, the stress immediately relaxes down to ~110 MPa [40].

This drastic relaxation is due to cavity nucleation as shown in the first snapshot of Fig. 4.9, where beads are colored by their coordination numbers which is the number of its neighbors within the force field (LJ potential) cutoff distance. The higher the coordination number, the denser the beads are packed. Following this color scheme, the cavities can be visualized in the simulation cell and grow with increasing strain. The stress-strain curve (Fig. 4.8) shows a rather mild strain hardening between 20% and 200% strain. As shown in Fig. 4.9, cavities grow both longitudinally and laterally in this strain regime. The work hardening behavior is a result of the network strands realigning themselves in the loading direction, which yields large strains without significant stress increase. After about 200% strain, most of the network strands are significantly stretched in the loading direction, and the entire simulation cell is changed to a network of ligaments and cavities. Further increasing the strain leads to bond stretching in the ligaments, thereby increasing the stress. Eventually, some of the bonds fail which results in a sequence of bond failure and leads to the final failure of the material by rapid scission of a large number of strands at about 230% strain [40].



Fig. 4.9 Snapshots of the deformation sequence. (Generated by Atomeye [41])



Fig. 4.10 (a) Atomistic and (b) coarse-grained models of the representative molecule attached to the Cu substrate; (c) Free energy surfaces of the CG model computed using different CG Lennard-Jones parameters, compared to the free energy surface of the corresponding full-atomic model (in the shown graphs, $\sigma_{EC} = \sigma$)

4.3.5 CG Epoxy/Copper Model Generation

The epoxy molding compound is described by the potentials given in Sect. 4.3.3. The copper substrate is modeled by using the virtual FCC crystalline structure, with an appropriate lattice constant. In [42], the nearest-neighbor distance between the FCC substrate beads is chosen to be 1.204σ and corresponds to a lattice constant of $1.204\sqrt{2}\sigma = 7.463$ Å. In addition, to describe the interactions between the Cu beads and to maintain the crystalline structure of the substrate during the MD simulations, each Cu bead is linked to its nearest neighbors on the FCC lattice site using a spring with a spring constant of $1000\varepsilon/\sigma^2 = 79.04$ kcal⁻¹ mol·Å⁻² [43].

The CG model for the epoxy/Cu interface is based on an LJ 12-6 potential with parameters ε_{EC} and σ_{EC} (see, e.g., Eq. (4.6)). These parameters need to be determined from the results of a full atomistic model (Fig. 4.10a, b). Next, the free energy surface of the CG epoxy molecule and Cu substrate system is calculated and depends

on ε_{EC} and σ_{EC} . The values are now quantified such that the free energy surface of the CG model matches that of the full atomistic model. Figure 4.10c depicts the free energy surfaces using the CG bimaterial model with different Lennard-Jones potential parameters. Calculations show that the free energy surface becomes very close to that obtained from the full atomistic model when $\varepsilon_{EC} = 3\varepsilon$ and $\sigma_{EC} = \sigma$, where ε and σ are the Lennard-Jones parameters for the CG epoxy (Sect. 4.3.3 and [40]). More details can be found in [43].

4.3.6 CG Epoxy/Copper Model Results

The CG epoxy/copper model consists of a rectangular block for the epoxy on a Cu substrate containing four (111) atomic planes. Periodic boundary conditions are used on all the lateral surfaces. The model has a total of 7,964,588 beads, corresponding to a physical volume of $\sim 89 \times 89 \times 79$ nm³ (at 300 K). The tensile deformation of the bimaterial is simulated by prescribing a vertical rigid-body velocity to the Cu substrate while fixing the very top layer (~ 1 nm thick) of the epoxy. The prescribed downward velocity corresponds to a strain rate of 10^8 s⁻¹ in the epoxy block. The temperature is kept constant at 300 K using the Langevin thermostat, which appeared to be critical in maintaining the system at a constant and uniform temperature [43].

The structure of the epoxy near the substrate surface is of great interest for understanding adhesion properties. Figure 4.11a shows a zoomed-in view of the near-interface structure of the epoxy after full equilibration at room temperature. It



Fig. 4.11 (a) Zoomed-in view of the interfacial zone. Gray and red beads are the EPN and BPA beads, respectively. Yellow beads are the Cu beads (for better visualization, the epoxy and BPA beads are not drawn to scale); (b) Stress-strain curve for the tensile simulation of the epoxy/Cu bimaterial



Fig. 4.12 Snapshots of the deformation process for the 90% cross-linked epoxy/Cu bimaterial under tension

can be observed that the epoxy beads tend to be densely packed into a few distinctive bands. The further away from the interface, the less distinctive the band structure becomes. Such structural feature is due to the rather planar, simplified, geometry of the substrate surface, and the Lennard-Jones interactions between epoxy and substrate beads. Ab initio calculations [44] showed that the benzene rings have a strong adsorption to metal surfaces and prefer to align along the Cu surface. In earlier full atomistic studies of the same epoxy/Cu bimaterial [45], densely packed benzene rings were also observed near the interface. These results confirm that our coarse-grained model for the epoxy/Cu bimaterial correctly capture the structural characteristics of the epoxy/Cu interface.

The obtained stress-strain curve for the strain rate of 10^8 s^{-1} is shown in Fig. 4.11b. The curve shows an elastic response until the stress reaches the interface strength of ~260 MPa at a strain of ~5.4%. Subsequently, the bimaterial experiences a drastic stress reduction down to ~125 MPa (similar to Fig. 4.8). At about 25% strain, final interfacial failure occurs.

Figure 4.12 depicts several snapshots of the deformed configuration at a strain rate of 10^8 s^{-1} . It is seen that at 15% strain, cavities start to nucleate in the epoxy near the interface as a consequence of the relatively weaker force field between the epoxy and the Cu substrate [43]. After reaching the tensile strength and subsequent stress decrease, a weak strain hardening takes place that extends to about 25% strain which is accompanied by cavity growth as well as increased stretching of the polymer strands. Upon reaching the ultimate failure strain of 25%, the epoxy within the interfacial zone is fully stretched. The strong covalent bonds between the polymer beads prevent further deformation in the epoxy. As a result, the polymer strands are pulled off from the Cu substrate as shown in the snapshot at 30% strain in Fig. 4.12. Eventually, this leads to a rather clean interfacial separation between the epoxy and the substrate as shown in the snapshot at 40% in Fig. 4.12.

To study the deformation of the epoxy near the interface region in more detail, the normal displacement as function of the distance from the substrate is plotted in Fig. 4.13a for three different (macroscopic) strain levels. First, the displacement profile prior to yielding (5% strain) is nearly linear, which means that the strain (i.e., the slope of the displacement profile) is nearly constant within the epoxy. Second,



Fig. 4.13 (a) Displacement profiles along the normal direction for the 90% cross-linked epoxy/Cu bimaterial at three macroscopic strain levels; (b) The extracted traction-separation relationship based on the definition of the interfacial zone

after yielding, the deformation in the epoxy is highly localized to a thin zone of approximately 10 nm near the interface. The average strain inside the interfacial zone is approximately 115% at 15% macroscopic strain and approximately 185% at 25% macroscopic strain. Outside this localization zone, the strain in the epoxy remains at about 2% at both 15% and 25% strain levels. In fact, although not shown, once localization occurs, the bulk strain outside the interfacial zone remains at ~2%, irrespective of the overall strain level. It is remarked that previous full atomistic studies [45] on the same epoxy/Cu bimaterial did not reveal such highly localized deformation. This can be explained by the fact that the material volume used in the full atomistic simulations is smaller than the size of the interfacial zone and therefore unable to capture the localized deformation. This illustrates the necessity of accessing the correct length scale to fully understand the mechanical behavior of polymeric materials and interfaces.

Interestingly, Fig. 4.13a also indicates that the deformed bulk volume during separation increases with increasing strain. This apparent increase of the interfacial zone thickness is entirely due to the increased deformation inside the interfacial zone. The total mass of the interfacial zone remains unchanged. This discovery confirms the applicability of a cohesive zone model in the macroscopic scale where the epoxy/Cu bimaterial is treated as a continuum. It is remarked that this conclusion is not general as the preceding chapter showed that for elastomer/Cu systems, the application of continuum-based cohesive zone models is less straightforward due to the discreteness of the underlying microstructure. For the epoxy/Cu system, the elongation of the interfacial zone thickness can be defined as the separation between the Cu surface and the bulk epoxy at the continuum scale. The relationship between this interfacial separation and the applied tensile stress can be easily obtained by keeping track of the displacement profile at each load increment. As the applied tensile stress versus separation

relationship gives the desired traction-separation law to be applied in the cohesive zone model at the macroscopic scale (Fig. 4.13b). It can be observed that the thus obtained traction-separation curve shows the general features of traction-separation laws for polymer/metal interfaces. The traction first increases almost linearly with increasing separation. Once reaching its strength, the traction drops drastically, followed by a weak strain hardening until reaching the cohesive strength and critical separation. It is remarked that the cohesive zone model is one of the most commonly used constitutive laws to describe the deformation and failure of materials interfaces (as illustrated in the preceding chapter). However, in most applications, the traction versus separation relationship is assumed ad hoc and calibrated via indirect experimental observations. In contrast, Fig. 4.13b shows a macroscopic traction-separation curve for polymer/metal interfaces which is readily obtained from CGMD simulations at the atomic scale [43]. This perfectly illustrates that, in order to improve the predictive capabilities of material and interface models, tailored multi-scale methods are essential [8, 46, 47].

4.4 Wetting, Adhesion, and Molecular Stress Cycling (Molecular Coffin-Manson) for Reliability

In this section, two basic examples will be shown to examine the effects of formulation components on performance. The first example concerns bleed, which is defined as excessive and unwanted wet-out or surface diffusion [48, 49] into areas that interfere with further material integration of the device structure. The second example covers adhesion [50–52], which includes the importance of molecular stress cycling as a molecular analog of the Coffin-Manson response.

4.4.1 Wetting

Wetting is the first property of interest when understanding the attraction of the material to its substrate and the final adhesion. Experimentally, contact angle is used to describe wettability, but when a reactive formulation is in question, the contact angle result may be misleading because it will represent the uncured formulation components along with any solvent, diluents, modifiers, or other volatile ingredient used. The same can be said of a polymer in solution. The solvents may help the polymer penetrate better onto the substrate but may misrepresent native wetting quality of the polymer. By contrast, wetting analysis within a molecular model will show whether contact is being made with the substrate of interest as well as the impact of the composition. Since the model compositions can be changed at will, comparisons can be done on the impact of unreacted versus reacted components, as well as the impact of solvents and diluents. Subsequent adhesion analysis is then required to understand the abilities of the cured material to adhere to the substrate.

The first example is wet-out of a solvent-free reactive formulation. In this case the formulation is a die attach, which is a highly silver flake-filled solventless resin system. The die attach under investigation was found to wet-out onto neighboring bondpads in a phenomenon called "bleed." The phenomenon is simply surface diffusion which is controlled by the surface energies of participants. However, the issue becomes more complicated when the product is expected to perform regardless of the conditions and surfaces, and those conditions are not set by the developer of the die attach. The bleed molecular models were quite simple geared toward the actual tests themselves which measured the spread of a drop of the formulation after a set period of time. A stoichiometric representation of the organic binder portion of the formulation was energy minimized with a block of silver atoms (representing the silver flake filler) in order to represent the formulation. This mass was then introduced to the substrate, and the entire structure was allowed to equilibrate at RT for a set period. For comparison purposes the period of equilibration was kept constant for all cases. The results from the model indicated that it was less important to find the energy equilibration point but more important to keep the timing constant which is more in-line with both bleed and contact angle experiments. Both the substrate and the filler block were fixed to keep the periodic nature of these materials intact.

As may be imagined, because these are molecular models, a realistic filler size could not be represented, but the filler is still represented in the model, as wetting to the filler itself could further modify wetting to the substrate. Because these models targeted trend analysis, a parallel placement of the filler and substrate surface was used in all cases, rather than adding in the compounding influence of geometrical effects between the filler and surface. For die-attach applications, this was a valid assumption as cross sections of die-attached regions of a package showed parallel organization of the silver flake in relationship to the surface. The binder wet-out is thus simulated by a combination of both the filler and substrate interaction with the binder. Typically a silver filler was used to mirror the formulation work, but any filler could be used. The substrate material was varied according to the surfaces this die attach may see (silicon, copper, silver, gold, copper oxide, and chromium oxide). Like experimental bleed tests, wet-out using the molecular model was measured as the distance migrated on the surface from the starting mass. An example of the model before and after equilibration is shown in Fig. 4.14. In each picture, the top gray



Fig. 4.14 Example of wet-out of die-attach components before and after RT equilibration. Left, before equilibration; right, after equilibration. The substrate is nickel oxide (red oxygen, blue nickel). The filler is silver (gray silver). For the organic binder, dark blue nitrogen; red oxygen; gray carbon; white hydrogen

block is silver, the bottom layer is nickel oxide, and the binder formulation components are in-between.

The models were repeated with different compositions to give an idea of the compositional effect. Some of the initial results that were compared against experiment are found in Fig. 4.15a, which showed that qualitatively we should be able to tell the difference between a high bleed and a low bleed formulation. While this may be uninteresting to those not involved in bleed or surface diffusion issues, the importance of the model was found when it was discovered that the energy drop found in the model over the trajectory was related to the surface energy of the formulation. A calibration curve back to surface energies was then developed from the extrapolated (surface-free) energy changes in the models (Fig. 4.15b).

The energy drop was then used as a relative gauge of the surface energy of the formulation, and quite quickly trends of the formulation surface energies could be constructed against different formulations and fillers. Figure 4.16a shows that the amount of wetting will drop with an increase in the surface energy of the formulation. The general wetting trend is in keeping with the expectations of wetting theory which says that wetting will not occur if the surface energy is less than the combined interfacial and liquid surface energies [53]:

$$\gamma_s \le \gamma_{sl} + \gamma_l \tag{4.9}$$

This general relationship suggested that to decrease bleed, a decrease of the surface energy of the substrate or an increase of the surface and interfacial surface energies of the formulation is needed. This relationship was of prime importance to the dieattach formulation developers, as it was quickly acknowledged that of the three surface energy variables, the formulators could only really control the "liquid" effects, i.e., the formulation, including both the binder and the filler (this is primarily because the formulation supplier has no practical design control over the substrates or the other surfaces that the material would see). However the general effect of the formulation is found in Fig. 4.16b which shows that, as the surface energy of the substrate increases, there is an increase in bleed.

4.4.2 Adhesion

Adhesion is another important property for die attach, underfills, via fills, and molding compounds that were under development. Molecular modeling was engaged to understand and improve adhesion, and the simulation technique was a simple one of minimizing a strand of the representative polymer (resin+curatives and any modifying agent), minimizing it to a surface and forcing it from the surface, as represented by the schematic in Fig. 4.17. The distance forcing method employed a simple forcing potential that removed the polymer from the surface by shearing it from the surface. This is a non-equilibrium molecular dynamics method (NEMD), and it was thought to be more representative of the molecular responses to stress



Fig. 4.15 (a) Actual bleed trends: model vs. experiment; (b) Surface energy calibration curve developed from models of known materials



Fig. 4.16 (a) Wetting vs. formulation surface energy showing general drop in bleed with formulation surface energy; (b) The effect of water on bleed using two different formulations (A is water sensitive and B is not)



Fig. 4.17 Schematic of the adhesion model which uses a forcing potential to the end of the binder polymer chain

during use, which can be adjusted depending upon the time scale or evolution under study.

Typically the forcing potential was applied at the end of the polymer chain, or if it was more folded or branched to the end of the long axis, in the direction of the chain axis in order to determine the highest energy resistance to the removal. For cohesion, a dual strand of the polymer was minimized together (the second strand used as the "substrate") and a forcing potential applied at opposite ends through the center axis, or as close to the center axis as possible, in order to shear the strands apart lengthwise. For all comparisons, the total simulation time was kept constant. It

was rationalized that for polymers, this technique could then follow the timedependent evolution of the strain with an energy response as a combination of non-bond interfacial forces as well as the bond-bond, bond-angle, and torsion effects that would follow the strain imposed depending upon their interactions and the responses from the parameterizations.

It is worthwhile to point out that because the goal was to develop relative trends than absolute values, the tactic engaged was to find the maximum resistance to separation that the interactions might offer by aligning and stressing in the direction which allowed the highest contact. This was done to maximize the comparison analysis and to help eliminate, or at least reduce, the uncertainty when issues of cure and conditioning are entered into an already complicated variable space. Trial and error showed that lower resistance energies were derived using other forcing directions, suggesting that the adhesion or cohesion of polymers has a maximum interaction footprint that is different depending upon the resin and curative combination. All adhesion comparisons were usually done at multiple rates by increasing the target distance to be accomplished within a set simulation time. The need for understanding rate dependencies was initially rationalized based upon the fact that on a molecular level, there is no guarantee that all atoms are moving at the same rate. It was then found that generally when the maximum energy barrier was plotted against the average model rate, the barrier would increase with rate up to a point when the energy trend would break. The break point was used as the point of maximum possible resistance of the modeled pair interaction (the energy and rate dependency range was found to be important to know, as the low end rate extrapolation could be used for parameterizing coarse-grained diffusion models; see Sect. 4.8).

An example adhesive energy curve is shown in Fig. 4.18a showing that in most cases the molecular trajectory will go through an energy maximum that can be used to estimate relative adhesion strength performance. In addition, the initial slope of the energy-displacement curves could be used to extract the elastic modulus (as with the maximum energy, the modulus was also found to be rate dependent, and a similar energy break was used to determine the highest possible modulus). By running the



Fig. 4.18 (a) Adhesion energy trajectory example; (b) Adhesion comparisons of resin candidates plotted against the relative surface energy of the possible substrates the formulation may touch (each group shown is in order of lowest to highest substrate surface energy; the first bar in each group is the cohesive energy



Fig. 4.19 (a) Simulated vs. (b) experimental adhesion effects of moisture ("Exp" denotes an experimental formulation target under investigation)

simulations on different substrates (which usually ranged from silica to nickel oxide), comparisons of resin candidates could be run for down-selection of the best candidate depending upon the surfaces it might see. Figure 4.18b shows an example of such comparison in which the resin adhesion is plotted against different substrates using their surface energies, showing how different resins might respond with different substrates. This is only one example of model usefulness as the comparison can be used for initial evaluation of resins when faced with different substrate requirements.

Another example of general concern was determining the resistance to moisture of the adhesive formulation. This was, and continues to be, a main issue for long-term environmental stability. The flexibility of the molecular model is demonstrated by being able to easily simulate candidates without water then with water as a modifying agent. Figure 4.19 shows the model results of resins compared for water-resistant adhesives, along with the experimental validation. As can be seen from the comparison, the model adequately predicts that one of our experimental polymers should perform with superior adhesion retention once moisture is introduced, which was verified when testing was done. The laboratory test experiments were run as-cured and after moisture (85 °C/85RH) preconditioning. One of the resins (A1) is severely impacted by water, demonstrating that for that resin there is a significant plasticizing effect with water.

The models were taken further by examining whether molecular modeling could reproduce stress-cycling reliability trends. In these cases, the impact under investigation was determining if molecular cycling could adequately predict long-term performance, as is predicted by Coffin-Manson. As is well-known, the Coffin-Manson equation relates the number of cycles to the strain through an exponential relationship: $\varepsilon = MN^z$, where ε is strain and N is the number of cycles [54]. A log-log plot then gives a linear relationship where reliability can be judged based upon the expected strains experienced. For molecular stress cycling, after the polymer had been stressed, the forcing potential was removed and the whole model was allowed



Fig. 4.20 Molecular stress-cycling schematic



Fig. 4.21 Schematic of molecular stress-cycling test result showing Coffin-Manson type relationship

to relax as shown in the schematic of Fig. 4.20. This process was repeated until the polymer segments were totally displaced, or no resistance to stress was found in the forcing potential phase.

The molecular cycling was then repeated with different strains until the Coffin-Manson relationship could be built. A simple test case revealed that like experimental reliability tests, the cycles to failure follow a typical exponential relationship (Fig. 4.21) which could be further reduced to a linear relationship by plotting the log of the strain against the log of the cycles.

As moisture reliability has been an important topic to all adhesives (including die attaches, underfills, via fills, and molding compounds), stress cycling was simulated with and without water for new adhesive binders. In addition, both adhesion and cohesion were examined, in order to determine whether cohesive or adhesive failure was more likely. The study involved evaluation of different resins and hydrophobic flexibilizers that may enhance moisture resistance and both the components and formulations were evaluated using the molecular stress cycling. In the interest of time, limited cycling was simulated, and the results extrapolated once a reasonable curve could be generated. The candidates were then plotted against one another by extracting the highest strain sustained at 1000 cycles for relative performance comparison as shown in Fig. 4.22. Modeling comparisons were done on both resins and test formulations, and provided data for our down selection. For instance resin C looked promising to maximize adhesion. However, the modified Formulation A showed both an optimum adhesive and cohesive cycling response.



Fig. 4.22 Resin and formulation selection process based upon the maximum strain that might be sustained at 1000 cycles from molecular stress-cycling simulation



Fig. 4.23 Effects of moisture for maximum adhesion (left) and maximum strain sustained at 1000 cycles (right)

Formulation work looking for reliability robustness was then aided by modeling the formulated interfaces with and without water. Both adhesion and stress-cycling models were applied in order to get the best idea of possible performance. In parallel, experimental adhesion tests were done both before and after conditioning. The modeled adhesion (Fig. 4.23, left) suggested an adhesion order of A>B>C which was exactly the order of the experimental results. However, after using the molecular stress cycling, Formulation B was found to be the better candidate (Fig. 4.23, right). Experimental adhesion tests after humidity conditioning and cycling showed A~B>C, and after thermal cycling followed by thermal shock B>A>C; B was clearly expected to be more robust, in agreement with the molecular cycling model. So for modeling, using cycling clearly did a better job at predicting which material would be more reliable than the single cycle adhesion model. The need for running cycling tests rather than relying on adhesion tests was also found to be generally true experimentally.

The most convincing test for the validity of molecular stress cycling was found when the modeling was used to evaluate resin and cured structures for a via-fill paste application for boards and packages. In this case, the molecular stress-cycling


Fig. 4.24 Molecular stress cycling of possible resins (left) and cured components of the base resin (right)



Fig. 4.25 Cross sections of vias after thermal cycling (condition B: -55 to 125 °C, liquid/liquid immersion, 10 min cycles)

modeling additionally looked at the possible reliability of both the base resin and various cure structures that might form in order to bias the chemistry of the formulation toward the most robust direction (Fig. 4.24).

When vias were actually filled and tested, the new material survived a higher number of cycles under condition B (-55 to 125 °C, 10 min cycle) than the competitors at the time. Cross sectioning showed the damage in commercial via fills whereas the new via fill paste showed no damage (Fig. 4.25). This is a good example where the molecular modeling was allowed to participate in the material development process all the way from research concept to commercialization. The combination of simulation and experimental test validation demonstrated that this type of feedback cycle could speed the development and the moisture-resistant die-attach adhesives and via fills were all commercialized (Fig. 4.25).

4.5 Underfills and First Forays into Scale-Bridging from Molecular Insights

Another interesting application involving both molecular modeling and discrete element modeling (DEM) was looking at variables to improve the filler distribution after the underfill process is complete. Figure 4.26 shows an acoustic image of a bumped die after underfilling showing unwanted streaking signifying uneven particle distribution. The underfill process and material under investigation at the time required capillary flow underneath the bumped die. Today the underfilling process is replaced by other techniques, but this modeling example is included to demonstrate model scaling.

Flow speed, filler settling, filler striation, and voiding are all properties that require a mechanistic understanding in order to improve the materials, which are all at higher length scales than is available from molecular modeling. However, because of the heavy dependence upon surface energy properties for the capillary fill process involved in underfilling to occur, some of the fundamental energies should also have a molecular origin. Although both binder and filler effects on flow are expected from a combination of surface energy and particle dynamics drivers, at the time both could not be implemented into a single molecular model, and a multi-scale strategy was in order. To accomplish this, both molecular modeling and DEM were applied.

For the scaling work engaging DEM, the services of the Particulate Science and Technology Group (under Dr. Masami Nakagawa) at Colorado School of Mines (CSM) apply DEM to understand the effect of the filler particle dynamics within the formulation on the final filler distribution under the die. Like molecular modeling, DEM uses discrete particles and the interactions existing between the particles governed by classic Newtonian physics. However, DEM can also take into account much larger scales than molecular modeling, which can deal with particle shape and distribution, and is an ideal transition example between molecular modeling and continuum methods in order to study a filled composite system. For this study, particle distribution as well as lubrication, drag, and adhesion forces has been taken

Fig. 4.26 Example acoustic image of filler taken of a silicon die after underfilling (flow direction is bottom to top)



into account and has been discussed in previous articles [55–57], so only the key results will be covered here.

It is known that the spatial distribution and dynamics of particles within a suspension is governed primarily by the forces that act among them as discussed by Bossis and Brady [58]. Most importantly to the impact of molecular modeling was the realization that the particle interactions will for the most part be controlled by the resins of the formulation. These interactions could be derived directly from molecular models. After reviewing the molecular surface energy trends previously calculated using molecular modeling, it was agreed that perhaps a molecularly derived adhesion/repulsion could be derived directly from a molecular model to help represent the dynamics of the filler particles. So the molecular modeling used a modified "bleed" experiment, in which the resin was placed between the filler particle and the substrate, but in this case both surfaces were silica surfaces (to represent the silica filler, but could also represent the oxygen-terminated silicon surface of the die), and the energy drop was monitored while the silica surfaces were stepped closer and closer to one another. In this manner energy/distance curves could be constructed for each binder type, which are shown in Fig. 4.27 for a high and low surface energy binder. These energy curves were the basis of the parameterization of the filler particles for DEM. For the DEM simulation, the major missing parameters were adequate definition of the adhesion, and the energy curves allowed initial estimations of this parameter and adjustment to the governing energy expressions. In this manner, there was no need to explicitly model the binder in DEM, as the binder effect was implicit in the energy relationships. Most importantly, the energy curves gave us a handle back to the composition of the binder.

Two two-dimensional particle flow cases were simulated by DEM. In one case, the effect of speed and particle distribution was studied in order to determine how to control filler settling. The second case explored the reason for uneven distribution found in the acoustic image, in which the filler must flow around an array of solder bumps. The results of the first case involving filler settling are shown in Fig. 4.28. For this case, filler particles with specific particle size distributions were allowed to flow between the top and bottom surfaces. The fluid effects were changed by adjusting the velocity of flow. It was found that the larger particles immediately fell to the bottom, but more mixing of the smaller particles could be found if the flow



Fig. 4.27 Energy profile of solid-solid interaction modified by intervening binder. Left: high surface energy binder, high adhesive forces. Right: low surface energy binder, low adhesive forces



Fig. 4.28 Effect of flow speed on filler settling and mixing. Top: starting filler distribution before flow. Bottom right: result with flow at higher speed. Bottom left: results with flow at lower speed



Fig. 4.29 DEM flow around bumps showing the impact of adhesive forces, flow direction is bottom to top; (a) left, no adhesive forces used; (a) right, moderate adhesion added; (b) no adhesive forces used in a full bump array. The solder bumps are represented by the large circles, and the filler particles are represented by the small circles

speed was reduced. It is the velocity effects that were of interest, as speed would be controlled by the surface energies of the compositions.

The most significant link to the molecular models was found in the second DEM case looking for filler distribution effects. The left picture of Fig. 4.29a shows the case of filler flow if the particles do not contain the adhesive forces in the energy expressions, as does Fig. 4.29b but this time for a full bump array. This simulation did not exhibit the ragged flow found-front found in reality but also did not exhibit any filler filling behind the solder bumps. The right-side picture of Fig. 4.29a shows the end frame of a DEM simulation where adhesive forces have been added, showing filling starting to occur behind/between the solder bumps, but filling is incomplete. Figure 4.30 also shows a bump array simulation with high adhesion forces used. The simulation stopped before very many particles had been injected, due to the agglomeration of filler particles. Also, rather than a straight-line trajectory as found in Fig. 4.29b, more complete filling is occurring behind the solder bumps, as well as an expected

Fig. 4.30 DEM simulation after unusually high adhesion forces have been added



ragged flow front due to the agglomeration of the filler. The ragged flow front was found from the case that used energies representing high adhesive forces in the DEM.

These simple DEM simulations showed us that to control the flow front and the backfilling behind bumps, the binder had a significant effect on fill distribution mostly due to high adhesive forces.

In follow-on formulations, the high adhesive forces between the silica filler particles were weakened by surface treatment of the filler lowering the surface energies. These formulations showed significantly lower streaking, demonstrating the predictive quality of the scaled DEM models (in another DEM investigation targeting conductive adhesives, an electrical resistive chain model was built based upon contact points after filler compaction. Although the study is not included here, as it does not include molecularly derived forces, this study further demonstrated the role of optimizing filler shape as well as particle distribution based upon particle models [57]).

4.6 Scaling the Adhesive Interface Using Coarse-Grained Molecular Models

In this section the scaling from the molecular level to a coarse-grained mesoscale level by direct parameterization of the coarse-grained particles is discussed. This section presents a summary of the findings reported in more detail in [1, 59, 60] and was initiated by a consortium of the EU-funded project NanoInterface (NMP-2008-214371). Here, the main interface targeted for the coarse-grained mesoscale modeling was the copper oxide-binder interface.

Coarse-grained mesoscale models, like DEM and classical molecular dynamics, are particle models which apply the basic Newtonian rules of interaction and movement. The general concept behind coarse graining is to combine groups of atoms into new larger particles or "beads." Like DEM and molecular modeling, the energy relationships between the particles/beads must be constructed and parameters defined to govern how the particles interact. Typical coarse-grained force fields include the Martini force field [61] which typically uses functional groups as the particles/beads. The beauty of coarse graining is reducing calculation complexity by reducing the number of particle centers that need to be calculated. This simplification lets the modeler accomplish simulations of larger systems faster than using the explicit molecular model representing the same structures. The work in this section

made use of the software Mesocite (Biovia) and the embedded Martini force field. Typically coarse-grained force fields like the Martini force field employ parameterization of simple small functional groups. However in this work a bigger jump in scaling was applied by using the entire repeat unit, in order to test whether scaling could be further jumped by use of a larger bead and to further demonstrate the usefulness of coarse-grained molecular models in the multi-scale hierarchy. It must be cautioned however, that the molecular shape of the potential target bead must be considered as currently all mesoscale "beads" are spherically shaped. For our purposes, the three-dimensional nature of the repeat unit was considered appropriate for scaling to a larger bead and still maintains the correct structural relationships. However, if the structure is more linear, smaller beads might be appropriate. In the future, if the mesoscale software progresses sufficiently, bead shapes can be included so that the functionality of the mesoscale level can be improved in a similar fashion as DEM tools [57] that have shown that particle shape and the interactions between the shapes can be included.

Pictures of the repeat unit are found accompanying the energy diagrams in Fig. 4.31. From these pictures it is easy to see that, in order to represent the repeat unit, at least ten functional group beads are swapped for one repeat unit bead. This simplification enabled models to be built representing formula weights up into the millions, rather than the thousands which is typical for models simulated on a desktop computer. The polymer used in this study was one developed by Delft University, based upon a Novolac epoxy as part of the NanoInterface consortium [21].

The parameterizations for the epoxy have been well-described [1, 59, 60], but it is worthwhile to reiterate the parameters required. As mentioned previously, the general Martini force field was modified which required definition of both bond and non-bond energies. It was found that the most important interactions that needed



Fig. 4.31 (a) Example trajectory for parameterizing the cohesive case; (b) Example of adhesive molecular modeling used to determine some of the coarse-grained particle parameters, representing an epoxy on a copper oxide substrate (the view is top down onto the copper oxide surface)

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to be defined to accommodate the large repeat unit were the bead-bead non-bond energy, the bead bond length (the repeat unit length was usually averaged from a larger molecular model of a polymer), the van der Waals (VdW) distance (usually derived from the molecular models when the non-bond energies are derived), and the bead bond force constant (derived from a molecular model in which a repeat unit stretched). In addition it was concluded that a last parameter was needed for realistic simulation of the stress-strain curve (to failure), which was not part of the Martini force field: a bead-bead bond length scission criterion. This criterion was found by stress-dynamic molecular models that stretched the repeat unit until bond distortion occurred so the atomistic bonds were ready to break, which was usually past the maximum in the energy to strain curves derived from the dynamics. The stress dynamics (using forcing potentials) were repeated at different speeds, and the maximum bead length determined at bond distortion (end-end distance) was plotted against the energy. It was found that the maximum bead length converged at a consistent length. This length was taken as the maximum that the bead will extend before scission occurs. The maximum bead bond length criterion was applied at every step in the mesoscale model, and bonds were deleted as soon as the criterion was met. It was found early on, while working on the simulations of adhesion and cohesion, that without it, the wrong interface was predicted to fail.

Figure 4.31 shows example energy trajectories of models used to determine the bead-bead non-bond energies. Figure 4.31a shows the cohesive case of the Delft epoxy, and Fig. 4.31b shows the adhesive case to copper oxide. For the cohesive case, it is almost always in the axial chain direction; for the adhesive case is it almost always parallel to the flat substrate surface (or if the substrate is another polymer, it ends up being similar to the cohesive case, in chain axial directions).

Coarse graining can be done in two ways within the Mesocite software package. The bead itself can be defined then the polymer built from each bead, or an initial network can be built in the molecular modeling builders, and the beads defined by the architecture defined in the molecular model. For these examples the latter was used and once the initial unit cell was built, supercells (replication of the initial unit cell) could be constructed to build the superstructure. Figure 4.32 shows some of the molecular models and their coarse-grained unit cells to illustrate the concept of the computational simplification possible with coarse graining. The cube at the far left



Fig. 4.32 Left, molecular model (FW~23,000); middle, coarse-grained unit cell of molecular model (FW~23,000); right, optimized CG supercell (FW~8 M)

was the initial molecular model of the epoxy oligomer. The repeat unit (which consisted of the epoxy and curative) was used to define the coarse-grained "bead," and the coarse-grained representative of the oligomer is shown by the middle cube of Fig. 4.32. Simplification of the model is demonstrated as the left and middle pictures represent the same molecular structure. The right cube represents the middle cube replicated until the total mass was well over 8 M. This initial coarse-grained model is 50 nm on a side, as shown in Fig. 4.32, far right. As current state-of-the-art IC features are now <10 nm, these coarse-grained models demonstrated that IC-size structures can be modeled explicitly; however, because of computational time constraints, the coarse-grained models were reduced to 12–15 nm structures. The coarse graining included the copper oxide-epoxy adhesive interface, in which the copper oxide was simply coarse-grained using its unit cell as the bead.

To create the copper oxide interface, a vacuum unit cell of the optimized supercells was created, which was then capped with a layer of copper oxide beads. The copper oxide beads were derived directly from a copper oxide crystalline unit cell. For simplicity (and in keeping with known experiment), it was assumed that the copper oxide did not fail. In this manner, the bonds of the copper oxide remained fixed, and just the non-bond interactions of the copper oxide-epoxy interface were parameterized, using the same procedures as before. An interface model of the copper oxide+epoxy was then constructed using a vacuum cell configuration (vacuum on either side of the copper oxide-epoxy bilayer) creating an infinite bilayer, and this interface construction was energy minimized. It was discovered that to obtain the highest interfacial energies, an additional compaction step was needed, in which the copper oxide was slowly moved down toward the epoxy and briefly equilibrated at room temperature at each step until a new constant energy optimum was found. Without the compaction step, the initially minimized interface was in a local, rather than a global minimum. In all cases the immediate bottom polymer beads next to vacuum were fixed to prohibit global movement of the layer and prevent unreasonable expansion of the polymer into the vacuum.

For the adhesion model, the copper oxide was stepwise displaced into the vacuum away from the polymer layer. Each displacement step was followed by a brief room temperature (RT) equilibration, in which the polymer was watched to see if it would follow the displacement of the interface due to the bond and non-bond interactions. In order to capture a non-equilibrium dynamic, each of the equilibration steps were kept to a minimum, just enough to get past the initially high energies imposed by the displacement step, but never enough to get to equilibrium. However the total number of RT equilibration steps was always kept constant, in order to approximate some relative level of "time." In addition a second simulation was run to look at the pure cohesive interface. In this case, the same vacuum cell was used, but half of the polymer was stepwise displaced into the vacuum, each step also followed by a brief RT equilibration, again to see if the remaining epoxy would follow the rest of the mass. After each step for both the adhesive and cohesive cases, any bead bond that exceeded the maximum bond length criterion was severed. An example of starting and ending (after failure of the interface) models is shown in Fig. 4.33a, b. As with the molecular models, energy versus displacement curves could be



Fig. 4.33 Before (**a**) and after (**b**) side views of the coarse-grained adhesive (vacuum cell) models, showing that failure occurs within the cohesive side of the interface (lighter colored polymer beads left on the darker copper oxide beads); (**c**) shows an example of the simulated stress-strain curve derived from the adhesion models represented in (**a**, **b**) and the associated properties that can be derived from the energy curve

constructed from which modulus, local yield (departure from elastic), global yield, energy gain (storage), and energy loss could be obtained. An example of such a curve is provided in Fig. 4.33c. Construction of these stress-strain curves from the mesoscale model energies has been previously covered in-depth [1, 59] so only the results of the analysis will be discussed here.

The best verification of using coarse-grained models came from two different areas of simulation. One was the modulus prediction based upon the cohesive simulations. It was found that the modulus predicted from the molecular models (2.0 GPa) was the same as the modulus predicted from the coarse-grained models (2.12 GPa) and both matched the experimental modulus (~2.0 GPa), demonstrating a high degree of consistency across the length scales. The second example was the qualitative failure mode. Experimental test results indicated that adhesive failure occurred with some epoxy being left behind on the copper side. That is, failure was not pure adhesive failure that would have led to clean copper surfaces. The coarsegrained adhesive models demonstrated failure within the epoxy rather than clean adhesive failure. Both the modulus and the correct location of failure further demonstrated that a jump in coarse-grain scale to large grains could be done without loss in predictive power (and could be the start of even larger jumps, when software becomes available that will accommodate bead shapes). Start and end side views are shown in Fig. 4.33 of one of the adhesive cases. Clearly failure is in the polymer side of the interface; however, the failure is not purely cohesive either, as indicated in Fig. 4.34a, b. Here, the horizontal cut (rotated top-down view) of just the epoxy beads immediately next to the copper oxide layer at the start and at the end of the simulation is shown. As can be seen from the qualitative change in bead density of this layer, which decreases after failure, there is a mix of both adhesive and cohesive failure occurring, just like observed experimentally. The amount of material left behind after interfacial failure seems to track with the cross-link density and qualitatively tracks with the strength of the interface derived from the energetics. It is remarked that the competition between cohesive and adhesive failure by a continuum mechanics approach was discussed in Sect. 4.5 of the preceding chapter. Cross-



Fig. 4.34 (a) Before and (b) after epoxy layer (top-down view) of the polymer layer immediately next to the copper oxide. The beads represent an epoxy repeat unit and the lines between them are the bead bonds; (c) impact of cross-link density on modulus

link density is another variable that was tracked in these models, and it was found that in general the modulus increases with cross-link density to a point (or decreases with the mass between cross-links) nonlinearly. Figure 4.34c shows the existence of a crossover point when the cross-link density is increased where the adhesive modulus starts to become significantly better than the cohesive modulus.

The base models were adjusted to include the effect of moisture content and interface roughness. An example of moisture impact on the adhesive model is shown in Fig. 4.35, which shows the side views of the start and end models. When compared to Fig. 4.33, it is obvious that the effect of moisture is to increase the amount of deformation before adhesive failure and also to decrease the amount of polymer left behind. That is, the models showed that the failure shifts toward adhesive interface failure. This should not be surprising because the models show that water tends to form its own layer on the copper oxide, which should disrupt some of the polymer adhesion to the substrate.

Roughness was another variable imparted to the adhesive interface by use of a sawtooth copper oxide interface. It was found that there is an angle dependence to the modulus trend, and the higher the sawtooth angle (which means a shallower sawtooth leading to lower shearing), the higher the adhesive modulus and the higher the energy gain of the system. Interestingly, something similar happens with the amount of material being left behind, with an increase in material at the higher sawtooth angle. This base trend is in keeping with the higher modulus but also agrees with the higher energy gain as more material is involved in the failure mechanism. There is an inflection found in all of these trends, suggesting the effect of roughness is nonlinear. Until now all of the adhesive models were run in the same deformation mode in which the copper oxide layer was moved in tension into the vacuum space of the unit cell. However it is possible to also move the copper oxide sideways, in order to investigate increasing shear. To investigate this mixed mode behavior, the flat adhesive interface models were moved in diagonal directions and compared to the sawtooth models which also should contain aspects of both shear and tension. Figure 4.36 shows that the modulus trends with deformation direction are nonlinear,



Fig. 4.35 (a) Before and (b) after side view of the adhesive failure coarse-grained models with moisture involvement; (c) before and (b) after top down views of the polymer layer immediately next to the copper oxide with water beads involved (light-colored beads)

and the different model cases (flat vs. sawtooth) start to lay on top of one another. The shear direction is still showing the lowest modulus, and the tensile direction is showing the highest.

However the next case that was tried gave results that were totally unexpected. To test a mixed tension/shear case, one of the sawtooth cases was used and a sideways movement of the copper oxide across the sawtooth applied, as shown in Fig. 4.37. For this case the energy curves exhibited a cyclic response, as the epoxy polymers went under compression and tension with the sawtooth. The cycles were roughly equivalent to the period of the sawtooth, and the first cycle had an unusually high modulus (not expected from the trends in Fig. 4.36) that were much higher than those found in pure tension, which tapered off with cycling. In addition, at failure, when all bead bonds are broken, there was qualitatively much more material left behind than the original flat interface model, when Fig. 4.34a, b is compared to Fig. 4.37c which uses the same dimensional model, with only the roughness of the copper oxide changed. This suggested that the sawtooth does help to engage more material and lock-in more mass into the response.

Although these are not crystalline models, the observation that there may be material bunching or pileups depending upon the deformation and the roughness



Fig. 4.36 Angular dependence of displacement direction on the modulus



Fig. 4.37 High sawtooth angle Cu_2O interface in shear (horizontal direction), (a) at the start and (b) after failure; (c) polymer remaining on Cu_2O side of interface at failure

brought up a similarity to grain-strengthening or the Hall-Petch relationship where dislocation pileups at grain boundaries increase strength [62]. In crystalline materials the Hall-Petch relationship shows that the yield is inversely proportional to the square root of the grain size, $\sigma_v = \sigma_0 + kd^{-0.5}$, where σ_v is the yield strength or hardness, d is the grain size, and σ_0 and k are material constants. So if there is a similarity to the function of the sawtooth and grain size, a linear relationship should emerge if the inverse square of the yield strength is plotted against the sawtooth pitch to represent the grain size. When the global (maximum energy) and local (deviation from elastic) yields were extracted from the simulated stress-strain curves, it was found that the global yield energies do follow a Hall-Petch relationship with the sawtooth pitch (as do the energies extracted at maximum bond breakage, further tying the bond disruption to the yield). These findings have been reviewed previously [2], showing the Hall-Petch-like relationships found and the similarity to other strength concepts. For instance, maximizing the interactions to maximize the strength is not counter to polymer mechanistic concepts which optimize interactions that lead to limited kink movement. On a very basic molecular level, these mechanism all conceptually rely on maximizing physical interactions to maximize deformation resistance (analogous the grain-strengthening argument). These interaction arguments are important to understand and develop, as they are the underlying basis of why molecular models can be used to engineer materials.

4.7 Mixed Modeling for Thick Film Dielectrics Used in Displays

This example shows aspects of different molecular models (DFT and MD) that were used in order to piece together the performance issues of a dielectric that was targeted for use in displays. There were two application areas of interest at the time: as a planarizing layer and as an encapsulating layer, shown in Fig. 4.38. Although not an IC packaging material, the application is involved in the packaging of light-emitting diodes (LEDs). Additionally the examples demonstrate that sometimes both classical and quantum techniques should be used to get the whole picture. More specifics have been previously reported [1, 2, 63–65].

4.7.1 Planarization Dielectric

During the development of this dielectric, which is an organo-silicate, significant shrinkage was found after cure (Fig. 4.39). The shrinkage was disconcerting because it was entirely unexpected based upon previous formulations. Reasons for the film shrinkage were thought to range from weight loss due to additional cure (and loss of silanol or alkoxy groups), weight loss due to depolymerization, or thickness loss due to packing or polymer rearrangement. Molecular modeling was engaged to determine which was more likely.

The first experimental data to be used for molecular modeling was that of an FTIR of the silicate layer. This would help piece together whether or not the polymer was



Fig. 4.38 Use areas for thick film silicates. (a) General location of dielectrics (filter overcoats, transistor encapsulants, passivation layers, and planarization layers); (b) Schematic of use as a planarization layer



Fig. 4.39 SEM cross section showing shrinkage of the silicate dielectric used as a planarization layer before cure (left) and after cure (right)

degrading. The FTIR results indicated that there was a significant loss in the cage content of the silicate architecture and an increase in the ladder content, which would indicate that additional cure was not causing shrinkage, but the architectures are devolving toward lower cure-type structures. While this alone would not support weight-loss theories from depolymerization, it did support the alternate theory of polymer rearrangement and compaction. It was also discovered that films with the most shrinkage were found contaminated with high levels of metals, but no weight loss differences could be found between the high metal formulations and low metal level formulations. This bolstered the theory that compaction could be a culprit due to known studies which found that metals could depolymerize silicates [66, 67]. If only partial depolymerization was occurring, then no weight loss would be observed, but the new oligomers might compact, which would explain the experimental findings.

The partial depolymerization and compaction were investigated in two ways. DFT was used to calculate the adsorption tendencies of the silicate for the metals, and reaction thermodynamics of cage depolymerization, and simple volume models of groups of silicate architectures (cages, ladders, and rings) were compared for the possible reaction products of cage depolymerization. In both cases, the depolymerized entities emerged as the likely culprit. From DFT, the metal centers were found to be energetically highly absorptive to the silicates, and opening of the cages to ladders and ring structures (the beginning of depolymerization for these structures) was thermodynamically highly exothermic and highly favorable. Partial rather than full depolymerization would explain the lack of weight loss repeatedly found in experimental testing done in parallel to the modeling efforts.

The volumes of simple pairs of depolymerized formulation component structures were then compared. These comparisons showed that up to 35–40% shrinkage (Fig. 4.40, dark bars) could occur upon full depolymerization of the cage structures, which is exactly what was observed. The same volume analysis was used to look at another proposed component (Fig. 4.40, light bars) which indicated there were compositions that might counter the shrinkage by offering some expansion. Formulation components were then looked at for the ability to resist the shrinkage forces



that should exist during cure. This was done using forcing dynamics of formulation component pairs and testing for whether the expected interaction mechanics were enhanced or degraded. Figure 4.41 shows the results of this modeling test in which the moduli and relative strengths were simulated by forcing dynamics. According to these results, one of the newly proposed components should be better able to resist shrinkage. The formulation compositions were then computationally tested for volume change like before. One of the new formulations showed markedly improved shrinkage stability (which is contrasted to the original formulation in Fig. 4.41) and was chosen to move forward.

4.7.2 Encapsulation Dielectric

Another application of a thick film silicate was as an encapsulation layer. The issue for this application was proximity to the liquid crystal (LC) within the display and the impact on the switching of the display pixels. It was thought that the dielectric



Fig. 4.41 Results of modeling of improved formulation over the original showing general trend of improved modulus and strength when the new and original formulation is compared

could slow the switching speed of the IC by current leakage in the layer. To answer whether our dielectric could be involved, the band structures of the formulations were calculated by means of DFT. The bandgaps were estimated directly from conduction to valence bandgap in the band structure. It was found that the bandgaps could be manipulated and increased by choice of monomer and by adjusting the cure which would change the cured material structure, to further ensure that our materials were not causing leakage. In addition, the question was asked whether our material could be involved as part of the dielectric response due to the proximity next to the liquid crystal of the display. One standard test was the voltage holding ratio test (VHR) which tests the ability of a layer to hold a voltage. To answer this question, polarizabilities were calculated based on two of the leading formulations, representing different cure states (silanol content and density being two of the major variables). The higher polarizability was thought be better for VHR, as it should be related to the ability to align with a field. The polarizabilities provided us with one of the best performance correlations, as one of the formulations (Formulation B in Fig. 4.42) showed consistently high values. This material also had higher measured dielectric constant, which is also consistent with its higher polarizability. When VHR testing was done at the customer, it was found that this same material was identified with the best VHR and these formulations were chosen for further development.

formulations



Coarse-Grained Diffusion in a Simulated Photoresist 4.8 Polymer

Another application of coarse-grained models involved diffusion through a polymer [68]. Although the polymer was a simulated photoresist, this example is included because the main topic of diffusion is of general interest to packaging materials and further illustrates the usefulness of coarse graining. In this case, it was thought that one of the organic bases used in a layer next to the photoresist was poisoning the photoresist's acid catalyst so the question was posed to confirm that this was the case and coarse graining was used, encouraged by previous work looking at diffusion of fluorinated blowing agents [68]. The photoresist itself was approximated using methyl methacrylate in which the entire repeat unit was parameterized as a bead. The different bases simulated were based upon those known to be used in the layer next to the photoresist. They were generally highly hydrophilic molecules with an organic base head and a hydrophilic polymer tail. The beads were defined based upon the functionality of the base head and the repeat unit in the long chain tail. The different parameterizations that were constructed were based upon nine different interactions: base-base, base-tail, base-acrylate, base-water, tail-tail, tail-acrylate, tail-water, water-water, and water-acrylate. The bases were built using the same base head but varying the size of the tails to represent the sizes of bases available commercially.

A coarse-grained PMMA polymer mass was built and optimized (approximately $200 \times 200 \times 350$ Å), and a 200×350 Å vacuum unit cell created with 200 Å thickness. To force diffusion only in one direction, a physical barrier layer was also used consisting of a graphite layer placed near the top of the polymer mass. Usually molecular modelers do not use a barrier layer configuration for diffusion, but this proved to be a good practice in a past study in order to concentrate diffusion in one direction for the evaluation of fluorocarbon blowing agents [68].



Fig. 4.43 Example diffusions at the start (left) and end (right) of the simulations. (a) Small MW base diffusion; (b) larger MW

All of the interactions of the base components were parameterized using the same forcing potential technique previously used. However, because this was a diffusion model in which the average forward velocities during diffusion should be small, the non-bond energies were parameterized by the zero intercept of the energy-distance curves in order to establish a lower rate regime than that covered by the mechanical models. This is also the parameterization technique that was used previously for the blowing agents diffusion which found that by using non-bond forces more in-line with an unforced condition, realistic diffusion constants were found (both relative trends and extrapolated values). The barrier itself used artificially high non-bond interactions to prohibit diffusion through the layer (discovered by trial and error in the previous work on the blowing agents). The bases were applied in the vacuum space between the bottom of the polymer and the barrier layer and equilibrated at room temperature for 500 ps. This configuration would force diffusion only in one direction, but no forcing potential was used. In these examples, the direction is defined by where the diffusants are deposited relative to the barrier layer. Diffusion direction in these models is generally bottom to top of the unit cell. The barrier layer beads were fixed for all simulations. In addition, because of computer limitations, the polymer mass was fixed.

An example of before and after snapshots of the amine beads for a low MW and higher MW bases are shown in Fig. 4.43 with the polymer-barrier layer darkened more in order to highlight the light-colored bases. High penetration of the smallest base was found (Fig. 4.43a) which was parameterized as a single bead because of size. However, increasing the molecular weight (MW) started to prohibit penetration (Fig. 4.43b) indicating that MW is a major variable toward penetration into the polymer and may be a factor in the photoresist poisoning. The possibility of poisoning deep inside the photoresist layer is possible, if smaller bases are present.

In addition, moisture was applied within the bases (optimized together before applying them to the polymer) in the diffusion simulation. The trends were generally similar as those simulations without water, suggesting size is the predominant variable. Interestingly, water-induced agglomeration was found for the larger bases, which was expected due to the high hydrophilic nature of the tail used. Figure 4.44b shows an example of the base agglomeration due to water during the simulation. Agglomeration is very evident at the end where the bases have



Fig. 4.44 One of the largest bases simulated. The left side is the start of the simulation and the right side the end. (a) No water case showing no diffusion of the large base, but penetration into the acrylate (below) has begun; (b) case using moisture showing agglomeration of water with the base, which is highly hydrophilic showing even less movement of the base. The effective mass is larger, so there is no hint of penetration. Water is indicated by the light-colored isolated beads and the darker lines are the highly hydrophilic base, while the darkest lines are the acrylate polymer (below, as in **a**)



Fig. 4.45 (a) Results of mean squared displacement (MSD) which estimates diffusivity; (b) maximum distance any base penetrated into polymer. Both show the MW dependency

agglomerated with water and with themselves. The effect can be compared to the case without water, which is shown in Fig. 4.44a in which the large base is just starting to penetrate the polymer. When agglomeration occurs, the artificially high mass (due to agglomeration) has not even approached close to the polymer, and only the small leftover water beads are beginning to penetrate further confirming the MW dependency of these bases.

Both the root-mean-squared displacements (MSD) and the maximum penetration (defined as the furthest distance a base unit diffused into the polymer) was measured and both confirmed that size was the major variable with and without moisture involved (Fig. 4.45). Remarkably, a small base, without the long hydrophilic tails of the other bases, has enhanced diffusion when moisture is involved, and maximum penetration occurs through the full thickness of the polymer layer. Testing has been limited but confirms that size for this type of organic base generally helps control diffusion as the simulations suggest.

Hydrophobic base examples have not yet been simulated, but the current simulations suggest we should see a different effect from lower hydrophilic bases. The surface diffusion trends of Sect. 4.4 suggest that a low hydrophilic nature should penetrate more given the lower surface energies of a hydrophobic material. That is, according to surface theory, lower surface energy liquids should have higher surface wetting, which should help penetrating power along the surfaces of the polymer strands. So extended wetting is expected into the material with the lower hydrophilic bases. We have seen evidence of this kind of penetration along polymers structures in other molecular modeling simulation studies of copper diffusion in porous dielectrics [12, 69, 70].

4.9 Atomistic Simulation of Porous Low-Dielectric Constant Materials

In this section, the chemical-mechanical relationship of the amorphous, porous silica-based low-dielectric (low-k) material (SiOC:H, also referred to as black diamond) is obtained by means of a series of atomistic simulations [71]. The molecular network structure is generated by means of given concentrations of four basic building blocks. This dielectric material was applied in IC backend structures of which the dielectric constant k can be reduced in two ways: (i) replacing oxygen by the methyl groups, H, or OH, or (ii) by creating porosity within the material [72]. The mechanical stiffness of this material is one of the main parameters that governs the reliability of IC backend structures. In order to understand the variation in the mechanical stiffness and density resulting from modifications to the chemical configuration, sensitivity analyses were performed. The trends indicated by the simulations exhibit good agreement with experimental data. In addition, the simulation result shows that Young's modulus of the SiOC:H is dominated by the concentration of only two basic building blocks, whereas the density is influenced by all the basic building blocks.

4.9.1 Atomistic Model of SiOC:H

A schematic picture of SiOC(H) is shown in Fig. 4.46 [73]. The different Si atoms are usually related to the number of linked O atoms: zero (Z), mono (M), di (D), tri (T), and quadri (Q). The bond terminators are of the type Si–R, where R is the –CH3, –O, and –OH functional group [74]. Measurement results [74] show that the concentration of Si–Si bonds is relatively low compared to Si–O and Si–C bonds.

Instead of generating the amorphous structure manually [75] or based on amorphous silicon [76], the SiOC:H structure is realized by means of the basic building blocks. The size of the void is assumed equal to the basic building blocks, while the groups are not allowed to connect to voids. It is further assumed that only a single



Fig. 4.46 Chemical structure of SiOC:H illustrating the connection capability of the basic building blocks



Fig. 4.47 (a) Generated approximate molecular configuration of amorphous SiOC:H (b) is the molecule after minimization

bond exists between any two atoms. In order to establish the molecular model of SiOC:H, the concentration of the basic building blocks (from experimental data) is used as input to the algorithm. The distribution of the building blocks obeys three formulating rules, including the chemical characteristics of the Q, T, D, and M blocks, the average distribution of the basic building blocks, and the minimization of the dangling bond in the molecule. The stereochemical structure is established by minimizing the total potential energy of the aforementioned topology. Details of the algorithm are provided in [71]. An example of an approximate topology of SiOC:H is illustrated in Fig. 4.47. Due to the cubic framework, most of the atoms are not in a state of equilibrium. To minimize the potential energy, a structural relaxation, also known as the geometrical optimization procedure [77], is employed. Consequently, an approximate SiOC:H atomistic model is obtained; see Fig. 4.47b. This geometry is subsequently used as initial configuration in the MD simulations.

The accuracy of the thus obtained structure was qualitatively validated by considering two molecules: SiOC:H prior to and after UV treatment [71]. FTIR experiments [74] showed that the Si-O-Si bond angle is reduced after UV treatment. The results from the two models, based on the experimentally obtained building block concentrations, confirm the loss of the bond angles. In addition, the calculated Young's moduli and density values for materials show a good agreement with experimental values [78].

4.9.2 Simulation Results

To study the effect of the separate building blocks on the resulting stiffness and density, a parametric study was performed in which several "series" were defined: series A is similar to the actual low-k materials, the chemical composition in series B is similar to A; the models C1, C2, and C3 emphasize the effect of Q, T, and D, respectively; and D1 is the extreme case air. The particular ratios are shown in Fig. 4.48a. The simulation results in terms of Young's modulus and density are given in Fig. 4.48b. Generally speaking, the A and B series show similar properties as the ratios of the different building blocks are comparable. For the C series, however, the simulated Young's moduli and densities exhibit large variation. Most prominently, the sensitivity shows that the basic building block Q positively affects Young's modulus and density while the amount of D appears to have an inverse effect on the properties. Clearly, increasing the porosity decreases both Young's modulus and density.



Fig. 4.48 (a) Shows the ratio of building blocks for each model; (b) calculated Young's modulus and density values

4.10 Conclusions

This chapter attempted to underscore the versatility of molecular modeling to solve different issues that arise in the performance of materials and their interfaces used in electronics packaging. It concentrated on the use of comparison models in order to more quickly impact materials developed for specific applications, as well as on developing models that predict specific properties.

There have been many lessons learned and discovered over the course of doing materials development using molecular modeling, of which several are covered in this chapter: (1) Small forcing dynamic models are quick and give the right trends. (2) The impact of the substrate surface energy on wetting runs the opposite to the impact of the formulation on wetting. (3) The impact of moisture generally increases wetting (bleed) behavior above that predicted by theoretical trends alone, but which can be found directly in the simulation. It is most likely a combination of impacting the formulation surface energies and substrate. (4) Adhesion and cohesion trends are well-captured by the simple forcing dynamic model. The effect of moisture can be captured, and those interfaces more sensitive to plasticization by water can be found. (5) Stress-cycling simulations are better suited to understand reliability issues than a simple adhesion model (i.e., adhesion and cycling are not equivalent and must be used depending upon the performance requirement). (6) Moisture disruption of adhesion is demonstrated in the molecular models by the lower energies found. Energetically, water is found to weaken both the adhesive and cohesive side of the interface. (7) Scaling molecular models to larger models such as DEM can be done by providing key energy relationships from the molecular models. (8) Scaling molecular models to coarse-grained mesoscale models has been done with a jump in scaling using larger repeat units (rather than functional group) without degradation in predictive power which broadens the applicability of mesoscale models. (9) There is remarkable continuity between the elastic moduli found (molecular model, coarse grain, and experiment) suggesting a correlation between modulus and molecular level origins. (10) The coarse-grained mesoscale model also adequately reproduces the observed failure mode (mixed adhesive/cohesive failure), including the effects of water and interface roughness. (11) For the epoxy-copper oxide interface, mesoscale yield energies for the adhesive bond are found to be degraded more severely by moisture than the cohesive side, leading to the observed loss of adhesion. (12) Larger diffusion modeling can be accomplished using coarse-grained mesoscale diffusion in order to evaluate material trends, but care must be used in parameterizing the beads to reflect low global rates.

Due to the rapid development of micro-/nano-electronic technology, structures are approaching submicron and nanoscales. To design reliable structures and devices at low cost, it is essential to establish the structure-property relation, i.e., the relation that quantifies the critical properties (e.g., fracture toughness) as function of chemical composition, fabrication process, and dimension. Molecular modeling is advancing rapidly. With the advent of high-speed computing, larger molecular systems can be explicitly modeled. When combined with the advancements in multi-scale methods, this results in truly predictive simulation capabilities at macroscopic (product) scale by means of dedicated scale bridging techniques, as discussed in Sect. 4.8 of the preceding chapter. Consequently, *materials and interface engineering* will become possible, most ideally within an industrial setting.

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Chapter 5 Soft Mold Nanoimprint: Modeling and Simulation



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5.1 Introduction

Nanoimprint lithography (NIL) is a promising process for low-cost nano-pattern mass production. De-molding is a critical part in the nanoimprint process. Due to the mechanical contact with the substrate during the printing process, small features on the mold are easily damaged [1] which limits the application of nanoimprinting. The interaction between the mold and the substrate greatly affects the patterning result. Low adhesion force at the de-molding interface is preferred in NIL [2]. It is hard to measure the adhesion force at the interface between the nano-patterned mold and the substrate. As the feature goes down to the micron scale, the material property dominates the interfacial adhesion force [3]. A simulation model, which is able to estimate this interaction, is urgently needed. Currently researches are focused on simulating the thermal nanoimprint process [4, 5]. Fan et al. have introduced a multiscale approach for investigating the interfacial delamination, which links nanoscale material properties and macroscale adhesion force measurement together [6]. Simulation methods for the de-molding process in UV nanoimprint are still lack of study. Compared to the thermal nanoimprinting, UV nanoimprinting requires lower imprint pressure and shorter process time. It has a wide range of application, especially for flexible electronics fabrication. Due to the length scale issues, molecular dynamic (MD) simulation or traditional finite element methods cannot be employed individually to simulate the de-molding process. As a result, in this chapter, a multi-scale approach combining both MD simulation and finite element analysis is proposed to simulate and predict the adhesion force between the nano-patterned mold and the polymer film substrate in UV NIL.

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5.2 General Steps for Multi-scale Simulation

The present study is focused on incorporating material behavior at the de-molding interface of the nano-patterns. As the process is aimed at nanoscale features, MD simulation is an effective tool to study the interaction with an interfacial force field [7]. To simulate the soft mold UV nanoimprint process, the mold material, polyvinyl alcohol (PVA) is selected, modeled, and according to the patent from AMO [8], benzyl(meth)acrylate-based material is used as the UV-curable photoresist (PR). The hydrophobic coating material trichloro(1H,1H,2H,2H-perfluorooctyl)silane is applied on top of the PVA surface to reduce the adhesion force.

The illustration of nanoscale simulation is shown in Fig. 5.1. MD simulation is used to calculate the interfacial energy between the PVA mold and the methacrylatebased resist layer (Fig. 5.1a). By recording the atomic configurations and energies of the system from each simulation step during the mold separation, the energydisplacement curve is plotted. A stress-displacement curve can be achieved from the slope of the energy-displacement curve. The results are then utilized to characterize the material properties at the interface.



Fig. 5.1 Illustration of the steps of MD simulation: (a) 3D molecular model of UV nanoimprint, (b) energy calculation, (c) stress calculation



Fig. 5.2 Simulation method linking nanoscale and macroscale [6]

Finite element models are then built using ANSYS with an interfacial element at the PVA-PR interface. The constitutive relations from MD simulations (stress-displacement curve) are incorporated into the cohesive zone model to study the de-molding process under tensile loading, which covered the length scale from nanoscale to macroscale (Fig. 5.2). The force-displacement relation, computed from the macroscale model in ANSYS, is used to compare and verify with the experimental results. A peel-off test is conducted to measure the adhesion force between the PVA film and the PR-coated Si wafer. To reduce the time of computation, 2D models are adopted in the finite element calculation.

5.3 Molecular Dynamics Model

To investigate the mechanical properties of materials at the nanoscale, accurate modeling of the atomic interaction is essential. The main objective of the nanoimprint process is to fabricate small features at the sub-100 nm range. MD

simulation is an effective tool to study the interaction with an interfacial force field under external loading.

5.3.1 3D Atomic Molecular Model

The simulations are conducted by using the DISCOVER module of the Materials Studio software (Accelrys Inc.). Multi-material systems are built for the MD modeling. The 3D molecular model contains three parts. The top part is the mold, while the bottom layer is the Si wafer. A polymer layer is inserted between them. Two types of molds are built and computed. The first one is a pure PVA mold, and the second one is a PVA mold with a monolayer of silane coated on it. The 3D molecular model of PVA has a ratio of 1:1 containing cis-and-trans configurations. The molecular weight of the PVA in the experiment was over 89,000. To reduce the calculation time, the chain length of the PVA molecule in the model is 20. The simulation was focused on the interface behavior. The molecule model of PVA represented part of the molecule which was close to the interface. The Si crystal layer, with the $(1\ 0\ 0)$ surface facing up, is modeled as the substrate. Figure 5.3 shows the images of the molecular models for each material. The total number of molecules was determined by the density of materials. The density of each material is listed in Table 5.1. Figure 5.4 shows the full model configurations of the two systems being studied. Both models were built with a rectangular simulation cell, which has a periodic boundary condition in the x-y plane. The cell box dimension in the x-y plane is 23.04 $\dot{A} \times 23.04 \dot{A}$. Although a cutoff distance of 9.5 \dot{A} is set in the system, a large vacuum space is put on top of the model to avoid any interaction across the mirror image in the z-direction during the calculation.



HALL C



Fig. 5.3 Molecular models of PVA, benzyl(meth)acrylate, and trichloro(1H,1H,2H,2H-perfluorooctyl)silane

Materials	Density (g/cm ³)
Poly(vinyl alcohol)	1.269
Benzyl(meth)acrylate-based photoresist	0.897
Trichloro(1H,1H,2H,2H-perfluorooctyl)silane	1.302

Table 5.1 Densities of the materials in the NIL model





5.3.2 Energy and Stress Calculation

At the beginning, the molecule was well aligned in the cell. However, the polymer should be an amorphous material. After building the molecular model, energy minimization was carried out to find the equilibrated molecular structure of the system by using the Minimizer function in the DISCOVER module, which turns the molecular configuration into an amorphous structure. The COMPASS (Condensed-Phase Optimized Molecular Potentials for Atomistic Simulation Studies) force field was selected for the model. The COMPASS force field enables accurate prediction of material properties for a broad range of materials under different conditions. The convergence level for energy minimization was customized with maximum iterations of 10,000. No constraint was applied to the molecules.

Then the dynamic simulation in the DISCOVER module was computed, while a constant number of particles, constant volume, and constant temperature (NVT) ensemble was adopted in the simulation. The simulated temperature was at 298 K. And the 10,000 time steps were computed. Each time step represents 1 fs. The simulation provided the stable molecule configuration at room temperature. And the energy components, both potential energy and kinetic energy, were calculated. Figure 5.5 shows the change of molecular conformation in each of the simulation



Fig. 5.5 Evolution of the molecular model during the simulation

steps. The change of molecular conformation represented the reduction of the total free energy of the system.

The changes of different energy components are shown in Fig. 5.6a, b, where the potential energies are lower than the non-bond energies. In Fig. 5.6a, there was no kinetic energy involved when conducting the energy minimization. After 7000 iterations, the structure had reached a stable state, and the free energy of the system almost reached the equilibrium state. In Fig. 5.6b, the system temperature was elevated from 0 to 298 K during the dynamic simulation. Kinetic energy was considered in this computation. The total energy increased at the beginning and then reached an equilibrium state at the end of the simulation.

The potential energy (E_0) of the system was obtained after the dynamic simulation. The potential energy of the system provided the information of forces acting on each atom, which can be used to determine the acceleration, velocity, and position of each atom. At this step, the distance between the mold and the PR was considered as 0 Å. It represented the status before the de-molding process. Single material system models were also constructed to calculate the energy level of the mold and the substrate separately. E_a and E_r represent the potential energies of the PVA mold and the substrate, respectively. The interfacial energy (E_{In}) can be calculated from the energy difference using the equation below:

$$E_{In} = E_0 - (E_a + E_r)$$
(5.1)

By using the same method as discussed above, the interfacial energy E_{In} for each interface in the system can be calculated. Figure 5.7 shows all the E_{In} of the system at 298 K. For a defect-free nanoimprint process, the PR would stay on top of the substrate material (Si wafer) after the de-molding process. In addition, it should have a low adhesion force with the mold. So E_{In} at the Si-PR interface should be larger than E_{In} of the PR-PVA interface for a defect-free nanoimprint process. The calculation from the MD models gives a consistent result. And the energy value of the PR-silane interface is further reduced by the silane coating, showing that the silane coating should improve the experimental imprint result.

In the NIL de-molding process, the system is subjected to a tensile displacement. The mold is separated from the PR layer. To simulate the de-molding process in nanoimprinting, all the atoms except for those few layers of atoms near the interface



Fig. 5.6 Energy curves in simulation: (a) energy change during minimization, (b) energy change during dynamic simulation



Fig. 5.7 Value of interfacial energy E_{In} at each interfaces

are held rigid in all the following simulations. The mold (PVA molecule and silane) atoms are selected as a whole and moved up a distance Δd in z-direction, as shown in Fig. 5.8. A tensile displacement was applied on the system in a single simulation step, and energy equilibration was conducted again to relax the free energy of the whole system, while the atoms inside the dash line boxes are fixed to maintain displacement. By calculating the potential energy of the new configuration after the dynamic simulation, a value E_1 is obtained. When the material system is subjected to an external displacement, force will be transferred to the interface by the interaction among atoms whose position and velocity are governed by the above potential energy. The interaction between the mold and PR is by Van der Waals force. The Van der Waals force has little effect when the distance is larger than 2 nm [9]. To obtain the relation between the energy and displacement, the value of Δd should be less than 1 \dot{A} .

The above steps were repeated until the total displacement is larger than the cutoff distance (9.5 \dot{A}). The same displacement step was applied on the system at each cycle. In each simulation cycle, the whole system went through an energy minimization and a dynamic operation for about 10 ps separately at a temperature of 298 K using the NVT ensemble. Each displacement step provides a value of potential energy E_i . The atomic configurations and energies of the system for each simulation step are recorded, and the results are plotted as an energy-displacement curve. The change of potential energy is the work done by the interfacial stresses. Interfacial stresses corresponding to the applied displacement can be obtained from MD simulations by calculating the slope of the energy-displacement curve. The interfacial stress is simply related to the interfacial energy by the following relation:



$$\sigma = (\mathbf{E}_{i} - \mathbf{E}_{i-1}) / (\mathbf{A} \cdot \Delta d_{i}) \tag{5.2}$$

where σ is the interfacial tensile stresses, A is the interfacial area and Δd_i is the displacement applied on the system in each simulation step. E_i is the potential energy of the system.

Figure 5.9a, b shows the energy-displacement and stress-displacement relation obtained from MD simulations, respectively. The relation for the tensile stress shows the nonlinear behavior of the interface. The interfacial stress sharply increases at the beginning of 1 Å and then decreases with the increasing displacement. A large change of the stress happens within a very short distance of 1 Å. The de-molding process is modeled as a crack opening. In each stress curve, there is a bifurcation point, where the continuous failure mode will transfer to a discontinuous failure mode. At the bifurcation point, the interaction force between the atoms will be at the maximum value where the macroscopic response of the interface is the initiation of delamination. After the bifurcation point, the discontinuous failure mode takes over and the stress-strain curve describes the de-molding process. It is clearly shown in the curves that the silane coating significantly reduces the interfacial stress up to 50%. The stress value at the bifurcation point is then output to the FEM model to


Fig. 5.9 Energy-displacement and stress-displacement relations

conduct further simulation at the macroscale. The simulation results from the MD model provide the material property of the cohesive zone elements in the FEM simulation.

5.4 Finite Element Model

The cohesive zone model (CZM) is widely used to simulate fracture processes in different kinds of composite materials under different loading conditions [10]. The key of the CZM is the traction-displacement constitutive relation, which includes cohesive strength, separation distance, and cohesive energy. These cohesive parameters could be obtained from the above constitutive relation derived by MD simulations.

A bi-material system finite element model was built by using ANSYS with interfacial element at the mold-PR interface, as shown in Fig. 5.10. The model was used to simulate the de-molding process under tensile loading in UV nanoimprinting. Because both the PVA mold and the PR layer had thicknesses at the micron scale, the mesh size needs to be as small as few micron. Larger mesh sizes will lead to a discontinuous solution error, as the soft mold undergoes a large deformation during de-molding. To reduce the computational time, the problem was simplified to a 2D model using the plane strain assumption. The constitutive relations from MD simulations (stress-displacement curve) were extracted to provide material properties for the cohesive zone element.

In the model as shown in Fig. 5.10, the top layer was PVA film, while the substrate was cured PR. The PVA film and PR layer both had a thickness of 20 μ m. The size of model was in the macroscale, and the adhesion force between the PVA and the PR is very small. The deformation of the PVA mold was assumed to be linear elastic, homogeneous and isotropic. The mesh size for the elements was 5 μ m. The bottom surface of the PR was fixed. In the UV NIL, the thickness of PR is 200 nm, which is smaller than the mesh size, and the PR sticks on the Si substrate tightly. Therefore, the mechanical property of PR is replaced by Si in the finite element model. A vertical displacement of 0.8 mm was applied to one end of the PVA film. The total simulation time was 8 s, and the separation speed was 0.1 mm/s. The simulation time was divided by 8000 sub-steps. A contact de-bonding model was selected to be the type of fracture.





Fig. 5.11 Force-displacement curve from finite element model

The force reaction was calculated from the 2D model and plotted against the displacement, as shown in Fig. 5.11a, b. The figures contain curves which are plotted by using different numbers of simulation sub-steps. In the simulation, the force decreases when increasing the number of sub-steps. The values become very close when the sub-steps are over 4000. In Fig. 5.11a, b, the top curves are from 1000 sub-steps, while the bottom curves represent 8000 sub-steps. The magnitude of the force was normalized by a scale factor in order to compare with the result of a 5-mm-wide sample. The simulated force increased rapidly with the displacement at

the beginning and reached the maximum value where delamination being initiated. And then the force decreased to a stable value for further displacement. This stable value represent the adhesion force for the de-molding process in UV NIL.

5.5 Experimental Measurement of Adhesion Force

A peel-off test was conducted to measure the adhesion force between PVA and PR. The experiment setup is shown in Fig. 5.12. Si wafers were used as the substrate material in the experiment. The width of PVA film was 5 mm. A UV-curable polymer layer was first coated on the Si, and then the PVA film was pressed against the polymer later. The PR layer was cured by exposing to UV light with the PVA on top of it. Then the sample was fixed on the testing stage of the universal testing machine (UTM). One end of the PVA film was connected to the 2N load cell. Vertical displacement was gradually applied by the UTM under constant speed of 0.1 mm/s.

Results of the force measurement are shown in Fig. 5.13. The peak values represent the initiation of cracking. When the displacement is larger than 4 mm, the measurement value represents the adhesion force between the mold and the substrate. Figure 5.14 compares the experimental and simulation results. The simulation value is chosen from the curve in which 8000 steps were used. The results fall within the same range.

The hydrophobic silane coating greatly reduces the adhesion force between the mold and the substrate. With this coating, the defect of delamination during the nanoimprint process was greatly reduced. As a result, the yield of the NIL process





Fig. 5.13 Force measurement from peel-off experiment



Fig. 5.14 Adhesion force between the mold and substrate

was improved. Figure 5.15 shows the imprint result using two types of PVA mold including a pure one (a) and a silane-coated one (b). The stronger adhesion between the resist layer and the pure PVA layer caused the delamination during the de-molding process. The bright area in Fig. 5.15a is the exposed Si surface, and Fig. 5.15b shows good pattern duplication.



Fig. 5.15 SEM of imprinted pattern on Si wafer: (a) using pure PVA mold, (b) using silane-coated PVA

5.6 Summary

A multi-scale simulation method combining MD and FEM simulations, which is able to predict the adhesion force during the de-molding process in soft mold UV nanoimprinting, was demonstrated. A 3D molecular model for the multi-material system was constructed for the MD simulation. The constitutive relations between PVA mold and PR were obtained from the change of potential energy of the system. The multi-scale approach was proposed using the derived constitutive relation in the MD simulation, which links different length scales together. Our proposed model shows that the hydrophobic silane coating greatly reduces the adhesion force between the mold and substrate.

The bi-material system was built by using the ANSYS code. Two-dimensional simulation based on a plane strain condition was performed to simulate the peel-off process of UV NIL. An experiment of the peel-off test was conducted to measure the adhesion force. The results from experimental measurement match the computed results from the multi-scale simulation method. By comparing the SEM images of UV nanoimprint, it confirms our assumption that the lower adhesion force improves the yield of the nanoimprinting process. The pattern quality from silane-coated PVA mold is comparable to the de-molding-free process with a much shorter process time.

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Chapter 6 Nanoparticle Properties



James E. Morris

6.1 Introduction

As the radius, r, of a spherical particle shrinks, the surface/volume ratio, 3/r, and the proportion of its constituent atoms at the surface both increase. The stable interatomic bonding arrangements which exist within large crystals are not satisfied for surface atoms, which therefore become more mobile and more reactive, and nanoparticle properties become dominated by surface properties.

The nanoparticles discussed below will all be metallic, but most of the phenomena described will also apply to nonmetallic materials. They will appear in three contexts:

- In an aqueous environment [1]
- In a "cermet" (i.e., in a two-phase ceramic-metal [2] or polymer-metal [3] mixture)
- On an insulating substrate surface, as a discontinuous (island) metal thin film (DMTF) array of nanoparticles [4]

In the first two cases, the nanoparticles are usually modeled as spherical, but shape becomes an issue for the DMTF.

Classical nucleation theory covers the initial formation and growth of the nanoparticles, but the predicted critical nucleus sizes (beyond which the nuclei can grow as stable units) in the sub-nm range are clearly inconsistent with the classical model's use of bulk thermodynamic properties. For nuclei containing only a few atoms, as is typically the case in all these systems, the "atomistic" nucleation theory is necessary [5].

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6.2 Structure

Nanoparticles can exist as perfect crystals, since impurities and lattice defects alike can migrate to the surface in relatively short times. Debye-Scherrer broadening of electron diffraction rings provides a means of determining nano-crystallite sizes, with their radii giving lattice spacings. The weakening of the internal lattice structure at finite sizes leads to contraction, Δd , of lattice spacings, d,

$$\frac{\Delta d}{d} = \beta\left(\frac{2\alpha}{r}\right),\,$$

due to surface tension α , where β is the (anisotropic) linear compressibility [6]. However, surface energy, σ , also varies with r as

$$\sigma(r) = \sigma(\infty) \left(1 + \frac{3}{8} \frac{r_m}{r} \right),$$

where r_m is the screening radius (<5 nm), so the more complete form is

$$\frac{\Delta d}{d} = \beta \left(\frac{2\alpha(\infty)}{r} \right) \left(1 + A \frac{r_m}{r} \right),$$

where A is a constant [6]. (A counter effect of lattice parameter increase with decreasing size has also been reported [7].)

In the absence of any other information, nanoparticles in cermets and aqueous suspensions are usually assumed to be spherical, at concentrations sufficiently below the percolation threshold that particle contacts and coalescence can be ignored. (The percolation threshold is the minimum concentration for metallic electrical conduction through the medium.) However, in liquid environments anyway, the size [1] and shape (i.e., spheres, cubes, or rods [8]) of the nanoparticles can be controlled by varying the precipitation conditions.

Once the nanoparticles are fabricated, they will tend to clump together, presumably under electrostatic forces, and some form of coating must be applied to keep them separated, usually some form of polymer or other organic coating for ease of removal when the nanoparticle property required needs to be activated [9].

In the absence of other considerations, the minimum energy configuration for a nanoparticle with bulk and surface energies would be a sphere, but the equilibrium minimum energy shape of a charged particle is actually an ellipsoid of rotation [10]. Looking through a DMTF, the nanoparticle islands appear to be slightly prolate in shape [11]. However, it is well established that the island size varies during DMTF deposition as r^2 proportional to time (or deposited mass) not r^3 as expected for quasi-spherical growth [12]. So the dominant particle shape is oblate, with possible causes being electrostatic, as mentioned above, or substrate adatom capture with insufficient thermal energy to reach a spherical equilibrium.

6 Nanoparticle Properties

Another factor in the nanoparticle's shape may be its degree of crystallization, and the relatively weak binding of the surface atoms in particular permits rapid motion and continual abrupt crystallographic reconstructions of 1-10 nm nanoparticles on a time scale of seconds [13, 14], with the relative stabilities of different crystallographic forms determined by the bulk and surface energies [15, 16].

The relatively rare electron micrographs of nanoparticle islands from the side [17] show that they are neither spherical nor hemispherical, as often assumed in simplistic models. For most metals on insulators, the contact angle, θ , is greater than 90° and can be reasonably calculated from bulk surface energies σ_{sv} , σ_{sc} , and σ_{cv} , where s, v, and c refer to substrate, vapor, and condensate, by

$$\sigma_{sv} = \sigma_{sc} + \sigma_{cv} \cos \theta$$

giving $\theta \approx 136^{\circ}$ for Au on glass, in good agreement with observation [4].

Chapter 7 reviews nanoparticle preparation, but there are a couple of niche techniques worthy of special mention. Chu et al. spin coat photoresist with dissolved Cu ions on the substrate and use a positively biased atomic force microscope tip to reduce the ions to metallic Cu [18]. A sequence of dots can form an electrical interconnect line, but although the thickness is nanoscale, the lateral resolution is barely submicron. In another electrical charge-driven technique, positive ions in solution are dispersed by the like charges and then deposited as charged nanoparticles by an electrically biased nozzle [19].

6.3 Electrical Properties

If the surface atoms are characterized by incompletely satisfied "dangling" chemical bonds and the surface can be considered to be disordered, then this disorder extends into the crystal interior as dimensions decrease. If metallic conductivity is associated with the band structure of a regular crystal, the question arises as to whether metallic properties can be maintained at nanoscale dimensions. It has been shown for Pd that metallic properties persist at room temperature down to a cluster size of about 12 atoms (≤ 1 nm diameter), with the metal-insulator transition occurring at smaller sizes as the temperature goes up (Fig. 6.1) [20]. Kreibig applied a different criterion, the experimental observations of dielectric absorption in glass containing Ag or Au nanoparticles, to conclude that the "cluster-solid state" transition occurs at ~500 atoms/particle, (i.e., ~2.5 nm diameter) [21].

The nanoparticle Fermi energy varies with size, leading to increasing work function, ϕ , as dimensions shrink

$$\varphi(\mathbf{r}) = \varphi(\infty) + \mathbf{B}/\mathbf{r},$$



Fig. 6.1 The metal-insulator transition as a function of number of atoms and temperature. Calculations were based on tight-binding (TB), pseudo-potential (SIESTA), and simpler (square band) models [20] (With permission)

where B is a constant [22], e.g., a shift from 4.50 to 4.53 eV for a 10 nm radius W nanoparticle [23]. At very small sizes, the work function changes fluctuate due to the changes in finite small numbers of surface atoms [24].

6.4 Catalysts

Catalysts are used to speed up chemical reactions, typically by one of the two mechanisms [25]:

- The provision of a new reaction path of lower activation energy
- The provision of a surface to which the chemical reactants can adhere and react more readily than, for example, in the gas phase

The rapid advances of nanotechnologies have spawned many new innovations in nanoparticle catalysts, including their application in biomedical applications [26], as "seeds" for the vapor-liquid-solid (VLS) growth process in chemical vapor deposition (CVD) of both carbon nanotubes (CNTs) [27] and nanowires [28, 29], and the use of carbon nanoparticles and CNTs as support structures for nanoparticle catalysts [30], ensuring maximum active surface exposure.

6.5 Melting Point Depression

At small sizes, nanoparticles may melt at temperatures significantly below the bulk melting point (MP) [31-34], due to increasing surface energy at small sizes [35]. This phenomenon has been studied for decades, along with the parallel rapid evaporation of such nanoparticles due to their increased vapor pressure at high surface curvatures [36]. An example plot is shown in Fig. 6.2 [32], for three different metals, illustrating that a unified theory may be possible and that significant reductions require nanoparticle dimensions of ~5 nm or less.

Different electron microscopy techniques have been used to determine the MP. Sambles, for example, monitored the evaporation of small particles at controlled temperatures and noted the size when the evaporation rate changed, interpreting this as the melting point [32]. Others have noted the transition from sharp to diffuse electron diffraction rings [37] or the loss of diffraction ring intensity [38]. Allen et al. [37] used dark-field images, interpreting the disappearance of the image as the melting point. One might also look for the disappearance of crystal facets to indicate melting, but the method fails at small sizes when solid particles may not exhibit faceting [37]. Comparisons of dark-field and bright-field images reveal a two-step melting process, with the abrupt appearance at the "solidus" temperature of a surface liquid sheath, surrounding a solid crystalline core which shrinks as the temperature continues to increase, until it disappears abruptly at the higher "liquidus" temperature [39]. More recently, differential scanning calorimetry has been used to determine the melting point [40].



Fig. 6.2 Experimental melting point depression for Au, Sn, and Pb, normalized to the bulk melting points [32]. (With permission)

To a first order, the MP, T_M , for a particle of radius, r, may be related to the bulk value, T_{∞} , by an empirical, experimental equation [37, 41]:

$$\frac{T_M}{T_\infty} = 1 - \frac{r_0}{r}$$

where r_0 is interpreted as the limiting radius for which the particle remains liquid at 0°K [42]. The two dominant approaches to the theory are thermodynamic [37, 38, 43–45] and the "surface layer" model [41, 46], compared in [42]. In general, the thermodynamic models vary in the formulae for r_0 (although one [44] suggests the form $T_M/T_{\infty} = 1 - [r_0/r]^2$). The existence of a liquid-like shell on the nanoparticle has been demonstrated [46], and a good match of theory to experiment can be obtained by adjustment of the unknown layer thickness, t_0 , to an equation of the form [46]

$$\frac{T_M}{T_\infty} = 1 - \left[A + \frac{B}{r} + \frac{C}{r - t_0}\right],$$

where A, B, and C are thermodynamic constants. The two-step melting process leads to complexities in alloy systems, due to compositional phase changes [40]. A more physically based form which agrees with experiment very well is

$$T_m(r) = T_m(\infty) * \left(1 - \frac{2 * \sigma_{sl}}{\rho_s * \Delta H_f(\infty) * r}\right)$$

where σ_{sl} is the surface tension between solid and liquid, ρ_s is the density of solid material, and $\Delta H_f(\infty)$ is the latent heat of fusion of the bulk material [47].

The high MPs of no-Pb solders lead to higher thermomechanical stresses than for conventional eutectic Sn-Pb solder, and melting point depression may be one mechanism to reduce the process temperatures and thermomechanical failure rates. The MP of Sn-Ag alloy, for example, has been shown to be reduced from 222 to 193 °C for 5 nm radius particles [48]. It turns out that normalized curves of Fig. 6.2 hold for alloys too [40] and a rough rule of thumb might be that the MP reduction from the bulk is roughly 5% at 5 nm radius. Clearly, suggestions in the literature of significant MP reductions in particles of a few 100s of nm have no basis and probably refer to sintering.

6.6 Sintering

The three mechanisms of coalescence of adjacent nanoparticles are shown in Fig. 6.3 [49]. "Ostwald ripening" results from the fact that the equilibrium rate of atomic "escape" for nanoparticles is inversely proportional to the radius of curvature. So for two adjacent particles of unequal size as shown in Fig 6.3a, the rate of atomic escape from particle #2 exceeds that from particle #1, resulting in net growth of particle #1 at the expense of the smaller particle #2. Clusters may also migrate freely about a



Fig. 6.3 Coalescence of nanoparticle "islands," due to (a) Ostwald ripening, (b) sintering, and (c) cluster migration [49]. (With permission)

surface (or in other environments) with thermal energy and may collide and coalesce with other similar clusters (Fig. 6.3c). It has been suggested that the driving force behind such coalescences may be electrostatic, due to random polarizations of the particles.

In this section, we are primarily concerned with sintering, as illustrated in Fig. 6.3b. The process is dependent upon the local radius of curvature, as

$$\frac{X^n}{r^m} = A(T)t$$

where A(T) is a temperature-dependent constant, t is time, and n = 7 and m = 3 for surface diffusion. If X and r are comparable, rearranging the equation to

$$t \alpha (X/r)^7 r^4$$

shows why sintering times are dramatically reduced for nanoparticles compared, for example, to microparticles, making even room temperature processing feasible.

The sintering process has been modeled by molecular dynamics [50, 51] and is exothermic at the critical point when the neck fills in [51]. Shin et al. use this property to achieve rapid low-temperature sintering of a silver oxide/silver carboxylate ink [52].

Sintering is an essential step in the effective use of nanoparticles to enhance conductivities of isotropic conductive adhesives (ICA) and in the application of ink-jettable conductive connectors in flexible electronics [53, 54] and Chaps. 3 (theory), 11, and 14.

6.7 Mechanical Properties

The effects of nanoscale particulates on the mechanical properties of thin films have been well studied [55, 56] and generally improve as film thicknesses and particulate sizes decrease. At an elementary level, one can consider the improvement to be due to the relative lack of grain boundaries and defects in nanocrystals [57]. For metallic thin films, for example, yield strength is proportional to $r^{-1/2}$, (the Hall-Pecht relation,) [55], and granular cermets display discontinuities in mechanical properties at the percolation threshold, with increased hardness figures observed for discrete particulate structures [56]. The different behaviors above and below percolation are due to the ability of dislocations to move along continuous metallic percolation paths above the threshold, whereas they are confined to the nanoparticles below [56].

For an atom in a crystal of lattice spacing a_0 , the restoring force σ for displacement x from equilibrium can be approximated by

$$\sigma = \sigma_{\max} \sin \left(2\pi x / \lambda \right)$$

for $x \le \sigma_{max}$. For small increments in x, the crystal strain = dx/a₀, and in the elastic region, Young's Modulus E = stress/strain = d $\sigma/(dx/a_0)$, so

$$d\sigma/d\mathbf{x} = \mathbf{E}/\mathbf{a}_0 = (2\pi/\lambda) \ \mathbf{\sigma}_{\max} \cos\left(2\pi x/\lambda\right) \approx (2\pi/\lambda) \ \mathbf{\sigma}_{\max} \text{for } \mathbf{x} \ll \lambda$$

i.e., $\mathbf{\sigma}_{\max} \approx \lambda E/2\pi a_0 \approx E/2\pi \text{ if } \lambda^{\sim} \mathbf{a}_0$

So one might expect materials to fracture at around $\sigma_{max} \approx E/10$ rather than at the more typical $\sigma_f \approx E/10^4$. But in thin films and whiskers, σ_f can reach around E/15, and similarly nanoparticles are expected to be much stronger than microparticles in composites because of the lack of grain boundaries, etc. [57]

In new applications, however, and for the effective modeling of nanocomposites at the nanoscale, the mechanical properties of the nanoparticles themselves must be known. The physical problems in making such measurements on individual nm scale particles will be obvious, but progress is being made. A theoretical basis for the increase of Young's modulus, compressibility, etc. of nano-dimension materials has been established [58] and shows that the dramatic increases in such properties begin (for Cu as an example) at 20 nm, accelerating below about 5 nm.

Direct measurement of the hardness of individual Si nanoparticles of radii 20–50 nm gives values around five times the bulk value for the smaller sizes, increasing with successive measurements as dislocations accumulate within the particles [59].

6.8 Coulomb Block

The energy of an isolated charged conducting spherical particle of radius, r, is

$$\Delta E = \frac{q^2}{4\pi\varepsilon} \cdot \frac{1}{r},$$

where q is the charge and ε is the effective dielectric constant of the surrounding medium, ΔE being the work done in removing charge –q from the initially neutral sphere to infinity. If the charge only needs to be removed to distance s from the sphere, e.g., to a contact or adjacent particle "island," the work done is reduced (Fig. 6.4) to [4, 60]:

$$\Delta E = \frac{q^2}{4\pi\varepsilon} \cdot \left[\frac{1}{r} - \frac{1}{r+s}\right]$$

In an assembly of N_∞ nanoparticles, Maxwell-Boltzmann (MB) statistics predict that n particles will be charged, where $[4,\,60]$



Fig. 6.4 Electrostatic charging energy ΔE as a function of island radius, r. The three clusters of lines correspond to $\varepsilon_r = 1$ (top), 2, and 4. Within each cluster, the four lines correspond to gap width, s = 1 (bottom), 2, 5, and ∞ nm. Thermal energy, kT, is shown for comparison at T = 4, 77, and 300 K [61]



Fig. 6.5 Electrostatic charging energy for island of radius r. The composite function $\Delta E(x) - qFx$ develops a maximum at high fields, where $\Delta E(x) = q^2/4\pi\epsilon x$ [61]

$$n = N_{\infty} \exp{-\frac{\Delta E}{kT}}.$$

Similarly, a single nanoparticle would be randomly thermally charged for a proportion $\exp{-\Delta E/kT}$ of the time [61, 62].

The thermal charging energy is reduced by the application of an electric field, F [63], which can supply part of the energy required (Fig. 6.5) [61]. At sufficiently high fields, the electrostatic "barrier" may disappear entirely, and this is the condition typically quoted for conduction to occur through a "coulomb blockade," consisting of a conducting nano-island between source and drain terminals, at separations sufficiently small for electron tunneling to occur. At 0°K, the abrupt threshold voltage is at $V = \Delta E/q$, but at finite temperatures, the I–V characteristics are rounded, due to thermal charging effects, until all nonlinearity vanishes when T ~ $\Delta E/k$. (These effects may be seen in Chap. 9, Figs. 9.15 and 9.16).

In practice, as mentioned above, small metallic islands on an insulating substrate are oblate ellipsoids of eccentricity e, and the charging energies must be modified (writing R = 2r+s and p = s/R) to [64]:

- For $F < F_{min} = (q^2/4\pi\epsilon R)4p(1+p)^{-1}[(1+p)^2 e^2(1-p)^2]^{-\frac{1}{2}},$ $\Delta E = q^2/C = (q^2/4\pi\epsilon R)(2/e)[\sin^{-1}e - \sin^{-1}(e(1-p)/(1+p))]/(1-p) - qRF$ • For $F_{min} < F < F_{max} = (q^2/4\pi\epsilon R)4p(1-p)^{-2}(1-e^2)^{-\frac{1}{2}},$
- For $F_{\min} < F < F_{\max} = (q^2/4\pi\epsilon R)4p(1-p)^{-2}(1-e^2)^{-1/2}$, $\Delta E = (q^2/4\pi\epsilon R)(2/e)[\sin^{-1}e - \sin^{-1}(e(1-p)R/((1-p)R + 2x))]/(1-p) - qFx/p$

where
$$x = \frac{1}{2} \operatorname{Re}(1-p) \{ [([\{2qp/\pi \varepsilon F(1-p)^2 R^2 e^2\}^2 + 1]^{\frac{1}{2}} + 1)/2]^{\frac{1}{2}} - e^{-1} \}$$

• $\Delta E = 0$ for F > F_{max}. (See also Chap. 29.)

Conduction across an assembly of nanoparticles takes place by electron tunneling [4], which leads to thermally activated conduction of the form

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$$\sigma = \sigma_0 \exp{-\left[\Delta E/kT\right]^{1/n}}$$

where $1 \le n \le 3$ [4]. The MB distribution of charged islands is swamped by injected charge, which sets up a space charge distribution and a nonlinear field distribution across the film [65–67]. The resistance of such films is sensitive to environmental gases, which modulate the metallic work function and hence the tunneling barrier [68, 69]. The Pd/H₂ combination is unique, in that the dissolution of H₂ in the Pd lattice changes the tunneling barrier width as well as height [70–72]. Applied stress will change the tunneling gap width, too, leading to a very high gage factor, which is linear in s until the stress also affects ΔE [73]. (These effects are treated in more detail in Chap. 29.) Polarization or ion drift in the DMTF substrate [74] (or cermet insulator [3]) can lead to long-term drift in the characteristics and residual currents or hysteresis effects. Islands evolve slowly toward their thermal equilibrium shapes by surface self-diffusion, also causing long-term drift in the electrical properties [75]. And, as a material with a negative temperature coefficient, island films and cermets are subject to thermal runaway, which can lead to thermal switching [76]. Reproducible switching has also been observed in such films [3].

6.9 Diffusion

Metal atoms may diffuse into the insulating phase from metal-to-ceramic/polymer interfaces, creating a localized "cermet" phase. A proportion of the migrating atoms may nucleate into stable nanoparticles that still diffuse away from the interface, but at a much reduced rate [77–80].

6.10 Optical Properties

The existence of a structure-dependent optical absorption peak in discontinuous thin metal films and other nanoparticle aggregates is well documented, with many papers in the research literature [81, 82]. The colors of Ag aggregates in solution can change from yellow to blue with nanoparticle shape changes or solution pH variation [83], and discontinuous Au films can change from blue to green to magenta as the structure changes with thermal annealing (Morris JE, 1969, Unpublished). These effects are unlikely to impinge upon electronic packaging unless possibly with optical interconnect systems but are included here to make the point that nanotechnologies have been with us for a long time and that a full appreciation of their historical context goes back to Michael Faraday [84] and Lord Rayleigh [85], who correctly attributed the colors of gold glass, gold leaf, and aqueous suspensions to the nanoparticle dimensions in the 1800s. The formal theory was first developed by Maxwell-Garnett (MG) [86, 87] and Mie [88] in terms of electron resonances in spherical metal nanoparticles in the 1900s, with contributions by Bruggemann [89]

and David [90] in the 1930s and by Schopper [91] in 1951, before effective medium approaches [92] gained ground in the 1970s.

Yamaguchi et al. [93] and Niklasson and Craighead [94] both showed that better agreement between experiment and theory was possible by treating the discontinuous thin film nanoparticles as oblate spheroids (with the minor axis perpendicular to the substrate) rather than as spheres. Normann et al. [95, 96] similarly modified the MG theory for prolate spheroids (with the major axis parallel to the substrate), while Granqvist CG and Hunderi O (1977, Optical properties of ultrafine gold particles, Personal communication) considered both models before concluding that more complex mixtures of shapes are necessary to match experiment.

Comparisons of experiment and theory have been made for varied structures: discontinuous thin metal films [97–101], cermets [102–104], and other colloidal forms [105–107]. Comparisons are made to both the MG [97–100, 102, 103, 107] and Mie [101, 103, 105, 106] theories. Doremus compared the optical properties of Ag and Au nanoparticles in sol and cermet forms [108, 109] and discontinuous Au films [110] to the Mie theory and finally concludes that the MG theory correctly predicts the absorption peak position but that the width depends upon mean free path limitations in the nanoparticles [7, 110]. Other authors have concluded that deviations of experiment from theory were due to the inappropriate use of bulk parameters.

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Chapter 7 Nanoparticle Fabrication



Masahiro Inoue, Yamato Hayashi, Hirotsugu Takizawa, and Katsuaki Suganuma

7.1 Introduction

A wide variety of nanotechnologies have been developed for the construction of nanostructures with tailored properties. Nanoparticles and related materials, which exhibit characteristic properties, are essential components for the preparation of functional nanostructures. Hence, the technology to handle nanoparticles and related materials needs to be developed to establish the industrial applications of the nanotechnologies.

Nanoparticle technology has a long history. Some metal nanoparticles have been used in stained glass windows even before quantum mechanics was developed [1]. The color of stained glass windows is caused by surface plasmonic effects of Au and Ag nanoparticles. Au and Ag nanoparticle dispersions are used to achieve red and yellow colors, respectively.

Fully fledged metal nanoparticle research started in the 1960–1970s. This research indicated that the melting point of a metal decreases as the size of the metal particle reduces below 100 nm [2]. Since Pawlow [3] reported theoretical modeling for a small particle system in 1909, the thermodynamics of solid–liquid phase equilibria in nanoparticles has attracted great interest from many scientists. Then, Takagi [4] first observed a decrease in the melting point of several metal

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nanoparticles in 1954. Takagi's work was subsequently followed by many researchers to establish the thermodynamics of nanoparticles [5].

In the late 1990s, metal nanoparticles and related materials were recognized as being among the key materials for manufacturing of advanced electronic devices. However, many challenges need to be overcome to establish the practical application of metal nanoparticles and related materials in the field of electronic packaging. Among them, the development of smart processing for mass synthesis of these materials is one of the most important goals. In addition, in situ surface treatment of nanoparticles needs to be performed during the synthesis process to avoid agglomeration and oxidation of the particles.

This chapter introduces basic concepts of the synthesis processes used for the fabrication of metal nanoparticles and related materials.

7.2 Nanoparticles and Related Materials for Electronic Packaging

Several nanomaterials, including metals, ceramics, and carbon-based materials, are promising candidates as the main components of nanopackaging materials. Typical nanomaterials used in nanopackaging applications are summarized in Table 7.1.

Metal nanoparticles for electronic packaging are briefly divided into two categories: noble metals [6] and lead-free solders (Sn-based alloys) [7]. The nanoparticles are used for preparing wires and electrodes and for interconnecting materials.

In addition, some functional nanoparticles have been synthesized. For example, ferromagnetic FePt nanoparticles [8] are promising candidates for the development of advanced high-density magnetic storage media.

A. Metals	
Noble metals (Au, Ag, Cu, etc.)	Nanoparticles, nanorods, nanowires
Solders (lead-free solders)	Nanoparticles
Magnetic materials (FePt, etc.)	Nanoparticles
B. Ceramics	
Electrical conductors (ITO, etc.)	Nanoparticles
Dielectrics (BaTiO ₃ , etc.)	Nanoparticles
Semiconductors (TiO ₂ , etc.)	Nanoparticles, nanotubes, nanowires
Magnetic materials (Fe ₃ O ₄ , etc.)	Nanoparticles
C. Carbon-based materials	
CNTs and related materials	Nanotubes, nanofibers, nanocoils, etc.
Graphene	Nanoplates, nanosheets
Nano-diamond	Nanoparticles

 Table 7.1
 Typical nanomaterials for nanopackaging

7.3 Metal Nanoparticle Fabrication Methods

7.3.1 Breakdown and Buildup Methods

In general, metal nanoparticles can be fabricated by breakdown or buildup methods, as depicted in Fig. 7.1. The breakdown method is a technique whereby the bulk metal is crushed by mechanical grinding (MG) or mechanical milling (MM). Even though it is a simple technique, it is difficult to control the particle size at the nanometer scale using the breakdown method. Moreover, several problems could occur during vigorous and long-term milling. Contamination of the metal particles from grinding or milling media needs to be avoided during these processes. This technique is unsuitable for soft metals because these metals exhibit extensive plastic deformation during milling.

In contrast, the buildup method involves the assembly of metal atoms and includes many variations. This method is roughly divided into chemical and physical processes. These buildup processes for the preparation of metal nanoparticles are briefly introduced here.

7.3.2 Nucleation Theories for Nanoparticle Fabrication Using Buildup Methods

7.3.2.1 Driving Force for Nucleation

In the case of the buildup methods, nanoparticles are always obtained through nucleation and subsequent nanocrystal growth. The driving forces of a transition



Fig. 7.1 Concepts of breakdown and buildup methods for the fabrication of nanoparticles

from metastable to stable state such as the nucleation process are the chemical potential difference ($\Delta \mu$) between these states. $\Delta \mu$ is proportional to supersaturation (*s*):

$$s = (C - C_{eq})/C_{eq} \tag{7.1}$$

where C and C_{eq} represent actual concentration and solubility (equilibrium concentration), respectively. During synthesis of nanoparticles using the buildup methods, the nucleation always occur in a supersaturation state.

7.3.2.2 Thermodynamic Description of Nucleation: Classical Nucleation Theory

The formation free energy of the clusters (nuclei) of the new equilibrium phase (ΔG) is determined by two different contributions including volume and surface contributions [9–12]. When the nucleus is assumed to be a sphere of radius *r*, ΔG during homogeneous nucleation is represented by

$$\Delta G = -\left(4\pi r^3/3\right)\Delta g_v + 4\pi r^2\sigma \tag{7.2}$$

where Δg_{ν} and σ are the difference in free energy per unit volume and interface free energy (interface tension) between the nucleus and surroundings.

Figure 7.2 schematically shows the relationship between ΔG and r. The critical radius of nucleus (r^*) is determined by setting $d(\Delta G)/dr$ to zero, so

$$r^* = 2\sigma / \Delta g_v \tag{7.3}$$

Clusters with radii above r^* can grow spontaneously to form nanoparticles.

By using of the energy barrier for nucleation (ΔG^*), theoretical description (classical nucleation theory) for the steady-state nucleation rate is represented by





Fig. 7.3 Variation in shape of a droplet depending on the interfacial free energy with substrate

$$J = \beta^* Z C_0 exp(-\Delta G^*/kT) \tag{7.4}$$

where Z, C_0 , k, and T are the Zeldovich factor, atomic fraction of site accessible to the cluster, Boltzmann's constant, and temperature, respectively. Since the Zeldovich factor indicates the probability of crystal formation from a critical cluster (cluster fluctuations around the critical radius), the term $ZC_0 \exp(-\Delta G^*/kT)$ corresponds to the number of critical clusters that can continuously grow, and β^* is the growth rate of a critical cluster.

Because ΔG^* is much lower at a substrate surface, heterogeneous nucleation (nucleation at a surface) is more easily induced than homogeneous nucleation [9–11]. Figure 7.3 schematically shows the contact angle of a droplet (θ). Heterogeneous nucleation can occur in the case of (b) and (c) in Fig. 7.3. The effect of the contact angle (balance of surface free energies and interface free energy) on heterogeneous nucleation and film growth will be discussed in Sect. 7.4.2.

7.3.2.3 Atomistic Modeling for Describing Nucleation Rate

In the classical nucleation theory that is based on thermodynamic analysis, the free energy of cluster formation is expressed using macroscopic material parameters.

In contrast, the atomistic theory describes associations of atoms to form clusters in terms of the binding energy of atoms [10, 11, 13]. It is assumed that an atom which forms part of a cluster is stabilized by its binding energy. The number of critical clusters to grow is estimated by a numerical analysis based on statistical mechanics.

Although the atomistic approach is different from the classical nucleation theory in the description of the nucleation process, relationships between the two theories have been discussed [10, 11].

7.4 Physical Processes

7.4.1 Nanoparticle Synthesis Through Homogeneous Nucleation

7.4.1.1 Gas Condensation and Atomization Processes

Physical processes consist of reactions that involve solidification from a gas or liquid phase to obtain metal particles (Fig. 7.4).



Fig. 7.4 Schematic illustrations of gas condensation and atomization methods

The gas condensation method [14] is a typical fabrication method for metal nanoparticles using a physical process. In the gas condensation method, starting materials, such as metallic, inorganic, and organometallic compounds, are vaporized by thermal evaporation sources, such as Joule heated refractory crucibles, electron beam evaporation devices under vacuum, or an inert gas atmosphere. The metallic cluster is formed in the vicinity of the source by homogeneous nucleation in the gas phase. In this method, the particle size is changed depending on the residence time of the particles in the gas phase, which is influenced by the gas pressure and the type of inert gas, evaporation rate, and vapor pressure. In general, the average particle size of the nanoparticles synthesized by this process tends to increase with increasing gas pressure and vapor pressure.

Another technique is the atomization method [15], during which the molten metal is rapidly cooled into droplets. Although this process is commonly used for industrial mass production, metal particles with micrometer or sub-micrometer sizes (not nanoparticles) are usually obtained.

7.4.1.2 Thermal Plasma Processes

Thermal plasmas that are generated at atmospheric pressure (or close to atmospheric pressure) can provide an effective reaction field for the synthesis of metal and ceramic nanoparticles [16–21]. The process of the thermal plasma synthesis is illustrated in Fig. 7.5. Precursors of the nanoparticles are vaporized in the thermal plasma. The vapor containing the precursors is subsequently quenched in the tail of the plasma to obtain a supersaturated state. During the quenching process, homogeneous nucleation occurs in the downstream vapor flow resulting in the growth of nanoparticles.



The nanoparticles synthesized during this process are easily collected using a filter or directly deposited on a substrate. Using this process, nanoparticles and nanostructured films can effectively be obtained without any surfactant molecules.

7.4.2 Nanostructure Formation on Substrates

When a material vapor directly deposits on a substrate, nucleation (heterogeneous nucleation) occurs to induce film growth. The film growth can be categorized into three modes, including Frank–van der Merwe (layer-by-layer growth), Volmer–Weber (island growth), and Stranski–Krastanov (layer-by-layer plus island growth) modes [22], as shown in Fig. 7.6.

The substrate temperature (T_s) is assumed to be high enough to obtain $\Lambda >> a$, where Λ and a are the surface diffusion length and the interatomic spacing of the deposited atoms. The Frank–van der Merwe mode is promoted under the conditions defined by Eq. (7.5).

$$\gamma_f + \gamma_i < \gamma_s \tag{7.5}$$

where γ_f and γ_s are the surface free energy (surface tension) for the free surfaces of film and substrate, respectively. γ_i indicates the interface free energy (interface tension) between film and substrate. This mode of thin film growth is used for preparing many types of layered semiconductor devices and for developing novel nanodevices [23–25].

In contrast, the Volmer–Weber mode occurs under the conditions of Eq. (7.6).

$$\gamma_f + \gamma_i > \gamma_s \tag{7.6}$$

In this case, the total surface energy is minimized by the island growth. By using this growth mode, discontinuous metal thin film devices can be prepared [26–28]. Although the films are composed of discontinuous metal islands, they can exhibit significant electrical conductivity. Therefore, these films are examined to apply for several sensors (e.g., strain gauges, gas sensors), photovoltaic modules, and optical/electrical switches. Fabrication methods must be developed to reproducibly control the microstructure composed of discontinuous islands to establish practical applications of these devices.

Conversely, the occurrence of the Stranski–Krastanov mode is associated with epitaxy [22, 29]. In this case, the growth mode is changed from layer-by-layer to island growth after monolayer formation. The Stranski–Krastanov mode is observed in systems containing a film/substrate interface that has a small interface free energy and large lattice mismatch. Because a thicker layer provides large strain energy, the growth mode is changed from layer-by-layer to island growth to lower the total energy of the systems.

Vapor deposition processes are one of the effective methods for the preparation of semiconductor nanodevices. For example, self-organization of quantum dots can be achieved using crystal growth by the Stranski–Krastanov mode [30]. Molecular beam epitaxy (MBE) deposition of InAs on GaAs or InP substrates has been well-studied for the preparation of self-organized quantum dots of InAs. Although the strain energy owing to lattice mismatch between the film and substrate is the driving force for the island growth, the strain can also induce the formation of dislocations that decrease the crystallinity of the islands. To control the particle size and crystallinity of the islands during the crystal growth, a strain-controlled growth process was developed [31]. Quantum dots are expected to be one of the key technologies used for the preparation of nanoelectronic devices [32].

7.5 Chemical Processes

7.5.1 Nanoparticle Synthesis by Reduction of Metal Ions

Although chemical processes include many different buildup techniques, these processes consist of a reduction reaction of the metal ions in a solution using



reducing agents and/or reducing energies such as heating and ultrasonic irradiation. The reaction mechanism for synthesis of metal nanoparticles is explained by the LaMer model [33]. As shown in Fig. 7.7, self-nucleation and seed formation occur during a supersaturation state. The particles size and size distribution of the nanoparticles can be controlled by optimizing the reaction rate during the supersaturation state.

When metal salts are used as the source for the fabrication of nanoparticles, the selection of the reducing agents is most important. Mild reducing agents are more suitable for the fabrication of nanoparticles because the reduction rate is slowed and it is easy to control the particle size. The particles tend to grow large when strong reducing agents (such as hydrazine) are used. In this case, the reaction rate is too fast to control the nanoparticle size.

In addition, the molecular structure of the metal source influences the particle size and the size distribution of the nanoparticles obtained after reduction. For example, amine-related compounds and organic acids (e.g., citric acid) act not only as the reducing agent but also as surfactants of nanoparticles.

To facilitate the reduction of metal ions in various solutions, the addition of reducing energy is also effective. Novel processes using ultrasound and microwave irradiation have been developed in addition to conventional heating.

Tables 7.2 and 7.3 show typical reducing agents and energy used and popular metal sources, respectively, for metal nanoparticle fabrication.

7.5.2 Thermal Decomposition of Organometallic Compounds

In addition to the reduction process of metal ions in various solutions, direct transformation processes of organometallic compounds have recently been reported for the synthesis of metal nanoparticles. Nakamoto et al. [34, 35] successfully synthesized several pure metal and alloy nanoparticles through the direct thermal

Reducing materials	Alcohols, aldehydes, sugars
	Hydroxy acids, hydroxylamines
	Thiols, NaBH ₄ , B ₂ H ₆ , H ₂ , Sn ²⁺ , Co ²⁺
	etc.
Reducing energy (irradiation)	Heating
	Microwave
	Ultrasound
	Photo (ultraviolet, etc.)
	etc.

Table 7.2 Typical reducing agents and reducing energies for metal nanoparticle fabrication

 Table 7.3 Typical metal sources for metal nanoparticle fabrication

Metal	Bulk, flake, powder, etc.
Metal salt	Nitrates, chlorides, hydrosulfates, cyanides
Organometal complex	Carbonyls, fatty acid complexes, alkoxides

decomposition of fatty acid-metal complexes. Kurihara et al. [36] also reported the synthesis of Ag nanoparticles by thermal decomposition of oxalate-bridging Ag oleylamine complexes. Ag nanoparticles prepared using this process showed excellent sinterability at a low temperature after they were printed on a substrate [37].

Furthermore, organometallic compounds such as β -ketocarboxylates can be used directly as inks for inkjet printing. After printing the organometallic inks, Ag wires and electrodes are obtained by curing at 100–150 °C in air [38].

7.5.3 Novel Processing Routes for Eco-fabrication

The biggest problems in industrial manufacturing are cost and environmental impact, which are closely linked. Figure 7.8 shows the relationship between cost and environmental impact on the preparation of metal nanoparticles [39, 40].

It is easy to fabricate high-purity nanoparticles using the physical method because the production proceeds in an inert gas. However, high-temperature heating and a large-scale chamber filled with an inert gas are necessary for mass production, and the yield is not very high. Therefore, a large initial cost and high running costs are required.

In contrast, the chemical method provides cost-effective fabrication of nanoparticles because spontaneous chemical reactions are used for synthesizing the particles. However, there are challenges related to the use of the raw materials (metal source and reduction agent). When a metal salt is used as the metal source, counter anions including NO^{3-} , SO_4^{2-} , and CI^- remain in the solution used for synthesizing the metal nanoparticles. Washing the nanoparticles is necessary to remove these anions after the synthesis process. In addition, more than 80 wt% of the organometallic compounds might become organic waste when they are used as



Fig. 7.8 Relationship between cost and environmental impact in industrial manufacturing of metal nanoparticles

the metal source for a reduction process of metal ions. Therefore, it is necessary to remove this waste after the synthesis process. The cost of fabricating nanoparticles using the chemical processes increases because of the posttreatment necessary for the purification of metal nanoparticles.

From the industrial manufacturing viewpoint, a well-balanced fabrication methodology is needed to control the cost and to protect the environment. In addition, the coexistence of high performance and low environmental impact will become increasingly important in nanotechnologies including nanopackaging. However, it is difficult to manage both the cost and the environmental impact using these methods. Therefore, innovative fabrication design is required to solve these problems.

Examples of metal nanoparticle fabrication methods that achieve both ecological and economic goals are introduced below.

7.5.3.1 Liquid–Solid Sonochemical Reaction

Hayashi et al. developed a new metal nanoparticle synthesis method using an ultrasonic cleaner as a reactor and a metal oxide (M_xO_y) and alcohol (C_xH_yOH) as raw materials [41]. Because the metal oxide does not dissolve in alcohol, the liquid–solid (alcohol–metal oxide) phase is ultrasonically agitated.

When a solid substance is subjected to pyrolytic treatment, the raw material is converted into a fine powder [42, 43]. In particular, noble metal oxides are simply decomposed by heating in air, i.e., without the need for a strongly reducing atmosphere [44]. This reduction is clean and ecological because noble metal oxides are nearly atoxic materials and only generate O_2 during decomposition. The starting materials are noble metal oxides and ethanol (EtOH), which are low emission (LE) materials.

An ultrasonic cleaner is an inexpensive domestic appliance, and metal oxides and alcohols are generally inexpensive and nontoxic. Ultrasonic processing as a chemical process is called a sonochemical process. Ultrasonic irradiation differs from conventional energy sources in duration, pressure, and energy per molecule and is unique in the interaction between energy and matter. The chemical effects of ultrasound do not come from direct interaction with a molecular species. Instead, they are derived principally from acoustic cavitation, which can produce temperatures as high as those on the surface of the sun and pressures as great as those at the bottom of the ocean [45]. Such a reaction field can be achieved with a domestic electronic ultrasonic cleaner.

We have synthesized noble metal nanoparticles by ultrasound in a liquid–solid (EtOH–noble metal oxide) slurry. The synthesis technique is very simple. EtOH and the noble metal oxide powder are simply placed into a beaker and irradiated by ultrasound (Fig. 7.9). When the liquid–solid slurry is irradiated by ultrasound, it reduces to metal nanoparticles, as described by Eq. (7.7):

$$M_x O_y \xrightarrow{\quad \text{in EtOH }))) \ R.T.} Metal \ nanoparticle + O_2 \uparrow + \Delta G$$
 (7.7)

where ΔG is the change in Gibbs free energy of this reaction. Ultrasonic irradiation is the key process in this reaction. Cavitation in a liquid occurs owing to the stresses induced in the liquid by the passing of a sound wave through the liquid [46– 48]. These bubbles (that are formed by the cavitation) are subjected to the stresses induced by the sound waves. The bubbles are filled with vapor and gas, and bubble





metal oxide particles in EtOH



Ultrasonic irradation
implosions occur. These implosions are the remarkable part of the sonochemical process. Each of these imploding bubbles can be seen as a high-temperature hot spot with a pressure of several hundred atmospheres. A hot spot reaction is considered to represent direct reduction, with the reduction of a metal oxide induced by the hot spots formed from ultrasonic cavitation and alcohol. EtOH is also important in this reduction. Ultrasonic reduction is accelerated by alcohol [49] and protects the metals from re-oxidization. The nucleation of the metal occurs at the hot spot in solution, followed by the growth and immobilization of the noble metal particles.

Figure 7.10 shows a transmission electron microscope (TEM) image of Ag nanoparticles synthesized by this sonochemical process. In this case, polyvinylpyrrolidone (PVP) was used as a surfactant for the nanoparticles. The particle size of the nanoparticles was changed by the PVP concentration. UV absorption peaks were observed at approximately 400 nm. These absorption bands correspond to the surface plasma resonance absorption of nanometer-sized Ag particles. The absorption peaks were shifted by changes in the Ag particle size.



Fig. 7.10 TEM images of Ag nanoparticle synthesized with PVP surfactant using a liquid-solid sonochemical process

The fabrication of nanoparticles by combining low-cost and low environmental impact can be achieved using such a synthesis method.

This ultrasonic irradiation process can be applied to the synthesis of a wide variety of noble metal nanoparticles. However, a long reaction time is needed to synthesize some metal nanoparticles such as Cu and Pt. To synthesize these nanoparticles, microwaves are irradiated into the liquid–solid reaction system in addition to the ultrasonic irradiation. Figure 7.11 shows a TEM image of Cu nanoparticles synthesized using this method. These Cu nanoparticles can be used for additive printing of electric wires and electrodes. In addition, Fig. 7.12 shows a TEM image of Pt nanoparticles synthesized without any surfactant. These Pt nanoparticles are currently commercialized to use as catalysts [50].



uiu O

Fig. 7.11 Scanning electron microscope (SEM) image of Cu nanoparticles synthesized by a liquid– solid sonochemical process assisted with microwave irradiation

Fig. 7.12 TEM image of Pt nanoparticles synthesized using a liquid–solid sonochemical process assisted with microwave irradiation

7.5.4 Shape-Controlled Synthesis by Chemical Processes

7.5.4.1 Polyol Method

The polyol method is one of the chemical processes used to synthesize sub-micrometer- or nanometer-sized metal particles originally developed by Fievet et al. [51]. In this process, metal ions are reduced in a polyol solvent such as ethylene glycol (EG) at a suitable reaction temperature. Control of the particle size and shape accomplished during polvol is the process bv the introduction of polyvinylpyrrolidone (PVP) as a surfactant and metal salts such as NaCl, CuCl₂, CuCl, and FeCl₃ [52].

Metal nanoparticles are obtained in the polyol solvent through the following three steps: nucleation, seed evolution, and nanocrystal growth. During a supersaturation state, the atoms aggregate to form small clusters (nuclei). Then, the clusters grow to an energetically stable structure (seeds). Several types of seeds including single crystal, singly twinned, and multiple twinned and plate with stacking faults can be formed during the polyol process.

The desired type of seed can be extracted selectively by controlling the oxidative etching reaction [52]. Because synthesis is performed in air, oxygen dissolves into the polyol solution to be a strong etchant for the seeds. The oxidative etching reaction can be controlled by using additives. For example, single crystal seeds remain during the reduction of the Ag ions when oxygen and Cl⁻ ions coexist in the polyol solution. In contrast, multiple twinned (fivefold twinned) Ag seeds can be selectively obtained when a redox pair such as Fe^{III/II} and Cu^{II/I} is present in the polyol solution. To accomplish the selective synthesis of seeds, metal salts are effectively used as the additives in the polyol method.

In addition, capping molecules such as PVP play an important role to achieve shape-controlled synthesis of metal nanoparticles and related nanomaterials. Chemisorption of the capping molecules on specific facets of the nanocrystals in the polyol solution results in anisotropic growth of the nanocrystals [52]. In the case of reduction of Ag ions, PVP molecules exhibit selective chemisorption on {100} facets of Ag nanocrystals to suppress crystal growth in this direction. Therefore, Ag atoms tend to deposit on {111} facets during the reaction process to promote anisotropic elongation of the {100} direction to form Ag nanowires in the polyol solution, as shown in Fig. 7.13.

In addition, the reaction kinetics need to be controlled carefully for shapecontrolled synthesis of metal nanoparticles and related nanomaterials. For example, Jiu et al. [53] successfully synthesized very long Ag nanowires (more than 60 μ m long) with a uniform diameter of 60 nm using a single-step polyol process by controlling the reaction conditions including the reaction temperature and stirring speed, as shown in Fig. 7.14a. The very long nanowires were successfully applied to the preparation of flexible transparent conductive films (Fig. 7.14b) [54].



Fig. 7.14 SEM images of (**a**) very long Ag nanowires synthesized by a polyol process and (**b**) transparent conductive films prepared with the Ag nanowires

7.5.4.2 Template Method

Several self-organized structures (templates) of organic molecules can be used as nanoreactors to control the size and shape of the nanoparticles.

A useful template is reverse micelles [55, 56] using amphiphilic molecules that have both hydrophilic and hydrophobic functional groups as surfactants. When amphiphilic molecules are added into a solvent, they form a self-organized structure, namely, micelles, above a critical concentration (CMC, critical micelle concentration). By using this phenomenon, oil-in-water (o/w) or water-in-oil (w/o) microemulsions can be stabilized by several amphiphilic molecules (surfactants). The stabilized w/o microemulsions are reverse micelles. To form reverse micelles, sodium bis-sulfosuccinate (Na(AOT)) is often used as a surfactant.

Because metal nanoparticles and related materials are usually synthesized in water or hydrophilic solvents, the size- and shape-controlled synthesis of nanoparticles can be achieved by using the aqueous core of reverse micelles as nanoreactors.

There are two synthesis schemes for the reverse micelle method. Metal nanoparticles can be obtained by the reactions between two different microemulsions containing metal ions and reducing agents. The reducing agents are injected into the micelles containing metal ions by intermicellar exchange to form metal nanoparticles. The other reaction scheme is the single emulsion method. Microemulsions containing metal ions in their aqueous core are directly reduced using reducing agents or physical energy. During the synthesis of metal nanoparticles using reverse micelles, the particle size is controlled by several conditions such as the type of solvent and surfactant, the concentration of reagents, and the molar ratio between the water and the surfactant.

Shape-controlled synthesis of metal nanoparticles is achieved by controlling the shape of reverse micelles [57]. The micelles can provide several shaped templates, including spheres, cylinders, planes, and lamellar phases. In addition, the growth direction of the nanoparticles is effectively controlled by selective chemisorption of ions and molecules on the facets of nanocrystals.

To control the shape of the templates for nanoparticle syntheses, Yin and Bathe et al. [58] have proposed the use DNA nano-molds. Many template shapes can be designed by self-organization of DNA molecules. After seeds of metal nanoparticles are fixed in the DNA molds, nanocrystal growth is induced to obtain nanoparticles.

7.5.4.3 Shape-Controlled Eco-fabrication of Nanomaterials

Recently, Hayashi et al. [59] reported eco-fabrication of Ag nanobeadwires. In this process, needle-shaped Ag carboxylates were synthesized as precursors using a liquid–solid reaction in an ethanol solution containing carboxylic acids under ultrasound and microwave irradiation. The morphology of the carboxylate precursors could be controlled by the concentration of the reagents and the ultrasound irradiation conditions. By optimizing the reaction conditions, precursors with a high-aspect ratio (diameter, a few hundred nanometers; length, a few micrometers) were successfully obtained, as shown in Fig. 7.15a.

Subsequently, the carboxylate precursors were easily reduced using hydrazine gas or Ar plasma irradiation to form Ag nanobeadwires (Fig. 7.15b). This precursor reduction process can be applied to mass fabrication of a transparent conductive film on various substrates including organic polymers such as polyethylene terephthalate (PET) and polycarbonate (PC).



Fig. 7.15 SEM images of (a) needle-shaped Ag carboxylate precursors synthesized by a sonochemical process and (b) Ag nanobeadwires obtained after reduction using hydrazine gas

7.6 Utilization of Metal Nanoparticles for Preparing Electric Wires, Electrodes, and Interconnects

7.6.1 Nanoparticle Inks and Pastes for Printing Processes

Metal nanoparticles are usually protected by surfactants in printing inks and pastes used for electronic packaging applications. The surfactants are necessary to maintain high dispersivity of nanoparticles in the inks and pastes. By contrast, the surfactants inhibit the formation of interparticle contacts that can create electrical conduction paths. The surfactants must be removed easily from the particle surface during curing after the inks and pastes are printed on a substrate. Because the surfactants need to have these two exclusive properties, the selection of appropriate surfactants is a key for preparing novel nanoparticle inks and pastes. The fundamental ideas behind the selection of surfactants for metal nanoparticles are briefly introduced in this section.

7.6.1.1 Dispersion of Nanoparticles

A large amount of van der Waals attractive forces and cohesive energy are generated between nanoparticles in colloids [60]. In addition, surface diffusion of constitutional atoms on nanoparticles is faster than those on microparticles. Therefore, nanoparticles strongly tend to aggregate and coalesce in their colloids. To obtain an individual dispersion of nanoparticles, surface modification using appropriate surfactants is needed during the preparation process.

The strategy used to achieve a stable dispersion of nanoparticles is different depending on the dielectric constant of the solvent (dispersant). When the solvent has a large dielectric constant, electrostatic repulsion can be effectively induced between the nanoparticles. In contrast, repulsive forces based on steric hindrance effects of the surfactant are predominantly generated between the nanoparticles in solvents that have a low dielectric constant because a large surface charge is not induced on the particles.

Although surfactants for metal nanoparticles are divided into low-molecularweight compounds and polymers, polar functional groups such as amino, carboxylic, mercapto, and hydroxyl groups commonly exhibit attractive interactions with the surface of nanoparticles.

When water is used as the solvent, the surface charge of the nanoparticles can be controlled by changing the pH of the solvent and the electrolyte concentration. In this case, the dispersion state of nanoparticles can be discussed using Derjaguin–Landau–Verwey–Overbeek (DLVO) theory [61] because interparticle interactions are determined by competing van der Waals (attractive) forces and electrostatic (repulsive) forces (electric double layer forces), as shown in Fig. 7.16.

In contrast, repulsive interactions between nanoparticles are promoted by the steric hindrance effects of surfactant molecules in solvents that have a low dielectric





constant such as hydrocarbons. To obtain a large repulsive force that overcomes the van der Waals (attractive) forces, the molecular chain length of the alkyl group of the surfactant is an important factor. A stable dispersion of metal nanoparticles is generally obtained when the length of the alkyl chain is above C_{12} .

7.6.1.2 Curing Behavior of Nanoparticle Inks and Pastes

Noble Metal Nanoparticle Inks and Pastes

After printing with inks and pastes that contain noble metal nanoparticles, the specimen is cured to induce low-temperature sintering of the nanoparticles. Although metal nanoparticles are potentially sintered even at ambient temperature [62], their sintering temperature is limited by the existence of surfactants.

To decompose the surfactants and induce low-temperature sintering, several curing processes including photo-, laser, and plasma irradiation have been examined in addition to a normal heating process. In addition, low-temperature sintering can be induced by a chemical treatment to wash the surfactants away from the surface of the nanoparticles [63].

When surfactants containing long alkyl chains (above C_{12}) are used for metal nanoparticles, they form a very stable molecular layer on the particles owing to the molecular interaction between the alkyl chains [64] (Fig. 7.17). Although this molecular layer is suitable to obtain a stable dispersion of nanoparticles, the decomposition temperature of the surfactants significantly increases. Therefore, molecular design of the surfactant is the key issue for the development of advanced metal nanoparticle inks and pastes.

A large number of studies have been conducted for the molecular design of surfactants for metal nanoparticles. As a result, various types of surfactants have been developed. For example, Kanehara [65] recently proposed the use of cyclic π -conjugated molecules such as phthalocyanine as a surfactant for noble metal



Fig. 7.17 TEM image of Ag nanoparticles and model of surfactant molecular layer formed on metal nanoparticles

nanoparticles. By using Au and Ag nanoparticles adsorbed with phthalocyanine, nanoparticle inks that exhibit electrical conductivity at low temperatures (even at ambient temperature) have been developed.

Nanosolder Pastes

Nanometer-sized lead-free solders (nanosolders) such as Sn-based alloys have been prepared using chemical and physical processes [7]. Nanoparticles from base metals such as Sn easily form an oxide scale on the surface. Although solder nanoparticles exhibit a lower melting temperature than microparticles, soldering is often interrupted by the oxide scale on the solder nanoparticles. To reduce the oxide scale, a carboxylic acid surfactant and several fluxing agents have been used to prepare nanosolder pastes. Improving solderability is a critical problem for establishing practical applications for nanosolder pastes.

7.6.2 Direct Deposition of Metal Nanoparticles

In addition to additive printing processes, such as inkjet and screen printing using nanoparticle inks and pastes, the direct deposition of nanoparticles to substrates can be an alternative manufacturing process for the formation of electric wires and electrodes. For example, the aerosol jet printing method has attracted interest in the electronic packaging field, as it can be potentially applied to three-dimensional (3D) interconnects as well as two-dimensional (2D) wiring [66, 67]. Currently, metal aerosol particles are prepared using a pneumatic or an ultrasonic atomizer from metal nanoparticle inks in a commercialized printer.

Modern aerosol jet printers are useful tools for additive manufacturing of electronic devices. However, it would be a more powerful tool if the metal aerosol particles synthesized in the gas phase could be deposited directly on substrates. Direct deposition of spark-generated metal aerosol particles (Ag, Pd, Pt, Au, and Cu particles) has been reported [68–70]. In contrast, these particles were used as catalysts for subsequent electroless Ag plating. To achieve direct formation of electric wires and electrodes using only the deposition process at atmospheric pressure, large-scale synthesis of metal nanoparticles in the gas phase needs to be conducted to obtain vapors with a high particle concentration.

Thermal plasma processes [16, 17] have the potential to be used for the largescale synthesis of metal nanoparticles with no surfactants at atmospheric pressure, as discussed in Sect. 7.4.1. The deposition processes of metal nanoparticles generated by thermal plasmas, including direct thermal chemical vapor deposition (CVD), indirect thermal CVD, and plasma spraying, have been mainly applied to the fabrication of ceramic films [16]. Large-scale synthesis of metal particles using advanced reactors such as an advanced RF-ICP (radio-frequency inductively coupled plasma) reactor [17] could be used to realize direct plasma deposition to form wires and electrodes in the future.

7.7 Summary

Nanopackaging will provide a breakthrough in the evolution of electronic devices in nanoelectronics. However, many problems remain to be solved before nanopackaging technology can be established. It is essential to develop material technologies for the preparation of packaging materials based on nanomaterials. Cost-effective mass production of nanomaterials such as nanoparticles and nanowires using green processes is necessary. To establish material technology for nanopackaging, interdisciplinary approaches extending into physics and chemistry will be important.

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Chapter 8 Nanoparticle-Based High-*k* Dielectric Composites: Opportunities and Challenges



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8.1 Introduction

The ever-increasing demands of miniaturization, increased functionality, better performance, and low cost for microelectronic products and packaging have been the driving forces for new and unique solutions in system integration, such as system on chip (SOC) and system in package (SiP). Despite the high level of integration, the number of discrete passive components (resistors, capacitors, or inductors) remains very high. In a typical microelectronic product, about 80% of the electronic components are passive components that are unable to add gain or perform switching functions in circuit performance. But these surface-mounted discrete components occupy over 40% of the printed circuit/wiring board (PCB/PWB) surface area and account for up to 30% of solder joints and up to 90% of the component placements required in the manufacturing process. Embedded passives, an alternative to discrete passives, can address these issues associated with discrete parts, including substrate board space, cost, handling, assembly time, and yield. Figure 8.1 schematically shows an example of realization of embedded passive technology by integrating resistor and capacitor films into the laminate substrates [1, 2]. One can add that

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Fig. 8.1 Schematic illustration of embedded passives integrated into the laminate substrate

similar solutions are possible for multi-chip modules (MCMs) based on thin- or thick-film technologies.

By removing these discrete passive components from the substrate surface and embedding them into the inner layers of substrate board, embedded passives can not only provide the advantage of size and weight reduction but also have many other benefits such as increased reliability, improved performance, and reduced cost.

In recent years, embedded passive technology has been commercialized for electronic packages in a limited manner due to materials and process issues. Therefore, to enable wider application of this technology, it is necessary to develop materials that satisfy the requirements of fabrication as well as electrical and mechanical performances [3, 4]. High dielectric constant (k) and low dielectric loss are two most important prerequisites for these materials before any real applications are possible.

In this chapter, research and development on high-k polymer and cermet composites for embedded capacitor applications are reviewed and discussed. More specifically, current research efforts toward achieving high-k and low dielectric loss nanoparticle-based dielectric composites are presented. Properties and the long-term stability of capacitors built into PCBs are described. High-k nanocrystalline thin-film layers are also presented in this chapter. Brief descriptions of thick-film and ceramic high-k material substrates are included too.

8.2 Dielectric Mechanisms

8.2.1 Capacitance, Dielectric Constant, and Polarization

Capacitance (*C*) is used as the measure of how much electric charge can be stored in a capacitor. The relationship between capacitance C of a planar sandwich-type capacitor with uniform dielectric constant $k = \varepsilon_r$ is given by the following equation:



$$C = \frac{\varepsilon_0 \varepsilon_r A}{t} \tag{8.1}$$

where ε_0 is the permittivity of free space (8.854 × 10⁻¹² F/m), A is the area of the electrical conductor, t is the thickness of the dielectric layer, and ε_r is the relative dielectric constant (relative electric permittivity) of the dielectric layer. It is evident that the larger the dielectric constant, the larger the capacitance which can be realized in a given space. Therefore, materials of high dielectric constant are favored in practical design of embedded passives for miniaturization.

The ability of the dielectric materials to store energy is attributed to the polarization, i.e., electric field-induced separation and alignment of the electric charges. There are several molecular mechanisms associated with this polarization (see Fig. 8.2). Ideally, the dielectric constant should be constant with regard to frequency, temperature, voltage, and time. However, each polarization mechanism has a characteristic relaxation frequency. Therefore, *k* values of most of the materials show a dependence on the frequency because the slower mechanism fails to respond and contribute to the dielectric storage when the frequency becomes larger. The *k* values of dielectric materials can also vary with temperature, bias, impurity, and crystal structure to different extents according to materials types [1, 5].

8.2.2 Dielectric Loss

Dielectric loss is a measure of energy loss in the dielectric during AC operation, which is a material property and does not depend on the geometry of the capacitor. Dielectric loss is usually expressed as the loss tangent/factor (tan δ) or dissipation factor (*Df*), defined as

$$\tan \delta = \frac{\varepsilon''}{\varepsilon'} + \frac{\sigma}{2\pi f \varepsilon'}$$
(8.2)

where ε' , ε'' , and σ are the real and imaginary parts of the electric permittivity and the electrical conductivity of the materials, respectively, and *f* is the frequency.

In general, dielectric loss results from distortional, dipolar, interfacial, and conduction loss. Distortional loss is related to the electronic and ionic polarization mechanisms. Interfacial loss originates from the excessive polarized interface induced by the fillers and specifically the movement or rotation of the atoms or molecules in an alternating electric field. Conduction loss is attributed to the dc electrical conductivity of the materials, representing the flow of actual charge through the dielectric materials.

The energy dissipated in a dielectric material, *W*, is proportional to the dielectric loss tangent and can be determined by the following equation:

$$W \approx \pi \varepsilon' \xi^2 f \tan \delta \tag{8.3}$$

where ξ is the electric field strength [6]. Therefore, a low dielectric loss is preferred in order to reduce the energy dissipation and signal losses, particularly for high frequency applications. Generally, a dissipation factor under 0.1% is considered to be quite low and 5% is high [1]. A very low dissipation factor is desired for RF applications to avoid signal losses, but much higher values can be tolerated for energy storage applications such as decoupling.

8.3 Materials Options for High-*k* Dielectrics

Dielectric theory suggests that high dielectric constant and low dielectric loss are the two most important parameters for dielectric materials to realize embedded capacitor applications. As such, to meet the stringent materials requirements, considerable attention has been devoted to the research and development of candidate high-k materials.

8.3.1 Ferroelectric Ceramic Materials

In the beginning, ferroelectric ceramic materials, including barium titanate (BaTiO₃), BaSrTiO₃ (barium strontium titanate), PbZrTiO₃ (lead zirconate titanate),

etc., have been used as dielectric materials for decoupling capacitors because of the high k – up to thousands for this type of materials [1, 7]. However, the very high processing temperature (>600 °C) required for sintering is unsuitable for the embedded capacitor applications in the low-cost organic PCB industry.

8.3.2 Ferroelectric Ceramic/Polymer Composites

Ferroelectric ceramic-polymer composites with high k have also been actively explored as major material candidates. The methodology of this approach is to combine the advantages from the polymers, which meet the requirements for the low-cost organic substrate process, i.e., low-temperature processibility, mechanical flexibility, and low cost, with the advantages from the ferroelectric ceramic fillers, such as desirable dielectric properties [3, 4, 8-14]. However, some challenging issues in these polymer composites for high-k applications have been addressed, such as limited dielectric constants, low adhesion strength, and poor processibility. A typical connectivity of polymer-ceramic composite is 0–3 composite, which indicates that ceramic fillers are dispersed without continuity in a three-dimensional connected continuous polymer matrix. Most of the k values of polymer-ceramic composites developed to date are below 100 at room temperature due to the low-kpolymer matrix (usually in the range of 2-6). By employing a relatively high-k polymer matrix, the k values of polymer-ceramic composites can be effectively enhanced because the polymer matrix k has a very strong influence on the k of the final composites [4, 12]. For instance, poly(vinylidene fluoride-trifluoroethylene) (P (VDF–TrFE)) copolymer, a class of relaxor ferroelectric, can have a relatively high room temperature k (~40) after irradiation treatment [15]. Bai et al. prepared Pb(Mg_{1/} $_{3}Nb_{2/3}O_{3}-PbTiO_{3}/P(VDF-TrFE)$ composites with k values above 200 [4]. Rao et al. reported a lead magnesium niobate-lead titanate (PMN-PT, 900 nm)+BaTiO₃ (50 nm)/high-k epoxy system (effective k, 6.4) composite with a k value about k150, for ceramic filler loading as high as 85% by volume [16]. But the high filler loading of ceramic powders will lead to some technical barriers for real applications of polymer-ceramic composite in the organic substrate because it results in poor dispersion of the filler within the organic matrix and almost no adhesion toward other layers in the PCB as well due to the low polymer content.

8.3.3 Conductive Filler/Polymer Composites

A conductive filler/polymer composite is another approach toward ultrahigh-k materials for integral capacitor application of next-generation microelectronic packaging, which is a kind of conductor-insulator composite based on percolation theory [17]. For conductive filler/polymer composites, the effective electrical properties approaching the percolation threshold are determined by scaling theory, which can be described as Eqs. (8.4) through (8.6) [18]:

$$\sigma = \sigma_{\rm M} (f - f_c)^t f > f_c \tag{8.4}$$

$$\sigma = \sigma_{\rm D} (f_c - f)^{-q} f < f_c \tag{8.5}$$

$$\varepsilon = \varepsilon_{\rm D} / |f - f_c|^q \cong \varepsilon_{\rm D} (\sigma_{\rm M} / \sigma_{\rm D})^{\rm s}$$
(8.6)

where $\sigma_{\rm M}$ and $\sigma_{\rm D}$ are the electrical conductivities of the conductive filler and polymer, respectively; f and f_c are the concentration and the percolation threshold concentration of the conductive filler within the polymer matrix, respectively; $\varepsilon_{\rm D}$ is the dielectric constant of the polymer matrix; and q, s, and t are scaling constants, related to the material property, microstructure, and connectivity of the polymerconductive filler interface [18]. Ultrahigh k can be expected with conductive filler/ polymer composites when the concentration of the conductive filler is close to (but does not exceed) the percolation threshold. Physically, this phenomenon can be interpreted in terms of a "super capacitor network" with very large area and small thickness: when the concentration of the metal is close to the percolation threshold, a large amount of conducting clusters are in proximity to each other but are insulated by thin layers of dielectric material. Sometimes the effective dielectric constant of the metal-insulator composite could be three or four orders higher than the dielectric constant of the insulating polymer matrix. Also, this percolation approach requires much lower volume concentrations of the filler compared to traditional approaches of high dielectric constant particles in a polymer matrix. Therefore, this material option represents advantageous characteristics over the conventional ceramic/polymer composites, specifically, ultrahigh k with balanced mechanical properties including the adhesion strength. Various conductive fillers, such as silver, aluminum, nickel, and carbon black, have been used to prepare the polymer-conductive filler composites or three-phase percolating composite systems [17, 19–24].

Although these composites were reported with high k values at the percolation threshold, they still cannot be considered as effective materials for embedded capacitor applications due to the accompanied high dielectric loss tangent and conductivity. Some researchers use semiconductor fillers to achieve relatively low conductivity at the percolation threshold as compared to conductive fillers. Dang et al. reported that LNO/PVDF (Li-doped NiO/polyvinylidene fluoride) composites were of effective k around 290 at 100 Hz at the percolation threshold $f_c = 0.10$ [25]. And the conductivity of the semiconductor fillers was also found to play an important role on the dielectric properties and the percolation threshold of the polymer-semiconductor composites. Other approaches to control dielectric loss will be discussed below.

8.4 Nanoparticle-Based Dielectric Materials

During recent years, great efforts have been made toward the synthesis and application of nanoparticles because of their unusual physical and chemical properties resulting from the nano-sized and ultra-large surface area. Polymer composite materials based on nanoparticles provide a potential solution to meet present and future technological demands in terms of good processibility and mechanical properties of polymers combined with the unique electrical, magnetic, or dielectric properties of nanoparticles [26]. Additionally, nano-sized particles are preferred for high-*k* dielectric composite materials because they could help achieve thinner dielectric films leading to a higher capacitance density. Therefore, more nanoparticles of ceramic, metallic, or even organic semiconductor have been introduced to prepare high-*k* dielectric materials recently.

8.4.1 Ceramic Nanoparticle-Based Dielectric Composites

In the past decade, a great deal of effort has been devoted to the development of ceramic/polymer composites (0–3 composites), but most of the ceramic fillers used are in the micron size range. Although finer particle size is required to obtain a thin dielectric film and to increase the capacitance density, extremely fine ceramic particles may lead to the change of crystal structure from tetragonal, which results in the high permittivity, to cubic or pseudocubic. Generally speaking, the tetragonality and hence the permittivity of ceramic particles decrease with the particle size. Uchino et al. [27] and Leonard et al. [28] found that the tetragonality of $BaTiO_3$ powders disappears finally when the particle size decreases to approximately 100 nm and 60-70 nm, respectively. Cho et al. prepared BaTiO₃/epoxy composite embedded capacitor films (ECFs) with average particle sizes of 916 nm (P1) and 60 nm (P2); the k values of ECFs made of P1 were higher than those made of P2, so the coarser particle is more useful than the finer particle to obtain high k of ECFs using unimodal powder. But by adopting bimodal fillers, fine nanoparticles can effectively enhance the k values by maximizing packing density and removing the voids and pores formed in the dielectric films. A dielectric constant of about 90 was obtained at a frequency of 100 kHz using these two differently sized $BaTiO_3$ powders [14]. Barium titanate- and another ferroelectric ceramic-based composites exhibit considerable temperature dependence of permittivity. If very low or nearzero temperature coefficient of capacitance (TCC) is demanded, special materials with high phase transition temperature are developed. Another way to obtain the low TCC in dielectric compositions consists in selection of such materials, in which capacitance changes in one of the materials compensate the capacitance changes in the other. The effect can be reached by combining polymer matrix and ceramic filler with appropriate TCCs or mixing two different filler materials with opposite TCC values [29], as shown in Fig. 8.3. In barium titanate-based polymer-ceramic



Fig. 8.3 Compensation of TCC in material mixed from two components with opposite TCCs

composites, the positive *TCC* of 600 ppm/°C can be compensated by mixing with $SrTiO_3$ exhibiting negative *TCC* of -1800 ppm/°C [30].

8.4.2 Conductive or Semiconductive Nanoparticle-Based Dielectric Composites

The dramatic increase of dielectric constant observed in the conductor or semiconductor/insulator percolation systems close to the percolation threshold arouses interest in developing conductive or semiconductive filler/polymer composites as candidate materials for embedded capacitor applications. Especially, conductive filler/polymer nanocomposites have been identified as promising materials to fulfill the material requirements for embedded capacitors. However, the dielectric loss of this type of materials is very difficult to control, because the highly conductive particles can easily form a conductive path in the composite as the filler concentration approaches the percolation threshold. Therefore, high dielectric loss and narrow processing windows have plagued metal/polymer composites in real applications. To solve the problems of the polymer-conductive filler composites, much work has been focused currently on the control of the dielectric loss of this system to overcome the abovementioned drawbacks.

8.4.2.1 Effect of Dispersion

Uniform dispersion of nanoparticles in nanocomposite materials is required because multiparticle agglomerates inside the polymer matrix will lead to undesirable electrical or materials properties. Therefore, dispersion of nanofillers in composite materials is currently of great interest in both industry and academia. However, in many of the dielectric nanocomposite materials currently being produced, there is difficulty in obtaining both homogeneous materials and repeatable results where dielectric properties are dependent on nanofiller dispersion. Zhang et al. selected CuPc oligomer, a class of organic semiconductor materials with k as high as 10^5 , as the high-k filler dispersed in a P(VDF–TrFE) matrix. The composite showed a k of 225 and a loss factor of 0.4 at 1 Hz at low applied field [31]. The high dielectric loss is due to the long-range intermolecular hopping of electrons. Wang et al. further chemically modified CuPc to bond to the P(VDF-TrFE) backbone to improve the dispersion of CuPc in the polymer matrix. Compared to the simple blending method, the CuPc oligomer particulates in grafted sample are of relatively uniform size in the 60-120 nm range, which is about five times smaller than that of the blended composite. Furthermore, dielectric loss was reduced, and dielectric dispersion over frequency was weakened [32].

8.4.2.2 Effect of Surfactant Layer

The surfactant layer coated on nanoparticle surfaces during nanoparticle synthesis could serve as a barrier layer to prevent the formation of a conduction path to control the dielectric loss. A Ag/epoxy nanocomposite with 22 vol.% Ag possessing a high k of 308 and a relatively low dielectric loss of 0.05 at a frequency of 1 kHz was reported by Qi et al. [19]. Forty nanometer Ag nanoparticles coated with a thin layer of mercaptosuccinic acid were randomly distributed in the polymer matrix. As shown in Fig. 8.4, k and dielectric loss increase with the filler concentration up to 22 vol.%. The decrease of k after that point is not due to conduction, and this is attributed to the porosity caused by the absorbed surfactant layer and solvent residue, especially at a higher Ag content. In addition, no rapid increase of the dielectric loss tangent values was observed. Therefore, the observed highest k value was not considered as a real percolation threshold, and the formation of a conducting filler network was prevented by the surfactant coating.

8.4.2.3 Coulomb Blockade (CB) Effect of Metal Nanoparticles

This novel approach is to take advantage of the unique properties of metal nanoparticles to control the dielectric loss of the conductive filler/polymer composite.

Ag nanoparticles were in situ synthesized in an epoxy resin matrix through the reduction of a silver precursor. The presence of the capping agent and its ratio with



Fig. 8.4 k and loss tangent dependences on Ag volume fraction and frequency [19]

respect to the metal precursor were found to have great effect on the size and size distribution of the synthesized Ag nanoparticles in the nanocomposites. Nanoparticles of roughly two size ranges formed in all mixtures, while the mixtures with higher concentrations of the capping agent showed the narrower size distribution as shown in Fig. 8.5.

The Ag/CB/epoxy composite was prepared by mixing an in situ formed nano-Ag/ epoxy composite and CB/epoxy composite. It can be seen from Fig. 8.6 that in situ formed Ag nanoparticles in the Ag/CB/epoxy composites increased the dielectric constant (k) value and decreased the dissipation factor (Df). The remarkably increased k of the nanocomposites was due to the piling of charges at the extended interface of the interfacial polarization-based composites. The reduced dielectric loss might be due to the CB effect of the Ag nanoparticles, a well-known quantum effect of metal nanoparticles. More specifically, the Ag nanoparticles of ultrafine size cause a high charging energy for the tunneling electrons and inhibit the charge transfer through the small metal island, reducing the conduction loss which represents the flow of charge through the dielectric materials.



Fig. 8.5 TEM micrographs of Ag/epoxy composites in the presence of a capping agent (C.A.) with (a) [C.A.]/[silver] precursor ratio R = 1, (b) R = 0.6, (c) R = 0.4, and (d) R = 0.2 [20]



Fig. 8.6 Variation of k and Df at 10 kHz with different loading levels of Ag nanoparticles [20]



Fig. 8.7 Ag nanoparticle size effects on (**a**) *k* and (**b**) *Df* values of Ag/CB/epoxy composites at different frequencies [20]

The size, size distribution, and loading level of metal nanoparticles in the nanocomposite have significant influence on the dielectric properties of the nanocomposite system. Smaller size and narrower size distribution of Ag nanoparticles, obtained in the presence of larger amounts of a capping agent, resulted in more evident single-electron tunneling by the Coulomb blockade effect and therefore reduction in conduction loss. Figure 8.7 illustrates the dielectric properties of the composites at different frequencies. The *k* values of composites containing Ag nanoparticles are larger over the whole frequency range than those of a control sample without Ag (Fig. 8.7a), while the decreased Df for nanocomposites containing Ag nanoparticles is observed in the low frequency range (10 kHz and 100 kHz in Fig. 8.7b) only. This might be explained as the fact that the conduction loss contributes to the whole Df value less significantly as the frequency increases. Therefore, the effect of metal nanoparticles on suppressing dielectric loss is nore evident in the high frequency range. Accordingly, the Df values of nanocomposites



containing Ag nanoparticles are higher than those without Ag nanoparticles at higher frequencies (1 MHz and 10 MHz in Fig. 8.7b).

8.4.2.4 Effect of High-*k* Silver Nanoparticles/Polymer Matrix Combined with Self-Passivated Conductive Particles

In this study, an in situ photochemical method was explored to prepare a metal nanoparticle-polymer composite as a high-*k* polymer matrix in which metal nanoparticles were generated by photochemical reduction of a metallic precursor within the polymer matrix. Compared with ex situ techniques, in situ techniques could facilitate a more uniform dispersion of nanoparticles in polymers, and a photochemical approach provides the advantages of simplicity, reproducibility, versatility, selectivity, and ability of larger-scale synthesis [33].

Figure 8.8 displays TEM micrographs of Ag nanoparticles synthesized via this method in an epoxy resin. Nanoparticle sizes ranged from 15 to 20 nm with smaller ones down to 3–5 nm. This demonstrated that ultrafine-sized, uniformly distributed, and highly concentrated metal nanoparticles could be obtained in the polymer matrix via in situ photochemical reduction.

Self-passivated Al particles were then incorporated in the as-prepared Ag-epoxy nanocomposite to further improve the k of Al/epoxy composites while maintaining the relatively low dielectric loss. Figure 8.9 displays the dielectric properties of Al/epoxy and Al/Ag-epoxy composites with different Al filler loadings at a frequency of 10 kHz. The composites showed more than a 50% increase in k values compared with an Al/epoxy composite with the same filler loading of Al. Moreover, the dielectric loss was maintained below 0.05. The results suggested that the in situ formed Ag-polymer nanocomposites via photochemical approach can be employed as a high-k polymer matrix to host various fillers such as conductive metal or ferroelectric ceramic fillers to achieve both high k and relatively low dielectric loss [33, 34].



Fig. 8.9 Dielectric properties of Al/epoxy and Al/Ag-epoxy composites with different Al filler loadings (at 10 kHz) [33]

8.4.2.5 Effect of Metal Nanoparticle Surface Modification

Surface modification of nanoparticles with organic molecules was employed to change the surface chemistry of nanoparticles and thus the interaction between nanoparticles and the polymer matrix. Full characterization of the surface-modified nanoparticle (SMN) showed that a thin layer was successfully coated on the nanoparticles surface via surface modification as visible in Fig. 8.10.

The surface coating layer on the nanoparticles was demonstrated to be able to decrease the dielectric loss and enhance the dielectric breakdown strength, which can be attributed to the interparticle electrical barrier layer formed via surface modification of nanoparticles preventing the metal cores from direct contact. Different surface modification conditions, such as surface modification agent type and concentration, solvent media, etc., may play complex roles in the degree of surface modification which impacts the changes of k and dielectric loss tangent values of SMN/polymer composites dramatically. The modification effect on the material properties is visible in Fig. 8.11. Therefore, surface modification of nanoparticles surface and the interface between the nanoparticle and the polymer matrix and thus tailor the corresponding property of interest of nanocomposites [35].



Fig. 8.11 Dielectric properties of SMN/epoxy composites with different SMN loadings and different modification degree [35]

8.5 Reliability of Polymer-Based Capacitors Embedded in PCB

As was mentioned in Introduction, nowadays demand for higher and higher density of electronic circuits as well as necessity for cost reduction, force manufacturers to develop typical printed circuit/wiring boards (PCB/PWB) with integrated passives. As shown in the previous subchapter, many researchers do their research on materials and technologies of the polymer-based materials with better and better properties. Commercially available materials for embedded capacitors consist of a dielectric with a thickness from several to 20–30 μ m and one or two Cu layers with a thickness of 18–70 μ m. Examples of dielectrics in such materials are listed below [36 and references therein]:

- Modified epoxy or modified epoxy-filled ceramic between Cu layers (FaradFlex from Oak Mitsui, capacitance density up to 1700 pF/cm²)
- Thin-film paraelectrics SiO_x (10–15 nF/cm²) and thin-film ferroelectrics (200 nF/ cm²) named InSite (Rohm and Haas and Energenius)
- Anodized Ta₂O₅ (capacitance density 200 nF/cm², Stealth Capacitor from Xanodics)
- BaTiO₃ thin film on copper (Interra from DuPont),
- Polymer film with copper deposited thereon (capacitance density about 216 pF/ cm², Gould Electronics)
- High T_g (170 °C) epoxy resin with 106 fiberglass (capacitance density about 143 pF/cm², BC2000 from Sanmina-SCI)
- Epoxy dielectric filled with BaTiO₃ (capacitance density from 0.78 to 4.65 nF/cm ², C-Ply from 3 M)

Working conditions of final product, especially PCB, are changeable – thermal cycles, changes of humidity, local heating, mechanical stress caused by components' packages, and systems housing may affect the properties of embedded capacitors. Stability investigations are necessary before introducing into the market.

Reliability evaluation of embedded capacitors based on polymer/barium titanate nanocompositebuilt in PCB is based on accelerated tests consisting in long-term thermal aging, thermal shocks, voltage stress, and modeling of time to failure according to obtained experimental data [37–41].

Commercially available materials in a form of dielectric foil with copper on both sides were applied for manufacturing of test capacitors embedded inside FR4-based PCB [37]. FaradFlex® materials with different permittivity were applied: BC24M epoxy without filler ($t = 24 \ \mu m$; k = 5.6), partially filled epoxy BC12M ($t = 12 \ \mu m$; k = 9.3), and BaTiO₃ filled/epoxy BC16T ($t = 16 \ \mu m$; k = 34.3). The capacitance changes up to about 5–10% were noticed during temperature change from room temperature to 100 °C as shown in Fig. 8.12a. Long-term aging at 100 °C revealed the highest capacitance change during the initial 40–50 h (Fig. 8.12b). Continuation of the aging for the material with ceramic filler shown stabilization of the capacitance, whereas for materials without filler or partially filled, the stabilization was not



Fig. 8.12 (a) Normalized temperature dependence of capacitance at f = 10 kHz for as-made or aged BC16T and BC24M embedded capacitors; (b) stability of 10×10 mm² capacitors during long-term aging at temperature of 100 °C [37]

observed, as visible in Fig. 8.12b. The characteristics of dissipation factor are the same as capacitance; however, normalized dissipation factor changes reached values between +515% and +150% (at 1 kHz) and from +127% to +18% (at 10 kHz) for BC16T. In case of BC24M (dielectric without ceramic filler), the relative change of *Df* after aging reached values from +96% to +80% (at 1 kHz) and from +62% to +43% (at 10 kHz) [37].

Polymer/BaTiO₃ nanocomposite with relative permittivity of 34 [38] after 1000 thermal shocks between -55 and 125 °C resulted in capacitance changes between -2% and -14% compared to initial values. The quality factor (Q = 1/Df) for different test boards with the same dimensions and materials changed from -25% to +78% [38]. Thermal aging at 85 °C and 85% RH for 100 h resulted in capacitance change of +2% and quality factor changes of -18%. Nanoparticle BaTiO₃-/epoxy-based capacitors exhibit good long-term stability of capacitance at temperature of 125 °C. However, during thermal aging with applied voltage, resistivity decreased significantly at temperatures above 75 °C [39].

I–V plots determined for epoxy/ceramic composites at different temperatures are presented in Fig. 8.13a, b for FaradFlex 12TM and 16T, respectively. The increase of electrical field causes increase of leakage current I_L , which can be described by power function (8.7).

$$I_L = a U^n \tag{8.7}$$

where *a* is constant and index *n* is increased with temperature in the range 0.80-1.13 for 12TM. Based on value of *n*, one can say that the I–V characteristics and the same insulation resistance are slightly nonlinear. Quite different and much more complicated behavior was observed for capacitors based on BaTiO₃-filled 16T material. The increase of leakage current appears from very low temperatures.

It is obvious that temperature also affects the breakdown voltage of the capacitors. The temperature increase from 85 to 125 °C leads to decrease of breakdown voltage



Fig. 8.13 Influence of temperature on $I_{\rm L} = f(U_{\rm DC})$ characteristics of (a) 12TM and (b) 16T capacitors [40]

up to 2.5 times [41]. Estimated mean time to failure (MTTF) at 105 °C comparing to the time at 125 °C is three to five times longer, dependently on parameters taken from the experimental results applied to the Prokopowicz equation [41].

Polymer-ceramic filler compounds are also sensitive to moisture, changing the properties of the capacitors: capacitance, dissipation factor, breakdown voltage, and leakage current. Capacitance and dissipation factor can increase by 20% during exposure in air at 85% RH and 85 °C as a result of moisture absorption into the epoxy resin [42].

Assuming the results, the stability of the material properties can limit possible applications of the buried capacitors, especially in medium and high power systems, where temperatures can increase up to 60–70 °C, working at high humidity conditions. In general, the higher permittivity of the dielectric, the higher the instability of parameters that can be expected during operation at elevated temperatures and voltage load.

8.6 Nanocrystalline Thin-Film Materials

Permittivity of polymer/ceramic composites is limited by the maximum filler load that can be introduced to the material. Filler loads above 60–70 vol.% deteriorate the processability, the adhesion strength between metallization and composite layer, and the thermal stress reliability. It is also obvious that the presence of a low permittivity matrix decreases the compound relative permittivity. If the polymer matrix can be eliminated, the permittivity of the material should increase.

Thin-film layers based of typical high permittivity compounds or solid solutions, for example, BaTiO₃ (BTO) [43–48], $Bi_2Mg_{2/3}Nb_{4/3}O_7$ (BMN) [49], $Bi_2Zn_{2/3}Nb_{4/3}O_7$ (BZN) [50], and (Pb_{0.85}La_{0.15})(Zr_{0.52}Ti_{0.48})_{0.96}O₃ (PLZT) [51],

Material	Mean crystallite/ grain size	k	Df	Method	Ref.
BaTiO ₃	20–50 nm	350 (1 MHz)	0.03 (1 MHz)	Aerosol deposition	[43]
BaTiO ₃ /Al	Al, 3 μm; BaTiO3, 50 nm	2500 (1 MHz)	0.1 (1 MHz)	-	[43]
BaTiO ₃	11 nm	64 (100 kHz)	0.073 (100 kHz)	-	[44]
BaTiO ₃ - PTFE	BaTiO3, 25 nm	15 (100 kHz)	0.091 (100 kHz)		[44]
BaTiO ₃	<10 nm	>100 (100 MHz)	<0.03 (100 MHz)	-	[45]
BaTiO ₃	<100 nm	1300	-]	[46]
BaTiO ₃	80 nm	370 (2 GHz)	0.06 (2 GHz)	Hydrothermal	[47]
BaTiO ₃	200 nm	400 (2 GHz)	0.1 (2 GHz)	synthesis	[48]
Bi ₂ Mg _{2/} ₃ Nb _{4/3} O ₇	8–10 nm	40 (100 kHz)	0.02 (100 kHz)	Pulsed laser deposition	[49]
Bi ₂ Zn _{2/} 3Nb _{4/3} O ₇	4.5 nm	60 (1 kHz)	0.07 (1 kHz)		[50]
PLZT	20–100 nm	240 (100 kHz)	<0.017 (100 kHz)	Chemical solution deposition	[51]
PZT	-	<300	<0.03	1	[52]

Table 8.1 Properties of nanocrystalline film capacitor materials

can be applied as a dielectric material for embedded capacitors. The layers can be prepared using various methods. Materials applied for embedded capacitors, which are processed together with the PCB, should be processed at a temperature lower than the maximum allowable temperature for the laminate used. Physical methods carried out at room temperature, like pulsed laser deposition (PLD) [49, 50] or aerosol deposition (AD) [43–46], are suitable in this instance. Higher temperatures or chemical harsh conditions during processing make fabrication of capacitors dielectrics together with the PCB impossible. Hence, the layers prepared using such methods like hydrothermal synthesis [47, 48] or deposition from chemical solution [51] can be made separately on metallic foil and then laminated into the PCB. In this case, the temperature limitation and polymer degradation risk do not matter. Examples of materials, methods used for manufacturing thereof, and basic properties are compared in Table 8.1.

Aerosol deposition is a promising method for preparation of dielectric layers of various materials. The technique consists of collision of high kinetic energy particles with the substrate and their adhesion to the substrate thanks to the energy. The particles are accelerated by flow through a nozzle with air at the proper pressure. When the powder used in the process has some distribution of particle size, mostly particles with lower size are deposited on the substrate [45]. Despite adhesion of only the smallest particles, larger particles are desired in the aerosol stream because

higher layer densities can be obtained thanks to collisions between the particles. A deficiency of particle collisions results in a porous microstructure of the layer [46]. The aerosol deposition method has many advantages – the process is carried out at room temperature and hence is appropriate for polymer substrates, the process is solvent-free, high density of manufactured layers can be reached, and hence high permittivity can be expected. The permittivity of BTO layers made using the method varied from 100 [45] to even 1300 [46]. The addition of a polymer material like PTFE [44] should improve the elasticity of the layer; however, the permittivity is decreased. The presence of metal particles in the layer can increase the permittivity of the layer [43] thanks to percolation phenomena, as described in the section concerning polymer composites.

Another deposition technique based on physical effects, suitable for fabrication of dielectric layers, is the pulsed laser deposition (PLD) method [49, 50]. The source material used for deposition of high permittivity dielectrics in this method can be prepared as a ceramic target made in a conventional ceramic process, comprising solid-state reactions of specified oxide powders, milling, pressing, and sintering [50]. The material is evaporated in a vacuum chamber using a laser. The process can be carried out in a reactive gas such as oxygen [49]. Layers are deposited on substrates at room or elevated temperature. Embedded capacitors made of BMN deposited at 100 °C and 150 °C exhibit better dielectric and leakage current properties than films deposited at room temperature [49]. However, when the process is carried out at room temperature, post-process annealing at 150 °C defines the final properties in the case of the BZN layer [50].

Hydrothermal synthesis of dielectric materials from proper precursors is a chemical method. Using this technique, high permittivity nano-grained dielectrics can be prepared [47, 48]. 300-nm-thick BTO layers were synthesized on 12.5-µm-thick titanium foil from a water solution of Ba(OH)₂ at 95 °C [47]. Samples after annealing at 160 °C were laminated onto FR4 laminate using epoxy prepregs. The layer exhibited relative permittivity of 370 and Df of 0.06 [47]. Another approach consists in initial coating of the PCB with titanium and then synthesis of a BTO layer on the PCB [48]. The layers were synthesized using water solution of Ba(OH)₂ at 80, 150, or 200 °C. The layers prepared at the highest temperature exhibited uniform grain size below 200 nm and the thickness of about 155 nm. For other temperatures, the grain size varied from 200 nm to 1 µm. Thicknesses of the layers were below 250 nm. The highest permittivity and Df were exhibited by the layers synthesized at 80 °C (450 and 0.25 at 1 kHz). The lowest permittivity and Df were obtained for layers prepared at 200 °C (400 and 0.1 at 1 kHz) [48]. Additional processing, like oxygen plasma treatment, can reduce the leakage current of the dielectric made by the hydrothermal method, thanks to elimination of hydroxyl groups [48].

Dielectric layers can be deposited from a chemical solution containing inorganic precursors and organic solvent. The solution is successively spun on the substrate and pyrolyzed several times in order to prepare a thick enough layer. Example of the material deposited using this method is PLZT [51]. The layer was pyrolyzed at 450 °C and finally crystallized at 600 °C. The PLZT layer was deposited on nickel-covered copper foil, preventing the base substrate from oxidizing at a relatively high

process temperature. Permittivity above 200 and *Df* below 0.02 were obtained [51]. Similar processes can be carried out for PZT (lead zirconate titanate) material [52].

Thin dielectric films with nanocrystalline structure exhibit good dielectric properties thanks to high density and the absence of any other materials, especially low permittivity phases. Such layers in comparison to polymer-based material can reveal better stability at elevated temperatures – the limit results from phase transitions in dielectrics instead of structure degradation.

8.7 Ceramic and Thick-Film Dielectric Composites

Thick-film and ceramic materials are typically prepared from powders of various sizes typically from dozens of micrometers down to hundreds of nanometers. Thermal treatment of such materials is typically carried out at temperatures above 800 °C. Hence, the grains in such composites can be bonded by a glass matrix or directly sintered together. The conduction mechanisms are similar in materials made of particles with nano- and micrometer size. Therefore, the composites made in thick-film or ceramic technologies are also included in the chapter concerning the nanoparticle-based dielectrics.

Thick-film and ceramic materials for capacitor applications are typically based on very common BaTiO₃ [53–56]. However, many other materials with improved properties or extended temperature of operation compared to barium titanate are developed. Examples of such materials are doped BaTiO₃ [57, 58], CaCu₃Ti₄O₁₂ [59, 60], Bi_{2/3}CuTi₄O₁₂ [61], or more complex systems like $(1-x)(Bi_{1/2}Na_{1/2}TiO_3-BaTiO_3) -x(K_{0.5}Na_{0.5}NbO_3)$ [62] and $(K_{0.5}Na_{0.5})NbO_3-Bi(Zn_{2/3}Nb_{1/3})O_3$ [63]. The materials in a form of powder can be used for preparing screen-printable pastes [53, 54, 62] and flexible tapes [55, 57–59, 61] or can be pressed to pellet form [58, 62, 63].

Usually, bulk specimen manufacturing is the initial stage during development of ceramic materials, considering determination of processing parameters as well as the main properties. The materials can be used for fabrication of multilayer ceramic capacitors (MLCC) or capacitors integrated with ceramic substrates on their surfaces or inside. Surface and buried components can be processed in standard thick-film technology from screen-printable dielectric pastes. Such materials, based on barium titanate and its compounds, are commercially available products intended for use as materials processed together with low-temperature cofired ceramics (LTCC) for manufacturing embedded capacitors inside the LTCC modules. These materials exhibit relative permittivity between 50 and 250 and *Df* below 0.02 at 10 MHz [53, 54]. However, the *Df* can increase when dielectric and electrode materials are incompatible [54]. The capacitors exhibit satisfying stability; after aging at 250 °C, the parameters changed less than $\pm 3\%$ [53]. The barium titanate-based capacitors have a main drawback – their relatively low Curie temperature causes the capacitance to change under typical temperatures of operation below 125 °C. Much higher

operating temperature can be obtained for dielectric compositions based on some complex solid solutions, for example, $(1-x)(Bi_{1/2}Na_{1/2}TiO_3-BaTiO_3)-x$ (K_{0.5}Na_{0.5}NbO₃) [62]. Screen-printed capacitors based on this material exhibited permittivity of 1430 and *Df* of 0.06. Permittivity variance below 10% was observed for temperature changes from 62 to 382 °C [62].

In thick-film processing, the thickness repeatability of screen-printed dielectrics is poor, resulting in high scatter of capacitance values. Better thickness uniformity can be reached by applying ceramic tapes. Direct integration of any high permittivitybased tapes with low permittivity LTCC is not possible because of differences in sintering temperatures of the materials. The LTCC is typically fired at 850–900 °C, whereas for pure barium titanate, a temperature range between 1200 and 1300 °C is required [58]. Taking that fact into account, some additives like glass [59] or sintering aid [57, 58] should be applied to the material before preparing of the dielectric tape. For pure BaTiO₃-based tape applied as a dielectric layer buried into a LTCC module, relative permittivity of 475 and Df below 0.03 can be obtained [55]. In this case, densification is possible thanks to the glass phase in the LTCC tape; however, the parameters are far removed from those for pure barium titanate sintered at typical temperatures. The presence of the glass phase and interaction between the high permittivity and LTCC materials always results in decreased permittivity. Nevertheless, application of proper electrode material can limit diffusion processes, achieving acceptable parameters of the dielectric material. Permittivity above 300 for Sr-doped BaTiO₃ tape cofired with the LTCC was achieved thanks to appropriate electrode metallization [57]. During sintering of different ceramic tapes, for example, BaTiO₃ and LTCC tapes, shrinkage differences can cause damages inside the multilayered structure. One solution to reduce the nonuniform shrinkage consists in application of pressure during the firing process [55, 56] – then delamination and camber can be reduced. However, when pressure cannot be applied during the process, the different materials should have the same or similar shrinkage behavior. Thanks to proper additives to the dielectric material, the shrinkage, densification process, and firing temperature can be adjusted [58]. The barium titanate doped with LiF and CuO can be well densified at temperatures between 800 and 900 °C. When 10 wt% additions of LiF and CuO in ratio of 1:1 to the barium titanate is applied, the shrinkage is the same as for LTCC fired at 860 °C [58].

Ceramic tapes were developed for application in manufacturing of MLCC. First multilayer capacitors were based on barium titanate, but temperature stability forced manufacturers and researchers to develop materials less sensitive to temperature changes. Dielectric layers in the MLCC with higher and higher capacitance densities should be thinner and thinner. Hence, the grain size must also be reduced. When the BaTiO₃ dielectric thickness of few μ m is used in the capacitors, the average grain size is lower than 0.5 μ m, down to 0.3 μ m [56]. Unfortunately, the reliability of capacitors with dielectric thicknesses below 6 μ m decreases significantly [56].

8.8 Summary

Generally speaking, high-k dielectric materials which can be realized for embedded passive applications are required to have high dielectric constant, low dissipation factor, high thermal stability, simple processibility, and good dielectric properties over a broad frequency range. However, no such ideal materials that satisfy the prerequisites simultaneously abovementioned have been realized vet. Nanocomposite materials based on nano-sized particles have the potential to meet both present and future technological demands due to their unique properties, and these materials have been studied extensively. Several techniques to further improve the overall dielectric properties of these candidate materials for real applications can be understood from theoretical predictions, which indicate that the dielectric constant of materials can be maximized and dielectric loss can be suppressed by the following methods:

- 1. Optimized formulation of dielectric materials with high filler loading of high dielectric constant ceramics for ceramic-polymer nanocomposites and appropriate loading level of conductive fillers in the neighborhood of percolation threshold for conductive filler-polymer nanocomposites.
- 2. Improvement in morphology of dielectric materials such as filler size and distribution, packing, and dispersion in the polymer matrix.
- 3. Appropriate processing methods.
- 4. Modification of the filler interface to suppress the dielectric loss. Improvement of dielectric properties of ceramic-polymer composites can sometimes deteriorate stability of the materials, so much attention should be paid to reliability and compatibility evaluation before introducing them to mass production. As distinct from polymer-filler-based dielectrics, in materials prepared using thin-film, thick-film, and ceramic techniques, low permittivity phases can be eliminated, and higher permittivity can be achieved. Polymer-nanoparticle-filled and thin-film materials can be used for manufacturing of capacitors built into printed circuit boards. In case of ceramic and thick-film techniques, capacitors can be integrated on ceramic substrates' surface or inside the substrates. Mentioned methods were developed mainly for better miniaturization and reduction of electronic devices' production costs, as well as improvement of devices' reliability and operation frequency bandwidth.

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Chapter 9 Nanostructured Resistor Materials



Damian Nowak, Andrzej Dziedzic, Fan Wu, and James E. Morris

9.1 Introduction

This chapter focuses on nanostructured resistor materials in which there exists a macroscopic scale of inhomogeneity. In such a material, there are small, yet much larger than atomic, regions where macroscopic homogeneity prevails and where the foregoing macroscopic parameters suffice to characterize the physics, but different regions may have quite different values for those parameters. If we are interested in physical properties only at scales that are much larger than those regions and at which the material appears to be homogeneous, then the macroscopic behavior can again be characterized by bulk effective values of the conductivity (σ) and dielectric coefficient (ε).

There is some literature [1–4] on the electrical properties and structural properties of nanostructured resistor materials. However, there are few data, especially in a systematic way, on the relationship between the microstructure and the DC and AC electrical properties of nanostructured resistor materials. In this chapter, detailed studies of structural, compositional, and electrical properties of nanostructured resistor materials. A detailed understanding of the charge transport in nanometallic particle systems such as three-dimensional

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cermets and two-dimensional discontinuous metal films is important to the achievement of a successful model for the conductivity of nanostructured resistor materials.

In this chapter, a brief overview of nanostructured resistor materials is given first. Then electrical conduction models are discussed, including compositional, structural, and electrical (I-V, R-T) characterizations. The next part of this chapter is then related to fabrication and microstructure and to electrical and stability properties of surface and buried polymer or cermet thick-film resistors.

9.2 Nanostructured Resistor Material Overview

Nanostructured resistor materials are composite materials of conductor and dielectric. There are two types of nanostructured resistor materials. The first one includes films consisting of a physical or chemical mixture of metals and dielectrics and is generally classified under the general heading of cermets, from ceramic-metal. Cermet films are prepared by a number of different methods such as evaporation or sputtering of an oxidizable metal in the presence of some oxygen [5, 6], co-evaporation [7], co-sputtering [8], simultaneous or alternating plasma polymerization and metal evaporation [9], or implantation of metal ions in polymers [10]. Another type is the discontinuous metal film, which is formed during the initial stage of depositing thin metal films either by evaporation [11] or sputtering [12, 13].

In the case of two-dimensional discontinuous films, these correspond to three growth stages. In the initial stages of growth, discrete nuclei are formed, and these are generally stable once they consist of several atoms. The nuclei grow by capturing migrating surface adatoms or atoms direct from the vapor phase, and when the island separation is reduced to a few nm, it is found that direct electrical current can pass through the film. With further island growth, the stage is reached where coalescence occurs. This is generally accompanied by a more rapid decrease in electrical resistance. Eventually, island coalescence leads to the formation of an interconnected network of capillaries that conduct like a normal metal. The important feature of this class of structure is that the overall film resistance is dominated not by the resistivity of the capillaries but by the manner in which they are connected. It is quite usual to observe very wide differences in resistance between films having nominally identical masses of metal per unit area, and this is due to the distribution of material on the substrate. The third structural class, the continuous metal film, is formed when the holes between the capillaries are filled in and the film approximates to a plane parallel slab, generally of polycrystalline metal. Surface and grain boundary scattering govern the resistivity of the film in this regime. Figure 9.1 shows atomic force microscopy (AFM) images of aluminum films with structures belonging to these three regimes [13].

Figure 9.2 shows the sheet resistance variation with the deposition time for the discontinuous aluminum films [13].

In the metallic regime, electronic conduction retains most of the properties of bulk metal. For example, granular Ni-SiO₂ films exhibit bulk ferromagnetism for



Fig. 9.1 AFM images of aluminum films with film structures of (a) nucleation stage, (b) coalescence stage, and (c) continuous film stage [13]



Fig. 9.2 Surface resistivity versus deposition time [13]

0.7 < x < 1 [14], where x is the atomic fraction of Ni in the composite. However, properties that depend on electronic mean free paths are drastically modified due to strong electron scattering from dielectric particles and grain boundaries. For instance, the electrical conductivity decreases by orders of magnitude from its crystalline value, and the temperature coefficient of resistance (*TCR*), although positive, is very much smaller than in bulk metals [15].

In the dielectric regime, which consists of isolated, nanometer size metal islands, two important physical quantities are substrate-assisted electron transport [16] and the thermally activated charging energy required to transfer an electron between two neutral islands [11].

Electrical conduction in the transition regime, which consists of a random interconnected array of metallic capillaries, is of particular interest because of its relevance to the mathematical topic of percolation theory. The electrical conductivity in this regime is due to percolation along the metallic capillaries and electron tunneling between isolated metal islands. Conduction in the island structure is, as stated earlier, an activated process that gives rise to a negative *TCR*, while conduction in the capillaries is of a normal metallic type with a reduced positive *TCR*.

The transition from nonmetallic to metallic conduction in nanostructured resistor materials is governed by the volume or area fraction of the substrate covered by metal. Consider a substrate as an orthogonal lattice upon which metal nuclei can grow, but only at the nodes (sites). As growth proceeds, the stage will be reached where adjacent nuclei actually come into contact and coalesce. Although in the hightemperature limit a single nearly spherical nucleus may be expected to be formed upon coalescence of two smaller nuclei, in general elongated capillaries tend to be formed. Thus, the nuclei constitute the sites, their size governs the strength of interaction, and the capillaries are equivalent to the bonds. There are basically two problems in percolation theory. The "site" problem is concerned with the variation of physical properties in terms of the proportion of occupied sites. The "bond" problem is concerned with the variation in terms of bonds present. From the point of view of electrical conduction, it is of interest to determine the stage at which the transition from metallic regime to dielectric regime occurs. In fact, for a granular metal film, this will not be a sharp transition since there will be a range of structures in which conduction between islands will occur simultaneously with metallic capillary conduction, and initially the resistance contributions will be of similar values. Eventually the tunnel contribution will be completely shorted by the capillaries. For a two-dimensional lattice, Scher and Zallen got a critical surface fraction of 44% of the covered surface area when large-scale connected paths formed [17].

Analysis of the structural and electrical transport data yields detailed information on the granular metal film parameters: average metal particle size, average metal particle separation, and their distributions. When an electron is transferred from one initially neutral island to another, a certain amount of work must be done against electrostatic forces. Therefore, the only electrons which could be transferred were those excited to a level of the order of $e^2/4\pi\epsilon r$ above the Fermi level of the particular island of radius, r, [18], where e is the electronic charge and ϵ is the effective dielectric constant of the medium. This energy can be supplied thermally at temperature, T, and, if Boltzmann statistics are obeyed, then the total number of charged islands, n, can be written as

$$n = N \exp(-\delta E/kT) \tag{9.1}$$

where *N* is the total number of islands and δE is the activation energy which must be supplied to overcome the electrostatic force, expressed by the Neugebauer and Webb formula

$$\delta E = \frac{e}{4\pi\varepsilon_0\varepsilon_r r} \left(\frac{s}{r+s}\right) - Fs \tag{9.2}$$

where s is the island separation and F is the applied electric field.

The activated tunneling conduction model expresses the conductivity as

$$\sigma = Ks^2 e^2 D \exp\left(-\frac{\delta E}{kT}\right) \tag{9.3}$$

where *K* is a geometrical constant and *D* is the interisland tunneling probability.

The Neugebauer and Webb theory and some other extended models proposed through the last several decades [19–22] have been able to account for several of the experimental observations and were in good qualitative agreement with experimental observation. Agreement between experimental and theoretical activation energy, δE , is sufficient to validate the fundamental electrostatic activated tunneling model (s), which is recognizable as the basis of the Coulomb blockade. However, questions remained before the problem of the mechanism of transport in granular metal film systems could be totally resolved:

- The absolute conductances are found to be orders of magnitude greater than theory.
- Despite attempts to apply variable range hopping concepts and percolation theory, the statistical effects of distributed *r* and *s* values, and island shapes, have yet to be included successfully.
- It is unclear whether the high- or low-frequency dielectric constant should be used in δE .
- Experimental results described in the next paragraphs are inconsistent with existing theories and indicate that major modification of the basic thermally activated tunneling mechanism is needed.

Borziak et al. [23] reported three significant experiments. With previously deposited electrodes, they were able to fabricate discontinuous films with different island structures immediately adjacent to the contact, with smaller islands and/or wider gaps. These symmetrical "inhomogeneous" films showed that the voltage drop is always greater at the positive end of the film. The second result was the observation of stable and reproducible switching in such films, but the explanation of this effect is still elusive. In the third experiment, the inhomogeneous films were also made asymmetric, i.e., with different inhomogeneous structures at the two electrodes, whereupon the DC resistance became polarity dependent, i.e., a diode-like effect. These results cannot be explained on the basis of the conduction models discussed in the last paragraph and indicate that the conduction mechanism must depend significantly upon the islands at the electrodes [24, 25].

The asymmetric film study has been extended to AC effects by Morris [25]. In the traditional model, the film is regarded as a matrix of identical island/gap elements, with the metal island resistance in series with the parallel combination of gap tunnel resistance R_g and capacitance C_g , where $\delta E = \frac{1}{2} \frac{e^2}{C_g}$. C_g values determined by AC measurements on this model are universally orders of magnitude greater than those consistent with δE . With the asymmetrical inhomogeneous film, two corner frequencies appear, yielding two distinct values for both R_g and C_g , corresponding to the two electrodes. In addition, the C_g values match well to capacitances between the electrodes and film across a single gap width. At extreme asymmetries, a "pseudo-inductive" effect makes an appearance, as one contact resistance becomes very large, representing a time delay to establish steady-state conductance in the film by injection of the charge carriers which account for the higher conductances than predicted by a Boltzmann distribution of charged islands [26, 27]. These 2D effects are expected to be replicated in 3D cermet resistor films.

9.3 Physical Properties of $Cr_x(SiO)_{1-x}$ and $(Cr_xSi_{1-x})_{1-y}N_y$ Nanostructured Resistors

9.3.1 Microstructure and Composition

All the $Cr_x(SiO)_{1-x}$ samples were sputter deposited from Cr-SiO targets in an Ar ambient. All the $(Cr_xSi_{1-x})_{1-y}N_y$ films were deposited in Ar/N₂ ambients. C_{N2} is the nitrogen concentration in the Ar/N₂ mixtures.

9.3.1.1 Rutherford Backscattering (RBS) Analysis

The chemical compositions of the samples were determined by Rutherford backscattering (RBS). We confirmed the consistency of these data by energy dispersive X-ray (EDX) analysis by means of a LINK AN10000 EDS system attached to a JSM-840 SEM. RBS is considered as likely to give the most accurate composition values since this method is quantitative from first principles and does not require elemental standards. The quantitative results of the EDX analysis are influenced by a series of effects; in particular this method needs standards and various corrections.

Table 9.1 shows the atomic concentration data from RBS measurements. Figure 9.3 shows the depth profile generated from the theoretical fitting to the experimental data. The sample used in the RBS measurement is a 30-nm-thick $Cr_x(SiO)_{1-x}$ film deposited from a target with [SiO]/[Cr] = 80/20.

Table 9.1 Atomic	Depth (nm)	N	0	Si	Cr	Si/Cr	Si/N	
concentration from RBS	<32	5.03	45	31.0	16.5	1.88	0.59	
	32–274	-	67	33	-	-	-	
	>274	-	-	100	-	-	-	



Fig. 9.3 Depth profile generated from the theoretical fitting to the experimental data

N2 partial pressure (mTorr)	Anneal temp. (K)	at% O	at% C	at % Si	at% Cr	at% N
0.8	540	28.10	1.29	44.07	19.84	6.67
0.4	450	16.07	0.63	57.06	22.66	3.56
0.1	No	12.66	0.45	59.67	25.41	1.81
0.8	540	25.87	3.86	45.37	17.91	6.98
0.4	400	13.65	1.39	61.76	19.31	3.89
0.8	540	26.66	0.85	48.09	18.08	6.32
0.4	400	14.62	0.88	62.49	17.61	4.40
0.6	450	15.59	2.14	58.89	18.50	4.88
0.4	No	10.95	0.30	65.30	19.37	4.08

Table 9.2 Relative atomic % determined from ESCA survey spectra



	100 eV	103 eV
N ₂ partial pressure (mTorr)	Silicon	Silica
0.8	44.71	55.29
0.4	24.86	75.14
0.1	23.47	76.53
0.8	40.23	59.77
0.4	16.40	83.60
0.8	12.71	87.29
0.4	33.42	66.58
0.4	13.69	86.31
0.4	05.12	94.88

9.3.1.2 X-Ray Photoelectron Spectroscopy/Electron Spectroscopy for Chemical Analysis (XPS/ESCA)

The purpose of the XPS analysis is to determine the chemical composition of annealed $Cr_x(SiO)_{1-x}$ films, evaluated at the surface and after ~10 nm sputter etch. The experimental details of the ESCA analysis are listed as follows:

The ESCA data of samples deposited from a target with [SiO]/[Cr] = 80/20 with different nitrogen concentrations, C_{N2} , are shown in Table 9.2. The survey spectra show the presence of Cr, Si, O, C, and N at the surface, as expected. The relative atomic percent of these species shown in the table matches the nitrogen partial pressure during the reactive sputtering very well. The carbon found in the films is from the target. No other species were detected.

Two peaks were identified in the region of Si. The low binding energy peak is suggestive of silicides or silicon, while the higher binding energy component is representative of silica-type species. See Table 9.3 for relative amounts of Si species.



Fig. 9.4 SIMS mass spectra of $Cr_x(SiO)_{1-x}$ film

9.3.1.3 Secondary Ion Mass Spectroscopy (SIMS) Analysis

The SIMS analyses were performed on a PHI-6600 quadrupole mass spectrometer with oxygen primary ion bombardment and using positive secondary ion mass spectrometry.

The peaks in the mass spectra, shown in Fig. 9.4, have been assigned and indicate the presence of H, C, B, N, O, Cr, and Si in the sample. Figure 9.4 also indicates that there are several forms of Cr existing in the film: metallic Cr, CrB, CrO, and Cr silicide – CrSi.

9.3.1.4 Transmission Electron Microscopy (TEM) Analysis

The microstructure of the samples was investigated by TEM. Samples for TEM studies were deposited on carbon-coated copper grids from Electron Microscopy Science or silicon nitride membrane windowsTM grids from SPI.

For electron-microscope studies, films of about 20 nm thickness were deposited. Figure 9.5 shows electron micrographs for two film compositions. Figure 9.6 shows electron diffraction diagrams of the same samples. Figure 9.5a, c shows the structure observed as deposited at room temperature. In both cases the films were found to be



Fig. 9.5 Transmission electron microscopy images of $(Cr_x Si_{1-x})_{1-y}N_y$ films with $C_{N2} = 0.5\%$: (a) x = 0.2, unannealed; (b) x = 0.2, annealed at 540 °C in N₂ ambient for 1.5 h; (c) x = 0.6, unannealed; and (d) x = 0.6, annealed at 540 °C in N₂ ambient for 1.5 h

well amorphous with crystalline regions. The principal structures found in deposited films with [SiO]/[Cr] = 80/20 is a "cellular" microstructure of dark islands around 1–2 nm in size surrounded by medium of lighter contrast about 2–3 nm wide. It is likely that the dark islands contain the high Z component of the film, i.e., the Cr. EDX indicates the film is amorphous or that there is only very short-range order in the film, which is indicated by the diffuseness of the diffraction patterns. Figure 9.5b, d shows the structures after annealing at 540 °C in ambient N₂ for 0.5 h. Films with higher [SiO]/[Cr] ratios have finer metal island dispersions. Annealing has the same effect of islands growing coarser for both samples but has the opposite

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Fig. 9.6 Electron-diffraction diagrams of $(Cr_xSi_{1-x})_{1-y}N_y$ films with $C_{N2} = 0.5\%$: (a) x = 0.2, unannealed; (b) x = 0.2, annealed at 540 °C in N₂ ambient for 1.5 h; (c) x = 0.6, unannealed; and (d) x = 0.6, annealed at 540 °C in N₂ ambient for 1.5 h

effect of separation between islands for the samples. For the annealed samples, the microstructure remains similar to that as deposited. However for the film with [SiO]/ [Cr] = 80/20, the island size grows from ~1 to 2–4 nm, and the spacing between islands increases from 2–3 nm to about 5 nm. The crystalline phase remains largely unchanged, especially as evidenced by little change seen in the diffraction pattern in Fig. 9.6b. For the sample deposited from a target with [SiO]/[Cr] = 40/60, the island size grows from 2–4 to 5–10 nm, and the spacing between islands actually decreases to <1 nm, or some of the islands are connected to form metallic pathways. These structural changes are also reflected in electrical measurements on the samples prior to and post annealing. Based on the activated tunneling conduction model discussed above for granular metal, the film resistance R may be written approximately for effective tunneling barrier height Φ as

$$R = C \exp\left(A\phi^{1/2}s + \frac{\delta E}{kT}\right) \tag{9.4}$$

where A and C are constants, and the temperature coefficient of resistance (*TCR*), α , is defined as

$$\alpha = \frac{1}{R} \frac{dR}{dT} = -\frac{\delta E}{k} \frac{1}{T^2}$$
(9.5)

from which we see that the *TCR* becomes less negative as island radius increases. For the film with [SiO]/[Cr] = 80/20, the island radius, *r*, and spacing, *s*, both increase after annealing at 540 °C. Therefore, according to Eqs. (9.5) and (9.6), the sheet resistance increases after annealing, and the *TCR* becomes less negative post anneal. For the film with [SiO]/[Cr] = 40/60, the sheet resistance decreases after annealing, and the temperature coefficient of resistance changes sign from negative to positive post annealing at 540 °C. From Fig. 9.6d, it is observed that there are two possible charge transport paths in the annealed film with [SiO]/[Cr] = 40/60, these being:

- 1. Normal metallic conduction in the metallic capillaries
- 2. An activated conduction process between the metallic islands

So there are two parallel independent conduction processes in this annealed film, which is the reason behind the sign change of its TCR.

The diffraction pattern in Fig. 9.6d shows the presence of two new rings compared to the as-deposited sample. The change in the pattern indicates that a change is occurring in the film around this temperature. Crystalline grains of Cr and CrSi₃ were observed after 540 °C anneal in ambient N₂, which was also confirmed by the EDX analysis that will be presented later.

Figure 9.7 shows TEM images of four Cr_xSi_{1-x} films deposited from different Cr compositions: 10%, 30%, 50%, and 60%, respectively. Figure 9.8 shows their corresponding electron diffraction diagrams.

Figure 9.9a, b shows electron micrographs of an as-deposited $(Cr_xSi_{1-x})_{1-y}N_y$ film with x = 0.4 and y = 0 and 0.1, respectively. The film thickness is 25 nm. The film consists of small Cr islands (dark areas), the mean diameter of which is around d = 2 nm, embedded in an amorphous Si matrix (light areas). Figure 9.9b shows that the structure of the reactively sputter-deposited film is similar to that of the film deposited by pure Ar sputtering.

Most of the Cr islands in Fig. 9.7 are disconnected by small SiO bridges, so the film is below the percolation threshold. In a schematic representation, Fig. 9.10 shows the structural properties of the Cr_xSi_{1-x} films, revealing both disconnected



Fig. 9.7 High-resolution TEM (HRTEM) images of samples with different Cr compositions: (a) 10%, (b) 30%, (c) 50%, and (d) 60%

and connected Cr islands, simply given as circles in Fig. 9.10. As identified in Fig. 9.10, island diameters, r, and center-to-center distances, R, have been measured. From the corresponding mean value (r, R), the mean island separation s = R - r was calculated.

In Table 9.4, *x* is the Cr volume fraction, *t* the film thickness, *r* the mean particle diameter, σ_r the standard deviation of *r*, *R* the mean center-to-center distance, σ_R the standard deviation of R, *s* the mean gap size between particles obtained from s = R - r, and σ_s the standard deviation for *s*.

Cross-sectional HRTEM is also performed on $Cr_x(SiO)_{1-x}$ films as deposited, as shown in Fig. 9.11. No magnification markers are shown on the micrographs since the lattice fringes serve as scale markers (with the main spacing of the fringes corresponding to the Si(111) planes, i.e., 0.313 nm). The specimens were tilted to the Si[110] zone axis to ensure that the $Cr_x(SiO)_{1-x}$ layer was viewed directly edge on. The images show the Si substrate, the oxide layer, the CrSi layer, and finally the



Fig. 9.8 Electron-diffraction diagrams of samples with different Cr compositions: (a) 10%, (b) 30%, (c) 50%, and (d) 60%

part of the passivation layer. A combination of high-resolution and diffraction contrast imaging was used to enhance contrast of the layers while still providing lattice images from which to accurately determine the size of metallic islands in the $Cr_x(SiO)_{1-x}$ layer and the layer thickness. While the boundary between the oxide and the $Cr_x(SiO)_{1-x}$ layer is quite well defined, the top part of the $Cr_x(SiO)_{1-x}$ layer is somewhat diffuse, suggesting that the density of the $Cr_x(SiO)_{1-x}$ film varies along the growth direction. Diffraction contrast imaging reveals small dark regions, 1.5–2 nm in size, in the $Cr_x(SiO)_{1-x}$ layer. No lattice fringes are evident in this layer in any of the images. This matches the observations from top TEM images and indicates that there is no long-range crystalline order within the $Cr_x(SiO)_{1-x}$ layer as deposited.



Fig. 9.9 Electromicrographs of $(Cr_xSi_{1-x})_{1-y}N_y$ films: (a) x = 0.4, y = 0, (b) x = 0.4, y = 0.1





Table 9.4 Measured (unannealed) $Cr_x(SiO)_{1-x}$ film parameters (defined in Fig. 9.10); Cr/SiO = 60/40

Film	<i>t</i> (nm)	<i>r</i> (nm)	$\sigma_{\rm r}$ (nm)	<i>R</i> (nm)	$\sigma_{\rm R}$ (nm)	s (nm)	$\sigma_{\rm s}~({\rm nm})$
#1	20	4.3	1.61	4.65	1.54	1.69	0.59
#2 ($y = 0.1$)	21	2.6	0.79	4.03	0.91	2.43	0.71



Fig. 9.11 Cross-sectional HRTEM image of a $(Cr_xSi_{1-x})_{1-y}N_y$ film with x = 0.2 and y = 0, unannealed

9.3.2 Temperature Dependence of Resistivity

Two systems were investigated in this study:

- $Cr_x(SiO)_{1-x}$ with various x values
- $(Cr_xSi_{1-x})_{1-y}N_y$ with fixed x and various y values

It can be seen that the metal-insulator transition occurs by choosing proper x or y values. There are lots of data available on the first system, but this study was the first investigation on the $(Cr_xSi_{1-x})_{1-v}N_v$ system.

The conductivity of the Cr-Si-N(O) films depends on temperature, Cr concentration, and deposition conditions. In this system, the concentration x of the Cr is increased from zero; at a certain value of x, the film structure changes from the dielectric regime to the metallic regime. It also can be explained that the states at the Fermi level become delocalized and a transition to the metallic state occurs.

Three regions (metallic, semiconducting, and transition) can be distinguished in the temperature dependence of the conductivity. The results for the Cr-Si-N system with [SiO]/[Cr] = 40/60 for various nitrogen concentrations, C_{N2} , are shown in a R $(T)/R_0$ versus logT plot in Fig. 9.12a and log(R(T)) versus $T^{-1/2}$ in Fig. 9.12b. The sample with nitrogen concentration $C_{N2} = 2.6\%$ is metallic, whereas samples with $C_{N2} = 26\%$ and 40% are semiconducting, and the sample with $C_{N2} = 12.6\%$ should be classified as in the transition region. The results for the Cr-Si-N system with [SiO]/[Cr] = 80/20 for various C_{N2} are shown in a $R(T)/R_0$ versus logT plot in Fig. 9.13a and R(T) versus log $T^{1/2}$ plot in Fig. 9.13b: samples with $C_{N2} = 2.6$, 12.6, 26, and 40% are all to be classified as semiconducting. The conductivities are shown as logR versus $T^{-1/2}$ plots in Figs. 9.12b and 9.13b. The semiconducting samples are well described by



Fig. 9.12 Cr-Si-N system with [SiO]/[Cr] = 40/60: (a) $R(T)/R_0$ versus logT and (b) log(R(T)) versus $T^{-1/2}$



Fig. 9.13 Cr-Si-N system with [SiO]/[Cr] = 80/20: (a) $R(T)/R_0$ versus logT and (b) log(R(T)) versus $T^{-1/2}$

$$\sigma(T) = \sigma_1 \exp\left\{-\left(\frac{T_0}{T}\right)^{1/2}\right\}$$
(9.6)

(where σ_1 and T_0 are constants) over only certain temperature regions, indicating again that the variable range hopping theory is not applicable to all cermet systems. It can be seen that the results are qualitatively similar for both systems, but the semiconducting behavior for the silicon-to-chromium ratio of 40/60 sets in at much higher nitrogen concentrations than for a silicon-to-chromium ratio of 80/20. The decrease in σ_1 with increasing nitrogen concentration and increasing T_0 should be noticed in Figs. 9.12b and 9.13b. This is one important difference from the behavior of the binary system Cr_xSi_{1-x} , in which σ_1 in the semiconducting region is the same for all as-deposited samples. Annealing has opposite effects on σ_1 between the binary systems where the semiconductor transition sets in at much higher nitrogen concentrations than for a silicon-to-chromium ratio of 80/20 and 40/60. Annealing the Si_{1-x}Cr_x samples leads to a decrease in σ_1 for the [SiO]/[Cr] = 40/60 system but an increase in σ_1 for the [SiO]/[Cr] = 80/20 system. The change of σ_1 can be interpreted as a consequence of the formation and growth of metallic clusters. In this interpretation, the size of metallic clusters in Cr-Si-N films should increase with increasing T and at much higher nitrogen concentrations C_{N2} . The increase in T_0 with C_{N2} implies an increase in the distance between the metallic clusters. Thus the dependence of the parameters T_0 and σ_1 of Eq. (9.6) on C_{N2} can be explained by an increase in both the average size and the separation of the metallic clusters with C_{N2} .

Note that Neugebauer demonstrated consistency in resistivity variations with composition between M-SiO and M-SiO₂ cermets (where M represents a variety of metals), if the M-SiO data is reinterpreted as $M/Si-SiO_2$ [28], i.e., if the excess Si is regarded as adding to the metallic content. Cr cermets were included in the study but are significantly more complex than the noble metal cermets, due to the formation of Cr silicides and oxides.

9.3.3 I–V Characteristics

There are two kinds of test structures, lateral and vertical, on which I-V characteristics were measured. Figure 9.14 shows these two structures schematically. Figure 9.14a shows the lateral test structure, and Fig. 9.14b shows the vertical one. For the lateral structure, two Al electrodes $50 \times 100 \,\mu\text{m}$ and 110 nm thick were first



Fig. 9.14 (a) Lateral and (b) vertical test structures for *I*–*V* characteristics



Fig. 9.15 I–V characteristics of a vertical $Cr_x(SiO)_{1-x}$ granular film test structure at different test temperatures

deposited onto a Si substrate through a mask. A $Cr_x(SiO)_{1-x}$ film was then deposited by co-sputtering SiO and Cr. The volume fraction of Cr was controlled by varying the number of Cr strips placed on a Si target during the co-sputtering. The thickness of the film was varied from 10 to 15 nm. The substrate was kept at ambient temperature during the sputtering. For the vertical test structure, a bottom electrode is deposited first, and then the $Cr_x(SiO)_{1-x}$ film is deposited.Figure 9.15 shows typical *I–V* characteristics of a vertical $Cr_x(SiO)_{1-x}$ granular film test structure shown in Fig. 9.14b. The thickness of the $Cr_x(SiO)_{1-x}$ film is about 10 nm. As the temperature decreases, step-like structures appear in the *I–V* curve. Similar step-like *I–V* curves have been reported for the system containing nanoparticles [29–31]. The observed step structures can be explained by the Coulomb blockade (CB) and Coulomb staircase (CS). Electron transport between metal Cr islands is by thermally activated tunneling. When tunneling occurs, the charge on the island suddenly changes by the quantized amount, *e*. The associated change in the Coulomb energy is conveniently expressed by the approximate form of Eq. (9.2):

$$\delta E = \frac{e^2}{4\pi\varepsilon_0\varepsilon_r r} \tag{9.7}$$

where $\varepsilon_r = 3.8$ is the relative dielectric constant of the SiO₂. From the TEM images, it can be seen that a typical island radius $r \approx 2$ nm. The charging energy is ~0.59 eV, which is easily resolvable even at room temperature. However, in present samples, the electron transport across the film occurs via Cr islands. Since the device size is very large (50 × 50 µm), a very large number of parallel local current paths exist between the two electrodes. In each current path, there are only a few metal islands,



Fig. 9.16 *I–V* characteristics of a lateral $Cr_x(SiO)_{1-x}$ granular film test structure at different test temperatures: (a) 293 K, (b) 250 K, (c) 180 K, (d) 120 K, and (e) 77 K

assuming evenly distributed Cr islands with diameter ≈ 2 nm and gap sizes between islands ≈ 1 nm, n < 3. The local transport property of each path will be controlled by the charging energy of the islands contained in it, and the CB and CS structures will appear on the *I*–*V* curve of each local path. Such local transport properties of granular metal films can be studied by STM, and the observation of CB and CS structures has already been reported [32–34].

In contrast to the previous local transport measurements by scanning tunneling microscopy (STM), the I-V curves obtained from the lateral test structure, shown in Fig. 9.16, reflect the macroscopic conductance of the whole system. If each local path in a large device has a similar conductance, the CB and CS structures observed for many paths will be smeared out by averaging the conductance of many paths. On the other hand, if the conductance of the local paths is distributed over many orders of magnitude, the macroscopic conductance of the films under low bias voltage is considered to be determined by a special path with the largest conductance. In this case, the CB and CS structures are expected to be observable even for a macroscopic size device. The current-voltage characteristics obtained in this study yield a power-law dependence over a wide temperature range. The steady-state current may be expressed as a function of bias voltage V and temperature T:

$$I = f(V, T) \tag{9.8}$$

The total derivative is

$$dI = \frac{\partial I}{\partial V} \Big|_{T} dV + \frac{\partial I}{\partial T} \Big|_{v} dT$$
(9.9)

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The term

$$g_T = \frac{\partial I}{\partial V}|_T$$

is the small signal conductance at constant temperature. From Figs. 9.13 and 9.16, for constant bias voltages,

$$I|_V = m_1 T + I_0 \tag{9.10}$$

$$g|_V = m_2 T + g_{0V} \tag{9.11}$$

From Fig. 9.16, for constant temperature,

$$g|_T = m_3 V + g_{0T} \tag{9.12}$$

where m_1 , m_2 , m_3 , I_0 , g_{0V} , and g_{0T} are small signal constants. Substituting in Eq. (9.9) yields

$$dI = (m_3 V + g_{0T})dV + m_1 dT (9.13)$$

assuming $g_{0T} = 0$, and hence,

$$I = m_3 \frac{V^2}{2} + m_1 [T(V) - T(0)]$$
(9.14)

This equation would be expected to hold over the linear regions of the above results. However, it would not be expected to hold for bias voltages approaching 0 V or for higher temperatures. Equation (9.14) can also be rewritten as

$$I = AV + BV^2 \tag{9.15}$$

where *A* and *B* are temperature-dependent constants. This dependence suggests that the total current consists of two components, one ohmic in nature and the other more akin to a space charge-limited flow. The tunneling process between islands can be expressed by rewriting Eq. (9.8) as follows:

$$I(V,T) \propto V \exp(-\delta E/kT)$$
 (9.16)

which corresponds to the ohmic term in Eq. (9.15). Now, if there is a capacitance C_g associated with the two metal particles, then a space charge will exist in the dielectric given by

$$Q = C_g V \tag{9.17}$$

where V is the voltage drop between the islands. Assuming that this charge can move in the insulator by a tunneling process between traps, then the space charge contribution to the current is given by

$$I_s = C_g V / \tau \tag{9.18}$$

where τ is the transition time. τ is inversely proportional to the transmission probability *D*, which is directly proportional to *V*. Thus we arrive at the relationship:

$$I \propto V^2 \tag{9.19}$$

Equations (9.16) and (9.19) can be combined to give an overall I-V characteristic of the form suggested by Eq. (9.15). The observed temperature dependence above can be explained well by the tunneling theory by taking into account the electrostatic charging energy of metal islands.

The Coulomb blockade (CB) suppression of the current around the zero voltage region is clearly observed from the current-voltage (I-V) characteristics in Figs. 9.15 and 9.16, especially at the low-temperature measurements at 77 K. It is also found that the observed structures in I-V curves vary from one sample to another, even for samples prepared under the same conditions. This suggests that the transport in metal granular films is a highly selective process and that the transport is dominated by only a few special paths with the largest conductance. In Fig. 9.15, I-V curves are shown for the vertical sample. A Coulomb blockade and the Coulomb staircase step structure with a periodic step width of about 10.4 mV are clearly seen. Each step corresponds to the incremental charging of a nanoparticle by a single electron. The step width of 104 mV (>> kT) corresponds to a capacitance of 1.6×10^{-18} F. Since the tunneling resistance is very sensitive to the barrier width, the current path with the largest conductance is expected to contain a particle whose size is in the largesized tail of the particle size distribution. The diameter of the largest particle that was found from the HRTEM image of Fig. 9.17a (plane view) and Fig. 9.17b (crosssectional view) is about 5 nm. Taking the dielectric constant of the SiO₂ barrier as 3.9, the capacitance of a Cr nanoparticle with respect to the Al electrode is estimated to be 1.5×10^{-18} F by the image charge method, which is in good agreement with the experimental value. The agreement supports that the macroscopic conductance of sample 1 is governed by a single path containing a serial connection of two Cr nanoparticles of about 5 nm diameter.

9.4 Integrated Resistors: Fabrication and Properties

Electronic devices, components, circuits, and systems should be faster, smaller, lighter, and cheaper. Proper functionality of modern electronic circuits demands both active devices and passives (primarily resistors, capacitors, and inductors but also nonlinear resistors – thermistors and/or varistors, potentiometers, etc.). About 10^{12} of passives, which undergo deep technological and constructional transformation, are used by the electronic industry every year. The aim of this chapter is to present the current situation in the area of surface and embedded (buried) passives made with different microelectronic technologies – thick-film (TF), low-temperature co-fired ceramics (LTCC), and printed circuit board (PCB). Integrated passive

Fig. 9.17 HRTEM

view; (b) cross section



technology is the best for very high component density with increased electrical performance, improved reliability, reduced size and weight, and lower cost. Replacing surface mount devices by embedded passives will lead to the reduction of overall part count, elimination of solder joints, and improvement of wireability and frequency due to elimination of parasitic inductance. The material, technological, and constructional solutions and their relation with the electrical and stability properties chosen are analyzed in detail for modern embedded microresistors, both described in the literature and self-fabricated and/or characterized. The role of such components in modern electronic circuits is also discussed.

9.4.1 Electrical and Stability Properties of Surface and Buried Thin- and Thick-Film Resistors

9.4.1.1 Miniaturized Surface Thick-Film Resistors

Miniaturization is the crucial problem in all electronic applications. Demand for the continuous reduction of dimensions is caused by a number of factors: one is the cost reduction, and another is the necessity for permanent circuit speed increases due to





ever more sophisticated applications operating at higher frequencies. Thick-film technology has been well known for many years. It has many advantages on its side, like low cost and durability, but many of these pluses are outweighed by one major disadvantage, namely, large planar dimensions. A few years ago, a new class of photosensitive inks emerged, promising further downscaling of passives. Resistors made with such materials were studied in [35]. Although usage of these inks may significantly reduce passives' dimensions, the systems covering the full spectrum of necessary inks (conductive, resistive, dielectric) are commercially not available, and probably for long time, the technology described will not be considered to be a standard one. In the research presented here, classical manufacturing processes were supported with highly nonclassical production methods involving lasers as the main tools for structure shaping. Similar approaches to miniaturization are described, for example, in [36, 37].

The first group of samples were fabricated by an initial screen printing process, with the use of three different conductive inks: Ag, Au, and PdAg. After firing, conductive paths were laser-cut in order to form small (30–300 μ m) electrode gaps (Fig. 9.18a). This procedure defined the length of resistors. The last step involved screen printing of resistive inks over conductive paths. In this process, resistor bodies were formed within the laser-made gaps (Fig. 9.18b). For technology control purposes, passives were prepared of typical planar dimensions with lengths defined in an initial conductive layer screen printing on the same substrate as the laser-made resistors. Similar steps have been undertaken for fabrication of samples characterized by minimized resistor widths. Here resistors of typical lengths and widths have been made and cut after screen printing and firing with laser beam along their lengths, as shown in Fig. 9.18c, in order to produce extremely tight structures.

Commercial DuPont inks with 100 Ω /sq (DP2021) and 10 k Ω /sq (DP2041) sheet resistance were used. For manufacturing of resistor structures with very small widths (down to 30 µm), other resistive DuPont inks – DP6620 (100 Ω /sq) and DP6641 (10 Ω /sq) – were used. Test samples were made on alumina as well as on LTCC substrates (DP 951).



Fig. 9.19 Sheet resistance vs. resistor's length

Measurement of resistance made calculations of real sheet resistance ($R_{sq.}$) possible. Some characteristics showing calculated R_{sq} are given in Fig. 9.19. Results show that short, laser-made resistors exhibit smaller sheet resistance values in comparison with nominal ones. The observed decreases of sheet resistance could be explained by the simple fact that in fabrication of very small resistors, bulges appear close to their contacts, because resistor lengths in this case are so small that the effect mentioned leads to considerable increase of resistor thicknesses. This affects sheet resistance making it lower than expected. Moreover the diffusion of conducting material from paths into resistor bodies also contributes to this effect.

On the other hand, resistors cut in length are characterized by higher sheet resistance than nominal for the inks applied (Fig. 9.20). It is supposed that in this case, the so-called heat-affected zone, i.e., the region very close to the laser beam cut, changed its properties in such a way that its resistivity was increased in comparison with unaffected region of the resistive layer.

Further investigations brought results on the *TCR*. Extremely short resistors show *TCR* increases in comparison with the longer ones (Fig. 9.21). This proves the existence of normal dimensional effects caused by diffusion of metallic grains from contacts into the resistor body. However, resistors with constant length but various widths (prepared by laser scribing of resistive film) have almost constant values of *TCR* (Fig. 9.22).

Long-term stability was evaluated with the aging process conducted in a climate chamber in which samples were stored at 150 °C for 150 h. All structures were aged under the same conditions. Figures 9.23 and 9.24 present resistance changes after aging. As it is shown in these figures, most small resistors suffered resistance change, within the range $\pm 1\%$. It seems that the type of conductive ink and



Fig. 9.20 Sheet resistance vs. resistor's width



Fig. 9.21 TCR vs. resistor's length



Fig. 9.22 TCR vs. resistor's width



Fig. 9.23 Relative resistance change vs. resistor's length (DP2021)

resistor/conductor interface is very important for long-term stability properties of miniaturized resistors. Passives made with an Au-based ink have better stability than those involving Ag or PdAg.

It is possible to conclude that tight-shaped resistors obtained in combined manufacturing processes are characterized by somewhat better parameters than



Fig. 9.24 Relative resistance change vs. resistor's length (DP2041)

those exhibited by short structures. Nonetheless, the resistors examined with reduced planar dimensions are somewhat worse from the point of stability and other parameters than standard-sized passives, described in [38]. Although mentioned disadvantages of microresistors have to be taken into account in practical applications, it is shown that further miniaturization of thick-film resistors is still possible, beyond today's boundaries even with the use of standard material.

9.4.1.2 Embedded Resistors in LTCC Substrates

Multichip modules (MCM) are an extension of hybrid technology, which permits a higher packaging density than can be assured by other approaches. Modern MCM substrates consist not only of interconnection lines but also of many integral (embedded) passives. In this manner they fulfill the demands for the next generation of packaging needs. The development of low-temperature co-fired ceramics (LTCC) technology has enabled embedding (burying) passives (resistors (Fig. 9.25), capacitors, inductors) within a ceramic substrate in a single firing step. The composition of low-temperature ceramic tapes is similar to most screen-printed low permittivity thick-film dielectrics. But the organic resins and binders are different to permit the slurry to be cast and dried into tape. These tapes typically consist of glass compounds mixed with alumina or silica. They possess properties of both ceramics and glasses. LTCC substrates offer hermetic and reliable packaging with the possibility to have multiple layers and high-density internal interconnections.



Fig. 9.25 Schematic cross section of surface and buried microplanar (left) and microvolume (right) LTCC resistors

Table 9.5 Comparison of electrical parameters of surface co-fired (SC) and buried (B) resistors (resistor dimensions $-1.5 \times 1.5 \text{ mm}^2$)

Paste	Substrate	Description	Resistance [Ω]	Noise index S ^a	Noise exponent γ^{b}
DP8039	DP951	L8039SC	5830	20.6	1.004
DP8039	DP951	L8039B	27,411	40.6	0.980
DP2041	DP951	L2041SC	6869	4.80	1.016
DP2041	DP951	L2041B	34,943	7.64	0.990

^a $S = \langle fS_V \rangle / V^2$ (in units of 10⁻¹⁵ 1/Hz)

^bWe have the following relationship: $S_V = S \cdot V^2 / f^{\gamma}$

The physical and chemical compatibility between different materials is one of the most important matters during co-firing of passive components and ceramic tapes [39, 40]. One example is the different shrinkage and mismatch of thermal expansion coefficients of buried (resistive) material and dielectric surround. Another example is the possibility of chemical reactions between these two materials. All these issues are systematically studied, and the progress in understanding the relation between microstructure and electrical properties of buried resistors is continuously being made [41]. Experimental and theoretical approaches mostly concern resistivity and its temperature dependence, and the behavior at high frequencies and under DC voltages, or noise properties of resistors buried resistors shows that embedding a resistor within a LTCC substrate usually leads to significant enhancement of resistance but not (or weak) of noise intensity [42]; selected examples are presented in Table 9.5.

The standard long-term thermal aging test (500 h or 1000 h at 150 °C) is unselective for modern thick-film or LTCC resistors because the relative changes in resistance are within the $\pm 0.2\%$ range, independently on technological variants. Therefore, the step-aging profile was used for analysis of the relative changes in resistance and changes in hot temperature coefficient of resistance (*HTCR*) versus storage time and temperature [44, 45]. (After 200 h aging at a specified temperature, followed by measurements of resistance and *TCR*, the temperature was raised in the next step by about 50 °C, with the same samples held in these new conditions for the next 200 h and measured.) The above aging procedure was repeated for 96, 162,

Aging conditions		200 h/					
Resistors	Changes	96 °C	162 °C	207 °C	253 °C	300 °C	350 °C
L2041SC	$\Delta R/R_0$	+0.02	+0.12	+0.37	+0.73	+0.50	-1.73
	$\Delta HTCR$	-5	+7	+7	+15	+5	-6
L2041B	$\Delta R/R_0$	-0.02	+0.05	+0.02	+0.06	-0.28	-1.06
	$\Delta HTCR$	-3	-6	+1	-7	+5	0
ESL3414 B, SC	$\Delta R/R_0$	+0.02	+0.09	+0.12	+0.41	+0.49	+0.10
	$\Delta HTCR$	-3	-4	-2	-3	-3	-20
ESL3414 B, buried	$\Delta R/R_0$	-0.03	-0.02	-0.01	+0.06	-0.02	-0.10
	$\Delta HTCR$	-2	-3	-7	-5	+2	+6

Table 9.6 Comparison of relative changes of resistance (in %) and changes in *HTCR* (in ppm/°C) for thermally aged surface and buried LTCC resistors

207, 253, 300, and 350 °C, and the results were collected in Table 9.6. The embedded resistors were somewhat more stable than surface ones. The embedded CF021 (100 Ω /sq) and CF041 (10 k Ω /sq) resistors were extremely stable – they exhibit fractional resistance changes within the ±0.3% range and changes in *TCR* less than 20 ppm/°C, independently of processing conditions and aging temperature. Surface resistors exhibit slightly larger changes of fractional resistance and *TCR*. Similar stability levels are characteristic for DP2041 structures.

9.4.1.3 Thick-Film and LTCC Resistors at High-Temperature Operation

An increasing interest in high-temperature electronics (i.e., electronics operating above the "traditional" temperature range, which is equal to +125 °C for military electronics or +150 °C for automotive electronics) has been observed in recent years [46]. Some applications, for example, electronics for oil and gas exploration and production, distributed controls for aircraft, industrial process control, or even space exploration, operate at much higher temperatures. Recently thermal aging behavior at even much higher temperature was checked for microresistors with regulated length made on LTCC (DP951, 300 µm thick) substrates by combining standard screen printing and photoimageable techniques [47]. Conductive paths were prepared from Ag65 photosensitive ink [48]. The distance between electrodes, i.e., the proper resistor length, was designed as 90, 120, and 300 µm. The 200 µm width resistors from DP2021 (DuPont, 100 Ω/sq) or R490A (Heraeus, 10 Ω/sq) pastes were screen-printed through a 325 mesh screen. The conductive and resistive pastes were co-fired at 850 °C. Measurements of dynamic resistance changes at elevated temperature (so-called in situ measurements of long-term stability [49]) were performed directly. They were step-aged at 300, 400, and 500 °C. Examples of dynamic resistance changes are shown in Figs. 9.26 and 9.27. The elevated temperature caused decrease of resistance for the DP2021 resistors. The observed drift was about -1.75% at 300 °C. However, storage at 400 °C caused more significant



Fig. 9.26 Relative resistance changes for DP2021 resistors



Fig. 9.27 Relative resistance changes for R490A resistors

changes of resistance, up to -7%. The R490A resistors exhibit resistance drift of about $\pm 2\%$ at 300 and 400 °C. The results show that this chosen group of materials not only can be applied in consumer electronics at standard operating temperatures but also meet demands for high-temperature electronic application.



9.4.1.4 Polymer Thick-Film Resistors

Polymer thick-film resistors (PTFRs) are the example of composites consisting of insulator polymer matrix and conductive carbon filler (different kinds of carbon black (CB), graphite (G), or their blend). Thanks to simplicity and cheapness of fabrication, as well as interesting electrical properties, they are not only the subject of much research but are also widely and successfully applied in thick-film, printed circuit board, or laminated multichip module techniques [50–52]. These components have been used in electronics for almost 40 years, although their electrical properties are not equal to those of high-temperature cermet thick-film resistors. The main problems are related to stability, especially for humidity exposure and continuous storage at elevated temperature.

There are many kinds of CB. It should be classified according to "structure," i.e., granularity and dispersion ability [53]. The schematic morphology of high, medium, and low structure carbon black as well as flaky-shaped graphite is shown in Fig. 9.28 (very fine grains of HSCB can create complicated aggregates and agglomerates in the films).

This subchapter describes carbon/polyesterimide thick-film resistive composites. Polyesterimide (PEI) resin with high thermal durability serves as an insulating matrix, whereas medium structure carbon black (MSCB), a blend of MSCB and graphite (G), and high structure carbon black (HSCB) have been used as active phases. The chosen physicochemical investigations, electrical measurements (dependence of sheet resistance, hot *TCR* on kind and content of conductive filler, and curing temperature), and various stability tests have been used for complete descriptions of MSCB/PEI, (MSCB+G)/PEI, and HSCB/PEI thick-film resistor series.

The resistive inks have been prepared by the proper mixing of carbon black and/or graphite with PEI. Compositions with HSCB contents from 0.4 to 10 vol%, MSCB contents from 5 to 45 vol%, and MSCB + G contents from 10 to 40 vol% (50/50 blend of MSCB and flaky-shaped graphite) have been prepared. $5 \times 5 \text{ mm}^2$ resistors have been screen-printed on alumina substrates with Pd-Ag contacts and cured in an air-circulating box oven at 523 K, 573 K, or 623 K. The PEI-based films exhibit very interesting physicochemical and electrical properties for curing temperature range between 523 and 623 K. The electrical properties are primarily affected by the kind and contents of the active phase as well as the curing temperature. Both increasing the conductive filler amount and the curing temperature cause a decrease in sheet resistance and simultaneously drift of the HTCR toward more negative values [54]. Independently on the kind of carbonaceous filler, the changes of the basic electrical properties for particular resistor systems are larger for smaller concentrations of the active phase. One should note that the basic electrical properties of the HSCB/PEI system are much less sensitive for curing conditions than for the MSCB/PEI system.Carbon-polymer resistors and classical cermet thick-film compositions are both known as percolative materials. Percolation theory permits one to characterize (calculate) the effective properties of random inhomogeneous two-phase systems with comparable concentration of both phases (near the percolation threshold) but with significant differences in their properties. Experimental and numerical investigations have shown that effective conductivity σ_e is an analogue of the order parameter in the theory of phase transitions, where temperature T is replaced by the concentration of the well-conducting phase, p, and the critical temperature $T_{\rm c}$ is replaced by the percolation threshold, $p_{\rm c}$. There are three ranges of universal behavior of effective conductivity [55, 56], where separate equations describe a universal behavior of effective conductivity, above $(p > p_c)$, below $(p < p_c)$ p_c), and in the vicinity ($p \approx p_c$) of percolation threshold:

$$\sigma_{e} = \sigma_{1}\tau^{t} (A_{0} + A_{1}h\tau^{-(t+q)} + ...), p > p_{c}, \tau >> \Delta$$

$$\sigma_{e} = \sigma_{1}\sigma_{2} \left(D_{0} + D_{1}h^{-\frac{1}{t+q}} |\tau| + ... \right), |\tau| \leq \Delta$$

$$\sigma_{e} = \sigma_{2}\tau^{-q} (B_{0} + B_{1}h|\tau|^{-(t+q)} + ...), p < p_{c}, |\tau| >> \Delta$$

(9.20)

where Δ – smearing region (described below).

Clearly, the above equations consist not only of the basic components but also smaller ones. A_i , B_i , and D_i indicate constants, which according to absolute value are almost equal to one. It is interesting to become familiar with the concept of a smearing region, $\Delta = (\sigma_1^q \sigma_2^t)^{1/t+q}$ – it is such $|\tau|$, where good and bad conductive





phases provide equal contributions to the effective conductivity, i.e., $\sigma_1 \Delta^t = \sigma_2 \Delta^{-q}$. The qualitative behavior of σ_e is shown in Fig. 9.29. The above presented theory was successfully applied for analysis of temperature dependence of resistance and 1/f noise in percolation and percolation-like systems [57, 58]. The experimental dependence of the resistivity ρ (or sheet resistance R_{sq} in the case of film components) on the volume fraction v of the conductive phase is called the blending curve. It is commonly used in the analysis of the electrical properties of composites. Very often, the power law of Eq. (9.21) fits the blending curve

$$R_{\rm sq.} = R_0 (v - v_c)^{-t} \tag{9.21}$$

where R_0 is constant, v_c critical volume fraction of conductive phase, and *t* critical conductivity exponent above v_c . Therefore, sets of optimal v_c and *t* are looked for in various experimental data. Based on Eq. (9.21), the experimental data presented on log-log scales should lie near a line with slope -t. Sometimes it is assumed that the power law can be applied in the range from the percolation threshold p_c to $p_c + 0.2$ [59].

The optimal v_c and t values for $R(v_{CB})$ curves for systems based on high structure (HSCB) or medium structure (MSCB) carbon black are given in Table 9.7. Analysis presented in [60] gives experimental values of v_c between 0.0003 and 0.244 and t between 1.13 and 5.0 for other powder filler/organic matrix composites.

Values of R_0 range from tens to several hundred m Ω /sq for HSCB-based systems and about two orders larger for MSCB-based ones. This corresponds to resistivities from 2×10^{-6} to $6 \times 10^{-4} \Omega$ m, respectively, for nominal thickness of the film equal to 25 µm. Increase of curing temperature leads to decrease of conductivity index *t*. These changes are much larger for MSCB/PEI systems than for HSCB/PEI.

Moreover, Table 9.8 contains values of v_c and t for other powder filler/organic matrix composites.
Table 9.7Values ofparameters from Eq. (9.21)for HSCB/PEI andMSCB/PEI systemscured at varioustemperatures [54]		HSCB/PEI system			
	T _c [K]	R_0 [ohm/sq.]	v _c	t	
	523	0.070	0	3.110	
	573	0.275	0	2.647	
	623 0.264		0	2.554	
		MSCB/PEI system			
	T _c [K]	R_0 [ohm/sq.]	V _c	t	
	523	1.15	0.0737	3.652	
	573	7.31	0.0796	2.695	
	623	24.27	0.0841	1.755	

Table 9.8 Experimental values of critical volume fraction v_c and conductivity index *t* for conductive powder filler/organic matrix composites

Conductive powder filler + organic matrix	V _c	t	Ref.
Ketjenblack carbon black (HSCB) + high-density polyethylene	0.020	1.9	[<mark>61</mark>]
Asahi carbon black + high-density polyethylene	0.244	2.0	[<mark>61</mark>]
Ketjenblack EC300N carbon black + polystyrene	0.002	2.2	[62]
Graphite (aspect ratio $\cong 100$) + epoxy resin $\sigma_{=}$	0.013	2.5	[63]
Monarch 1100 carbon black (HSCB - 14 nm) + araldite F resin	0.005	2.0	[64]
Carbon fiber ($\Phi = 9 \ \mu m$, $l = 1000 \ \mu m$) + araldite F resin	0.0093	3.0	[<mark>64</mark>]
Carbon fiber ($\Phi = 9 \ \mu m$, $l = 3000 \ \mu m$) + araldite F resin	0.0024	2.9	[65]
Low structure CB (200 nm) + high-density polyethylene	0.170	2.9	[<mark>66</mark>]
SAKAP-6 carbon black (MSCB, surface area – 200 m ² /g) + polyesterimide (PEI) resin, $T_c = 523$ K	0.100	2.415	[<mark>67</mark>]
SAKAP-6 carbon black + PEI resin with TiO ₂ filler, $T_c = 523$ K	0.060	2.709	[<mark>67</mark>]
Graphite (aspect ratio ≈ 10) + PEI resin, $T_c = 523$ K	0.140	1.133	[<mark>67</mark>]
Vulcan P carbon black + linear low-density polyethylene	0.24	5.0	[68]
Ag (500 nm) + polystyrene	0.12	1.3	[68]
Pd (200 nm) + polystyrene	0.19	2.9	[68]
Ketjenblack high structure carbon black + polymer	0.0003	2.0 ± 0.2	[<mark>69</mark>]

Additionally, the stability properties have been qualified based on long-term thermal aging (423 K, 300 h) and long-term moisturization. The excellent long-term stability properties have been obtained for HSCB/PEI under different environmental exposures. In all cases the fractional resistance changes are much smaller than for the MSCB/PEI and (MSCB+G)/PEI systems. Long-term thermal aging at 423 K (extremely high temperature for PTFRs) causes resistance to decrease by only about 1.0–1.5%, and long-term moisturization leads to a 1.5% resistance increase at 85% relative humidity. This is approximately five times less than for MSCB-based systems.

The results presented prove that carbon/polymer thick-film microcomposites are and will be useful in the fabrication of the next generation of passive components.

9.4.1.5 Embedded Passives in Printed Circuit Boards

The first trials of embedded capacitors and resistor started in the 1960s or early 1970s of the last century [70, 71]. Up to the present day, many materials which can be used for passives were elaborated, but the technology is only used in a limited range. But nowadays the miniaturization of conventional passive electronic components is reaching its limits, and the next obvious choice is to integrate them with the PCB. The embedding of passives into PCBs allows further miniaturization, has the potential to reduce cost, and moreover exhibits superior electrical behavior with respect to the minimization of parasitic effects. The use of passive components also gives environmental benefits. They have no package, and by minimizing the size of the PCB, they allow reduced amounts of waste. There is less consumption of energy and solder for solder processing after the component transfer into the PCBs. Embedded component manufacturing technologies are consistent with the manufacturing technology of PCBs (subtractive technologies are used which are practically nonhazardous for the environment at the present state, and the others use additive technologies which are environmentally friendly). It seems that this technology will be more frequently used in the near future.

Currently, the number of available materials for embedded passive manufacturing is growing [72]. The materials for thin-film resistors generally have a thickness below 1 μ m. Several materials (alloys), characterized by a relatively good chemical resistance and constant surface resistivity (dependent on the layer thickness and composition), are used. The following ones can be mentioned among them:

- NiP alloy electroplated onto the copper foil permitting resistor manufacturing by subtractive processing (Ohmega-Ply RCM from Ohmega Technologies, sheet resistance from 10 to 250 Ω /sq)
- NiP plated directly onto the inner layer through an additive process (M-Pass from MacDermid, sheet resistance 25–100 Ω/sq)
- NiCr alloy, nichrome-aluminum silicon, and CrSiO film (sheet resistance between 25 and 1000 Ω /sq) from Ticer Technologies
- Doped platinum deposited on copper foil (InSite from Rohm and Haas (Shipley), sheet resistance from 50 to 1000 Ω/sq)

A next-generation material, allowing simultaneous formation of both resistors and capacitors within the PCBs, also appeared on the market recently.

The stability of such thin-film resistors was determined based on relative resistance changes during aging tests. Two types of Ohmega-Ply laminate were used for fabrication of structures with resistive layer thicknesses of 0.4 µm and 0.1 µm (sheet resistance 25 Ω /sq and 100 Ω /sq, respectively). The rectangular resistors, with widths from 0.25 to 1.5 mm and aspect ratios n = l/w between 1 and 4, were designed and fabricated. Moreover, parts of the samples were covered with two types of cladding: resin-coated copper (RCC) or Laser Drillable Prepreg (LDP) 2×106 . The cladding gives additional protection from environmental conditions. In this case, test samples were placed on a hot plate with constant temperature:



Fig. 9.30 Relative resistance changes for Ni-P 25 Ω /sq resistors with LDP 2 × 106 (*left*) and RCC (*right*) claddings

Table 9.9 Activation energy for long-term thermal aging of Ni-P 25 Ω/sq thin-film resistors

Cladding	Without		LDP 2 × 106		RCC	
Length	1 sq	4 sq	1 sq	4 sq	1 sq	4 sq
<i>E</i> [eV]	0.40	0.42	0.34	0.33	0.27	0.27

100, 130, or 160 °C. Resistance drifts of tested resistors in the time domain are shown in Fig. 9.30. The results revealed a square root of time dependence of resistance changes. A single aging mechanism occurs here, which can be described by the following equation [73]:

$$\frac{\Delta R}{R_0} = At^n e\left(-\frac{E}{kT}\right) \tag{9.22}$$

where A is the pre-exponential constant characteristic for particular aging mechanism, t is time, n is the time dependence (and is about 0.5), E is the activation energy, k is the Boltzmann constant, and T is the temperature. The activation energy of the aging process can be calculated using the approximation of results presented on Arrhenius plots

$$\ln\left(\frac{\Delta R}{R_0}\right) = \ln(A) + n \cdot \ln(t) - \frac{E}{k} \cdot \frac{1}{T}$$
(9.23)

where the activation energy is a slope of linear function, which fits results. Computed values are shown in Table 9.9.

In case of these resistors, their long-term stability is almost not affected at all by their geometry. However, the type of encapsulation and aging temperature significantly affect the observed resistance drift; cladded structures exhibit much smaller activation energy, and this suggest weaker changes vs aging temperature. Another comparison of thin-film resistors embedded into PCBs concerns their pulse durability (determined by calculating the maximum nondestructive electric field, maximum



Fig. 9.31 Maximum nondestructive volume power density for Ni-P resistors (100 Ω /sq), $t_{imp} = 1$ ms

	E _{max} [V/mm]			P _V [W/mm ³]		
	100 Ω /sq, 2 × 1 mm, cladding			100 Ω /sq, 2 × 1 mm, cladding		
Pulse time [ms]	None	2×106	RCC	None	2×106	RCC
0.01	5.6	10.8	11.8	2.9E + 5	1.1E+6	1.4E+6
0.1	4.0	7.9	7.5	1.6E + 5	5.8E+5	5.6E+5
1	3.1	5.1	5.0	9.1E+4	2.1E+5	2.1E+5
10	1.8	2.7	2.5	2.9E+4	6,1E+4	5.9E+4
100	1.0	1.5	1.3	1.1E+4	1.9E+4	1.7E+4
1000	0.6	0.8	0.7	3.9E + 3	5.0E+3	4.9E + 3
10,000	0.5	0.6	0.6	2.3E+3	3.0E + 3	2.8E+3

Table 9.10 Maximum nondestructive electric field E_{max} [V/mm] and volume power density P_V [W/mm³] as a function of pulse duration

nondestructive surface power density (Fig. 9.31), or maximum nondestructive volume power density).

The maximum nondestructive pulse amplitude decreases for thin-film resistors with reduced length and width. However, other parameters increase their values when dimensions of resistors decrease. Cladding affects pulse durability. Coated structures have better durability than uncovered ones. In most cases the LPD 2×106 cladding gives the best pulse durability. Pulse durability decreases very quickly with increase of pulse duration (Table 9.10).

The results of measurements, advanced characterizations, and analyses presented above for thin-film resistors embedded in PCB, as well as other investigations not discussed in this chapter (e.g. [74, 75]), confirm that such passives exhibit basic electrical properties and long-term thermal stability at levels acceptable for many consumer applications. Moreover, in many cases, parameters of embedded passives prevail over surface ones. Therefore, this technology will be used in the near future more frequently.

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Chapter 10 Inductors: Micro- to Nanoscale Embedded Thin Power Inductors



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10.1 Introduction

Electronics is traditionally driven by transistor scaling. However, this created a huge gap between the device scale that is driven by transistors and the system scale determined by system components such as passives. Presently high-end electronic systems are composed of almost 90% passive components, taking up almost 70% of the total board area. To address the gap, the emerging trends for smartphones, IOTs, wearables, and all other small systems requires major breakthroughs in passive component technologies. This requires an entirely different set of materials to enable system functions that include digital, optical, thermal, RF, mm wave, power, and many others. This chapter focuses on inductors as key system components and their migration to nanoscale for better performance and densities.

"Inductor" is a generic term for components having specific inductance that can be used to store energy in the form of a magnetic field [1]. They are used in a wide range of power supply applications including dc-dc converters, voltage regulator modules, and point-of-load (POL) converters. They are of the utmost importance for high-frequency applications, especially in wireless/radio communication devices.

Inductors in Power Applications Increased power states and their variations in emerging electronic systems are driving the need for integrated power supply modules in 3D architectures for efficient power management. Integrated voltage

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regulators reduce the interconnect power losses by reducing the interconnect length and also delivering power at higher voltage and lower current to the point-of-load (POL) converters. They also reduce the need for passives by increasing the switching frequency and saves power by better per core voltage control. Delivering noise-free power with the required voltage and current levels is a major barrier to such systems, both for performance in terms of power efficiency and bandwidth and system miniaturization in terms of thickness and X-Y dimensions.

Several voltage regulators and noise filters are incorporated between the power source and device load in order to regulate the power supply. These regulators consist of a network of switches and storage components such as capacitors and inductors that transfer power to the load at the desired levels. The key size, performance, and cost barriers in integrated voltage regulators arise from the lack of suitable magnetic materials with required properties such as permeability, loss frequency stability, and current handling. Today's inductors for power supply are either surface-mounted or integrated in the package or on chip. They are primarily based on ferrites and are surface-mounted as discrete components. This results in higher parasitics, thus degrading system performance. A ferrite inductor of $\sim 1.8 \times 1.12 \times 0.91$ mm³ has inductance of up to 1.5 microhenries and a quality factor (O) of 15 at 1–10 MHz [1]. Their larger component thickness creates additional challenges with respect to component embedding. Most high-permeability ferrites are usually stable up to 5 MHz, as suggested by the Snoek's limit, which further limits their performance. Advanced magnetic materials with high power density and high Q can transform these bulky components to planar thin film components. However, these magnetic materials need to be enhanced to handle high output currents without inducing process complexity and cost.

Inductors in RF Applications Inductors form the key building blocks for passive networks that are applied to matching networks, filters, diplexers, etc. Inductor integration in RF modules traditionally evolved with low-temperature co-fired ceramic (LTCC) substrates. The primary reason is the superior properties of LTCC such as low dielectric loss, low moisture absorption, high reliability based on the hermetic nature of ceramics, high temperature stability, and ability to form complex 3D multilayered circuits. The technology eventually migrated to organic laminate packaging because of cost and higher component density from fine-line multilayered wiring. In spite of the advances in designs, inductor miniaturization with high Q is a major challenge that requires advances in new nanomagnetic materials with low loss and high frequency stability.

Air core inductors are generally preferred over magnetic core inductors, where loss is of significant concern and the required inductance densities are low. For high inductance densities with low losses, magnetic cores are inevitable. Such cores should have high permeability to achieve inductance, high saturation magnetization to avoid decrease in the inductance at high currents, low coercivity, high resistance to avoid eddy current loss, and high frequency stability in order to significantly decrease the number of windings needed to achieve the required inductances and thus could catalyze the effective miniaturization of devices. Small length scales leading to enhanced exchange coupling and ease of tailoring properties through additional degrees of freedom make nanogranular magnetic materials an attractive choice in achieving a high degree of compactness for such high-performance devices [2]. The enhanced properties at nanoscales, however, do not fit well with the classical theory of magnetism. Significant works on modeling of local anisotropy and exchange interactions between constituents in nanostructures by Herzer et al. are important in this regard [3, 4].

This chapter presents a comprehensive review of inductor research, including design, materials, and fabrication, with special attention to recent advances in nanogranular magnetic materials for high-performance inductive cores. It provides insights into the evolution of magnetic nanomaterials with better properties using innovative synthesis techniques [2]. Furthermore, the translation of research into high-volume products can only be possible if scalable and cost-effective fabrication processes are developed. Fabrication processes for micro- and nanoinductors are described in the last part of this chapter.

10.2 Inductor Design

Performance of a device depends upon two key factors – design and inherent material properties. Innovative designs benefitting from advanced materials, structures, and fabrication processes can dramatically enhance the performance of devices, which would not be possible with just simple designs backed up by standard material properties. Number of turns, width of metal traces, spacing between them, and inner and outer diameters are some of the important design parameters. Various designs have been proposed to achieve high quality factors. This section reviews some of the important designs.

10.2.1 Spiral Inductors

Spiral inductors are comprised of two-dimensional copper windings and are the most widely studied, which can be attributed to their high-efficiency and simple fabrication process. This design renders a very high quality factor due to the ease in attaining very large core cross-sectional areas. Air core and magnetic core spiral inductor designs have been studied by various researchers. Yamaguchi et al. proposed variations in the design, including closed magnetic circuit-type spiral inductors [5], sandwiched spiral inductors [6], on-top-type ferromagnetic spiral inductors [7], microslit spiral inductors [5, 8], and surface planarized spiral inductors [8]. They also reported various patterned spiral inductors for better performance [5]. A number of magnetic cores have been studied with spiral inductors, including Co-Zr-Nb [9], Co-Fe-B [10], Co-Fe-B-N [11], and Fe-Hf-N [12]. A quality factor of more than ten was reported for all these inductors. Spiral inductors are designed in different shapes including square, hexagonal, octagonal, and circular [13]. Figure 10.1 illustrates



Fig. 10.1 Schematics of polygonal spiral inductors: (a) square, (b) hexagonal, and (c) octagonal (© IEEE 1999) [13]



Fig. 10.2 Comparative extracted quality factors of 3 nH square and octagonal spiral inductors (© IEEE 2005) [14]

schematics of some of them. Polygonal spiral inductors have been reported to render higher quality factor and performance.

For RF spiral inductors, Hizon et al. have proposed several polygonal designs of monolithic spiral inductors for very-high-frequency applications [14]. Figure 10.2 illustrates the comparison between the performances of square and octagonal inductors. As is evident, the quality factor of octagonal spirals is higher than that of square

spirals due to small series resistance that is extracted in octagonal spiral inductors. Octagonal structures have also been reported to have lower shunt capacitance because of their more hollow structure.

Inductance (L) of a spiral inductor depends on several parameters including the number of turns (N) and fill ratio (R_{Fill}) that is defined as the ratio of the difference between outer and inner diameters to the average diameter (D_{Avg}) [13], as is evident from Eq. 10.1.

$$L = \rho_L N D_{Avg} \ln \left(8 R_{Fill} \right) \tag{10.1}$$

where ρ_L is a material-dependent constant. Therefore, an optimization of all the abovementioned parameters is necessary to insure high performance of the device.

10.2.2 Spiral Sandwiched with Magnetic Composite Films

The need for miniaturized inductors with low dc resistance and high rating current has stimulated research in thin film composite inductors. Yamaguchi et al. proposed sandwich structures to increase the quality factor of the inductor [6]. The Vishay Group makes high-quality inductors by pressing low-permeability iron-resin composites and magneto-wire coil together [15]. The iron powder, however, has been reported to be very prone to oxidation and thus requires a passive layer. Also the inductor is very thick (3 mm), which limits the size of the device [15]. Kowase et al. proposed a composite magnetic core of Mn-Zn ferrite/polyimide to avoid this problem [16]. This film was reported to have very large saturation magnetization (M_s) of about 2 kG and was still not saturated even at large magnetic fields up to 2.5 kOe. The proposed structure consisted of two designs: Type 1 with an inner square spiral coil between a top and bottom composite magnetic film core and Type 2, a planar inductor with the same spiral core between a top composite magnetic core and a bottom 1-mm-thick Ni-Zn ferrite substrate. The design is schematically illustrated in Fig. 10.3.

It was found that the inductance increased with the film thickness. For Type 1 the saturation was reached at 300 μ m, whereas the Type 2 planar inductor still recorded increases even at thicker conditions. This difference is attributed to the high-permeability ferrite substrate layer. They also reported larger than a threefold increase in inductance in Type 2 as compared to the air core inductor as evident from Fig. 10.3c. The quality factor also improved (Fig. 10.3c).

10.2.3 Toroidal Inductors

Toroidal inductors comprise of a continuous magnetic loop with a copper winding wrapped around them. Most discrete inductors are based on such toroidal designs. Such designs can saturate at very low currents, which limits their power handling.



Fig. 10.3 Schematic of composite magnetic core inductor: (**a**) an inner square spiral coil between a top and bottom composite magnetic film cores and (**b**) a planar inductor with the same spiral core between a top composite magnetic core and a bottom 1-mm-thick Ni-Zn ferrite substrate; (**c**) comparison of magnetic performances of Type-2 inductor with air-core inductor ($^{\odot}$ IEEE 2005) [16]



Fig. 10.4 Different designs of toroidal inductors: (**a**) core without air gap, (**b**) core with an air gap, and (**c**) core in a spiral shape (© IEEE 2005) [17]

Air gaps are introduced to increase the current handling. Liakopoulos and Ahn proposed a novel design for toroidal inductors for high current and power electronics applications [17] as can be seen in Fig. 10.4. Some of the important design parameters for such inductors include number of turns (N), coil length (L_{coil}), length of air gap (L_{gap}), relative permeability of core materials (μ_{rel}), effective magnetic path area (A_{mag}), and effective gap area (A_{gap}) [17]. A theoretical expression for effective inductance can be given by Eq. 10.2 [17]:

$$L = \frac{4E(-7).\pi.N^2}{\frac{L_{coil}}{\mu_{rel}A_{mag}} + \frac{L_{gap}}{A_{gap}}}$$
(10.2)

Evidently, the inductance is expected to increase with increase in the number of coil turns. Also, it should be noted that an increase in the effective magnetic path area can enhance the inductance of the device.

Inductors with planar permalloy cores with no air gaps were reported to have inductance values of more than 10 μ H and a dc resistance as low as 1–4 Ω at low frequency (<2 kHz) thus making them suitable for power applications [17]. However, the inductance decreased drastically at higher frequency. High-frequency

performance could, however, be enhanced by introducing an air gap in the core and also by introducing spiral cores instead of planar cores. Both of the above designs introduce air gaps in the magnetic flux path and thus reduce the eddy current loss at high frequencies.

10.2.4 Solenoid Inductors

Unlike toroid inductors, solenoid inductors are based on 3D windings on open-ended magnetic cores. Such inductors offer high inductance, high quality factor, and low dc resistance [18]. However, inefficient packaging and high leakage flux at high frequency make them less attractive. In addition, parasitic effects resulting from conductor line spacing and dielectric constant of the substrate are of major concerns. Edelstein and Burghartz reported comparison between magnetic performances of spiral and solenoidal inductors [19]. They reported that the magnetic fluxes in the solenoid type inductors are mostly associated with the coil itself and thus they are less prone to eddy current loss as compared to spiral inductors. However, the substrate losses are reported to be comparable with those in spiral inductors.

10.2.5 Inductors with Microslits

At high-frequency applications, as in wireless and communications, Q is a key parameter. Due to material considerations, air cores are preferred over ferromagnetic cores. However, a ferromagnetic core with high permeability can achieve high inductance and thereby reduce the number of windings needed for a specific application. Novel designs have been proposed to minimize the losses of a magnetic core, including introduction of microslits in the core material along the easy axis. Microslits introduce attributes that artificially control the shape anisotropy and magnetostatic energy to shift ferromagnetic resonance (FMR) to higher frequencies [8]. Such designs, in addition, reduce the eddy current loss and leakage flux to a significant extent by ensuring fully closed magnetic circuits [20]. Reduction of leakage flux is vital as the leakage flux interferes with the electronic circuits and doesn't contribute to the effective inductance. There are various parameters that dictate the design of microslits and assure high quality factors. These include compatibility of microslit fabrication with existing technology, thermal stresses and stability, easy axis orientation associated with demagnetization and domain configuration, geometrical design, leakage flux, and stray capacitance [5].

Microslit inductors are fabricated on ferromagnetic films by patterning. The simplest pattern (shown in Fig. 10.5a) consists of microslits along the easy axis direction. Width and spacing of the microslits and judicial selection of the ferromagnetic core are key parameters that determine the anisotropy field, effective demagnetization field (N_d), FMR, inductance, and Q [8].



Fig. 10.5 Inductor core with patterned microslits: (a) unidirectional slits along the easy axis direction [8] and (b) bi-directional micropatterns (© IEEE 2000) [21]

Various research groups have demonstrated enhanced performance with microslited inductor cores. Yamaguchi et al. reported micropatterned sputter-deposited CoNbZr ferromagnetic films of 200 nm thickness with an enhanced anisotropy field of 70 Oe as compared to the intrinsic value of 10 Oe [8]. Similarly, the FMR was reported as high as 2.5 GHz with microslit of thickness 200 nm, width 20 μ m, and 4 μ m spacing, as a result of the microslits' introduction. Also Q was improved. Similar work on micropatterned FeAlO films showed an increase in Q (from 5.6 to 7.7) at 1 GHz for a 2000 nm slit due to effective reduction in the resistance [7].

The aforementioned unidirectionally patterned film, however, utilizes only half of the total area available on the film. Performance of the device can be increased further by an improved design that can make use of more area. Such design consists of preferential micropatterning to form bi-directional micro-wire arrays as shown in Fig. 10.5b [21]. Preferential micropatterning helps split the easy axis into two different directions making use of the high shape anisotropy of the film. This arrangement makes the full area of the film active through the excitation of the hard axis. In addition it further raises the FMR frequency.

Typical fabrication flow for such micropatterns involves deposition of thin magnetic film followed by ion milling or photolithography for micropatterning. Yamaguchi et al. reported such bi-directional microslit fabrication on 100-300-nm-thick amorphous $Co_{85}Nb_{12}Zr_3$ film, deposited by radio-frequency magnetron sputtering, using ion milling [21]. Such a patterned structure was reported to render coercivity as low as 0.4–0.7 Oe. Moreover, the effective anisotropy field was improved; for 100 nm film, it was noted as high as 30 Oe. The frequency profile also improved. Real permeability did not show any degradation at higher frequency as compared to vertically aligned inductors with no slit. Almost 11% increase in the inductance (7.5 nH) over that with an air core inductor was also noted with a 5-nm-thick underlayer of Ti. Q (6.3) was comparable to that of an air core. Baba et al. reported an even larger inductance of 8.2 nH in a bi-directional patterned film with a 10 µm line and 1 µm space, which was twice as large as that in a similar inductor with a uniaxial magnetic film [22]. It should be noted that this is attributed to the variation in slit width and other parameters. As described before, slit width is



Fig. 10.6 Magnetic characteristics of bi-directional micropatterned CoNbZr film: (a) inductance and (b) quality factor (© IEEE 2000) [21]



Fig. 10.7 Schematics of micropatterned inductors (a) with orthogonal bar slits and (b) with cross slits (© IEEE 2000) [8]

one of the parameters that dictate Q and the inductance of the pattern [21]. Figure 10.6a, b illustrates the frequency-dependent Q and inductance of such bi-directional microslits at various slit widths. Also it compares the values with air core inductors. As evident from Fig. 10.6a, a magnetic core has a higher inductance than an air core at all frequency ranges of interest. The introduction of microslits, however, witnesses a decrease in inductance in the low-frequency range. The amount of drop in inductance increases with increase in the slit width. Nevertheless, a significant enhancement in the quality factor is observed with micropatterns (Fig. 10.6b). Increases in slit width further increase Q.

Introduction of orthogonal bar slit patterns or cross-slit patterns, instead of parallel slits, can also increase the available magnetic film area utilization [8]. Schematics of such designs are shown in Fig. 10.7a, b, respectively.



Fig. 10.8 Magnetic characteristics of inductors with various slit patterns: (a) inductance as a function of frequency and (b) quality factor as a function of frequency (© IEEE 2000) [8]

Yamaguchi et al. studied such designs on conventional Al-Si spiral coils with $Co_{85}Nb_{12}Zr_3$ film cores [8]. Figure 10.8a, b illustrates the magnetic performances of such designs. As evident from Fig. 10.8a, the inductance with no-slit and cross-slit patterning is 21% larger than that of air core inductors. Peak inductance is achieved at 1.3 GHz. Also, it can be noted that cross-slit patterns have the highest inductance as compared to orthogonal bar-slit and parallel-slit patterns. The FMR frequency is shifted toward higher frequency range through an artificially controlled demagnetizing field and magnetostatic energy. A decrease in the eddy current losses resulted in higher Q with the introduction of slits (Fig. 10.8b).

10.2.6 Closed Magnetic Circuit-Type Inductor

Yamaguchi et al. reported that the performance of a magnetic core spiral inductor can be improved by an optimized arrangement of patterned magnetic films against the spiral legs [5]. They studied different arrangements of patterned films and compared the results with nonpatterned films. Figure 10.9 shows various arrangements of patterned films.

Plain film inductors are provided with no slit patterned on the magnetic film and nonterminated top and bottom magnetic film edges. The aligned type faces the leg of the spiral. The shift type faces the gaps of each leg, and the closed magnetic circuit type is equivalent to the aligned type with terminated top and bottom magnetic film edges. In-plane eddy current loss becomes prominent in the shift type arrangement, as the middle of the coil leg, where the leakage flux attains a maximum, faces the gap between the magnetic films. Similarly stray capacitance is dependent on the film



Fig. 10.9 Cross-sectional view of relative position of magnetic film with respect to the spiral leg [5]



Fig. 10.10 Comparative evaluation of magnetic characteristics of various inductors as a function of frequency [5]

arrangement. Any voltage difference between the coil turns causes a displacement current. Plain-type and shift-type arrangements shunt the displacement current caused by voltage difference, which might result in a low self-resonant frequency [5]. The comparative performance of each arrangement is shown in Fig. 10.10. As is evident, the plain-, closed-, aligned-, and shifted-type arrangements show inductance in decreasing order. Due to overlap between the two ferromagnetic layers, the closed type has a lower FMR frequency than that observed in either shifted or aligned inductors. Nevertheless, it is higher than that of plain film inductors. The air core inductor resonates at 15 GHz, whereas the self-resonant frequency of the ferromagnetic inductor was found to be 10 GHz, due to stray capacitance and inductance. The resonant frequency values are in increasing order with plain film, shifted, closed,

aligned, and air core inductors. The resonant frequency is dictated by the inherent conductivity of the film. The highest air core resonant frequency is attributed to the absence of any conductive film. An additional terminating structure between two ferromagnetic films in the aligned type introduces added stray capacitance, and thus they resonate at lower values than closed and aligned types. Plain inductors have the largest electrodes, resulting in the highest stray capacitance and thus the lowest resonant frequency value.

Effective core resistance was recorded in increasing order with plain, closed, aligned, shifted, and air core. The shifted type showed higher quality factor (as high as 13) than others as evident from Fig. 10.10b. However, a localized decrease in the quality factor at 3 GHz was noted due to FMR.

10.2.7 Suspended Air Core Design

Losses and parasitics are prime packaging design issues. These issues have been addressed by using suspended air core inductors. Air gaps reduce the winding capacitance, which results from the spatially separated coils from the central lead as in spiral coils. In addition, the dc handling capacity is improved before saturation takes place. A schematic of such design is shown in Fig. 10.11. Goldfarb and Tripathi reported such a suspended spiral inductor in integration with a transistor using air-bridge technology. A 3 µm gap between the inductor and the substrate was achieved [23].

Park and Allen reported an improved design for a suspended inductor with air core using surface micromachining [24]. The air gap between the inductor and the substrate was made as high as 60 μ m, and a thick electroplated conductor line of copper was also deposited. Thick conductors improved the quality factor. They also demonstrated LC filters based on these inductors. The advantage of this design over the air-bridge technique is that a large air gap can be maintained with the help of plated copper. Moreover, thick copper plating increases the cross-sectional area and thus decreases the dc resistance. Chang et al. also reported suspended inductors on silicon, where the air gap was introduced by selective etching of silicon under the





inductor coil to minimize the effect of lossy silicon [25]. Another air gap spiral inductor structure was reported, which used glass microbump bonding (GMBB), by Chuang et al. [26]. Kim and Allen also investigated the effect of air gaps in solenoid inductors [27]. The air gap was introduced using micromachining and electroplating.

10.3 Nanogranular Magnetic Core Materials

Reduction of inductor size without distorting performance is possible with the discovery of new high-performance materials as magnetic cores [21]. High permeability and enhanced magnetic flux reduce the overall size by reducing the number of turns. Resulting reduction in the coil length decreases the coil loss. Stray capacitance decreases as a result of low coil length. Eddy current losses could also be minimized with magnetic cores of higher resistance. This reduces the required thickness of insulator between coil and substrate even for low-resistivity substrates.

The limitations of microgranular magnetic cores, however, are not able to meet the growing demand of electronic devices especially at high frequencies where losses become very prominent due to the inherent conductivity of the magnetic materials. In addition, eddy current losses decrease the effective permeability and, hence, the inductance of the device. One possible remedy is the use of highresistivity materials [28] that also retain soft magnetic properties and high permeability. There is a growing need to develop new materials that could simultaneously achieve high permeability, low coercivity, and high resistivity and also be deposited with adequate thickness to achieve high current handling. The issue has been addressed by the introduction of ultrasoft nanocrystalline thin films with ultrahigh frequency permeability [15] and high resistivity.

Nanostructures improve the magnetostatic and magnetodynamic properties of the material. The use of nanogranular ultrathin magnetic films to improve the magnetic performance seems to defy the classical theory [29]. According to the classical physics, the effective coercive field strength (H_{CK}) is equal to the summation of intrinsic coercive strength caused by magnetostrictive residual stresses, nonmagnetic inclusion, and high-energy distorted region of the grain boundaries [30–32]. Equations 10.3 and 10.4, respectively, show the theoretical values of the grain boundary component of coercivity and initial relative permeability (μ_r), as determined by the classical theory [29, 33, 34].

$$H_C \approx \rho_C \frac{\gamma_W}{J_S.D} \tag{10.3}$$

$$\mu_r \approx \rho_\mu \frac{J_S^2}{\mu_0 \sqrt{AK_1}} D \tag{10.4}$$

where γ_w is the boundary wall energy, which depends upon the anisotropic constant (K₁), lattice parameter, and Curie temperature, J_S is the saturation polarization, D is the grain diameter, μ_o is the permeability, A is the exchange stiffness, and ρ_C and ρ_μ

are material-dependent constants. Evidently, from the above equations, the coercive field is expected to increase and the permeability to decrease with increase in the grain boundary area, i.e., with decrease in the grain size.

Anisotropy and coercivity modeling by Herzer for nanostructured materials, however, found that the classical rule does not hold good at the nanoscale [34]. Critical phenomena at the nanoscale result in attractive properties. It has been found that the classical rule is valid only when the grain size is greater than the ferromagnetic exchange length, where the magnetocrystalline anisotropy is not suppressed due to the ferromagnetic exchange interaction [35].

Due to easy magnetization alignment along the easy axis and in-grain domain formation, magnetization in large grains is a function of magnetocrystalline anisotropy, which is measured by the difference in the B-H hysteresis loop along the easy and hard axes. At the nanoscale, however, it is determined by the simultaneous occurrence of magnetic anisotropy energy and the ferromagnetic exchange energy. Ferromagnetic exchange interaction forces the magnetic moment to align parallel to it and thus restricts the alignment along the easy axis. When the grain size is smaller than the effective exchange interaction length L_{ex} (Eq. 10.5), the coercivity and the permeability are given by Eqs. 10.5 and 10.6, respectively [34], as follows:

$$L_{ex} = \sqrt{\frac{A}{\langle k \rangle}} \tag{10.5}$$

$$H_C = \rho_C \frac{K_1^4 \cdot D^6}{J_S \cdot A^3} \tag{10.6}$$

$$\mu_r = \rho_\mu \frac{J_S^2 A^3}{\mu_0 K_1^4 . D^6} \tag{10.7}$$

where $\langle k \rangle$ is the anisotropy density that is given by the mean fluctuation amplitude of anisotropy energy and other constants are as discussed above [34].

Therefore, materials with intrinsically low anisotropy, e.g., permalloy, can exhibit very low coercivity with very high permeability, if the grain size is restricted below the effective exchange-coupling length as can be seen in Fig. 10.12. As is evident, coercivity is maximum, and permeability is minimum when the grain size equals the effective exchange length (L_{eff}) of 40 nm. Dramatic changes in the coercivity and anisotropy are interpreted in terms of the smoothing part of the exchange interaction, averaging out locally fluctuating anisotropy, so that there is only a small net anisotropy effect on the magnetization process.

Nanostructures do not merely decrease the coercivity and increase the permeability, but they also limit the losses occurring at high frequency. Various loss mechanisms including eddy current loss, FMR loss, and Landau-Lifshitz (LL) damping loss limit the applicability of magnetic films at high frequencies [15]. Eddy current losses, e.g., resistive, capacitive coupling through space layers, etc., are determined by the conductance, shape, and thickness of the film. The cutoff frequency for infinitely wide films due to eddy current loss can be given by



Fig. 10.12 Coercivity and initial permeability as functions of the average grain size D (© IEEE 1990) [34]

$$f_{cutoff} = \frac{4\rho}{\pi\mu_0\mu_i d^2} \tag{10.8}$$

where ρ is the resistivity, μ_i is the intrinsic initial permeability, and d is the thickness of the film [15].

Thin coating with foreign or native oxides to increase the dc resistance is the most prevalent method to decrease the eddy current loss. However, it should be noted that the former does not improve frequency response and the latter decreases the quality factor [36]. Advanced engineered nanostructural materials can render an optimized value of high resistivity (low eddy current loss) as well as high quality factor.

Losses due to FMR and LL damping occur when the applied field frequency matches with the characteristic frequency of the materials [15]. LL damping is caused by structural factors that include demagnetization fields, magnetization dispersion, and domain structure-ripple fields. The FMR frequency for a thin film with a unidirectional demagnetizing field is given by

$$f_{FMR} = 2\pi\gamma (H_k \mu_0 M_S)^{1/2}$$
(10.9)

where γ represents the gyromagnetic constant and H_k the in-plane anisotropy field. The critical phenomena as seen in nanogranular thin films have also been reported to occur in sandwich structures when the layer thickness is restricted to below the exchange-coupling length. Dirne et al. [37] reported such critical behavior in Fe/CoNbZr multilayers.

The discussions above reinforce the attractive properties of nanogranular magnetic materials. Such specially designed materials can simultaneously render low anisotropy and low magnetostriction, e.g., the addition of silicon to low anisotropic nanomaterials can decrease the magnetostriction also. Various kinds of nanostructures based on nanogranular thin films, nanocomposite thin films, and sandwich structures with nanometer scale layers have been studied. In general, popular ferromagnetic materials can be divided into three broad categories – iron based, cobalt based, and iron-cobalt based. Polymeric nanocomposites and advanced novel materials are other attractive choices.

10.3.1 Iron-Based Nanostructural Cores

Permalloy (Fe-Ni) is the most popular among iron-based alloys for inductor applications [36, 38-46]. Magnetic properties are best in the composition range of 30–80% Ni [33]. Good anisotropy is observed due to short-range atomic pairing [47, 48]. As discussed, the magnetic properties are functions of crystalline anisotropy and magnetostriction. Magnetostriction of an inductor is defined as the mechanical response to magnetization (i.e., the change in the shape of inductor under changing magnetic field). Low magnetostriction helps to achieve high permeability, avoids mechanical stress-induced magnetoelastic anisotropy, and reduces noise (e.g., in switched mode converters used in voltage regulator modules and toroidal inductors used in hi-fi amplifiers). Magnetostriction can be decreased in these alloys by addition of nonferrous elements such as copper, silicon, and molybdenum. Yoshizawa et al. reported low magnetostriction in ultrafine (~10 nm) Fe_{73.5}Cu₁Nb₃Si_{13.5}B₉ alloys due to the addition of copper and silicon [49]. Herzer reported a similar effect [34]. A variation of the abovementioned composition (Fe₇₃Cu₁Nb₃Si₁₆B₇) is commercially available under the name of Vitroperm 800 [50]. Microstructural studies of these alloys revealed homogeneously distributed ultrafine grains of body-centered cubic Fe-Si [3]. Addition of nitrogen and aluminum, similarly, increases the saturation magnetization (M_s). Fe-Al-N has been reported to have $M_s > 20 \text{ kG}$ [51, 52]. Such attractive properties are, however, limited to small compositional range. In comparison, Fe-Al-O gives better properties and large compositional freedom. This alloy is reported to have large M_s (~12 kG), dc resistivity (~500 $\mu\Omega$ -cm), and high resonant frequency (~2 GHz) making it suitable for high-frequency applications [7, 8]. Various designs have been proposed that use Fe-Al-O nanogranular inductor cores. Yamaguchi et al. reported very high inductance in such designs (~8 nH at 1 GHz for 100 nm thin film) [8, 21]. However, a flux saturation reduces the inductance (\sim 7.2 nH) [7]. Low eddy current loss has also been reported in two-phase heteroamorphous/granular Fe-based alloys [12, 53, 54]. However, such structure has limited application due to its low anisotropy field.

10.3.2 Cobalt-Based Nanostructural Cores

Dramatically different magnetic and electrical properties of nanogranular thin films can be obtained by changing the gas flow ratio during sputtering. For example, Fig. 10.13 shows the dependence of saturation magnetization and electrical



Fig. 10.13 Dependence of (a) magnetic and (b) electrical properties of Co-Fe-Hf-O films on gas ratio [58]; (c) coercivities of various compositions of Co-X-O-based alloys [57]

resistivity of Co-Fe-Hf-O films on the gas flow ratio. When the gas flow ratio increases above 12%, a significant change in the properties is measured. At a gas flow ratio close to 15.4%, the saturation magnetization attains a maximum value, and the coercivity of the film decreases and reaches its minimum of 0.3 Oe. Simultaneously, the resistivity of the film increases to 1700 $\mu\Omega$.cm, more than a tenfold increase over the metallic Co-Fe-Hf film (approximately 100 $\mu\Omega$.cm).

The origin of such a significant change in these properties is studied by understanding the overall structural evolution using XRD. Films with varying flow ratio were grown, and the structural evolution was compared. At low gas flow ratios, there is a broad peak corresponding to amorphous Co-Fe-Hf-O. When the $O_2/(Ar+O_2)$ gas flow ratio increases, Hf atoms gradually dissolve out of the metallic Co-Fe-Hf material to form HfO₂ due to the strong affinity of Hf to O₂. This is evident by the formation of the HfO₂ peak in the XRD spectrum seen at the 12% gas flow ratio. This is also consistent with a continuous decrease in the lattice spacing of CoFe grains, because Hf atoms with a larger atomic size separate out of CoFe lattices. At a 15.4% O_2 , there is a good phase separation between HfO₂ and CoFe, resulting in a stable CoFe (110) peak position and a minimum coercivity of the Co-Fe-Hf-O film. Additional increase in the oxygen content (16%) causes oxidation of CoFe grains denoted by reduced diffraction intensity and degradation of magnetic properties.

Magnetostriction can further be decreased with Co-based alloys. Masumoto et al. have reported almost zero magnetostriction [55, 56]. Studies of various oxide alloys reveal that only Co-Al-O and Co-Zr-O are suitable for the low-coercivity applications [57].

Nanostructural films of Co-Al-O have also been investigated [57, 59]. Nanometer particle size (53 nm) Co₈₅Al₁₅-based oxides, with a uniformly distributed FCC phase of alpha-cobalt oriented along the lowest anisotropy field plane, were reported to have very low coercivity (~5 Oe) due to an incoherent magnetization and low anisotropic energy orientation [57]. Magnetic closure-domain formation due to the nanogranular dipole moment also significantly decreases the coercivity [35, 60]. Eddy current loss is also minimal in these films due to high resistance. Energy-dispersive X-ray analysis and electron energy-loss spectroscopy studies reveal aluminum and oxygen-rich interparticle regions [57]. This results in preferential oxidation of the interparticle region and, thus, enhanced dc resistance and reduced eddy current loss. The concentration of oxygen, however, should be optimized for an optimum combination of various magnetic parameters. The optimum value reported for $Co_{85}Al_{15}$ -based oxide films includes resistivity of 500 $\mu\Omega$ cm (as high as Fe-based alloys), $M_s \sim 10 \text{ kG}$, $H_c < 5 \text{ Oe}$, and $H_k \sim 70 \text{ Oe}$ at 1% oxygen concentration [57]. Such optimal properties are, however, possible at high temperatures.

In contrast, Co-Zr-O alloys reveal optimal properties even on water cooled substrates, making it more suitable for CMOS technology [61]. Studies of the magnetic behavior of these films show that unlike Co-Al-O, Co-Zr-O alloys do not exhibit super-paramagnetism at 55% cobalt. Moreover, least coercivity is visible at more than one composition (Co, 55 and 70%). Anisotropy as high as 150 Oe is reported in $Co_{60}Zr_{10}O_{30}$ films. A very low value of H_c is also noted when the percolation threshold is approached due to formation of virtual multi-domains. These films have been reported to show excellent high-frequency properties. The real component of permeability has been reported to remain almost constant up to 1 GHz. The FMR frequency is equal to 3 GHz. However, the absolute value of permeability is much less (~60).

Studies on nanostructural evolution in such alloys reveal initial formation of finedispersed ZrO as a result of preferential oxidation. Resulting stress in the matrix results in nanostructure formation. Additional stress and large concentration of Co in the matrix are the primary known factors that affect the final coercivity, anisotropy, and resistivity of the matrix [61].

Nanostructural nitrides of Co alloys exhibit more compositional freedom than oxides [57]. Structural studies reveal the amorphous inter-particulate regions surrounding microcrystalline nanoparticles. Nitrides, however, exhibit low anisotropy

(~35 Oe). Another kind of Co-based magnetic nanocrystalline alloys is Co-Zr-Nb [5, 8, 21, 62]. These alloys exhibit resonant frequencies less than 1 GHz. Various designs have been studied using such core. Details of these studies can be found in the references [5, 8, 21, 62].

10.3.3 Fe-Co-Based Nanostructural Cores

Fe-based and Co-based nanogranular alloys can yield very high resistance resulting in low eddy current loss. They, however, exhibit low permeability and saturation magnetization at high frequencies. This issue can be addressed using Fe-Co-based oxides and nitrides. According to the Pauling-Slater curve, Fe-Co alloys have the highest magnetization (>20 kG) among the iron alloys [62]. However, high magnetostriction in such alloys allows neither high anisotropy nor low H_c. Composite structures, nevertheless, can partly address this issue. Addition of nonmagnetic elements, e.g., silicon and nitrogen, has also been useful to decrease the magnetostriction and thus coercivity. Addition of nickel has also been reported to decrease the coercivity (~ 1.2 Oe) [63]. Saturation magnetization (M_s) higher than that achieved in permalloy is also noted due to nickel addition. However, Osaca et al. reported very low dc resistivity (~21 $\mu\Omega$ cm) in such alloys making them unattractive for high-frequency applications [63]. Addition of aluminum in Co-Fe nitrides has also been found to decrease the coercivity to 1 Oe as compared to 5 Oe in unadulterated alloys [64, 65]. Saturation magnetization in such alloys can also be enhanced to a value as high as 17.6 kG [66]. Anisotropy coupling between magnetic nanograins and electric field-induced atomic ordering also results in high magnetocrystalline anisotropy (~45.6 Oe) [67]. Addition of boron also increases the saturation magnetization of Fe-Co [10]. Minor et al. report saturation magnetization as high as 24 kG in Fe-Co-B thin films [68].

Fe-Co-Zr-O has also been found to exhibit excellent properties for inductor cores [69, 70]. Randomly oriented nanogranular alloy (\sim 10 nm) can decrease the coercivity (~1.9 Oe). The averaging effect of randomly orientated exchange coupling, however, decreased the net magnetocrystalline anisotropy. Such a film rendered permeability as high as 400 up to 1 GHz. Also, such films showed much lower dc resistivity (~36 $\mu\Omega$ cm) than expected in nanogranular structures. This is attributed to electron percolation due to connected conducting grains. Resistivity can, however, be increased by engineering the microstructure. Lee et al. achieved very high resistivity by ensuring fine and isolated α -Fe(Co) grains in $Co_{17,08}Fe_{49,76}Zr_{16,24}O_{16,91}$ film on a silicon substrate [71]. However, such an engineered microstructure increases the volume fraction of oxide phases and thus can have detrimental effect on saturation magnetization. Therefore, it is imperative to control the process parameter to ensure low coercivity, high resistance, and high saturation magnetization. Magnetostatic and magnetodynamic property analysis of thin films showed the simultaneous occurrence of coercivity of 0.3 Oe, anisotropy of 44.9 Oe, saturation magnetization of 16.8 kG, and resistivity of 462.8 $\mu\Omega$ cm in

random grains (average size, 10 nm). Better high-frequency performance has also been reported. The effective permeability as high as 800 was reported up to 2 GHz.

Fe-Co-Al-O nanogranular thin films have also been found to be attractive. RF reactive magnetron sputter-deposited films (50–1000 nm) have been reported to have larger M_S (~22 kG) [15] than 15 kG as achieved in Fe-based and Co-based (~15 kG) [2] and 16.8 kG as could be achieved in the Fe-Co-Zr-O alloys [71]. Ultrahigh dc resistivity (900 $\mu\Omega$ cm) was also achieved. The resistivity of the films increased as the extent of oxides increased at the grain boundary as well as with the increment of refinement of the CoFe grains, completely separated by the oxide matrix (Al₂O₃ or FeCo oxide) and nanogranular structure. Moreover, high anisotropy and high permeability were observed.

10.3.4 Permalloy/Fe-Co Alloy Thin Film Sandwich

As discussed in earlier sections, conventional nanomaterials are not very promising for high-frequency applications. Exotic structures such as composite/sandwich structures have been studied to address this issue [72]. According to the LL equation, high saturation magnetization, high resistance, and high anisotropy are necessary for a magnetic material for high-frequency applications [73]. Such sandwich structures can render saturation magnetization and permeability as high as observed in Fe-Co alloys. In addition, this can exhibit high resistivity and high anisotropy as observed in permalloy [5]. Wang et al. reported a sandwich structure of Ni_{0.81}Fe_{0.19}(5 nm)/ Fe_{0.7}Co_{0.3})_{0.95}N_{0.05} (100 nm)/Ni_{0.81}Fe_{0.19} (5 nm) [64, 74, 75]. Reportedly, even a small volume of permalloy could dramatically reduce coercivity (~0.6 Oe). Ultrahigh and almost constant permittivity (~1000) up to 1.2 GHz was also achieved. The resistivity was, however, very small (50 $\mu\Omega$ cm). Katada et al. reported such structures with saturation magnetization of 24 kG and dc coercivity of 3 Oe [76].

Native oxides, similarly, have been found to decrease the eddy losses. High resistance of native oxide in combination with the high saturation magnetization flux and high anisotropy of Fe-Co-N film makes sandwich structures of native oxide and Co-Fe-N suitable for high-frequency applications [73]. Kakazei et al. reported the magnetic behavior of Co-Fe-N sandwiched between native/deposited nonmetal-lic oxides [77]. Jiang et al. studied a sandwich structure of $Fe_{70}Co_{30}N$ (45 nm)/ $Ni_{55}Fe_{45}$ [62]. The composite structure was fabricated using RF reactive sputtering. The resistivity of the film increased with increase in the nitrogen content. A single layer was isotropic, and significantly higher coercivity was achieved (~80 Oe). However, a seed layer of NiFe of 1 nm thickness significantly reduced the coercivity (~6 Oe), and well-defined uniaxial anisotropy was achieved due to effective magnetic coupling between the magnetic layers. This can also be attributed to partial cancelation of crystalline and magnetostatic anisotropy due to epitaxially grown FeCoN nanograins on NiFe seed layer.

Decrease in the coercivity is also witnessed with nonmagnetic seed layers [72, 74, 78]. Ha et al. reported another sandwiched structure consisting of discontinuous Co-Fe-N thin films and native oxide [62]. The structure was fabricated using RF reactive magnetron sputtering (Co₃₀Fe₇₀ target). The Co-Fe-N film thickness was maintained at 2 nm. The native oxide layers were formed by exposing the film to an oxygen atmosphere. Coercivity in such multilayers was found to be dependent on the exchange coupling of metallic magnetic nanograins through magnetic oxides. Ha et al. also reported linear dependence of the anisotropy field with external applied field during deposition. Field anisotropy (H_k) as high as 67 Oe was achieved for an external applied field of 120 Oe. The coercivity was as low as 0.32 Oe in the hard axis. They also studied the effect of resistivity on thickness. It was found that the resistivity decreases with increase in the thickness in the 1.6-5 nm range. Saturation magnetization flux was also reported to be high. This was attributed to the formation of magnetic oxides (CoFe₂O₄ or Fe₃O₄) during oxidation [79]. Moreover this structure showed excellent high-frequency characteristics. Permeability as high as 1100 was achieved up to 1 GHz.

10.3.5 Nanoscale Ferrite Composites

Recently, various researches have been carried out to develop compatible polymer matrix composites for inductor cores [80–84]. Liu et al. proposed an alternative solution to low inductive magnetic powder-filled composites [28, 85]. They reported a low-temperature process-capable amorphous nickel-zinc ferrite-filled nanocomposite, and a three-layer structure with a planar gold coil was fabricated on a glass wafer. The composite was deposited on the coil and heated at different temperatures. The filler was prepared by sol-gel, and the particle size was less than 200 nm. They reported a relative magnetic permeability of 150–200 for 20% filler by volume, which is six to eight times the reported value for polymer matrix composites with 90% filler.

10.4 Fabrication Techniques

As described in Sect. 10.2, an inductor consists of a magnetic core that is integrated with copper windings. Demand for superior magnetic properties such as high permeability, frequency stability, current handling, and low coercivity has led to the evolution of nanostructured magnetic materials [2]. The magnetic films also need to be deposited in adequate thickness for current handling. A cost-effective fabrication process is needed to translate the research into useable products.

Various thin film processes including radio-frequency magnetron sputtering (rfms), electroplating, and plasma-enhanced chemical vapor deposition (PECVD) were developed for the deposition of magnetic thin films. Electroplating,

nonetheless, is the most popular choice – due to its low cost, simplicity, and low-temperature process. Electroplating involves deposition of materials on a conducting surface under the influence of an electric current. This is particularly useful for lithographically patterned structures. Electrodeposition, however, is not very suitable for generating complex stoichiometry or structures with low conductivity for low eddy current losses. They are not suitable for high frequencies. For complex stoichiometric magnetic thin films, rf sputtering has been studied the most. Screen printing processes have also been reported for the deposition of polymeric composite materials as the magnetic core. Recently spin-sprayed magnetic thin films have drawn significant attention [86–90]. Patterning is a very important process for the design of conductors as well as the magnetic films.

Patterned magnetic films increase the high-frequency characteristics of inductors as described in Sect. 10.2. The shape anisotropy and dc resistance can be artificially enhanced by suitable patterning. This enables the designer to design tunable inductance profiles in a single film [2, 36]. Moreover, closure domain structures at the edges of patterned film can also be suppressed [36]. A suitable design with very small feature size is only possible with advanced lithographic techniques. Martin et al. have done a comprehensive review on lithographic processes [2]. Several modifications have been reported to make lithography more compatible with materials and technologies. For fabrication of multilayer 3D micro-inductor components, a new lithography technique (UV LIGA) has been developed [17]. Other patterning processes include micromachining [24] and ion milling [5].

Micromachining techniques have also been widely studied for the fabrication of 3D inductors. Surface micromachining is a low-cost fabrication process compatible with integrated passive technology. Pre-deposition of a sacrificial layer (e.g., polyimide) is another technique to fabricate suspended cores. Advances in microelectromechanical system (MEMS) technology have, thus, been extended to the fabrication of inductive components [91].

RF inductors usually require an aligned domain structure along the coil direction. Various kinds of annealing treatments are performed to align the domains, including nonmagnetic field annealing, static magnetic field annealing, and rotational magnetic field annealing.

10.4.1 Nonmagnetic Core

Nonmagnetic inductors are popular for realizing integrated inductors due to their relatively simple structure and easier integration. They are widely used in RF circuits. They have limited applicability in power converters due to their lower inductance.

Advanced IC technologies allow power MOSFETs to switch at extremely high frequency (over 100 MHz) with acceptable switching loss [92]. At such high frequencies, small inductances in nH scale can meet the requirements of DC-DC converters in portable electronics. Thus, for such high frequencies (>100 MHz),



Fig. 10.14 Out-of-plane air core inductor by plastic deformation and magnetic assembly [93]

nonmagnetic spiral inductors can easily be realized on power IC chips, with acceptable inductance values and Q factors. The most common example of this is the integrated spiral inductors in Intel's Haswell processors.

Nonmagnetic core inductors on chip are generally spiral inductors with metal layers. Spiral inductors by CMOS technology suffer from high resistance due to the thickness limitation of the interconnection metal layers. It is well known that in-plane spiral inductors generate losses in the silicon substrate. To address this limitation, out-of-plane spiral inductors were realized as shown in Fig. 10.14, by post-CMOS technologies to reduce the substrate loss. The inductor was fabricated in plane first and then was pulled out-of-plane by external magnetic force. Because of the plastic deformation, the inductor stayed out of plane after the release of the external magnetic force [93].

10.4.2 Printed Magnetic Core

In order to combine the favorable properties of magnetic materials with simple processing sequences, small particles of magnetic materials are suspended in a nonmagnetic matrix or binder [80, 85] to synthesize a paste. The paste is then screen-printed to form the inductor core. For example, 1.2 μ m NiZn ferrite particles and 0.8 μ m MnZn ferrite particles are mixed with polymers such as polyimide to form the paste. The mixtures were coated and patterned by screen printing and were cured at 160–300 °C. The resistivities of the fabricated magnetic components were 0.01 M Ω ·cm for NiZn-based composite and 1 M Ω ·cm for MnZn-based composite. The saturation flux densities are 0.43 T and 0.28 T, respectively. However, without high-temperature sintering, the permeabilities are relatively low, ~25 for NiZ-based composites and 32 for MnZn-based composites, respectively. Thus, the resistivity of the fabricated micromagnetic core is increased dramatically at the expense of



Fig. 10.15 Integrated inductors based on ferrite-polymer composites [79–90]



Fig. 10.16 A microfabricated toroidal inductor with electroplated NiFe [95]

relatively low saturation flux density and low permeability. Figure 10.15 shows an integrated inductor with the composite of ferrite powder and polymer bonder.

Compared to electroplating and sputtering, the fabrication process is much simpler and offers flexibility in selecting the magnetic material. First, the composite is screen-printed onto the substrate. Photoresist molds are then created, followed by electroplated copper windings. Next, the molds and seed layers are removed, and the composite is screen-printed on the top again to finish the fabrication. The reported inductance densities were 300–500 nH/mm² and remained constant up to 10 MHz.

10.4.3 Plated Magnetic Core

The magnetic cores for inductors can also be fabricated via electroplating. The fabrication process starts with electroplating of the bottom metal. The isolation layer is then coated, followed by electroplating the magnetic core layer and electroplating of vias. The final step involves formation of the top metal layer [82]. Figure 10.16 shows a microfabricated toroidal inductor.

Most inductors with electroplated magnetics use NiFe alloys as the magnetic core. However, they show high loss and low permeability at high frequencies. An improved material, CoNiFe, has been reported to have better saturation flux density and higher resistivity [63] and has been used for integrated high-frequency inductors [94].

10.4.4 Sputtered Magnetic Core

Sputtered films were used as the magnetic cores for inductors on the top of power MOSFETs. Monolithic DC-DC converters were thus demonstrated by Fuji Electronics, TSMC, Intel, and others [96, 97]. Fuji's inductor consists of two 9 µm sputtered CoHfTaPd magnetic plates with a 35-µm-thick spiral copper winding sandwiched in between as shown in Fig. 10.17.

In the work on on-chip power inductors by Intel Corp., magnetic nanolaminates with elongated spiral coils (referred to as race track designs) showed $9 \times$ higher inductance densities than the state of the art. Their work demonstrated that nanolaminates can increase the roll-off frequency to 300–800 MHz. These inductors take advantage of the uniaxial magnetic anisotropy for higher frequency stability and current handling [98]. Figure 10.18 shows an integrated inductor on 130 nm CMOS Si. The magnetic films are 2-µm-thick Co-Zr-Ta, deposited by sputtering. Inductor wires were microfabricated by electroplating 5 µ of copper on top of 0.5-µm-thick SiO₂, isolating the copper from the first Co-Zr-Ta level. Polyimide was then deposited over the copper to planarize the surface before the deposition of a second level of CoZrTa. Magnetic vias were formed to connect the top and bottom magnetic materials. These inductors are intended for applications with switching frequencies of above 100 MHz.

Properties of Co-Zr-Ta laminates can be enhanced by incorporating boron, which increases the resistivity and suppresses the eddy current in the laminates [99]. The Co-Zr-Ta-B was prepared by DC magnetron sputtering. Oxygen was introduced during sputtering to form cobalt oxide which was used as insulating layers to





Fig. 10.18 Cross-sectional view of inductor integrated on 130 nm CMOS [100]

separate Co-Zr-Ta-B films and form magnetic laminates. An external dc magnetic field was applied during deposition to induce magnetic anisotropy.

Surface roughness on the inductor coil deteriorates the magnetic performance of the inductor. Surface planarization was found to be effective in raising the inductance and the quality factor simultaneously [8]. Surface planarization reduces the surface roughness and thus makes the gap between coil to magnetic film nearly constant and small. Yamaguchi et al. achieved surface roughness as low as 1.2 nm using surface planarization [8]. A significant enhancement in the inductance was reported up to 2 GHz. Planarized inductors were measured to have inductance values as high as 8.26 nH at 1 GHz (22% larger than that of the air core and 2% more than the non-planarized inductor). This increase in the inductance is attributed to the enhanced magnetic field near the magnetic film due to the decrease in the coil to film gap. The quality factor also showed a 14% increase as a result of planarization.

Monolithic integration of solenoid inductors on CMOS ICs was also investigated by TSMC. The inductors consist of a composite amorphous cobalt alloy and insulation layers as the core. The insulation layers were used to suppress eddy currents and improve frequency stability. TSMC's inductors showed high inductance, high current density, and low dc resistance and were suitable for power conversion applications. The inductors can achieve an inductance density of 290 nH/mm² and a Q of 15 at 150 MHz. When coupled together, the inductors exhibited current density of 11 A/mm² and a coupling coefficient of ~0.85. Figure 10.19 shows TSMC's fabricated inductors.

The peak quality factor can be increased further to around 1 GHz if slots were introduced to break the magnetic films and form magnetic bars as shown in Fig. 10.20. The slots were aimed at truncating eddy currents in the magnetic films, resulting in suppression of eddy current losses at higher frequency ranges. Two magnetic laminates were integrated into the inductors and connected with magnetic





Fig. 10.20 Schematic of on-chip spiral inductor with Co-Zr-Ta-B magnetic thin film and magnetic bars [101]

vias for maximum flux enhancement, and polyimide was used to insulate inductors from magnetic materials [99]. In order to optimize the performance, the magnetic films were aligned such that the hard axis is perpendicular to the copper coils. The Co-Zr-Ta-B films were patterned into slits and bars using electron-beam lithography, film deposition, and lift-off process.

Using the micropatterned slit approach, Wu et al. demonstrated $4.4 \times$ improvement in inductance up to 1 GHz and $1.6 \times$ improvement for peak Q at 500 MHz for on-chip inductors when Co-Zr-Ta-B films were integrated, as shown in Fig. 10.20 [101]. The good frequency stability of inductance and quality factor make the integrated inductors suitable for RF applications.

While the importance of nanomagnetic films for power inductors is clearly established because of their high field anisotropy, low coercivity, and high permeability, more R&D is needed to establish the benefits of nanomagnetic films for RF inductor applications beyond 2 GHz.

10.5 Conclusions

This chapter reviews advances in nanomagnetic materials and their integration into high-density power and RF inductors. Various types of inductor designs were reviewed, and recent developments in this regard were highlighted. For magnetic cores, high permeability to achieve inductance, high saturation magnetization to avoid dramatic decrease in the inductance at high currents, low coercivity, high resistance to avoid eddy current loss, and high-frequency characteristics have been identified as key parameters that can significantly decrease the number of windings needed to achieve required inductances and thus could catalyze the effective miniaturization of the devices. Novel nanogranular magnetic materials were identified as one of the key enablers for these applications. Achieving nanomagnetic structures with adequate thickness to meet current handling requirements is a major challenge. Several innovative fabrication approaches are being developed to integrate advanced magnetic cores with windings to create high-density inductors.

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Chapter 11 Nano-conductive Adhesives



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11.1 Introduction

Electrically conductive adhesives (ECAs) are composites of polymeric matrices and electrically conductive fillers. Polymeric matrices have excellent dielectric properties and thus are electrical insulators. The conductive fillers provide the electrical properties and the polymeric matrix provides mechanical properties. Therefore, electrical and mechanical properties are provided by different components, which is different from metallic solders that provide both the electrical and mechanical properties. ECAs have been with us for some time. Metal-filled thermoset polymers were first patented as ECAs in the 1950s [1–3]. Recently, ECA materials have been identified as one of the major alternatives for lead-containing solders for microelectronic packaging applications. There are two types of conductive adhesives: isotropically conductive adhesives (ICAs) and anisotropically conductive adhesives/films (ACAs/ACFs).

ICAs, also known as "polymer solder," are conductive in all directions. The conductive fillers provide the composite with electrical conductivity through contact between the conductive particles. With increasing filler concentrations, the electrical

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Fig. 11.2 ICA particle contacts establish conduction from component to chip carrier

properties of an ICA transform it from an insulator to a conductor. Percolation theory has been used to explain the electrical properties of ICA composites. At low filler concentrations, the resistivities of ICAs decrease gradually with increasing filler concentration. However, the resistivity drops dramatically above a critical filler concentration, Vc, called the percolation threshold (Fig. 11.1). It is believed that at this concentration, all the conductive particles contact each other and form a three-dimensional network. The resistivity decreases only slightly with further increases in the filler concentrations [4–6]. In order to achieve conductivity, the volume fraction of conductive filler in an ICA must be equal to or slightly higher than the critical connection and mechanical bond in an interconnection joint. In an ICA joint (Fig. 11.2), the polymer resin provides mechanical stability and the conductive filler, typically a bimodal distribution of silver flakes and powder, provides electrical conductivity. Filler loading levels that are too high cause the mechanical integrity of adhesive joints to deteriorate. Therefore, the challenge in formulating an ICA is to



Fig. 11.3 Percolation resistivity curves for Ag/epoxy composites [9]

maximize conductive filler content to achieve a high electrical conductivity without adversely affecting the mechanical properties. The percolation threshold for a composite filled with spherical particles is around 40% by volume, but in the typical ICA formulation, it is about 25–30% due to the increased surface/volume (S/V) ratio of the flakes [7, 8]. The threshold goes down to around 5% (Fig. 11.3) with the use of nanoparticle fillers in the form of a "porous powder" with even higher S/V ratios but at the expense of an order of magnitude increase in resistivity [9].

Recently, anisotropic conductive adhesives/films (ACAs/ACFs) are becoming popular as promising candidates for lead-free interconnection solutions in microelectronic packaging applications due to their technical advantages such as fine-pitch capability (<40 µm pitch), low-temperature processing ability, low-cost and environmentally friendly materials and processing, etc. ACAs/ACFs consist of conducting particles (typically 5–10 μ m in diameter) and polymer matrix which provide both attachment and electrical interconnection between electrodes [10–12]. In particular, ACFs are widely used for high-density interconnection between liquid-crystal display (LCD) panels and tape carrier packages (TCPs) to replace the traditional soldering or rubber connectors. In LCD applications, traditional soldering may not be as effective as ACFs in interconnecting materials between indium tin oxide (ITO) electrodes and TCP. ACFs have also been used as an alternative to soldering for interconnecting TCP input lead bonding to printed circuit boards (PCBs). ACAs/ACFs provide unidirectional electrical conductivity in the vertical or Z-axis. This directional conductivity is achieved by using a relatively low volume loading of conductive filler (5-20 volume percent). The low volume



Fig. 11.4 A series of schematics illustrating the steps in forming an ACA joint: (**a**) Component parts: a bumped die and mating carrier with ACA spread over the surface. (**b**) Die is mounted with the carrier and held in place when cured. (**c**) Side view of the completed assembly

loading is insufficient for interparticle contact and prevents conductivity in the X-Y plane of the adhesive. The ACA/ACF is interposed between the two surfaces to be connected. Heat and pressure are simultaneously applied to this stack-up until the conductive particles bridge the two conductor surfaces. Figure 11.4 shows the configuration of a component and a substrate bonded with ACA. Once the electrical continuity is produced, the polymer matrix is hardened by thermally initiated chemical reaction (for thermosets) or by cooling (for thermoplastics). The hardened dielectric polymer matrix holds the two components together and helps maintain the pressure contact between component surfaces and conductive particles. Because of the anisotropy, ACA/ACF may be deposited over the entire contact region, greatly facilitating materials application. Also, an ultra-fine-pitch interconnection (<40 μ m) could be achieved easily. The fine-pitch capability of ACA/ACF would be limited by the particle size of the conductive filler, which can be a few microns or a few nanometers in diameter.

To meet the requirements for future fine-pitch and high-performance interconnects in advanced packaging, ECAs with nano-material or nanotechnology attract more and more interest due to the specific electrical, mechanical, optical, magnetic, and chemical properties. There has been extensive research on nano-conductive adhesives which contain nano-fillers such as nanoparticles, nanowires, or carbon nanotubes. This chapter will provide a comprehensive review of most recent research results on nano-conductive adhesives.

11.2 Recent Advances on Nano-isotropic Conductive Adhesive (Nano-ICA)

11.2.1 ICAs with Silver (Ag) Nanowires

Wu et al. developed an ICA filled with nano-silver wires and compared the electrical and mechanical properties of this nano-ICA to two other ICAs filled with micrometer-sized (roughly 1 μ m and 100 nm, respectively) silver particles [13]. The nanowires had a diameter of roughly 30 nm and a length up to 1.5 um, and the nanowires are polycrystalline in nature. It was found that, at a low filler loading (e.g., 56 wt%), the bulk resistivity of ICA filled with the Ag nanowires was significantly lower than the ICAs filled with 1 μ m or 100 nm silver particles. The better electrical conductivity of the ICA-filled nanowires was attributed to the lower contact resistance between nanowires and more significant contribution from the tunneling effects among the nanowires [13].

It was also found that, at the same filler loading (e.g., 56 wt%), the ICAs filled with Ag nanowires showed similar shear strength to those of the ICAs filled with the 1 μ m and 100 nm silver particles, respectively. However, to achieve the same level of electrical conductivity, the filler loading must be increased to at least 75 wt% for the ICA filled with micrometer-sized Ag particles, and the shear strength of these ICAs is then decreased (lower than that of the ICA filled with 56 wt% nanowires) due to the higher filler loading.

11.2.2 Effect of Nano-sized Ag Particles on ICA Conductivities

Lee et al. studied the effects of nano-sized filler on the conductivity of conductive adhesives by substituting nano-sized Ag colloids for micro-sized Ag particles either in part or as a whole to a polymeric system (polyvinyl acetate – PVAc) [14]. Electrical resistivity was then measured as a function of silver volume fraction.

It was found that, when nano-sized silver particles were added into the system at 2.5 wt% each increment, the resistivity increased in almost all cases, except when the quantity of micro-sized silver was slightly lower than the threshold value. At that point, the addition of the about 2.5 wt% brought significant decrease in resistivity. Near the percolation threshold, when the micro-sized silver particles are still not connected, the addition of a small amount of nano-sized silver particles helps to

build the conductive network and lowers the resistivity of the composite. However, when the filler loading is above the percolation threshold and all the micro-sized particles are connected, the addition of nanoparticles seems only to increase the relative contribution of contact resistance between the particles. Due to its small size, for a fixed amount of addition, the nano-sized silver colloid contains a larger number of particles when compared with micro-sized particles. This large number of particles should be beneficial to the interconnection between particles. However, it also inevitably increases the contact resistance. As a result, the overall effect is an increase in resistivity upon the addition of nano-sized silver colloids.

Ye et al. also reported a similar phenomenon [15], i.e., the addition of nanoparticles showed a negative effect on electrical conductivity. They proposed two types of contact resistance, i.e., restriction resistance due to small contact area and tunneling resistance when nanoparticles are included in the system. It was believed that the conductivity of micro-sized Ag particle-filled adhesives is dominated by constriction resistance, while the nanoparticle-containing conductive adhesives are controlled by tunneling and even thermionic emission. Fan et al. also observed the similar phenomenon (adding nano-sized particles reduced both electrical and thermal conductivities) [16]. The introduction of nanoparticles between the micron-sized flakes and powder may simply add more high-resistance interparticle contacts and lower electron mean free paths.

Lee et al. also studied the effects of temperature on the conductivity of ICAs. Heating the composite to a higher temperature can reduce the resistivity quite significantly. This is likely due to the high activity of nano-sized particles. For micro-sized paste, this temperature effect was considered negligible. The interdiffusion of silver atoms among nano-sized particles helped to reduce the contact resistance quite significantly, and the resistivity reached $5 \times 10^{-5} \Omega$ -cm after treatment at 190 °C for 30 min [14]. Jiang et al. showed that, when suitable surfactant was used in the nano-Ag incorporated ICA, the dispersion and interdiffusion of silver atoms among nano-sized particles could be facilitated and the resistivity of ICA could be reduced to $5 \times 10^{-6} \Omega$ -cm [17]. This is the crucial result, where the surfactant in question permitted the nanoparticles to form sintered contacts between the flakes and powders.

11.2.3 ICA Filled with Aggregates of Nano-sized Ag Particles

To improve the mechanical properties under thermal cycling conditions while still maintaining an acceptably high level of electric conductivity, Kotthaus et al. studied an ICA material system filled with aggregates of nano-sized Ag particles [9]. The idea was to develop a new filler material which did not deteriorate the mechanical property of the polymer matrix to such a great extent. A highly porous Ag powder was attempted to fulfill these requirements. The Ag power was produced by the inert gas condensation (IGC) method. The powders consist of sintered networks of ultra-fine particles in the size range 50–150 nm. The mean diameter of these aggregates

could be adjusted down to some microns. The as-sieved powders were characterized by low level of impurity content, an internal porosity of about 60%, and a good ability for resin infiltration.

Using Ag IGC instead of Ag flakes is more likely to retain the properties of the resin matrix because of the infiltration of the resin into the pores. Measurements of the shear stress-strain behavior indicated that the thermomechanical properties of bonded joints may be improved by a factor up to 2 independent of the chosen resin matrix.

Resistance measurements on filled adhesives were performed within a temperature range from 10 to 325 K. The specific resistance of an Ag IGC filled adhesive was about $10^{-2} \ \Omega$ -cm and did not achieve the typical value of commercially available adhesives of about $10^{-4} \ \Omega$ -cm, despite the reduced percolation threshold from c.30% by volume to c.5% (Fig. 11.3). The reason may be that Ag IGC particles are more or less spherical whereas Ag flakes are flat. So the decrease of the percolation threshold because of the porosity of Ag IGC is overcompensated by the disadvantageous shape and the intrinsically lower specific conductivity. For certain applications where mechanical stress plays an important role, this conductivity may be sufficient, and therefore the porous Ag could be suitable as a new filler material for conductive adhesives.

11.2.4 Nano-Ni Particle-Filled ICA

It is generally known that metal powders present properties that are different from those of bulk metals when their particle sizes are made as small as nanometer size. Powders are classified into particles, microparticles, and nanoparticles according to size. Although the classification criteria are not clear, particles with diameter smaller than 100 nm are generally called nanoparticles. This classification is based on the fact that when its particle size is smaller than 100 nm. For example, when the particle diameter of such magnetic materials as iron and nickel nears to 100 nm, their magnetic domains are changed from multiple to single, and their magnetic properties also change [18]. Majima et al. reported an application example of metal nanoparticles to conductive pastes, focusing on the properties of a new conductive adhesive that were not found in conventional ICAs [18].

Sumitomo Electric Industries, Ltd. (SEI) developed a liquid-phase deposition process using plating technology. This nanoparticle fabrication process achieved purity greater than 99.9% and allowed easy control of particle diameter and shape. The particles' crystallite size calculated from the result of X-ray diffraction measurement was 1.7 nm, which lead to an assumption that the particle size of primary particles is extremely small. When the particle size of nickel and other magnetic metals becomes smaller than 100 nm, they are changed from multi-domain particles to single-domain particles, and their magnetic properties change. That is, if the diameter of nickel particles is around 50 nm, each particle acts like a magnet with two distinct magnetic poles and magnetically connects with each other to form chain-

like clusters. When the chain-like clusters are applied to conductive paste, electrical conduction of the paste is expected to be better than the existing paste. The developed chain-like nickel particles were mixed with predefined amounts of polyvinylidene fluoride (PVDF) that acts as an adhesive. Then, n-methyl-2-pyrrolidone was added to this mixture to make conductive paste. This paste was applied on a polyimide film and then dried to make a conductive sheet. Specific volume resistivity of the fabricated conductive sheet was measured by the quadrupole method. The same measurement was also conducted on the conductive sheet that uses paste made of conventional spherical nickel particles. Measurement of the sheet resistance immediately after paste application showed that the developed chain-like nickel powders had low resistance of about one-eighth of that of the conventionally available spherical nickel particles. This result showed that, when the newly developed chain-like nickel particles were applied as conductive paste, high conductivity can be achieved without pressing the sheet. SEI tested and developed the metal nanoparticles and investigated the possibility of application to conductive paste [19, 20].

11.2.5 Other Nano-fillers for ICAs

There are obviously many more possible choices for metallic nanoparticle fillers and for nanoparticles to work in conjunction with more traditional micron-scale flake and powder fillers. One of the more intriguing choices is the addition of wide bandgap semiconductors SiC or BN nanoparticles to a conventional Ag flake and powder epoxy [21]. Increases in resistance with time are correlated with moisture uptake, and it is noted that the Ag/Ni/Sn contacts are likely subject to galvanic corrosion.

11.2.6 Nano-ICAs for Via Filling in Organic Substrates

Das et al. have developed conductive adhesives using controlled-sized particles, ranging from nanometer scale to micrometer scale, and use them to fill small diameter holes to fabricate Z-axis interconnections in laminates for interconnect applications [22]. See Chap. 13 for a detailed treatment.

11.2.7 Nano-ICAs Filled with Carbon Nanotubes (CNTs)

11.2.7.1 Electrical and Mechanical Characterization of CNT-Filled ICAs [23]

The density of commercially available silver-filled conductive adhesive is around 4.5 g/cm³ after cure. Metal-filled electrically conductive adhesives offer an alternative to typical lead-tin soldering with the advantages of being simple to process at

lower temperatures without toxic lead or corrosive flux. The disadvantage of conventional metal-filled conductive adhesives is that high loading of filler decreases the mechanical impact strength, while decreasing filler loading results in poor electrical properties. CNTs are a new form of carbon, which was first identified in 1991 by Sumio Iijima of NEC, Japan [24]. Nanotubes are sheets of graphite rolled into seamless cylinders. Besides growing single wall nanotubes (SWNTs), nanotubes can also have multiple walls (MWNTs) – cylinders inside the other cylinders. The CNT can be 1-50 nm in diameter and 10-100 µm or up to few mm in length, with each end "capped" with half of a fullerene dome consisting of five and six member rings. Along the sidewalls and cap, additional molecules can be attached to functionalize the nanotube to adjust its properties. CNTs are chiral structures with a degree of twist in the way that the graphite rings join into cylinders. The chirality determines whether a nanotube will conduct in a metallic or semiconducting manner. CNTs possess many unique and remarkable properties. The measured electrical conductivity of metallic CNTs is in the order of 10^4 S/cm [25]. The thermal conductivity of CNTs at room temperature can be as high as 6600 W/mK [26]. The Young's modulus of a CNT is about 1 TPa. The maximum CNT tensile strength is close to 30 GPa, with some reported at TPa [27]. The density of MWNTs is 2.6 g/cm³, and the density of SWNTs ranges from 1.33 to 1.40 g/cm³ depending on the chirality [28]. Since CNTs have very low density and long aspect ratios, they have the potential of reaching the percolation threshold at very low weight percent loading in the polymer matrix.

Li and Lumpp developed new epoxy-based conductive adhesives filled with MWNTs [29]. Preparation and processing methods for the new conductive adhesives were developed. It was found that ultrasonic mixing process helped disperse CNTs in the epoxy more uniformly and made them contact better, and thus lower electrical resistance was achieved [29]. The contact resistance and volume resistivity of the conductive adhesive decreased with increasing CNT loading. The percolation threshold for the MWNTs used in Li's experiments is less than 3 wt%. With 3 wt% loading, the average contact resistance was comparable with solder joints. It was also found that the performance of CNTs filled conductive adhesive was comparable with solder joints at high frequency. By replacing metal particle fillers with CNTs in the conductive adhesive, a higher percentage of mechanical strength was retained. For example, with 0.8 wt% of CNT content, 80% of the shear strength of the polymer matrix was retained, while conventional metal-filled conductive adhesives only retain less than 28% of the shear strength of the polymer matrix [30].

Experiments conducted by Qian et al. [31] show 36–42% and 25% increases in elastic modulus and tensile strength, respectively, in polystyrene (PS)/CNT composites. The TEM observations in their experiments showed that cracks propagated along weak CNT–polymer interfaces or relatively low CNT density regions and caused failure. If the outer layer of MWNTs can be functionalized to form strong chemical bonds with the polymer matrix, the CNT/polymer composites can be further reinforced in mechanical strength and have controllable thermal and electrical properties.

11.2.7.2 Effect of Adding CNTs to the Electrical Properties of ICAs

Lin and Lin studied the effect of adding CNTs to the electrical conductivity of silverfilled conductive adhesive that had various filler loadings [32]. It was found that the CNTs could enhance the electrical conductivity of the conductive adhesives greatly when the silver filler loading was still below the percolation threshold. For example, a 66.5 wt% filled silver conductive adhesive without CNTs had a resistivity of 10^4 Ω -cm, but showed a resistivity of 10^{-3} Ω -cm after adding 0.27 wt% CNT. Therefore, it is possible to achieve the same level of electrical conductivity by adding a small amount of CNTs to replace the silver fillers.

11.2.7.3 Composites Filled with Surface-Treated CNTs

Although CNTs have exceptional physical properties, incorporating them into other materials has been inhibited by the surface chemistry of carbon. Problems such as phase separation, aggregation, poor dispersion within a matrix, and poor adhesion to the host must be overcome. Zyvex claimed that they have overcome these restrictions by developing a new surface treatment technology that optimizes the interaction between CNTs and the host matrix [33]. A multifunctional bridge was created between the CNT sidewalls and the host material or solvent. The power of this bridge was demonstrated by comparing the fracture behavior of the composites filled with untreated and surface-treated nanotubes. It was observed that the untreated nanotubes remained in the matrix even after the fracture, indicating strong interaction with the matrix. Due to their superior dispersion in the polymer matrix, the treated nanotubes achieved the same level of electrical conductivity at much lower loadings than the untreated nanotubes [33].

11.2.8 Inkjet Printable Nano-ICAs and Inks

Areas for printing very fine-pitch matrix (e.g., very fine-pitch paths, antennas) are very attractive. But there are special requirements for inkjet printing materials, namely, the most important ones are low viscosity and very homogenous structure (like a molecular fluid) to avoid sedimentation and separation during the process. Additionally, for electrical conductivity of printed structures, the liquid has to contain conductive particles, with nano-sized dimensions to avoid blocking the printing nozzle and to prevent sedimentation phenomenon. Nano-sized silver seems to be one of the best candidates for this purpose, especially when its particle size dimensions will be less than 10 nm. (See also Chap. 14).

Inkjet is an accepted technology for dispensing small volumes of material (50–500 pl). Currently traditional metal-filled conductive adhesives cannot be processed by inkjetting (due to their relatively high viscosity and the size of filler material particles). The smallest droplet size achievable by traditional dispensing techniques is in the range of 150 μ m, yielding proportionally larger adhesive dots on the substrate. Electrically conductive inks are available on the market with metal particles (gold or silver) <20 nm suspended in a solvent at 30–50 wt%. After deposition, the solvent is eliminated and electrical conductivity is enabled by a high metal ratio in the residue. Some applications include a sintering step. However, these traditional nano-filled inks do not offer an adhesive function [34, 35].

There are many requirements for an inkjettable, Ag particle-filled conductive adhesive. The silver particles must not exceed a maximum size determined by the diameter of the injection needle used. At room temperature the adhesive should resist sedimentation for at least 8, preferably 24 h. A further requirement by the end user on the adhesive's properties was a two-stage curing mechanism. In the first curing step, the adhesive surface is dried and remains meltable. In this state the product may be stored for several weeks. The second curing step involves glueing the components with the previously applied adhesive. By heating and applying pressure, the adhesive is remelted and cured. Thus, the processing operation is similar to that required for soldering. A conductivity in the range of $10^{-4} \Omega$ -cm in the bulk material is required. An adhesive less prone to sedimentation was formulated by using suitable additives. Furthermore, the formation of filler agglomerations during deflocculation and storage was reduced. This effect was achieved by making the additives adhere to the filler particle surfaces. This requires a very sensitive balance. If the insulation between individual silver particles becomes too strong, overall electrical conductivity is significantly reduced.

Jana Kolbe et al. demonstrated feasibility of an inkjettable, isotropically conductive adhesive in the form of a silver-loaded resin with a two-step curing mechanism [36, 37]. In the first step, the adhesive was dispensed (jetted) and pre-cured leaving a "dry" surface. The second step consisted of assembly (wetting of the second part) and final curing. The attainable droplet sizes were in the range of 130 μ m but could be further reduced by using smaller (such as 50 μ m) and more advanced nozzle shapes.

See Chap. 14 for inkjet deposited interconnections.

11.3 Advances in Nano-ACA/ACF Technologies

11.3.1 Low-Temperature Sintering of Nano-Ag-Filled ACA/ACF

One of the concerns for ACA/ACF is the higher joint resistance since interconnection using ACA/ACF relies on mechanical contact, unlike the metal bonding of soldering. An approach to minimize the joint resistance of ACA/ACF is to make the



Fig. 11.5 SEM photographs of 20 nm-sized Ag particles annealed at different temperatures for 30 min: (**a**) room temperature (no annealing); (**b**) annealed at 100 °C; (**c**) annealed at 150 °C; (**d**) annealed at 200 °C; and (**e**) annealed at 250 °C (markers: (**a**) 3 μ m (**b**) 2 μ m (**c**) 2 μ m (**d**) 3 μ m (**e**) 3 μ m) [38]

conductive fillers fuse to each other and form metallic joints such as metal solder joints. However, to fuse metal fillers in polymers does not appear feasible, since a typical organic printed circuit board (Tg ~ 125 °C), on which the metal-filled polymer is applied, cannot withstand such a high temperature; the melting temperature (T_m) of Ag, for example, is around 960 °C. Research showed that T_m and sintering temperatures of materials could be dramatically reduced by decreasing the size of the materials [38-40]. It has been reported that the surface premelting or disorder of the fine nanoparticles (<100 nm) is a primary mechanism of the T_m depression and low-temperature sintering processes [39]. For nano-sized particles, faster sintering behavior can occur at much lower temperatures, and, as such, the use of the fine metal particles in ACAs would be promising for fabricating high electrical performance ACA joints through eliminating the interface between the contacts and metal fillers. The application of nano-sized particles can also increase the number of conductive fillers on each bond pad and result in more contact area between fillers and bond pads. Figure 11.5 shows SEM photographs of nano-Ag particles annealed at various temperatures. Although very fine particles (20 nm) were observed for as-synthesized (in Fig. 11.5a) and 100 °C treated particles (in Fig. 11.5b), dramatically larger particles were observed after heat treatment at 150 °C and above. With increasing temperatures, the particles became larger and appeared as solid matter rather than porous particles or agglomerates. The particles shown in Fig. 11.5c–e were fused through their surfaces and many dumbbell-type particles could be found. The morphology was similar to a typical morphology of the initial stage in the typical sintering process of ceramic, metal, and polymer powders. This low-temperature sintering behavior of the nanoparticles is attributed to the extremely high interdiffusivity of the nanoparticle surface atoms, due to the significantly energetically unstable surface status of the nano-sized particles with a large proportion of the entire particle volume contained in the surface layer.

For the sintering reaction in a certain material systems, temperature and duration are the most important parameters, in particular, the sintering temperature. The current-resistance (I-R) relationship of the nano-Ag-filled ACA is shown in Fig. 11.5. As can be seen from the figure, with increasing curing temperatures, the resistance of the ACA joints decreased significantly, from 10^{-3} to $5 \times 10^{-5} \Omega$. Also, higher curing temperature ACA samples exhibited higher current-carrying capability than the low-temperature samples. This phenomenon suggested that more sintering of nano-Ag particles and subsequently superior interfacial properties between fillers and metal bond pads were achieved at higher temperatures [41], yet the X-Y direction of the ACA maintains an excellent dielectric property for electrical insulation (Fig. 11.6).

Test results for nano-Ag ACFs are contained in [42] where it is shown that there are negligible leakage currents between 30 μ m fine-pitch contacts and that the contact resistance is comparable with or less than most comparable solder joints, with the contact resistance stability rivaling solder's with aging and under high-temperature and high-humidity tests. Similar results are shown for a bumpless bonding technology [43].



Fig. 11.6 Current-resistance (I-R) relationship of nano-Ag-filled ACAs with different curing temperatures [41]

11.3.2 Self-Assembled Molecular Wires for Nano-ACA/ACF

In order to enhance the electrical performance of ACA/ACF materials, selfassembled molecular (SAM) wires have been introduced into the interface between metal fillers and the metal-finished bond pad of ACAs [44, 45]. These organic molecules adhere to the metal surface and form physicochemical bonds, which allow electrons to flow. As such, they reduce electrical resistance and enable a high current flow. The unique electrical properties are due to the tuning of metal work functions by those organic monolayers. The metal surfaces can be chemically modified by the organic monolayers, and the reduced work functions can be achieved by using suitable organic monolayer coatings. An important consideration when examining the advantages of organic monolayers pertains to the affinity of organic compounds to specific metal surfaces. Table 11.1 gives the examples of molecules preferred for maximum interactions with specific metal finishes; although only molecules with symmetrical functionalities for both head and tail groups are shown, molecules and derivatives with different head and tail functional groups are possible for interfaces concerning different metal surfaces.

Different organic molecular wires, dicarboxylic acid and dithiol, have been introduced into ACA/ACF joints. For a low-temperature curable ACA (<100 °C) with incorporated SAM wires and micron-sized gold/polymer or gold/nickel fillers, lower joint resistance and higher maximum allowable current (highest current applied without inducing joint failure) were achieved. For high curing temperature ACA (150 °C), however, the improvement was not as significant as for low curing temperature ACAs, due to the partial desorption/degradation of the organic mono-layer coating at the relatively high temperature [46]. However, when dicarboxylic acid or dithiol was introduced into the interface of nano-silver-filled ACAs, significantly improved electrical properties could be achieved for a high-temperature

Formula	Compound	Metal finish
H-S-R-S-H	Dithiols	Au, Ag, Sn, Zn
$N \equiv C-R-C \equiv N$	Dicyanides	Cu, Ni, Au
O=C=N-R-N=C=O	Diisocyanates	Pt, Pd, Rh, Ru
	Dicarboxylates	Fe, Co, Ni, Al, Ag
НО ОН		
NH	Imidazole and derivatives	Cu
R-SiOH	Organosilicone	SiO ₂ , Al ₂ O ₃ , quartz, glass, mica, ZnSe,
	derivatives	GeO ₂ , Au

Table 11.1 Potential organic monolayer interfacial modifiers for metal finishes

R denotes alky and aromatic groups



Fig. 11.7 Electrical properties of Ag nano-ACA with dithol or dicarboxylic acid [47]

curable ACA/ACF, suggesting the coated molecular wires did not suffer degradation on silver nanoparticles at the curing temperature (Fig. 11.7). The enhanced bonding could be attributed to the larger surface area and higher surface energy of nanoparticles, which enabled the monolayers to be more readily coated and relatively thermally stable on the metal surfaces [47].

11.3.3 Silver Migration Control in Nano-silver-Filled ACA

Silver is the most widely used conductive filler in ICAs and exhibits exciting potentials in nano-ACA/ACF due to many unique advantages of silver. Silver has the highest room temperature electrical and thermal conductivity among all the conductive metals. Silver is also unique among all the cost-effective metals by nature of its conductive oxide (Ag₂O). In addition, silver nanoparticles are relatively easily formed into different sizes (a few nanometers to 100 nm) and shapes (such as spheres, rods, wires, disks, flakes, etc.) and well dispersed in a variety of polymeric matrix materials. Also, the low-temperature sintering and high surface energy make silver one of the promising candidates for conductive filler in nano-ACA/ACF. However, silver migration has long been a reliability concern in the electronics industry. Metal migration is an electrochemical process, whereby metal (e.g., silver), in contact with an insulating material, in a humid environment and under an applied electric field, leaves its initial location in ionic form and deposits at another location [48]. It is considered that a threshold voltage exists above which the migration starts.

Such migration may lead to a reduction in electrical spacing or cause a short circuit between interconnections. The migration process begins when a thin continuous film of water forms on an insulating material between oppositely charged electrodes. When a potential is applied across the electrodes, a chemical reaction takes place at the positively biased electrode where positive metal ions are formed. These ions, through ionic conduction, migrate toward the negatively charged cathode and over time, they accumulate to form metallic dendrites. As the dendrite growth increases, a reduction of electrical spacing occurs. Eventually, the dendrite silver growth reaches the anode and creates a metal bridge between the electrodes, resulting in an electrical short circuit [49].

Although other metals may also migrate under specific environment, silver is more susceptible to migration, mainly due to the high solubility of silver ion, low activation energy for silver migration, high tendency to form dendrite shape, and low possibility to form stable passivation oxide layer [50-52]. The rate of silver migration is increased by (1) an increase in the applied potential, (2) an increase in the time of the applied potentials, (3) an increase in the level of relative humidity, (4) an increase in the presence of ionic and hydroscopic contaminants on the surface of the substrate, and (5) a decrease in the distance between electrodes of the opposite polarity.

In order to reduce silver migration and improve the reliability, several methods have been reported. The methods include:

- 1. Alloying the silver with an anodically stable metal such as palladium [49] or platinum [53] or even tin [54]
- Using hydrophobic coating over the PWB to shield its surface from humidity and ionic contamination [55], since water and contaminates can act as a transport medium and increase the rate of migration
- 3. Plating of silver with metals such as tin, nickel, or gold, to protect the silver fillers and reduce migration
- 4. Coating the substrate with polymer [56]
- 5. Applying benzotriazole (BTA) and its derivatives in the environment [57]
- 6. Employing siloxane epoxy polymers as diffusion barriers due to the excellent adhesion of siloxane epoxy polymers to conductive metals [58]
- 7. Chelating silver fillers in ECAs with molecular monolayers [59]

As an example shown in Fig. 11.8 [60], with carboxylic acids and forming chelating compounds with silver ions, the silver migration behavior (leakage current) could be significantly reduced and controlled.

11.3.4 ACF with Straight-Chain-Like Nickel Nanoparticles

Sumitomo Electric recently developed a new-concept ACF using nickel nanoparticles with a straight-chain-like structure as conductive fillers [61]. They applied the formulated straight-chain-like nickel nanoparticles and solvent in a





mixture of epoxy resin on a substrate film. Then, the particles were made to orient toward the vertical direction of the film surface and fixed in resin by evaporating the solvent. In the estimation using 30 μ m-pitch IC chips and glass substrates (the area of Au bumps was 2000 μ m², the distance of space between neighboring bumps was 10 μ m), the new ACF showed excellent reliability of electrical connection after high-temperature, high-humidity (60 °C/90%RH) test and thermal cycle test (between -40 and 85 °C). The samples were also exposed to high-temperature, high-humidity (60 °C/90%RH) for insulation ability estimation. Although the distance between two electrodes was only 10 μ m, ion migration did not occur and insulation resistance was maintained at over 1 G Ω for 500 h. This result showed that the new ACF has potential to be applied in very fine interconnections.

11.3.5 Nanowire ACF for Ultra-fine-Pitch Flip Chip Interconnection

In order to satisfy the reduced I/O pitch and avoid electric shorting, a possible solution is to use high aspect ratio metal posts. Nanowires exhibit high possibilities due to the small size and extremely high aspect ratio. In the literature, nanowires could be applied in FET sensors for gas detection, magnetic hard disk, nanoelectrodes for electrochemical sensor, thermal-electric device for thermal dissipation and temperature control, etc. [62–64]. To prepare nanowires, it is important to define nanostructures on photoresist. Many expensive methods such as e-beam, X-ray, or scanning probe lithography have been used, but micrometer length nanowires cannot be achieved. Another less expensive alternative is electrodeposition of metal into a nano-porous template such as anodic aluminum oxide (AAO) [65] or block-copolymer self-assembly template [66]. The disadvantages of a blockcopolymer template include thin thickness (that means short nanowires), nonuniform distribution, and poor parallelism of nano-pores. However, AAO has benefits of higher thickness (>10 μ m), uniform pore size and density, larger size, and very parallel pores. Lin et al. [67] developed a new ACF with nanowires. They used AAO templates to obtain silver and cobalt nanowire arrays by electrodeposition. And then low viscous polyimide (PI) was spread over and filled into the gaps of nanowires array after surface treatment. The bimetallic Ag/Co nanowires could be keept parallel during fabrication by magnetic interaction between the cobalt and the applied magnetic field. The silver and cobalt nanowires/polyimide composite films could be obtained with nanowire diameter of about 200 nm and maximum film thickness up to 50 μ m. The X-Y insulation resistance is about 4–6 G Ω , and Z-direction resistance including the trace resistance (3 mm length) is less than 0.2Ω . They also demonstrated the evaluation of this nanowire composite film by stress simulation. They found that the most important factor for designing nanowire ACF was the volume ratio of nanowires. But actually the ratio of nanowires cannot be too small to influence the electric conductance. They concluded that it is important to get a balance between electric conductance and thermal-mechanical performance by increasing film thickness or decreasing the modulus of the polymer matrix instead of reducing the ratio of nanowires.

Nanowire ACF technology is covered more extensively in Chap. 22.

11.3.6 In Situ Formation of Nano-conductive Fillers in ACA/ACF

One of the challenging issues in the formation of nano-filler ACA/ACF is the dispersion of nano-conductive fillers in ACA/ACF. A lot of research has been going on in recent years to address the dispersion issue of nanocomposites because nano-fillers tend to agglomerate. For the fine-pitch electronic interconnects using

nano-ACA/ACF, the dispersion issues need to be solved. The efforts usually include the physical approaches such as sonication and chemical approaches such as surfactants. Recently, a novel ACA/ACF incorporated with in situ formed nanoconductive particles was proposed for next-generation high-performance fine-pitch electronic packaging applications [68, 69]. This novel interconnect adhesive combines the electrical conduction along the Z-direction (ACA-like) and the ultra-finepitch (<100 nm) capability. Instead of adding the nano-conductive fillers in the resin, the nanoparticles can be in situ formed during the curing/assembly process. By using in situ formation of nanoparticles, during the polymer curing process, the filler concentration and dispersion could be better controlled and the drawback of surface oxidation of the nano-fillers could be easily overcome.

11.3.7 Nano-polymer Fillers in ACFs

There are ongoing research studies of the use of metal-coated polymer spheres as ACF fillers [70–75]. One advantage is that the compressibility of the polymer ensures a greater contact area between the particle and contact pad without requiring the higher process pressures necessary to deform the contact and/or particle for metal fillers to achieve a similar result. In addition, the polymer can provide a better match to the epoxy matrix thermal coefficient of expansion. The disadvantage is that the metal shell coating on the polymer coating can crack under excessive processing pressure, cutting the conduction path. Experimental studies to date have focused on micron-scale particles, but there has been modeling work on the possible benefits of, for example, 20 nm diameter particles with ~1 nm metal coatings [76, 77]. The conclusion is the smaller particles show increased compressive strength dependent on the coating thickness.

11.3.8 Nano-fiber Stabilization of ACF Filler Particles

When pressure is applied to a simple ACA or ACF during curing, the epoxy resin flows outward in the x and y directions, as intended, to fill around the contact bumps, etc. However, this flow tends to carry the conductive particles with it, sweeping them off the contact pads and into the areas between them, where they may pile up and short circuit adjacent contacts. The conventional ACF solution is to confine the particles to a semi-cured (or otherwise high viscosity) area of the film or tape to restrict movement and to laminate this layer with another lower viscosity film (or two) which flows and fills the cavities to provide the encapsulation and adhesion functions.

Another innovative solution has been developed which immobilizes the conductive particles in electrospun polymer nanofiber chains by adding them to the electrospinning polymer reservoir. This process and its results are covered more fully in Chap. 12 and [78–81].

11.3.9 ICA/ACA Nano-fillers for Thermal Applications

Of course, just as the ICA, ACA, and ACF materials can be used as electrically conductive die attach, they can also serve a dual role as thermally conductive (die attach) materials. As one example, [82] compares silver nanorods, nickel nanochains, and silver nanoparticles as supplementary fillers added to commercial silver flake-filled commercial die attach. Of the three, the nanoparticles were the most effective, essentially doubling the thermal conductivity of the flake-filled composite to over 20 W/mK.

Carbon nanotubes and graphene have also been used as fillers in thermally conductive composites, a topic treated more fully in Chap. 27. In [83], the thermal conductivities of graphene oxide and $Al(OH)_3$ -coated graphene epoxy composites are compared, but with the goal of preserving the electrically insulating properties of the epoxy.

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Chapter 12 Nano-materials in Anisotropic Conductive Adhesives (ACAs)



Kyung-Wook Paik and Kyung-Lim Suk

12.1 Introduction

As the display market demands higher resolution and higher functionality, electronic packages having higher I/O counts per unit area, higher density, and smaller size become necessary (Fig. 12.1) [1–5]. The trend for fine pitch becomes a major development direction in display electronics, because it can realize higher resolution from high-definition (HD) to full HD (FHD) to ultra-HD (UHD) and virtual reality (VR) displays as well as multifunctionality of display products. Figure 12.2 shows the schematics of display packaging structures, such as flex-on-board (FOB), flex-on-glass (FOG), chip-on-flex (COF), and chip-on-glass (COG). The ACAs bonding method has been widely used for display packaging technology due to its many advantages, such as low process temperatures, simple processing (no underfill), fine pitch capability, and environmentally friendly processes (lead-free and flux-free) [6].

Adhesives are classified into isotropic conductive adhesives (ICAs), anisotropic conductive adhesives (ACAs), and nonconductive adhesives (NCAs) according to the existence of conductive particles. Among them, ACAs are interconnection materials having spherical conductive particles in thermosetting polymer resins. As shown in Fig. 12.3, the cured ACAs provide mechanical bonding between chips and substrates by a thermosetting polymer resin and electrical connection by captured conductive particles between bumps and electrodes after applying heat and pressure. Usually metal-coated polymer conductive particles in ACAs provide good reliability because of the compliance of polymer balls. However, the use of ACAs for fine pitch interconnection has been limited, because conductive fillers can agglomerate between fine pitch bumps and electrodes during the bonding process

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Fig. 12.1 Electronic packaging trend in display applications. (Source: http://www.itconference.co.kr)



resulting in electrical short problems (Fig. 12.4). Therefore, new ACAs preventing electrical short circuits by fundamentally suppressing conductive particle movement are required.

A new concept of nanofiber ACAs incorporated conductive particles into nanofiber was introduced to suppress conductive particle movement and to obtain stable three-dimensional electrical properties of fine pitch electronics. If conductive particles are fixed in nanofibers, not only their movement is fundamentally prevented, but also all the particles are electrical insulated by dielectric polymer resins. In addition, nanofiber can be formed by an electrospinning method. The electrospinning method uses an electrical charge to draw very fine fibers (typically on the micro- or nanoscale) from a polymer solution [7, 8]. As shown in Fig. 12.5, an



Fig. 12.3 Schematic diagram of ACAs bonding structure



E: Collector units

Fig. 12.5 Electrospinning process and equipment

electrospinning machine is composed of a syringe equipped with conducting needle, a high-voltage power supply, and a collector unit. When an electrical potential is applied between a polymer droplet on the needle and the collector, the droplet becomes charged and electrostatic repulsion counteracts the surface tension of the droplet, which is stretched from a critical point. Finally, the liquid jet converts into solid nanofiber by solvent evaporation before arriving at the grounded target.

12.2 Effects of Conductive Particle Incorporated Nanofiber (CPIN) on Conductive Particle Movement and ACA Interconnection Stability

12.2.1 Introduction

The most critical issue facing current display devices is interconnecting the fine pitch driver chip on the display panel using ACAs without an electrical short-circuit phenomenon, since conductive particles in the adhesives can be agglomerated between fine pitch bumps and electrodes during the bonding process, thereby causing electrical shorts in the X-Y directions. Although insulating layer-coated conductive particles and/or viscosity-controlled ACAs have been introduced in commercial ACAs products, but such approaches have not been able to completely solve the fine pitch ACAs electrical problems [6, 9-13]. It is because the problems occur from conductive particle movements along with polymer resin flow of ACAs which was originally designed to fill the empty gaps between chips and substrates during the bonding process [14]. For this reason, the movements of conductive particles in ACAs are unavoidable, unless there is a fundamental solution to keep them from moving.

Therefore, a new idea of nanofiber ACAs with incorporating conductive particles to suppress their movements has been newly introduced. The concept of nanofiber ACAs was inspired by the Korean traditional dried fish product, so-called Gulbi as shown in Fig. 12.6, where dried fish are tied up with a continuous rope. A similar idea was conceived to suppress conductive particle movements by incorporating the conductive particles into electrospun nanofiber ropes. A CPIN structure embedded in B-stage adhesives restrains the conductive particle movements during the adhesive resin flow, thereby significantly reducing electrical short-circuit problems of fine pitch display devices and increasing the conductive particle capture rate. Moreover, a nanofiber polymer coated on the conductive particles can act as a good insulating material to prevent electrical shorts between neighboring conductive particles. After constraining the conductive particle movements, the nanofiber materials were designed to be melted by applied bonding heat and pressure to provide stable contact between the conductive particles and electrodes. The CPIN can be realized by an electrospinning method which has been used for various applications in fields such as sensors, tissue engineering, filtration, and so on [7, 15–18].

Fig. 12.6 "Gulbi" in Korea: the idea of CPIN (conductive particle incorporated nanofiber)



Fig. 12.7 Nanofiber electrospinning equipment used in this study



12.2.2 Fabrication of CPIN Structure and Nanofiber ACAs

The fabrication of the CPIN structure was carried out by electrospinning the mixture of Nylon 6, Ni-/Au-coated polymer conductive particles, and formic acid. A voltage of 15 kV was applied between the Nylon 6 and conductive particle solution contained in a plastic syringe equipped with an Al needle and the grounded target, with the syringe simultaneously moved in the X-Y directions to obtain randomly distributed CPIN mats of 30×70 mm (Fig. 12.7). The CPIN mats were dried in a vacuum oven at $120 \degree$ C for 2 h, and the morphologies of the mats were characterized.

To fabricate the novel nanofiber ACAs, 8 μ m thick B-stage thermo-curable epoxy adhesive films without added conductive particles were laminated on the top and bottom sides of CPIN mats at 80 °C. At this temperature, the epoxy resins can easily flow and penetrate into the porous CPIN structure without epoxy resin curing.

The fabricated ACAs have a composite epoxy adhesive film layer/CPIN layer/ epoxy adhesive film layer structure. Therefore, the resulting structure can provide both functions of electrical conduction and mechanical adhesion between a chip and a substrate. In order to evaluate nanofiber effects on conductive particle movements and electrical properties, the conventional ACAs and the nanofiber ACAs using the same epoxy adhesive resins were compared.

12.2.3 Conductive Particle Movement Tests and Simulation of Resin Flow

The conductive particle movements were analyzed using an optical microscope during the bonding process of an Au-patterned Si chip and a bare glass substrate as shown in Fig. 12.8 using conventional and nanofiber ACAs. Both ACAs were



Fig. 12.8 Fabrication processes of (a) Au-patterned Si test chips and (b) glass test substrates



Fig. 12.9 Schematic illustrations of (a) resin flow simulation, (b) conventional ACAs, and (c) nanofiber ACAs

laminated on the Si chips, and the average number of conductive particles on an Au bump, of area 1024 μ m², was calculated. Then, the Si chip and glass were aligned and pressed at the condition of 80 °C for 30 s at 120 MPa so that the polymer resin can fill the empty regions between the chip and substrate. The aligned Si chip and glass were finally bonded at 270 °C for 15 s at 60 MPa, and then the electrical properties of the ACA joints were characterized.

To investigate the fundamental effects of the nanofiber on conductive particle movements, simulation of resin flow of both conventional and nanofiber ACAs was performed. It was assumed that the epoxy resins follow the characteristics of a Newtonian fluid. The total amount of resin is preserved, so-called continuity of fluid, and the Z-direction velocity caused by the joint gap reduction is constant. The Darcy's law related to the flow of a fluid through a porous medium was applied to the nanofiber ACAs. The schematic illustrations of resin flow simulation, conventional ACAs, and nanofiber ACAs were shown in Fig. 12.9.

The volumetric flow rate of epoxy resins on an Au bump can be calculated from the following Eq. (12.1) and bump dimensions (2x:y = 13:80)

$$Q(x, y, t) = 2x \cdot y \cdot W = 2x \cdot h \cdot v + 2y \cdot h \cdot u, \qquad (12.1)$$

where Q is the volumetric flow rate; W(t) is the Z-direction velocity caused by the joint gap reduction; x and y are the width and length of an Au bump, respectively; u(x,t) and v(y,t) are the flow velocities in the X and Y directions; and h(t) is the change of joint gap with time, t, that pressure is applied. From Eq. (12.1), the flow

velocity and the change of joint gap width can be expressed as the following Eqs. (12.2)-(12.4).

$$\mathbf{u}(\mathbf{x},t) = \frac{2}{3} \frac{\mathbf{x} \cdot \mathbf{W}}{\mathbf{h}(t)} \tag{12.2}$$

$$\mathbf{v}(\mathbf{y}, \mathbf{t}) = \frac{1}{3} \frac{\mathbf{y} \cdot \mathbf{W}}{\mathbf{h}(\mathbf{t})} \tag{12.3}$$

$$h(t) = \frac{h^* - h_o}{t^*} \cdot t + h_o$$
(12.4)

where h_o and h^* are the initial and final joint gaps at t = 0 and $t = t^*$, before and after bonding. The pressure difference, which eventually correlates to the tensile strength of the nanofiber structure of nanofiber ACAs, was calculated by integrating the Darcy's equation (Eq. 12.5). Tensile strength applied to the X and Y directions follows Eqs. (12.6) and (12.7).

$$\nabla P_{\text{pressure}} = -\frac{\eta_{\text{viscosity}}}{K_{\text{permeability}}} \cdot \left[u(x,t) + v(y,t) \right]$$
(12.5)

$$\left|\nabla P_{x,_{pressure}}\right| = \int_{0}^{b} \left[\frac{\eta_{viscosity}}{K_{permeability}} \cdot u(x,t)\right] dx = \frac{1}{3} \cdot \frac{\eta_{viscosity}}{K_{permeability}} \cdot \frac{x^2 \cdot W}{h^*} = \sigma_x \quad (12.6)$$

$$\left|\nabla P_{y,_{\text{pressure}}}\right| = \frac{1}{6} \cdot \frac{\eta_{\text{viscosity}}}{K_{\text{permeability}}} \cdot \frac{y^2 \cdot W}{h^*} = \sigma_y$$
(12.7)

where ∇P is the pressure gradient, η is viscosity, K is permeability, and σ is the tensile strength.

12.2.4 Characterization of Electrical Properties

The insulation resistance between each adjacent pair of 24 bumps with 7 μ m spaces was evaluated by applying a constant voltage of 10 V and measuring current changes. The electrical short criterion of the X-Y axis insulation resistance was determined to be less than 10⁸ Ω . In situ Z-axis contact resistances were measured using nanofiber mats and the four-point structure during heating from 150 to 270 °C at 60 MPa.
12.2.5 Results and Discussion

12.2.5.1 Fabrication of CPIN Structure

Electrospinning Nylon 6 polymer was reported to produce nanofibers with diameters of several tenths of a nanometer in a spider web-like nanoweb, i.e., a two-dimensional nanofiber network structure enabled by electrically forced fast phase separation [19–21]. If conductive particles are incorporated in a nanofiber and each particle and the nanofiber can be anchored by the nanofiber and nanoweb, the conductive particles cannot freely move during the bonding processes. Therefore, Nylon 6 was considered as a polymer precursor to produce Nylon 6 CPIN. In this study, the mass-producible novel nanofiber ACAs were successfully demonstrated using an electrospinning process (Fig. 12.10a) to incorporate conductive particles into nanofibers and the lamination process of thermo-curable epoxy adhesive films on the CPIN mats.

The SEM image of CPIN (Fig. 12.10b) indicates that conductive particles with about 300 nm diameter were successfully incorporated into the Nylon 6 nanofiber and that they were randomly distributed. During the electrospinning process, electrically driven Nylon 6 jets which forced fast phase separation from liquid to solid produced ultrathin nanoweb structures of about 8 nm diameters (Fig. 12.10b, c) [20]. This nanoweb of nanofiber-nanofiber and conductive particle-nanofiber linkages form a strong network which effectively restrains the conductive particle movements during the resin flow. The cross-sectional SEM and TEM images (Fig. 12.10d, e) reveal that the conductive particle was coated by Nylon 6 nanofiber with the 50–90 nm thickness range. And this result was also confirmed by the elemental analysis of the TEM image (Fig. 12.10e). The thin polymer layer provided an additional insulating function between conductive particles as well.

12.2.5.2 Analysis of Conductive Particle Movement

To fabricate the novel nanofiber ACAs, 8 µm thick B-stage thermo-curable epoxy nonconductive films (NCFs) were laminated on the top and bottom sides of a CPIN mat at 80 °C; at this temperature, the epoxy resins can easily flow and penetrate into the CPIN without causing any epoxy curing. The fabricated ACAs had a composite structure with an epoxy adhesive film layer/CPIN layer/epoxy adhesive film layer. Therefore, the resulting structure can provide both functions of electrical conduction and mechanical adhesion between a chip and a substrate. In order to evaluate the nanofiber effects on conductive particle movements and electrical properties, conventional ACAs and the nanofiber ACAs were prepared using the same epoxy adhesive resins (only differences are the presence of nanofiber and the amount of conductive particles). Generally, the conductive particles in conventional ACAs can move freely without any obstruction during the resin flow, and a small number of particles are captured on Au bumps. For this reason, two or three times larger



Fig. 12.10 Fabrication and characterization of conductive particle incorporated nanofiber (CPIN) structures. (a) Schematic illustration of electrospinning setup, (b) SEM image of CPIN structures, (c) magnified SEM image of nanowebs, (d) cross-sectional SEM image of a CPIN, and (e) TEM image and elemental analysis result of nanofiber layer covering a conductive particle

numbers of particles were used in conventional ACAs to provide stable contact resistance to fine pitch display devices. After the resin flowing at 80 °C, the majority of particles were agglomerated between the Au bumps (Fig. 12.11a). However, the CPIN structure suppresses the free particle movements by the effects of nanofiber resistance to the external flowing force (Fig. 12.11b). The effects of the nanofiber on the conductive particle movements were observed using an optical microscopy after the bonding process (resin flowing at 80 °C and final bonding at 270 °C under 60 MPa pressure) of display driver COG substrate. In the case of conventional ACAs, only 27% of initial particles were captured on Au



Fig. 12.11 Conductive particle movements of conventional and nanofiber ACAs during bonding process. Schematic illustrations of chip-on-glass (COG) assembly bonded using (**a**) conventional ACAs and (**b**) nanofiber ACAs. And optical images of conductive particle distribution of COG assembly using (**c**) conventional ACAs and (**d**) nanofiber ACAs

bumps of a Si chip, and 73% were agglomerated around them (Fig. 12.11c). On the other hand, the nanofiber ACAs showed a 2.7 times higher capture rate at 74% and permitted fewer conductive particles agglomerated around the Au bumps, resulting in significantly reduced electrical short probability. The displacement of conductive particles in conventional ACAs calculated from Eqs. (12.2) and (12.3) is shown in Fig. 12.12a, b. The particles initially at the coordinate of (2.55 μ m, 50 μ m) were moved along with the resin flow and finally captured at a bump edge; therefore, the particles in the area of 5.11 μ m by 50 μ m could be captured on an Au bump. The percentage of the calculated area compared to the Au bump was 24.6% which is similar with the experimental results, 26.8% capture rate after resin flow (Figs. 12.12c and 12.13a). The calculated area in the case of nanofiber ACAs through the Darcy's law was 95.7%, and it also showed the almost same result with the measured capture rate, 97% (Figs. 12.12d and 12.13a).



Fig. 12.12 Displacement of conductive particles in (a) X direction and (b) Y direction of conventional ACAs and calculated capture rate of (c) conventional ACAs and (d) nanofiber ACAs

12.2.5.3 Effects of CPIN Structure of Nanofiber ACAs on Three-Dimensional Electrical Resistances

The effects of the nanofiber on conductive particle movements and short-circuit rates were quantitatively characterized in the views of the change of particle density and electrical resistance of neighboring Au bumps during a COG bonding process. The number of particles of the ACAs decreased from the initially designed 37 to 10 during adhesive resin flow, resulting in a capture rate of only 27%. However, in the case of nanofiber ACAs, about eight particles out of initial ten particles were captured, a capture rate of 74%, after the final ACA bonding process. It is clear that the nanofiber structure effectively prevented conductive particle movement during the bonding process. In other words, the majority of conductive particles of the conventional ACAs escaped from the bump joint area and agglomerated between bumps, resulting in an electrical short between bumps (Figs. 12.11a, 12.12c, and 12.14). The insulation properties of both the nanofiber ACAs and the conventional ACAs were investigated using the test patterns of insulation resistance for a total of 768 nearby joints. As one can see, the joints bonded using the ACAs showed wide range of insulation resistances from 75 to $10^{11} \Omega$, and 62.5% joints were electrically shorted because of the agglomeration of conductive particles between bumps (Fig. 12.13b, c). However, the nanofiber ACAs showed a 100% insulation property. Besides, Fig. 12.13 Effects of the nanofiber on conductive particle movements and short-circuit rates. (a) Changes of the number of conductive particles per a bump, (b) insulation resistances measured of 32 points (each point has 24 joint; therefore the total number of joints were 768) of COG assembly, and (c) short-circuit rates



another important advantage of the nanofiber ACAs is that they can reduce the material cost by reducing the initial number of added conductive particles, which are the most expensive materials in ACAs.

In addition, to prevent electrical shorts by suppressing conductive particle movements, it is also important to obtain stable and low Z-axis contact resistance. As explained before, the nanofiber can act as an excellent insulating material between particles and bumps. In order to provide a good electrical bump joint property, there should be no remaining nanofiber material at the interface between the captured conductive particles and the bumps. Therefore, the nanofiber materials should be melted at the final stage of the ACA bonding process. The effects of nanofiber melting on the electrical Z-axis contact resistance are shown in Fig. 12.14. In situ Z-axis contact resistances of the COG assembly were measured during the bonding processes from 150 to 270 °C under 60 MPa, and heat flow by a dynamic scanning calorimeter (DSC) with a heating rate of 10 °C/min and the compressive modulus of



Fig. 12.14 Temperature dependence of Z-axis contact resistances. (**a**) Contact resistances of COG assembly using Nylon 6 CPIN (left Y-axis), heat flow of Nylon 6 (right Y-axis), and compressive modulus of Nylon 6 (outermost right Y-axis) as a function of temperature. (**b**) SEM image of initial CPIN structure and cross-sectional SEM images of COG assembly bonded at 150 °C and 270 °C, respectively

Nylon 6 were measured with a heating rate of 10 °C/min under 200 mN. The endothermic heat flow around 230 °C indicates the melting temperature of the Nylon 6 (Fig. 12.14a, right axis). At this temperature, the electrical Z-axis contact resistance rapidly decreased from 60 to 0.48 Ω , and then the resistance was stabilized at about 0.13 Ω . The main reason for the higher electrical Z-axis contact resistances of COG assembly bonded at temperatures lower than 230 °C is that the Nylon 6 nanofiber layer remained at the interfaces of the conductive particles/Au bumps and conductive particles/electrodes (Fig. 12.14b). Although increased strain of Nylon 6 at the temperature due to decreased compressive modulus caused significant change of nanofiber morphology, the polymer layer still remained in the joint, resulting in higher Z-axis contact resistance of 60 Ω at 150 °C bonding temperature. In contrast, the conductive particles processed at temperatures higher than 230 °C showed direct contact between the conductive particle, the Au bump and the glass electrode, because the Nylon 6 nanofiber material was completely melted and squeezed out by the applied pressure during the final bonding process (Fig. 12.14b).

12.2.6 Summary

The nanofiber ACAs substantially suppress the conductive particle movements during ACAs bonding processes. Among the many nanofiber polymer resins, the Nylon 6 nanofiber ACAs produced the best electrical insulation and Z-axis contact resistance, and it showed remarkable improvements compared to the conventional ACAs. Therefore, nanofiber ACAs can solve the current technical limitations of fine pitch assembly less than 20 μ m for next-generation COF and COG display applications.

12.3 Effects of Nanofiber Material Properties on Nanofiber ACAs Interconnection Stability

12.3.1 Introduction

In the previous section, nanofiber ACAs with conductive particles incorporated within nanofibers in CPIN structures were introduced as a fundamental approach to minimize conductive particle movements. New nanofiber ACAs combined with various nanofiber materials to obtain better electrical performance for ultra-fine pitch applications are considered in this section. Nanofiber ACAs are composite materials composed of curable adhesive resin and CPIN structure. As the previous results have shown for 7 μ m spaced bumps, nanofiber ACAs showed stable Z-axis contact resistance and excellent X-Y axis insulation properties. However, there is no previous investigation about the effects of nanofiber material properties on the captured conductive particle density, insulation resistance, and contact resistance, although nanofiber material properties such as tensile strength and melting temperature can significantly affect the nanofiber behavior during the nanofiber ACA bonding processes. The mechanical and thermal properties of nanofiber polymers depend on the chemical structures and molecular weight of polymer material as well as nanofiber diameter and electrospinning conditions [22–28].

In this section, the effects of nanofiber thermal and mechanical material properties on ACAs interconnection stability are considered for fine pitch applications. Three kinds of nanofiber materials, polyvinylidene fluoride (PVDF), ethylene vinyl alcohol (EVOH), and Nylon 6, which have different tensile properties and melting temperatures, are coupled with conductive particles to form PVDF-CPIN, EVOH-CPIN, and Nylon 6-CPIN, respectively, with three nanofiber ACAs fabricated and characterized.

12.3.2 Experiments

12.3.2.1 Fabrication of Nanofibers and CPIN (Conductive Particle Incorporated Nanofibers)

Polyvinylidene fluoride (PVDF), ethylene vinyl alcohol (EVOH), Nylon 6, dimethylacetamide (DMAc), acetone, 1-propanol, and formic acid were used as raw materials. The electrospinning conditions were optimized for each polymer material as listed in Table 12.1. 18 wt% of PVDF was dissolved in the solvent mixture of DMAc and acetone with the same ratio and electrospun by applying 8 KV. The optimized polymer concentration of EVOH was 13 wt% in the mixture of 1-propanol and distilled water. 6.5 KV was applied to the EVOH solution to produce uniform nanofibers. A Nylon 6 solution in 75 wt% formic acid was electrospun by applying a high voltage of 15 KV between the solution and target. The pump rate, working distance, and needle diameter were set as 10 μ L/min, 10 cm, and 150 μ m, respectively.

The process of incorporating conductive particles into three kinds of nanofibers was performed using the optimized ratio of polymer and the conductive particles. The calculated polymer volumes of PVDF, EVOH, and Nylon 6 were 0.62 mL, 0.62 mL, and 1.54 mL on the basis of 5 g of solvent, because each polymer has a different density, as listed in Table 12.2. When the individual ratio of polymer and conductive particles of PVDF, EVOH, and Nylon 6 were 1:0.90, 1:0.61, and 1:1, respectively, the particle contents per unit polymer volume were almost the same at 1.08 g/mL. The optimized contents of conductive particles were added to each polymer solution and electrospun using the electrospinning conditions summarized in Table 12.1 to fabricate CPIN structures.

Conditions	PVDF EVOH		Nylon 6	
Polymer concentration	18 wt%	13 wt%	25 wt%	
Solvent	DMAc, acetone (1:1)	1-propanol, DI water (1:1)	Formic acid	
Voltage	8 KV	6.5 KV	15 KV	
Pump rate	10 µL/min			
Working distance	10 cm			
Needle diameter	150 µm			

Table 12.1 Electrospinning conditions used in this study

 Table 12.2
 The optimized conductive particle contents per unit volume of polymers

Conditions	PVDF	EVOH	Nylon 6
Polymer density	1.77 g/mL	1.2 g/mL	1.08 g/mL
Polymer volume	0.62 mL	0.62 mL	1.54 mL
Polymer conductive particles	1:0.90	1:0.61	1:1
Conductive particles (g)/polymer (V)		1.08 g/mL	



Fig. 12.15 Micro-tensile test equipment for measuring the tensile properties of nanofibers

12.3.2.2 Tensile Test of Nanofiber Mats

Tensile tests of PVDF, EVOH, and Nylon 6 nanofibers were performed using the D638 condition of ASTM standard at 80 °C, because at this temperature tensile stress by epoxy resin flow is applied to the nanofiber. Every nanofiber was cut as test sample type V of the D638, which has a gage length of 7.6 mm, width of 3.2 mm, and overall length of 63.5 mm, and maintained in a furnace at 80 °C for more than 3 min, as shown in Fig. 12.15. With a crosshead speed of 10 mm/min of a tensile tester, the tensile strengths of three kinds of nanofiber were measured.

12.3.2.3 Analysis of Conductive Particle Movements

The conductive particle movements were analyzed using an optical microscope during the bonding process of an Au-patterned Si chip and a bare glass substrate using three kinds of nanofiber ACAs: PVDF, EVOH, and Nylon 6 nanofiber ACAs. To fabricate nanofiber ACAs, B-stage thermo-curable epoxy adhesive films were laminated on the top and bottom sides of a CPIN mat at 80 °C; at this temperature, the epoxy resins can easily flow and penetrate into the CPIN without causing any epoxy curing. The fabricated ACAs had a composite structure with an epoxy adhesive film layer/CPIN layer/epoxy adhesive film layer. Therefore, the resulting structure can provide both electrical conduction and mechanical adhesion between the chip and the substrate. In order to evaluate the tensile strength effects of nanofiber on conductive particle movements and X-Y axis insulation property, PVDF, EVOH, and Nylon 6 nanofiber ACAs as well as conventional ACAs were compared using the same epoxy adhesive resins. All ACAs were laminated on the Si chips, and the average number of conductive particles on an Au bump with an area of

1024 μm^2 was calculated. The Si chip and glass substrate were then aligned and pressed at 80 °C for 30 s at 120 MPa so that polymer resin could fill the empty regions between the chip and the substrate. Finally the aligned Si chip and glass were bonded at 200 °C in the case of PVDF nanofiber ACAs, 220 °C for the EVOH nanofiber ACAs, and 270 °C for the Nylon 6 nanofiber ACAs for 15 s at 60 MPa, and the capture rate of conductive particles was statistically characterized.

12.3.2.4 DSC (Differential Scanning Calorimetry) Behavior of Nanofibers

To investigate thermal properties of nanofiber on ACA interconnection stability, heat flow of polymer bulk materials and nanofiber materials was measured using a DSC equipment with the heating rate of 10 $^{\circ}$ C/min.

12.3.2.5 Characterization of Electrical Stability of Nanofiber ACA Interconnection

X-Y Axis Insulation Resistance

X-Y axis insulation resistance of 360 nearby bumps with 7 μ m spaces was evaluated by applying constant voltage of 10 V and measuring current changes as shown in Fig. 12.16a. The electrical short criterion of the X-Y axis insulation resistance was determined to be less than 10⁸ Ω .

Z-Axis Contact Resistance

In situ Z-axis contact resistances of COF assembly bonded using PVDF, EVOH, and Nylon 6 CPIN structures at the increased temperature from 80 to 270 °C were measured using a four-point structure, as shown in Fig. 12.16b. These results were correlated with the DSC scan results in order to analyze the effects of nanofiber melting on contact resistance. The Z-axis contact resistance of nanofiber ACAs COF assemblies were bonded at various temperatures, 200 °C for PVDF nanofiber ACA, 220 °C for EVOH nanofiber ACA, and 270 °C for Nylon 6 nanofiber, because each nanofiber had different melting temperatures.



12.3.3 Results and Discussion

12.3.3.1 Effects of Tensile Strength of Nanofibers on Conductive Particle Movements and X-Y Axis Insulation Resistance

The tensile properties of the nanofiber materials of nanofiber ACAs play an important role in controlling conductive particle movements during adhesive resin flow. The capability of nanofiber ACAs to withstand the resin flowing force depends on the tensile properties of the nanofiber materials such as the ultimate tensile strength (UST) and degree of strain. According to the viscosity and curing behavior of the epoxy resin used in this study, the minimum viscosity was obtained at 80 °C without any epoxy curing reaction. For this reason, the tensile test of the nanofiber materials was also performed at 80 °C to investigate the effects of the tensile properties of the nanofiber materials on conductive particle movements. SEM images of electrospun PVDF, EVOH, and Nylon 6 nanofiber are shown in Fig. 12.17. Nylon 6 and PVDF are well-known engineering thermoplastics having superior tensile strength and toughness relative to other thermoplastics. The tensile properties of Nylon 6 and



Fig. 12.17 SEM images of (a) PVDF, (b) EVOH, and (c) Nylon 6 nanofibers



Table 12.3 Tensile properties of PVDF, EVOH, and Nylon 6 nanofibers

Properties	PVDF	EVOH	Nylon 6
Ultimate tensile strength (MPa)	16.20	9.40	19.24
Elastic modulus (MPa)	12.38	43.98	26
Strain (%)	5.73	3.52	2.82

PVDF nanofiber were better than those of EVOH nanofiber as well (Fig. 12.18). The Nylon 6 nanofiber showed the highest UTS value, 19.2 MPa, with PVDF nanofiber and EVOH, respectively, presenting values of 16.2 MPa and 9.4 MPa. However, the EVOH nanofiber had a 1.7 and 3.5 times higher elastic modulus than that of Nylon 6 and PVDF nanofibers, respectively, due to its semicrystalline structure originating from the repeating unit of its ethylene group. Meanwhile PVDF nanofiber showed the largest strain, because it had a lower glass transition temperature (Tg) of about -35 °C. The tensile properties of the three kinds of nanofibers are summarized in Table 12.3.

The conductive particle movements of nanofiber ACAs fabricated by laminating adhesive resins on CPIN structures were analyzed during the bonding process. The bonding process was divided into two steps, the resin flowing step to fill the spaces and reduce the gap between the chip and the substrate and the main bonding step to provide stable joint contact by complete melting nanofiber layers and full curing epoxy resins. With respect to the UTS value, Nylon 6 nanofiber ACA, having the highest UTS, successfully suppressed the particle movement, showing a 97% capture rate after resin flow and a 77% rate after the main bonding step. The reduction of the capture rate during the main bonding is due to additional reduction of the joint gap between the chip and the substrate, because the 5–7 µm thickness Nylon 6 nanofiber structure was completely melted and conductive particles were sufficiently deformed (Figs. 12.19 and 12.20). The capture rate of EVOH nanofiber ACAs was changed from 68.6% to 61.4% during the two-step bonding processes. This result indicates that stronger nanofibers can withstand resin flow effectively



resulting in better conductive particle capture rate. Nylon 6 showed a higher capture rate than PVDF (97% versus 85.2%) after resin flow, due to the stretchable property of PVDF. Therefore, it was confirmed that the tensile properties of the nanofibers significantly affect the conductive particle movements. Nevertheless, nanofiber ACAs showed an improved particle capture rate in a range of 61–77%, which is roughly 2–3 times higher than that of the conventional ACAs. From the results, in order to thoroughly suppress particle movements during resin flow, the nanofiber should have UTS value larger than 9.4 MPa and strain value lower than 5.7. Meanwhile, the X-Y axis insulation resistances of 360 joints of a COF assembly bonded using nanofiber ACAs ranged from 10^{10} to $10^{11} \Omega$, which is higher than the short criterion of $10^8 \Omega$, and consequently no electrical short circuits occurred with the use of the nanofiber ACAs. However, conventional ACAs showed 66% insulated circuit rate (Fig. 12.21). The nanofiber ACAs exhibited not only suppressed conductive particle movements during resin flow but also improved X-Y axis insulation characteristic.

Fig. 12.21 The insulated

circuit rates of conventional

ACAs, PVDF, EVOH, and Nylon 6 nanofiber ACAs



12.3.3.2 Effects of Thermal Properties of Nanofiber on Z-Axis Contact Resistance

Along with tensile properties, the thermal properties of nanofibers are important characteristics for nanofiber ACAs. Reducing material size down to a nanoscale affects material properties such as thermal and electrical properties as well as mechanical properties. Similar results can be observed in nanofiber polymer materials. A DSC analysis of the bulk and nanofiber structure of PVDF, EVOH, and Nylon 6 was conducted, and the results are shown in Fig. 12.22. The upper solid line indicates the heat flow of nanofiber materials, and the lower dotted line represents that of bulk materials. The heat flow of PVDF nanofiber started to increase at around 140 °C, which is the starting point of material melting, and peaked at 164.9 °C, the peak melting temperature of PVDF nanofiber. The peak melting temperature of PVDF nanofiber showed a 2–4.5 °C lower peak melting temperature than their bulk materials (Fig. 12.22).

To investigate the nanofiber melting effects, in situ Z-axis contact resistances of COF assemblies bonded using PVDF, EVOH, and Nylon 6-CPINs were measured from 80 to 270 °C. The contact resistance of all samples abruptly decreased below 300 m Ω from the starting point of nanofiber melting and stabilized to 4–6.4 m Ω above the melting temperature of nanofiber (Figs. 12.23 and 12.24). PVDF, EVOH, and Nylon 6-CPIN were completely melted at 200, 220, and 270 °C, respectively. The bonding temperature of Nylon 6 nanofiber was higher than that of the other nanofiber ACAs, because it has a 30–60 °C higher melting temperature. However, the Z-axis contact resistance of the COF assembly bonded using Nylon 6 nanofiber ACA was sufficiently low, below 10 m Ω , which is the same as the values of conventional ACAs (Fig. 12.25). Stable joint formation was observed as well. Furthermore, PVDF and EVOH nanofiber ACAs also produced stable contact resistance and joint formation despite of different bonding temperatures.











12.3.4 Summary

Noble nanofiber ACAs were demonstrated, and the effects of nanofiber material properties on nanofiber ACA interconnection stability were investigated in terms of tensile properties and thermal properties of nanofiber materials. The Nylon 6 nanofiber showed the highest UTS of 19.2 MPa compared to PVDF nanofiber having 16.2 MPa and EVOH having 9.4 MPa resulting in the highest conductive particle capture rate. Although the three kinds of nanofiber ACAs showed different conductive particle capture rates, they all showed perfect X-Y axis insulation properties at 20 μ m pitch interconnections of COF assembly. The Z-axis contact resistance of all samples abruptly decreased below 300 m Ω from the starting point of

Fig. 12.24 SEM images of nanofibers before and after melting (**a**) PVDF, (**b**) EVOH, and (**c**) Nylon 6-CPIN structures



nanofiber melting and stabilized at 4–6.4 m Ω above the nanofiber peak melting temperature. All nanofiber ACAs showed excellent conductive particle capture rate, perfect X-Y axis insulation property, and stable Z-axis contact resistance. Therefore, nanofiber ACAs can solve the current technical limitations of fine pitch assembly at less than 20 μ m for next-generation display applications.

12.4 Micro-solder Ball Incorporated Nanofiber Anisotropic Conductive Adhesives (Nanofiber Solder ACAs) for Fine Pitch COF Assembly

12.4.1 Introduction

Electronic packaging technology has advanced in the direction of integrating diverse components into one package to satisfy the demands for multifunctionality as well as portability [29, 30]. For this reason, various packaging structures have been introduced, for instance, multi-chip module (MCM), package on package (POP), package in package (PIP), and eventually 3D chip stacks [31–34]. All those approaches require increased input/output (I/O) counts, resulting in fine pitch assembly [10, 35]. Therefore, the most critical issue in current electronic packaging is how to assemble fine pitch components without electrical shorts in the X-Y direction [10, 36–39]. There has been much research on fine pitch interconnecting technology using micro-solder balls less than 200 μ m pitch, but the problems of solder ball handling and low yield still remain [40–43]. In addition, there have been very few reports so far about the fine pitch interconnection below 25 μ m pitch using micro-solder balls especially for 3D chip through silicon via (TSV) stacks with Cu/Sn-Ag hybrid bumps [35, 39, 44].

In this section, a new electronic packaging interconnection material is introduced that makes 25 μ m pitch interconnection possible using micro-solder balls. A new

concept of nanofiber ACAs have been introduced to suppress the conductive particle movement during resin flow and to improve the fine pitch capability through the nanofiber structure [7, 17, 45–48]. Using the same concept, micro-solder balls are incorporated into the nanofiber by an electrospinning method. Micro-solder/ nanofiber structure embedded in polymer adhesive resins can suppress the micro-solder ball movement during resin flow, because the micro-solder balls are tied up with nanofiber structure.

12.4.2 Experiments

12.4.2.1 Incorporation of Micro-solder Balls into Nanofiber by an Electrospinning Method

Nylon 6, formic acid, 3 µm diameter Ni-/Au-coated polymer ball, and micro-solder balls (Sn3.0Ag0.5Cu) were used. The size distribution of micro-solder balls was from 400 nm to 6 µm, and the average diameter was about 2 µm (Fig. 12.26). The number of conductive balls was determined on the basis of the total number of balls in the Nylon 6 solution. As shown in the equation below, the number of polymer balls and micro-solder balls can be calculated using the polymer ball density (d_p), polymer ball diameter (r_p), micro-solder density (d_{MS}), and micro-solder ball diameter (r_{MS}).

$$N_{p} = N_{MS} = \frac{W_{p}}{d_{p}^{*} V p} = \frac{W_{MS}}{d_{MS}^{*} V_{MS}}$$

$$d_{p} = 3.07 \qquad d_{MS} = 7.37$$

$$r_{p} = 1.5 \ \mu m \quad r_{MS} = 0.95 \ \mu m$$
(12.8)

where N is the number, W the weight, and V the volume of conductive particles in the ACAs.

The Nylon 6 solutions containing either polymer balls or micro-solder balls were transferred to the syringe of an electrospinning machine and were then electrospun by applying 15 kV of electrical voltage between the needle of the syringe and the grounded Al target at a pump rate of 10 μ L/min. More detailed electrospinning conditions are listed in Table 12.4. Micro-solder ball incorporated nanofiber and polymer ball incorporated nanofibers were dried in a vacuum oven at 120 °C for 1 h and then pressed at 160 °C for 30 s to obtain dense nanofiber structures. The morphology and cross-sectional image of micro-solder/nanofiber was analyzed using a field emission scanning electron microscopy (FE-SEM) and focused ion beam (FIB) system.



 Table 12.4
 Electrospinning conditions of polymer ball/nanofiber and micro-solder ball/nanofiber

 Conditions
 Polymer ball
 Micro-solder ball (Sn3.0Ag0.5Cu)

Conditions	Polymer ball	Micro-solder ball (Sh5.0Ag0.5Cu)
Nylon 6: conductive ball	1:1	1:0.57
Nylon 6 concentration	25 wt% in formic aid	
Voltage	15 kV	
Pump rate	10 µL/min	
Working distance	10 cm	
Needle diameter	150 μm	



12.4.2.2 Analysis of the Soldering Behavior of Micro-solder Balls Within the Nanofiber/Epoxy Matrix

The solderability of nanofiber solder ACAs is the most important property for good electrical interconnection. The B-stage epoxy films were laminated on a microsolder ball/nanofiber mat. And then, the Si chip having 25 μ m bump pitch was bonded on a glass substrate using nanofiber solder ACAs at a temperature ranging from 170 to 270 °C with increments of 20 °C for 15 s under a pressure of 60 MPa. The soldering behavior was observed using an optical microscopy.

12.4.2.3 Analysis of the Interconnection Stability of Nanofiber Solder ACAs

The size of a Si chip is 16×1.5 mm with 700 µm thickness, and the chip has 1163 peripheral I/O patterns of electroplated Au bumps with dimensions of 13 µm width, 80 µm length, and 10 µm height. Both the chip and flexible substrate have the patterns of 25 µm pitch, as shown in Fig. 12.27. The interconnection stability of the nanofiber solder ACAs was investigated by measuring the electrical resistances and observing the joint morphologies of COF assembly and was compared with that of the polymer ball nanofiber ACAs. To investigate the interfacial reaction of microsolder balls between the Au bump and the Sn-coated Cu electrode, TEM analysis was performed. The COF assembly contains two kinds of electrical test structures: the four-point structure for Z-axis contact resistance measurement and insulation structure for X-Y axis insulation resistance was determined to be less than $10^8 \Omega$.

12.4.2.4 Reliability Test

An unbiased autoclave test fulfilling the JEDEC standard (JEDEC STD-22-B, Method A102) was conducted. This test employed severe conditions of pressure, humidity, and temperature that accelerate the penetration of moisture through the nanofiber solder ACAs. The COF assemblies bonded using polymer ball nanofiber ACAs and nanofiber solder ACAs were loaded into an autoclave chamber heated to 121 °C under 2 atm pressure at 100% relative humidity for 48 h. The Z-axis contact resistance was measured during the autoclave test with intervals of 12 h. When the measured resistance was higher than 100 m Ω , it was determined that the bump joint was electrically failed.

Fig. 12.27 SEM images of 25 μm pitch patterns of (**a**) a Si chip and (**b**) a flexible substrate



12.4.3 Results and Discussion

12.4.3.1 Micro-solder Ball Incorporated Nanofiber

Nylon 6 has been known as a good polymer to produce nanofiber as well as nanowebs, which are two-dimensional nanofiber networks enabled by electrically forced fast phase separation [20, 21]. Nylon 6 nanofiber can effectively incorporate conductive balls through an electrospinning method. In this section, micro-solder balls were incorporated into Nylon 6 nanofiber in order to suppress the micro-solder ball movement during the resin flow and to form stable Sn3.0Ag0.5Cu solder joints between fine pitch Au bumps of a chip and Sn-finished Cu electrodes of a flexible substrate. Therefore, fine pitch interconnection stability at 12 µm bump space can be achieved using nanofiber solder ACAs in terms of joint morphologies and electrical



Fig. 12.28 (a, b) SEM images of micro-solder/nanofiber composite and (c) cross-sectional SEM image of micro-solder/nanofiber composite

properties. When an electric voltage of 15 KV was applied to the Nylon 6 solution, the charged solution was stretched toward the grounded Al target, and formic acid was evaporated simultaneously. The resulting nanofiber structure is shown in Fig. 12.28. The SEM images of micro-solder/nanofiber composite show that the micro-solder balls were incorporated into Nylon 6 nanofiber with random distribution, and the average nanofiber diameter was about 270 nm. Both nanofiber and nanofiber-coated micro-solder balls were networked by ultrathin nanowebs whose diameter was from about 7 to 17 nm. The cross-sectional SEM image (Fig. 12.28c) indicates that micro-solder balls were successfully wrapped with a nanofiber layer as well. It is considered that the polymer layer covering the micro-solder balls can provide an electrically insulating effect between micro-solder balls and fine pitch electrodes.

12.4.3.2 Soldering Behavior of Micro-solder Balls Within the Nanofiber/Epoxy Matrix

An understanding of the soldering behavior of micro-solder balls is important for using nanofiber solder ACAs. The soldering behavior of micro-solder balls was different from that of conventional Sn3.0Ag0.5Cu solder balls, because the solder balls were incorporated into the nanofiber structure and the epoxy matrix. To obtain stable solder joints, the bonding conditions should satisfy the following requirements. First, the micro-solder balls have to directly contact the Au bumps and Sn-coated copper electrodes. Second, sufficiently higher temperature than the melting temperature of Sn3.0Ag0.5Cu (218 °C) should be applied to the solder ball joint. A Si chip and a nanofiber solder ACA laminated glass substrate were bonded at various temperatures from 170 to 270 °C for 15 s to determine the solder wetting temperature (Fig. 12.29). At temperatures lower than 210 °C, the microsolder balls were slightly deformed due to the bonding pressure of 60 MPa, while the micro-solder balls were partially wetted on Au bumps over 230 °C, and completely wetted at 270 °C, because the melting temperature of Nylon 6 was 222.3 °C. At 270 °C, the molten micro-solder balls were completely wetted between Au bumps and Sn-finished Cu electrodes, and the epoxy resins were cured at the same time.



Fig. 12.29 Soldering behavior of micro-solder balls incorporated in the nanofiber solder ACAs at various bonding temperatures



Fig. 12.30 Cross-sectional SEM images of (a, b) polymer ball/nanofiber joint and (c, d) microsolder/nanofiber joint

12.4.3.3 Interconnection Stability of the Nanofiber Solder ACAs

Figure 12.30 shows the joint morphologies of the COF assembly bonded using polymer ball nanofiber ACAs and nanofiber solder ACAs. Figure 12.30a, b shows that the polymer ball was deformed and in good contact with the Au bump and electrode without any Nylon 6 nanofiber entrapped layer. Unlike the polymer ball nanofiber ACAs, in the case of the nanofiber solder ACAs, continuous Au-Sn-Cu alloy was observed between the Au bump and the electrode (Fig. 12.30c, d). Continuous solder wetting without flux material used in the conventional soldering process could be possible presumably due to the broken native Sn oxide layer of the molten solder by applied pressure. Two kinds of alloys were observed at the microsolder ball joint: the Au-Sn-Cu alloy at the position 1 and Cu₃Sn at the position 2, as shown in Fig. 12.31 and Table 12.5. In general, Cu₆Sn₅ and Cu₃Sn intermetallic compounds (IMCs) are formed at the interface of Sn3.0Ag0.5Cu solder and Cu pad [49]. However, in this case, (Au,Cu)Sn IMC with substantial amount of Au was also observed because of the Au bumps [50].

In addition to joint morphologies, electrical properties of COF assembly were also analyzed to investigate the interconnection stability. The Z-axis contact resistance of the nanofiber solder ACAs was 4.6 m Ω , which was 12% lower than that of the polymer ball/nanofiber ACAs because of metallurgical solder alloy contact rather

Fig. 12.31 FIB SEM image of a micro-solder ball joint



Table 12.5Compositionalanalysis of micro-solder jointof Fig. 12.31		Au		Sn		Cu	
	Position	wt%	At%	wt%	At%	wt%	At%
	1	64.56	50.86	32.96	43.09	2.47	6.04
	2	1.62	0.64	37.42	24.57	60.96	74.79

than physical contact of polymer balls (Fig. 12.32a). The insulated circuit rates of both the polymer ball/nanofiber ACAs and the nanofiber solder ACAs were 100%, as shown in Fig. 12.32b. As a summary, the nanofiber solder ACAs successfully demonstrated excellent micro-solder ball wetting, stable Z-axis contact resistance, and excellent fine pitch capability at a 25 μ m fine pitch COF assembly.

12.4.3.4 Unbiased Autoclave Reliability

The unbiased autoclave reliability (also known as a pressure cooker test) is an accelerated moisture resistance test to rapidly penetrate moisture along the interface between the ACAs and other components such as Si chips or substrates. Usually, the deterioration of contact joints starts from the outermost area of electronic packages assembled using adhesives. This phenomenon is clearly observed in the case of polymer ball/nanofiber ACA as shown in Fig. 12.33a, b which indicated the rapid contact resistance increase. However, Fig. 12.33c, d show the no contact resistance increase and very stable resistance values for nanofiber solder ACAs. In the case of polymer ball/nanofiber ACAs, the contact resistance rapidly increased after 12 h, and





about 7% of the total contact joints failed after 48 h. And the averaged contact resistance increased from 5.2 ± 1.1 to 39.0 ± 142.7 m Ω . These problems were due to the deterioration of physical contact of polymer ball between Au bump and Cu electrode by the hygroscopic expansion of polymers. On the other hand, for nanofiber solder ACAs joints, the metallurgical solder alloy contact formed as (Au,Cu)Sn and Cu₃Sn IMCs significantly improved the unbiased autoclave reliability. The Z-axis contact resistances of micro-solder/nanofiber ACAs were much more stable than that of the polymer ball/nanofiber ACAs because of the metallurgical contact of nanofiber solder ACAs. There also was no failure joint observed in the nanofiber solder ACA joints after the PCT test.

12.4.4 Summary

In this section, very stable contact resistances, perfect X-Y axis insulation, and excellent unbiased autoclave reliability were obtained at the 25 μ m pitch of COF assembly using nanofiber solder ACAs. The nanofiber solder ACAs were fabricated by laminating epoxy adhesive films on a micro-solder ball incorporated nanofiber mat made by electrospinning Nylon 6 solution containing micro-solder balls. Micro-



Fig. 12.33 Unbiased autoclave reliability test results. (a) Accumulative distribution and (b) average Z-axis contact resistance of polymer ball/nanofiber ACAs joint and (c) accumulative distribution and (d) average Z-axis contact resistance of nanofiber solder ACAs joint

solder balls were successfully incorporated into the Nylon 6 nanofiber structure, and because of solder wetting on the Au bumps and Sn-finished copper electrodes, (Au, Cu)Sn and Cu₃Sn IMCs were formed at the interface. The continuous IMCs formed in micro-solder ball joint lowered the Z-axis contact resistances and significantly improved moisture resistance compared with the physical contact-based conventional polymer ball contact. Therefore, the nanofiber solder ACAs can provide an excellent alternative solution for fine pitch interconnections of various electronic assemblies such as COF, COG, and 3D chip stacks.

12.5 Conclusion

Display-related electronics such as cellular phones, laptops, and UHD televisions require higher resolution and finer electrode pitch, which is the center-to-center distance between nearby electrodes. The most critical issue for interconnecting the fine pitch driver chip on a high-resolution display panel using anisotropic conductive adhesives (ACAs) is an electrical short circuit between neighboring electrodes, because conductive particles can be agglomerated between fine pitch electrodes during the bonding process resulting in display defects. In this study, a new concept

of nanofiber ACAs that incorporates conductive particles into nanofibers to suppress conductive particle movement was demonstrated, and nanofiber materials were optimized in terms of their tensile properties and melting temperatures. Finally, the concept of nanofiber ACAs can be successfully extended to the novel nanofiber solder ACA to achieve lower contact resistance, perfect insulation property, and excellent reliability for 20 µm pitch COF assembly.

In Sect. 12.2, novel nanofiber ACAs that incorporate conductive particles into nanofiber structure to obtain stable electrical properties of fine pitch display devices were introduced. The conductive particle movements during adhesive resin flow were fundamentally suppressed by the conductive particles being incorporated into the nanofiber (CPIN) structure. The nanofiber ACAs showed superior characteristics compared to the conventional ACAs, providing 2.7 times higher particle capture rate and outstanding insulation properties at 20 μ m fine pitch interconnections.

Section 12.3 showed the effects of material properties of the nanofiber on nanofiber ACA interconnection stability in terms of tensile properties and thermal properties of nanofiber materials. The Nylon 6 nanofiber showed the highest ultimate tensile strength, 19.2 MPa, whereas the PVDF nanofiber and EVOH presented values of 16.2 MPa and 9.4 MPa, and therefore Nylon 6 showed the highest conductive particle capture rate. Although three kinds of nanofiber ACAs showed different capture rates, they had perfect X-Y axis insulation properties at 25 μ m pitch COF assembly. The Z-axis contact resistance of all samples abruptly decreased below 300 m Ω from the starting point of nanofiber melting and stabilized to 4–6.4 m Ω above the nanofiber melting temperature.

Section 12.4 demonstrated a fine pitch COF assembly using nanofiber solder (Sn3.0Ag0.5Cu) ACAs which offer several advantages, such as suppressing microsolder ball movement during resin flow, perfect X-Y axis insulation at 25 μ m fine pitch, and improved unbiased autoclave reliability. Micro-solder balls were successfully incorporated into nanofiber structures and showed good solderability within the nanofiber/epoxy matrix. (Au,Cu)Sn and Cu₃Sn IMCs were formed through an interfacial reaction of Au bumps, Sn3.0Ag0.5Cu, and Sn-finished Cu electrodes. The continuous IMCs formed in micro-solder ball joints lowered the Z-axis contact resistances and significantly improved moisture resistance compared with the physical contact-based conventional polymer ball ACAs. As a result, nanofiber solder ACAs can provide an excellent alternative solution for fine pitch interconnections of various electronic assemblies such as COF, COG, and 3D chip stacks.

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Chapter 13 Nanoparticles in Microvias



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13.1 Introduction

Electronic packaging provides for mounting and physical support of electronic components, removal of heat from devices (e.g., integrated circuit chips), protection of devices from the environment, and electrical interconnection of components. This electrical interconnection enables distribution of both electronic signals and power throughout the package by means of multiple layers of metal circuit traces. Electrical interconnection between layers (vertically) is typically made with drilled and plated holes.

The demand for high-performance, lightweight, portable computing power is driving the microelectronics industry toward miniaturization of many electronic products and the components that comprise them [1]. Greater I/O density of IC chips and more demanding performance requirements necessitate greater wiring density and a concomitant reduction in feature sizes for electronic packages. To incorporate a greater degree of electronic function into a smaller volume, circuit traces and the holes used to connect them must have smaller physical dimensions [2–6]. The term "microvia" has been coined to describe small holes used for layer-to-layer electrical interconnection. Somewhat arbitrarily, they are generally accepted to have diameters on the order of 150 μ m or smaller.

Today, the high end of the semiconductor market appears to be standard application-specific integrated circuits (ASICs), structured ASICs, and fieldprogrammable gate arrays (FPGAs). These devices continue to need an increasing number of signal, power, and ground die pads. A corresponding decrease in pad

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pitch is required to maintain reasonable die sizes. The combination of these two needs is pushing complex semiconductor packaging designs. This packaging challenge is especially critical in flip-chip ball grid array (BGA) packages where the need for density has to coexist with good electrical, thermal, and reliability performance. Migration from wirebond to flip-chip packages has been driven by the need to combine electrical and thermal performance advantages with density, without compromising component reliability. In flip-chip designs, the backs of the die are exposed, so direct access is available for heat sinking as opposed to a wirebond die-up package. Further, flip-chip packaging provides improvements in electrical performance, such as reduced power supply noise due to reduction in inductance as well as increases in power and ground connections. Flip-chip packaging also provides significant increases in the number of rows of signal die pads that can be interconnected. However, typical flip-chip packages increase the mechanical coupling of the die to the printed wiring board. This normally results in lower reliability performance, either at the die bumps, as in the case of organic BGAs, or at the printed wiring board (PWB)-to-package interface, as is the case for ceramic BGA packages. Various interconnection methods have been employed to compensate for this increased coupling. Although a typical plastic flip-chip package normally exhibits good BGA reliability, the coefficient of thermal expansion (CTE) mismatch between die and package typically limits the size of the device that can be used. Techniques such as BGA ball depopulation under the die, at the corners of the die, or at the die periphery, reduce mechanical coupling and therefore allow increased device sizes. Unfortunately this reduces the improvement in signal I/O. Ceramic flip-chip packages have good CTE match to silicon. However, these packages have a large CTE mismatch to the printed wiring board. This constrains the package size and, in turn, constrains the package I/O. There are new materials that increase the CTE of the ceramic package to provide increased second level reliability performance at the expense of additional CTE mismatch to the die. Replacement of the BGA ball by a solder column is also helpful.

Specific organic package material sets have been investigated and developed to eliminate the deficiencies of both typical plastic and ceramic packages. A highly compliant poly(tetrafluoroethylene) (PTFE) material has been proven [7] to meet all these organic flip-chip reliability challenges. But each new generation of device technology places further significant pressures on package density.

There are a number of traditional approaches to reducing size and increasing density in packages. These include reduction in the width and spacing of metal traces and the addition of wiring layers. Formation of circuit features with reduced dimensions by subtractive techniques is facilitated by the use of thinner metals (typically copper), but this sometimes compromises electrical performance by way of higher resistance of the thinner, narrower circuit lines. This shortcoming may be mitigated somewhat by the use of semi-additive (or pattern plating) processes to form lines having a greater aspect ratio (ratio of line height to line width). Adding wiring layers is a straightforward means of providing greater density of function in the package. However, added layers invariably translate to added cost. It is therefore imperative to make the most efficient use of real estate used for wiring in order to keep the number



of wiring layers to a minimum. For interconnection with traditional plated throughhole (PTH) technology, two PTHs are required to complete a circuit trace. PTHs block channels that could otherwise be used for wiring (Fig. 13.1a). Packaging designs that are most effective in optimizing the use of available wiring space incorporate blind and buried vias. As opposed to PTHs, blind and buried vias do not span the full thickness of the substrate. A blind via is formed in a manner whereby it terminates on a previously formed metal feature internal to the substrate and is subsequently metallized. A buried via is formed as a through hole in a thin core. Following metallization and formation of circuit traces, the thin core is laminated with other subcomposites into a thicker substrate. In this chapter, the term microvia is used to describe both blind and buried vias with small dimensions. Blind and buried vias provide for vertical electrical interconnection that can be terminated at any wiring plane(s), at any depth, within the packaging structure. Replacement of conventional plated through holes with such vertically terminated vias opens up additional wiring channels on layers above and below the terminated vias.

As via diameters decrease to accommodate more dense designs, plating of the vias becomes more of a challenge. This problem is alleviated to a degree by use of thinner, laser-friendly [8–12] dielectric materials. Although the use of blind vias frees up wiring space, its utility is limited by the challenge of plating blind vias with aspect ratios (depth to diameter) greater than 1:1. As the distance between the planes to be interconnected increases, it is necessary to either increase the size of the blind vias or sequentially add several layers of dielectric material, each interconnected from layer to layer with blind vias. However, such a fabrication technique can be costly owing to the cumulative yield loss incurred when adding layers sequentially.

One method of extending wiring density beyond the limits imposed by these approaches, while fabricating structures with vertically terminated vias of arbitrary depth, is a strategy that allows for metal-to-metal Z-axis interconnection of subcomposites during lamination to form a composite structure [13–19]. Interconnection is made using an electrically conducting adhesive (ECA). The adhesive is generally in the form of a conductive paste.

During the past few years, there has been increasing interest in using electrically conductive adhesives as interconnecting materials in the electronics industry [20–25]. Conductive adhesives are composites of polymer resin and conductive fillers. Metal-to-metal bonding between conductive fillers provides electrical conductivity [22–29], while the polymer resin provides favorable processing attributes and mechanical robustness [22–25, 30]. Several investigators have reported on the electrical resistivity of metal-filled polymer composites [31–38]. In an effort to increase electrical conductivity, conductive adhesives usually have a high degree of filler loading. However, this tends to weaken the overall mechanical strength of the adhesive. For layer-to-layer electrical interconnection, reliability of the conductive joint formed between the conductive adhesive and the metal surface to which it is mated is of prime importance.

The area of nanotechnology, encompassing the synthesis of nanoscale materials, understanding and utilization of their exotic physicochemical and electronic properties, and organization of nanoscale structures into predefined superstructures, promises to play an increasingly important role in many key technologies of the new millennium [39–51]. As far as high-density electronic packaging is concerned, there is an ever-growing need to achieve high-density printed wiring boards and laminate chip carriers through Z-axis electrical interconnection using paste-filled microvias [13–19]. Current trends indicate that via diameters for printed wiring boards are approaching 100 μ , whereas those in laminate chip carriers are on the order of 50 μ , or less. Conductive adhesives can have broad particle size distributions, and larger particles can be a problem when filling smaller holes (e.g., diameter of 60 μ m or less), resulting in voids. Consequently, researchers in the field of materials processing have been looking at nanoparticle approaches for the development of conductive adhesives that can fill smaller diameter holes.

Nanoparticles (1–100 nm) have been investigated for more than a decade using a rather wide range of experimental methods [52, 53]. Various investigations of their chemical, mechanical, electrical, magnetic, and optical behavior have already demonstrated the possibility of controlling the properties of nanoparticles through control of the sizes of their constituent clusters or powders and the manner in which the constituents are assembled. The microstructural features of importance include particle/grain size, distribution, and morphology. Nanoparticles exhibit a variety of considerably improved properties with respect to coarse-grained particles. These include increased hardness/strength, enhanced diffusivity, improved ductility and toughness, lower electrical resistivity, higher thermal expansion coefficient, lower thermal conductivity, and soft magnetic properties. Recently, conducting nanoparticles, nanotubes, and nanowires are getting significant attention in the microelectronics industry for miniaturization. Nanomaterials are flexible to use as
conductive adhesives and inks and can be screen or injection printed to produce fine conducting features. Low-temperature sintering to achieve high conductivity is one of the major advantages of nanosystems. However, only limited literature is available on the electrical properties of nanoparticles within the microvia.

In recognition of the importance and issues of nanoparticle-based conductive adhesives, there has been a worldwide research and development effort directed toward high-performance adhesives in recent years. The scope of this chapter is to summarize some recent activities and advances in the area of electrically conductive adhesives formulated using controlled-sized particles, ranging from nanometer scale to micrometer scale, and used to fill small diameter holes (microvias) for Z-axis electrical interconnection applications. A purpose of this review is to provide a better understanding of the nature of nanoparticle-based conductive adhesives, as well as to highlight the significant progress made on microvia filling for Z-axis electrical interconnections. In particular, a strategy that allows for metal-to-metal Z-axis (vertical) interconnection using ECA-filled microvias is described. This chapter discusses nanoparticles and nanoparticle-based conducting adhesives in microvias for these Z-axis interconnections. Recent work on adhesives formulated using controlled-sized particles to fill small diameter microvias is highlighted, particularly with respect to their integration into organic laminate chip carrier substrates. The mechanical strength and reliability of the electrically conductive joints formed between the adhesive and metal surfaces are addressed. A variety of conductive adhesives with particle sizes ranging from nanometer scale to submicron and micron scale were investigated. The review also describes the microstructures, conducting mechanism, volume resistivity, mechanical strength, and reliability of adhesives formulated with a variety of metals and alloys such as Cu and Ag and low melting point (LMP) alloy, used as conductive filler particles in the ECA. As a case study, an example of a silver-filled conductive adhesive used to fill microvias for Z-axis interconnection in a flip-chip plastic ball grid array package having a 150 µm die pad pitch is given. The processes and materials used to achieve smaller feature dimensions, satisfy stringent registration requirements, and achieve robust electrical interconnections are discussed.

13.2 Electrically Conductive Adhesives/Inks for Microvias

A conductive adhesive is a composite material consisting of a nonconductive polymer binder and conductive filler particles. When the filler content is high enough, the system is transformed into a good electrical conductor. Conductive adhesive-filled microvias can provide the conductive path required to achieve connection from one circuit element to another. Electrical connection is achieved primarily by interparticle conduction. For electrical conduction, particles should make intimate contact (physical and/or tunneling) and form a network (conductive chain), which helps in the transfer of electrons. This conductive path is formed at a threshold volume fraction of conductive filler which can be calculated using the

Fig. 13.2 Photograph of a cross section showing a conductive adhesive in a microvia. In this instance, interconnection is made vertically between copper pads and laterally to a copper inner plane



percolation theory of spherical particles. Conductive ink composed of metal particles can also be used in microvias. Inks are typically made of a dispersion of nanoparticles in solution. Metal-to-metal sintering between conductive filler particles provides electrical conductivity.

The electrically conductive material used for via filling must be corrosionresistant, be easily adaptable to the existing manufacturing process (e.g., screen printing), demonstrate low shrinkage after processing, possess high mechanical strength, exhibit good adhesion to PCB materials, and be available at a low cost. Figure 13.2 shows a typical example of a conductive adhesive used in the microvia. Here conducting particles provide low resistance, and the polymer component of the adhesive produces reliable bonding within the joints. Conductive adhesives used for via filling generally need to be isotropic conductive adhesives (ICAs), that is, exhibit good conductivity in all directions. Figure 13.2 shows land-to-land (z-direction) and inner plane connections (x,y direction). Either thermosetting or thermoplastic materials may be used as the polymer matrix in the adhesive. Epoxy, cyanate ester, silicone, and polyurethane are all widely used thermosets. Phenolic epoxy, maleimide, acrylic, and preimidized polyimide are commonly used thermoplastics. Thermoset epoxies are by far the most common binders. They provide excellent adhesive strength, good chemical and corrosion resistance, and low cost. Thermoplastics are usually added to allow softening and rework under moderate heat. An attractive advantage of thermoplastic ICAs is that they are reworkable, that is, they can easily be repaired. A major drawback of thermoplastic ICAs, however, is the degradation of adhesion at high temperature between the ICA and the substrate to which it is bonded. A drawback of polyimide-based ICAs is that they generally contain solvents. During heating, voids are formed when the solvent evaporates. Most commercial ICAs are based on thermosetting resins.

Conductive fillers provide the composite with electrical conductivity through contact between the conductive particles. Conductive filler materials include silver (Ag), gold (Au), nickel (Ni), copper (Cu), and carbon (C) particles in various sizes and shapes. Among the different metal particles, Ag flakes are the most commonly

Table	13.1	Resistivities	of
various	s mate	erials	

Materials	Resistivity (ohm•cm)
Cured unfilled epoxy	10 ¹⁵
Diamond	10 ¹⁴
Glass	10 ¹⁰
Undoped ICP	10 ¹⁰
Silicon	10 ⁵
Doped polyaniline	10^{-1}
Best ICP	10^{-4}
Nanotubes	10^{-4}
Silver-filled epoxy	10^{-4}
Solder	10^{-5}
Silver	10^{-6}

used conductive fillers for current commercial ICAs because of their high conductivity, simple paste formulation process, and excellent contact among the flakes. In addition, Ag is unique among all the cost-effective metals by nature of its conductive oxide. Oxides of most common metals are good electrical insulators. Copper powder, for example, becomes a poor conductor after aging. Nickel- and copper-based conductive adhesives generally do not have good resistance stability, because both nickel and copper are easily oxidized. Even with antioxidants, copper-based conductive adhesives show an increase in bulk resistivity after aging, especially under high-temperature and high-humidity conditions. Table 13.1 summarizes bulk resistivities of some pertinent materials.

13.3 Nanoparticle-Based Conductive Adhesives in Microvias

13.3.1 Material Categories

The term "nanoparticle" generally refers to the class of ultrafine metal particles with a physical structure or crystalline form that measures less than 100 nanometers (nm) in size. Nanoparticles can be 3D (block), 2D (plate), or 1D (tube or wire) structures [54, 55]. In general, nanoparticle-filled conductive adhesives are defined as containing at least some percentage of nanostructures (1D, 2D, and/or 3D) that enhance the overall electrical conductivity or sintering behavior of the adhesives. Figure 13.3 represents a theoretical comparative model for a variety of possible structures based on powder filling in a microvia. In this model, the volume of the microvia is constant for all six cases. Conductivity is achieved through metal-metal bonding. Increasing the number density of particles increases the probability of metal-metal contact. Each contact spot possesses a contact resistance. For microparticles, the number density of particles will be much less than for nanoparticles. Therefore, microparticle-filled vias will tend to have a lower contact resistance





(fewer contacts required over a given length), although the probability of particleparticle contact will be less. In the case of a nano-micro mixture, the microscale particles could maintain a low contact resistance, whereas the nanoscale particles can increase the number of particle contacts. Nano- and microparticle mixtures could be nanoparticle-microparticle, nanoplate (2D)-microparticle, nanotube (1D)microparticle, or any combination of these three cases.

Another possibility is use of a low melting point (LMP) filler. The LMP filler melts and reduces interparticle resistance. Hence, nanoparticle-based conductive adhesives can be categorized as nano-, controlled micro-, nano-micro-, or LMP-based systems. Finally, use of a conducting polymer [56, 57] instead of the high-resistance polymer binder has been reported to enhance the overall conductivity of adhesives.

13.3.1.1 Nano-based Adhesives (NBAs)

Metal nanoparticles with particle size less than 100 nm are useful for developing a variety of ink or paste formulations that can be used to generate small conducting features. Larger particles can be a problem when filling small microvias, resulting in voids. Such problems can be solved by employing nanometer-sized metal particles. However, aggregation of the particles driven by van der Waal forces and/or high surface energies must be overcome. Homogeneous dispersion of fine nanoparticles in the organic matrix is a critical step in order to achieve highly conducting adhesives that sinter at low temperatures. Organic modification of the surface of the particles can alter the surface energy of the particles such that aggregate-free dispersions can be obtained [58]. A silane modifier can influence dispersibility but may also alter the curing behavior (e.g., cross-link density) of the polymeric matrix [59, 60]. Organic protective agents [61] such as polyvinylpyrrolidone (PVP) protect nanoparticles

Fig. 13.4 SEM micrograph of a nanoparticle-based conductive adhesive



from agglomerations and disperse easily in an organic matrix. In the case of inks, nanoparticle inks can be used to fill microvias using an ink-jet process [61–67].

Nanoparticles can self-sinter and form a continuous conduction path. The high surface area possessed by nanoparticles necessitates an excess amount of solvent in order to make a highly loaded silver paste or ink. Figure 13.4 shows the microstructure of a nano-silver-filled adhesive. Nano-filled adhesives achieve electrical conductivity through sintering during the polymer curing and solvent evaporation process. However, solvent evaporation may cause paste shrinkage. Adhesives with high cure shrinkage generally exhibit voiding leading to resistive opens. Therefore, it is important to use as little solvent as possible in pastes used for via filling. Nanoparticles, nanotubes, and nanowires can be used as fillers for pastes used in via fill applications. For example, a novel ICA has been developed by using Ag nanowires as conductive fillers. The electrical and mechanical properties of this adhesive were compared with that of conventional ICAs filled with micrometersized Ag particles or nanometer-sized Ag particles [68]. It was found that at a lower filler content, the ICA filled with Ag nanowires exhibited lower bulk resistivity and higher shear strength than the ICA filled with micrometer-sized Ag particles or nanometer-sized Ag particles. Carbon nanotube-based adhesives are another possible option for use in microvias [69, 70].

13.3.1.2 Controlled Size Sub-micro- and Microparticles

As particle size increases from nano to micro, the sum of the surface areas of the particles within a given volume decreases. Microparticles need higher loading to achieve percolation. Particle size and distribution of particles are important for via



Fig. 13.5 Micrographs for the cross-sectional views of adhesives made with (a) silver microparticles and (b) Cu microparticles

fill applications. Larger particles could plug a microvia during the filling operation and generate voids and open circuits. Recently, controlled size particles in the range of a few microns have been getting interest for via fill applications [13]. Figure 13.5 shows Cu- and Ag-based microparticle-filled conductive adhesives. In the silver adhesive, the average filler diameter is in the range of 5 μ m. Filler loading was high, adjacent particles united mutually, and necking phenomena between fillers occurred; namely, a conduction path was achieved [26], as shown in Fig. 13.5a. A similar result was observed for an adhesive filled with 4 µm Cu particles (Fig. 13.5b). A mixture of different shapes and sizes of microparticles can be used for highly conductive adhesives. Silver particles consisting of a mixture of micro $(2.0-3.5 \mu)$ granular particles, sub-micro $(0.6-1.5 \mu)$ granular particles, and flake $(0.5-5.0 \mu)$ particles have been used to achieve very low resistivity [71]. Silver flakes sometimes show thickness in the submicron to nanometer range. Low-cost sub-micrometer nickel particles can also be used for conductive adhesives [72]. Metal nano-coated microparticle-based adhesives are also used in microvia applications. One of the common examples is the use of gold- or silver-coated copper particles [73]. Typically, the gold or silver nano-coating protects copper surfaces from oxidation.

13.3.1.3 Nano-micro Mixture

Nano-sized conductive particles have been proposed as conductive fillers in ICAs for fine-pitch interconnects. Although the nano-silver fillers in ICAs can reduce the percolation threshold, there has been concern that incorporation of nano-sized fillers may introduce more contact spots due to their high surface area and consequently

Fig. 13.6 SEM micrograph showing a cross-sectional view of an adhesive with a mixture of silver nanoparticles and microparticles



induce higher resistivity compared to micron-sized fillers. In nano-micro mixtures, nanoparticles occupy interstitial positions to improve particle-particle contact for conductivity [13]. Figure 13.6 represents microstructures of nano-micro silver-filled adhesives. It can be seen that individual nanoparticles connect the larger microparticles.

Addition of 2% (wt/wt) nanoparticles into microparticles dispersed in epoxy was reported to improve electrical conductivity [74]. Another study [75] showed addition of nanoparticle content to conventional conductive adhesives increased electrical resistance. Addition of nano-sized silver colloids to micro-sized Ag flakes usually increased resistivity, probably due to increased contact resistance. Only near the percolation threshold would the addition of nano-sized silver particles decrease resistivity by helping to form a conductive path. It was also reported [76] that addition of nano-sized particles to microparticles reduced the percolation threshold from 60 to 50 wt% but increased overall resistivity. Nano-sized silver particles can fill the gaps between silver flakes of conductive adhesives and help electron transport at lower metal loading. However, due to the small particle size and high surface area (and consequently, high contact resistance) of nanoparticles, the measured resistivity of the adhesives was higher than that of the Ag flake-filled adhesives. So, it is clear that resistivity of nano-micro system will depend on their particle sizes (nano/micro) and concentration.

13.3.1.4 Low Melting Point (LMP) Fillers

Another interesting approach for improving electrical conductivity is to incorporate low melting point (LMP) filler into the epoxy matrix [77–79]. Solder is the best known example of a LMP material. A LMP/polymer composite paste material can be developed by mixing solder powder particles, thermoplastic polymer resin in a volatile solvent, and a fluxing agent [77]. Upon reflow, an oxide-free, partially coalesced LMP/solder connection is obtained, which is polymer strengthened and





reworkable at a low reflow temperature or in the presence of an organic solvent. It is also possible to use a hybrid of solder and metal powder with high melting point to exploit the advantages of both [78]. This conductive adhesive is a mixture of a LMP powder, a metal powder of high melting point (such as copper), a fluxing agent, a polymer resin, and other additives. The low-melting-alloy filler melts when its melting point is achieved during the cure of the polymer matrix. The liquid phase dissolves the high melting point particles. The liquid exists only for a short period of time and then forms an alloy and solidifies. Electrical conduction is established through a plurality of metallurgical connections formed in situ from these two powders in a polymer binder. Figure 13.7 shows a cross section of a LMP-based adhesive. LMP melts and produces a continuous metallic network. Here, the electrical connection is established through transient liquid phase sintering (TLPS) among metal and LMP powders. High electrical conductivity can be achieved using this method [79]. One critical limitation of this technology is that the number of combinations of low-melting and high-melting fillers is limited. Only certain combinations of two metallic fillers which are mutually soluble exist to form this type of metallurgical interconnections.

13.3.2 Nanoparticle Sintering

In general, nanoparticles in conductive adhesives can reduce the percolation threshold and introduce more contact spots due to the high surface area and consequently induce higher resistivity compared to micron-sized fillers. A recent study showed that nano-silver particles could exhibit sintering behavior at the curing temperature Fig. 13.8 SEM micrograph of an ECA fabricated using a mixture of silver nanoparticles and microparticles and laminated at 275 °C. Sintering is observed



of adhesives [80]. It is well established that sintering temperature increases with increasing particle size. Addition of nanoparticles into micro-filled adhesives will reduce sintering temperature significantly. The number of contact spots of nanoparticles is greater than with microparticles, for the same volume, as shown in Fig. 13.3a, b. The overall resistance of the adhesive-based interconnection is the sum of the resistances of the individual fillers, the resistance between fillers (interparticle resistance), and the resistance between the filler and pads. In order to decrease the overall resistance, it is desirable to reduce the contact resistance between filler particles and rely more on bulk metal conductance. If nanoparticles are sintered together, then the number of contacts between filler particles is reduced. This leads to lower contact resistance (Fig. 13.8). By using effective surfactants for the dispersion, and effectively capping those nano-sized silver fillers in ECAs, obvious sintering behavior of the nano-fillers can be achieved. As a result, an improved electrical conductivity of nano-silver-filled ICAs can be achieved at a lower loading level than that of micro-filler-ICAs with a filler loading of 80 wt.% or higher. Sintering of silver adhesive was further evaluated using high-temperature curing. Here a mixture of nano and micro silver particles was used. Figure 13.8 shows an SEM micrograph of an ECA fabricated using a mixture of silver nanoparticles and microparticles and cured at 275 °C. Sintering is observed, and conductivity is achieved through a continuous metallic network. Comparable sintering was not observed at this temperature for ECAs fabricated without the addition of nanoparticles. It appears that at a sufficiently high concentration, nanoparticles are more prone to immediate particle-particle contact, facilitating sintering.

13.3.3 Conductivity Requirements in Microvias

Obviously, low resistance is a desirable attribute of joints formed by conductive adhesive-filled microvias. Typical volume resistivity of the conductive adhesives is



Fig. 13.9 Volume resistivity of silver adhesive as a function of curing temperature

in the range of 10^{-3} ohm-cm to 10^{-6} ohm-cm. Volume resistivity of Cu, LMP, and silver-filled pastes has been reported [13] to be 5×10^{-4} ohm-cm, 5×10^{-5} ohm-cm, and 2×10^{-5} ohm-cm, respectively, for conductive adhesives cured at ~190 °C for 2 h. All composites fabricated from LMP and Cu-epoxy nanocomposites showed a resistivity of about 10^{-4} – 10^{-5} ohm-cm, whereas silver composites showed resistivity of about 10^{-4} – 10^{-6} ohm-cm. Silver nanoparticles showed volume resistivity in the range of 10^{-4} ohm-cm, and the resistivity decreased to 10^{-5} ohm-cm when nanomicro mixtures were used. Resistivity was lowest for silver-filled paste. Volume resistivity decreases with increasing curing temperature due to sintering of metal particles. Figure 13.9 shows volume resistivity of silver-epoxy adhesive as a function of curing temperature. There is a significant resistivity drop with increasing curing temperature from 150 to 175 °C.

Exposure of ECAs to ambient conditions before curing can affect paste properties of the final product. Figure 13.10 presents volume resistivity values for the same adhesive, cured at various temperatures, as a function of aging times [13] at room temperature prior to their thermal curing. After 72 h, curing of the ECA at 50 °C, 190 °C and 265 °C resulted in values of 50×10^{-5} ohm-cm, 32×10^{-5} ohm-cm, and 2×10^{-5} ohm-cm, respectively. Change in resistivity with aging was significant when cured below 200 °C, but it was not significant when cured at or above 250 °C. A sharp increase in resistivity is observed up to 24 h of aging, and thereafter it increases slowly.

Figure 13.11 shows viscosity as a function of exposure time at room temperature for a silver-filled epoxy ECA. Viscosity measurement was done using a 50 Pa stress under N_2 . Adhesive viscosity increased by about 30% after 40 h and doubled after 70 h. Differential scanning calorimetry (DSC) measurements indicated that this



Fig. 13.10 Volume resistivity of silver adhesive with aging as a function of curing temperature



change was the result of polymer cross-linking such that the adhesive was partially cured at room temperature. When subsequently cured at 200 °C, the resistivity of this adhesive is greater than that of cured adhesive that was not stored at room temperature for any significant time. For curing above 250C, particle sintering plays an important role in maintaining low volume resistivity or high conductivity.

In general, ICA pastes exhibit high resistivity before cure, but the conductivity increases dramatically after curing. ICAs achieve electrical conductivity during the polymer curing process as a result of shrinkage of the polymer binder. Accordingly, ICAs with high cure shrinkage generally exhibit better conductivity. With increasing cross-linking density of ECAs, the shrinkage of the polymer matrix increases, and subsequently decreased resistivity is observed. For epoxy-based ICAs, a small amount of a multifunctional epoxy resin can be added into an ICA formulation to increase cross-linking density and shrinkage and thus increase electrical conductivity. Jeong et al. [81] reported the effect of curing behaviors, solvent evaporation, and shrink on conductivity of adhesives. As curing time increases, the silver particles in the polymer are concentrated due to the incremental solvent evaporation rate and the shrink rate. As a result, the silver particles in the polymer form an electric path. These results reveal that the increased shrink rate and solvent evaporation rate in conductive adhesives during the curing process improve their conductivity.

With the addition of only a small amount of short-chain dicarboxylic acid, the conductivity of ICA can be improved significantly due to the easier electronic tunneling/transportation between Ag flakes and subsequently the intimate flake-flake contact [82]. The conductivity of silver oxides formed at the surface of silver flakes is inferior to that of the metal (silver) itself. Incorporation of reducing agents such as aldehydes further improves the electrical conductivity of ICAs due to a reduction reaction between aldehydes and silver oxides that generates pure metal silver in ECAs during the curing process [83].

Electrical resistivity of the specimens also varied significantly depending on the subsequent annealing process. However, the electrical resistivity achieved after annealing at temperatures above the curing temperatures clearly depended on the particular curing temperature that was used. The characteristics of the polymer structure in the adhesive binder vary with curing temperature, and this affects the electrical properties of the ICA. That is, the characteristics of the polymer structure obtained during the curing process affect the electrical resistance of the ICA, even after subsequent annealing processes.

13.3.4 Adhesion of Conductive Joints

Adhesion between the adhesive and the substrate to which it is mated is critical to the reliability of the semiconductor package. There are two types of adhesion mechanisms, physical bonding and chemical bonding, which contribute to the overall adhesion strength of a polymer on a surface [84]. Chemical bonding involves the formation of covalent or ionic bonds to link the polymer and the substrate [84]. Physical bonding involves mechanical interlocking or physical adsorption between the polymer and the surface of substrate. In mechanical interlocking, polymer and substrate interact on a more macroscopic level, where the polymer flows into the crevices and the pores of the substrate surface to establish adhesion [84]. Therefore, a polymer is expected to have better adhesion on a rougher surface because there is

Adhesive	90° peel strength (lb/inch)	Tensile strength (PSI)	Failure mode
Low melting point (LMP) alloy	1	600	Cohesive
Copper (Cu)	1.77	2056	Cohesive
Silver (Ag)	2.75	3370	Cohesive

Table 13.2 Tensile strength and failure modes for a variety of ECA formulations

more surface area and "anchors" to allow for interlocking between the polymer and the substrate.

Bond strength of adhesive joints was evaluated using 90° peel test and tensile strength measurements. Peel strengths as high as 2.75 lb/in. were measured for silver-filled pastes on roughened Cu foils, while LMP-filled pastes yielded peel strengths as low as 1.00 lb/in. Temperature cycle tests were run using a thermal shock chamber, cycling between -55 and 125 °C, with exposure times of 10 min at each temperature. Tensile strength was measured before the test, and after 1000 cycles, using an MTS tensile testing machine at a pulling rate of 0.025 in. per minute, and measuring until the joint ruptured. All pastes were stable after 1000 cycles. For all tensile strength test samples, cohesive failure within the paste was the observed failure mode. Table 13.2 summarizes 90° peel strength and tensile strength for various conductive adhesives. Silver-filled paste yielded the maximum mechanical strength.

Plasma cleaning of surfaces has been considered as one of the effective approaches to enhance the adhesion strength of conductive adhesives [85]. During the plasma etching process, the plasma radicals react with contaminants, and long chain organic molecules can be broken down into small gaseous ones (mostly gaseous water and carbon-oxide conjunctions). These particles can be removed during the plasma cleaning process.

Another approach to improve adhesion is by using coupling agents [86]. Coupling agents are organo-functional compounds based on silicon, titanium, or zirconium. A coupling agent consists of two parts and acts as an intermediary to "couple" the inorganic substrate and polymer. For example, silane has different type organic chains that interact with the polymer and the substrate. Gianelis et al. reported various silane coupling agents [87]. Roughening of surfaces, for example, by sand blasting, chemical etching, plasma treatment, or anodization to specific morphologies, has been employed to enhance the adhesion strength and provide structural durability in humid or corrosion environments [88, 89].

A further approach is to lower the elastic modulus of adhesive resins. By using low elastic modulus resins, the thermal stress at the adhesion interface can be reduced, improving the adhesion strength [90, 91]. However, a modulus value that is too low deteriorates the cohesive force and, thus, decreases the adhesion strength. Therefore, the elastic modulus needs to be optimized to improve the adhesion properties.

In addition to the methods listed above, other factors such as curing conditions and IC packaging structure may also affect the adhesion strength of conductive adhesives.

Tests	Silver adhesive	Cu adhesive	LMP adhesive
IR-reflow	Passed	Passed	Passed
$(3 \times \text{ reflows at } 225 \text{ °C})$			
PCT (4 h)	Passed	Passed	Passed
(121 °C/100%RH)			
Solder shock	Passed	Passed	Passed
(15 s dip at 260 °C)			
IR-reflow + PCT + solder shock	Passed	Passed	Passed
$(3 \times \text{ reflows } +121 \text{ °C/100\%RH} + 15 \text{ s solder dip at } 260 \text{ °C})$			
IR-reflow + solder ($3 \times$ reflows + 15 s solder dip at 260 °C)	Passed	Passed	Passed
	1	1	1

Table 13.3 Reliability test results

13.3.5 Reliability of Conductive Joints

Conductive adhesives are of little value in electronic packaging unless they can survive the rigors of testing which modules or boards receive. To test the reliability of joints formed using conductive adhesives, a film of adhesive about 100 μ m thick was laminated between two copper substrates. The adhesive film was surrounded by a 100 μ m thick layer of glass cloth-reinforced dielectric (pre-preg). The surrounding 100 μ m thick dielectric helped to maintain proper adhesive thickness during lamination. Reliability of the laminate was ascertained by pressure cooker test (PCT), solder shock, and IR-reflow. For PCT, samples were exposed to 100% humidity with a constant pressure of 19 PSI at 121 °C. Table 13.3 summarizes test results. Samples were stable after reliability test, and there was no delamination after PCT, solder shock, and IR-reflow. Laminates were also exposed to PCT (4 h) followed by a 15 s of solder dip at 260 °C.

13.4 Microvia Hole-Fill Study

Reliable metal-epoxy adhesives were used for microvia fill applications to fabricate Z-axis interconnections in laminates. Figure 13.12 shows LMP, Cu, and Ag adhesive-filled microvias as representative examples. Holes having a diameter of roughly 55 μ m, with an aspect ratio of about 3 to 1, were filled with different pastes. All pastes had continuous connection from top to bottom. LMP melted and grew as a big grain and separate organics (black regions). Cu and Ag both maintained their particle-particle connection mechanism and also maintained paste uniformity in the holes. Thus, it is possible to make a wide variety of conductive adhesives that can be used for Z-axis electrical interconnection in electronic packages.

Reliability of conductive joints in the test vehicle was further examined by 1000 cycles of deep thermal cycling (DTC), IR-reflow ($3 \times$, 225 °C), PCT, and

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Fig. 13.12 Adhesive-filled joining cores: (a) LMP, (b) Cu, and (c) silver



solder shock. No intrinsic failure mechanisms were observed. There was no delamination. Conductive joints are stable even after multiple IR-reflow $(3\times)$ followed by multiple $(3\times, 15 \text{ s})$ solder dips.

13.5 Case Study: Test Vehicle with Filled Microvias for Z-Axis Interconnection

13.5.1 Core Fabrication

Integral to the methodology described in this chapter is the use of core building blocks that can be laminated in a manner such that electrical interconnection between adjacent cores is achieved. The cores can be structured to contain a variety of arrangements of signal, voltage, and ground planes. In addition, signal, voltage,



with parallel lamination to produce a 4S laminate chip carrier.....



and ground features can reside on the same plane. As a case study, this z-interconnection methodology was used to fabricate a package for a flip-chip device having a pad pitch of 150 μ m. Two basic building blocks are used for this case study (Fig. 13.13). One is a 2S/1P core. The power plane (P), a 35 μ m thick copper foil, is sandwiched between two layers of a PTFE-based dielectric. The PTFE is filled (60% by weight) with silica particles to achieve a reduced CTE for the dielectric material, more closely matched to that of copper. PTFE is used because of its favorable electrical, mechanical, and thermal properties. The dielectric constant and loss tangent of the silica-filled PTFE at 10 GHz are 2.7 and 0.003, respectively.

The signal (S) layers are comprised of copper features generated using a semiadditive (pattern plating) process. A line thickness of 12 μ m was achieved with minimum dimensions for line width and space of 25 μ m each. Minimum land-to-line spacing was also 25 μ m. Laser-drilled through vias had a diameter of 40 μ m, while blind vias were laser-drilled with a 50 μ m diameter. The latter diameter was selected to avoid the need to plate blind vias having an aspect ratio greater than 1:1. The diameter of plated pads around the through and blind vias was 75 μ m. These dimensions enabled wiring designs having one line per channel in the most densely populated areas of the chip site.

The second building block in this case study is a 0S/1P core, or "joining core." This core is constructed using a copper power plane, 35 µm thick, sandwiched between layers of a dielectric material composed of a silica-filled allylated polyphenylene ether (APPE) polymer. Dielectric constant of this material is 3.23 at 1 GHz, and the dielectric loss tangent is 0.003 at 1 MHz. Through holes in the core are filled with an electrically conductive adhesive (as seen in Fig. 13.12). Figure 13.14 shows a process flow chart for fabrication of the 0S/1P cores.



Fig. 13.14 Schematic process flow for fabrication of a 0S/1P joining core



13.5.2 Composite Lamination

By alternating 2S/1P and 0S/1P cores in the lay-up prior to lamination, the conductive paste electrically connects copper pads on the 2S/1P cores that reside on either side of the 0S/1P core. Two signal layers are added to the composite structure each time one adds an additional 2S/1P core and an additional 0S/1P core. A structure with four signal layers composed of five subcomposites (two 2S/1P cores and three 0S/1P cores) is shown schematically in Fig. 13.13. Although this particular construction comprises alternating 2S/1P and 0S/1P cores, it is possible to place multiple 0S/1P cores adjacent to each other in the stack.

The adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. High-temperature/high-pressure lamination was used to cure the adhesive in the composite and provide z-interconnection among the circuitized subcomposites. Figure 13.15 shows optical photographs and SEM micrographs, taken prior to composite lamination, of a joining core having paste-filled holes with a diameter of 55 µm. It can be seen that the conductive adhesive height is higher than that of the surrounding dielectric (see Fig. 13.15d). This excess height helps to produce robust conductive joint between two 2S/1P cores during lamination process. Photographs of a composite laminate structure are shown in cross section in Fig. 13.16.

Special processing of the metal surfaces on 2S/1P cores and the conductive paste in the 0S/1P cores is required to provide robust and reliable joints with the conductive paste. Figure 13.17a shows photos of a cross section taken from a laminate for which metal surfaces were not treated to provide robust mating with the paste. Following exposure of the laminate to four cycles of conditions that simulated solder reflow temperatures, the paste separates from the opposing metal surface.



Fig. 13.15 Photographs of adhesive-filled joining cores. (a) Large area optical photograph, (b) higher magnification optical photograph, (c) corresponding low magnification SEM micrograph, and (d) higher magnification SEM micrograph



Fig. 13.16 Photograph of z-interconnect laminates shown in cross section

Figure 13.17b illustrates the result after similar temperature cycling for metal surfaces that have been treated. These joints are very robust.

Figure 13.18 (top) shows an SEM micrograph of a portion of a via stack, in cross section, from which the dielectric surrounding the plated via in the 2S/1P core and the paste column in the 0S/1P core had been removed using a CO_2 laser. The bottom micrograph in Fig. 13.18 shows the metal pad, 75 µm diameter, after having been



Fig. 13.17 Photographs of cross sections taken from temperature-cycled metal-paste joints for which the metal mating surfaces were untreated (a) and treated (b)

Fig. 13.18 SEM

micrograph showing cross section of paste-to-land joint in via stack (top). The dielectric surrounding the stack had been removed from the cross section using a CO_2 laser. An SEM micrograph of the joint circled in the top photo after removal of the via stack from the sample, and fracture of the paste column, is shown in the bottom photo. Silver paste remained on the land after fracture



removed from the laminated composite. The conductive paste column in contact with this land was fractured after removal. The fracture occurred within the paste, indicating that the joint between the metal and the paste had extremely good mechanical integrity.

The z-interconnect package technology in this study uses a high-performance material set to yield excellent reliability and electrical performance [47, 92, 93]. It also offers excellent escape density and wireability. In addition to making wiring



Fig. 13.19 Ability to terminate vias at any internal layer (bottom) provides additional channels for wiring and reduces or eliminates stubs associated with PTHs (top)

channels available, this z-interconnection technology reduces losses for high speed signals. PTHs have been replaced with blind and buried vias, reducing or eliminating stubs (Fig. 13.19).

13.5.3 Reliability of Paste-Filled Microvias in the Final Package

For the laminate in the example above, the average CTE of the composite is 18.3 ppm/°C. This is comparable to that of copper, 17 ppm/°C, whereas the CTE of the silica-filled PTFE is 25 ppm/°C, and that of silica-filled APPE is 41 ppm/°C. It is apparent that the CTE of the laminate structure is dominated by that of the copper planes in the composite cross section.

The test vehicle was a chip carrier having a flip-chip die pad pitch of $150 \,\mu\text{m}$. The die size was 9.3 mm square owing to the limitation of the BGA I/O (pitch and substrate body size) and the die pad pitch. The body size (package outer dimensions) was 52.5 mm square with a 1 mm BGA pad pitch.

Assembled components (chip on composite) were subjected to JEDEC Level 4 preconditioning per the following conditions:

Test	Conditions	Duration
Accelerated thermal cycling (component on card with heat sink)	0–100 °C BLR	3600 cycles
Deep thermal cycling (DTC)	-40 to 125 °C	1000 cycles
High-temperature storage	150 °C	1000 h
Pressure cooker test (PCT)	121C/100%RH/2 atm	96 h
Wet thermal shock	-55 to 125 °C	1000 cycles

Table 13.4 Stress testing conditions

5 cycles from −40 to +60 °C 24 h at 125 °C 96 h at 30° and 60% RH 3× reflows, 225 °C peak

Components were then subjected to environmental stress testing using the tests and conditions outlined in Table 13.4. No intrinsic failure mechanisms were observed. There was no die cracking, underfill delamination, BGA ball fatigue, dielectric cracking, or delamination.

13.6 Conclusion

Nanoparticle-based adhesives have shown remarkable advantages and are attractive for use in microvia fill applications. A variety of nano- and micro-filled Cu and silver and LMP-based conducting adhesives can be used in microvias for Z-axis interconnection. High aspect ratio, small diameter (~55 µm) holes have been successfully filled. Reports show silver-filled adhesives are electrically and mechanically better than Cu- and LMP-filled adhesives. Nanoparticle-based adhesives exhibit sintering at lower temperatures that are required for sintering of microparticle-based adhesives, resulting in higher electrical conductivity. All adhesives maintain high tensile strength even after 1000 cycles of DTC testing. Conductive joints were stable after 3x IR-reflow, 1000 cycles of DTC, PCT, and solder shock. Adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. High-temperature/high-pressure lamination was used to cure the adhesive in the composite and provide stable, reliable nanoparticle-filled microvia-based z-interconnections among the circuitized subcomposites.

A high-performance z-interconnect package can be provided which meets or exceeds JEDEC level requirements if specific materials, design, and manufacturing process requirements are met. Proper lamination process settings, core metallurgy treatment, and selection of proper joining metallurgy result in an excellent package that can be used in single- and multi-chip applications. By designing an organic package without electrical stubs and without through holes, high wiring density and excellent electrical performance can be achieved. Novel means of providing vertical electrical interconnection in organic substrates can help semiconductor packaging keep pace with the needs of the semiconductor marketplace.

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Chapter 14 Silver Nanoparticles for Inkjet-Printed Conductive Structures in Electronic Packaging



Jan Felba

14.1 Printed Conductive Structures in Microelectronics

In modern microelectronics production, additive fabrication processes offer a thematic contrast to traditional micro-fabrication processes that rely critically on subtractive patterning. Printing, a bottom-up process, plays an important role in this production, especially when nanomaterials are printed. There are many areas in which such printing is used [1], but only electrically conductive structures in electronic packaging are the object of interest in this section.

Packaging of today's miniaturized electronics is based on conductive microstructures and contacts with dimensions in the range of tens of micrometers. Such lines or much more complicated patterns are possible on the condition that both special technologies and materials are applied. Printing is one of the key technologies which is used in microelectronics manufacturing. This even created a new name for the electronics produced this way, namely, "printed electronics." There are many printing technologies used for this [2], which can be divided into two basic categories – contact or noncontact. Screen, flexographic and offset-gravure printing are examples of methods in which printed material is applied on a substrate directly by contact with a dispensing system. In noncontact methods, liquid flows freely between a dispenser and a substrate. As an example of such methods, Fig. 14.1 presents a continuously working printing technique: M³D (Maskless Mesoscale Material Deposition). The printed suspension is atomized in a mist generator. The resulting aerosol stream is aerodynamically focused by an annular flow of sheath gas to as small as less than a tenth of the size of the nozzle orifice. This technique allows us to obtain printing conductive structures with dimensions below 10 µm [3], also on non-planar substrates, even for high aspect ratio structures.

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In the electronic industry for printing structures with complex geometry, digital injection technologies have been preferred. Such technologies are favored mainly due to the higher processing precision, limited basically by the size of the dispensed liquid drops. A relatively simple set of devices is used for the electrostatic inkjet method (Fig. 14.2). The system consists of a glass capillary, an extraction electrode, a ground electrode, and a high pulse voltage power supply. A high pulse electric voltage signal is applied to the upper electrode located against the wire inside the nozzle as the ground electrode, which enables the microdripping droplet ejection mode. The droplet can be formed without being constrained to the diameter of the nozzle tip. Consequently, from the glass capillary having a diameter of 100 μ m, it is possible to generate droplets of diameter 30 μ m when the suspension contains nanosized silver [4] or much less in the case of other liquids [5].

Electrode Substrate – 0

Well-defined continuous silver lines, 20 μ m wide and ~500 nm thick, have been transferred using the laser-induced forward transfer (LIFT) technique [6, 7]. In this technique, a printed material, deposited on an optically transparent support, is moved to a substrate by a high-energy focused laser pulse (Fig. 14.3). However, it is difficult to find proper parameters of the technology process to obtain stable continuous electrically conductive lines free from bulging [8].



For printing conductive structures, the piezo drive inkjet technology has been widely applied rather than other digital injection technologies. The technology needs a special liquid, usually termed "ink," which should satisfy at least the following three requirements: has very low viscosity, can be treated as a "true solvent" without component separation during high acceleration, and is able to make electrically conductive structures. There are four major ink types to produce metal tracks with inkjet printing methods [9], namely:

- Nanoparticle inks, which are metallic nanoparticle suspensions with some additives to prevent particle agglomeration and sedimentation.
- Metallo-organic decomposition inks which are high-concentration metal salts dissolved in organic solvents or aqueous solutions; after printed on substrates, the salts decompose into conductive metal under heating conditions.
- Catalyst inks for electroless plating in which a chemical reducing agent transforms metal ions to solid metal; the solid metal film is attached to solid surface by autocatalysis mechanism occurred on metal surface.
- Inks dispensed separately through two drop generation channels; when two droplets meet on the printed pattern, metal recovers from the redox reaction to form highly conductive thin films (Fig. 14.4).

The system with two dispensers creates opportunities for printing various components. For example, silver ammonia and then formaldehyde solutions were separately ejected, mixed, and reacted on glass slides. These inkjet-printed lines were then further heated at 150 °C to decrease the electrical resistivity up to $1.2 \cdot 10^{-5}$ $\Omega \cdot cm$ [10].

Inks containing metal nanoparticles are commonly used materials for printing electrically conductive structures in microelectronics. The "conductivity" condition of such suspensions requires applying electrically conductive particles, and the "true solvent" demands particles with dimensions as small as possible, not higher than



tens of nanometers. Ink for inkjet printing of conductive microstructures is typically based on noble metals of nano-sized dimensions because of the chemical inertness in ambient atmospheres and good electrical conductivity. Silver nanoparticles meet these conditions well and are most often used as the ink fillers. However, it is also possible to create conductive structures using nanoparticles of gold [11] and even palladium. In case of Pd, it is used for the creation of printed sublayers on which nickel is plated. The conductive lines formed have widths of 52 μ m [12].

Using copper as an ink filler seems to be attractive because of its very good conductivity and lower bulk material price than noble metals. However, one of the most crucial challenges of such application is the reactive nature of copper nanoparticles which form an oxide layer which is electrically nonconductive. As in the case of silver preparation during the production process, copper nanoparticles are also coated by an insulating layer [13] which prevents the ink filler from agglomeration. Such a coating can be a barrier to oxidation (when printing) but then has to be removed for good electrical conductivity of the printed layer – usually at high temperature by a sintering process. In order to prevent the oxide layer from forming, the sintering should be carried out either in an inert environment or at high speed so that the oxide layer does not have time to form. As an inert atmosphere, nitrogen or hydrogen can be used. Under these conditions, the sintering process was carried out at temperatures, respectively, 200 °C [14] and 230 °C for 1 h [15]. In the special condition named cool powder sintering (CPS) [16], it is possible to form bulk-like copper at 180 °C. The 3-µm-wide printed lines have resistivity as low as 2.6.10⁻⁶ Ω ·cm, and their texture is void-free. High-speed sintering may be performed when the printed layer is affected by the energy transferred to heat of high power density, e.g., using laser beams [17, 18].

The problem of Cu oxidation disappears if the coating is a conductive material. For example, coating 40 nm copper nanoparticles with a 2 nm layer of silver [19] or with carbon [20] prevents oxidation of the copper core and preserves its metallic characteristic.

Recently, a growing interest in the use of inks for inkjet printing technology containing carbon nanomaterials should be noted. This is because carbon nanotubes (CNTs) and graphene are desirable for the production of conductive structures due to a very high electrical conductivity of these materials. Unfortunately, CNTs are difficult to disperse in a liquid when an ink is being prepared. The main problem is the formation of agglomerates with submicron size, which are difficult to break by normal sonication. Acceptable colloidal suspensions can be prepared using the method which combines dielectrophoresis and megasonification [21]. However, the problem is how to obtain a good electrical contact between the individual nanotubes after printing. To create an electrical pathway, CNTs are chemically treated to obtain carboxyl functionalities on their surface, and it is necessary to print multiple layers [22]. Using multi-walled CNTs, straight conductive lines were successfully printed, with sheet resistances corresponding to the class of dissipative materials [23]. Much better results can be obtained when CNTs are aligned. With self-ordering of the multi-walled CNTs, conductive track widths in the range of 5–15 μ m were achieved with the electrical resistivity of a few 10⁻⁵ Ω ·cm [24].

A similar resistivity value of printed structures was obtained when graphene was used. However, printing has to be repeated many times (up to 200 layers), and the sintering process of the printed structures was conducted in an oven filled with argon gas at 400 °C for 3 h [25]. It is assumed that the number of sheet-to-sheet contacts between graphene layers strongly influences the electrical parameters of a printed path which depends on many factors [26]. The improvement of these contacts can be due to silver nanoparticles which were uniformly distributed on graphene nanosheets after post-annealing process and acted as conductive bridges between graphene flakes [27]. The type of materials used, properties of the ink, technological parameters of printing, thermal process after printing, and the atmosphere in which annealing is performed are variously reported in the literature [28–30], and currently there is no clear recipe of making electrically conductive structures using graphene.

The subject of this section is confined to inkjet printing technology using ink containing silver nanoparticles. Nanoparticles can be in the regular form which can be described in one dimension. This means that the uses of irregular forms of Ag nanoparticles as the fillers of ink for printing to, e.g., silver nanowires [31] are not cited.

The content is partially based on the first edition of this book [32].

14.2 Silver Nanoparticles

Silver nanoparticles can be produced by several methods with two general approaches – physicochemical and chemical. Methods can be briefly described as "metal dissipation in plasma process", "metal vapor deposition", "chemical reaction process", "electrochemical process", "thermal decomposition process", "laser

Production method	Salt	Average particle size, [nm]	References
Thermal decomposition		≤10	[34-40]
		10-100	[41]
Chemical reaction	Silver nitrate AgNO ₃	≤10	[42]
		10-40	[43-48]
		≥40	[49, 50]
			[51–55]
	Silver acetate CH ₃ CO ₂ Ag	≤10	[56]
			[57]
Laser ablation		≤10	[58]
		10-50	[58]
Gas evaporation		≤10	[59, 60]

Table 14.1 Production methods of silver nanoparticles used for inkjet printing

ablation", and others. Additionally, some microorganisms such as bacteria, fungi, and yeast have been exploited for silver nanoparticles synthesis [33]. It would be unjustifiable to describe all these methods, as only methods which yield singular nanoparticles separated from others can be used for production of filler for inkjetprinted formulations. The final product must be protected from agglomeration which means that the particles must be coated with an organic protective layer at a definite moment of the production process. Additionally, the particles should have a narrow size distribution and be contamination-free. Literature in the field of inkjet printing provides information about which method was applied to obtain the silver used in the ink. This information is summarized in Table 14.1.

From Table 14.1 it can be seen that one of the known ways of obtaining Ag powder with particles in the atomic size range is the release of metallic Ag from silver salts of fatty acids during their thermal decomposition in an oxygen-free atmosphere. In order to obtain highly divided powders (to the size of several nm), it is necessary to moderate their coagulation during the production process, e.g., by a protective coating of fatty acid. This recognized fact has been applied in the technology of obtaining Ag salts of fatty acids covered with excess acid which moderates the coagulation of the released silver during further thermal processing. During studies of thermal decomposition of silver salts/fatty acids, it was found that reaction conditions have the main influence on end results of Ag particles with narrow size distribution. As a standard result, very homogeneous and pure products are obtained with constant reaction parameters, and the particle size does not exceed 10 nm (Fig. 14.5). Nanoparticles can be in the form of single crystals, simple twins, multiple twins [38], or other regular form.

Silver salts can also be used for Ag nanoparticle production by chemical reduction using various reducing agents. Generally, synthesis of metal nanocrystals starts from zerovalent metal compounds or salts dissolved in a solvent. In particular for Ag, these precursors are in the oxidation state (Ag⁺), and thus, during the reaction, Ag⁰ atoms are produced as metal nanocrystal building blocks. Two synthetic ways are possible. The first possibility consists in reducing the precursor compound into



Fig. 14.5 Histogram of silver nanoparticles distribution produced by thermal decomposition method [34, 61]

zerovalent atoms, which then aggregate into the nuclei and grow into nanocrystals. In the second, the unreduced metal species associate with nuclei and then are reduced to zerovalent metal species [62].

Silver salts are usually insoluble in any solvent, and thus the most often used precursor for Ag nanocrystal production is silver nitrate (AgNO₃), which shows a good solubility in polar solvents. The preferential seed shapes from silver salt reduction are icosahedral and decahedral, thermodynamically favored from the face-centered cubic lattice of metallic silver [62]. The process can be as follows: when a reducing agent (in this case triethanolamine) is added gradually to the AgNO₃ solution, the reduction of Ag⁺ proceeds slowly, and then the concentration of Ag⁰ approaches the critical concentration for nucleation. When nucleation occurs, some Ag⁰ species convert to nuclei, some Ag⁺ are reduced continuously to Ag⁰, and the nucleation step continues for a relatively long period of time. As the silver nanoparticles grow, the mixture gradually becomes dark and turbid because large particles reflect and scatter more light than small ones [43].

Above is an example of the reaction. However, another salt may be a starting material, and many reducing agents can be used, such as monoethanolamine (MEA) [45], trisodium citrate [49], formaldehyde [46, 54], sodium borohydride [47], hydrazine [50], glucose [44], or the aforementioned triethanolamine (TEA) [43]. This variety of the reaction components causes differences in the dimensions of nanoparticles produced (Table 14.1).

Metal nanoparticles with very low dimensions and narrow size distribution can also be prepared by laser ablation or gas evaporation. In the method of laser ablation from a metal target in a liquid phase, the cleaned Ag target was placed on the bottom of a glass vessel filled with ethanol, deionized water or acetone, which were used as the liquid environment. The surface of the metal plate is irradiated by a pulsed laser beam with different parameters (wavelength, pulse duration and pulse energy, pulse repetition rate). A lens is used to focus the beam on the metal surface (Fig. 14.6). **Fig. 14.6** The principle of silver nanoparticles production by laser ablation method from a metal target in liquid phase



The liquid and its type play very important roles in the technological process. As a result, changing the nature of the liquid environment is an easy and flexible way to control the size distribution and stability of Ag colloidal nanoparticles. Silver nanoparticles thus produced are practically spherical and have typically average diameters over a dozen nm [63]. Experiments with a pulsed Nd:YAG laser showed that Ag nanoparticles in acetone or deionized water have a mean size of 5 nm and 13 nm, respectively [58].

In the gas evaporation method, nanoparticles are synthesized by evaporation/ condensation, which could be carried out using a tube furnace at atmospheric pressure. The source material within a boat centered at the furnace is vaporized into a carrier gas. The absence of solvent contamination and the uniformity of nanoparticles distribution are the advantages of this method in comparison with chemical processes. However, a tube furnace occupies a large space, consumes a great amount of energy while raising the environmental temperature around the source material, and requires a lot of time to achieve thermal stability [64]. To obtain a small amount of the product, the silver nanoparticles could be synthesized using a small ceramic heater with a local heating area. It was found that in such conditions, the particle size depends on the heater temperature: from 6.2 to 21.5 nm with temperature changing from 1000 to 1350 $^{\circ}$ C [65].

The detailed characterization of nanoparticles is a crucial point in their further application as the filler of an ink for printing. Their size, composition, and thickness of the organic protective layer play important roles in an ink's physical parameters. In order to understand these dependencies, many measurement techniques are being applied. And so, estimation of size distribution of silver nanoparticles can be done by high-resolution transmission electron microscopy (HRTEM), atomic force microscopy (AFM), dynamic light scattering (DLS), or ultraviolet and visible spectroscopy (UV-VIS). Energy-dispersive X-ray spectroscopy (EDX) can be used for chemical analysis and X-ray photoelectron spectroscopy (UPS) and local scanning tunneling spectroscopy STS techniques can be used as valuable techniques in electronic structure investigations of silver nanoparticles This is especially important in the case of studies of quantum size effects on nanoparticles [66].

14.3 Material for Inkjet Printing

The technology of fluid dispensing without direct contact between dispenser and substrate is termed "inkjet printing." Because of this, the fluids are usually described as inks, but in fact they are homogeneous suspensions containing metallic nanoparticles with viscosity no higher than tens of mPa·s. Some producers (e.g., [67, 68]) name their products also as nanopastes, even though their viscosities are relatively low. The name nanoparticle paste is legitimate when materials with metallic particles of nano-dimension are used for other printing technologies. An example may be quoted of a fine pitch pattern with both line width and distance between them of 30 μ m, screen printed with the use of paste containing silver particles of average diameter 8.8 nm [35]. If a nanofluid was used for inkjet printing, then only the term "ink" is used in this section, independently of the author's original terminology.

Three groups of ink parameters can be distinguished which determine the suitability of inkjet printing for industrial production. The first group is connected with the ink base material which makes it possible to receive electrically conductive structures. The ink contains at least two components: liquid (diluent) and solid particles. After printing, the liquid usually evaporates, and only the particles determine the conductivity. In the case of silver particles, high electrical conductivity is expected as bulk silver at room temperature has the very low resistivity of $1.59 \cdot 10^{-6}$ $\Omega \cdot cm$ [69].

The second group is connected with properties that allow the ink to be used in systems for printing. In the commonly used printing systems (Sect. 14.4), singular droplet formation with volumes of a few picoliters is only possible at both low ink viscosity and low surface tension. Viscosity is a measure of the resistance of a fluid to deform under shear stress. It is commonly perceived as "thickness" or resistance to flow. Viscosity describes a fluid's internal resistance to flow and may be thought of as a measure of fluid friction. The SI physical unit of dynamic viscosity is the Pascalsecond (usually mPa·s). Viscosity μ tends to fall exponentially as temperature increases:

$$\mu(T) = \mu_0 \exp(-bT),$$
(14.1)

where T is temperature and μ_0 and b are coefficients.

Surface tension is an effect within the surface layer of a liquid that causes that layer to behave as an elastic sheet. Surface tension is caused by the attraction between the molecules of the liquid by various intermolecular forces. In the bulk of the liquid, each molecule is pulled equally in all directions by neighboring liquid

Diluent	Ag particle size [nm]	Metal content [wt%]	Viscosity [mPa·s]	Surface tension $[mN \cdot m^{-1}]$	References
Water	≤10	10-30			[70]
	10-50	≤10	≤10	20-30	[50]
					[49]
		10-30	≤10	>40	[45]
					[71]
			10-20	20-30	[44]
Ethanol	10-50	10-30			[46]
Toluene	≤10		≤ 10	30-40	[72]
			≤ 10	20-30	[73]
Tetradecane	≤10	30–50	≤ 10	30-40	[34, 61]
					[74]
		>50	≤ 10		[60, 67, 75]
			10-20		[76]
					[71, 77–79]
	10-50	>50	≤ 10		[80]
Ethylene glycol	10–50	30–50			[47]
A-terpineol	≤ 10	≤ 10			[81]
Water/ethylene glycol	≤ 10	10-30			[56]
	10-50	10-30	≤ 10	>40	[43, 45]
		30–50	≤ 10	30-40	[82]
Ethanol/ethylene glycol	10-50	10–30	10-20	20-30	[83-85]
					[86]
					[71, 87]
	>50	10–30			[74]
Triethylene glycol/ monoethyl ether	10–50	30–50			[88–90]
Cyclohexane/α-terpineol	≤ 10	≤ 10			[91]
Ethylene glycol/glyc-	10-50	10-30	10-20		[92]
erin/ethanol					[93]

Table 14.2 Parameters of ink used for inkjet printing

molecules, resulting in a net force of zero. Surface tension is measured in Newtons per meter (usually $mN \cdot m^{-1}$).

By practice, it is required that the ink viscosity should not be higher than tens of mPa·s with its surface tension on the order of tens of $mN \cdot m^{-1}$. In fact, irrespective of the ink solvent, viscosity values are below 20 and in most cases lower than 10 mPa·s (Table 14.2). From the table it is also noted that in practice the surface tension does not exceed 40 mN·m⁻¹.

Forming the droplet in the nozzle of the printing head capillary, the pressure wave accelerates the liquid with up to 10^5 g [94]. Ejection with such acceleration should not cause changes in the ink structure. This means that the printing process cannot

affect the ink components selectively and the liquid should behave as a true solvent. This requires metal particle dimensions as small as possible – in practice not larger than several tens of nanometers. Table 14.2 does not inform precisely about the size of the nanoparticles, but it can be estimated that about 42% of the cited cases when the ink was used contained nanoparticles of size no higher than 10 nm and 98% <50 nm.

It is only possible to obtain and keep single metal particles in the solvent by coating them with a protective layer in the production process. Without those layers, particles would tend to aggregate and form bigger structures. Shelf life, i.e., the length of time that the ink may be stored prior to its use, has to be as long as possible in stable thermodynamic conditions. Instability results from the lack of homogeneity and can change the viscosity of the ink, caused mainly by solid particle agglomeration, their sedimentation in a suspension, or evaporation of the solvent. Such features are particularly important in the case of breaks in printing, when the cartridge of a printing head is filled with the ink, and can be treated as a third group of important ink parameters. The instability of ink content may result in a lack of printing repeatability.

In laboratory conditions, assessment of the stability of ink can be carried out by measuring the viscosity and evaluating the solid particles' sedimentation. While the measuring of the viscosity needs a special device, the assessment of the sedimentation (although described in detail in the literature (e.g., [95])) usually depends on the type of suspension and is proposed as another laboratory procedure. This procedure may be as follows [96]:

- The solution is kept at a constant temperature, c.a. 23 °C without any stirring or shaking.
- Every few days, a sample is taken from the surface layer (with the depth less than 10% of the column solution).
- Silver content C_{Ag} in the sample of solution is measured, according to the equation

$$C_{Ag} = \frac{m_{Ag}}{m_{Ag+pl} + m_s} \cdot 100\%$$
(14.2)

where m_s is the weight of the solvent, m_{Ag+pl} mass of silver nanoparticles coating with protective layer, and m_{Ag} mass of silver (measured after evaporation of solvent and protective layer removal at high temperature). Of course, decrease of the silver content of the sample (C_{Ag}) points to the sedimentation of particles in the solution.

As was mentioned, each conductive particle is covered with an organic protective layer. The most important function of this layer is to prevent aggregation of metal particles as well as to keep them stable in a suspension. It means that the type of coating and its relationship with the solvent strongly influence the ink stability. Their structure and function are usually classified as electrostatic or steric stabilization [97].


Electrostatic stabilization is achieved by producing a charge on the nanoparticles surface. The charge of neighboring particles can generate a repulsive electrostatic force which keeps the particles at a certain distance [98]. Steric stabilization consists in attaching polymer chains to the surface of particles. Spatial action of those chains causes the distance between particles, and they are dispersed in liquid [99]. It is also possible to combine steric with electrostatic stabilization.

Generally, steric stabilization for the ink production seems to be better than electrostatic. Steric stabilization consists of attaching polymer chains to the surface of particles wherein the chains may be chemically attached or physically adsorbed on the particle surface. As the result of the polymer's presence, the particles cannot come close to each other and remain dispersed in the liquid. This kind of stabilization is more effective in the case of concentrated solutions; it may be applied to multicomponent systems, and agglomerates formed can be broken again into individual particles.

For steric stabilization the poly(vinyl pyrrolidone) (PVP) can be used as the polymer. PVP has a structure of a polyvinyl skeleton with two groups of the opposite polarity – hydrophobic and hydrophilic (Fig. 14.7), where n is the polymerization number. The easiest way it can be explained is that the hydrophobic group surrounds the metal particles preventing their agglomeration, while the hydrophilic chain has a high affinity for water and other polar solvents and results in excellent dispersion of nanoparticles in a liquid. In fact, PVP's effect on the silver nanoparticles may be more complicated [51].

When silver particles are synthesized from $AgNO_3$ by chemical reduction processes, it was stated that the mole ratio $PVP/AgNO_3 = 1.5$ is a critical value. If the ratio was less than 1.5, the PVP protection effect was not complete, whereas if the ratio was above this value, further polymer protection became unnecessary [51].

PVP can be very effective for maintaining the stability of ink. As presented in Fig. 14.8, the ink containing Ag particles with average diameter of 50–70 nm covered by PVP layers show high stability of parameters for at least 6 months [96].

In the literature concerning inkjet printing conductive structures, information about the type of protective polymer layer is given rather rarely. However, one can find, apart from PVP [44, 46, 51, 52, 54, 100], that the following polymers are also used as protective layers:

- Poly(acrylic acid), PAA [43, 45]
- Carboxymethyl cellulose, CMC [49]
- 3-Mercaptopropionic acid [70]



Fig. 14.8 Viscosity and silver content in the ink (measured according to Eq. (14.2)) vs time

- Amine-type dispersant [60]
- Alkylamine [91]

Electrostatic stabilization is proposed mostly for water-based inks. Using CMC as an organic protective layer, it was stated that an ink with silver nanoparticle content of 1.1 wt% was relatively stable. However, during 7 months of storage at ambient temperature, the average particle size increased from 40–70 to 90–120 nm [49].

Table 14.1 presents the production methods for making the silver nanoparticles with small sizes suitable for inkjet printing. Kosmala et al. [50] propose a different approach in which a complicated organic protective layer plays an important role. Produced by a simple and cost-effective wet chemistry method, silver particles agglomerate to relatively large sizes in the range of 10–300 nm, with the majority of particles larger than 120 nm. The ink was prepared by dispersing Ag nanoparticles in water with the presence of a triblock copolymer, PEO-PPO-PEO, and then being treated with high-intensity focused ultrasound. The presence of polymers poly (ethylene oxide)-hydrophilic and poly(propylene oxide)-hydrophobic reduces agglomerates to ~50 nm. During 20 days the viscosity increased no more than 10%, and no sedimentation was observed.

After silver nanoparticle production, the content of the polymer protective layer C_{pl} is only a small part of the silver particle mass – usually less than few wt.%. This value can be estimated by polymer removal in high temperature according to the simple equation:

$$C_{pl} = \frac{m_{Ag+pl} - m_{Ag}}{m_{Ag+pl}} \cdot 100\%$$
(14.3)

where m_{Ag+pl} is the mass of the silver nanoparticles coating with the protective layer and m_{Ag} is the mass of pure metallic silver, measured after thermal heating. For example, it was stated that the silver particles with average size of 50–70 nm lost 0.8% of their weight after heating at a temperature of 500 °C for 1 h, which indicates the C_{pl} value [97].

14.4 The Principle and Equipment for Inkjet Printing

Inkjet is a noncontact dot matrix printing technology in which droplets of ink are jetted from a small source directly to a specified position on a printing substrate to create an image. The process can be controlled by digital signals which allow the system to create single drops. More precisely, a small liquid column leaves the printing head, breaks off, and forms a droplet which flies freely through the air (Fig. 14.9).

Inkjet printing technology has a long history [102, 103]. Initially, it was used in the publishing and graphics industries. The patent (from 1965) for thermal inkjet printing [104] and patents (1972) where the piezoelectric effect was proposed for forcing a droplet from a printing head [105, 106] were milestones which enabled the use of this technique in other industries. Now, inkjet printing has been implemented in many different designs and has a wide range of potential applications [107]. There are two basic technologies of inkjet printing which have been used in the laboratory and industry: continuous inkjet (CIJ) and drop on demand (DOD) [108].

Continuous inkjet systems produce a pressurized fluid stream which is broken into droplets using a piezoelectric element. By stimulating the piezoelectric element at high frequencies (in the range of 20 Hz to 80 kHz), capillary waves are generated within the fluid domain, and the fluid stream forms continuous and consistent droplets with uniform size and spacing. Depending on the drop deflection methodology, CIJ can be designed as a binary or multiple deflection system. In a binary deflection system, the drops are either charged by special electrode or uncharged. Next, the drops pass through the electric field generated by high-voltage deflector plates that deflect the charged droplets which are collected into a gutter for recirculation. The uncharged droplets are allowed to fly directly onto the substrate. When a substrate is moved (in the x–y directions), droplets make the printed pattern. Of course the alternative system can be applied; uncharged particles are trapped, but charged drops are deflected, leave the printhead, and form a pattern on the substrate.



Fig. 14.9 The steps of droplet formation in inkjet technology [101]



Fig. 14.10 Continuous inkjet printing (CIJ): the drop generator works continuously, and a pattern on a substrate depends on the deflection system. (Adapted from [108])



Fig. 14.11 Drop-on-demand (DOD) inkjet printing: single droplets are ejected through an orifice at a specific point of time

The multiple deflection system has more control possibilities. Droplets are charged and deflected at different levels to create an image without moving the substrate (Fig. 14.10). The uncharged drops fly straight to a gutter to be recirculated. The system is particularly useful for 3D printing [109], as the ink droplets travel a relatively long distance (100 mm) before being deposited onto the substrate.

The majority of activity in inkjet printing today is based on the drop-on-demand method. Depending on the mechanism used in the drop formation process, the technology can be categorized into four major methods: thermal, piezoelectric, electrostatic, and acoustic inkjet. Most of the DOD inkjet printers on the market today make use of a piezoelectric principle (Fig. 14.11). In this system, one single



Fig. 14.12 Different piezoelectric drop-on-demand technologies [110]

drop is ejected through an orifice (the printhead nozzle) at a specific point in time. As a substrate moves opposite to the drop's source, the combination of the speed and direction of substrate movement, as well as the frequency of "shots" or breaks, makes it possible to obtain the required printed pattern shape.

Depending on the piezoelectric deformation of the ceramic element and the force causing the ink ejection, the printing systems can be further classified into four main types: squeeze mode, bend mode, push mode and shear mode (Fig. 14.12) [110]. For the squeeze mode, radially polarized tubes are used. In both bend and push mode designs, the electric field is generated between the electrodes parallel to the polarization of the piezo-material. In a shear mode printhead, the electric field is designed to be perpendicular to the polarization of the piezo elements (Fig. 14.12) presents only part of the system – the cross section perpendicular to the direction of the jets).

The much more popular system uses a piezo actuator which surrounds a glass capillary. The end of the capillary forms a nozzle with diameter in the range of a few dozen of micrometers. Applying a voltage pulse, the piezo actuator contracts and creates a pressure wave which propagates through the glass into the liquid. In the nozzle region, the pressure wave accelerates the liquid with up to 10^5 g [94], and droplets are formed (Fig. 14.9). This part of the printhead is defined by two parameters, nozzle diameter and volume of ejected liquid. Typically, the diameter of the nozzle ranges from 20 to 100 µm, but smaller orifices (e.g., 12.1 µm [84]) are also used. The majority of printers have cartridges with volumes of 10 pl, but for very fine printing, a drop has a volume of 1-2 pl [76, 84, 86]. Standard heads generate drop rates up to 2000/s and a maximum throughput of 1 µl/s. Such printing efficiency is possible under the condition that the liquid viscosity does not exceed

several tens of mPa·s for unheated systems. When the reservoir of liquid and the printhead are heated, it is possible to print ink with a higher initial viscosity as it tends to diminish with increasing temperature, according to Eq. (14.1). In practice, however, as is apparent from Table 14.2, inks in use have viscosities of less than 20 and mostly less than 10 mPa·s.

The DOD inkjet printing process consists of five stages: drop ejection, drop flight, drop impact, drop spreading, and drop solidification. The size, shape, and volume of the ejected droplets are affected by a number of factors of the printhead and fluid features, mostly viscosity and surface tension. Surface tension plays an important role in droplet formation. The smaller the volume, the higher the force that keeps small drops together. Liquid acceleration inside and outside of the droplet generator nozzle makes these phenomena much more complicated. 3D simulations of the droplet formation during the injection printing process show that formation of the meniscus and its shape are the results of both pressure and surface tension, which significantly influence the generation process [111]. The surface tension of ink mostly ranges from 20 to 40 mN·m⁻¹ (Table 14.2).

It was calculated by numerical analysis and experimentally observed that droplet formation also depends strongly on the shape of the electrical pulse applied to the piezo actuator. Chen et al. [112] stated that higher operating voltages result in larger ejected ink droplets but that there is also an optimal discharge time interval. On the other hand, Meyer [94] concluded that increasing the voltage pulse on the piezo actuator causes an increase in drop speed that means an increase of the kinetic energy of the system leading to a larger drop volume. The dependence is almost linear, and with changing the voltage from 60 to 120 V, the drop speed increases more than 3.3 times.

The droplet shape should be nearly spherical. Sometimes a long tail may form from the droplet due to the droplet ejection conditions. This tail may eventually collapse back into the body of the main droplet, or it may separate and break into a stream of smaller droplets, called satellite droplets [102]. The diameter of a flying spherical drop depends on its volume (e.g., 2 pl \rightarrow 16 µm [21]) and may reach a value of less than 1 µm in a super fine inject system [76].

Every singular ejected drop for each "shot" of printing action makes dots on the substrate. The deposition mechanism of a discrete droplet on a substrate can be separated into two stages [113]: an impact-driven stage in which the impact kinetic energy is dissipated and a surface energy-driven stage where the droplet spreads to a diameter dependent upon the surface energy interactions between the ink and the substrate, which play a fundamental role influencing the wettability of a solid surface by a liquid. High surface energy of the substrate induces smaller contact angle and spreads the ink deposits (θ_{C1} in Fig. 14.13). Such surfaces are called hydrophilic. Hydrophobic surfaces are characterized by low surface energy and allow better control of the ink when the contact angle is higher (θ_{C2}), enabling printing of more sophisticated structures. It was found that for such surfaces with proper subsequent droplet overlap and printing speed, the printed line width may be smaller than the droplet diameter [70]. Generally, there is a strong correlation between increasing line width and decreasing contact angle θ of the ink on the substrate



Fig. 14.13 The contact angle θ_C which specifies the wettability; γ_{SG} , γ_{SL} , and γ_{LG} – solid-gas, solid-liquid, and liquid-gas interfacial energies, respectively

surface [73]. It is worth noting that the adhesion of inkjetted materials to the surface is better in the case of better wettability [75].

The surface energy can be modified using various surface treatment agents or other treatments such as plasma or UV-ozone. Guidelines for surface treatment conditions are hard to give because the proper conditions depend on substrate materials, inks, and surface treatment materials. Environmental conditions such as temperature and pressure also affect the ink behavior [75]. The solution may be an additional material layer deposited on the substrate which changes its surface energy to obtain higher resolution of the printed line. When a hydrophobic pattern was deposited on a hydrophilic polyimide surface (treated beforehand by O_2 plasma), the ink droplets move away from hydrophobic to hydrophilic areas. As a result, smoother gap widths of about 15 μ m were obtained [114].

In addition to the surface energy, the printing algorithm is crucial to the printing quality. The printing algorithm defines in which order ejected droplets form the final pattern. If a high-resolution pattern is printed in a non-sequential manner, singular drops may join each other forming bigger drops that cause bulking of lines. With a proper algorithm of printing, separate droplets have time to dry, and the adjacent droplets do not merge together. It can be done by dividing the final printed picture into a few parts that are printed one after another. In each printing pattern, dots do not touch each other and only after the final printing stage is the picture obtained without gaps and voids, as expected [115]. Of course, the final resistance of the path depends on the number of printed layers (one on the other after drying the former one), which is clearly related to the total thickness. However, resistance does not decrease linearly with increasing amounts of printed layers [45].

It is desirable to receive dots of very regular shape and highly uniform structure (Fig. 14.14 left) on the substrate. The shape of dots remains symmetric if the substrate moves only during the break between "shots." Otherwise, if the substrate is moving very quickly, the dot shape will be deformed as it can be seen in Fig. 14.14 (right).

The combination of shot frequency, substrate speed, and the number of passes may lead to forming printed lines with slightly deformed edges (Fig. 14.15 left) or, as is usually desirable, to forming lines with stable width and thickness (Fig. 14.15 right). The possibility of printing more complicated figures depends on the control software of the X-Y table which moves the substrate, the algorithm of printing, and the substrate temperature. This temperature influences the rate of the diluent evaporation and decides whether the next droplet overlaps the previous one which



Fig. 14.14 Singular printed dot [34, 61]



Fig. 14.15 Printed lines [34, 61]

already has the form of a solid or is still liquid. In practice, the substrate temperature is on the level of a few hundred degrees, but its range may be from ambient temperature up to even $150 \,^{\circ}$ C [81, 90].

Active alignment control makes printing more precise. The system consists of nozzles, image sensors, and a target tracking system. Each nozzle is integrated with a micro-lens for an image sensor and a pair of electrodes to control inkjets according to the output of the image processing. The performance of the target detection system was accurate enough to obtain 5 μ m precision alignment. The fabricated nozzles achieved the patterning of Ag nanoparticles, which can be used as conductive wires after sintering. The width of the pattern was less than 20 μ m with errors less than 3 μ m [116].

On the hydrophilic surface, the printed dot may not be uniform in its structure (as shown in Fig. 14.14 left) and may have a diameter many times greater than the diameter of the droplet. Additionally, the silver nanoparticles are gathered almost solely on the periphery of the resulting spot. This self-assembly phenomenon named as the "ring stain effect" or the "coffee-ring effect" appears due to the specific suspension flow and nonuniform evaporation of the solvent during droplet drying [90, 117]. Under normal inkjet printing conditions, the coffee-ring effect is detrimental, and both the ink and printing parameters are chosen to avoid such a shape. It was found, however, that this effect can be particularly damaging when

low-viscosity ink is used for printing narrow lines. Heated at a constant temperature of 200 °C, lines in cross section have a concave shape caused by this "coffee-ring effect," as small droplets exhibit accelerated solvent evaporation rates, resulting in preferential evaporation of the solvent near the edges. FE-SEM images reveal numerous large voids in the center produced by convection flow, which transports nanoparticles from the center to the edge during ink solvent evaporation. As a result, the resistivity (calculated according to Eq. (14.4)) of the narrowest lines is about fourfold higher than that of the widest lines with more homogeneous structure [92]. It was stated that the "coffee-ring effect" can be eliminated by mixing the diluent with ethylene glycol, which could eliminate particle segregation during evaporation [82].

On the other hand, the "coffee-ring effect" has been used to print parallel lines [52]. In this process, a linear liquid pattern was printed. Next, according to the "coffee-ring" phenomenon, silver particles were continuously transported toward the edge of the printed pattern creating two parallel lines, with an average of $5-10 \mu m$ width in the cited case and with the distance between them of 60 and 80 μm . This twin-line deposition technique allows the printing of more complex structures such as sets of rectilinear grids [118].

14.5 Electrical Conductivity of Printed Microstructures

Shortly after printing, the physical state of a pattern depends on ink properties. However, it is desirable to quickly receive a solid form by diluent evaporation, and in many cases for this reason, the substrate is heated in the printing process. The solid microstructures are electrically nonconductive, because, as it was mentioned earlier, each silver nanoparticle is covered with an organic protective layer. The most important function of this layer is to prevent aggregation of metal particles as well as to keep them stable in a suspension. This electrically insulating layer at relatively low voltage makes DC conduction impossible, and to obtain good electrical conductivity, the printed structures require an additional procedure to remove this protective layer and convert to a bulk metal-like structure. In the literature, this procedure is usually called a sintering process.

The measure of the usefulness of printed structures in electronic packaging is their conductivity. However, more often the resistivity ρ (in $\Omega \cdot cm$) is in use. Electrical resistance *R* (in Ω) of a printed strip with constant geometry, width *w*, thickness *h*, and length *l*, allows you to calculate the material resistivity according to the formula:

$$\rho = R \frac{w \cdot h}{l}.\tag{14.4}$$

Of course, the aim is to get the value of ρ close to the resistivity of bulk silver, i.e., $1.59 \cdot 10^{-6} \ \Omega \cdot cm$. However, it should be noted that the thickness measurement may

be laden with significant inaccuracy. The measurement is performed with limited precision (e.g., $0.8 \pm 0.3 \,\mu\text{m}$ [119]), and a printed structure in cross section generally has a shape deviating from the rectangular form (e.g., [78, 89, 90].) It was stated that when low-viscosity silver ink is printed and heated at a constant temperature of 200 °C, the wider printed lines (>0.400 μm) were convex in shape, but the narrower printed lines (<300 μm) were concave [92]. Therefore, resistivity values reported in the literature as estimated according to Eq. (14.4) should be considered approximate. The exact resistivity value should be calculated from the formula:

$$\rho = R \frac{A}{l} \tag{14.5}$$

where A is cross-sectional area of printed line, which is difficult to measure.

Table 14.3 summarizes the different sintering methods that are presented in the current literature. In fact, the overall thermal heating is one of the easier ways to remove the organic layer which separates individual nanoparticles. The result is observed as the decreasing of structure resistance R (Fig. 14.16). From this, and similar [119, 121] graphs, it can be observed that the thermal process of conductance improvement consists of three parts: the first in which in heating temperature the high resistance remains stable; the second, when the resistance decreases in a relatively short period of time; and the third with low resistance changes. It is interesting that if the final resistance is almost the same for the range of 195–240 °C temperature changes, the time of the first part of the heating process is much longer with lower temperature.

The sintering process consists of two stages. In the first, thermal decomposition and removal of protective layer is the dominant phenomenon. At the beginning of this stage, the resistance drops significantly. It seems to be clear that removing the protective layer makes a lot of new electrical paths between the particles in a short period of time, and printed structures start to be conductive. Such a conclusion can be supported by the result of impedance measurement at different frequencies. Figure 14.17 presents impedance modulus spectra after different times of heating at 250 °C. The straight lines after 50 min of heating indicate the removal of the protective layer. However, the more interesting observations are for when the protective layer is not completely removed at shorter heating times. The electrical chart representing printed layer that time indicates the lack of homogeneity of the layer, which presents parallel branches for current transport, resistance for continuous paths, and capacitive for separated particles [36]. Also DSC curves show an endothermic reaction at this stage, which indicates progressive mass reduction [121].

In the second stage, when the protective layer is removed, the diffusion (or partial melting) and recrystallization phenomena start to play a dominant role. SEM observation of the specimen surface reveals the nucleation of pure Ag particles in the form of spheroids of diameters about 0.1 μ m [61]. There is again a strong endothermic reaction which indicates sintering via diffusion and other processes, and in this stage, a mass reduction cannot be seen [121]. The images of silver pattern surface (Fig. 14.18a, b) show that the grain sizes increase dramatically after 30 min heating time [88]. At higher temperatures the grain growth is more spectacular (after 60 min

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10–50 <600 [129]
Photonic flash Time [ms]
≤5 [47]
[122]
5–10 ≤1 [46]
>500 [93]
Plasma radiation Gas Time [min]
5–10 Argon ≤ 60 [77]
≤60 [56]
10–50 >60 [122]
[71, 87]

Table 14.3 Sintering methods and final resistivity of printed structures

(continued)

		Sintering paran	neters	
Sintering method	Sintered structure resistivity $[10^{-6} \Omega \cdot cm]$	Temperature [°C]	Time [min]	References
Microwave			Time [s]	
radiation	<u>≤5</u>			[85]
	10–50		240	[78]
Electrical			AC/DC	
excitation	≤5		DC	[79, 89]
	5-10		AC	[130]
Chemical reaction		<i>Temperature</i> [°C]	Time [min]	
	≤5	>150		[45]
	5–10	Ambient		[45]
	10–50		≤100	[91]
			>100	[55]

 Table 14.3 (continued)



Fig. 14.16 The changes of printed structure resistance during heating time at different temperatures [40]

at 400 °C – of about 2500% [127].) However, it is difficult to explain the characteristic decrease in electrical resistivity of the printed structures only by grains size changing [119]. Probably the shrinkage phenomenon plays also an important role. The shrinkage of 25% was observed when printed structures were sintered at 250 °C for 3000 s [90].



Fig. 14.17 Dependence of the impedance modulus spectra of the printed layer on the sintering time at 250 °C in the air [131]



Fig. 14.18 FESEM images of printed microstructures: (a) before sintering, (b) after sintering at 250 °C for 30 min, (c) after laser sintering for 1 s [88]

The total time of the sintering process is difficult to estimate. However, with some assumptions (in the case of dependences presented in Fig. 14.16), it was estimated that the sintering process is consistent with an Arrhenius law with activation energy of 1.05 eV [39]. It is also calculated that the activation energy of the first stage is much higher than that of the second stage [132]. The sintered material shows a typical metallic type of conductance with temperature coefficient of resistance equal to 2080 ppm/K, which is a lower value than for bulk silver (3800 ppm/K) [40].

Diffusion and recrystallization of the silver particles take place after removal of the protective layer. However, the removal is a continuous process (Fig. 14.19), and there is no clear limit of the sintering stages. After heating of printed structures (with



Fig. 14.19 Weight loss of protective layer during the thermal process, measured according to Eq. (14.3) [96]

the use of the ink other than the one previously analyzed) for 1 h at 150 °C, the resistivity was estimated at $5 \cdot 10^{-5} \Omega \cdot cm$, despite the presence of the residue of the protective layer [96].

The sintering process may be accelerated by applying a high-efficiency heat source (e.g., a laser beam) which only directly affects the printed structures. Numerical modeling predicts that surface temperatures can reach more than 250 °C, while the temperature just several tens of micrometers below the heated surface is only slightly higher than room temperature [129]. This is the reason why the laser beam can be effectively used to sinter structures printed on low-cost transparent polymer substrates which are not resistant to high temperatures.

The method needs selective tracking of a laser beam and delivery of the precise amount of energy into the printed pattern. The second requirement is especially difficult to meet, as the beam has a Gaussian energy distribution. Therefore, in order to obtain a beam having a uniform energy distribution, some additional optical elements are necessary. For example, a series of cylindrical lenses and an iris can transform a Gaussian laser beam of 2.2 mm diameter to a sheet beam of 7.0×0.2 mm cross section with an energy variation no more than 12.5%. Such a beam irradiating a printed structure for only 1 s yielded a resistivity of $9.5 \cdot 10^{-6} \Omega \cdot cm$. This time was too short for recrystallization, and as it can be seen in Fig. 14.18c, the grain size is almost unchanged, although the boundaries of the silver nanoparticles are merged [88].

It is worth noting that the sintering effects depend on laser beam wavelengths. Near-infrared lasers have a poor absorbance but good transmittance in the silver-rich printed structures. In such case the light reaches the substrate surface and the generation of heat starts there. The heat then sinters the structure from the substrate side to the structure surface together with a relatively calm evaporation of residual diluent and the organic protective layer. As a result, a printed pattern is formed with uniform adhesion as well as a dense structure with relatively small pores. In contrast, visible lasers, having high absorbance and almost no transmission, sinter almost all the structure near the surface before reaching the substrate. An explosive evaporation of the organic substance leads to the formation of a sintered structure with large pores and a coarse-grained surface [60].

At this point it is necessary to mention the subtractive technique of laser sintering. In this technique, the surface is coated with an ink containing silver nanoparticles, wherein the laser beam heats only a desired structure with high accuracy. After the laser sintering process, the remaining nanoparticles are removed by washing in an organic solvent [133, 134].

Without the precise tracking of a laser beam, light can also be used in the photonic sintering method. The method is useful especially for low-cost mass production when structures are printed on transparent foil substrates. Pulsed light from a flash lamp irradiates all substrates, but only the printed structures translate the photonic energy into enough heat to sinter them, without overheating the substrate which is not resistant to high temperature.

Usually, high-energy flash lamps are used, and the overall delivered energy depends on the number of pulses. Figure 14.20 shows the influence of the pulse number on the resistance of printed structures. It can be seen that initially the resistance decreases rapidly with the number of pulses due to microstructure changes (e.g., after three pulses, the grain size is three times bigger than that of unsintered silver nanoparticles [47]) and then becomes stable. It means that in this technological condition, the sintering process has been finished and that subsequent pulses influence only the substrate foil which began to distort [135]. In fact, mostly, the layer near the top layer of the structure is sintered due to the photothermal effect in this region. The thickness of this near-surface layer of between a few tenths of nm and a



Fig. 14.20 Influence of the number *N* of light pulses (1200 J; 250 μ s) on the resistance, *R*, of printed structures with two distances from the lamp [135]

few tenths of μ m depends on two critical heat transfer factors, namely, the material properties and flash duration. Heating of the inner part of a printed structure depends also on the thermal conductivity of the substrate. Under the same photonic sintering conditions, the resistivity of a layer printed on PET amounted to $6.2 \cdot 10^{-6} \ \Omega \cdot cm$, while for one printed on photographic paper – about $5 \cdot 10^{-5} \ \Omega \cdot cm$. Photographic paper has much lower thermal conductivity, and the higher measured resistivity is due to defects in the substrate [46].

A significant advantage of the photonic flash sintering method is the short time of the process. When a xenon stroboscope lamp is placed at the focus of an elliptical reflector, very high photonic energy densities can be delivered locally. In a system with a 1000 W lamp, lines printed on inexpensive polymer foils (PET or PEN) were sintered up to about $1 \cdot 10^{-5} \Omega \cdot cm$ in 1 s [93].

The absorption of light from a flash lamp by a silver nanoparticle layer is easier to analyze and understand when a large area of thin film is illuminated. It was stated that there is significant densification of the photonically sintered silver, which reaches 84% of the bulk silver density. The light absorption by the uncured silver films is broadband, and that plasmon resonance is not the dominant feature of the phenomenon. This indicates that the absorption of the silver films acts like that of bulk silver rather than that of individual silver nanoparticles. The temperature simulations indicate that the nanoparticle films melt within 300 μ s from the beginning of the pulse during the photonic sintering process. This result indicates that traditional solid-state sintering models cannot be applied to photonic sintering [136].

Structures printed on foil substrates can be also sintered by plasma radiation. This process is carried out at a relatively low temperature without affecting the underlying polymer substrate. The best results were obtained using low-pressure argon plasma; with the exposure time of 60 min, the measured resistivity was reported as $1.34 \cdot 10^{-5}$ $\Omega \cdot cm$ [71]. To lower the resistivity after low-pleasure plasma sintering, the samples were additionally microwave flash sintered. The final resistivity of printed structures was in the range of $10^{-6} \Omega \cdot cm$ [56]. It is possible to accelerate the sintering process using the locally acting (plasma pencil) atmospheric pressure plasma. Such treatment, at a substrate temperature of 110 °C, delivers resistivity values of $1.55 \cdot 10^{-5}$ $\Omega \cdot cm$ after a single sintering pass, equal to a processing time of less than 4 s [87]. Of course the process requires precise tracking of printed structures by the plasma pencil.

It is difficult to predict the results of plasma sintering. The process starts from the top layer of the structures. Through-sintering does not occur with greater thicknesses than the penetration depth of the plasma species. It means that independently of the structure thickness, only its top layer determines the effective resistivity of the sintered material [77]. Additionally, results are strongly dependent on the structural morphology resulting from the ink properties, like polarity of the solvent systems, metal loading, and particle size [71].

An alternative to selective heating of the printed structure is the use of microwave radiation. However, the impact of the energy is limited, and the penetration depth of the microwave irradiation into silver at a frequency of 2.45 GHz is only 1.3 μ m. This means that such a method can be effective only for thin printed layers. The advantage

is the short processing time – within 240 s, the resistivity of the material reached $3 \cdot 10^{-5} \Omega \cdot \text{cm}$ [78]. Lower values of the resistivity can be obtained using special antennas; however the surface area influenced by the microwave energy is limited to tens of mm². The effect strongly depends on the total antenna area, the pre-curing time, and the geometry of the printed lines [85].

It is well known that an electric current flowing through a conductor generates heat. The effect has been used for the electrical sintering of printed structures. After application of a DC, the process is very rapid – the major transition occurs within a few seconds or even microseconds, with the final resistivity close to that of bulk silver [79, 89]. Besides advantages (extremely short sintering times, reducing substrate heating as heat generation occurs only in the printed layer), the method has significant drawbacks:

- Every printed line (with stable width and thickness) sintered separately needs ohmic contacts for the application of voltage.
- The resistance of synthesized structures may change by several orders of magnitude during processing, which requires special power supplies to protect the structure against damage.

As the protective layer separates the individual silver particles in the printed structure, AC also seems to be effective (Table 14.3). A high-voltage, high-frequency source was used for electrical excitation of the printed structure, but an additional impedance matching circuit (impedance transformer) was placed between the voltage source and the sintered layer to avoid sample destruction due to excessive current flow. In the first stage, the applied high voltage (10 kV, 80 kHz, 1 s) partially destroys the protective layers, and an electrically conductive path is formed. During the next stage, a lower voltage is generated (100–300 V, 50 kHz – 1 MHz, 5 s), and finally, the initial resistance decreases from several M Ω to a dozen Ω [74]. Unfortunately, because of the requirement for constant connections to the power supply, the method cannot be applied in mass production with roll-to-roll printing systems. For such production, electrical sintering with microwave contactless heads [130] has greater application prospects.

It is also possible to achieve acceptable electrical resistivity at lower temperatures. Ag nanoparticles protected by dodecylamine are successfully sintered at room temperature in an air atmosphere. In order to remove the protective layer, printed structures were dipped in methanol. Figure 14.21 shows the microstructural changes of Ag nanoparticles by the methanol dipping process. As shown in Fig. 14.21a, Ag nanoparticles of average diameter of 7 nm are packed in a highly dense structure. After 1 h dipping, as shown in Fig. 14.21d, the Ag nanoparticles completely disappeared, and a high-density Ag structure was achieved. As a result, after 2 h dipping, the sintered structures possess resistivities of $7.3 \cdot 10^{-5} \ \Omega \cdot cm$ [55]. Otherwise, the surface on which structures are printed may be coated with a component which reacts with the organic protective layer covering the Ag nanoparticles. For example, ink containing Ag particles with PAA as the protective layer was printed on photo paper pre-coated with poly(diallyldimethylammonium chloride) (PDAC). PAA and PDAC react with each other which makes spontaneously printed patterns



Fig. 14.21 The microstructural changes of printed structure surface observed by FE-SEM: (a) initial state, (**b–d**) after dipping in methanol for 180 s, 600 s, and 3600 s, respectively [55]

conductive at room temperature. The resistivity of the twice-printed structures was measured as $1.39 \cdot 10^{-4} \ \Omega \cdot cm$ or $1.08 \cdot 10^{-5} \ \Omega \cdot cm$ after heating at 180 °C [45].

Overall thermal heating is still the most reliable method for sintering of printed structures made on the basis of silver nanoparticles. However, the large-scale, speedy printing techniques (e.g., roll-to-roll) on low-cost flexible substrates with low thermal resistance require the use of an alternative sintering method. In this respect four printing techniques were compared to assess:

- The resistivity of sintered structures
- Roll-to-roll compatibility (suitability for the large-scale manufacturing)
- Temperature (influencing a substrate material)
- Controllability (how well the sintering process is controlled)

For each criterion (except resistivity), the number of characters negative indicates poor results, while good results are indicated by the number of characters positive. This subjective comparison is presented in Table 14.4.

It can be seen from the table that none of the comparative method is ideal for large-scale printing on flexible substrates with low thermal resistance; however, photonic sintering can be identified as the most promising alternative sintering technique to replace conventional thermal sintering.

		Roll-to-roll	Sintering	
Sintering method	The lowest resistivity	compatibility	temperature	Controllability
Overall thermal heating	$3.6 \cdot 10^{-6} \Omega \cdot cm$	2(-)	2(-)	1(+)
Laser beam radiation	$4,6\cdot10^{-6} \Omega\cdot cm$	2(+)	1(-)	3(+)
Photonic flash	$3.3 \cdot 10^{-6} \Omega \cdot cm$	3(+)	3(-)	2(+)
Plasma radiation	$1.5 \cdot 10^{-5} \Omega \cdot cm$	3(-)	3(+)	1(+)

 Table 14.4
 The usefulness of sintering methods in large-scale printing on low-cost flexible substrates [123]

The electrical properties of the printed structures were analyzed in this section. It may be also interesting to know that a sintered layer of silver nanoparticles has 82% density, 99%, specific heat, 68% thermal diffusivity, and 55% thermal conductivity of bulk silver [137].

14.6 Inkjet-Printed Conductive Microstructures

Inkjet printing has become the most attractive direct patterning technique due to its ability to create versatile designs with full digital control. Various types of electrically conductive printing macrostructures are expected to become key technologies for advanced electronics packaging. The main benefit is connected with fine pitch lines and space and easy scale up of products. The inkjet technology can be easily used for 3D stacking. It needs only repeating printing circuit layers over insulating layers by changing ink tanks. Vertical connection can be drawn by stacking ink drops without any contact between printheads and substrates (via holes can be filled with conductive ink drops).

In large-scale production, "printable electronics" on flexible substrates plays an increasingly important role in modern electronics. The basic condition of such production is the possibility to use cheap foils as the printing substrates. The first few materials listed in Table 14.5 can be assigned to this group. The table shows also the widths of the printed lines on these substrates but only in the range not higher than 200 μ m. In many publications the analyzed structures are printed with much larger dimensions which reduce the error in the evaluation of their resistivity (according to Eq. (14.4)).

Inkjet, the reliable printing technology, is more and more attractive to flexible electronic industries. Apart from the possibility of using low-cost flexible substrates, the technology has such advantages as:

- Direct printing of metal patterns on large areas
- Maskless production of structures of various in shape
- Real-time production by digital design
- Small loss of materials (as an additive process)

	Glass transition	Printed line	D.C
Substrate	temperature [°C]	width [µm]	References
PET (polyethylene terephthalate)	65-85	100–150	[88]
		150-200	[77, 125]
PC (polycarbonate)	~147	150-200	[77]
PAR (polyarylate)	~190	150-200	[125]
PEI (polyether imide)	~217	150-200	[125]
Photographic paper		50-100	[79, 130]
		50-100	[10]
		100-150	[46]
PI (polyimide)	360-410	≤ 10	[59]
		10-50	[70, 83, 86]
		50-100	[67, 130, 138]
		100-150	[46, 72]
Glass	>500	≤10	[139]
		100-150	[88, 90]
Silicon		≤10	[76]

Table 14.5 Width of lines printed on different substrates

But the essential question is whether such patterning made by silver nanoparticles can be competitive to "traditional" technologies used to create electrically conductive structures and contacts with regard to trace resolution, surface quality, microstructure, and electrical conductivity. The results of such comparisons are presented in Table 14.6.

Since there is no standard specification for acceptance of ink traces, criteria based on IPC-601311 [141] were set up to evaluate the trace resolution. An acceptable resolution should satisfy the following two requirements:

- 1. Deviation of the trace width from the nominal resolution is less than 20%, e.g., for a nominal resolution of 75 μ m, the trace width must be within the range of 60–90 μ m.
- 2. Trace boundary is sharp and parallel, with no metal shifted out of the defined trace boundaries.

If either of the requirements is not satisfied, the printed circuit is deemed unacceptable. However, it would be difficult to arbitrarily designate an acceptable resolution of line/space width, and it should be assumed that it is not worse than those obtained in other technologies.

The types of substrates and pattern features listed in Table 14.6 demonstrate that inkjet printing has technical advantages over other technologies. It has higher resolution, lower resistivity, denser structure, and a shining surface. Another advantage of Ag layers over thick film Cu is that it has higher resistance to humidity and corrosion so no cover layer is needed to protect it.

Industrial applications need special requirements with relation to the ink and technology. For stable ejection of such ink, it is required that aggregation and

Table 14.6 Pattern features I	made by different techno	logies and materials (columns 2	2-5 from [140], column 6	from Tables 14.1	, 14.3, and 14.5)
Technology	Lithograph film Ag	Thick film Ag	Thick film Cu	Etched Cu	Inject printing
1	2	.0	4	5	9
Material	Particles Ag, 1–2 µm with epoxy resin, ink	Particles Ag, 1–5 µm with epoxy resin	Particles Cu, 0.2–1 µm	Cu clad	Particles Ag, ≤10–100 nm with diluent
Substrate	Polyester	Polyester, polyimide	Polyimide	Polyimide	PET, photographic paper, polyimide
Curing/sintering conditions	125 °C, 4 min	150 °C, 3 min/320 °C, 6 min	320 °C, 6 min	125 °C, 4 min	Ambient, $\leq 150-250$ °C, ≤ 1 ms-120 min
Nominal resolution (line/space width) [µm]	50-250	100-400	100-400	50–250	≤10-200
Acceptable resolution (line/space width) [µm]	<u>></u> 200	≥150	≥150	≥50	
Resistivity [Q·cm]	$3.6 \cdot 10^{-2}$	$9.1 \cdot 10^{-5} / 6.7 \cdot 10^{-5}$	$6.2 \cdot 10^{-5}$	$2.2 \cdot 10^{-5}$	$\leq 5 \cdot 10^{-6} - 1 \cdot 10^{-4}$

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Fig. 14.22 Fine pitch pattern formation, with line and space 30 μ m/30 μ m formed by screen printing [35] (left) and by inkjet printing [59] (right)

sedimentation of particles must be inhibited under any conditions and that the ink used does not increase the viscosity at the meniscus, which is the surface of the liquid-air boundary near the nozzle of the printhead. For high productivity of printable electronics, drop volume uniformity is important to use many nozzles or many heads (usually more than 100). It is recognized that the drop velocity is proportional to drop volume which determines the line width of printed patterns or the thickness of printed areas. The uniformity of drop volume on the level of $\pm 1\%$ and the drop placement accuracy of $\pm 3 \ \mu m$ seems to be enough for industrial uses of inkjet technologies.

Acceptable pitch resolution (listed in Table 14.6) is in the range not higher than 200 μ m. Such a value is reached by using conventional conductive pastes in screen printing technology. Ag nanoparticle pastes can easily form the fine pitch pattern with line and space widths less than 50 μ m by screen printing. Figure 14.22 (left) shows an example of the fine line with line and space of 30 μ m/30 μ m formed on an alumina sheet after firing [35].

Finer patterns can only be achieved by inkjet printing. Figure 14.22 (right) presents a set of wiring lines printed with ink containing Ag nanoparticles on glass [59]. The width of the lines is about 3 μ m on a 10 μ m grid in the lattice area. The ink contains Ag nanoparticles with an average size of 5 nm.

In the electronics industry, direct circuit patterning based on the bit-map data transferred from CAD [1] enables fast printing of electrical circuits on different rigid or flexible substrates, even on fabrics (Fig. 14.23), that are the base for electronic components packaging. In a printing machine, two lines of 180 nozzles each may produce multilayer circuit boards [142]. During the first step of the production process, the metallic pattern is printed on the insulation layer, and then vertical wiring posts are formed, joining the layers of metal wiring. The second layer of insulation is made, avoiding the posts, and the second pattern layer is printed. By repeating the steps, it is possible to form multilayer circuit boards. In the 20-layer circuit board with a thickness of 200 μ m, there are Ag line widths of 50 μ m, thickness of 4 μ m, and a minimal line pitch of 110 μ m.



Fig. 14.23 Printed circuit on flexible substrates with low thermal resistance [143]

Inkjet printing was found to be a promising and capable technology for the industrial-scale manufacturing of passive electronic devices, such as capacitors, diodes, and with some constraints, for coils printed on polyethylene naphthalate (PEN) substrates [144] or on LTCC ceramics [145]. It is also possible to create 3D microstructures. A simple form of pillar with high aspect ratio could be built by ejecting droplets at the same spot. The condition is that the drying time is extremely short. With the life time of the wetting area estimated at only about 0.1 s, the pillar with height of 80 µm is created in about 3 s [76]. By moving the inkjet head, it is possible to construct more complicated microstructures like micro-plugs or microsocket arrays [76] or a three-dimensional MEMS system [81]. It is also possible to make electrical connections between layers in multilayer printed circuit boards. Such connections are usually done by holes with small diameters filled by electrically conductive materials. The filling technology is simple; the surface of a board with a matrix of holes (usually formed by laser ablation) was inkjet printed from one or both opposite sides. As a result (Fig. 14.24) in polyimide substrates with a thickness of 100 µm and holes 30-60 µm in diameter, the resistances of connections were several hundred m Ω [120] (and single ohms for holes of 90 µm [146].) There are also trials with filling of through-silicon vias [80]. Such vias have been used in 3D packaging of microelectronic devices, where they provide electrical interconnections through stacked wafers and devices.

Electronic system production using inkjet technology offers several improvements compared to subtractive masking processes. Manufacturing processes can be more efficient, straightforward, and flexible, while expensive steps can be omitted. It is expected that more and more manufacturing systems will use inkjet printing, e.g., in a complex electronic module consisting of a whole functional subsystem [75, 115].



Fig. 14.24 SEM picture of a 40 μm diameter hole filled by an inkjet printing process [120]

There are more and more industries in which basic processes are carried out with inkjet printing technology using a very wide range of materials. This material can be resistive, semiconducting, sensitive, and more, but to produce an efficient system, it is also necessary to use electrical contacts and electrodes with a low resistance made with the use of inks containing silver nanoparticles (e.g., electrodes in solar cells [147].)

In recent years the possibility of inkjet printing antennas for radio frequency identification (RFID) tags using silver nanoparticle ink has been successfully studied. The read range of inkjet-printed RFID tags depends, among other things, on the antenna shape, the ink type, and the number of printed layers. Antennas can be printed on polyimide [148]; on polyethylene terephthalate (PET) [149]; on renewable, environmental-friendly materials such as wood, paper, and cardboard [150]; or even on leather substrates [151].

Similar material and technology can be used for near-field communication (NFC) antennas. They are printed directly also on a ferrite substrate using a silver inkjet printing process which improves parameters important for NFC [152].

It has been shown that the technology of inkjet printing using ink containing silver nanoparticles is highly useful in flexible electronics production. It is possible to obtain reliable, low resistance interconnects with controlled geometry between different components or special patterns of complex shapes. However, the required structures are possible to achieve only with the right technology and the right materials used.

The term right material means ink properties adequate for use, in particular:

- The diameter and shape of silver particles
- The organic protective layer covered metal particles which determines ink stability and has to be easily removable
- Viscosity and surface tension
- Levels of impurities

Also the substrate is important – particularly its surface, which should be well cleaned, in some cases activated, or even covered with another material.

Two technology steps may decide the final results, printing, and processes after printing. Proper printing which influences the shape of structure on the substrate requires the choice of:

- Types, numbers, and temperature of printing heads
- Volume of dots
- Printing frequency and speed of substrate to receive the proper dot spacing and printing pattern
- Temperature of substrate

The final technological step mainly decides the electrical conductivity of the printed structure. It is necessary to choose properly:

- Drying parameters of structures just after printing
- Sintering method
- Sintering process parameters

The right choice of the abovementioned factors makes inkjet printing of electrically conductive structures an increasingly important technology in the development of flexible electronics.

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Chapter 15 A Study of Nanoparticles in SnAg-Based Lead-Free Solders



Masazumi Amagai

15.1 Introduction

Tin-lead (Sn-Pb) solder alloy has been widely used as interconnection material in electronic packaging due to its low melting temperatures and good wetting behavior on several substrate platings such as Cu, Ag, Pd, and Au. Recently, due to environmental and health concerns, a variety of new lead-free solders have been developed. Lead-free solders lack the toxicity problems associated with lead-contained solders. However, unlike lead solders, the recently employed lead-free solders do not have a long history and manufacturing process, and also board-level reliability has not been established well. Especially, drop test performance is a serious concern for mobile products like cellular phones, cameras, video, and so on. Sn-Ag-Cu alloys are leading candidates for lead-free solders.

However, Sn-Ag-Cu alloys are not enough to meet severe board reliability requirements. Two lead-free solders were introduced in 2003 [1]. One was Sn-Ag-Ni-P. The other was Sn-Ag-Cu-P. Sn-Ag-Ni-P system has a balance of thermal cycling, bend, drop, and internal void test performance. On the other hand, Sn-Ag-Cu-P system has a significant advantage for drop test performance. The combination of Cu and P significantly reduced intermetallic compound (IMC) thickness.

Recent mobile electronic products (e.g., cellular phones) require a thermal aging process followed by drop and bend tests. Thermal aging affects IMC and Kirkendall voids. Kirkendall voids under IMC reduce the strength of solder joint and degrade drop test performance significantly. It was found that Kirkendall voids in lead-free solder joints could be greatly reduced by adding Ni and In to Sn-Ag-Cu. Sn-Ag-Cu-Ni-In, which was introduced in 2004 [2], improves drop test performance over Sn-Ag-Cu-P.

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Previous lead-free solders we introduced were four- or five-element-based leadfree solders. Effects of additional elements on the growth of IMC were not identified with so many elements in the solders. In this study, we focused on three elements to study the growth of intermetallic compounds. Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, and Au inclusions in Sn-3Ag-based lead-free solders were evaluated, to study whether these nanoparticles increase IMC thickness and grain size after four solder reflows. Also, IMC element analyses were carried out to study if nanoparticles were dissolved in IMC after one and four solder reflows. Then, Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, or Au inclusions in Sn-3.0Ag-based lead-free solders were evaluated to study whether these nanoparticles can reduce the frequency of occurrence of IMC fracture in high-impact pull tests. In addition to IMC analyses, the thickness of these nanoparticles on solder ball hardness was studied, since large solder displacement under drop impact improves drop test performance. Solder hardness is relative to solder ball displacement, so low solder hardness (soft solder) improves drop test performance. Therefore, the hardness test was performed to study if nanoparticles increase solder hardness after one solder reflow and two solder reflows +100 °C thermal aging (0 h, 100 h, 200 h). Finally, Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, or Au inclusions in Sn-1.0Ag-based lead-free solders were evaluated to study if these nanoparticles can improve drop test performance. Ni, Co, and Pt were very effective for drop test performance. Sn-1.0Ag was used to study drop test performance, since Sn-1.0Ag shows better drop test performance than Sn-3.0Ag [2].

In this study, it was found that adding Co, Ni, or Pt, located to the left of Cu in the periodic table, to SnAg-based solder alloys did not increase IMC thickness and grain size significantly after the solder reflow process and thermal aging. Hence, these nanoparticles resulted in good drop test performance compared to Cu, Ag, Au, Zn, Al, In, P, Ge, and Sb [3].

15.2 Nanoparticle Effects on Solder Intermetallic Compound Grain Size and Thickness

Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, or Au inclusions in Sn-3Ag-based lead-free solder balls were evaluated to study if these nanoparticles affect IMC thickness and grain size after four solder reflows. These solder ball samples were attached to OSP Cu solder pads through the reflow process (maximum temperature, 245 °C).

Figure 15.1 shows the sample preparation procedure to observe solder IMC grain size and thickness. Following the solder reflow process, solder balls were cut and polished with a sandpaper. To expose IMCs, solder balls were chemically etched using Meltex HN-980 M. The samples were then cleaned ultrasonically twice in water. IMC grain size and thickness were subsequently observed with scanning electronic microscopy (SEM).

Figure 15.2 shows IMC with Sn3.0Ag. (a, b) show a top view of IMCs and a cross section of IMCs after one solder reflow, respectively. (c, d) show a top view of IMCs and a cross section of IMCs after four solder reflows, respectively. (The same



Fig. 15.1 Sample preparation procedure

conditions will apply to a-d in subsequent figures below.) Four solder reflows increased the grain size and thickness of IMCs compared to one solder reflow.

Figure 15.3 shows IMC with Sn3.0Ag0.05Al. Four solder reflows increased the grain size and thickness of IMCs compared to one solder reflow. There is no significant difference between no aluminum and the inclusion of aluminum in Sn3.0Ag in the grain size and thickness of IMCs. Some voids were also observed for Sn3.0Ag0.05Al. This may be due to aluminum oxidation, since it is easy to oxidize aluminum. Based on the results, it was found that aluminum added to Sn3.0Ag could not reduce the grain size and thickness of IMCs compared to the no aluminum case.

Figure 15.4 shows IMC with Sn3.0Ag0.03Ni. There is a significant difference between no nickel and nickel in Sn3.0Ag in increasing the grain size and thickness of IMCs. 0.03 wt% Ni reduced the grain size and thickness of IMCs after four solder reflows, compared to no nickel case. Based on the results, it was found that the addition of nickel (in particular, 3% wt% Ni) to Sn3.0Ag was very effective for reducing the grain size and thickness of IMCs.

Figure 15.5 shows IMC with Sn3.0Ag0.5Cu. There is no significant difference between Sn3.0Ag and Sn3.0Ag0.5Cu in increasing the grain size and thickness of IMCs from one reflow to four solder reflows. Hence, it was definite that copper added to Sn3.0Ag did not affect the grain size and thickness of IMCs very much.

Figure 15.6 shows IMC with Sn3.0Ag0.03Co. As can be seen in the pictures, nano cobalt particles added to Sn3.0Ag were very effective for reducing the grain size and thickness of IMCs compared to the no cobalt case after four solder reflows.

Figure 15.7 shows IMC with Sn3.0Ag0.3In. There is no significant difference between no indium and the inclusion of nano indium particles in Sn3.0Ag in increasing the grain size and thickness of IMCs from one solder reflow to four solder reflows. Thus, it can be seen that nano indium particles added to Sn3.0Ag did not affect the grain size and thickness of IMCs significantly.

Figure 15.8 shows IMC with Sn3.0Ag0.3Sb. There is no significant difference between no antimony and the inclusion of nano antimony particles in Sn3.0Ag in increasing the grain size and thickness of IMCs from one solder reflow to four solder reflows. Thus, it was found that nano antimony particles added to Sn3.0Ag did not affect the grain size and thickness of IMCs considerably.

Figure 15.9 shows IMC with Sn3.0Ag0.1Zn. There is no significant difference between no zinc and the inclusion of zinc particles in Sn3.0Ag in increasing the grain

Fig. 15.2 Intermetallic compound with Sn3.0Ag. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows


Fig. 15.3 Intermetallic compound with Sn3.0Ag0.05Al. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



Fig. 15.4 Intermetallic compound with Sn3.0Ag0.03Ni. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



Fig. 15.5 Intermetallic compound with Sn3.0Ag0.5Cu. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



Fig. 15.6 Intermetallic compound with Sn3.0Ag0.03Co. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows







Fig. 15.8 Intermetallic compound with Sn3.0Ag0.3Sb. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



Fig. 15.9 Intermetallic compound with Sn3.0Ag0.1Zn. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



size and thickness of IMCs from one solder reflow to four solder reflows. As with aluminum, some voids were also observed for Sn3.0Ag0.05Zn and Sn3.0Ag0.1Zn. This may be due to zinc oxidation, since it is easy to oxidize zinc. As can be seen in pictures, it was observed that nano zinc particles added to Sn3.0Ag did not affect the grain size and thickness of IMCs tremendously.

Figures 15.10 and 15.11 show IMC with Sn3.0Ag0.03P and Sn3.0Ag0.1Au, respectively. Gold and phosphorus could not prevent increasing the grain size and thickness of intermetallic compounds from one to four solder reflows. Thus, it is obvious that nano gold or phosphorus particle inclusions in Sn3.0Ag did not affect the grain size or thickness of IMCs significantly.

Figures 15.12 and 15.13 show the IMC with Sn3.0Ag0.05Pt and the IMC with Sn3.0Ag0.05Ge. As can be seen in the pictures, nano platinum particles added to Sn3.0Ag was very effective for reducing the grain size and thickness of IMCs compared to no platinum case after four solder reflows. However, germanium could not prevent increasing the grain size and thickness of IMC from one to four solder reflows.

Table 15.1 summarizes the comparison of nanoparticles versus no nanoparticles added to Sn3.0Ag for the grain size and thickness of IMCs and also the change of the grain size and thickness of IMCs between one and four solder reflows. It is obvious that nickel, cobalt, and platinum play an important role for preventing the growth of IMC thickness and grain size.

15.3 Are the Nanoparticles Dissolved in the IMC?

IMC element analyses were performed to study if nanoparticles were dissolved in IMC after one solder reflow and four solder reflows. FE-SEM was utilized to observe elements in the IMCs.

Figure 15.14 shows IMC element analysis (wt%) for Sn3.0Ag0.03Ni. (a, b) show the element analysis after one solder reflow and four solder reflows, respectively. As can be seen in pictures, it is obvious that nickel was dissolved in Cu6Sn5 and subsequently formed (CuNi)6Sn5. The ratio of Ni:Cu:Sn for wt% was 1.3–2.9:43–53:45–54 and 1.2–4.0:42–54:43–55 for one solder reflow and four solder reflows, respectively. It seems that four solder reflows increased Ni wt% in the IMC compared to one solder reflow.

Figure 15.15 shows the IMC element analysis (wt%) for Sn3.0Ag0.03Co. (a, b) imply the same as mentioned previously. As with nickel, cobalt was dissolved in Cu6Sn5 and subsequently formed (CuCo)6Sn5. The ratio of Co, Cu, and Sn for wt% was 1.7–3.2:43–58:49–54 and 0.5–2.3:42–48:50–55 for one solder reflow and four solder reflow, respectively. Co wt% is smaller than Ni wt% in the IMC.

Figure 15.16 shows the IMC element analysis (wt%) for Sn3.0Ag0.05Pt. (a, b) imply the same as mentioned previously. As with nickel and cobalt, nano platinum particles were observed in the IMC. The ratio of Pt:Cu:Sn for wt% was

Fig. 15.10 Intermetallic compound with Sn3.0Ag0.03P. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



Fig. 15.11 Intermetallic compound with Sn3.0Ag0.1Au. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



Fig. 15.12 Intermetallic compound with Sn3.0Ag0.05Pt. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



Fig. 15.13 Intermetallic compound with Sn3.0Ag0.05Ge. (a) Top view of IMC after one solder reflow. (b) Cross section of IMC after one solder reflow. (c) Top view of IMC after four solder reflows. (d) Cross section of IMC after four solder reflows



		IMG comparison v after 4 time reflow	vith Sn3.0 Ag processes	IMC change from 1 time to 4 time reflow processes		
Nanoparticle	Wt%	Grain size	Thickness	Grain size	Thickness	
Ni	0.01	Small	Low	Not large	Not large	
	0.03	Small	Low	Small	Small	
	0.05	Small	Low	Small	Small	
Cu	0.1	Same	Same	Large	Large	
	0.3	Same	Same	Large	Large	
	0.5	Same	Same	Large	Large	
	0.7	Same	Large Large			
	1	Same	Same	Large	Large	
Со	0.01	Small	Low	Not large	Not large	
	0.03	Small	Low	Small	Small	
In	0.1	Same	Same	Large	Large	
	0.2	Same	Same	Large	Large	
	0.3	Same	Same	Large	Large	
Sb	0.1	Same	Same	Large	Large	
	0.3	Same	Same	Large	Large	
	0.5	Same	Same	Large	Large	
Zn	0.05	Same	Same Large		Large	
	0.1	Same	Same	Large	Large	
Р	0.03	Same	Same	Large	Large	
Au	0.1	Same	Same	Large	Large	
Ge	0.05	Same	Same	Large	Large	
Pt	0.05	Small	Low	Small	Small	
Al	0.05	Same	Same	Large	Large	

Table 15.1 Summary of IMC effects of nanoparticle additions to Sn3.0Ag

2.4–3.6:43–64:43–53 and 2.6–3.8:42–48:35–53 for one solder reflow and four solder reflows, respectively.

Figure 15.17 shows the IMC element analysis (wt%) for Sn3.0Ag0.5Sb. (a, b) imply the same as mentioned previously. Unlike nickel, cobalt, and platinum, nano antimony particles were not observed in the IMC.

Based on the results of FE-SEM, Ni, Co, and Pt from the evaluated elements (Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, Au) were dissolved into the IMC and then formed three elements-based IMC.

15.4 Nanoparticle Effects on Solder Ball Hardness

Large solder displacement under drop impact improves drop test performance, since large solder displacement can reduce stress in IMCs. Solder hardness is relative to solder ball displacement, so low solder hardness (soft solder) improves drop test



Fig. 15.14 IMC element analysis (wt%) for Sn3.0Ag0.03Ni. (a) IMC element analysis after one solder reflow. (b) IMC element analysis after four solder reflows





Location	Ni	Cu	Sn	Total
1	3.27	44.54	52.19	100.00
2	3.70	43.54	52.76	100.00
3	4.01	42.76	53.22	100.00
4	2.94	43.97	53.10	100.00
5	2.16	42.10	55.73	100.00
6	2.67	45.03	52.31	100.00
7	·	54.52	45.48	100.00
8	1.26	54.87	43.87	100.00
9	1.58	48.16	50.25	100.00

Fig. 15.15 IMC element analysis (wt%) for Sn3.0Ag0.03Co. (a) IMC element analysis after one solder reflow. (b) IMC element analysis after four solder reflows



b



Location	Co	Cu	Sn	Total
1 (101,130)	2.11	42.75	55.14	100.00
2 (268,127)	1.99	44.53	53.48	100.00
3 (443,122)	2.38	43.58	54.03	100.00
4 (66,142)	2.65	45.01	52.34	100.00
5 (246,142)	1.42	45.88	52.71	100.00
6 (418,140)	2.02	44.82	53.16	100.00
7 (128,160)	0.88	48.13	50.99	100.00
8 (276,159)	0.50	47.99	51.51	100.00
9 (451,157)	1.66	45.36	52.99	100.00

а	1	1.1			
	AA			14.	1.1
	4		5	2 1	3 6
		1			
	Location	Cu	Sn	Pt	Total
	1 (89,120)	46.80	53.20		100.00
	2 (318,127)	43.83	52.48	3.69	100.00
	3 (413,130)	42.95	53.96	3.08	100.00
	4 (89,140)	47.12	50.37	2.52	100.00
	5 (284,137)	53.22	43.74	3.04	100.00
	6 (436,139)	49.33	48.18	2.49	100.00

Fig. 15.16 IMC element analysis (wt%) for Sn3.0Ag0.05Pt. (a) IMC element analysis after one solder reflow. (b) IMC element analysis after four solder reflows





Location	Cu	Sn	Pt	Total
1 (129,105)	43.94	52.18	3.88	100.00
2 (258,102)	43.05	53.45	3.50	100.00
3 (396,87)	43.43	53.09	3.48	100.00
4 (121,115)	46.77	50.49	2.74	100.00
5 (243,112)	46.26	51.06	2.68	100.00
6 (386,107)	44.83	52.52	2.64	100.00
7 (168,119)	61.25	38.75	·	100.00
8 (309,122)	52.98	47.02	·	100.00
9 (416,125)	64.28	35.72		100.00

Fig. 15.17 IMC element analysis (wt%) for Sn3.0Ag0.5Sb. (a) IMC element analysis after one solder reflow. (b) IMC element analysis after four solder reflows

a +	1+4		+2 5 6	
			1	
	Location	Cu	Sn	Total
	1 (37,163)	46.35	53.65	100.00
	2 (264,153)	47.36	52.64	100.00
	3 (376,175)	47.21	52.79	100.00
	4 (67,180)	49.44	50.56	100.00
	5 (261,170)	46.29	53.71	100.00

b

6 (351,187)

49.45



50.55

Location	Cu	Sn	Total
1 (70,90)	46.24	53.76	100.00
2 (268,97)	45.97	54.03	100.00
3 (425,100)	46.31	53.69	100.00
4 (48,100)	45.58	54.42	100.00
5 (263,114)	46.72	53.28	100.00
6 (402,112)	47.34	52.66	100.00
7 (90,120)	47.96	52.04	100.00
8 (260,127)	48.13	51.87	100.00
9 (387,125)	46.63	53.37	100.00

100.00



Fig. 15.18 Solder hardness (Vickers) after nano copper particles (0.01-0.07 wt%) were added to An1.0Ag

performance. Hardness testing was performed to study if nanoparticles increase solder hardness after one solder reflow and two solder reflows followed by $100 \,^{\circ}C$ thermal aging (0 h, 100 h, 200 h).

Figure 15.18 shows solder hardness (Vickers) after nano copper particles (0.01-0.07 wt%) were added to Sn1.0Ag solders. Sn3.0Ag0.05Cu was used as a reference solder. Sn1.0Ag shows lower solder hardness than Sn3.0Ag. Since 0.01-0.07 wt% Cu added to Sn1.0Ag did not increase solder hardness compared to no Cu adding to Sn1.0Ag, it is believed that 0.01-0.07 wt% Cu does not affect solder displacement under drop impact. It can be seen that two solder reflows followed by 100 °C thermal aging decease solder hardness compared to one solder reflow.

Figure 15.19 shows solder hardness (Vickers) after nanoparticles (In, P, Sb, Co, Pt, P, Ni, Zn) were added to Sn1.0Ag solders. Except for Sb and Zn, solder hardness was not affected by nanoparticles. Sb, P, Ni, and Pt show solder hardness was increased after two solder reflows. It seems that solder hardness was increased after 100 °C thermal aging for 100 h. Most of nanoparticles show solder hardness became harder after 200 h, 100 °C thermal aging.

15.5 Fracture in IMCs in High-Impact Pull Test

Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, or Au inclusions in Sn-3Ag-based lead-free solders were evaluated to study if these nanoparticles can reduce the frequency of occurrence of IMC fracture in high-impact pull tests.



Fig. 15.19 Solder hardness (Vickers) after nanoparticles (In, P, Sb, Co, Pt, P, Ni, Zn) were added to Sn1.0Ag solders





Figure 15.20 shows the apparatus for high-impact ball pull testing. A Dage 4000 bond tester was used in this test.

A pull jaw holds a solder ball and subsequently lifts up at 50 mm/sec speed.

Figure 15.21 shows fracture modes after high-impact pull testing. Mode 1 is solder pad fracture. Mode 2 is fracture in solder. Mode 3 is no fracture, with pull jaw slip due to solder deformation. Mode 4 is fracture in the IMCs, which shows a failure (not good - NG) in this test.

Figure 15.22 shows high-impact pull strength and fracture mode before and after 100 °C thermal aging (100 h) for Cu (0–1.0 wt%), Co (0.01–0.03 wt%), or Ni (0.01–0.05 wt%) added to Sn1.0Ag. One should pay attention to the fracture mode rather than fracture strength. As can be seen in the graph, nickel and cobalt show lower frequencies of occurrence of fracture in the IMCs than copper.

Figure 15.23 shows high-impact pull strength and fracture mode before and after 100 °C thermal aging (100 h) for Sb (0.1–0.5 wt%), In (0.1–0.3 wt%), Bi (0.1–0.3 wt %), Ge (0.03 wt%), Al (0.005 wt%), Pt (0.05 wt%), or Zn (0.05–0.1 wt%) added to



Fig. 15.21 Fracture mode



Fig. 15.22 High-impact pull strength and fracture mode before and after 100 °C thermal aging (100 h) for Cu (0–1.0Cu wt%), Co (0.01–0.03 wt%), or Ni (0.01–0.05 wt%) added to Sn1.0Ag

Sn1.0Ag. Platinum also reveals a lower frequency of occurrence of fracture in the IMCs than copper.

Based on the result of fracture mode, it is obvious that nickel, cobalt, and platinum decrease fractures in intermetallic compounds compared to other nanoparticles.

15.6 Nanoparticle Effects on Drop Test Performance

Co, Ni, Pt, Cu, Zn, or Sb inclusions in Sn-1.0Ag-based lead-free solders were evaluated to study if these nanoparticles can improve drop test performance.

Figure 15.24 shows the drop test apparatus (Yoshida-seiki HDST-230). The package was a 12×12 mm BGA, a $30 \times 120 \times 0.8$ mm PCB with a Cu + OSP



Fig. 15.23 High-impact pull strength and fracture mode before and after 100 °C thermal aging (100 h) for Sb (0.1–0.5 wt%), In (0.1–0.3 wt%), Bi (0.1–0.3 wt%), Ge (0.03 wt%), Al (0.005 wt%), Pt (0.05 wt%), or Zn (0.05–0.1 wt%) added to Sn1.0Ag

Fig. 15.24 Drop test apparatus





Fig. 15.26 Drop acceleration

(NSMD Type) pad finish, and a solder paste (Senju M705-GRN360-K2V). The samples were left for 5 days before drop test was carried out. The daisy chain resistance was monitored. When the resistance exceeds 1.5 times initial one, it was counted as a failure.

Figure 15.25 shows the drop test table feature. The PCB was screwed down with a 15cN*m torque, and the package was faced downward.

Figure 15.26 shows the drop test acceleration (1500G in this test).

Figure 15.27 shows a Weibull plot of drop test failure for 0.02Ni, 0.04Ni, 0.02Co, 0.5Sb, 0.1Zn, or 0.05Pt included in Sn1.0Ag0.01Cu and a reference solder (Sn1.0Ag0.01Cu, SAC101) before 100 °C thermal aging (100 h). As can be seen in the graph, Ni, Co, and Pt were very effective for drop test performance. In particular, 0.02Ni, 0.05Pt, and 0.02Co show better drop test performances than 0.04Ni, 0.5Sb, and 0.1Zn.

Figure 15.28 shows a Weibull plot of drop test failures for 0.02Ni, 0.04Ni, 0.02Co, 0.5Sb, 0.1Zn, or 0.05Pt inclusions in Sn1.0Ag0.01Cu and a reference solder (Sn1.0Ag0.01Cu, SAC101) after 100 °C thermal aging (100 h). As with no thermal aging, Ni, Co, and Pt were also very effective for drop test performance. In particular, 0.02Ni, 0.05Pt, and 0.02Co show better drop test performance than 0.04Ni, 0.5Sb, and 0.1Zn.



Fig. 15.27 Weibull plot of drop test failures before 100 °C thermal aging



Fig. 15.28 Weibull plot of drop test failures after 100 °C thermal aging (100 h)

A transition metal like Co, Ni, and Pt located to the left of Cu in the periodic table (Fig. 15.29) did not increase IMC thickness and grain size significantly after the solder reflow process and thermal aging when added to SnAg-based solder alloys. Hence, SnAgX solders show better drop test performance. (X means a transition metal like Co, Ni, and Pt.) On the other hand, a transition metal like Cu, Ag, Au, and Zn, a typical metal like Al and In, or a metalloid like P, Ge, and Sb, located to the right of Cu in the periodic table, when added to SnAg -based solder alloys, show increased IMC thickness and grain size after the solder reflow. Hence, SnAgY solders show poor drop test performance. (Y means Cu, Ag, Au, Zn, Al, In, P, Ge, and Sb).

	Periodic Table																
Na	Mg											A	<u>Si</u>	P	<u>s</u>	<u>CI</u>	<u>Ar</u>
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
K	<u>Ca</u>	<u>Sc</u>	Ti	Ā	<u>Cr</u>	<u>Mn</u>	Fe	<u></u>	N	<u>Cu</u>	Łŋ)Ga	Ge	<u>As</u>	<u>Se</u>	<u>Br</u>	<u>Kr</u>
Rb	<u>Sr</u>	Y	Zr	Nb	Mo	Tc	<u>Ru</u>	<u>Rh</u>	Pd	Ag	Cd	ln	<u>Sn</u>	6ь	Te	Ī	Xe
<u>Cs</u>	Ba	•	Hf	Ta	w	Re	<u>0s</u>	lr	P	A	Hg	п	<u>Рb</u>	<u>Bi</u>	Po	At	Rn

Fig. 15.29 A periodic table and evaluated nanoparticles

15.7 Conclusion

Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, or Au inclusions in Sn-3Ag-based leadfree solders were evaluated to study if these nanoparticles increase IMC thickness and grain size after four times solder reflow. Co, Ni, or Pt inclusions in Sn-3Ag-based lead-free solders did not increase IMC thickness and grain size significantly after four solder reflows. Al, P, Cu, Zn, Ge, Ag, In, Sb, or Au inclusions in Sn-3Ag-based lead-free solders increased IMC thickness and grain size after four solder reflows. IMC element analyses were carried out to study if nanoparticles were dissolved in the IMC after one solder reflow and four solder reflows. Co, Ni, and Pt were dissolved in IMC, which did not increase IMC grain size and thickness significantly after four solder reflows. Al, P, Ge, In, and Sb were not observed in the IMC, which increased IMC grain size and thickness after four solder reflows. Large solder displacement under drop impact improves drop test performance. Since solder hardness is related to solder ball displacement, low solder hardness (soft solder) improves drop test performance. Hence, hardness tests were performed to study if nanoparticles increase solder hardness after one solder reflow and two solder reflows +100 °C thermal aging (0 h, 100 h, 200 h). Sn1.0Ag shows lower solder hardness than Sn3.0Ag. Cu, In, Ni, Co, and Pt did not increase solder hardness. Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, or Au inclusions in Sn-3.0Ag-based lead-free solders were evaluated to study if these nanoparticles can reduce the frequency of occurrence of IMC fracture in high-impact pull tests. Co, Pt, and Ni included in Sn3.0Ag-based lead-free solders show a low frequency of occurrence of IMC fracture compared to Cu, Sb, In, Bi, Ge, Al, and Zn in highimpact pull tests. Co, Ni, Pt, Al, P, Cu, Zn, Ge, Ag, In, Sb, or Au inclusions in Sn-1.0Ag-based lead-free solders were evaluated to study if these nanoparticles can improve drop test performance. Ni, Co, and Pt were very effective for drop test performance.

The addition of a transition metal like Co, Ni, and Pt (located to the left of Cu in the periodic table) to SnAg-based solder alloys did not increase IMC thickness and grain size significantly after the solder reflow process and thermal aging. Hence, these nanoparticles lead to better drop test performance than Cu, Ag, Au, Zn, Al, In, P, Ge, and Sb.

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Chapter 16 Nano-underfills and Potting Compounds for Fine-Pitch Electronics



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16.1 Introduction

Packaging materials undergo dimensional changes under environmental exposure to temperature change. Thermomechanical cyclic loads induce stresses and damage interconnects. Underfills compensate for the mismatch in coefficients of thermal expansion between silicon and the printed circuit board. They have been used as a supplemental restraint mechanism to enhance the reliability for flip-chip devices and chip-scale packages in a wide variety of applications, including portable consumer electronics like cellular phones, laptops, under-the-hood electronics, microwave applications, system in package (SIP), high-end workstations, and several other high-performance applications. Figure 16.1 shows an underfilled flip-chip assembly, with solder interconnects between the silicon chip and the PCB. It surrounds the solder balls. Underfill technology has evolved to meet the demand of decreasing feature size and increasing input/output (I/O) number in the integrated circuit (IC) chip.

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Fig. 16.1 Underfill between silicon and PCB

16.2 Potential of Nano-underfills

Capillary-flow underfills rely on the flow of the underfill into the gap between the bonded die and substrate. This process may be slow and often requires a batch cure after dispense. No-flow underfills are an attractive alternative to the use of capillary-flow underfills, eliminate the need for post-reflow batch cure operation, and reduce production cycle time. Instead, no-flow underfills are cured during the reflow process. In addition, no-flow underfills typically contain a fluxing component, eliminating the need for flux dispensing and cleaning. No-flow underfill adhesives are mostly unfilled or filled with very low filler loading due to interference of fillers with solder joint yield.

Epoxy is a common ingredient used in the underfill material, because of its desirable characteristics like corrosion resistance and good adhesion, in addition to physical and electrical properties. However, epoxies by themselves possess a high coefficient of thermal expansion (CTE) (above 80 ppm/°C), making them unable to meet the very first requirement of a good underfill material. For this reason, the epoxies are filled with filler particles that decrease the CTE of the adhesive. Common filler particles include silica and ceramics. Commercially available epoxies contain micron-sized filler particles. The no-flow underfills are largely unfilled or have very low filler loading because micron-sized filler particles interfere with the solder interconnection process [1, 2]. Low filler loading in no-flow underfills causes the CTE to be higher than capillary-flow underfills.

Nano-silica particles do not settle in an underfill formulation and do not interfere with the solder interconnection process, unlike micron-sized particles. Nano-silica imparts the same modulus enhancement and CTE reduction to adhesives as microsized silica particles. In addition, nano-silica particles can achieve much higher filler particle loading than micron-sized particles without affecting the solder joint resistance, thus providing greater control over underfill properties. Underfill formulation, including volume fraction, and size, distribution, and material properties of the filler particles influence the elastic modulus, coefficient of thermal expansion, and mechanical deformation behavior and determine the thermomechanical reliability of flip-chip devices.

16.3 Nanoparticle Production

Production techniques are mainly classified into four categories including condensation from a vapor [3], chemical synthesis [4], solid-state processes [5], and supercritical fluids [6]. Each of the processes is briefly described below.

16.3.1 Vapor Condensation

This method is used to make metallic and metal oxide ceramic nanoparticles. A solid metal is evaporated followed by rapid condensation to form nano-sized clusters that settle in the form of a powder. Metal can be vaporized using various approaches including the exploding wire technique, vacuum evaporation on running liquids, and chemical vapor deposition.

In the exploding wire technique, an electrical arc is created at the surface of a metal wire with sufficient energy to explode or vaporize clusters of atoms. These clusters condense within an inert gas into nanoscale particles [7]. The vacuum evaporation on running liquids method uses a thin film of a relatively viscous material, an oil, or a polymer, on a rotating drum. A vacuum is maintained in the apparatus, and the desired metal is evaporated or sputtered into vacuum [8]. The chemical vapor deposition (CVD) technique uses both liquid and gas forms of a substance, which are put into a reactor. Depending on several parameters like gas-liquid ratio, the order of gas, liquid addition, heat application duration, different particle shapes, and different sizes can be created [9].

Variation of the medium into which the vapor is released affects the nature and size of the particles. For example, inert gases are used to avoid oxidation when creating metal nanoparticles, and reactive oxygen is used to produce metallic oxide ceramic nanoparticles. The main advantage of this method is low contamination. Particle size is controlled by variation of parameters such as temperature, gas environment, and evaporation rate.

16.3.2 Chemical Synthesis

The most widely used chemical synthesis technique consists of growing nanoparticles in a liquid medium composed of various reactants. Chemical techniques are better than vapor condensation techniques for controlling the final shape of the particles. The final size of the particles is controlled by stopping the process when the desired size is reached or by choosing chemicals that form particles that are stable and stop growing at a certain size [4].

16.3.3 Solid-State Processes

Grinding and milling can be used to create nanoparticles [10]. The milling material, milling time, and atmospheric medium affect resultant nanoparticle properties. Bead mills are used to grind coarse particles into the nanometer range. Bead mills grind suspended solid particles by impact and shearing forces between moving grinding beads. Very-fine-particle-sized grinding media beads, in the range of $70-125 \mu$, are used. This process has a limitation; industrial equipment that can use these small beads on a continuous basis is not well known or well accepted due to the difficulty in handling the small beads, i.e., removing them for the suspension after dispersing the particles or loading and discharging the small beads into the machine.

16.3.4 Supercritical Fluids

Supercritical fluids (SCFs) are used as a medium for metal nanoparticle growth [6]. Supercritical fluid precipitation processes can produce a narrow particle size distribution. A gas becomes a supercritical fluid above a critical point, at a certain temperature (critical temperature, T_c) and pressure (critical pressure, P_c). CO₂ is used because of its relatively mild supercritical conditions ($T_c = 31$ °C, Pc = 73 Bar). CO₂ is also inexpensive, nontoxic, noncorrosive, not explosive, and flammable.

16.4 Surface Modification of Underfills

In order to improve the rheological behavior of the nano-silica composite no-flow underfill, filler surfaces are treated using silane-coupling agents [11]. The nano-sized silica particles may have a high surface area covered by silanol groups. This hydrophilic surface does not process good compatibility with the polymer resin, and therefore the silica cannot be wetted very well by the resin. On the contrary, the silica particles with hydrophilic surface easily adhere to each other through hydrogen bonding and form irregular agglomerations. The agglomerations of the nano-silica can form a network through the whole polymer matrix and occlude liquid polymer in their interparticle voids, thereby affecting the rheology of the composite underfill and giving a significant rise to the viscosity as filler loading increases. The high viscosity of the no-flow underfill not only makes underfill dispensing difficult but prevents the chip from collapsing and forming solder joints during the solder reflow process as well. The presence of filler agglomerations will decrease the maximum filler loading, resulting in an inferior thermal mechanical performance.

In order to decrease the viscosity of underfill and to increase the extent of filler loading, it is therefore necessary to reduce the degree of agglomeration. For nanosized filler, the mechanical mixing and dispersion methods such as high-speed shearing or milling are not effective to break down the agglomerations because the



Fig. 16.2 SEM photographs of nano-silica composite materials [12]. (a) Untreated 30. (b) Treated 30

electrostatic forces holding the particles together are stronger than the shear force created by the velocity gradient. In such circumstances, chemical treatment of nanoparticle surface is necessary to achieve better compatibility and dispersion of the filler in epoxy resin.

Silane-coupling agents are often used to treat the silica filler due to their unique bifunctional structure with one end capable of reacting with the silanol groups on silica surface and the other end compatible with the polymer. The modification process is described as a hydrolysis and condensation reaction between the silane-coupling agents and the silica surface in a polar medium. The bonding between the silane and the silica surface removes the surface silanol groups and changes the hydrophilic surface into a hydrophobic surface. Figure 16.2 shows the ideal result of surface treatment is to reduce the filler-filler interaction and to achieve the homogenous distribution of the nano-sized silica in the polymer. Figure 16.2a shows that the nano-silica without silane treatment formed large agglomerations, and Fig. 16.2b shows the nano-silica after silane treatment.

16.5 Computational Techniques for Property Design

Property prediction techniques for formulation of the underfills with desirable thermomechanical characteristics can significantly impact the reliability of finepitch assemblies. In this section, reliability of nano-silica underfills and methodologies for property prediction are discussed, and models are presented for the prediction of underfill properties [13, 14]. The models are based on constituent component properties and enable the prediction of effective equivalent properties of statistically isotropic composites formed by random distribution of spherical filler particles. Drugan [15, 16] showed that the representative volume element (RVE) is an effective technique for prediction of elastic composites. Segurado [17] also demonstrated the RVE with a modified random sequential adsorption (RSA) algorithm as a reliable approach to estimate the equivalent properties. Lall [13, 14] used an algorithm similar to the RSA algorithm to generate statistically isotropic cubic unit cells of underfill containing up to 38% nano-fillers. Developed unit cell has been analyzed, and the elastic modulus and CTE of the underfill are computed by using RVE implementation in implicit finite elements.

16.5.1 Unit Cell Generation

The modulus of elasticity and the CTE of nano-underfills can be predicted by the implicit finite element models of three-dimensional cubic unit cells. The unit cell is generated by randomly distributing spherical fillers in an epoxy matrix. The volume of the cube is L^3 , N is the total number of particles, and r is the radius of the spherical particle. Volume fraction (γ) of the filler is determined as the ratio of total volume of the sphere to the volume of the cube:

$$\gamma = \frac{N\left(\frac{\pi}{4}r^3\right)}{L^3} \tag{16.1}$$

The volume fraction of the cube is controlled by varying the total sphere number N as required by the value of L. The radius of the sphere r is kept the same for the analysis of all volume fractions. The fillers should be distributed in such way that the unit cell should be isotropic, i.e., equivalent in all directions, and it should be quite suitable for generating a good finite element mesh. An algorithm based on modified RSA adsorption can be used to generate the random center coordinates of the nanosilica particles in the underfill [17]. According to this algorithm, all the accepted random coordinates of the particles (for $\gamma = 0-0.25$) pass the following conditions. (a) If the particle surface touches the surface of the cube, or if they are very close, it may not be possible to mesh, or the generated finite element mesh will be distorted, or some time meshing may not be possible at all. To avoid these, the particles are kept inside of the cube at some minimum distance d_2 from the surface of the cube:

$$d_2 = r + 0.1r \tag{16.2}$$

To fulfill the above condition, center coordinates of the ith particle must pass the following check:

$$\begin{aligned} x^i_j &\geq d_2 \qquad \quad j=1,2,3 \\ \left|x^i_j - L\right| &\geq d_2 \quad j=1,2,3 \end{aligned} \tag{16.3}$$

(b) If two adjacent particles overlap each other, they will violate the rigid sphere condition. In addition, two adjacent particles cannot touch each other. To fulfill this condition, center coordinates of the ith particle must pass the following check:

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$$d_1 = 2.07^* r \tag{16.4}$$

$$\left\| \left(\vec{x}^{\,i} - \vec{x}^{\,k} \right) \right\| \ge d_1 \qquad \quad k = 1, \dots, (i-1) \tag{16.5}$$

The modified RSA method has been used to achieve volume fraction higher than $\gamma = 0.25$. For the unit cells with volume fraction, γ , such that $0 < \gamma < 0.25$, all the particle centers are kept inside the cube, and no particle overlaps the outer surfaces of the cube. For unit cell volume fractions more than 0.25, the particles are allowed to overlap the surface boundary of the cube. If any particle overlaps the surface, the portion of the particle outside the cube is carefully cut into several sections and copied at a suitable position on the opposite surface of the cube. First, a cubic cell with volume fraction less than 0.25 is generated by fulfilling the above two conditions, and then the cell is compressed into a smaller size while keeping the size of the sphere do not change during the operation, but the cell is compressed, giving a higher volume fraction of filler content. The length of the cubic cell is compressed first, by multiplying it by a user-defined shrinking factor c_f (<1). The new length of the cube is given by

$$L_n = c_f^* L \tag{16.6}$$

If the old position of the center of the ith particle is given by \vec{x}^i , then the new position of the particle \vec{x}_n^i will be given by

$$\vec{\mathbf{x}}_{\mathrm{n}}^{\mathrm{i}} = \vec{\mathbf{x}}^{\mathrm{i}*} \mathbf{c}_{\mathrm{f}} \tag{16.7}$$

Once the particles have moved, they will be allowed to overlap the surface of the cube, but no particle center will be outside of the cube. If the new coordinates of the i th particle \vec{x}_n^i fall outside of the cube, then it is moved back in the cube at a random position between the surface and at an inward distance $(r-\alpha)$, where α is a user-defined constant and $\alpha > 0.1r$. If the particle center sits at a distance r from the surface of the cube, then the particle surface will touch the cube surface, and meshing will not be possible. If the particle overlaps any other previously accepted position, then it will be moved to a new random position in a random direction. The new position will be given by

$$\vec{\mathbf{x}}_{n}^{i} = \vec{\mathbf{x}}_{n}^{i} \pm \beta \tag{16.8}$$

where β is a small random number. Smaller β ensures faster convergence. The new position of the particle will be accepted only if all above conditions are fulfilled. Since the algorithm involves random movement and random positioning, each of the iterations may not produce an acceptable distribution. The algorithm also counts the number of iterations and stops the program if the number of iterations exceeds a certain number.



Fig. 16.3 Centroids for acceptable nanoparticle distribution

	Moment of inertia	Moment of inertia	Moment of inertia
Volume fraction	About axis 1	About axis 2	About axis 3
0.10	100105.25	85311.77	86064.94
0.20	208298.14	195363.03	210952.10
0.25	278355.74	259266.68	254355.15
0.38	168768.24	179810.48	186470.79

Table 16.1 Moment of inertia of acceptable nanoparticle distributions

16.5.2 Isotropy of the Unit Cell

Once a valid distribution of the filler particles has been created, the algorithm also calculates the centroid and moment of inertia of the distributed particles. These quantities are calculated to check the isotropy of the distribution. The distribution with centroids at positions in the neighborhood of 0.5 L is accepted. An isotropic distribution will have identical moment of inertia for the nanoparticles about three orthogonal axes. Figure 16.3 shows a plot of the coordinates of the centroids of the accepted distribution for different volume fractions. Table 16.1 shows the values of moment of inertia for the accepted distributions for several volume fractions. In almost all cases, moments of inertia about all three axes have very close values. This indicates that the generated unit cell is isotropic in all directions.

16.5.3 Randomness of Filler Distribution

The radial distribution function describes on average the presence of the filler particles around an arbitrary particle. To calculate the radial distribution function, series of concentric spheres are drawn around an arbitrary particle at a small fixed



Fig. 16.4 Plot of radial distribution function

interval Δr apart. Randomness of filler distribution can be used to ensure that no periodicity exists in the filler distribution. A radial distribution function of filler centroids, g(R), is used for this purpose [18]. The function is given as

$$g(\mathbf{r}) = \frac{\mathbf{n}(\mathbf{r})}{\rho 4\pi r^2 \ \Delta r} \tag{16.9}$$

where g(r) is the radial distribution function, n(r) is the mean number of particles in a shell of width Δr at distance r, and ρ is the mean atom density. Figure 16.4 shows a plot of g(R) for a distribution of filler volume fraction 0.20. The distributions are not periodic as very little presence of spikes of maxima and minima is seen.

16.6 Finite Element (FE) Model of Unit Cell

Lall [13, 14] created FE models of the cubic unit cells to predict the CTE and elastic modulus of the nano-underfill. In these models, spherical silica fillers are generated in an epoxy cube. The length of the epoxy cube is equal to the length of the unit cell considered in the unit cell algorithm. The filler particles are generated by using the center coordinates and radius. For the models having volume fraction of filler more than 0.25, fillers overlapping the cube surface are carefully cut into pieces and copied at a suitable place onto the other side of the cube. The model geometry is meshed by an 8-node tetrahedral brick element. Figures 16.5, 16.6, and 16.7 show representative models of the unit cell and filler distribution. Figure 16.8 shows an example of the mesh generated in the FE analysis (FEA) models. Figure 16.9 shows the isotropic distribution of particles with volume fraction, $\gamma = 0.38$. Table 16.2 shows the material properties of the filler and epoxy matrix.



filler distribution, $\gamma = 0.20$

Fig. 16.6 Front view of

16.7 Prediction of Coefficient of Thermal Expansion (CTE)

FE models can be used to predict the CTE of the nano-underfill for different volume fractions of filler particles. Symmetric boundary conditions are used at the cube faces at x, y, and z equal to zero. The degrees of freedom are coupled at the faces at x, y, z









equal to L. The temperature of the model is raised to a user-defined uniform temperature. This ensures that the cube faces will not be distorted after deformation. Calculated CTE values are presented in Fig. 16.10. The CTECoefficient of thermal expansion (CTE) of the underfill decreases linearly with the increase of volume fraction of the filler particles. Figure 16.10 shows predicted and experimental CTE values in x-, y-, z-directions together on the same graph. This graph shows that CTE
Fig. 16.9 Isotropic view of filler distribution, $\gamma = 0.38$



Table 16.2 Material properties for epoxy matrix and nano-silica particle

	Elastic modulus (GPa)	Poisson ratio	CTE (ppm/°C)
Filler	77.8	0.19	0.5
Epoxy	2.5	0.40	62.46



Fig. 16.10 Prediction of x, y, z CTE by finite element analysis of unit cell



Fig. 16.11 Prediction of elastic modulus by FEA analysis of unit cell

in all directions is almost identical which once again proves that the generated unit cells are isotropic.

16.8 Prediction of Elastic Modulus

In this section, elastic modulus prediction of nano-underfill for different volume fractions is presented. For this analysis, different boundary conditions than the CTE models are used. Displacement in the x-direction is zero at the cube surface at x equal to zero. A fixed boundary condition is applied at one of the points at the mid-position of the surface at x equal to zero. Tensile load is applied at the surface at x equal to L in the form of uniform pressure. A suitable small value of the pressure load will give better results because the modulus is defined as the initial slope of the linear part of stress-strain curves. Figure 16.11 shows the elastic modulus vs. volume fraction of filler particle. Elastic modulus increases exponentially with the increase of volume fraction of the filler particles.

16.9 Prediction of Bulk Modulus

In this section, nano-underfill bulk modulus calculations by finite element analysis of the above unit cell are discussed. A fixed boundary condition is applied on the node at the origin. The origin is located at one corner of the unit cell. The x, y, and z deflections are kept zero on the surfaces located at x = 0, y = 0, and z = 0,



Fig. 16.12 Prediction of bulk modulus by FE analysis of unit cell

respectively. A uniform tensile loading in the form of hydrostatic pressure is applied on the surfaces located at x = L, y = L, and z = L, respectively. The degrees of freedom are coupled in the corresponding directions at x = L, y = L, and z = L, respectively. The loading causes an increase in the volume of the cube without changing the shape at all. Since the unit cells are isotropic, it generated a uniform change in length in all directions. Bulk modulus values are calculated by using the following formula:

$$\mathbf{k} = \frac{\mathbf{\sigma}}{\frac{\Delta V}{V}} \tag{16.10}$$

where k = bulk modulus, σ = value of applied hydrostatic stress, V = original volume, and ΔV = change in volume. The analysis has been performed for unit cells with γ = 0, 0.1, 0.2, 0.25, and 0.39. Figure 16.12 shows the predicted bulk modulus as a function of volume fraction of the filler particle. In this case, the bulk modulus of the epoxy without any filler is 4.16 GPa, and it increases monotonically with increased volume fraction of the filler particles.

16.10 Prediction of Poisson's Ratio

The unit cell approach has been used to predict the Poisson's ratio of the nanounderfill, and quantify the lateral deformation of the underfill under stress. Displacement in the x-direction is zero at the cube surface at x equal to zero. A fixed boundary condition is applied at one of the points at the mid-position of the surface at x equal to zero. Tensile load is applied on the surface at x equal to L in the form of uniform



Fig. 16.13 Prediction of Poisson's ratio of nano-underfill by FE analysis of unit cell

pressure. Nodal degrees of freedom on surfaces at y = 0 and L and z = 0 and L are coupled at corresponding directions. Loading causes extension in the x-direction and contraction in three y- and z-directions. Poisson's ratio is calculated by using the extension and contraction values. Figure 16.13 shows that Poisson's ratio decreases nonlinearly with increase of filler volume fraction.

16.11 Viscoelastic Model for Nano-underfills

Underfills exhibit time-dependent, strain-rate-dependent deformation response under thermomechanical loading. Nano-underfills are viscoelastic materials, which exhibit instantaneous elasticity, creep and recovery, stress relaxation, strain-rate dependence, and delayed recovery. Silica nanoparticles used in underfills exhibit linear elastic behavior. The viscoelastic property of the epoxy matrix is responsible for the time-dependent behavior of underfill.

Combination of Maxwell and Kelvin models has been used to represent viscoelastic material behavior in nano-underfills. The Maxwell model includes a linear spring element and a linear viscous dashpot element connected in series. Kelvin models include a linear spring and a linear dashpot connected in parallel. Generalized-parallel Maxwell models and generalized-series Kelvin models have been used, since they are capable of representing instantaneous elasticity, delayed elasticity with various retardation times, and stress relaxation with various relaxation times in addition to viscous flow. The generalized-parallel Maxwell model is better suited in cases where the strain history is prescribed since same prescribed strain is applied to each individual element, and also resulting stress is the sum of the individual contributions. The generalized-series Kelvin model is more convenient for viscoelastic analysis in cases where the stress history prescribed since same prescribed stress is applied to each individual element, and the resulting strain is the sum of the individual strain in each element. A generalized-series Maxwell model formed by connecting several Maxwell elements in series is capable of exhibiting behavior equivalent to a single Maxwell element. Similarly, a generalized-parallel Kelvin model is capable of exhibiting behavior equivalent to a single-element Kelvin model.

16.12 Input Constants for Viscoelastic Material Models

The finite element analysis software ANSYS[™] has been used to compute the predicted time-dependent behavior of the developed unit cell model. The nanounderfill material has been modeled using the Williams-Landel-Ferry (WLF) shift function constants and Prony series constants of volumetric and shear response. WLF shift functions have been calculated from the elastic modulus relaxation data and time-temperature superposition method.

Figure 16.14 shows the stress relaxation data used in calculation of the viscoelastic constants. Figure 16.15 shows the log-log plot of the temperature-dependent relaxation modulus versus time data obtained from the data shown in Fig. 16.14. The curve at 25 °C is taken as the reference curve, and other curves at 75, 100, and 125 °C are shifted sideways parallel to the time axis to an appropriate distance, and the single master stress relaxation curve shown in Fig. 16.16 is formed. The magnitude of the total shift for each curve has been plotted against temperature and is given in Fig. 16.17. WLF constants are calculated by substituting the temperature-dependent shift function a_T and temperature value into Eq. 16.11 and then performing nonlinear regression of that equation. Equation 16.11 was originally proposed by Williams, Landel, and Ferry and gives the relation between the shift



Fig. 16.14 Stress relaxation data used for calculating viscoelastic constants (strain level 1%)



Fig. 16.15 Log-log plot of the relaxation modulus versus time data



Fig. 16.16 Master relaxation modulus at 25 °C

factor and the temperature. Calculated WLF constants for the nano-underfill studied are $C_1 = T_0 = 25$ °C, $C_2 = -42.6$, and $C_4 = 517$ °C:

$$Log(a_{T}) = \frac{-C_{2}(T - T_{o})}{C_{4} + T - T_{o}}$$
(16.11)

Viscoelastic constants to represent volumetric response and shear response are calculated by using Prony series. A Prony series is derived from the solution of the generalized Maxwell model in parallel. The stress-strain relation of spring and dashpot can be represented as



Fig. 16.17 Temperature-dependent shift factor

$$\sigma = k\varepsilon_2 \tag{16.12}$$

$$\sigma = \eta \dot{\varepsilon}_1 \tag{16.13}$$

Total strain:

$$\varepsilon = \varepsilon_1 + \varepsilon_2 \tag{16.14}$$

Strain rate:

$$\dot{\epsilon} = \dot{\epsilon}_1 + \dot{\epsilon}_2$$
 (16.15)

Inserting Eq. 16.13 and time derivative of Eq. 16.12 in Eq. 16.15 will give

$$\dot{\varepsilon} = \frac{\dot{\sigma}}{k} + \frac{\sigma}{\eta} \tag{16.16}$$

or

$$\frac{d\varepsilon}{dt} = \frac{1}{k}\frac{d\sigma}{dt} + \frac{\sigma}{\eta}$$
(16.17)

Taking the Laplace transform of Eq. 16.17,

$$s\widehat{\epsilon}(s) - \epsilon(0) = \frac{1}{k}[s\widehat{\sigma}(s) - \sigma(0)] + \frac{\widehat{\sigma}(s)}{\eta}$$

Since $\varepsilon(0) = \sigma(0) = 0$,

$$s\widehat{\epsilon}(s) = \frac{1}{k}[s\widehat{\sigma}(s)] + \frac{\widehat{\sigma}(s)}{\eta}$$

Rearranging gives

$$\widehat{\sigma}(s) = \frac{ks}{s + \frac{k}{\eta}} \widehat{\varepsilon}(s)$$
(16.18)

Assuming applied strain is a step function and

$$\varepsilon(t) = \varepsilon_0 H(t)$$

then,

$$\widehat{\epsilon}(s) = \epsilon_0 \frac{1}{s}$$

$$\widehat{\sigma}(s) = \frac{ks}{s + \frac{k}{\eta}} \frac{\varepsilon_0}{s}$$

or

$$\widehat{\sigma}(s) = \frac{k\varepsilon_0}{s + \frac{k}{n}}$$
(16.19)

Taking the inverse Laplace transform of Eq. 16.19 gives

$$\sigma(t) = k\varepsilon_0 \ \exp\left(-\frac{k}{\eta}t\right)$$

Assuming $\tau = \frac{\eta}{k}$ gives

$$\sigma(t) = k\varepsilon_0 \, \exp\left(-\frac{t}{\tau}\right) \tag{16.20}$$

For the generalized Maxwell model, several Maxwell elements are connected in parallel as shown in Fig. 16.18. Since the Maxwell elements are in parallel, the stress relaxation response will be obtained by summing the stress relaxation responses of the individual elements. For the combination:

$$\sigma(t) = \varepsilon_0 \sum_{i=1}^{N} k_i exp\left(-\frac{t}{\tau_i}\right)$$
(16.21)



Prony series representation of the elastic modulus can be obtained by dividing the stress response equation by applied constant strain. The derived Prony series will have the following form:

$$E(t) = \sum_{i=1}^{N} k_i exp\left(-\frac{t}{\tau_i}\right)$$
(16.22)

A generalized-parallel Maxwell model with a free spring modulus k_{∞} , connected in parallel (Fig. 16.18), will give the modulus relaxation response to a constant strain ϵ_0 as shown in Eq. 16.23:

$$E(t) = k_{\infty} + \sum_{i=1}^{N} k_i exp\left(-\frac{t}{\tau_i}\right)$$
(16.23)

Denoting k's by E's will give

$$E(t) = E_{\infty} + \sum_{i=1}^{N} E_i exp\left(-\frac{t}{\tau_i}\right)$$
(16.24)

ANSYSTM allows a maximum of ten Maxwell elements to approximate the relaxation function. Equations 16.25 and 16.26 are used to approximate the relaxations of the shear modulus and bulk modulus:

$$G(t) = G_{\infty} + \sum_{i=1}^{n_{G}} G_{i} exp\left(-\frac{t}{\tau_{i}^{G}}\right)$$
(16.25)

$$k(t) = k_{\infty} + \sum_{i=1}^{n_k} k_i exp\left(-\frac{t}{\tau_i^k}\right)$$
(16.26)

where

$$\begin{split} G_\infty &= \text{final shear modulus (GPa)} \\ k_\infty &= \text{final bulk modulus (GPa)} \\ n_G &= \text{number of Maxwell elements to approximate G relaxation} \end{split}$$

Table 16.3 Prony		25 °C	75 °C	100 °C	125 °C
viscoelastic shear response	G ₁	0.0059	0.0208	0.1269	0.0215
	τ_1^G	9.39	17.55	0.9385	2.92
	G_2	0.0196	0.0278	0.0256	0.1146
	$ au_2^{ m G}$	10.91	35.43	13.91	0.3227
	G ₃	0.0646	0.0887	0.0374	0.0396
	$ au_3^{ m G}$	1.09	1.60	12.85	23.02
	G_4	0.0195	0.0294	0.0376	0.0212
	$ au_4^{ m G}$	12.12	32.07	12.85	2.94
	G ₅	0.018	0.0298	0.0093	0.0188
	τ_5^G	32.23	34.81	66.02	2.73
Table 16.4 Prony		25 °C	75 °C	100 °C	125 °C
Table 16.4 Prony		25 °C	75 °C	100 °C	125 °C
response	k ₁	0.0972	0.0922	0.1148	0.07078
	τ_1^k	16.09	31.15	13.24	2.84
	k ₂	0.0543	0.0804	0.4311	0.1345
	$ au_2^k$	16.12	31.15	0.9412	23.06
	k ₃	0.2078	0.0922	0.1146	0.0709
	$ au_3^k$	1.24	31.15	13.24	2.84
	\mathbf{k}_4	0.021	0.0919	0.1132	0.0679
	$ au_4^k$	1.27	31.15	13.21	2.93
	k 5	0.0429	0.3049	0.0288	0.3894
	τ_5^k	16.03	1.71	58.52	0.3223

 n_k = number of Maxwell elements to approximate k relaxation τ_i^G and τ_i^k = relaxation time for each Prony component (min)

For the present study, a total of five Maxwell elements are considered. Temperature-dependent Prony constants have been calculated by the nonlinear regression of Eqs. 16.24 and 16.25. Calculated Prony series constants are given in Tables 16.3 and 16.4 [19].

16.13 Material Property Measurement

A MT-200 tension/torsion thermomechanical test system from Wisdom Technology, Inc., has been used to test the samples in this study. The system provides an axial displacement resolution of 0.1 μ and a rotation resolution of 0.001°. Testing can be performed in tension, shear, torsion, and bending and in combinations of these loadings, on small specimens such as thin films, solder joints, gold wire, fibers, etc. Cyclic (fatigue) testing can also be performed at frequencies up to 5 Hz. In addition, a universal 6-axis load cell is utilized to simultaneously monitor three forces and three moments/torques during sample mounting and testing. An environmental chamber provides a temperature range capability of approximately -50 to 300 °C. For uniaxial testing with the MT-200, forces and displacements are measured. The axial stress and axial strain are calculated from the applied force and measured cross-head displacement using

$$\sigma = \frac{F}{A} \qquad \qquad \varepsilon = \frac{\Delta L}{L} = \frac{\delta}{L} \qquad (16.27)$$

where σ is the uniaxial stress, ε is the uniaxial strain, F is the measured uniaxial force, A is the original cross-sectional area, δ is the measured cross-head displacement, and L is the specimen gage length (initial length between the grips).

16.14 Uniaxial Testing

In this section, uniaxial testing specimens of the nano-underfill are discussed. The specimen preparation procedure is presented in Islam (2004). With the developed test specimen, tensile, creep, and relaxation tests have been performed for a wide temperature range. The nano-underfill material for detailed material testing is NUF1, which has a cure time of 30 min at 150 °C. The NUF1 underfill has a volume fraction in the neighborhood of $\gamma = 0.22$. The glass transition temperature of this material is 156 °C by the dynamic mechanical analysis (DMA) method. The thickness of the cured uniaxial specimen is 75–125 µm (3–5 mil). The typical length and width of a specimen are 90 mm and 3 mm, respectively. In all uniaxial tests, the effective test length of the uniaxial specimen is 60 mm.

16.14.1 Stress-Strain Data

Figure 16.19 shows typical stress-strain curves for underfill NUF1 at 50 °C and a strain rate of $\dot{\varepsilon} = 0.001 \text{ s}^{-1}$. The observed variation in the data between different tests is typical for cured polymeric materials. The elastic modulus E is the slope of the initial linear portion of the stress-strain curves. At 50 °C and $\dot{\varepsilon} = 0.001 \text{ s}^{-1}$, the value for this underfill is measured to be E = 3.74 GPa. This value is found by averaging the results from five tests. An empirical three-parameter hyperbolic tangent model has been used to model the observed nonlinear underfill stress-strain data. Such a model has been used historically to model the stress-strain curves of cellulosic materials [20, 21]. The general representation of the hyperbolic tangent empirical relation is

$$\sigma(\varepsilon) = C_1 \tanh(C_2\varepsilon) + C_3\varepsilon \tag{16.28}$$



Fig. 16.19 Hyperbolic tangent model fit to typical underfill stress-strain data (T = 50 °C, $\dot{\epsilon} = 0.001 \text{ s}^{-1}$)

where C_1 , C_2 , and C_3 are material constants. Differentiation of Eq. 16.28 gives an expression for the initial (zero strain) elastic modulus:

$$\mathbf{E} = \mathbf{C}_1 \mathbf{C}_2 + \mathbf{C}_3 \tag{16.29}$$

Likewise, constant C_3 represents the limiting slope of the stress-strain curve at high strains. For a given set of experimental data, constants C_1 , C_2 , and C_3 are determined by performing a nonlinear regression analysis of Eq. (16.28) through experimental data points. Based on the results from reference [21], the data from all of the stress-strain curves in a set should be fit simultaneously in order to obtain the best set of hyperbolic tangent model material constants.

The stress-strain data shown in Fig. 16.19 has been fitted with the hyperbolic tangent model using a nonlinear regression analysis. Results from this calculation are $C_1 = 53.60$ MPa, $C_2 = 68.67$, and $C_3 = 10.68$ MPa. Excellent correlation is observed. Such results are typical for all of temperatures at which testing has been performed. Typical variation of the stress-strain curves of the tested nano-underfills NUF1 (20% volume fraction) and NUF2 (10% volume fraction) w.r.t. temperature is shown in Figs. 16.20 and 16.21. The strain rate for these tests is $\dot{\varepsilon} = 0.001 \text{ s}^{-1}$. The total test time (to failure) of a typical tensile test is less than 5 s for room temperature experiments. Tests have been performed at T = 25, 50, 75, 100, 125, and 150 °C. The curves shown in Fig. 16.20 are the hyperbolic tangent empirical fits to the multiple curves measured at each temperature and therefore represent an average measured stress-strain curve at each temperature. The stress-strain curves in Fig. 16.20 illustrate considerable softening and viscoplastic-type behavior as the temperature is increased.



Fig. 16.20 Temperature-dependent average stress-strain curves of underfill NUF1 ($\dot{\epsilon} = 0.001 \text{ s}^{-1}$)



Fig. 16.21 Temperature-dependent stress-strain curves for nano-underfill NUF2 ($\dot{\epsilon} = 0.001 \text{ s}^{-1}$)

Elastic modulus decreases approximately linearly with the increase of temperature from 25 to 125 °C. Figure 16.22 shows temperature-dependent elastic modulus of underfill NUF1. The value of elastic modulus at 25 °C is in the neighborhood of 4.65 GPa. This correlates well with the predicted value of 4.4 GPa from the unit cell



Fig. 16.22 Elastic modulus of a nano-filler underfill (NUF1, volume fraction = 0.22) and a micro filler underfill ($\dot{\varepsilon} = 0.001 \text{ s}^{-1}$)

model (Fig. 16.11). For temperature T = 125 °C, elastic modulus decreases dramatically, and at T = 150 °C, elastic modulus is almost near to zero. This is typical as underfill approaches near to its glass transition temperature. Figure 16.22 shows a comparison of elastic modulus of the nano-underfill NUF1 versus micron-filler underfill UF1. UF1 is has micro-sized particles as fillers. The volume fraction of filler particle in UF1 is almost double than NUF1. Figure 16.22 shows that due to higher filler concentration, UF1 has higher elastic modulus than NUF1. The glass transition temperature (T_g) of UF1 is 150 °C, and its modulus drops greatly after 100 °C, but NUF1 has glass transition temperature at 156 °C, and its modulus drops greatly after 125 °C.

Measurement of accurate mechanical properties at extreme low temperatures is very important for various applications including the solar system exploration missions by NASA. In this present study, tests have been performed at very extreme low temperatures down to -175 °C. A newly developed environmental chamber is used with the MT-200 testing system for this purpose. Figure 16.23 shows stress-strain curves at -50, -100 and -175 °C. The measured data have been plotted together with the room temperature and higher stress-strain curves shown earlier in Fig. 16.20. The test data shows that underfill NUF1 becomes more linearly elastic as the temperature decreases to cryogenic temperature. Figure 16.24 shows the elastic modulus of underfill NUF1 at extreme low temperatures. The elastic modulus also increases linearly with decrease in temperature from the room temperature to negative temperatures. At -175 °C, elastic modulus of NUF1 became almost double than the room temperature value.



Fig. 16.23 Temperature-dependent stress-strain curves at extreme low temperatures ($\dot{\epsilon} = 0.001 \text{ s}^{-1}$)



Fig. 16.24 Temperature-dependent elastic modulus in cryogenic temperatures ($\dot{\epsilon} = 0.001 \text{ s}^{-1}$)

16.14.2 Creep Data

Creep curves for the underfills NUF1 and NUF2 are shown in Figs. 16.25 and 16.26. All the tests have been performed at a constant stress level of 10 MPa. Both underfills show strong influence of temperature upon the deformation under constant load.



Fig. 16.25 Temperature-dependent creep data of NUF1



Fig. 16.26 Temperature-dependent creep data of NUF2

At temperatures near T_g , the creep compliance is greatly increased. The micro-underfill (UF1, 22% volume fraction) with comparable volume fraction to the nano-underfill (NUF1, 20% volume fraction) shows greater creep compliance (Fig. 16.27).



Fig. 16.27 Temperature-dependent creep data of UF1



Fig. 16.28 Temperature-dependent stress relaxation test data of underfill NUF1

16.14.3 Preliminary Relaxation Data

Preliminary stress relaxation test curves for the underfill NUF1 are shown in Fig. 16.28. All the tests are performed for a constant strain level, which is 1% in this case. From test data, it is observed that the stress relaxation rate increases with the increase of temperature. All the tests were stopped after 100 min as it almost reaches to a very smaller rate of change of stress after this time.

16.15 Correlation of Stress Relaxation Behavior

The predicted relaxation behaviors of 10 percent volume fraction (NUF2) and 20 percent volume fraction (NUF1) underfills have been correlated with experimental data. A fixed boundary condition is applied at mid-side nodes of the y equal to zero surface. The y-displacement has been set to zero on the cube surface at y equal to zero. Tensile loading is applied at the surface at y equal to L in the form of uniform nodal displacement. Step displacement loading is chosen instead of ramp loading to make sure of instantaneous application of strain. The value of applied instantaneous strain is 1%, and it has been kept constant throughout the solution.

Nano-filler particles have been modeled as linear elastic. Viscoelastic material behavior of the generalized-parallel Maxwell model is applied for the epoxy matrix. In order to represent the viscoelastic properties of epoxy, WLF constant data, Prony viscoelastic shear response data, and Prony viscoelastic volumetric response data of epoxy have been used. During the stress relaxation test, the stress-strain value starts from zero and ramps up to the applied strain level before undergoing stress relaxation. The instantaneous modulus continuously decreases with relaxation to a value significantly lower than the initial elastic modulus. In the calculation of Prony constants, the initial ramping of stress-strain is ignored, and instantaneous strain-stress is assumed to be applied at time equal to zero.

The elastic modulus value of the epoxy is 2.5 GPa, measured from the initial slope of the stress-strain curve of a tensile test. The above elastic modulus value may not be appropriate for viscoelastic analysis, since the applied strain loading is instantaneous. Use of the initial elastic modulus value may considerably overpredict the relaxation behavior of the underfill. Instantaneous value at the start of stress relaxation has been used for analysis. In this case, a value of 1.84 GPa has been used for analysis. Nonlinear solutions have been performed in this case with several time sub-steps. The nodal stress response of the surface at y = L has been computed and plotted in Fig. 16.29. The predicted value for both the 10% and 20% volume fraction nano-underfill correlates well with the experimentally measured relaxation behavior.

16.16 CTE Measurement

The underfill CTE is the most critical thermomechanical property of underfill. Accurate measurement of the CTE of the cured underfill is challenging. In this section, a strain gage method has been applied to measure the CTE of cured underfill. The strain gage technique is a very accurate method for CTE measurement [22]. Hence, the specimen for this method should be very stiff, and in this case, much thicker underfill specimens than uniaxial test specimens are used. A $25 \times 15 \times 1$ mm specimen has been cast and cured at 150 °C for 30 min.



Fig. 16.29 Prediction of elastic modulus relaxation for NUF1 and NUF2 nano-underfills



Fig. 16.30 Strain gage reading from the gage on the reference material

A strain gage is then placed on the cured specimen. A special type of CTE measurement strain gage is chosen for this purpose. A similar strain gage is placed on a reference material. The reference material is a titanium-silicate bar (TSB) specially made for use in CTE measurements. The underfill specimen and the TSB are heated in an oven from room temperature to 120 °C, less than T_g of the underfill, NUF1. Figures 16.30 and 16.31 show the strain gage readings at different



Fig. 16.31 Strain gage reading from the gage on the test specimen

temperatures for the gages placed on the reference material and underfill specimen, respectively. The CTE is calculated by using the following equation [22]:

$$\alpha_{\rm S} - \alpha_{\rm R} = \frac{\varepsilon_{\rm S} - \varepsilon_{\rm R}}{\Delta T} \tag{16.33}$$

where α_S and α_R are CTE of the test specimen and reference material, respectively. ε_S and ε_R are strain gage output of the gages on the test specimen and the reference material, respectively, and ΔT is temperature difference. The calculated value of the CTE of the underfill NUF1 is 39 ppm/°C, which correlates reasonably with the predicted CTE value of 45 ppm/°C from the unit cell model (Fig. 16.10).

16.17 Thermal Shock Reliability Testing

Thermal shock testing of PB8 boards has been performed in a liquid-to-liquid thermal shock chamber. The chips were underfilled with NUF1. The duration of one complete cycle is 12 min. To complete a cycle, test boards are kept immersed for 5 min alternately in a cold and a hot bath with extreme temperatures (-55 to $125 \,^{\circ}C$ or -55 to $150 \,^{\circ}C$) and 1 min holding time in between. Figures 16.32 and 16.33 show the filler distribution in nano-filler and micron-filler underfills. Thermal shock results data are discussed below.

Fig. 16.32 Cross section of flip-chip device assembled with nano-silica underfill. The top edge of the dark gray area indicates the dieto-underfill edge



Fig. 16.33 Cross section of flip-chip device assembled with micron-underfill

16.17.1 Test Results and Failure Mechanism (Eutectic Solder)

The temperature range is from -55 to 125 °C. The die is PB8 (5.08×5.08 mm) perimeter bumped flip chip with 88 bumps total. The pitch is 0.203 mm. The ball diameter is 0.127 mm. The solder alloy is 37Sn63Pb eutectic. The substrate is high-T_g laminate with ten chip sites on each substrate. Underfill delamination is observed to be the predominant mechanism causing electrical failure of flip chip on board assembly. Figure 16.34 shows the failed devices after 3120 cycles of thermal shock and 100% failure of the population. Weibull distribution of failures is shown in Fig. 16.35. Underfill delamination from the chip interface provides the path for solder extrusion. Solder extrusion can be seen from X-ray inspection in Fig. 16.36 and SEM images of a flat-section sample in Fig. 16.37. Solder joint fatigue failures are caused by CTE mismatch between silicon and laminate substrate concurrent with underfill delamination. Fatigue cracks at the flip-chip interface are shown in Fig. 16.38.



Fig. 16.34 Delamination at underfill and die interface



Fig. 16.35 Weibull distribution of failures for 63Sn37Pb solder alloy bumps

16.17.2 Test Results and Failure Mechanism (Lead-Free Solder)

The test die is PB8 perimeter bumped flip chip with 88 bumps at 0.203 mm pitch. The ball diameter is 0.127 mm. The solder alloy is 95.5Sn3.5Ag1.0Cu. Test temperature extremes (-55 to 150 °C) for the lead-free solder bumped test vehicle are chosen to be higher than that for the eutectic test vehicle. A Weibull distribution of failures is shown in Fig. 16.39. Similar to the failures in eutectic interconnections, cracks at the underfill-to-chip interface provide the path for solder extrusion. Figure 16.40 shows the delamination at the chip-to-underfill interface after failure. Solder extrusion can be seen from X-ray inspection in Fig. 16.41 and SEM images of a flat-section sample in Fig. 16.42. Solder fatigue failure caused by CTE





Fig. 16.37 Flat-section showing solder extrusion in underfill (SEM image)



Fig. 16.38 Fatigue cracks at the flip-chip interface





Fig. 16.39 Weibull distribution of failures for LF2 solder alloy bumps subjected to -55 to 150 °C thermal cycling



Fig. 16.40 Delamination at the chip-to-underfill interface after failure



Fig. 16.41 Solder extrusion in X-ray image for 95.5Sn3.5Ag1.0Cu solder bumps

Fig. 16.42 Solder extrusion in underfill (SEM image) for 95.5Sn3.5Ag1.0Cu solder bumps





Fig. 16.43 Fatigue cracks at the flip-chip interface for 95.5Sn3.5Ag1.0Cu solder bumps

mismatch between silicon and laminate substrate and by underfill delamination is shown in Fig. 16.43.

16.18 Need for Potting Compounds in Electronics Operating at High-G Acceleration

Aerospace and missile applications require electronics to sustain high acceleration levels during normal operation. Missile applications increasingly use commercial off-the-shelf electronics components with the expectation of reliable operation under acceleration loads up to 50,000 g. Unlike consumer electronics, military systems have longer lifetimes, in the neighborhood of 20–40 years, and higher reliability requirements. The newest electronics technologies find their way into consumer applications much before their introduction into high-rel applications, such as

aerospace and missile platforms. The primary reason is risk-averseness toward the use of technologies that often push the edge of the envelope in terms of miniaturization and, in many cases, cannot be compared with the state-of-art systems in operation and lack decades of historical data to provide robust proof of their survivability. Tools and techniques are needed to determine the failure envelopes for new component technologies, which were originally designed for office benign applications, under high acceleration loads in current and next-generation military systems. One of the primary test standards to determine the survivability of electronics in consumer applications is the JEDEC Test Standard JESD22-B111 requiring components to survive a 1500 g, 0.5 ms pulse. The JESD22-B111 shock test board has 15 components in a 3×5 component array configuration on a 132×77 mm test board [JEDEC 2003]. The test method is widely used to assess the drop survivability of components for handheld electronic products, although the correlation of the test results with the survivability of the components in the product is quite weak. A component's survivability in a product is influenced by many factors including board construction, board size, board thickness, and component design rules. The same component may have large variance in shock survivability depending on the product implementation.

16.19 ABAQUS/Explicit Finite Element Modeling

An explicit finite element model in ABAQUS, explicit for unreinforced, underfilled, and potted test assemblies, can be developed for the prediction of the transient dynamics of board assemblies.

The PCB in the assembly is modeled with shell element 4-node reduced integration (S4R) elements. Packages, underfill material, and epoxy compound are modeled with continuum 3D element 8-node reduced integration (C3D8R) elements, and the solder interconnects modeled with B31 Timoshenko beam elements. An unreinforced test assembly model is shown in Fig. 16.44. Epoxy potted test vehicle model is shown in Fig. 16.45. A zoomed-in view of the model of an unreinforced package on the test assembly is shown in Fig. 16.46. The board assembly mounted in the configuration of the drop test on the drop tower is shown Fig. 16.47. The rigid drop floor for the drop test simulation has been modeled using rigid R3D4 elements. A reference node has been placed behind the rigid wall for application of constraints. Node-to-surface contact has been used for the impact between the shock table and the floor. An event length of 5 ms after impact has been modeled. Time history has been monitored at a time period of 0.1 ms at the corner solder joints of all BGAs in the test assembly.

Peak displacement contour predictions from the transient dynamic analysis of the shock event in ABAQUS/Explicit have been plotted. In each case, the solder joint strains have been extracted for the time step with the peak out-of-plane board displacement. Figures 16.48 and 16.49 show the out-of-plane deflection and corner solder joint strain, respectively, for the STYCAST 2850FT potted TV under



550



Fig. 16.46 Unreinforced package



10,000 g. The location of the corner solder joint where the peak solder strains were exhibited is shown by the red dots in the plot. The peak FE displacement for 10,000 g STYCAST 2850FT potted board is 2.52 mm, and peak solder strain is 3900 μ for the package CTBGA132. Figures 16.50 and 16.51 show the out-of-plane deflection contour and the corner solder interconnect strains of Armstrong A12 potted board under 10,000 g. Peak FE displacement is 2.49 mm, and the peak corner solder strain is 2900 μ e.

From the model predictions of 25,000 g shock, displacement contours and corner solder strains were extracted from the explicit dynamic analysis. Figures 16.52 and 16.53 show the displacement contours and the corner solder interconnect strains of unreinforced bare package TV subjected to 25,000 g shock. Peak displacement value at the center is 2.69 mm, and the peak solder interconnect strain is 6400 μ e. The displacement contour just after the impact and the corner solder interconnect strains for the ME531 (NUF-1) underfilled TV at 25,000 g shock are shown in Figs. 16.54 and 16.55, respectively. Peak displacement value is 2.54 mm, and the peak corner



Fig. 16.48 STYCAST 2850FT potted TV model displacement at 10,000 g shock



Fig. 16.49 Corner solder interconnect strains of STYCAST 2850FT epoxy potted board at 10,000 $\rm g$



Fig. 16.50 Armstrong A12 potted TV model displacement at 10,000 g shock



Fig. 16.51 Corner solder interconnect strains of Armstrong A12 potted board at 10,000 g



Fig. 16.52 Unreinforced bare TV displacement at 25,000 g shock



Fig. 16.53 Corner solder interconnect strains of bare TV at 25,000 g



Fig. 16.54 ME531 underfill reinforced TV displacement at 25,000 g shock



Fig. 16.55 Corner solder interconnect strains of ME531 underfill reinforced TV at 25,000 g



Fig. 16.56 Unreinforced bare TV displacement at 50,000 g shock

solder interconnect strain is 5900 $\mu\epsilon$. In comparison with the values at 10,000 g, the peak displacements at the 25,000 g shock level for both the unreinforced and the underfilled configurations show an increase of about 0.2 mm, and the peak solder strains also follow this trend by a change of 2500–3000 $\mu\epsilon$.

The out-of-plane board displacement and solder interconnect strains of unreinforced bare TV at 50,000 g shock are shown in Figs. 16.56 and 16.57, respectively. Peak displacement for the 50,000 g test condition is 3.29 mm, and the maximum solder interconnect strain value is seen for the package CTBGA84 with a peak strain value of 15,200 μ e. In Figs. 16.58 and 16.59, the out-of-plane displacement after the impact and the solder interconnect strains in the package corner for ME531 underfill reinforced TV at 50,000 g shock are shown, respectively. The peak displacement value from the contour is 3.18 mm, and the peak solder interconnect strain is seen in CVBGA360 with peak strain values of 14,800 μ e.



Fig. 16.57 Corner solder interconnect strains of bare TV at 50,000 g shock



Fig. 16.58 ME531 underfill reinforced TV displacement at 50,000 g shock



Fig. 16.59 Corner solder interconnect strains of ME531 underfill reinforced TV at 50,000 g

16.20 High-G Shock Survivability Tests

The transient dynamic shock event was captured using high-speed imaging, and 3D-DIC (digital image correlation) analysis was performed to characterize the full-field displacement and strain measurements. The displacement contours shown in this section were the peak deflection contours just after the impact. Figure 16.60 shows the DIC measurements show the out-of-plane displacement contours for STYCAST 2850FT epoxy potted board at 10,000 g shock event. The measured peak displacement near the center was 2.59 mm. Similarly, Fig. 16.61 shows the out-of-plane displacement contours for Armstrong A12 potted test board subjected to 10,000 g shock with a peak displacement at center measured was 2.48 mm. Figures 16.62 and 16.63 show the displacement contours for the 25,000 g shock event of bare unreinforced TV and ME531 underfill reinforced TV, respectively. The peak values corresponding to the bare TV and ME531 underfill TV at 25,000 g are 3.41 mm and 3.08 mm. Figures 16.64 and 16.65 show the displacement contours from a 50,000 g is 3.62 mm as shown in Fig. 16.66.

The peak displacements for ME531 underfill reinforced and Armstrong A12 epoxy potted TVs shown in Figs. 16.65 and 16.66 are 3.19 mm and 3.39 mm, respectively. The test board with STYCAST 2850FT epoxy failed at the second drop, and the potting material itself delaminated at the first drop under 50,000 g.



Fig. 16.60 Epoxy 2850FT at 10,000 g out-of-plane displacement



Fig. 16.61 Epoxy A12 at 10,000 g out-of-plane displacement


Fig. 16.62 Bare TV at 25,000 g out-of-plane displacement



Fig. 16.63 ME531 underfill reinforced TV at 25,000 g out-of-plane displacement



Fig. 16.64 ME531 underfill reinforced TV at 50,000 g out-of-plane displacement



Fig. 16.65 Armstrong A12 potted board at 50,000 g out-of-plane displacement



Fig. 16.66 Bare TV at 50,000 g out-of-plane displacement

16.20.1 PCB Strains

In-plane PCB-X and PCB-Y strains near the corner interconnects of the packages were extracted from DIC analysis. In each case, the corner location plotted is the solder joint with the maximum in-plane strain value. Figures 16.67 and 16.68 show the in-plane PCB-X and PCB-Y strains of STYCAST 2850FT potted board at 10,000 g shock. The peak value near the corner interconnects of the packages was in the neighborhood of 4800 μ e in PCB-X and 4100 μ e in PCB-Y. Similarly, Figs 16.69 and 16.70 show the in-plane PCB strains of Armstrong A12 potted board subjected to 10,000 g shock. Peak strains were 3300 μ e in PCB-X and 2700 μ e in PCB-Y.

Figures 16.71 and 16.72 show the in-plane PCB-X and PCB-Y strains of unreinforced bare TV subjected to 25,000 g shock. Peak values of PCB-X and PCB-Y are 4200 $\mu\epsilon$ and 6800 $\mu\epsilon$. Similarly, Figs 16.73 and 16.74 show the in-plane PCB-X and PCB-Y strains, respectively, of ME531 underfill reinforced TV. Peak values of PCB-X and PCB-Y in this case are 4300 $\mu\epsilon$ and 5600 $\mu\epsilon$. In-plane PCB strains at 50,000 g for unreinforced bare TV are shown in Figs. 16.75 and 16.76. The peak values near the corner interconnects are in the neighborhood of 4500 $\mu\epsilon$ in X and 6500 $\mu\epsilon$ in Y. Similarly the PCB-X and PCB-Y strains at 50,000 g



Fig. 16.67 PCB-X strains of STYCAST 2850FT potted board at 10,000 g



Fig. 16.68 PCB-Y strains of STYCAST 2850FT potted board at 10,000 g



Fig. 16.69 PCB-X strains of Armstrong A12 potted board at 10,000 g



Fig. 16.70 PCB-Y strains of Armstrong A12 potted board at 10,000 g



Fig. 16.71 PCB-X strains of bare TV at 25,000 g shock



Fig. 16.72 PCB-Y strains of bare TV at 25,000 g shock



Fig. 16.73 PCB-X strains of ME531 underfill reinforced TV at 25,000 g shock



Fig. 16.74 PCB-Y strains of ME531 underfill reinforced TV at 25,000 g shock



Fig. 16.75 PCB-X strains bare TV at 50,000 g



Fig. 16.76 PCB-Y strains bare TV at 50,000 g



Fig. 16.77 PCB-X strains of ME531 underfill reinforced TV at 50,000 g



Fig. 16.78 PCB-Y strains of ME531 underfill reinforced TV at 50,000 g

for ME 531 underfill reinforced TV are shown in Figs. 16.77 and 16.78, respectively. Peak values near the marked corner regions are 5300 μ e in X and 5500 μ e in Y. Figures 16.79 and 16.80 show the in-plane PCB-X and PCB-Y strains of Armstrong A12 potted board subjected to 50,000 g shock. The peak values of 6100 μ e in x and 4300 μ e in y can be seen from Figs. 16.79 and 16.80.



Fig. 16.79 PCB-X strains of Armstrong A12 potted PCB at 50,000 g



Fig. 16.80 PCB-X strains of Armstrong A12 potted PCB at 50,000 g

16.21 Survivability and Failure Analysis

Survivability of the components under various package configurations at each g-level is discussed in this section. Figure 16.81 shows the survivability comparison of the four configurations of test board subjected to 10,000 g shock. In the case of bare and underfill reinforced TVs, CTBGA228 and CVBGA360 packages were the

Survivability @ 10,000g shock



Fig. 16.81 Survivability of various TV configurations at 10,000 g shock

first ones to fail early just under five drops. These two packages have a bigger footprint compared to the rest. The underfill reinforced packages of CVBGA97, CTBGA84, and CTBGA132 survived at least five to seven drops more as opposed to the bare TV condition at 10,000 g shock.

Contrasting results were observed between the two potting compounds STYCAST 2850FT and Armstrong A12. The total number of drops to fail all the components on the STYCAST 2850FT potted board at 10,000 g shock is six with the earliest failure seen at first drop for CTBGA228 and CVBGA97 and 6th drop for CTBGA132. The reason for the early failure of the components is attributed to the hard and brittle nature of the cured STYCAST 280FT epoxy. During the progressive exposure of the test boards to drop, the potting material fractured into pieces and peeled off from the board. The Armstrong A12 potting compound performed very well in mitigating the early failure of at least two packages CVBGA97 and CVBGA360 when compared to the STYCAST potted board. These CVBGA97 and CVBGA360 packages survived 90 and 98 drops with the Armstrong A12 potting compound, respectively, and the drop performance increased at least by 50 drops when compared to the bare and underfill reinforced TVs.

The in-plane PCB strains near the package corners of Armstrong A12 potted board were considerably less when compared to the STYCAST board at 10,000 g. Armstrong A12 excellently absorbed the shock and minimized the flexure, which eventually increased drop performance. Unreinforced bare TV and ME531 underfill reinforced TV were subjected to 25,000 g shock, and the corresponding drops to failure chart are shown in Fig. 16.82. CTBGA228 was the first package to fail under two drops in both conditions followed by CTBGA360 failing under five drops. Survivability @ 25,000g shock



Fig. 16.82 Survivability of various TV configurations at 25,000 g shock



Fig. 16.83 Survivability of various TV configurations at 50,000 g shock

Unreinforced bare TV package CTBGA132 survived maximum of 31 drops under 25,000 g shock. When the g-level was increased from 10,000 g to 25,000 g, the number of drops to failure decreased by ten drops in the case of bare TV. Similarly, in the case of ME531 underfill, reinforced TV survivability decreased by eight drops. Figure 16.83 shows the survivability chart for the four package configurations subjected to 50,000 g shock. The CTBGA132 package survived the maximum

number of drops in both the bare TV configuration and underfill TV at 50,000 g shock, with 26 and 29 drops, respectively. When compared to the 10,000 g shock counterparts of the same test vehicle configuration, the drop performance has decreased anywhere between 15 and 20 drops. In the case of potted boards, the STYCAST TV followed the same trend, failing all the components in the first drop itself. The potting compound shattered the same mode as seen in the 10,000 g shock case. All the packages in the Armstrong A12 potted board were also failed under ten drops at 50,000 g shock. The considerable decrease in the performance can be attributed to the inertial and high dynamic nature of the 50,000 g ramp from 10,000 g shock.

16.22 Summary

In this chapter, a methodology based on the modified random sequential adsorption algorithm has been discussed, to generate statistically isotropic cubic unit cells of nano-underfills containing random-sized, randomly distributed nano-fillers. Finite element models based on random sequential addition algorithm have been presented for prediction of linear and nonlinear material properties of nano-underfill materials. Model validation of properties with experimental data has been discussed. CTEs, elastic moduli, and viscoelastic properties, including stress relaxation, have been predicted and correlated with experimental data, as a function of the filler volume fraction. In addition, the bulk modulus and Poisson's ratio have been predicted as functions of the volume fraction. Temperature-dependent properties, including stress-strain and stress relaxation data, have been measured as functions of temperature between the extremes of -175 and +150 °C for lead-free and -55 to 125 °C for eutectic bumped flip-chip die is used to evaluate the thermomechanical reliability of the flip-chip assemblies with nano-underfill.

The efficacy of potting compounds and underfills for fine-pitch electronics in fuzing applications has been discussed with data from high-speed 3D-DIC measurements along with explicit finite element modeling to study the transient dynamic behavior and characterize the in-plane board strain and out-of-plane deflection of assemblies. Solder joint strains during the shock event have been extracted for both g-levels between 10,000 and 50,000 g shock events on unreinforced, underfilled, and potted assemblies. Experimental data indicates that potting adds survivability margins for shock exposures up to 10,000 g. For shock exposures higher than 10,000 g, the delamination failure mode between the potting compound and the printed circuit board dominates reducing the design margin. Underfilling of the electronic components added survivability margin at all g-levels.

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Chapter 17 Carbon Nanotubes: Synthesis and Characterization



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17.1 Introduction

Carbon can form various types of structurally different frameworks due to the ability of the carbon atoms to form different species of valence bonds. The extremely organized coagulation process of carbon molecules resulting in the formation of the perfectly symmetric fullerene molecule despite the chaotic environment of the carbon arc is truly fascinating. Although many formation theories for the buckyball structure have been suggested, the "pentagon road model" is the most popular among many molecular physicists. The prominent features of this model are that carbon sheets have the tendency to accumulate isolated pentagonal carbon ring structures and grow into a carbon sheet with a large number of pentagons supporting its structure.

In the early years of the 1990s, Sumio Iijima, an electron microscopist from the NEC laboratories in Japan sifted through the soot formed inside the walls of the electric discharge chamber which was almost completely amorphous containing fullerene molecules. Iijima finally found remarkable graphitic structures when he observed cylindrical deposits on the cathode of the of the arc-discharge vessel [1]. A whole new era of intense research and experimental exploration began after the discovery of carbon nanotubes (CNTs) to understand their unique physical and electronic properties. Multiwalled carbon nanotubes (MWCNTs) and double-walled carbon nanotubes (DWCNTs) were produced during the initial arc-discharge experiments by various research groups all over the world. Synthesis of single-walled carbon nanotubes (SWCNTs) [2] was reported by Iijima and Toshinari Ichihashi of NEC, Japan [3], and Donald Bethune's IBM group from California [4] independently.

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This chapter describes the basic characteristics of various kinds of carbon nanotube synthesis techniques. Conventional techniques of CNT growth include vaporphase growth, corona discharge, catalyst-supported growth, pyrolysis of hydrocarbons, and laser ablation. More recent techniques like plasma-enhanced chemical vapor deposition (PECVD) and chemical vapor deposition (CVD) not only produce better quality CNTs but can also be patterned with the desired orientations on substrates [5]. This chapter attempts to explain the bottom-up approach of growing CNTs from primary growth mechanisms to the more sophisticated and modern techniques of controlled chemical synthesis of CNTs.

17.2 Synthesis of MWCNTs

Many growth mechanisms for MWCNTs have been studied, and subsequent experiments were also conducted for optimizing high-quality CNTs, which can also be bulk produced. The various techniques to synthesize MWCNTs are briefly described in this section. A mixture of benzene vapor and hydrogen was made to react in a reaction chamber in which a graphite rod was used as the substrate. A series of hightemperature treatments followed, which resulted in a material very similar to MWCNTs. This work by M. Endo et al. [6] created MWCNTs of good quality but relatively smaller yields when compared to the arc-discharge method. Two graphite electrodes placed inside an arc-discharge chamber were used in the arc-discharge method. The arc struck between these two electrodes in an inert gas environment resulted in not only high-quality nanotubes but also produced better yields than any other methods. Further experimentation by Ajayan and Ebbesen in their 1992 paper "Large scale synthesis of carbon nanotubes" [7] showed that the yield of CNTs is extremely sensitive to the pressure of helium gas introduced into the arc-discharge chamber. Other methods include electrochemical growth and catalytic growth of MWCNTs. Electrochemical growth was not very successful as it produced nanotubes with defective walls and also filled the innermost cylinder with chemical remnants. In the catalytic method, a pretreated substrate containing tiny catalytic particles on it is exposed to a temperature treatment chamber which results in nucleation of the fiber-like growths on the substrate surface (Dresselhaus et al. [8]).

17.3 Synthesis of SWCNTs

Donald Bethune and his team at IBM's research center in San Jose discovered SWCNTs [4]. The team's experiments began with exploring the electrical and magnetic properties of fullerene-related molecules, which enclosed metal particles. Blankets of soot, which clad the inner walls of their arc evaporation chamber, contained fullerene tubes of only one atomic layer. Subsequently, after more

research on improving the technique of SWCNT growth by arc evaporation method, the same IBM team in collaboration devised a catalytic method of growth of SWCNTs.

17.4 Arc-Discharge Method

The arc-discharge method was first used to produce C_{60} and other fullerene molecules by changing the conditions of the arc discharge [2], which makes it one of the easiest and most common methods to produce CNTs in abundance. CNTs synthesized by a conventional arc discharge are mostly accompanied by a carbonaceous mix of carbon nanoparticles of undefined physical characteristics [2]. The carbon arc-discharge method typically consists of two high-purity graphite electrodes placed in close proximity to each other with a separation distance of approximately 1 mm. An electric arc is struck between the graphite electrodes in an inert gas environment at low pressures by the application of homogenous electric voltage to produce a variety of fullerene molecules. Anodic carbon sublimes due to high temperature in the reaction zone resulting from potential difference and high current between the electrodes. The arc-discharge carbon molecules recondense at the cathode forming filamentous CNTs. The wide range of CNTs produced on the surface of the cathode have varying morphologies and suffer from a variety of defects like amorphous carbon matter deposited on the inside and outside of the CNT walls. SWCNTs can be formed by use of metallic catalysts within the hole in the anodic electrode. Scientifically useful specimens of CNTs can be retrieved from the crude end product of the arc discharge only after purification/distillation, which separates CNTs from carbon soot and other metallic residues. Research have scaled to new dimensions where Ishigami et al. have shown continuous production of MWCNTs through arc vaporization of graphite electrodes in liquid nitrogen [9].

A schematic representation of an arc discharge used by Yoshinori Ando et al. [10] from Japan is shown in Fig. 17.1.

17.4.1 Important Parameters for CNT Formation During Arc Discharge

The process of CNT creation near the cathode surface has been well explained by Eugene G. Gamaly and Thomas W. Ebbesen when they proposed a model for CNT formation based on the interaction of the bimodal carbon velocity distribution [11, 12]. According to Gamaly et al., the carbon particle distribution in the raw rodlike carbonaceous deposit at the cathode is bimodal. While one mode is comprised of carbon nanoparticles of small size with varying shapes, the other mode represents CNTs of typical micrometer lengths with an outer diameter of 2–20 nm



Fig. 17.1 Redrawn schematic of arc-discharge chamber used for producing carbon nanotubes [10]

and inner diameters between 1 and 3 nm. This study of the mechanism of CNT formation revolved around answering key questions about interesting observations regarding the carbon deposits on the cathode.

Physical conditions of the arc discharge for efficient CNT production include parameters like potential drop between electrodes, current density in the arc, the interelectrode spacing, plasma temperature, and pressure of the helium gas inside the chamber.

Electric parameters include the space-charge region near the cathode area where there is maximum potential drop due to the positive space charge around it. The gaseous mixture in the interelectrode region comprising neutral helium atoms and neutral and ionized carbon species is important for determining the ionization potential in the arc. The condition of the potential drop between the electrodes being lesser than the first ionization potential is important to maintain the stability of the arc. The introduction of ions in the buffer gas might destabilize the ionic current, leading to the instability of the arc.

The study also confirms that the vapor layer near the surface of the electrode is most suitable for reactions involving carbon cluster formations. The effect of cooling of the system also has an impact on the quality and growth structure of the CNTs produced.

17.4.2 Mechanism of CNT Formation During Arc Discharge

After conducting numerous experimental and theoretical studies, Gamaly et al. proposed a sequence of events during the formation of CNTs in the arc-discharge chamber [2, 12–14]. The vapor layer near the cathode surface is a result of evaporation of the solid graphite cathode consisting of saturated carbon vapors supporting maximum reactions to attach two groups of carbon particles having different velocity distributions. Two competing sources of carbon are as follows: one group, which is a result of the evaporation from the cathode surface, has a Maxwellian velocity distribution, while the other group composing of ions accelerated between the two potentials of the electrodes has a single energy component oriented along the direction of the current. Thus, it can be noted that the absence of symmetry in the Maxwellian carbon groups will lead to the formation of random carbon clusters with unpredictable geometries, while the reacting particles from the directed current flux may form the elongated structures like CNTs.

The process of carbon deposition to form rodlike structures on the surface of the cathode is a result of many layers of carbon deposition. The following is the sequence of events responsible for the formation of CNTs during the arc-discharge process:

Seed Formation Seed structures are believed to be important for the growth of the carbon tubules. Initial heating and ionization of the electrodes and interelectrode gas play an important role in establishing a steady ion current [11]. If the purge gas used to carry out DC arc discharge is pure hydrogen, a reduced carbon nanoparticles deposit is found in crude soot as opposed to hydrocarbon gaseous environment [15]. As discussed earlier, the initial velocity distribution of the interacting particles which is Maxwellian is accompanied by the directed current fluxes which give rise to seed structures [12].

CNT Growth The seed particle, which condenses on the cathode, interacts with the electric field in the cathode sheath to induce an electric dipole moment in the neighboring particles. The interaction between the various seed particles may align the electric field such that it results in the formation of linear carbonaceous structures [16]. Gamaly et al. also elaborated that the elongated carbon tubule formed due to the interaction of the directed ions with the solid surfaces is three orders stronger than that of the carbon cluster formation process. Hence, the arc-discharge carbon formation process supports growth of carbon tubules along the axis of the symmetry more than the undirected formation of random carbon fullerene molecules. Simultaneously, the formation of Maxwellian velocity-distributed carbon particles to the growing tubules, thus forming MWCNTs.

CNT Kinetics Although negatively charged CNT seeds are repelled in the cathode sheath, some seed particles can get deposited on the cathode surface due to the momentum provided by the ion flux and the CNT initial velocity at the edge of the cathode sheath [16]. Keidar et al. from the University of Michigan established the



Fig. 17.2 Redrawn graph demonstrating that CNTs with large aspect ratios can overcome the potential barrier therefore making a transition through the cathode sheath and are deposited on the cathode [16]

parameters responsible for the formation of CNTs in different locations inside the arc-discharge chamber [16]. It is summarized that CNTs with smaller aspect ratios can be influenced by the plasma jet and can get deposited on the chamber walls, while those with longer aspect ratios get deposited on the cathode surface. The velocity that a CNT gains due to the interaction with the flowing plasma and this dependency on the aspect ratio of the CNTs determines the location of formed of the CNTS – on the chamber walls or cathode surface as explained in Fig. 17.2.

The resulting CNTs formed from the above methods are produced in abundance, but at the cost of quality, since the graphitization of the tube walls suffers from imperfections. X. K. Wang et al. from Northwestern University [2] have improved the quality of the buckytubes as compared to those prepared by the arc-discharge method by modifying certain physical and electrical components of the arc-discharge chamber. A tungsten wire, which acts as an extension to a Tesla coil, was incorporated and made to point toward the arc region. The "stable glow discharge" was produced by a corona discharge triggered by the Tesla coil, thus overcoming the instabilities caused when the anode and cathode are made to strike each other during a conventional arc discharge. Figure 17.3 demonstrates the differences in the time dependence of current across the interelectrode gap during the formation of CNTs between a conventional arc discharge and stable glow discharge. A Hewlett Packard 7090A Measurement Plotting system was used for recording the resultant glow discharge spectrum of both the arc discharge and stable glow discharge techniques. The glow discharge displays minimal current



Fig. 17.3 Comparative redrawn graphical representation of current discharge as a function of time for (**a**) stable glow discharge and (**b**) arc-discharge methods [2]

fluctuations with respect to time indicating that the process is homogenous and continuous, while on the other hand, the continuous variations of current in the arc-discharge method are indicative of the process being transient.

Many more research teams have studied and improved the method of arc-discharge technique of producing nanotube in terms of experimental ease, quality of nanotubes, production quantity, and parameter control schemes. Journet et al. devised a method to produce SWCNTs by the electric arc technique [17] where the quality of CNTs produced were of the same as those generated by the laser ablation technique. H.W Zhu and his team from China introduced interesting modifications to the arc-discharge technique where CNTs were produced in a container with water, thus eliminating the need for vacuum or a water-cooled chamber. The water-arcing process [18] produced high-quality MWCNTs.

Despite significant progress in carbon arc-discharge methods, there is tremendous challenge to produce SWCNTs of desired properties and aspect ratios. Keider et al. have demonstrated that the lack of control and poor flexibility in plasma-based arc-discharge method can be improved by increasing the discharge plasma density with an application of strong magnetic field [19, 20]. Similar to "stable glow discharge," the applied magnetic field produces brighter plasma discharge as shown in Fig. 17.4 causing both the current and plasma density to be confined in a smaller reaction zone. As a result, recondensation of sublimed carbon molecules is confined to a smaller space, and its structure becomes more pronounced resulting in longer aspect ratios.



17.5 Laser Ablation Method

In the early 1990s, Richard Smalley and his colleagues from Rice University were using energized power pulsed lasers to vaporize metallic targets to form various metal particles. The team was successful in creating MWCNTs when the metallic targets were substituted with graphite and a laser beam was impinged on the surface in an inert gas environment [21]. CNTs formed by this method require extensive purification of impure carbonaceous soot which affects both the quality and quantity of the final CNTs [22].

The experiment required an Nd:YAG argon laser with a 50-cm-long quartz tube inside a temperature-controlled furnace. The quartz tube is sealed after placing the graphite target, and the chamber is maintained at vacuum <10 mTorr with temperatures at 1200 °C. The Gaussian laser beam energized with 250 mJ is pulsed at 10 Hz in 10 ns pulses. The laser beam is then made to scan across the surface of the target to deposit soot on top of a water-cooled conical copper-collecting rod. Figure 17.5 accounts for the experimental details provided. This technique is not suited for continuous and mass production of CNTs as it involves operation under high power and an expensive laser environment which yields small carbon deposits and increases production cost significantly.

Spherical fullerene molecules are likely to form in temperature environments close to 1000 °C, and the formation of close-ended CNTs is more likely in such cases of high-temperature conditions. The team made a very interesting observation about the existence of long-length (typical μ m range) MWCNTs which would normally be



Fig. 17.5 Redrawn schematic representation of the experimental setup used by Smalley et al. to prepare CNTS using the laser ablation technique [21]

absent at temperatures ranging well over 1000 °C as observed from Fig. 17.5. Owing to the high annealing temperatures, the fullerene yield would rather comprise of the more energetically stable spherical fullerene rather than long nanotubules which were otherwise expected to get closed off at the ends with the nanotube precursor exposed to such high temperatures. The final fullerene yield consisted of MWCNTs and spherical carbon molecules called "carbon onions." The absence of SWCNTs provides a key explanation to the process of the formation of MWCNTs in the laser ablation technique. Figure 17.6 explains the theory behind the formation of CNTs despite the high temperatures of the furnace. Based on the gas-phase mechanism, the team hypothesizes that the carbon atoms bridge between the adjacent edges of the growing graphene sheets, thus prolonging their open-ended structures.

In the same year, Guo et al. from Rice Quantum Institute devised a procedure to catalytically grow SWCNTs by the laser ablation technique [23]. A mixture of transition metals like cobalt and nickel catalyzed the carbon vaporization event during the direct laser vaporization process.

A few years later, C. D. Scott and his team of researchers from Houston theorized the growth mechanism for SWCNTs in the laser ablation process [24] using two Nd: YAG pulsed lasers impinging on a graphite target containing a certain percentage of cobalt and nickel. The team's investigation suggested that the carbon, which is the source for nanotube formation, is found not only in the graphite target but also from the carbon particles present in the reaction zone. Fullerene molecules formed during the laser vaporization process may also participate as carbon feedstock, thus effectively reducing the contamination rates of SWCNTs during the tubule formation



Fig. 17.6 Redrawn figure represents fullerene branching paths during the CNT formation in the laser ablation technique [21]

process. Contemporarily, M. Yudasaka and his coworkers from NEC Corporation, Japan, thoroughly delved into the process of SWCNT formation during the laser ablation process in the presence of nickel, cobalt, and nickel-cobalt catalysts [13]. The Japanese team of scientists, along with Sumio Iijima, revealed that the yield of SWCNTs depended on the target composition schemes of the catalysts, viz., cobalt and nickel.

When the conventional laser ablation method shown in schematic Fig. 17.5 is loaded with metallic catalysts as described earlier, it forms carbonaceous soot directly on the water-cooled Cu collector. However, in the current decade, controlled growth of CNTs directly on substrates is strongly desirable with potential applications in nanoelectronic industrial applications. Aïssa et al. investigated, developed, and demonstrated an "all-laser CVD-like" process for on-substrate growth of SWCNTs on SiO₂/Si substrates using an UV KrF excimer laser. The metal catalyst nanoparticles first deposited onto the substrates act as seed sites for subsequent growth of CNT networks [25].

The size of the metallic nanoparticle formed highly influences yield and thermal oxidation of amorphous carbon which affects the purification efficacy. Studies demonstrate that catalyst particle sizes can be controlled by the number of laser pulses for ultrafast growth of MWCNTs by tip-end growth mode. The resulting CNTs synthesized via pulsed laser ablation of targets in liquid exhibited periodic structure and chirality.



Fig. 17.7 (a) Cobalt (Co) and carbon (C), theinhomogenous mix resulting in no growth of SWCNTs. (b) More homogeneous distribution of nickel (Ni) or nickel-cobalt (NiCo) resulting in the formation of SWCNTs. (c) chemical reactivity of Ni and C reduced at lower temperatures leading to reduced yield of SWCNTs (d) iron (Fe) dissolves in carbon and the mixture remains as a solid solution at room temperature making it impossible for Fe clusters to segregate in the C-Fe droplets, thereby eliminating the possibility of growth of any SWCNTs

Figure 17.7 pictorially depicts the dependency of SWCNT yield on metal species [13]. Figure 17.7a: cobalt (Co) does not melt very well in the carbon (C), thereby causing inhomogeneous distribution of Co and no growth of SWCNTs. Figure 17.7b: nickel (Ni) or nickel-cobalt (NiCo) distribution was more homogenous in the molten carbon causing the formation of SWCNTs. Figure 17.7c: chemical reactivity of Ni and C would be reduced at lower temperatures leading to reduced yield of SWCNTs. Figure 17.7d: iron (Fe) dissolves in carbon and the mixture remains as a solid solution at room temperature making it impossible for Fe clusters to segregate in the C-Fe droplets, thereby eliminating the possibility of growth of any SWCNTs.

17.6 Pulsed Corona Discharge Method

In 2004, Lekha Nath Mishra and his colleagues have used the pulsed corona discharge technique to prepare CNTs [26] by deposition of methane at atmospheric pressure. The process of successful production of hydrogen and CNTs has been attributed to the enhanced electric field near the surface of the inner electrode. The experimental technique paves the way for mass production of hydrogen as an energy source and CNTs for industrial and academic purposes.

A few years later, Noriaki Sano et al. from Japan made use of a needle electrode by atmospheric pressure corona discharge [27]. The carbon source was methane in a hydrogen stream, and CNT formation was observed at the tip of the needle-shaped cathode. MWCNTs were created at a localized surface on the tip of the needlelike electrode, and strong electric fields enhanced CNTs to form a freestanding MWCNT forest at the cathode tip.

Recently, H. S. Uhm and his team from Korea have devised a new technique to produce CNTs with a portable microwave plasma torch at atmospheric pressure [28]. Acetylene, which acted as a carbon source, was used in conjunction with iron pentacarbonyl acting as the metal catalyst. A high-temperature furnace was also incorporated to increase the yield of CNTs.

17.7 Other Methods

Catalytic pyrolysis: In 1998, H. M. Cheng and his coworkers produced bundles of SWCNTs by catalytic decomposition of hydrocarbons at temperatures around 1200 °C using the floating catalyst method [8]. Under different growth conditions, the addition of thiophene made it possible to enhance the production of SWCNTs and MWCNTs. Shortly thereafter, an Australian group of researchers synthesized large arrays of CNTs on glass and quartz substrates by pyrolysis of iron phthalocy-anine in the presence of Ar/He at 800–1100 °C [29]. Aligned CNTs were also patterned into microarrays through a partially masked surface or contact printing process. De-Chang Li et al. devised a method to synthesize aligned CNT films by pyrolysis. The growth mechanism of the pyrolytic method of growing CNTs was theorized to involve the participation of iron nanoparticles of two different sizes. The smaller iron particles act as the active catalyst responsible for the nucleation of the nanotube, while the larger iron particles behave as the feedstock of carbon for the formation of CNTs. The bamboo-like growths after pyrolysis are a result of surface diffusion of carbon atoms on the larger iron particle.

The arc-discharge, laser vaporization method and the catalytically supported methods of synthesizing CNTs are capable of producing SWCNTs and MWCNTs in bulk and economically. The above-described methods of fabricating CNTs are difficult to integrate, and factors like the location and alignment of CNTs during their synthesis are under very little experimental control. The CVD method of synthesizing CNTs has shown promising results of producing high-quality CNTs in large quantities. Synthesizing CNTs using CVD schemes has resulted in producing organized CNT structures/arrays, which can be readily integrated into various electronic, sensing, mechanical, and chemical application-oriented devices.

17.8 Chemical Vapor Deposition (CVD) Method

The CVD technique is the most common catalyst-based technique used in research as well as commercial production of CNTs. This method has a capacity to economically grow large volumes of CNTs, with lengths up to 18 mm with controlled growth direction [30]. In this process, hydrocarbons are catalytically decomposed at temperatures below 1100 °C onto a metallic surface to form carbon structures of desired geometry [31]. The parameters that affect the growth of CNTs are the catalyst materials, catalyst particle sizes, and the related support, temperature, pretreatment time, carbon source, and pressure of the carbon source.

17.8.1 Parameters Affecting the Growth of CNTs

17.8.1.1 Temperature

Temperature has an influence on the dimensions of the diameter as well as type of CNTs synthesized, i.e., whether they are SWCNTs or MWCNTs. It has been observed that there is an increase in the diameter of the CNTs with an increase in the temperature. The average CNT outer diameter has been found to increase from 20 to 150 nm and the growth rate from 1.6 to 28 μ m/min with increasing temperature in a fixed-bed reactor [32]. In contrast, many researchers did not find a significant change in diameter due to temperature variation [33]. Nerushev et al. demonstrated that the diameters of CNTs depend on particle size, the growth temperature, and the carbon flux rate, rather than only on temperature. At a certain critical condition, CNTs with similar diameters were grown [34]. Therefore, further investigation is required for understanding the temperature dependence on the growth process. Figure 17.8 shows CNT growth rate and diameter dependence on temperature.



17.8.1.2 Pressure

The fluidized bed reactor (FDCVD) process is generally performed at atmospheric pressure. There has been no significant understanding that indicates that the FDCVD process is dependent upon pressure variations. It has been found that in the plasma-enhanced CVD technique, parameters such as diameter, quality, and growth rate can be changed under controlled pressure [35]. An increase in the diameter, with improved quality and faster growth rate, has been observed as the pressure decreases. Growth rates of 1–3 mm/min and CNT diameters of <30 nm with well-graphitized features have been observed in the higher-pressure system, as compared to lower growth rates, larger diameter sizes, 0.1 mm/min growth rate, 60–80 nm CNT diameters, and bamboo-like structures in the low-pressure system.

17.8.1.3 Carbon Source

Carbon monoxide, methane, ethylene, acetylene [29], benzene [36], camphor [37], methanol [38], and ethanol [38] are the different carbon sources used in CVD processes. Different structural formation of the hydrocarbon chains as either the straight chain or the benzene ring has influence on the type of CNTs formed, as compared to the thermodynamic properties (e.g., enthalpy). It has been observed that methane and aromatic molecules favor the formation of SWCNTs. Toshiaki Nishii et al. [39] and Liu et al. [40] used carbon monoxide, methane, and ethylene as carbon sources for growth of SWCNTs.

17.8.1.4 Metal Catalyst

Metal transition catalyst is used for growth of MWCNTs and SWCNTs. Cobalt [41], nickel [42], and iron [43] metal nanoparticle and their alloy act as catalysts in CVD process. To achieve better selectivity, metals such as molybdenum, platinum, and copper have been used in combination with the metals catalysts. The type of metal catalyst is an important parameter in synthesis of CNTs as it determines the rate of carbon decomposition, yield, selectivity, and quality of products. Alloys of different composites provide an added advantage than pure metal nanoparticle. The University of Cincinnati has demonstrated the synthesis of the 18-mm-longest MWCNTs using a novel catalyst composite. In addition, with the use of a catalyst alloy, such as FeZrN, low-temperature growth of CNTs is possible [44]. The metal catalysts-surface interaction helps in understanding the morphology of catalyst on the base substrate, thereby the growth mechanism, base or tip (illustrated in Fig. 17.12). The tip-growth mechanism is where decomposition of hydrocarbons takes place on the metal surface with carbon diffusing downward and pushing the metal catalyst off the substrate. On the other hand, hydrocarbons decompose on the lower surface of

the metal with the carbon diffusing upward in the base-growth mechanism. Different substrates, typically Al_2O_3 , MgO, or SiO₂, are used as catalyst supports to disperse the catalyst onto the surface for CNT growth in CVD techniques.

17.8.1.5 Particle Size

The catalyst particle size has a major role in determining size as well as the type of CNTs: MWCNTs or SWCNTs [45]. The catalyst particle size that determines the nature of CNTs is still unclear and needs to be studied. It has been determined that the growth rate and the highest production yield can also be determined by the catalyst metal nanoparticle size. In CVD, there is a contradiction in the correlation between the catalyst nanoparticle and the CNT diameter. For example, in the base-growth mechanism with a catalyst particle diameter of 20 nm, CNTs with small diameter were synthesized, whereas the CNTs' diameter sizes were equal to those of the catalyst particle diameters in the tip-growth mechanism. Furthermore, irrespective of particle size, the diameter of the CNTs can be changed by controlling the residing time of the reactive gas in the reactor chamber [46].

17.8.2 Basic Concepts

In CVD processes, CNTs are synthesized by using two gases that are injected into the reactor: the process gas and the hydrocarbon gas. Acetylene, ethylene, ethanol, and methane are the most common gases containing carbon, whereas ammonia, nitrogen, and hydrogen are used as process gases. Prior to the inflow of the gas into the reactor, the substrate is prepared. Substrates are usually silicon, glass, or aluminum. Catalyst metal nanoparticles are deposited onto the substrate by solution, e-beam evaporation, or sputtering, which serves as a catalyst for the growth of carbon nanotubes. Later the substrates are placed into the reactor tube at temperatures varying from 700 to 900 °C and at atmospheric pressure. During the reaction process, injected hydrocarbons decompose near the catalyst nanoparticle, and the carbon atoms are transported to the edge of the metal particle to form a novel structure. Figure 17.9 shows microscope images of SWCNTs using a scanning electron microscope (SEM).

However, CVD schemes also support synthesis of CNTs at low temperatures (as low as 100 $^{\circ}$ C) and at atmospheric pressure (1 MPa) in the presence of a corona discharge [47]. The discharge process can be traced back to the 1850s when Siemens succeeded in generation of ozones with silent discharge techniques [48]. In the corona discharge plasma-enhanced CVD, synthesis of CNTs starts with the creation of metallic templates with the desired pore depth and density. Once the template has been created, the process of corona discharge starts in a plasma reactor which consists of wire electrodes, a thermocouple, a quartz tube, the gas discharge, and a plate electrode. The discharge is created in the reactor chamber at high voltage in the



Fig. 17.9 SEM images of MWCNTs synthesized using the CVD technique. The diameter of each MWCNTs is approximately 12–15 nm

presence of methane and hydrogen, which now act as precursors for the growth of CNTs. The common characteristics that influence the CNT formation in this process are the pressure, temperature, electric field, and electron energy [47]. The intensity of the electric field inside the chamber is influenced by the system pressure. If the pressure inside the chamber is increased, then the electric field intensity should be increased so as to obtain a steady field distribution. In order to compensate for the increase in pressure, a high voltage has to be supplied between the electrodes, which makes the system unstable. Thus, to maintain stability, the pressure in the reactor is maintained at atmospheric pressure [49].

17.8.3 Classification of CVD Methods

The synthesized process is classified based on catalyst type, the reactor alignment, the growth mode, and type of CNTs synthesized.

17.8.3.1 Classification Based on Catalyst

The size and shapes of CNTs are determined by the growth condition and the catalyst nanoparticles. The size and uniform distribution of the catalyst determine the radii of CNTs and preparation of pure CNTs with a uniform thickness, respectively. A sol-gel catalyst has assisted in synthesizing CNTs, which are aligned, isolated, and dense [50]. Substrates of mesoporous silica embedded with iron nanoparticles are fabricated by the sol-gel method. After 48 h of growth, 2-mm-long CNTs are formed [51]. Metal nanoparticle catalysts are embedded on the base substrate by physical evaporation or by sputtering in a simple and the most common method, whereas in the gas-phase metal catalyst method, both the catalyst and the hydrocarbon gas are injected into a tube reactor, and the catalytic reaction takes place in the gas phase [52]. SWCNTs were produced by condensation of a laser-vaporized carbon-nickelcobalt mixture at 1200 °C. The SWCNTs were formed when a graphite rod doped with Ni and Co was evaporated. SWCNTS have also been synthesized from a mixture of benzene and ferrocene (C₁₀H₁₀Fe) in a hydrogen gas flow. Similarly, the NEC Corporation, Japan [53], has synthesized CNTs by using reactant gases such as high-purity methane (CH_4) and hydrogen (H_2) . Ferrocene was used as a catalyst at 750 °C. The carbon decomposition was allowed to occur using methane gas in the presence of ferrocene gas. The reaction is:

$$CH_4(g) + H_2(g) \xrightarrow[Ferrocene]{600-1200°C} C(s) + 3H_2(g)$$

Of all the catalyst types discussed in this section above, large-scale synthesis has been achieved by gas-phase metal catalyst as the nanotubes are free from catalytic supports and the reaction can occur continuously.

17.8.3.2 Classification Based on Reactor

The reactor tube can be utilized either in the horizontal or in the vertical position for synthesis of CNTs. In a fixed-bed method [54], the reactor is aligned in the horizontal direction, whereas in the fluidized bed method [55], it is in a vertical position. Figures 17.10 and 17.11 show schematics of the reactor setups for the fixed- and fluidized bed methods, respectively.

Production volumes of CNTs in a fixed-bed reactor process are less than in the fluidized bed reactor. This is due to the fact that larger amounts of catalyst, with respect to the surface area of the quartz boat, would only increase the bed depth in a fluidized bed reactor. Thus, catalyst powders residing at the bottom of the quartz boat face diffusion limitations that thereby lower the overall activity of the catalyst. The different parameters affecting the growth of CNTs have been summarized. It has been demonstrated by Kathyayini et al. [56] and Zeng et al. [57] that there is an increase in production of the CNTs, by using the same amount of catalyst on larger contact areas compared to a contact area reduced by half. This is due to the fact that



Fig. 17.10 Redrawn schematic representation of the CVD reactor for the fixed-bed method. Both MWCNTs and SWCNTs of diameters ranging from 0.8 to 40 nm can be synthesized [55]



reaction of gases occurs on a larger surface area in the prior case, whereas in a fluidized bed reactor due to continuous mixing, there is an increase in reactive surface area and hence there is a large-scale production of CNTs. Synthesis of CNTs in a fluidized bed reactor eliminates diffusion limitations and also reduces fluidic effects when the process gas flow rate is maintained below the fluid velocity in the vertical reactor.

17.8.3.3 Classification Based on Growth Mechanism

The classification is based on the metal catalyst nanoparticle that is located either at the tip or at the base of CNTs. It depends upon the bulk/surface diffusion and also the interactive strength between the metal catalyst and the base substrate surface. The tip-growth mechanism is recognized due to weak catalyst-substrate interactions, i.e., low interfacial energy, while the base-growth mechanism is recognized due to strong interactions [58]. It has been demonstrated that there is a base-growth mode between Fe metal nanoparticles and alumina substrates due to strong bonding between them. Figure 17.12 represents the growth models of CNTs. In addition to the above-defined parameter, the growth mechanism is also dependent on the reaction temperature as previously discussed in Sect. 17.8.3.



Methods	Arc discharge	Laser ablation	CVD
Pioneer	Iijima (1991) [1]	Guo et al. (1995) [23]	Yacaman et al. (1993) [59]
Methods	CNTs synthesized on the graphite rod by direct cur- rent arc evaporation in the presence of inert gas	Evaporation of graphite metal using laser ablation on the metal transition target	Deposition of hydrocar- bon onto the metal transi- tion target in the presence of process gas
Type of CNTs growth	Both MWCNTs and SWCNTs	Only SWCNTs	Both MWCNTs and SWCNTs
Percent yields (%)	<75	<75	>75
Optimal tem- perature (°C)	>3000	>3000	>1200
Optimal pressure	50–7600 Torr (generally under vacuum)	200–750 Torr	760–7600 Torr (generally at atmospheric press)
Advantage	Simple, inexpensive, high- quality CNTs produced	Relatively high qual- ity of SWCNTs at room temperature	Large-scale CNTs are produced using FDCVD technique
Disadvantage	Requires high temperature and cannot be scaled up	Expensive technique; not good for large- scale CNT production	Quality of CNTs is not as good

Table 17.1 Comparison between arc discharge, laser ablation, and CVD techniques

17.8.3.4 Classification Based on Type of CNTs Synthesized

Both types of CNTs, i.e., SWCNT and MWCNT, can be grown using the CVD method. Temperature has a strong influence on the formation of specific types of CNTs, SWCNTs and MWCNTs, in this process. MWCNTs are generally observed at moderate temperatures (those between 500 and 800 °C), while SWCNTs tend to be observed at higher temperatures (>800 °C). Also, the size of the metal catalyst determines the nature of CNTs grown.

Table 17.1 shows the comparison between most of the common techniques used for the production of CNTs. The table describes the advantages and disadvantages between arc discharge, laser ablation, and CVD methods.

17.9 Vapor-Liquid-Solid (VLS): CVD Method

In this technique, the nanoparticle catalyst is used as a vapor-liquid-solid (VLS) growth catalyst for the synthesis of CNTs. T. Uchino et al. demonstrated that the germanium (Ge) nanoparticle can act as a seed for vapor-liquid growth of CNTs [14]. Using Raman measurement, SWCNTs were identified, and diameter ranges from approximately 1.6 to 2.1 nm. It has been noted that unlike metal catalyst nanoparticles, there was no reduction in the melting temperature of Ge nanoparticles. Not much detailed study or research has been conducted to analyze the effect of different parameters on the growth of CNTs in this technique, and further investigation is required for better understanding of it.

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Chapter 18 Characteristics of Carbon Nanotubes for Nanoelectronic Device Applications



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18.1 Introduction

Carbon has the incredible ability to combine with itself in varied proportions to form molecules of distinctly disparate physical structures. The evolution of modern organic chemistry began with the growing interest among scientists to experiment with carbon clusters formed during synthesis of carbon compounds. These studies on carbon-related compounds began with the support of rigid understanding of a common form of carbon – graphite. The carbon molecule C_{60} which was discovered in trace amounts in the carbon clusters was a soccer-shaped fullerene molecule which had 60 carbon atoms arranged in a way that each atom was placed at a vertex of a truncated icosahedron [1]. The discovery of Kratschmer et al. to produce C_{60} in bulk served as a platform for extensive study on carbon-related molecules by scientists, chemists, and material science experts all over the world.

Significant findings were not recorded until Sumio Iijima, an electron microscopist from NEC Laboratories, Japan, discovered tubular fullerenes [2] in the cathode of an arc evaporation chamber. The procedure of arc evaporation resulted in mass production of high-quality carbon nanotubes, [3]. A whole new era of carbon nanotube (CNT) research began after Iijima published his first paper on carbon nanotubes – "Helical Microtubules of graphitic carbon" – in 1992. Pictorially, one can understand the structure of the CNT to be more like an elongated fullerene molecule with half a buckyball capped at either end to form a capsule – like carbon enclosure. Figure 18.1 shows a schematic 3D representation of a single-walled carbon nanotube. (Note that the image depicts the morphology of a single-walled carbon nanotube in a rudimentary fashion and does not incorporate the hexagonal building blocks of a nanotube.)

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Scanning tunneling microscopy studies have provided strong evidence that carbon nanotubes occur in varied chiral configurations [4] and layers [2]. Atomic force microscopy studies have brought to light the amazing mechanical [5] and electrical properties [6] that CNTs exhibit. Carbon nanotubes can be classified into two major types based on their layer properties – single-walled carbon nanotubes (SWCNTs) and multiwalled carbon nanotubes (MWCNTs). Though there are both catalytic and non-catalytic methods to synthesize CNTs, the non-catalytic method of arc evaporation is popular not only for its high quality and bulk production of CNTs but also because the principle behind this mechanism is better understood than the other techniques.

SWCNTs can be conceptualized as a sheet of paper rolled out into a single hollow cylindrical structure [7]. SWCTs promise a great future for the stream of "carbon nanotechnology" owing to their large surface area, high aspect ratios, and a good capacity for functionalization. SWCNTs have been used mostly by the electronic industry to replace interconnect networks with molecular quantum wires [8] which demonstrate high conductivity. Recent advancements in the field of transistors have proved that SWCNT-based field-effect transistors exhibit good device characteristics like high gain and good switching speeds and prove fully operational at room temperature [9].

MWCNTs, reinforced with more outer layers, are morphologically different from single-walled carbon nanotubes. Electron transport cannot be counted as one-dimensional conduction since there are many atomic layers of graphite surrounding the innermost cylinder as seen in Fig. 18.2. Most atomic force microscopy techniques involve using MWCNTs to conduct studies on their tensile and elastic properties [10, 11]. Such studies related to the mechanical properties of MWCNTs have resulted in several constructive applications in industrial commercialization of consumer products. MWCNTs are used as strengthening fiber materials and as field emission tips in scanning probe microscopes.



Finally, in summary the properties of CNTs are determined by their synthesis methods, and this in turn determines their applicability. Described below are the various ways in which CNTs can be classified based on their structural and electrical properties.

18.2 Classification of Carbon Nanotubes

18.2.1 Classification Based on Layer Properties

CNTs can be classified mainly based on the number of layers which comprises each tubule.

Experimental observations on MWCNTs are more conclusive among researchers than that on SWCNTs. This is owing to the fact that MWCNTs were discovered earlier than SWCNTs. Studies and research data on SWCNTs are more recent and are relatively more conceptual than experimental. Figure 18.3 depicts schematically an ensemble of the various types of CNTs based on the number of layers each is composed of.

18.2.1.1 Multiwalled Carbon Nanotubes (MWCNTs)

MWCNTs are composed of concentric cylinders of varying diameters of graphene sheets rolled about the tube axis [12]. They were first discovered occurring in bundles and with various other graphitic structures occurring in the cathodic soot



Fig. 18.3 Schematic of cross-sectional views of CNTs depicting layer properties where N represents the number of layers of each CNT: (a) SWCNT, (b) double-walled CNT, (c) MWCNT with four layers, (d) MWCNT with five layers

inside the arc discharge chamber and as hard graphitic deposit on the electrode. The very first observation made by Iijima showed that each layer was separated by a distance of 0.34 nm [2]. This high-resolution TEM data showed that the outermost diameter of the cylinder ranged from being 2.5 nm to about 30 nm, with lengths of the nanotubes roughly occurring between a few nanometers to several micrometers.

MWCNTs, concentric hollow tubular structures of graphitic layers, are successfully synthesized in the laboratories as described above. Three arrangements of graphene layers have been reported so far in MWCNTs' formation: (a) the Russian doll configuration or coaxial cylindrically curved model in which graphitic layers are arranged in hollow nested concentric tubes with increasing radii, (b) the scroll model in which a single graphitic layer is arranged in spiral configuration, and finally (c) the mixed model consisting of both the configurations [12].

Most MWCNTs do not retain their original number of layers all along their lengths. The reason behind this reduction in the number of concentric cylinders is that the innermost layer walls begin to fuse after a certain length along the length of the nanotube. This effectively caps the central cores of the nanotube resulting in the appearance of a reduced number of layers. Cap terminations occur in different shapes, which can be revealed by high-resolution transmission electron microscopy.

A schematic representation of MWCNT capping is shown in Fig. 18.4.

18.2.1.2 Double-Walled Carbon Nanotubes (DWCNTs)

Although DWCNTs can be classified as a subclass of MWCNTs, their behavior is mostly like that of SWCNTs. Their double-walled nature, however, gives them special electrical, chemical, and mechanical properties making them unique to certain applications. However, synthesis of DWCNTs remains considerably challenging due to polydispersity, i.e., found in a heterogeneous mixture of SWCNTS and MWCNTs. Green et al. first demonstrated a way to separate DWCNTs from heterogeneous mixture based on density gradient ultracentrifugation [13]. DWCNTs can be analogous to coaxial cables. The outer cladding of the coaxial cable provides insulation to the inner core. In the same way, the outer tube of the DWCNT protects



Fig. 18.4 Schematic depicting capping in longitudinal cross sections of MWCNTs: (a) MWCNT with N = 3 reducing to N = 2 after capping and (b) MWCNT with N = 9 having several caps reducing N = 6

the inner tube from environmental elements, thus maintaining its purity. In other words, the outer wall provides an interface with the outer electrical or gaseous experimental systems without affecting the inner core. The outer tube can also be used as a good host to functional groups, thereby making the outer shell a good functionalization surface while preserving the inner tube mainly for electron transportation purposes.

DWCNTs are being explored for possibilities of using them as molecular bearings and cylindrical molecular capacitors [14]. Many research groups have investigated further into the electronic and structural properties of DWCNTs and have discovered that "electron-libration" coupling in certain types of DWCNTs can be utilized as a potential possibility for achieving superconductivity in MWCNTs [15]. A cross-sectional view of a typical DWCNT has been shown in Fig. 18.3b.

18.2.1.3 Single-Walled Carbon Nanotubes (SWCNTs)

As indicated earlier, SWCNTs were discovered after MWCNTs, and only after much study did certain research teams announce the synthesis of such structures. The very first SWCNTs were produced by two independent groups, which included Iijima from NEC and Donald Bethune from IBM, CA. The initial SWCNTs produced were either twisted or curled rather than straight and tubelike. With diameters of only 1 nm, they were also composed of several particles of carbon debris. Intense research on SWCNT synthesis has led to better quality yields presently. SWCNTs tend to frequently occur in arrays or tightly packed bundles. However, D.S Bethune et al. have significant findings of SWCNTs to be mostly circular. S. Ruoff and his team observed that sometimes the cylindrical symmetry of the CNTs get flattened out by the adjacent tubes due to van der Waals forces between the individual tube walls

[17]. High-resolution transmission electron microscopy images indicate that these deformations occur along the contact area over the walls between two SWCNTs. Another group from IBM, New York, has supported its findings on the effect of van der Waals forces on SWCNTs which are lying on a substrate. Their studies signify that van der Waals forces on the walls of SWCNTs resting on a substrate cause radial and axial deformations, modifying the overall geometry of each nanotube. Such deformation of the SWCNTs may have further implications on the electrical properties of adsorbed nanotubes.

A cross-sectional view of a typical SWCNT is depicted schematically in Fig. 18.3a.

18.2.2 Classification Based on Chirality

CNTs are made of graphene sheets in which carbon atoms form a perfect ensemble very similar in structure to chicken wire with carbon atoms occupying the vertices of the hexagonal unit cells. Considering the structure of an individual SWCNT as an ideal model, one can imagine its structure as a graphene sheet rolled up end to end to form a seamless tube, capped with hemispherical halves of a C_{60} fullerene molecule. While trying to understand the meaning of chirality, we neglect the caps of the nanotubes and assume the tube length is much greater than the diameter. Chirality defines exactly how much twist is present in the graphene sheet when it is wrapped with respect to the axis of the tube. In other words, chirality depends on the amount of twist introduced with respect to the axis of the tube when rolling up the graphene sheet.

The "chiral vector" can calculate the chirality for each tube. A brief explanation is provided along with a few illustrations in order to understand the procedure to calculate the chiral vector of an ideal SWCNT. Here, it is assumed that a defect-free graphene sheet, which makes up the SWCNT under examination, is spread to represent a 2D lattice structure. The lattice comprises of hexagonal unit cells, which are fused such that the combination results in a sheet. With reference to the book by Dresselhaus et al. [18], the chirality vector defines the structure of any type of tube and direction of rolling and is labeled "C":

$$\mathbf{C} = \mathbf{n}\mathbf{a_1} + \mathbf{m}\mathbf{a_2} \tag{18.1}$$

where $\mathbf{a_1}$ and $\mathbf{a_2}$ are the unit cell base vectors of the graphene sheet and n and m are the chiral indices and n > m. When the graphene sheet is wrapped, the ends of the chiral vector meet each other with the sheet forming the walls of the cylinder. Therefore, the chiral vector forms the circumference of a circular cross section of an SWCNT. The number of unit vectors in the honeycomb crystal lattice of graphene and the chiral vectors also impacts the electrical properties of SWCNTs. The diameter "d" of CNTs can be calculated using the lattice constant "a" using [19]



Fig. 18.5 Schematic representing unit cells of an armchair SWCNT structure

$$d = \frac{a\sqrt{m^2 + mn + n^2}}{\pi} \tag{18.2}$$

Different values of chiral indices can depict different types of twists in CNTs. The various types of chirality are discussed further and are furnished with illustrations. The type of chirality determines the electrical nature of CNTs. Further reading on the electrical properties of CNTs is provided in Sect. 16.2.3.

18.2.2.1 Armchair

The chiral indices "n" and "m" of an armchair SWCNT are always equal to each other, i.e., n = m for all armchair structures. A schematic representation in Fig. 18.5 depicts a 2D graphene lattice which when wrapped with a definite chiral angle produces an armchair SWCNT. Figure 18.5, which is adapted from Dr. Harris' "Carbon nanotubes and related structures" [20], depicts the armchair structure of a carbon nanotube. The rectangular box gives an idea of the orientation of the unit cells when the 2D graphene sheet is rolled along the longer side of the box as the axis of the cylinder.

18.2.2.2 Zigzag

The chiral index "m" of a zigzag SWCNT is always equal to zero, i.e., m = 0 for all zigzag structures. A schematic representation in Fig. 18.6 depicts a 2D graphene lattice which when wrapped with a definite chiral angle produces a zigzag SWCNT. The figure is also adapted from [20] and depicts the zigzag structure of a carbon nanotube when rolled up along the rectangular box as the axis.



Fig. 18.6 Schematic representing unit cells of a zigzag SWCNT structure

18.2.2.3 Chiral

All other SWCNTs which are not either armchair or zigzag are invariably chiral in nature. Any lattice pattern, which does not appear to have a mirror image, can be called a chiral CNT. Here, the hexagonal unit cells of the graphene sheet are wrapped such that they twist helically around the axis of the nanotube. Such uniqueness in its twist angle gives chiral nanotube very different electrical properties from its counterparts.

18.2.3 Classification Based on Electrical Properties

Studies have shown that the type of chirality in CNTs determines the electrical nature of nanotubes. CNTs are shown to exhibit metallic properties in armchair chirality or when (n - m) is a multiple of 3. Otherwise CNTs are described as semiconducting in nature [19].

18.2.3.1 Electrical Properties of MWCNT

Studies by Saito et al. [21] reveal interesting electrical behavior of DWCNTs. It was observed that two SWCNTs of zigzag chirality, which are inherently metallic in nature, result in a double-walled coaxial CNT, also metallic in nature when an interlayer coupling force is introduced between the two concentric cylinders. Similarly, the same hypothesis holds good for semiconducting nanotubes as well. Saito's research team along with Fujita conducted further experiments with metal-semiconducting and semiconducting-metal DWCNTs predicting that such structures also retain their original electrical character when introduced to intertubule coupling

forces. Such robustness of DWCNTs can lead to a hypothesis that they can be used as a coaxial cable with an inner conducting core and an outer insulating cladding as mentioned in Sect. 18.2.1.

18.2.3.2 Electrical Properties of SWCNT

SWCNTs can be classified based on their mode of conduction. A summary is extracted from various studies involving SWCNT energy dispersion bands leading to theoretical conclusions about their electrical behavior, and the same is provided in the next sections.

18.2.3.3 Metallic SWCNT

SWCNTs are monolayered in nature and hence do not suffer from electronic distortions occurring as a result of intertubule interactions, unlike MWCNTs. There exists a degenerate point between the valence and conduction bands at the point where the two bands cross in a normal energy dispersion spectrum of an SWCNT [22–24]. This existence of the degenerate point implies the distance between the two bands is nearly zero, resulting in high conductivity. Hence very low excitation energy is also sufficient to excite the electrons from the valence to the conduction bands. Hence all armchair SWCNTs are theoretically anticipated to behave as metallic-type nanotubes [21].

18.2.3.4 Semiconducting SWCNT

The semiconducting nature of an SWCNT is not as straightforward as that explained for their metallic behavior in Sect. 18.2.3. If the same calculation procedures are carried out for determining SWCNT's semiconducting properties, the results obtained are quite disparate. Studies have revealed that CNTs with different chiral properties exhibit different electrical behaviors [23, 25]. Consider two SWCNTs, both with zigzag chirality but having dissimilar chiral vectors (9, 0) and (10, 0). Observing the appearance of an energy gap in the energy dispersion band diagrams of a (10, 0) SWCNT, conclusions have been made that a (10, 0) SWCNT is semiconducting. On the contrary, a (9, 0)-type SWCNT is predicted to exhibit metallic conducting properties (m – n = 3×3).

18.3 Properties of Carbon Nanotubes

Their nanoscale size, unique structure, compositional elements, robustness, and immense surface area for functionalization are a few of the properties which give CNTs interesting prospects to be used in many varied applications. A brief idea about the different properties of CNTs is furnished further.

18.3.1 Electrical Properties

The electrical properties of CNTs are affected by their chirality and diameter as referred to in Sect. 18.2.3. CNTs can occur as metallic or semiconducting nanotubes. Theoretically, nanotubes are highly conductive and can have an electron density around thousand times higher than metals like copper. Although they can have stable high current densities of $J > 10^7$ A/sq-cm [26], CNTs have a constant resistivity. Phaedon Avouris, a nanotube researcher at the IBM labs, also stated in one of his lectures that current density can be pushed to a maximum of 10^{13} A/sq-cm. Owing to its nanoscale dimensions, a nanotube can be thought of as a quantum wire, through which electron transport happens ballistically.

Stefano Sanvito and his research team [27] from the School of Physics and Chemistry, Lancaster University, UK, conducted experiments on MWCNTs using a scattering technique. Their findings provided significant proof which explained the reason behind observing unexpected integer and noninteger conductance values in MWCNTs. They elaborate on how the intertubule interactions block some of the quantum conductance channels in MWCNTs and redistribute the current nonuniformly over the individual tubes across the nanotube structure, thus giving rise to quantized conductance. Trygve et al. from Harvard University conducted experiments where "counting" atoms was possible using an SWCNT-based atom detector. Counting rates of 10^4 ions/s were achieved using a 5-µm-long SWCNT. The capture of individual atoms occurred in quantized steps as seen in Fig. 18.7 below. The sharp steps resulted from the angular momentum quantization of the atoms, which are attracted toward the quantum wire. The steps observed in the "angular momentum quantum ladder" (Fig. 18.7) demonstrates quantized conductance for a neutral polarizable particle system.

18.3.2 Mechanical Properties

Experiments and intense research on CNTs have proved that they are stiffer than steel and are extremely flexible. They are very robust and can resist damage from external factors of the surrounding environment. Scanning probe microscopy studies have proved that they are very elastic since they regain their original structure after



 Table 18.1 Comparison of mechanical strengths of CNTs and common building materials,

 Applied Nanotech Inc.

Material	Young's modulus (GPa)	Tensile strength (GPa)
Single-walled nanotube	1054	150
Multiwalled nanotube	1200	150
Steel	208	0.4
Ероху	3.5	0.005
Wood	16	0.008

the stress is removed. Several research teams conducted experiments to obtain the values of Young's modulus and tensile strength of CNTs. A collection of such data is provided in Table 18.1.

The graph below in Fig. 18.8 compares Young's modulus values to compare with that of different nanomaterials.

Other groups like Wong et al. performed interesting atomic force microscopy techniques to determine Young's modulus of MWCNTs. The factor responsible for the elastic modulus of MWCNTS and SWCNTs is still being studied because of controversies in theories proposed by different research teams. While some think it is the diameter and the shape of the MWCNT which determine its elasticity, a few others claim it is due to the disorder between the many layers of the MWCNT.

18.3.3 Thermal Properties

Common results exhibited by graphite when exposed to temperature conditions must be in a way similar to the kind of behavior CNTs will probably exhibit when



subjected to the same conditions. However, since tube diameter in a CNT is orders of magnitude less than that of a unit crystal of graphite, the thermal behavior of CNTs is very different. In addition, there is increased stress induced in the CNT walls due to the increased curvature of the tube as compared to that of planar graphite. Such stress factors tend to affect thermal properties of CNTs as well. Most researchers believe that thermal properties of CNTs depend upon the amount of current passing through it. Jianwei Che and his team [29] theoretically deduced the thermal conductance of a zigzag (10, 10) CNT. Thermal conductance for such a CNT was found to be 2980 W/m-K. Berber and his team, however, provided experimental results supporting the thermal conductivity of a (10, 10) nanotube to approach 6600 W/m-K as the current applied to it is increased [30]. A recent publication by Hone et al. [31] shows that the conductivity of CNTs is large even in bulk samples, whereas aligned bundles of SWCNTs show a thermal conductivity of over 200 W/m-K at room temperature.

18.3.4 Chemical Properties

The open ends of a CNT are very susceptible to chemical agents and are sensitive to many functional groups. Functionalizing them with different chemical groups to suit certain unique applications can also chemically modify the walls of a CNT. Properties like a high surface area for functionalization give them important applicability in sensor devices and electrochemical device applications. Prof. Kwanwoo Shin from Sogang University in Korea and his team have been conducting experiments to study the effects of high-intensity radiation on CNT-based electronic devices like transistor networks.

18.4 Applications

Researchers have proposed many plausible applications for carbon nanotubes ever since their discovery a decade ago. Although applications like hydrogen storage still remain debatable, most applications have revolutionized certain sectors of the IC in the industry. Their high current carrying capacity, high thermal conductivity, and mechanical stability make them good interconnect material in electrical circuits. Carbon nanotubes are qualified to be used as carbon composites for strength enhancement in fabrics and building material. Common sports equipment like golf balls, baseball bats, and tennis racquets are made lighter and stronger by integrating them with CNTs. Scientists have also proposed the probable usage of CNTs while building space elevators. Rapid advancements have been achieved in manufacturing field emission displays with carbon nanotubes. Properties like sharp geometry, mechanical strength, and electrical conductivity have been exploited to make AFM and STM tips mounted with CNTs improving resolution drastically. One of the most fascinating applications lies in implementing carbon nanotubes in making sensors.

18.4.1 Sensors

Nanomaterial-based sensor systems of the future will radically improve in their sensitivity, selectivity, and rapid response criteria. These new age detector systems equipped with better control and cross-examination features will not only be capable of single molecule detection but also multiplexed detection of diverse signals necessary for diagnosing various analytes. Carbon nanotubes are being used as chemical, gas, and biological sensors. The main advantage behind CNT-based sensors is the miniscule amounts of sensing material needed and an equally small amount needed for the purpose of sensing. Although most CNT sensor devices use the same sensing material, they differ in their sensing mechanisms and detection schemes. While some sensing mechanisms depend on mechanical properties of carbon nanotubes, others rely on their electronic transportation processes. Detection schemes on the other hand can vary from being optical or mechanical to observing variations in the overall frequency response of the sensor device. Although optical detection schemes are still evolving, electrical detection is more desirable due to its increased reliability. The electronic industry has incorporated CNTs while manufacturing semiconductor devices. Such CNT amalgams have been used as sensing material for various sensor applications. Most commonly, an interdisciplinary team of researchers is required to build sensors, since expertise in all sciences is required to develop a working sensor, which is commercially viable. The following sections provide a brief insight into a few state-of-the-art CNT-based sensor systems.

18.4.1.1 CNTs as Biological Sensors

Rolled up seamless layers of graphene sheets in cylinder formats make CNTs to exhibit excellent physical, chemical, electrical, optical, and mechanical properties which can be leveraged toward design of biological sensors [32]. Motivated by its unique properties and quasi-1D structure with more densities of states and multiple binding sites for ligand functionalization, today biological applications of CNTs span both in vivo and in vitro spectrum of healthcare [33]. The availability of dangling bonds on its outer surface provides binding sites for functionalized molecules either through covalent or π - π stacking along the length of CNTs [34]. Functionalization renders CNTs' conditions favorable to interact with biological molecules and low toxicity, the essential factors for a biosensor design.

Current flow in one-dimensional structures like CNTs is extremely sensitive to even the slightest changes occurring on its charge carrying outer surface. Hence when biological analytes adsorb on the CNT walls, this binding event perturbs normal charge transport in the quantum wire. CNTs are thus an ideal sensor material for most applications. CNT-based biosensors comprise one of the most important real-life applications of CNTs. These nanoscale sensing elements prove extremely sensitive and selective in many varied applications. Vast research is being conducted on CNTs in order to probe deeper into their applicability. CNTs have attracted attention for defense applications because of their ability to sense trace amounts of deadly biological agents and hence fight global terrorism. The cost of medical diagnostics and the time consumed for tiresome lab routines for diagnosis can be avoided by using nanomaterial-based sensors. Nanomonitors based on CNT sensing elements are being developed instead to hasten diagnosis.

Single molecule detectors using CNTs are being developed at the University of Illinois at Urbana-Champaign. Coated CNT-based sensors fluoresce when they come in contact with the target molecule, and the wavelength of such emissions is recorded to analyze the trapping of the target molecule. Sofia et al. [35] have developed an amperometric biological sensor with aligned MWCNTs on a platinum substrate. CNTs display a dual role in this sensor by acting as a good medium by providing large surface area for immobilization of functional groups and as a medium for electron conduction.

DNA sensors have been developed and are under extensive study due to their vast applicability in the field of forensic science, genetic engineering, and gene therapy. Covalent functionalization of CNTs involves formation of carboxyl groups. Zheng et al. observed that CNTs become soluble in water following oxidation, thus making them unsuitable for biological applications due to the high salt content of physiological buffers [33]. Selecting a functional molecule which does not alter the intrinsic properties of CNTs as well permits robust loading characteristics as key for biosensor design. Cai et al. [36] functionalized MWCNTs with a carboxylic group for the detection of a specific hybridization. This MWCNT-based DNA sensor demonstrated better charge transport characteristics and functionalization ability than an earlier model of a DNA sensor with carbon electrodes directly functionalized with oligonucleotides.

18.4.1.2 CNT FETs Gas Sensors

Section 16.4.1 briefly illustrates a few methods developed by research teams to devise gas sensors. These methods involve using CNTs as either nanocomposites or single CNT-based sensor devices. Interest in producing CNT field-effect transistor (FET)-based gas sensors is also rising since CNTs can act as excellent transducers owing to their large charge sensitive surface area. This property of high surface area makes CNT FETs sensitive to ambient environments, especially to oxygen and oxygen-containing compounds [37, 38]. Research by Tans et al. [39] has shown that SWCNTs synthesized by the chemical vapor deposition technique were used to fabricate FETs with channel lengths of 2.5 µm and 5 µm to detect alcoholic vapors. Detection is dependent on observing changes in the FET parameters like saturation current and threshold voltage, and this was achieved for a wide range of alcoholic vapors when the entire device is exposed to an alcoholic vapor environment. Most FETs suffer from a conductance limitation due to the Schottky barrier created in the CNT-metal interface. In order to overcome this current carrying limitation, Ali Javey et al. [40] incorporated palladium on the sensor to interface with the SWCNTs. As a noble metal, palladium acts a better wetting substance for the CNTs, thus reducing the charge barrier for electron conduction and improving current. CO₂ is a common gas, which is associated with most biological processes. Sensing CO₂ for domestic use is also important in many public access areas. Many researchers have undertaken research on CNT-based sensors already. However, a few research teams like Alexander Star et al. [41] constructed a CNTFET to detect CO₂. They have reported the use of chemically functionalized CNTs with a specific recognition layer for CO₂ sensing. They employed a polymer coating method for functionalizing unlike other studies, in order to overcome modification of the physical properties of CNTs due to covalent bonding.

The following reading will provide information about more traditional CNT-based semiconductor devices. It gives us an idea of devices, which the IC industry is trying to incorporate in the current technology to either improve certain features of an existing technology or to devise an entirely new strain of technology, based on CNTs.

18.5 CNT with Single Junction

18.5.1 Schottky Diode (CNT: Metal Junction)

The contact formed at the metal-nanotube interface behaves as an electrical Ohmic contact or as an active junction (Schottky diode). The nanotubes make several different types of contact to the metal; of these the configuration with side contact, where CNTs positioned on metal contact by weak van der Waals forces and end-bonded CNTs that are connected to the metal by covalent or metallic bonding,



Fig. 18.9 Two types of nanotube/metal contacts: (a) CNT side contacted through the weak van der Waals adhesion. (b) CNT end bonded to the metal by covalent or metallic bonding. (Redrawn from Leonard and Tersoff [42])

reduces dimensionality. They have a strong effect on active device formation. Fermilevel pinning plays an important role in formation of these devices. Figure 18.9 shows the two different types of CNT and metal contact by two different bonding mechanisms.

18.5.1.1 Fermi-Level Pinning

The barrier height at the planar interface due to Fermi-level pinning is independent of metal work function given by

$$\phi_b = E_c - E_F \tag{18.3}$$

where E_c and E_F are the energy conduction band edge and Fermi level.

In addition, the energy band diagram indicates negligible band bending characteristics due to doping near the interface [42].Now considering the planar interface between metal and semiconductor, the barrier height that is dependent on the metal work function is given by

$$\phi_{b_0} = X_m - X_s \tag{18.4}$$

where $X_{\rm m}$ and $X_{\rm s}$ are the metal work function and semiconductor ionization potential.

However, there is a finite density of states at the metal-semiconductor interface inside the bandgap of the semiconductor. These bandgaps have a complex wave function that is called "metal-induced gap state" (MIGS). This wave decays exponentially into the semiconductor due to the boundary condition at the interface with the metal. Therefore the induced charge at the interface due to MIGS creates a dipole ring or sheet at the interface. This charge changes the position of the Fermi level, thereby raising or lowering the barrier where the charge near the semiconductor surface vanishes, and MIGS controls both the turn-on voltage and the band bending of the device. The barrier height is independent of the metal/work function and is dependent on the pinned Fermi level deep inside the semiconductor energy bandgap.

18.5.1.2 CNT Devices with Planar Interface

For CNTs with the planar interface, the charge is modeled by a dipole and is given by

$$\sigma(z) = D_0 (E_N - E_F) e^{-qz}$$
(18.5)

where D_o is the density due to MIGS, and E_N is the neutrality level which depends upon the atomic structure level which varies with z due to the electrostatic potential. E_F is the metal Fermi level and z is the distance from the metal-NT interface. q represents the average exponential decay value due to all the states in the bandgap because of charge in the metal and due to MIGS at the interface. Leonard et al. demonstrated this in their work [42].The barrier height is increased to

$$\phi_b = \phi_b^0 + E_F - E_N \tag{18.6}$$

In the schematic diagram [41] for the planar Schottky barrier, charge neutrality level is at the center of the semiconductor bandgap, and the metal Fermi level is located at the midgap. Figure 18.10 shows a schematic diagram of the CNT planar interface devices.

18.5.1.3 CNT Device with Round-Ended Interface

Round end-bonded contacts between CNTs and metal are similar to the traditional planar contact where the semiconductor ends at the metal. For studying the Fermilevel pinning in this type of contact, it has to be taken into consideration that the MIGS is a dipole ring instead of a sheet. Therefore it has an overall effect of electrostatic potential and band bending. The electrostatic potential decays as the

Fig. 18.10 Schematic representation of CNT device that forms a Schottky barrier at planar interface between CNT and metal by weak van der Waals force. (The figure is redrawn from Anantram and Léonard [43].)



third power of the distance from a dipole ring [43]. There is rapid exponential decay of potential that vanishes after a few nanometers. Thus, as the barriers are a few nanometers in size, the electrons tunnel through them, with the result that Fermilevel pinning has a less significant effect on the end-bonded CNT/metal contacts. In summary, it can be concluded that the type of contact produces different work functions that play an important role in device formation. The fabrication of the round end-bonded Schottky junction between CNTs and metal (Ti and Si) has been demonstrated [44].

18.5.1.4 Schottky Versus Ohmic Contact

The presence of Schottky barriers at these contacts gives a measure of temperature dependence of the current, where the current increases with the temperature. This is in contrast to Ohmic contacts where the temperature dependence is opposite, i.e., the current decreases with an increase in temperature.

18.5.2 CNT-Based p-n Junction Diode

The p-n junction CNT diode shows rectification behavior, i.e., current-voltage characteristics with forward conduction and reverse blocking characteristics similar to the semiconductor diode. For CNTs the characteristics of the p-n junction depend on certain parameters: the dielectric constant of the material that it is embedded into, the doping fraction, D(E,z) the CNT density at z position, and the Fermi function F(E). This can be explained by Eq. (18.7), where the CNT charge density is given by

$$\sigma(z) = \frac{e}{\varepsilon} f - \frac{e}{\varepsilon} \int D(E, z) F(E) dE$$
(18.7)

And the density of states is given by

$$D(E,z) = \frac{a\sqrt{3}}{\pi^2 R V_0} \frac{|E|}{\sqrt{(E+eV(z))^2 - (E_g/2)^2}}$$
(18.8)

where:

R – CNT radius Vg – energy gap V(z) – electrostatic potential

Based on these equations, it was determined that the same band bending characteristics [45] are observed in planar p-n junction devices for different doping fractions. As the screening of coulomb interaction is ineffective in one-dimensional



CNTs, the charge distribution curve logarithmically decays away from the junction. There is a need for adding continuous charge to avoid dropping potential and to maintain the potential constant away from the junction. This phenomenon occurs due to the electrostatic dipole rings, in contrast to the dipole sheet as seen in the planar devices, whereas in a normal planar device, there is a constant charge near the junction, which vanishes outside the depletion region.

The same behavior is observed in a Schottky planar junction between a metal and CNT. Figure 18.11 is redrawn showing the charge distribution at the interface of metal and CNT [9].

Figure 18.12 shows the depletion width of a CNT with respect to doping fraction. As the doping fraction reduces, the depletion barrier decreases, thus creating a tunneling effect due to the reduced barrier and giving rise to negative differential resistance devices [46].

The calculated I–V curve demonstrates a negative differential resistance curve plotted using Eq. 18.7. The negative differential resistance is calculated by Eq. (18.9):

$$I = \frac{4e^2}{h} \int T(E) [F_L(E) - F_R(E)] dE$$
(18.9)

where T(E) is the transmission probability across the junction and FR(E) and FL (E) are Fermi functions in the right and left leads, respectively.



18.5.2.1 p-n Junction Depending on Type of Doping

The doping is controlled by the introduction of dopant atoms and charge transfer by metallic electrodes and hence determines the device characteristics. There are two types of doping:

- 1. Electrostatic doping
- 2. Chemical doping

18.5.2.2 p-n Junction: Electrostatic Doping

The electrostatic doped p-n junction shows an ideal device characteristic, whereas chemical doped shows electrical properties that result in the leaky behavior due to high doping concentration and abrupt junction formation. In this device, the gate voltage controls the doping strength. This is accomplished by fabricating two identical back gate electrodes [47] (Fig. 18.13).



18.5.2.3 p-n Junction: Chemical Doping

Rectifying p-n junction bipolar diodes are formed by modulated chemical doping of the CNTs [48]. This is performed by catalytically patterning CNTs onto SiO₂. The CNTs are formed as p-type due to an absorbed oxygen molecule from the atmosphere. The n-type CNT on the other hand is made by adding a poly(methyl methacrylate) (PMMA) layer on the first half p-type CNT, exposing the other half to potassium dopant (K) in vacuum. The potassium dopants are produced by electrical heating of the potassium source. The devices were fabricated by Zhou et al. in 2000 [48]. Figure 18.14 shows the layout diagram of this device.

18.5.3 CNT Metal-Semiconducting Junction

Rectification diodes are formed by crossing metal and semiconductor CNTs [49] and by the formation of a kink-shaped intramolecular junction [50, 51]. The device characteristics of cross metal-semiconductor and intramolecular junction devices were demonstrated by M. S. Fuhrer et al. (2000) and T. Yamada et al. (2002), respectively.

18.5.3.1 CNT Crossed Metal-Semiconducting Junction

In the CNT crossed metal-semiconducting (MS) junction, rectification is shown as both the CNTs show the same graphene band structure thus having identical work functions. The metallic work function should align in between the bandgap of the semiconducting CNT. Thus, in both the cases, the Fermi level is in the middle of the CNT bandgap and is at the same energy as the Fermi level in a metallic tube. This leads to the presence of a Schottky barrier at the crossing point between the two



CNTs. In addition there is a barrier height approximately equal to half the bandgap of the semiconductor CNT. This is due to barrier height associated with the depletion region. The nanoscale depletion region acts as a leaky tunneling barrier. The Schottky barrier in three-terminal MS junction devices offers a rectification to form a p-n junction Schottky metal-semiconductor diode. The device characteristic shows a nonlinear rectification behavior for metal-n-type semiconductor junction due to the Schottky barrier. Figure 18.15 shows the schematic representation of the device fabricated.

18.5.3.2 Intramolecular Metal-Semiconducting CNT Junction

The intramolecular semiconductor-metal junctions [52] are fabricated by introducing the pentagon and heptagon carbon ring defect pairs by mechanical deformation. The 5–7 pentagon-heptagon pair is placed onto the opposite side of the CNTs to have a large caplike angle of curvature. A sharp kink of 40° was observed [53]. The device characteristic is shown in Fig. 18.16.

The junction formed causes the rectification behavior rather than the electrode contact. The I–V characteristics are similar to the p-n junction diode at room temperature.

18.6 Field-Effect Transistors (FETs)

FETs [54] are generally fabricated using semiconducting CNTs. The nanoscale CNT-based FET shows different characteristics than the traditional microscale semiconductor-based FET. The CNTs are bridged between two electrodes, and the Si substrate is used as a back gate, which controls the switching action for the transistor. The drain current versus drain voltage characteristics is studied for the transistor. When the gate voltage is varied from negative to positive, the CNT conductance characteristics are modified from high to low. The transistors are classified based on the type of contact and the doping profile.

18.6.1 Classification Depending on Types of Doping

18.6.1.1 Unipolar CNT Transistor (P-Type or N-Type)

The absorption of oxygen molecules onto CNTs results in the formation of p-type tubes. The transistors fabricated with these CNTs show unipolar p-type behavior. The transistor-doped holes show no electron transport at the high positive gate voltage, which results in a high Schottky barrier at the metal-semiconductor interface. This is due to the maximum Fermi-level pinning near the valence band at the nanotube-metal interface. The n-type CNT is very essential in complementary logic devices and circuits. The p-type CNT can be converted into n-type by doping the CNT surface chemically by alkali metal or by the simple method of annealing in vacuum and in an inert gas. The annealing modifies the Schottky barrier height at the contact due to adsorption of oxygen. In doping, barrier thickness is changed, and there is a shift in the threshold voltage [55].

The figure observed by Avouris (2002) [55] shows the transfer characteristics produced by annealing and by doping the CNT with potassium metal. First the n-type unipolar device is fabricated using thermal annealing, and then oxygen is introduced at each step. It was observed that as the oxygen is increased, the current at the positive bias decreased and increased at the negative bias.

The behavior of the n-type transistor produced by potassium doping is different from the annealing process. At low doping, there is shift in the curve toward the more negative bias voltage. The device doesn't show any ambipolar behavior as there is no significant current during the intermediate doping. During the high doping, there is an increase in the current flow in the device.

18.6.1.2 Ambipolar CNT Transistor

During the addition of oxygen, at an intermediate step, the transistor behaves as an ambipolar transistor. There is conduction of holes and electrons depending upon the

gate bias. An ambipolar device [37, 56] is hole conducting (p-channel) when the gate bias is sufficiently negative and electron conducting when gate bias is sufficiently positive (n-channel).

18.6.2 Classification Depending upon Type of Contact

18.6.2.1 CNT Transistor with Ohmic Contact

The CNT transistors are studied by taking zero-bias conductance into consideration. The zero-bias conductance is given by

$$G = \frac{4e^2}{h} \int P(E) \left[-\frac{\partial f(E)}{\partial E} \right] dE$$
(18.10)

The conductance characteristics and band bending curves are plotted by using the conductance equation by Leonard et al. [57].

The plot shows three regions of interest. The traditional transistor behaves in only two regions, i.e., on off state, i.e., I and II region. At high negative bias voltage, the device exhibits high conductance. This corresponds to the ON state of the transistor. As the voltage is increased, the conductance drops to zero, and the device turns into the OFF state. This is analogous to the conventional transistor. Region III is observed only in the CNT-based transistor and is a gate resonant tunneling effect. This is due to the tunneling through the localized states in the CNT with the coulomb blockade showing a negative differential resistance.

The band diagram explains the behavior of the transistor. At a low voltage, the metal work function is high, and the Fermi level is below the valence band. Therefore there is a hole transport in the channel without any barrier. Thus the conductance is very high. As the gate voltage increases, the band is pulled down creating a barrier for hole transport, conductance drops to zero, and the transistor is in the OFF state. The third region shows interesting behavior. Gate voltage is increased; the conduction band is pulled down into the bandgap creating an electrostatic quantum dot with a discrete localized state. The electron can tunnel through the quantum dot showing a sharp conductance peak at high voltage as explained earlier giving rise to strong negative differential resistance.

To summarize, in both the conventional and the CNT FET, the current saturates due to an increase in the drain voltage. The saturation is due to "pinch-off" in normal transistors, whereas the current is limited by the number of carriers (holes or electrons) from the leads for CNT FETs. The presence of the resonating effect is observed only in the CNT transistor.

18.6.2.2 CNT Transistor with Schottky Contact

When the barrier is predominantly Schottky, the transistor operates as a Schottky barrier (SB) transistor. The switching is due to the contact resistance rather than the channel conductance. There is also a significant change in band bending as compared to the Ohmic contact transistor. The metal/nanotube contact and the applied voltage determine the performance of the Schottky CNT FET.

The band diagram shown by Avouris et al. [58] demonstrates sharp band bending near the contact due to the Schottky barrier instead of the observed CNT properties. Due to the sharp band bending, electrons can tunnel through it leading to a sharp increase in the current. In the ON state, the band is raised up, and the hole carrier tunnels into the valence band due to the reduced tunneling distance. With the increase in gate voltage, the valence band is pulled down, creating a large tunnel barrier approximately equal to the channel length, making it impossible for the holes to reach the other end of the contact, thus allowing the transistor to operate in the OFF state. Here, it is also observed that the metal Fermi level is at the center of the valence and the conductance bands, thus creating a large SB. This transistor therefore operates as a SB FET. If the SB is small, the device works as the normal conventional FET. FET devices fabricated this way show sharp increases in the conductance as the gate voltage is varied, indicating the presence of a Schottky barrier at the contact of the device. The Schottky contact-based CNT FET [59, 60] operates differently than the conventional transistor or the Ohmic contact CNT FET.

18.7 CNT-Based Single-Electron Transistors

The molecular quantum CNT wire-based transistors are known as single-electron transistors [61]. They consist of conducting islands connected by tunneling barriers to two metallic electrodes. If the temperature and bias voltage are less than the energy required to add an electron to the island, the device is in the blocked state. It is generally observed only in (n, n) armchair metallic CNTs. The quasiperiodic series of sharp peaks are observed in the conductance versus gate voltage curve. The device characteristics show coulomb blockade and also indicates the coulomb charging of CNTs when the contact resistance is larger than the quantum resistance h/e² and the capacitance of the device is low enough to have significant charging energy due to the addition of a single electron.

The peak spacing is given by

$$\Delta V_g = (U + \Delta E)/e\alpha \tag{18.11}$$

where:

 $U - e^2/C$ is the coulomb charging energy for every single-electron addition in the dot ΔE – single-particle level spacing



- α Cg/C the rate of change of electrostatic potential of the dot due to the change in applied back gate voltage
- C, Cg total capacitance of the dot and the capacitance between dot and back gate electrode, respectively

The peak amplitude of an isolated peak is approximately equal to e^2/h . where e and h are the electronic charge and Planck's constant, respectively. The rationale for the SET characteristics is as follows in Fig. 18.17.

The band energy diagram in Fig. 18.17 shows the relation of gate voltage Vg and drain voltage V. The dot is filled with the N electrons and the energy separation of U + ΔE for adding the (N + 1)th electron to the excited single-particle state. The above levels are evenly spaced with ΔE . The high conductance coulomb blockade peak is due to the alignment of the Fermi level of the metal contact with the lowest empty energy state, thus allowing single-electron tunneling through the dot at V = 0. The low conductance valley indicates suppression of electron tunneling due to the singleelectron charging energy U. The voltage V dependence can be observed that as the voltage V is increased, the right-hand contact is pulled below the energy level of the highest electron filled state allowing an electron tunneling giving rise to a conductance peak. With the additional increase in voltage V, the contact is further pulled down below the highest filled state allowing additional electron tunneling from the additional state resulting in generation of additional resonating peak conductance. It is also observed [63] that the height of the conductance peak is dependent on the temperature. There is reduction in height and broadening of the peak as the temperature is increased. The conductance peak is held constant with increasing temperature if the density of the states is continuous as seen in the bulk semiconductor devices.

In summary, nanoelectronic devices using CNTs have more control and improve electrical characteristics over a normal operating condition. However, they show quick degradation outside the regular operating condition.

18.8 Integrated Device Fabrication

18.8.1 Nonvolatile Random Access Memory

Nonvolatile random access memory (NRAM) [64] is a high-density electrostatically switchable wire array memory module. The molecular-scale device structure consists of a crossbar array formed by groups of CNTs on the substrate and groups of perpendicular CNTs suspended on a periodic support array. The bistable ON/OFF principle at the cross-points is related to the two minima observed on the total energy versus distance curve. The total energy equation is given by

$$E_T = E_{vdW} + E_{elas} + E_{elec} \tag{18.12}$$

where E_T is the total energy of the single crossbar device element, E_{vdW} is the van der Waals energy, E_{elas} is elastic energy, and E_{elec} is electrostatic energy. The ON state is determined by the minimum (vdW) force observed due to contact between two CNTs, and the OFF state is determined by the minimum elastic energy observed when the distance of separation is finite. Figure 18.18 shows the schematic diagram of the NRAM, and Fig. 18.19 shows the total energy diagram at each crossbar junction element indicating the ON and OFF state.

In addition, there is a significant variation in the resistance value due to reversible switching under normal ambient conditions at room temperature. The resistance values associated with the device ON/OFF state is observed in Fig. 18.20. The ON and OFF resistance is approximately 140 M Ω and 1.36 G Ω , respectively. The resistance value is in the higher range (M Ω -G Ω) due the large contact resistance which is generally observed between the CNTs and the metal contact [65].





Fig. 18.19 The graph illustrates the total energy versus the distance of separation curves indicating the minimum energy for (a) ON state and (b) OFF state. (Redrawn from Léonard and Tersoff [57])



This NRAM module shows promise in the next-generation semiconductor electronic world. Rueckes et al. have a patent number 6706402 for the NRAM technology. It was developed at Nantero Inc., Woburn, MA, USA.

18.9 Limitations to Carbon Nanotube Technology

Nanotechnologists all over the world are exploring various aspects of research ranging from the fundamental material research to their applications. Nanotechnology thrives due to the extensive interest shown by both academia and industry. In this chapter we have focused on one type of nanomaterials, i.e., carbon nanotubes. This material has ubiquitous applications in the current sociopolitical environment: it promises improvement in current defense applications like fighting biological agents

and making traditional weapons more effective. Clinical diagnostics have experienced a large-scale makeover in most of its detection schemes, which are faster, multiplexed, portable, and more reliable.

Carbon nanotube technology has also been receiving extensive attention in making cutting-edge sensor technology (see Sect. 16.5.1) and semiconductorbased devices, but despite its numerous applications, it suffers from a few drawbacks. Like most other nanomaterial-based device technologies, it faces the problem of interfacing the nanoscale sensor materials and macroscale measurement systems. Although CNTs have shown promising results with respect to their electrical properties, integrating them with realistic electric circuits remains a challenge owing to the difficulty in alignment of these nanoscale structures in the desired positions. A method to mass-produce CNTs has not been established yet, and the current means to do so involve using expensive manufacturing equipment. Synthesizing CNTs of predetermined diameters and chirality remains the biggest challenge of all. Microscopy equipment is not only uneconomical but suffers from technical limitations since imaging requires expertise and involves cumbersome techniques to achieve perfection. High-intensity electron/ion beams used in different electron microscopes might burn out CNTs to form amorphous carbon while attempting to improve resolution. Transmission electron microscopy involves elaborate and difficult methods for sample preparation. It is capable of giving a good idea about the diameter of a CNT but can provide only limited data related to CNT chirality. Probing a single unidimensional wire like a CNT requires expertise and sometimes a good amount of fortune! Invasive techniques involving carbon-based nanoscale substances like CNTs for use in biological analytes has been believed to be hazardous to health of the living organism under examination.

Despite many disadvantages, fruitful research is being pursued with newer and better reasons to incorporate CNTs in most state-of-the-art nanoelectronic devices.

18.10 Nanopackaging

Producing reliable systems which maintain good signal integrity and are economy friendly are two important aspects for both the manufacturer and the buyer. The manufacturing industry thrives on making low-voltage, high reliability, and high-speed systems, which can be integrated with future devices. When such is the goal, as discussed in the previous sections of this chapter, traditional sensor devices based on CNT composites for gas detection and CNT arrays for biomolecular detection are highly sensitive to the agents under examination, even to the concentration levels of 1 ppb. Such sensitive systems behave quite differently under laboratory conditions. When being made commercially viable, however, care has to be taken that sensor systems are properly packaged in order to protect the sensor material from external contamination. Manufacturers need to take care of not only biological type of contaminants but also electrical. Stray electric charges from other instruments or a static discharge from the person handling the device are also potential threats to

unpackaged devices. The electronics linking the sensor element to the measurement systems must also be packaged well to avoid corruption in the sensitive signals that are exchanged between them. CNT-based semiconductor devices also require nanopackaging.

Nanopackaging for nanomaterial-based semiconductor devices is done in two levels: wafer packaging and system board level. Wafer-level packaging uses nanomaterials to bring about improvements in the electrical, thermal, and mechanical properties in the chip to package interconnections. The advantages of waferlevel packaging are the small size and low cost of the product. These added benefits of wafer-level packaging are because the package size is only a little more than the actual device itself, and it costs less since all interconnections are done at this level in one parallel step. Such devices are also faster since there is reduced interconnect lengths. System-level packaging on the other hand deals with packaging the entire device after wafer-level packaging, to the various measurement systems. Systemlevel packaging requires matching of components and making compatibility possible between all kinds of measurement systems, thus making the device portable. Portability however brings with it the risk of contamination and damage to the device. Nanopackaging ensures both rigidity and resistance to contaminants.

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Chapter 19 High Electromagnetic Shielding of Plastic Transceiver Packaging Using Dispersed Multiwall Carbon Nanotubes



Wood-Hi Cheng, Pi Ling Huang, and Chia-Ming Chang

19.1 Introduction

The widespread deployment of low-cost optical access networks for fiber-to-thehome (FTTH) applications will necessitate a considerable reduction in the cost of key components such as optical transceiver modules. Optical transceiver module costs are primarily dependent on their packaging. Owing to its low-cost nature and ease of manufacture, the plastic packaging technology has been considered as one of the major choices for reducing the costs of fabricating optical transceiver modules for use in the FTTH applications [1-5]. However, plastics alone are inherently transparent to electromagnetic (EM) radiation, and hence provide no shielding against radiation emissions. To improve the EM shielding for the plastic packaging, electronic conductive properties have to be added into the plastic hosts for adequate EM shielding. The currently available techniques for preventing EM interference (EMI) or EM susceptibility (EMS) shielding include conductive sprays, conductive fillers, zinc-arc spraying, electro-plating or electrolysis-plating on housing surfaces, modifications of electrical properties during the molding stage, and other metallization processes. Among these methods, the most popular one for EM shielding is to compound plastics with discontinuous electronic conductive fillers, such as metal particles, metal flakes, stainless fiber, graphitized carbon particles, graphitized carbon fibers, metal-coated glass, and carbon fibers [6, 7].

Experimental evidence has shown that the carbon fibers with an aspect ratio of 1000 are good conductive fillers for providing a high EM shielding [8, 9]. Optical transceiver modules employing nylon and liquid crystal polymer (LCP) reinforced with carbon fiber showed that the measured shielding effectiveness (SE) was over

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20 dB with 25% of weight percentage of the carbon fiber mixed in the nylon and LCP composites [3, 4]. In addition, the SE performance will be higher for higher weight percentages of the carbon fiber and thicker material of the carbon-fiber mixture. However, with such plastic composites, the dominant cost of the package is the carbon-fiber fillers. Therefore, developing a plastic composite housing with a low weight percentage of carbon fiber and with good shielding ability is necessary for fabricating a low-cost and high SE optical transceiver module. Recently, low-cost, lightweight, and high EM shielding package for the optical transceiver module has been made by employing the woven continuous carbon-fiber (WCCF) epoxy composite with the compression molding technology [4, 10]. Epoxy resins are one of the best matrix materials for carbon-fiber composites because they adhere well to a wide variety of carbon fibers. By weaving the continuous carbon fiber in a balanced twill structure (BTS) with excellent conductive networks, it was found that the SE of the package housing, while keeping a very low weight percentage of carbon fiber, can reach about 80 dB under the far-field source measurement and about 25 dB in the near-field source measurement [4, 10].

As the electronic and mechanical properties of carbon nanotubles (CNTs) are remarkable [11, 12], CNTs have been the focus of considerable research and development for use in nanoscale electronic and optoelectronic applications, such as integrated circuit (IC) interconnections [13], optical emission devices [14], and electrical interconnect [15–17]. CNTs are also considered as one of the electronic conductive fillers for EM shielding of transceiver-package applications because of their smaller diameter, higher aspect ratios, higher conductivity, and better mechanical properties [18, 19]. The aspect ratios of most CNTs could be higher than 1000, which offers a good condition to form overlapping conductive CNTs networking, to provide a high EM shielding. The electrical percolation behavior of the polymerbased CNT composites is also discussed in the literature [20-23]. The electrical conductivity changes dramatically, when the concentration is around a threshold value. Once the concentration is higher and away from the threshold, the conductivity increases slowly. The threshold value is usually small and less than 0.9 wt% of the CNT composite in thin film [22]. The low percolation threshold results from the homogeneous dispersion of CNTs in the matrix and the high aspect ratio of CNTs. For thick layers of the polymer-based CNT composites, the percolation threshold phenomenon usually becomes more complex, and the dispersion of CNTs in the composite may become more difficult.

According to basic EM shielding theory, the SE increases as the material conductivity increases [18, 19]. Multiwall carbon nanotube (MWCNT) means a tube with many CNTs inside. The more polymer-based MWCNT material is added, the more overlapping conductive MWCNT networking, and hence the higher conductivity and the higher SE are expected. However, the high aspect ratio and low ionic character of MWCNTs are not easily dispersed within the plastic hosts. The lack of dispersing ability in the polymer matrices is caused by internal van der Waals' force among the MWCNTs and their consequent aggregation [24–26]. Without fine dispersion, the MWCNTs may form local clusters and poor homogeneity would exist in the MWCNT composite. As a consequence, added MWCNTs are required increasing the weight percentage in order to achieve good electrical conductivity and comparable SE. For developing a cost-effective material, fine dispersion of MWCNTs in the polymer matrix is essential. Recently, finely dispersed MWCNT composites have demonstrated [27] a remarkable SE improvement in comparison with previously reported non-dispersed MWCNT composites [18, 19] and comparable to the results reported by Kim [28, 29]. This indicates that the fine dispersion of MWCNTs is the dominant factor for fabricating higher conductive materials. Packaging with film composites with low weight percentages of dispersive MWCNTs [18, 19]. The proposed dispersed MWCNT composites may be suitable for packaging low-cost and high-performance optical transceiver modules for use in the FTTH lightwave transmission systems.

In this chapter, a novel polymer-based MWCNT with high SE and effective electromagnetic susceptibility (EMS) performance is proposed for use in packaging a high-speed 2.5 Gbps plastic transceiver module. Both polymer-based dispersed and non-dispersed MWCNT composites are fabricated and then the SE performances are compared. The sections of this chapter are organized as follows. Section 19.2 describes the fabrication of dispersed and non-dispersed MWCNT composites. The measurement results of SE for plastic composites at a far-field source and for realistic package at a near-field source of the monopole type are presented in Sect. 19.3. Section 19.4 represents the shielding effectiveness and EMS performance of an optical transceiver module. Conclusions and discussion are given in Sect. 19.5.

19.2 Fabrication of MWCNT Composites

19.2.1 Material Properties of MWCNTs

CNTs have excellent characteristics in both mechanism and electricity, such as a high yield strength, a high current density, a high electrical conductivity, and less heat dissipation [12]. Basically, a CNT is a hollow tube, which is constructed from carbon atoms. This kind of hollow structure of carbons is called fullerene. Usually, fullerenes consist of hexagons and pentagons that form a spherical shape. The most famous one is C_{60} , which is built by 60 carbon atoms [12]. A CNT is a fullerene, but it is in a long hollow tube structure and its ends are semispherical-shaped cups. The tube wall atoms are hexagonally bonded like graphite and the tube-tip atoms are mixed with hexagonal- and pentagonal-bonded-like C_{60} [12]. Basically, it explains the origin of the high strength and excellent electrical characteristics. The CNT has a high mechanical strength and a large aspect ratio. The latter aspect makes it suitable as a filler of plastic composite for conductive networks, which contribute to an increase in the conductivity of the composite for EM shielding purpose.

MWCNT means a tube with many CNTs inside. These CNTs include metallic and semiconducting properties. And the CNTs inside a MWCNT could be


Fig. 19.1 (a) SEM photograph of MWCNTs. (b) TEM photograph of MWCNTs

concentric or spirally spread. A MWCNT with both metallic and semiconducting CNTs inside is also metallic conductive [30], which can be used as a conductive filler to make plastic composites. In this study, the MWCNT is produced by the arc-discharge deposit method (ADM) [31]. The electrodes are graphite rods with a distance about 1–2 mm apart. The applied voltage is 15–30 V, the operated dc current is around 50–150 A, and the applied argon gas pressure is 500–760 mbars. The deposit at the cathode includes 25% MWCNTs, 10% carbon nanocapsules, and 65% amorphous carbon. The aspect ratio of these MWCNTs is about 200–500 under scanning electron microscope (SEM) observation. The MWCNTs produced by ADM are not like those produced by a chemical vaporization deposit (CVD) method where metal-catalyst particles exist. The metal-catalyst particles such as Fe and Co will influence the conductivity, which has been reported by Kim's group [28, 29]. The MWCNTs are needle-like, sticking out of many hollow carbon nanocapsules as shown in Fig. 19.1a. Figure 19.1b shows a transmission electron microscope (TEM) photograph of MWCNTs, which illustrates the multilayer CNTs.

19.2.2 Material Properties of Non-dispersed MWCNT-LCP Composites

The polymeric materials applied in this study are liquid crystal polymers (LCPs) [9]. The LCPs exhibit a highly ordered structure in both the melt and solid states and are often applied to replace materials such as ceramics, metals, composites, and other plastics, because of their outstanding strength at high temperature and their resistance to chemical resistance, weathering, radiation, and flame. The LCPs have been applied for many injection and compression-molded parts for their excellent properties [3–5, 9]. All materials applied in this study are powder for easy mixing and dispersion. A compression molding machine with temperature controllers was employed to mold specimens. The processing temperatures were set at



Fig. 19.2 Electrical conductivity as a function of mass fraction of MWCNT-LCP composite

300–350 °C for LCP carbon-materials-filled composites [9]. A compression-molded circular specimen with a diameter of 133 mm and a thickness of 1 mm was made as an electromagnetic interference (EMI) specimen. An annulus 32 mm and 76 mm in inner and outer diameter, respectively, was cut for measuring the EM SE of the composites.

According to basic EM shielding theory, the higher conductivity has the higher SE. The more MWCNTs that are added, the more overlapping conductive MWCNT networks are formed, and hence the higher conductivity and the higher SE are obtained [4, 18, 19]. The conductivity of the MWCNT-LCP composite specimen was measured by a four-terminal technique. Comparing with the ADM MWCNT-LCP, the CVD MWCNT-LCP was made of purified MWCNTs in a CVD method from Desunnano Ltd. [31]. Figure 19.2 shows the relations between weight percentages of MWCNTs and electrical conductivity. It revealed that the higher weight percentage of MWCNTs exhibited a higher electrical conductivity. The higher conductivities of CVD MWCNT-LCP composite compared to ADM MWCNT-LCP composite is due to the higher aspect ratio and the remaining catalyst Fe enclosed in CVD MWCNTs. Using the SEM to examine the MWCNT-LCP composite, the morphology shows many trunk-like long fibers. However, in the MWCNT-LCP composite, it is hard to distinguish MWCNT from LCP, since the LCP itself has a highly ordered structure and envelops the MWCNTs, as shown in Fig. 19.3a. For the purpose of examining the real MWCNT dispersion, we use an ion technique to break the atomic bonds of LCP and MWCNT. Hence, the MWCNT morphology can be clearly observed, as shown in Fig. 19.3b.

The mechanical strength of the MWCNT composite can be characterized by the tensile strength measurement. Figure 19.4 shows the relationship between the tensile strength and the weight percentage of MWCNT composite. The tensile strength increases as the MWCNT weight percentage increases. This is due to the



Fig. 19.3 (a) SEM photograph of MWCNTs embedded in LCPs and (b) SEM photograph of MWCNTs distribution in composite (locally)



Fig. 19.4 Tensile strength as a function of mass fraction of MWCNT-LCP composite

reinforcement of the polymer-based MWCNT composites regardless of the MWCNT functionalization. Fillers such as MWCNT, with a high aspect ratio usually exhibit a high tensile strength and a good flexural strength. However, the MWCNT reinforcement material seldom carries over to the composite due to poor load transfer from matrix to MWCNT reinforcement, unless the MWCNTs are appropriately functionalized. The modulus of the composite usually improves with MWCNT reinforcement, regardless of functionalization. The higher slope of CVD MWCNT-LCP composite as compared to that of the ADM MWCNT-LCP could be attributed to the high aspect ratio of the CVD MWCNT. However the differences of conductivity and tensile strength of the ADM MWCNT-LCP and CVD MWCNT-LCP composites are small, as shown in Figs. 19.2 and 19.4. The ADM MWCNT-LCP composites still have with a high aspect ratio advantage.

19.2.3 Material Properties of Dispersed MWCNT-PI Composites

The polymeric material applied in this work is polyimide (PI) [27]. In the literature, it has been reveled that the carbon nanotubles may be dispersed by the methods of chemical modification and physical adhesions [32–34]. The chemical modification requires a treatment of acids, such as HNO₃, and H₂SO₄, which may adversely damage the MWCNT structure, inevitably requiring a great deal of surfactant addition for the adhesion process [32]. The physical method for dispersing the MWCNTs in ionic liquid (IL) dispersants [33, 34] was adopted in this study. The method involves an intensive grinding of the mixture of IL and MWCNTs followed by dissolving into N-methylpyrrolidone (NMP) solvent. The van der Waals force and π - π stacking interactions between the MWCNTs were mitigated by the mixing with the imidazolium ions in the MWCNT-IL hybrid solution [33]. The dispersion was efficiently reinforced by taking advantage of a strong affinity of the imidazolium cation for the π -electronic MWCNT surface. The dispersion mechanism in this work is that the organic cations of the IL potentially interact with π -electronic compounds through the so-called "cation- π " interaction [33].

Examination using an UV-vis spectrometer has evidenced the uniformity of the MWCNT-IL suspension at the absorption of 550 nm light. Figure 19.5 shows the absorption for various weight ratios of MWCNT-IL dispersions in the NMP. It was found that the MWCNTs from CVD were easier to disperse than those from the ADM method. The difference perhaps reflects their relative impurity levels due to contamination from the manufacturing. The MWCNTs from the CVD method are 95% pure, whereas the ADM method generates MWCNTs with less purity. The



Fig. 19.5 UV-vis spectrometer absorption of various weight ratios of MWCNT-IL hybrid dispersed in NMP solvent at wavelength of 550 nm



Fig. 19.7 Relation between MWCNT weight percentage and electrical conductivity of (a) IL-dispersed MWCNT-PI composite and (b) non-dispersed MWCNT-LCP composite

impurities include carbon nanocapsules (CNC), carbonaceous impurities or ash, and amorphous carbon [18]. In our experiments, it requires more IL to disperse the ADM produced MWCNTs. To fabricate the MWCNT-PI composite, a poly(amic acid) (PAA) resin precursor was allowed to mix with the finely dispersed MWCNT-IL suspension at the MWCNT weight percentage of 0.1–30%. After vigorous mixing, the slurry was cast onto a glass substrate and cured into MWCNT-PI composite films. In Fig. 19.6, a SEM micrograph of MWCNT-PI composite is shown for the fine dispersion of MWCNT embedded in the PI matrices.

The conductivity of the MWCNT-PI composite was measured by a four-terminal technique. Figure 19.7 shows the relations between weight percentage of MWCNTs and electrical conductivity. The measured electrical conductivity for the IL-dispersed MWCNT-PI composite in Fig. 19.7a [27] is compared to the non-dispersed MWCNT-LCP composite in Fig. 19.7b [18, 19]. These comparisons indicate that the IL-dispersed MWCNT-PI composites provide higher electrical conductivity. The finely dispersed MWCNT composites have demonstrated a remarkable improvement in comparison with our previously reported results

[18, 19] and comparable to the results reported by Kim [28, 29]. It clearly indicates that the fine dispersion of MWCNTs is the dominant factor for fabricating the higher conductive materials.

19.3 Electromagnetic Shielding Performance of MWCNT Composites

19.3.1 Shielding Measurements of Non-dispersed and Dispersed MWCNT Composites in the Far-Field Source

Figure 19.8 shows a setup for the SE measurement and a cross section of the coaxialtype transmission-line holder. A flanged coaxial transmission-line holder was designed by following the ASTM D4935 method [35], which is used to measure the SE of a disk-shaped MWCNT-LCP specimen in far-field source. The testing frequency range is from 1 to 3 GHz, since we focus on 2.5 Gb/s lightwave transmission applications. The diameter of the inner conductor was 33 mm, and the outer conductor had inner and outer diameters of 76 mm and 133 mm, respectively, according to the definition of ASTM D4935 [35]. The electromagnetic SE of the MWCNT-LCP composites was measured by an insertion of the disk-shaped specimen with a diameter of 133 mm and a thickness of 1 mm between the two identical flanges. The purpose of the SE test procedure is to quantitatively measure the insertion loss that results from introducing the test specimens. The result of the far-field measurement is shown in Fig. 19.9. The SE of the MWCNT-LCP composites was measured from 38 to 45 dB in the frequency range of 1–3 GHz, which is

Fig. 19.8 Measurement setup for the shielding effectiveness of the plastic composites based on the ASTM D4935 method and a cross section of the coaxialtype transmission-line holder





Fig. 19.9 Far-field measurement of 50% weight percentage MWCNT-LCP composite

suitable for industry use. The SE of the MWCNT-LCP composite is also comparable to the other shielding plastic composites such as carbon fiber (CF)-nylon, CF-LCP, and WCCF-epoxy [4].

For a coaxial holder transmission-line circuit, there are significant parasitics between the holders and specimen. The equivalent circuit of a flanged coaxial holder with specimen can be modeled for theoretical calculation when the parasitic effects are considered [3, 8, 9, 19]. The calculated result of SE versus frequency is also shown in Fig. 19.9. Both measured (solid line) and calculated (dashed lines) results of the far field are in good correlation.

The SE of the MWCNT-PI composite is measured by the ASTM D4935-92 method [35]. In Fig. 19.10, the SE for a dispersed MWCNT-PI of 850 μ m thickness (30% weight percentage) and non-dispersed MWCNT-LCP in 1200 μ m thickness (30% and 50% weight percentages) are compared. The SE results are higher than 40 dB in the frequency range between 1 and 3 GHz for the 30% weight percentage dispersed MWCNT-PI and the comparable 50% weight percentage non-dispersed MWCNT-LCP. The result indicates that the lower weight content of the dispersed MWCNT-PI can achieve a higher SE. This implies that lower-cost MWCNT composites can be used to build the EMI shielding module box of an optical transceiver. According to the shielding theory, a shielding effect is generally dependent on the increase of electrical conductivity and film thickness. With the higher electrical conductivity but a thinner film, the dispersed MWCNT-PI (850 μ m) was found to have a comparable SE to that of the non-dispersed MWCNT-LCP (1200 μ m).



Fig. 19.10 SE of dispersed 30 wt% MWCNT-PI, 50 wt% and 30 wt% MWCNT-LCP

19.3.2 Shielding Measurements of Non-dispersed and Dispersed MWCNT Composites in the Near-Field Source

Near-field measurement is used to examine the SE of the specimen assembly, which is closer to the radiant source. It is more like the actual situation of a real application. A monopole-type antenna was used as the radiant source. Then, we put the monopole-type antenna into a module box built of the MWCNT-LCP composite to measure the difference of reference level and shielding level, which is the SE of the module box in the near-field situation. The SE measurement in a near-field source was carried out in a fully anechoic EM compatibility (EMC) chamber, as shown in Fig. 19.11 [3–5]. Because the hybrid absorbers combining the ferrite tiles and foam absorbers were aligned on the metal-shielded wall inside the chamber, good wave-absorbing performance could be achieved from 30 MHz to 18 GHz for the EMC chamber. The radiation source was put on a wooden table from which an antenna was seated at a distance of 3 m for receiving the radiated field. Because the interconnecting length on the optical transceiver module was generally about 1-2 cm, an electric monopole with a 2 cm length was used to emulate the radiation energy inside the molded housing. The SE behavior in the near-field source is similar for both non-dispersed MWCNT-LCP and dispersed MWCNT-PI.



Fig. 19.11 SE-measurement setup for near-field monopole-type source in a fully anechoic EMC chamber

19.4 Electromagnetic Shielding Performance of Transceiver Packages

19.4.1 Optical Transceiver Modules

An optical transceiver module consists of a 1.3 μ m laser (TOSA), a photodiode (ROSA), two ICs, and a plastic housing [3, 4]. These high-speed electric signals with a fast rising/falling edge would result in significant EMI problems as the transceiver modules are mounted onto digital communication systems. Metallic housings are the general solution to reduce the EMI of the module for complying with the Federal Communications Commission (FCC) EMI regulation. But due to low cost and lightweight considerations, the plastic packaging or housing becomes one of the major trends for future optical transceiver module designs [1–5].

The optical transceiver modules were fabricated by the MWCNT-LCP composites. The shape of the molded package housing was a rectangular box with the dimensions of $70 \times 30 \times 20$ mm. The weight percentage of MWCNT was 50%. In general, the SE increases as the mass fraction of MWCNT increases. However, when the mass fraction of MWCNT increases more that 50%, the MWCNT-LCP composite becomes easy to break when compressing the specimen. This might be due to less LCP to fill out all the space inside the composite specimen, which makes gaps or caves and reduces the strength of the specimen.

A novel polyimide film material, consisting of finely dispersed MWCNTs, was also developed for uses in packaging a 2.5 Gbps plastic transceiver module. In Sect. 19.3.1, the IL-dispersed MWCNT-PI composites with 30% weight percentage MWCNTs exhibited high SE of 40–46 dB [27]. By comparison, the MWCNT-LCP

composites fabricated by nondispersive process required a higher weight percentage (50%) of MWCNTs [7, 8]. Therefore, the IL-dispersed MWCNT-PI composites with lower weight percentage (30%) of MWCNTs were employed to fabricate a 2.5 Gbps plastic transceiver module.

19.4.2 Electromagnetic Interference Measurement of Transceiver Module in the Near-Field Source

An optical transceiver module with transmission rate of 2.5 Gb/s was tested to evaluate the EM shielding against emitted radiation from the plastic packaging. The packaged transceiver communicated with a golden specimen module (GSM) with identical functions to the module under test (MUT) [3–5]. A pattern generator (Tektronix GTS1250) transmitted the differential PRBS patterns (2.5 Gb/s) to the GSM. Through a fiber-optic link, the data were received by the MUT working in the loopback mode inside the chamber.

An optical transceiver module usually consists of a transmitter and a receiver. In this work, due to the limited housing space in the MWCNT-LCP composite box, the SE measurement of the optical transceiver module is carried out by separate transmitter and receiver-module measurements.

The adopted optoelectronic devices under test did not radiate as high as the monopole antenna. So, the results for the monopole antenna enclosed in the module box might reflect the real shielding ability of the module box in the near-field situation. In brief, the MWCNT-LCP module box composite has shown a good shielding ability to reduce the radiation from optoelectronic devices such as transmitters, receivers, and transceivers under the testing frequency ranges of 1–3 GHz, and all the results meet FCC regulations [36].

19.4.3 Electromagnetic Susceptibility Performance of a Non-dispersed MWCNT-LCP Packaged 2.5 Gbps Transceiver Module in the Near-Field Source

The EMS or electromagnetic immunity of the optical transceiver modules to the EMI is one of the major concerns to maintain good signal quality over gigabits-persecond transmission rate [5, 37, 38]. In this work, the EMS performance of an optical receiver package fabricated by the MWCNT-LCP composite is experimentally evaluated by the eye diagram and bit-error-rate test for a 2.5 Gbps lightwave transmission system. Figure 19.12 shows the measurement setup for the EMS performance of the proposed package. A pulse pattern generator (PPG, Anritsu MP1763C) is used to transmit 2.5 Gbps signal to the transceiver module under test through an optical transmitter. The 2³¹-1 pseudorandom bit sequence (PRBS) pattern



Fig. 19.12 EMS measurement setup

is given by the PPG. The received signal is electrically returned to a bit-error-rate tester (BERT, Anritsu MP1764C), and the eye patterns can also be measured by a sampling scope (Tektronix CSA 8000C). To perform the EMS measurement of the packaged receiver, the monopole radiator excited by the PPG is used to interfere with the packaged module at a distance of 3 cm.

The display with eye mask gives qualitative values for noise, jitter, rise time, fall time, and pulse duration. Figure 19.13a–c show the eye diagrams of the packaged receiver boxes with the 20%, 30%, and 50% weight percentages of MWCNTs in the MWCNT-LCP composites, respectively. In Fig. 19.13a, there was a lot of worse jitter surrounding the X region, as indicated by the arrows. The applied amplitude on the interference monopole-type antenna was 0.75 Vp-p. Figure 19.14 plots the eye mask margin as a function of the MWCNT weight percentage, based on Fig. 19.13. The mask margin is defined as the ratio of the maximum allowable mask to the standard mask. The mask margins were improved 46%, 53%, and 54% for 20%, 30%, and 50% MWCNT weight percentage increases. The result clearly indicates that the higher MWCNT weight percentage has the better EMS performance.

Figure 19.15 shows the relationship between power penalty and MWCNT weight percentage. The amplitude of interference monopole-type antenna was 1 Vp-p. The power penalty is defined as the received power difference between unpackaged boxes without radiated interference and packaged boxes with radiated interference in dB unit at BER equal to 10^{-12} . The result showed that the power penalty decreased as the MWCNT weight percentage increased. The power penalties are less than 1.5 dB for three different MWCNT weight percentages. The result indicates that the higher weight percentage of the MWCNTs, the better is their shielding ability and EMS performance.



Fig. 19.13 Eye diagrams of the packaged module of different weight percentages of MWCNTS under radiation interference. (a) 20%, (b) 30%, (c) 50%. The arrows indicate the worse jitters surrounding at X region

19.4.4 Electromagnetic Susceptibility Performance of a Dispersed MWCNT-PI Packaged 2.5 Gbps Transceiver Module in the Near-Field Source

As described previously in Sect. 19.3.1, the IL-dispersed MWCNT-PI composites with 30% weight percentage MWCNTs exhibited high SE of 40–46 dB [27]. By comparison, the MWCNT-LCP composites fabricated by the nondispersive process required a higher weight percentage (50%) of MWCNTs [7, 8]. Therefore, the IL-dispersed MWCNT-PI composites with a lower weight percentage (30%) of MWCNTs were employed to fabricate a 2.5 Gbps plastic transceiver module.



Fig. 19.14 Relationship between mask margin and MWCNT weight percentage at the amplitude of monopole-type antenna of 0.75 Vp-p



Fig. 19.15 Relationship between power penalty and MWCNT weight percentage at the amplitude of monopole-type antenna of 1 $V_{p\text{-}p}$

A setup for measuring the performance for a 2.5 Gbps optical receiver was shown in Fig. 19.12. A pattern generator (HP 70841B) was used to transmit a 2.5 Gbps signal to the optical receiver module under test through an optical transmitter. The 2^{31} -1 pseudorandom bit sequence (PRBS) pattern is given by the pattern generator. The received signal is electrically returned to an error detector (HP 70842B), and the eye patterns can also be measured by a digital communication



Fig. 19.16 Eye diagrams of 2.5 Gb/s optical receiver (a) without shield and (b) with shield

analyzer (HP83480A). To perform the EMS measurement of the packaged optical receiver, the monopole radiator excited by the pattern generator is used to interfere with the packaged module at a distance of 4 cm. Figure 19.16 shows the eye diagrams of a 2.5 Gbps optical receiver in the absence and presence of MWCNT-PI shielding in the box under the interference of a monopole voltage amplitude 2 Vp-p. The transmission speed is 2.5 Gbps and the mask used is OC-48. The eye of the box with shielding is apparently more open than that in the absence of shielding. The mask margin is improved from 43% to 56% in the presence of MWCNT-PI shielding. The mask margin was related to the performance of the electronic circuit under test.

19.5 **Conclusion and Discussion**

According to basic EM shielding theory, the SE increases as the material conductivity increases [18, 19]. Multiwall carbon nanotube (MWCNT) means a tube with many CNTs inside. The more polymer-based MWCNT material is added, the more overlapping conductive MWCNT networking, and hence the higher conductivity and the higher SE are expected. However, the high aspect ratio and low ionic character of MWCNTs are not easily dispersed within the plastic hosts. The lack of dispersing ability in the polymer matrices is caused by internal van der Waals force among the MWCNTs and their consequent aggregation [24-26]. Without a fine dispersion, the MWCNTs may form local clusters so poor homogeneity exists in the MWCNT composite. As a consequence, the weight percentage of the added MWCNTs is required in order to achieve a good electrical conductivity and a comparable SE. For developing a cost-effective material, a fine dispersion of MWCNTs in the polymer matrices is essential.

In this study, a novel polyimide film material, consisting of non-dispersed and dispersed multiwall carbon nanotubes (MWCNTs), was developed for use in packaging a 2.5 Gbps plastic transceiver module. The results showed that the IL-dispersed MWCNT composites with 30% weight percentage MWCNTs exhibited high SE of 40–46 dB. By comparison, the MWCNT composites fabricated by a nondispersive process required a higher weight percentage (50%) of MWCNTs. Furthermore, the package housing developed, fabricated by IL-dispersed MWCNT composites, clearly improved EMS performance, mask margin, and power penalty for a 2.5 Gbps lightwave transmission system. This significantly improved result has marked the achievement of using the dispersive MWCNT composites for the high SE and suitability for packaging low-cost and high-performance optical transceiver modules used in the FTTH lightwave transmission systems.

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Chapter 20 Properties of 63Sn-37Pb and Sn-3.8Ag-0.7Cu Solders Reinforced with Single-Wall Carbon Nanotubes



K. Mohan Kumar, Vaidyanathan Kripesh, and Andrew A. O. Tay

20.1 Introduction

As integrated circuit (IC) technology continues to advance, there will be increasing demands on I/O counts and power requirements, leading to decreasing solder pitch and increasing current density for solder balls in high-density wafer-level packages [1]. As the electronics industry continues to push for miniaturization, reliability becomes a vital issue. The demand for more and smaller solder bumps, while increasing the current, has also resulted in a significant increase in current density [2] which can cause the failure of solder interconnects due to electromigration [3].

Solders are extensively used in IC technology as mechanical and electrical interconnects because of their ease of processing and lower cost. However, because of their relatively low melting temperatures, creep is a major concern. When electronic devices are switched on and off, the electronic packages experience cyclic changes in temperature. Due to differences between the packages and the substrate, cyclic changes in thermomechanical stresses are induced in the package-to-board solder joints. Such cyclic stresses in the solder joints eventually lead to failure of the solder joints through thermomechanical fatigue [4, 5].

With the relentless trend toward very fine-pitch IC packages, the cyclic stresses experienced by flip chip-to-board interconnects are increasing greatly resulting in a drastic drop in fatigue life of solder joints. One way of overcoming this problem is to

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use new materials which can provide enhanced mechanical, electrical, and thermal properties. Composite solders can offer improved properties [6]. Although a few researchers have investigated the influence of nanoparticles and nanotubes influence on the properties of solder [7–9], these investigators were mainly focused on the mechanical properties of the solders. In this study, the influence of nanotube addition on microstructural, mechanical, electrical, wetting, and thermal properties has been investigated. In addition to this, efforts have been made to evaluate the joint strength and creep strength of the composite solder joints.

Owing to their fascinating physical properties and unique structures, carbon nanotubes (CNTs) are receiving steadily increasing attention since their discovery [10]. Intense interest from researchers has been generated in utilizing these unique structures and outstanding properties, for example, in hydrogen storage, supercapacitors, biosensors, electromechanical actuators, nanoprobes for highresolution imaging, and so on [11, 12]. In recent years, there has been a steadily increasing interest in the development of CNT-reinforced composites due to their remarkable mechanical, electrical, and thermal properties [13–16]. Depending on their length, diameter, chirality, and orientations, CNTs show almost five times the elastic modulus (1 TPa) and nearly 100 times the tensile strength (150 GPa) of high strength steels [17]. The motive is to transfer the exceptional mechanical and physical properties of carbon nanotubes to the bulk engineering materials. Polymers, ceramics, and metal are favorable as matrix materials. CNT-reinforced polymerbased composites were widely synthesized by surfactant-assisted processing, repeated stirring, solution evaporation with high energy sonication, and interfacial covalent functionalization [18-20]. Much of the research in nanotube-based composites has been on polymer or ceramic matrix materials and less on metal matrix composites [21-23]. This is mainly due to the fact that uniform dispersion of CNTs in a metal matrix is quite difficult.

Nai et al. [9] demonstrated that the dispersion and homogenous mixing between MWCNTs and a lead-free solder matrix could be obtained by mixing nano-sized matrix powders with CNTs. They showed that the powder metallurgy process was a very promising technique for full densification of CNT/lead-free solder nanocomposites which showed remarkable enhancement of yield strength compared to that of unreinforced lead-free solders.

The current work provides an insight into the usage of SWCNTs as a reinforcing material for the enhancement of the solder material properties to be used in waferlevel chip-scale packages (WLCSP). The aim of this work is to fabricate and characterize CNT-reinforced nanocomposite solders and show their improved physical, thermal, electrical, mechanical, and wetting properties compared to the original Sn-Pb and Sn-Ag-Cu solders.

20.2 Experimental Aspects

20.2.1 Materials

The starting materials used in this study were Sn-Pb and Sn-Ag-Cu solder powders of Type 7 (2–11 μ m). The SWCNTs employed in this study were prepared using the chemical vapor deposition technique and typically have an average diameter of 1.2 nm and lengths between 5 and 10 μ m.

20.2.2 Preparation of Composite Solders

The solder powder and SWCNTs were weighed to the approximate weight % ratio. Different compositions were prepared with varying SWCNT content ranging from 0.01 to 1 wt%. The pre-weighed SWCNTs and solder powders were blended homogeneously using a V-cone blender operated at a speed of 50 rpm. The homogenously blended composite solder powders were consolidated by uniaxial cold pressing with a pressure of 110 bar in the case of Sn-Pb composite solders, while Sn-Ag-Cu composite solders were compacted at a pressure of 120 bar. The consolidated "green" composite solder compacts of diameter 35 mm were sintered at 150 °C for Sn-Pb composite solders and at 180 °C for Sn-Ag-Cu composite solders and at 180 °C for Sn-Ag-Cu compacts were finally extruded at room temperature with an extrusion ratio of 20:1.

20.2.3 Scanning Electron Microscopy

Samples were cut from the extruded solder bars with a diamond saw and mechanically polished with diamond pastes after cutting, finishing with 0.02 μ m grade. Microstructural observations were performed by scanning electron microscopy using a Hitachi FE-SEM 4100 operated at 10 kV. The elemental analysis of the phases was carried out using energy-dispersive X-ray spectroscopy (EDX) equipped with FE-SEM.

20.2.4 Thermomechanical Analysis (TMA)

The linear thermal expansion coefficient of composite solders was measured using a Perkin-Elmer TMA-7 thermal mechanical analyzer operated in expansion mode. Cylindrical samples of diameter 8 mm were employed. TMA data were obtained in the heating range of 25-125 °C in the case of Sn-Pb composite solders, while a

25-150 °C heating range was employed for the Sn-Ag-Cu composite solders at a rate of 5 °C/min. All TMA experiments were performed with a small loading force of 5 g to avoid deformation of the samples during testing. The CTEs of the composite solder specimens were obtained from the slope of the curve over a linear temperature range.

20.2.5 Differential Scanning Calorimetry (DSC)

The melting behaviors of the composite solder specimens were examined by a Perkin-Elmer DSC-7 system. DSC experiments were carried out at a heating rate of 10 $^{\circ}$ C/min from 25 to 250 $^{\circ}$ C. The heat flow as a function of temperature was recorded and analyzed. The entire scanning was carried out under an inert nitrogen atmosphere.

20.2.6 Electrical Properties

Electrical conductivity was measured on strips having dimensions of 50×10 mm cut from rolled composite solder preforms with a thickness of approximately 0.13 mm using a four-point probe technique.

20.2.7 Wettability

Solder alloys were cold rolled to preforms of thickness 1 mm and 0.13 mm for the joint tensile testing, wetting, and creep rupture analyses. The solder preforms were remelted four times in order to get a uniform structure and composition. Approximately 0.2 g of the remelted solder preforms were weighed using an electronic balance. The weighed solder preforms were cleaned with acetone in an ultrasonic bath. The substrate used was a thin copper plate of 99.9% purity and dimensions of $25 \times 25 \times 0.1$ mm. These small substrates were polished sequentially with silicon carbide sandpaper of up to 800 abrasive number and then cleaned ultrasonically in acetone for 10 min to achieve an ultraclean substrate for wetting experiments.

The measurement of contact angle was performed using the following technique. First wetting was carried out on a hot plate. Rosin mildly activated (RMA) flux was applied on a copper substrate. Some flux was then applied on the surface of the pre-weighed solder preform before placing it on the copper substrate. In preparation for the reflow, the substrate containing the solder and the flux was first preheated to 100 °C and then to the reflow temperature of 240 °C. After the time of reflow, the specimen was quickly removed, allowed to solidify, and later quenched to room temperature. The solder after reflow on the copper substrate was cleaned with

alcohol for 10 min to remove the flux residues. After each test, the solder drop was cut perpendicular to the interface, mounted in resin, and polished to examine the morphology and contact angle of solder on copper substrate. Then the photograph of the specimen was taken and analyzed with the help of commercially available software for measuring the spreading area.

20.2.8 Microhardness Testing

The sintered samples were polished to a mirror finish prior to the microhardness indentation tests. Microhardness of the composite solder specimens were measured using a Digital Micro-Hardness Tester with a Vickers indenter. The samples were indented with a load of 10 g, and an average of seven indentations was made at different locations of the composite solder specimens for further analysis.

20.2.9 Tensile Testing

The samples for tensile testing were machined from the extruded bars. Dog-boneshaped specimens of gauge length 25 mm and diameter 5 mm were prepared. Tensile experiments were carried out at room temperature on the specimens using an Instron 5569 tensile tester at a constant cross-head displacement of 1 mm/min. Five samples of each composite solder were tested. All samples were tested to failure.

20.2.10 Tensile Strength of Solder Joint

Cu samples of length 45 mm were cut from a 99.9% pure, half-hardened Cu bar with rectangular cross section (10×1 mm). These were etched in 50% sulfuric acid to get rid of the surface oxide layer. The mating surfaces were fluxed immediately with commercial RMA flux, and the rest of the surfaces were coated with solder resist to prevent them from being wetted by molten solder. Solder alloys were rolled into thin sheets of thickness 1 mm and sliced into pieces that approximately covered the mating surface area of the Cu samples. Then, the sliced solder pieces were placed between the mating surfaces of two Cu samples in an aluminum mold and were heated in a furnace to a temperature 50 °C above the liquidus of the solder. After holding in the molten state for 2 min, the samples were gently soldered with the help of a screw-driven mold to maintain a joint thickness of 500 µm by adjusting the screws placed at each end of the mold to obtain a good joint and were cooled in the furnace. It was found that the tensile testing specimens thus prepared resulted in joints with solder of thickness of between 300 and 400 µm.

20.2.11 Creep Rupture Analysis

The creep rupture tests were conducted using composite solder lap joints between two dog-bone-shaped copper pieces which were fabricated as follows. Two 99.9% pure, 0.1 mm thin copper sheets were first wire cut into the shape of a dog bone. The composite solder alloys were cold rolled to obtain performs of thickness 0.13 mm and cut into square specimens of dimensions 1×1 mm. The dog-bone-shaped copper substrates were cleaned with dilute sulfuric acid and rinsed with acetone. The narrow ends of the copper substrates were coated with solder resist to obtain a cross-sectional area of 1 mm². Then, RMA flux was applied to each narrow end of the substrate, and the composite solder preform was sandwiched between the two copper substrates. Reflow soldering was performed in a programmable oven. The creep rupture life tests were performed at room temperature with a dead load stress of approximately 10.4 MPa.

20.3 Results and Discussion

20.3.1 Microstructural Observation

The SEM and TEM microstructures of the as-received SWCNTs used in the present study are shown in Fig. 20.1. The FE-SEM microstructure of the original Sn-Pb solder is shown in Fig. 20.2a showing white contrast for tin grains and dark contrast for lead grains. The average grain size of the as-cast Sn-Pb solder was 5.12 μ m. Figure 20.2b shows the highly refined microstructure of 0.3 wt% SWCNT-doped Sn-Pb composite solder, which is a consequence of homogenous dispersion of the



Fig. 20.1 Images of SWCNTs: (a) SEM image of SWCNT, (b) TEM micrograph of SWCNT produced by a CVD process



Fig. 20.2 FE-SEM micrographs of 63Sn-37Pb solder with (a) 0 wt% SWCNT, (b) 0.3 wt% SWCNT



Fig. 20.3 FE-SEM micrographs of Sn-3.8Ag-0.7Cu with (a) 0 wt% SWCNT, (b) 1 wt% SWCNT

nanotubes. The average grain size of the composite is measured to be $1.08 \mu m$ by employing image analysis software. An obvious difference between the microstructures of the solder alloys with and without addition of nanotubes can be observed.

There is some porosity observed in the solder matrix. This is mainly attributed to the sintering process. During the sintering process, the matter of the solder matrix flows and the SWCNTs act as solid impurities [24]. The van der Waal forces cause the SWCNTs to get entangled with one another. Because of this phenomenon, it is very difficult to achieve a higher degree of homogeneous dispersion of the SWCNTs throughout the solder matrix. In this manner the entangled SWCNTs may have resulted in the formation of pores in the solder matrix which is being observed in the micrographs.



Fig. 20.4 Phase identification of SWCNT at the grain boundary of Ag₃Sn in sintered Sn-Ag-Cu/ CNT composite: EDS of the white region showing the presence of carbon

Figure 20.3 compares the microstructures of the Sn-Ag-Cu + SWCNT composite solders and pure Sn-Ag-Cu solder. The higher magnification micrographs in Fig. 20.3a reveal that the microstructure of Sn-Ag-Cu solder is composed of a dark gray phase (Cu₆Sn₅) and brighter light gray grains (Ag₃Sn) dispersed evenly in the β -Sn solder matrix. For the Sn-Ag-Cu pure solder sample, the average grain size of the secondary phase varied between $3.75 \,\mu\text{m}$ and $4.25 \,\mu\text{m}$. The average grain size of the secondary phase was found to be 0.5-0.8 µm with 1 wt% addition of nanotubes to the Sn-Ag-Cu solder as shown in Fig. 20.3b. In the SWCNT-reinforced solder samples, the SWCNTs are distributed at the boundaries of the Ag₃Sn equiaxed grains. They can be identified by the difference in contrast, which is mainly associated with the different atomic numbers of the individual phases under consideration. Brighter regions correspond to the higher atomic numbers, while darker phases correspond to the lower atomic numbers. The elemental analysis obtained by EDX is shown in Fig. 20.4. The intense "C" peak represents the presence of SWCNTs at the boundaries of the Ag₃Sn grains. This shows that the SWCNTs remained inside the solder matrix after sintering but were concentrated at the boundaries of the Ag₃Sn grains.

The possible reason for the size refinement is as follows. SWCNT is a ceramic material. While processing the composite solder specimens, the surface diffusion of the Ag_3Sn can be suppressed by the extremely quick translations of ceramic materials through the temperatures that exist during the sintering process [25]. The reinforcement of the microstructure, as shown in Fig. 20.2 with the varying content of SWCNT, demonstrates a strong dependence of the sintered microstructure of the composite solders on the initial composition and morphology of the starting materials.



Fig. 20.5 Variation of CTE of both Sn-Pb and Sn-Ag-Cu composites with wt% of SWCNTs

	63Sn-37Pb		Sn-3.8Ag-0.7Cu	
Wt% SWCNT	Onset temp (°C)	Melting temp (°C)	Onset temp (°C)	Melting temp (°C)
0	181.1	183.3	217.7	221.0
0.03	181.1	182.8	217.1	220.1
0.08	180.2	182.2	216.4	219.8
0.1	179.5	182.0	216	219.3
0.3	179	181.9	215.6	218.9
1	176.3	181.1	213.4	217.9

Table 20.1 Onset and melting temperatures of Sn-Pb and Sn-Ag-Cu composite solders

20.3.2 Coefficient of Thermal Expansion (CTE)

The CTE was measured using TMA and was obtained from the initial linear slope of the thermal strain-temperature plot. The CTEs of pure Sn-Pb and Sn-Ag-Cu were found to be 25.8×10^{-6} /°C and 18.7×10^{-6} /°C, respectively, which are comparable with those in the literature [26, 27]. The variation of CTE with wt% of SWCNT addition, for the Sn-Pb and Sn-Ag-Cu composites, is shown in Fig. 20.5. The composite solders exhibit lower CTE values than the parent alloys. It was observed that the CTE of both the solders decreases with increasing content of SWCNT. In general, the lower CTE can be attributed to the rigidity of the nanotubes and the fine dispersion of nanotubes in the solder matrix, which can obstruct the expansion of the solder matrix at elevated temperatures. However, factors such as the adhesion of nanotube-matrix interfaces at testing temperatures, the apparent lack of orientation of the nanotubes, and the inevitable agglomeration at higher nanotube loads might affect the CTE values of nanocomposite solders and need to be confirmed by further studies and analysis.



Fig. 20.6 DSC thermographs for a heating rate of 10 °C/min for (a) 63Sn-37Pb solder, (b) 63Sn-37Pb + 0.3 wt% SWCNT



Fig. 20.7 DSC thermographs for a heating rate of 10 °C/min for (a) Sn-3.8Ag-0.7Cu (b) Sn-3.8Ag-0.7Cu +1 wt% SWCNT

20.3.3 Differential Scanning Calorimetry Analysis

DSC measurements were carried out to determine the thermal properties such as melting point and onset temperature of both Sn-Pb and Sn-Ag-Cu composite solders containing varying amounts of SWCNTs. The results are given in Table 20.1. Typical DSC thermograms of the Sn-Pb and Sn-Ag-Cu solders and their composites with SWCNTs are shown in Figs. 20.6 and 20.7. The shapes of the thermograms closely resemble one another. They are characterized by a sharp endothermic peak associated with the onset temperature and a peak temperature that exactly corresponds to the melting temperature of the solder or composite solder. It can be seen from Table 20.1 that the melting point of the composite solders as well as the onset

temperature decreases with increasing content of SWCNTs. A similar decreasing trend in melting point was recently reported for the addition of nano-alumina and nano-SiO₂ to polyether ether ketone (PEEK) [28].

The possible reasons for the reduction in melting point of solders could be due to the increase in the surface instability with the higher surface free energy rendered by the addition of SWCNTs. Also, the size effect of carbon nanotubes can significantly alter the grain boundary/interfacial characteristics of solders, resulting in such a change in physical properties [24, 29, 30].

It can be seen from Table 20.1 that both nanocomposite solders show decreasing melting points and onset temperatures with increasing nanotube content. However, the Sn-Ag-Cu/SWCNT system shows a much lower melting temperature than the Sn-Pb/SWCNT system. This was mainly attributed to the good adhesion between the nanotube and Ag₃Sn of the lead-free solder matrix.

Addition of SWCNTs has resulted in lowering the melting point of the Sn-Ag-Cu and Sn-Pb composite solders by only 3.4 °C and 1.5 °C, respectively. This lowering is not large, and the resultant nanocomposite solders can readily be adopted with the current recommended reflow conditions.

20.3.4 Electrical Conductivity

Figure 20.8 shows the variation of the electrical conductivity of the Sn-Pb and Sn-Ag-Cu composite solders with SWCNT wt%. The electrical conductivities of Sn-Pb and Sn-Ag-Cu solder are 10.58%IACS (International Annealed Copper Standard) and 14.29%IACS, respectively. It is evident from the graph that increasing the SWCNT content increases the electrical conductivity of the composite solders. The electrical conductivity of the Sn-Pb based composite solders increased from 10.58%IACS to 11.04%IACS with the addition of 0.05 wt% of SWCNTs. Further



Fig. 20.8 Electrical conductivity of Sn-Pb and Sn-Ag-Cu composite solders versus SWCNT content



Fig. 20.9 Contact angles of composite solders on copper substrates with varying contents of SWCNT

addition of SWCNTs increased the conductivity value to 11.86%IACS. This increment is ~12% higher than the parent Sn-Pb alloy. A similar behavior is noted for the Sn-Ag-Cu-based composite solders. The room temperature conductivities of the bare Sn-Pb and Sn-Ag-Cu are comparable with those in the literature [27]. Similar increments in conductivity have been observed with epoxy nanotube composites [31].

The trend of increasing electrical conductivity of the nanocomposite solders with increasing amounts of SWCNT addition can be explained by the fact that at the percolation threshold, there is a network structure of nanotubes surrounded by the immobilized solder matrix. Even if the nanotubes do not touch each other, conductivity of the nanocomposites is increased as long as the distances between the tubes are lower than the hopping distance of the conducting electrons [32].

20.3.5 Contact Angle

Figure 20.9 shows the contact angles measured for both Sn-Ag-Cu and Sn-Pb solders as function of SWCNT content. As can be seen, the contact angle for both composite solders first decreases with SWCNT content up to about 0.1 wt% before increasing. The minimum value for Sn-Pb solder composite was 15.8° at 0.08 wt% SWCNT, while the minimum for Sn-Ag-Cu solder composite was 27° at 0.1 wt% SWCNT. The contact angle measured for Sn-Ag-Cu was 34.2°, which is very similar to the value reported by other researchers in the literature [27].

The effect of nanotube addition on the wettability can be explained as follows. An increase in the flux-copper surface energy, or decrease in flux-solder surface energy, will decrease the contact angle, thus increasing the wettability. SWCNT addition that



Fig. 20.10 Variations of the spreading area for composite solders with different wt% of SWCNT

promotes these changes will result in improved wettability. It is expected that increasing the SWCNT content to a certain extent could greatly increase the flux-solder surface tension because of chemical reactions. Similar findings have been reported by Loomans [33] for lead-free solder systems.

20.3.6 Wettability

The spreading area and wetting area of a fixed mass of solder were used to evaluate wettability [34]. Figure 20.10 shows the spreading area measured for both composite solders. This figure reveals a similar trend as the contact angle results. For both composite solders, the spreading area increases with SWCNT content up to about 0.1 wt% before decreasing. The maximum value for Sn-Pb solder composite was 159.5 mm² at 0.08 wt% SWCNT, while the maximum for Sn-Ag-Cu solder composite was 128.5 mm² at 0.1 wt% SWCNT.

It is believed that the addition of nanotubes enforced the orbital interaction between the tin atoms and the copper atoms and greatly improved the spreading area. However, further addition of nanotubes beyond a critical concentration deteriorated the wetting properties and reduced the spreading area of the composite solders. If there is a high level of nanotubes in the composite solder, tin atoms can no longer play the important role of base metal, since the orbital reaction between nanotubes and tin atoms is not strong. Therefore, the spreading area and wettability are worse with increasing levels of nanotubes beyond a certain critical value.



Fig. 20.11 Microhardness variation of the composite solders with different wt% of SWCNT



Fig. 20.12 Variations of yield strength of composite solders with wt% SWCNT

20.3.7 Microhardness

Figure 20.11 gives the microhardness values of the composite solder alloys as a function of SWCNT loading. Each value presented was obtained from an average of seven readings at different locations within each composite solder sample. A trend of increasing microhardness with SWCNT content was observed for both composite solder alloys. Microhardness tests show indeed that the SWCNT-reinforced Sn-Ag-Cu composite solders have slightly higher hardness than the SWCNT-reinforced Sn-Pb solder. The average microhardness of the Sn-Pb+0.5 wt% nanotube composite solder is approximately 16.5% higher than that of the Sn-Pb solder alloy, whereas 1 wt% addition of SWCNT to Sn-Ag-Cu solder resulted in nearly 18% improvement in the microhardness value as compared to the original Sn-Ag-Cu solder alloy.



Fig. 20.13 Effect of SWCNT loading on UTS of Sn-Pb and Sn-Ag-Cu composite solders

20.3.8 Tensile Properties

20.3.8.1 Yield Strength

The influence of nanotube addition on the yield strength of both composite solders has been investigated and plotted in Fig. 20.12. It can be seen that the yield strength of both composites increases with the nanotube content. It is interesting to note that in the case of Sn-Ag-Cu composite solders, the yield strength increases continuously with nanotube content, while for Sn-Pb solders, the yield strength reaches a maximum value at 0.3 wt% of nanotube addition before decreasing. In both cases, it was found that it was impossible for the solders to absorb more than 1 wt% of SWCNT. The maximum increase in yield strength for Sn-Ag-Cu solder composite at 1 wt% of nanotube reinforcement was 52.9% higher than its pure counterpart, whereas the maximum increase in yield strength achievable for Sn-Pb solder was ~18% at 0.3 wt % of nanotube addition.

20.3.8.2 Ultimate Tensile Strength

Figure 20.13 shows typical variations of the ultimate tensile strength (UTS) of Sn-Pb-based composite solders in comparison with Sn-Ag-Cu-based composite solders as a function of different concentrations of SWCNTs. All the measured tensile strengths of nanocomposite solders exhibited very small deviations. The trends observed are similar to the effect of nanotube addition on the yield strength. The UTS of Sn-Ag-Cu solder specimens increase monotonically with increasing SWCNT, while the UTS of Sn-Pb reached a maximum at 0.03 wt% of SWCNT before declining. The maximum UTS of Sn-Pb-based composite solders achieved with the addition of 0.3 wt% of SWCNTs was ~26% higher than undoped Sn-Pb solder. The effect of SWCNT on the UTS of solder is similar to its effect on polymers [31]. A maximum increase of about ~51% was observed for the Sn-Ag-Cu solder. The improvement in the tensile strength may be caused by the strong



Fig. 20.14 Variation of the tensile modulus of composite solders with wt% SWCNT

interactions between the solder matrix and the SWCNTs, which leads to good dispersion of SWCNTs in the nanocomposites. These well-dispersed SWCNTs may be the reason for the increase in the tensile strength. However, when the content of SWCNT is too high, the SWCNTs cannot be properly dispersed in the solder matrix and agglomerate into clusters because of the huge surface energy of SWCNTs [35, 36]. This probably caused the decrease of tensile strength as observed in the case of Sn-Pb solder doped with more than 0.3 wt% nanotube.

20.3.8.3 Tensile Modulus

The variation of tensile modulus of both composite solders (Sn-Pb and Sn-Ag-Cu) with wt% reinforcement of SWCNT is shown in Fig. 20.14. As with the yield strength and UTS, the tensile modulus for Sn-Ag-Cu composite solder increases monotonically with wt% reinforcement of SWCNT while that for Sn-Pb has a maximum at 0.3 wt%. The general increase of tensile modulus with %wt SWCNT is probably due the reinforcing effect imparted by the nanotubes that allowed a greater degree of stress transfer at the grain boundaries. A possible explanation can be given for the behavior for Sn-Pb composite solders by assuming a similar state of high-quality dispersion for all nanocomposites after the sintering process. An increasing amount of agglomerates in the sintered composite was observed for the SWCNT/Sn-Pb solder composites with nanotube content above 0.3 wt%. We propose these agglomerates to be a result of re-agglomeration which reduces the Young's modulus more significantly. The largest modulus of Sn-Ag-Cu composite solder was 12,642 MPa at 1 wt% SWCNT, which is almost 98% higher than the value of 6385 MPa for the original solder. The largest modulus for Sn-Pb composite



Fig. 20.15 Ductility of nanocomposite solders as a function of SWCNT content

solder was 14,216 MPa at 0.3 wt% CNT, which represents an increase of 53% over the value of 9276 MPa for the original solder.

20.3.8.4 Ductility

Ductility was quantified by measuring the plastic strain to failure. Appreciable ductility was measured for both Sn-Pb and Sn-Ag-Cu composite solders. A plot of ductility (% elongation) as a function of SWCNT loading is shown in Fig. 20.15. The tests demonstrated a downward trend of % elongation with increase in the SWCNT content for both composite solders. Sn-Ag-Cu solder shows a 33.3% elongation at break. Almost 26.6% elongation at break was found for 0.1 wt% of SWCNT added. The elongation to failure was observed to be 23.8% at the 1 wt% of SWCNT addition, which is ~27% lower than the virgin Sn-Ag-Cu solder matrix. This indicates that adding the nanotubes to Sn-Ag-Cu solder material increases brittleness which is consistent with the previous studies of composite solders reported by Chen et al. [36]. As shown in Fig. 20.15, the % elongation of 0.03 wt % reinforced Sn-Pb solders was obviously lower than those of pure Sn-Pb solder; the elongation decreases with increasing SWCNT content from 0.03 to 0.5 wt%. At 0.5 wt% SWCNT, the ductility is $\sim 24\%$ lower than the Sn-Pb solder. From this it is evident that both composite solders showed an increase in brittle characteristics due to the rigidity of the composite solder matrix as SWCNT content increased. In all the cases, the elongation to failure decreases. The major reason is that SWCNTs included into the solder matrix behave like physical constraints and restrict the deformation of the solder matrix.



Fig. 20.16 Influence of SWCNT content on the work of fracture of Sn-Pb and Sn-Ag-Cu composite solders

Table 20.2Grain sizes of theSn-Pb and Sn-Ag-Cucomposite solders

Solder alloy	Grain size (µm)	
63Sn-37Pb	5.12	
63Sn-37Pb + 0.3 wt% CNT	1.08	
Sn-3.8Ag-0.7Cu	3.75-4.25	
Sn-3.8Ag-0.7Cu + 1 wt% SWCNT	0.5–0.8	

20.3.8.5 Work of Fracture

Figure 20.16 shows a plot of the work of fracture versus the various SWCNT loading for the Sn-Pb and Sn-Ag-Cu composite solders. However, the work of fracture of Sn-Ag-Cu composite solders did not vary linearly with increase in SWCNT content. Maximum and minimum values were observed in this case. The minimum work of fracture was observed at 0.5 wt% addition of SWCNT, while the maximum was observed for the undoped Sn-Ag-Cu solder. For Sn-Pb solder, the minimum work of fracture occurred at 0.8 wt% CNT, while the maximum was observed for the undoped Sn-Ag-Cu solder.

20.3.9 Strengthening Mechanisms

20.3.9.1 Grain Size Refinement

Table 20.2 gives the grain size values measured using image analysis for both composite solders with and without reinforcement of nanotubes. As is common in composite materials, the grain size decreases as the weight fraction of reinforcement addition increases. Since nanotubes may act as nucleation sites for recrystallized grains during sintering, the volume fraction of recrystallization grains increases

when the reinforcement volume fraction increases; it can be observed that, as the weight fraction of the SWCNT rises, the grain size of the composite solder diminishes, causing strengthening by the Hall-Petch mechanism. SWCNTs control the grain size of the composite solders, since they prevent grain growth. This grain size refinement can be clearly seen in the microstructure of the composite solders shown in Fig. 20.3. The Hall-Petch relation can be formulated as

$$\sigma_H = \sigma_o + \frac{k}{\sqrt{D}},$$

where

 $\sigma_{\rm H}$ = yield stress σ_o = friction stress k = constant D = grain size

The yield stress increases as the grain size of the composite diminishes.

20.3.9.2 CTE Mismatch

63Sn-37Pb solder has a coefficient of thermal expansion of 25.8×10^{-6} /°C, while SWCNTs exhibit a much lower coefficient of thermal expansion of -1.5×10^{-6} /°C [35]. Hence, in the SWCNT-doped Sn-Pb solders, there exists a significant CTE mismatch between the SWCNT reinforcement and the solder matrix. This CTE mismatch can result in the prismatic punch of the dislocations at the interface which in turn can lead to the work hardening of the solder matrix. The dislocation density that is generated due to the CTE mismatch between the reinforcement and the solder matrix is directly proportional to the surface area of the reinforcement. The diameter of a SWCNT is very small leading to a lower density of Griffith flaws. Due to the lower Griffith flaws, the number of dislocations generated is likely to be higher, which in turn could result in the increased strengthening effect.

The dislocation density can be formulated as

$$\rho^{C} = \frac{10A\varepsilon f_{SWCNT}}{(1 - f_{SWCNT})bd_{SWCNT}}$$

where f_{SWCNT} is the weight fraction of the SWCNTs, ε is the misfit strain due to the difference in the CTE values of SWCNT and solder matrix, b is the Burgers vector, and d_{SWCNT} is the diameter of the SWCNT.

The increment in stress can be indicated by

$$\Delta\sigma_C = \sqrt{3\alpha\mu b}\sqrt{\rho^C},$$

where
μ = modulus of rigidity of the solder b= Burgers vector α = constant

20.3.9.3 Orowan Mechanism

The interaction between the dislocations and the SWCNTs can inhibit the motion of the dislocations, leading to bending of the dislocations between the nanotubes. Bending of dislocations produces a back stress, which could prevent further dislocation migration and result in an increase in yield stress. The Orowan mechanism is less significant in the metal matrix composites where the reinforcements are generally coarser in shape and the interparticle spacing is large, but it is more effective in the SWCNT-reinforced composites as the nanotubes effectively represent the fine particles having very narrow diameters of the order of a few nanometers. In this manner SWCNT can effectively strengthen the solder matrix by interacting with the dislocations.

Thus the increment in the shear strength of the composite solders can be written as

$$\Delta \tau = K^* \mu A^{1/2} b / r^* \ln{(2r/r_o)},$$

where

K = a constant characterizing the transparency of the dislocation forest for basalbasal dislocation interaction

 μ = modulus of rigidity of the solder matrix

r = volume equivalent radius of SWCNT = 7.087 nm

b = Burgers vector

A = constant = 0.093 for edge dislocations and 0.14 for screw dislocations

20.3.9.4 Residual Stresses

The CTE mismatch between the nanotubes and solder matrix resulted in the presence of residual stresses in the composite solder. The solder matrix remains in tension and the reinforced nanotubes in compression. A similar situation was observed when the metal matrix composites are reinforced with ceramic reinforcements [37]. Presence of residual stresses can also lead to the increment in the yield stress of the composite solders.

It is possible to conclude from the above discussion that the increment in yield strength and ultimate tensile strength of the composite solders has three main contributions: the grain size refinement, increase in dislocation density due to the CTE mismatch between the solder matrix and nanotubes, and the Orowan looping mechanism.



Fig. 20.17 Low magnification FE-SEM micrographs of the fracture surfaces of the Sn-Pb solder composite specimens with (a) 0.01 wt%, (b) 0.5 wt% SWCNT



Fig. 20.18 High magnification FE-SEM fractographs of Sn-Pb composite solders with (**a**) 0.01 wt %, (**b**) 0.5 wt% SWCNT

The decrease in ductility of the composite solders can be explained by the following mechanism. The reduction of ductility, with the higher reinforcement addition, is a very common phenomenon observed in metal matrix-based composites [38, 39]. The main reason may be the limited ductility exhibited by SWCNTs [40]. In addition, the SWCNTs may restrict the movement of dislocations either by inducing the large difference in the elastic behavior between SWCNTs and the matrix or creating the stress fields around the dislocations.

20.3.10 Fracture Studies

Fracture surfaces of Sn-Pb composites are shown in Fig. 20.17a, b. The lower magnification topographies which are represented indicate extreme ductile fracture modes, characterized by dimples on the surface. Closer observations at higher magnifications shown in Fig. 20.18a, b demonstrated the breakage of nanotubes.

Figure 20.17a shows the fractograph of the Sn-Pb solder specimens. The fracture surface shows evidence of high ductility with the dimples. However, the composite solders reinforced with nanotubes exhibited a limited ductility; the fracture occurred normal to the loading axis as is shown in Figs. 20.17 and 20.18. Figure 20.18 indicates that after tensile deformation, the solder matrix adheres well to the nanotubes due to the highly ductile nature of the matrix alloy. Dimples were observed on the composite solder surfaces in the region between the nanotubes and solder matrix. The nanotubes appeared to have been cut at the surfaces. From this observation, it can be inferred that the fracture took place in the solder matrix by void generation and propagation, finally resulting in the shearing of the nanotubes adhered to the matrix. This indicates that strong interface bonding has been developed in the nanotube-reinforced solder composites.

20.3.10.1 Fracture Mechanism for Sn-Pb Composite Solders

It is evident from the fractographs shown in Fig. 20.18 that the direction of the internal cracks in the composites is normal to the tensile loading axis. Here no nanotube pull-outs were observed. According to these findings, it is noted that the crack was initiated in the solder matrix and then propagated and sheared through the nanotube reinforcements. These findings are consistent with the strong interfacial bonding between the solder matrix and the nanotubes.

According to Lloyd [38, 39], there are three possible ways that fracture behavior can be observed in composite materials. (1) If the interface between the reinforcement and the matrix is weak, the crack can initiate and can propagate through the interface. (2) If the interface and the matrix are both strong, the reinforcement can be loaded up to the fracture stresses and then be cracked. (3) If the matrix is weaker than the interfacial and reinforcement strengths, the fracture may occur in the matrix by void coalescence and growth mechanism. In the present SWCNT-based composites, the fracture mechanism observed can be described as follows. The fracture probably initiated in the relatively weaker solder alloy matrix rather than at the soldernanotube interface or in the nanotube. The fracture can be initiated by void nucleation and propagation. When the crack reaches the nanotube-solder matrix interface, the nanotube-solder matrix interface does not separate due to the high interfacial bonding. Consequently high stresses will be developed at the nanotubes causing them to be sheared off when their failure stress is reached.



Fig. 20.19 Low magnification FE-SEM micrographs of the fracture surfaces of the Sn-Ag-Cu composite solder specimens with (a) 0.01 wt%, (b) 1 wt% SWCNT



Fig. 20.20 High magnification FE-SEM micrographs of the fracture surfaces of the Sn-Ag-Cu composite solder specimens with (a) 0.01 wt%, (b) 1 wt% SWCNT

20.3.10.2 Fracture Mechanism for Sn-Ag-Cu Composite Solders

The detailed fracture behavior of Sn-Ag-Cu composite solder specimens were revealed by extensive fractographic observations. Scanning electron microscopy was performed at high magnification to probe the fractured specimens that were deformed during tensile loading. Typical FE-SEM micrographs of fracture surfaces at lower magnification with the various additions of nanotubes are shown in Fig. 20.19. As can be seen in Fig. 20.20, the fractured surfaces of the composite specimens mainly consist of matrix dimples and fractured nanotubes. These observations are consistent with those reported in the literature where MWCNTs were employed [41]. From the fractured surface, it is observed that SWCNTs are

Fig. 20.21 Tensile joint strength values of Sn-Pb and An-Ag-Cu composite solders as functions of wt% of SWCNT

vertically aligned to the fracture surface during the tensile deformation of the composite solder specimens and this alignment might be one of the reasons for the increase in the strength of the composite solders. A similar effect has been observed in SiO_2 -based CNT composites [42].

Figure 20.20 shows that cracks run through the SWCNTs that remain in the matrix of the solders. It is evident that fracture occurred mostly by the failure of the matrix and not by the debonding of the interface between SWCNT and solder matrix. There is some evidence of partial debonding at the interface between Ag_3Sn and the lead-free solder matrix, but none at the interface between SWCNT and the solder matrix.

Because of the high aspect ratio of SWCNTs, micro cavities may form at the ends, and this is one of the ways micro cavities are formed inside the matrix. From Fig. 20.3, it is clear that Ag₃Sn has the equiaxed grain shape, compared to SWCNTs. As the deformation increases, the micro cavities that already exist in the matrix grow parallel to the tensile loading axis, and the deformation becomes localized into intense shear deformation zones in which the Ag₃Sn grains can be completely debonded to form voids. Subsequently, these voids in the shear deformation zones combine with the micro cavities at the ends of the SWCNTs to cause the failure of the solder matrix. Final failure occurs through the breakage of the SWCNTs.

20.3.11 Solder Joint Strength with Copper Substrate

Figure 20.21 illustrates the influence of the nanotube addition on Cu-solder-Cu joint strength under tensile loading conditions. It can be seen that the strength of the solder joints increased after the incorporation of nanotubes into the solder alloys. For Sn-Ag-Cu solder, the strength of the joint increased monotonically with the content of SWCNTs. The joint strength at 1 wt% was 59.1 MPa, approximately 32% higher







Fig. 20.22 Creep rupture times of the Sn-Pb and Sn-Ag-Cu composite solders as a function of wt% SWCNT

than the value for the undoped Sn-Ag-Cu solder. For Sn-Pb composite solders first increased with SWCNT content, reached a maximum, and then decreased. The maximum joint strength reached was 50.8 MPa with 0.3 wt% SWCNT, which was approximately 37% higher than the undoped Sn-Pb solder.

20.3.12 Creep Rupture Analysis

The creep rupture life of both Sn-Pb and Sn-Ag-Cu composite solders as a function of SWCNT content is presented in Fig. 20.22. Creep rupture life of both composites increased with increasing SWCNT content. In the case of Sn-Ag-Cu composite solders, the increase is monotonic, reaching a value of 14,043 min with a SWCNT content of 1 wt% which is about six times the creep rupture time for the undoped Sn-Ag-Cu solder. In the case of Sn-Pb composite solders, however, the creep rupture time first increases, reaches a maximum at 0.1 wt% CNT, and then decreases with further increase of SWCNT content. The maximum creep rupture life attained for Sn-Pb composite solder was 3324 min which is 8.29 times higher than the value for the undoped Sn-Pb solder.

20.4 Conclusions

The goal of this work was to produce and characterize novel SWCNT-reinforced composite solders for fine-pitch wafer-level packaging applications. Composites of Sn-Pb and Sn-Ag-Cu solders and SWCNTs were prepared by a sintering process. Microstructural studies of the composite solders confirmed the uniform and homogenous distribution of nanotubes in the solder matrix. Nanotube addition also resulted in grain refining. CTEs of the composite solders were found to decrease with increasing weight content of nanotubes. It was found that the melting point of composite solders was lowered with increasing content of SWCNT but the decrease is not substantial and can readily be integrated with existing manufacturing conditions. The contact angles and wettability of composite solders on copper substrates were studied. Among the solders tested, Sn-Pb + 0.08% SWCNT and Sn-Ag-Cu + 0.1% SWCNT exhibited the lowest contact angle and highest spreading area, indicating excellent wettability. Microhardness values improved with the amount of nanotube addition for both the composite solders due to homogenous dispersion of nanotubes throughout the solder matrix. Mechanical properties such as modulus, yield strength, and ultimate tensile strength showed improvement with the nanotube addition. It was found that for Sn-Ag-Cu solder, the improvement in mechanical properties increased monotonically with SWCNT content, while for Sn-Pb solder, the improvement first increased and reached a maximum before decreasing. SEM fractographs of the composite solder specimens revealed the ductile fracture mode of the composites, which is characterized by dimples. The addition of nanotubes significantly improved the creep rupture life of both Sn-Pb and Sn-Ag-Cu composite solders.

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Chapter 21 Nanowires in Electronics Packaging



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21.1 Introduction

In the light of continuous miniaturization of traditional microelectronic components, the demand for decreasing wire diameters becomes immediately evident. The observation of metallic conductor properties for certain configurations of carbon nanotubes (CNT) and their current-carrying capability [1] sets the minimal diameter of a "true" wire to about 3 nm (compare Chap. 19). Investigations are in progress even below that diameter on nanocontacts, formed by single metal atoms, i.e. quantum wires. Quantum wires can be produced by mechanical wire breaking [2] or its combination with etching and deposition [3] or other techniques. The properties of quantum wires are only about to be understood theoretically [4]. Doubtless, they are worth considering for packaging solutions in molecular electronics to come [5]. In this chapter we focus on metal wires and rods in the size range above 10 nm up to submicron diameters, evaluated already to be attractive for microelectronic packaging purposes. Techniques to generate, to characterize and to handle them, as well as their interaction with electromagnetic fields will be useful for packaging applications in the age of nanotechnology. With the wealth of information available, this review focuses on general trends and starting points for deeper study. Although the cited references are representative, they cannot be complete, since numerous activities are still ongoing to produce and to characterize new kinds of wire-like geometries from different materials.

Packaging-specific applications of nanowires (NWs) lie mainly in the fields of interconnect formation, sensor development and photonics. Given the common understanding of a wire, one would expect NWs to be usually cylindrical conductive strands with diameters below 100 nm, ideally of infinite length, but at least elongated. Whereas common wires are drawn from metal rods, NWs cannot be produced

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by wire-drawing and do not necessarily consist of a metal or one single material. But approaches to "draw" electrically conductive polymer NWs in electronic circuitry by initiating chain polymerization with a STM cantilever do exist [6].

Although rod-like colloidal structures are often mentioned as NWs in the literature, they should rather be regarded as rods or crystal needles. If they consist of metals, we include at least typical publications. Nevertheless, we exclusively focus on metallic wires and wire-like structures, even if they are fixed to a solid substrate as pillars or come as brushes or lawn-like structures. Supramolecular wire-like geometries are also depicted as "molecular NWs", like in the case of tropomyosin fibres, whose length and diameter can be directed by Na+ or Mg2+ concentration [7]. Desoxyribonucleic acid (DNA) can form molecular NWs [8] which in turn can be used as templates to produce true metal NWs (see below). Especially alien to traditional electronic engineering are charge-transfer complexes of wire-like geometries. Such supramolecular NWs, e.g. porphyrin NWs generated by ionic selfassembly, perhaps can be used in microelectronic devices thanks to their photocatalytic activity [9] and hence switchability. Those NWs fall beyond the scope of the present work. If molecular wires are largely short structures, seldom extending to the µm scale, CNTs can reach even mm length scales and are therefore just as interesting for microelectronic packaging. They have been proposed, e.g. as transistor elements in logic circuits, field-emitting structures or vias [10–15]. NWs and nanotubes can be produced from semiconductor materials like silicon, gallium nitride or others. Because of the familiarity of microelectronics with those materials, they could become even more important for sophisticated future microelectronic applications [16, 17]. Their synthesis and integration into classical planar technology, e.g. by the superlattice NW pattern transfer (SNAP) [18] and resulting application perspectives, have been reviewed recently [19-22]. Excluded from this compilation are all sorts of oxide and multicomponent oxide NWs, e.g. ZnO. We consider them to be more important for sensors due to well measurable conductivity changes with analyte adsorption [23].

Our own results in production, characterization and application of gold submicron wires in the shape of nanolawn have been included to share the excitement of NW packaging research, connecting usually separated fields like low-temperature joining and interfacing electronics with biological cells.

21.2 Nanowires and Packaging Research

Reliability issues arising from contemporary microelectronic applications have widened the scope of packaging over the last decades remarkably. Modern packaging research for the development of sustainable technologies covers photonics; optical waveguide and fibre integration; (bio)microfluidics; joining; thermal management; wire-, wafer- and flip-chip bonding; soldering and encapsulation; foil batteries; and energy harvesting and includes also solid mathematical modelling and simulation. This is shown in too many publications and annual reports to be reviewed here.

Metal NWs can be attractive for packaging in nearly every field mentioned [24] due to unique properties in comparison to mesoscaled and bulk materials. Their functional role as interfaces has been envisioned for future microelectronic applications towards 3D nanostructure integration [25]. Characteristics, production methods and proposed applications of metallic NWs have been reviewed in depth before [26–35]. Recent international research activities, evaluated and ranked by citation, indicate US leadership until 2005 [36]. Main international research institutes, engaged in microelectronic packaging in alphabetical order of the country, are:

- Interuniversity Micro Electronics Centre (IMEC), Belgium
- VTT Technical Research Centre of Finland/VTT Electronics, Finland, and Oulu University Electronics Materials, Packaging and Reliability Techniques, Finland
- Laboratoire d'Electronique de Technologie de l'Information (LETI), France
- Fraunhofer Institute Reliability and Microintegration (IZM), Germany
- Central Electronics Engineering Research Institute (CEERI), India
- Tyndall National Institute, Ireland
- Korea Advanced Institute of Science and Technology/Center for Electronic Packaging Materials (CEPM) and Samsung Advanced Institute of Technology (SAIT), Korea
- Philips Research Laboratories, Eindhoven, the Netherlands
- Institute of Microelectronics (IME), Singapore
- Industrial Technology Research Institute (ITRI), Taiwan
- · Packaging Research Centre at Georgia Institute of Technology, USA

21.3 Nanowires: Fabrication

In the plethora of production principles and approaches nevertheless, typical ones can be distinguished and will be presented below. The reproducible generation of metal NWs with identical diameters can be dated back until 1970, when Possin described metal deposition inside etched tracks of high-energy charged particles in mica and proposed to use this method to form NWs in track-etched polymers as well [37]. The technological importance of such tracks had been foreseen even earlier [38]. Many more applications for swift ions in nanoscale microelectronics have been designed independently [39]. Unilaterally etched pores in flex substrates have been proposed for improved copper adhesion [40]. For wire diameters above some tens of nanometers, the use of exotemplates is still the most important production technique so far [41]. Depending on the application, such templates can serve as the scaffold remaining after metal filling by the formation of composites, e.g. dipole storage devices [42]. But the exotemplate can also be dissolved yielding a lost form approach to produce suspended single wires or more complex metal nanostructures. Exotemplates are also suited to produce wires consisting of conductive polymers

[43, 44]. The most important (hard) exotemplates are anodic aluminium oxide (AAO) and track-etched polymer membranes (TEM).

Anodic aluminium oxide (AAO) [45] offers electrochemically tunable nanopores in a rigid matrix and therefore finds wide application for single wire and wire array production [46–49] even at a very large scale [50]. Dispersions of high aspect ratio wires can be produced [51], or layers of anisotropically conductive or magnetically polarizable materials in dielectric matrices can be prepared. Besides the standard aqueous metallization baths used, AAO is especially suited for plating from aprotic media, due to its high stability in organic solvents [52], opening a way towards electrochemical deposition of NWs consisting of metals with low redox potential (below hydrogen), like Al or Ti [53]. Due to its high stability, AAO has been also used for NW production by high-pressure filling with molten metals (for a compilation, see [35]).

Etched ion track polymer membranes (TEM) are other practically important exotemplates. Polyethylene terephthalate, polycarbonate [54, 55] and even polyimide [56] are typically used for their reproducible etchability [57]. Isodiametric and nearly monodisperse shape distributions can be generated following standard etching protocols [58]. Pore diameters in those materials reach about 0.002-1 µm for AAO and 0.010–20 µm for TEM. The density of the stochastically distributed pores in TEM can be chosen from a single pore [59, 60] up to ~109 cm⁻² depending on the desired pore diameter [61]. The percolation-based electrochemical pore etching in aluminium allows pore densities of AAO templates up to ~1011 cm-2 [e.g. commercially available ANOPORETM and ANODISK TM Inorganic Aluminum Oxide Membrane Filters]. Whereas the distribution of pores in TEM follows statistics fulfilling Poisson distribution criteria [62, 63], pores in AAO are always densely arranged. They can even be hexagonally packed over small domains and if combined with imprinting [64] even over the whole area of a wafer [65]. The typical distances between single pores (i.e. insulating material around neighbouring wires) reach the same dimension as the pore diameter for wires generated in AAO. The typical distances of pores in TEM without special precautions (e.g. mask or shutter) will always vary due to the inherent statistics of high-energy particles used. Therefore the distances between metal wires in ensembles generated with TEM, like the nanolawn we introduced [66], are varying too. With commercially available TEM (NucleoporeTM, SPI-poreTM, CycloporeTM, to name a few brands only), pore-to-pore distances vary between 0 and 2 μ m at a pore density of 106 cm⁻² on track-etched foils.

Supramolecular assemblies can work as exotemplates as well: self-assembling calix[4]hydroquinones form in aqueous photochemical solutions chessboard-like arrays of very narrow rectangular pores. Such pores have been used as silver ion-reducing templates in a process resembling photochemical development. Stable NW arrays consisting of 0.4 nm wires grown up to micrometre lengths have been prepared [67].

Molecular endotemplates [68], characterized by inner (bio-)molecular scaffolds (esp. proteins, lipids and DNA) in combination with a "toning approach" [8, 69–75], or bioparticles, e.g. tobacco mosaic virus, are suitable for metal wire production [76]

and should be mentioned as alternatives. Such a nanobiotechnological approach in combination with microelectronic technologies offers another additional advantage: the localized manoeuvrability of inorganic (conducting) structures, as shown for gold wires, driven by highly specific biochemical molecular machines (e.g. actinmyosin interaction) and a molecular fuel [77]. The metallization of (bio-)polymer endotemplates offers additional advantages for complex 3D arrangements of wires and wire networks at the microscale, due to inherent self-assembly principles and specifically directed labelling (addressing). Complex nanotubular networks as generated "naturally" by living cells on artificial substrates [78, 79] or produced artificially by manipulation of liposomes [80–82] can be transformed into hardwired circuitry by gentle metallization. This approach has been demonstrated for DNA [69] and lipid tubules [83, 84]. NWs can be grown also epitaxially at high temperatures by diffusion in grain boundaries [85]. The similar whisker growth is a notorious failure mechanism causing microelectronic reliability issues, worth mentioning in this context.

The colloid-chemical approach, effectively producing homogeneous – regarding their composition – one-dimensional nanomaterials from salt solutions, is usually diminished to the lower nanoscale and low aspect ratios. However, even several µm long gold wires measuring only 15 nm in diameter have been produced by chemical reduction [86]. Seed-mediated growth has been described for gold rods when the seeding nanoparticles have been attached to a solid substrate [87]. The introduction of rod-like micellar templates, e.g. the cationic detergent CTAB, allows the production of suspended cylindrical gold NWs [88]. Comparably long silver wires have been produced in a diameter-controlled (20–500 nm) manner by a modified polyol process [89] using different growth-controlling modifiers. A somewhat similar molecular shielding (templating) strategy, i.e. soft exotemplates, comprises the use of temporarily arranged supramolecular ensembles in block-copolymer solutions [90]. For a review of nanostructure-producing techniques with block-copolymers, see [91].

Classical photolithography and successors like deep UV lithography [92, 93], colloid mask/nanosphere lithography [94] and competing technologies, with nanoimprint (cold) lithography being the most ripened one among them [95], have been used to generate metal NWs directly on planar substrates. Typically, the NWs and NW grid arrays produced are oriented parallel to the substrate plane. Hence, they can be useful for applications as subwavelength metal gratings or directly as plasmonic waveguides and photonic crystals [96, 97] depending on a guiding medium in close proximity. In a top-down approach, photolithographically generated trenches in a resist layer can be filled forming stretched wires on a planar substrate [98]. A maskless alternative based on substrate steps to fabricate wires by deposition has been introduced as step-edge lithography (SEL) [99], the principles of which have been used to produce molybdenum NWs (15 nm-1 µm diameter and length up to 500 μ m). NW composites have been formed starting with electrodeposited molybdenum oxide wires and their reformation in hydrogen and subsequent lift-off in polystyrene layers [100]. Palladium wires, embedded in a cyanoacrylate film sensitive towards hydrogen, have been prepared as well

[101]. A similar growth of metal wires occurs along material cracks [102]. Among maskless NW production techniques, the direct writing approach, either by direct atomic metal deposition [103], e-beam-induced CVD [104] or indirect structuring of metal substrates with small molecules via dip pen technique [105], should be mentioned. With a sweeping AFM cantilever, copper NWs have been assembled from deposited nanoparticles on a polymer substrate and cut afterwards at will [106]. Direct writing techniques have been under intense investigation. To overcome seriality drawbacks, e-beam arrays [107] and cantilever arrays [108] have been proposed. Near-field laser nanofabrication has been scaled down to 80 nm resolution [109]. Two-dimensional photonic crystal structures in polymer have been produced by a combination of interference and e-beam lithography techniques [110]. Mean-while, similar structures are becoming attractive for wire fabrication via nanoimprint techniques.

Other techniques to generate metal wires include assembly from suspended metal particles by dielectrophoresis [111, 112]. Plasma-enhanced growth techniques, e.g. by vapour-liquid-solid growth or vapour-solid transitions, cannot be covered here but could become more important for packaging, if applied at reduced temperatures. Single crystalline Ni NWs with diameters of 40 nm confined inside multiwall CNTs have been grown by a CVD process with lengths of some tens of micrometres [113].

21.4 Metal Nanowires: Materials

Nearly every electrochemically reducible cation has been deposited inside the pores of different exotemplates already as a wire.

The galvanic deposition of metals inside nanopores has been thoroughly investigated from aqueous electrolytes [114] and from nonaqueous ionic liquids [115] extending the range of available wire materials. Therefore, besides the colloidchemical approach suitable for mass fabrication of nanoscale metal rods and wires [88], exotemplate methods can be used as well to prepare single wire contacts [116] or special polymer composites, requiring gramme amounts of monodisperse wires [50].

Envisioned applications of periodic arrays of magnetizable wires [117] embedded in a dielectric matrix (e.g. AAO) are information storage via perpendicular data recording, characterized, e.g. for arrays of ferromagnetic Ni and Co NWs, by high remanence and coercivities [118, 119]. The preparation of similar e-beam-written pillar arrays proposed for high-density data storage [120] is much more time consuming and hence expensive. Based on their giant magnetoresistance properties, magnetic multistack layers have been considered as high-density storage elements [121]. Magnetic polymers are another application of polymer composites, e.g. with Ni wires [122]. The integration of oriented wires into polymer films can be used for anisotropically conductive interposer fabrication useful for chip interconnection [123]. (See also Chap. 22).

21.5 Segmented Metal Nanowires

Such stacks, representing multilayered wires, can be prepared with exotemplates. The common practice of sequential layer plating of different metals or crystal morphologies yielding functional multilayers works well for exotemplate wires, too. Segmented NWs may possess different spectral characteristics, depending on the orientation of polarized light in relation to the axis of the wires [124, 125]. They therefore can serve as embedded identification tags (barcodes) or labels, without disturbing the usual fluorescence detection of biomolecules for lab-on-chip applications [126, 127]. With the stable material composition of each single wire in a large batch, alloy preformation for solder pastes, otherwise difficult to accomplish, seems easy. Usually observed component demixing upon storage with NWs can be prevented. A wet chemical, electroless plating approach also can yield multilayered, rather stacked wires [128] with a similar application potential. By a combination of template techniques and etching, segmented wires have been produced with "on-wire lithography" [129], bearing potential for applications in plasmonics, since etched gaps can be selectively filled with different dielectrics. The catalytic activity of NWs and their use as catalysts [130] and their stability in microreactors have been shown [131].

21.6 Metal Nanowires: Structure and Configuration

NWs grown in free solution by anisotropic crystallization will always be single crystals, possessing smooth crystal planes. On the contrary, the structure of NWs cast inside a hard exotemplate naturally will reflect the inner pore structure and arrangement typical for a lost form approach as shown for nanolawn, i.e. nanowires on a flat substrate (Fig. 21.1).

As for metal plating with commercial baths, grain sizes can be different, depending on bath composition, temperature, current density and regime. Extreme differences can be illustrated by smooth, amorphous pore filling with a commercial platinum bath and coarse grain pore filling with a gold plating bath (Fig. 21.2). Obviously, conditions can be found to generate wire-like crystal needles with diameters of single grains according in dimension to the template pore diameter. With overplating, large single crystals emerge. That has been described before for larger wires [47, 132].



Fig. 21.1 Generation of a metal nanolawn on a track-etched polymer template. (a) Isoporous membrane, (b) sputter coating, (c) plating, (d) stripping



Fig. 21.2 Crystallinity of metal wires plated in track-etched polymer pores. (**a**) Fine crystalline (Pt); (**b**) stacked grains of different sizes (Au); (**c**) FIB dissection of a typical gold wire, as in **b**; (**d**, **e**) single crystals grown inside pores (Au); (**f**) single Au crystal grown by overplating. Scale bars \mathbf{a} -**e** 1 µm, **f** 2 µm

21.7 Metal Nanowires: Mechanical Properties

The mentioned twinning is a good illustration of altered mechanical properties of an entire (nano)wire, caused by its single grain spanned diameter. The electrical conductivity of NWs will be crucially influenced by the electrons' mean free path and hence crystal defects [133]. The influence of crystal growth direction on twin formation during plating has been studied in this context for single crystalline Cu, Au and Ag NWs with 30–300 nm diameters [134]. In our cases, probably, plating bath additives are segregating at the grain boundary during annealing and facilitate crystal plane slip. Properties of single metal grains in wires and layers are currently under intense study [135], since necessary high-resolution analysis techniques, e.g. nanoindentation and EBSD detection, in scanning electron microscopy are becoming broadly available only now.

Contemporary techniques to characterize mechanical properties of one-dimensional nanostructures like nanotubes and NWs have been recently reviewed [136]. Since NWs have much in common with single grain layers, theoretical considerations [137] are similar. Their deep understanding is essential for micro-nanoreliability issues in future packaging [138–140]. Theoretical approaches for planar single grain layers [141] and gold NWs [142] should be identical. More investigations, as requested by Uchic et al. in 2004, are still necessary, to separate the critical influence of sample size from the observed material properties [143-145]. As already mentioned, the wire preparation conditions heavily influence the grain structure and crystallinity. So high-pressure injection cast wires are rather single crystalline [146].

21.8 Metal Nanowires and Temperature

So far, melting point depression, known from nanoparticle behaviour [147], has not been observed for NWs yet. However, Rayleigh instability, i.e. fragmentation of spatially confined NWs into loose pearl-chain-like structures [148], and – at least for



Fig. 21.3 Recrystallization of single wires of a typical lawn structure (Au). (**a**) Wires after template removal (at 65 °C), diameter corresponding to pore size. (**b**) Sample passing 400 °C exposure. (**c**) Sample recrystallization after 600 °C, growth of large crystals fed by small basal grains. (**d**) Twins found after recrystalization at 482 °C. Duration of all incubation steps, 10 min. All scale bars 1 μ m

multimetal NWs – a dramatic increase of intermetallic diffusion effects have to be considered. But also for homogeneous NWs, heating can cause typical recrystallization rearrangements. We observed dramatic grain growth at the tip of multicrystalline wires (Fig. 21.3) and crystal plane slip, i.e. twinning without additional mechanical load. Similar crystal plane slip has been attributed to mechanical stress during sample preparation [47] and has been surprisingly predicted for NWs of much smaller size [149].

21.9 Electrical Properties

Concerning the tip geometry of any NW, the advantages of miniaturized electrodes (and electrode arrays) for charge injection is obvious. Sharp wire tips are common in electrochemical scanning probe microscopy and with highest resolution in STM. Arrays of oriented carbon nanotubes found their way into field-emitting devices. Their metal counterparts have been proposed for field emission too [150–154]. Besides the tip geometry, surface enhancement by NW-decorated electrodes has been investigated as well [155].

Concerning their current-carrying capacity, metal NWs will be rather limited in comparison to CNTs. If moving top down along the size scale, common wire handling for (wedge or ball) bonding with diameters well above 5 μ m (usually 12.5–17.5 μ m) is still challenging (compare Chap. 31). However, the reliable current-carrying capacity of much smaller metal microwire bundles, configured like brushes, has been demonstrated earlier with via feedthroughs for board level interconnects by copper deposition in etched ion tracks [156]. Precise conductivity measurements of individual metal NWs became accessible by the single pore etching and plating, established at GSI Darmstadt, Germany [157]. Theoretical modelling in good agreement with experimental data has been done, e.g. for Bi NWs [158]. A nanoindent contact has been applied on electrochemically filled and polished AAO templates and used in systematic single wire measurements [159], where wire length

had been reduced down to 100 nm by polishing. In this way, significant charges up to 109 A/cm² could be injected into single Co/Cu NWs to study magneto-transport properties. Other measurement techniques often suffer from contact resistance problems. The majority of measurements on NW conductivity has been undertaken on stochastically arranged wires, thrown on a substrate and contacted by connector depositions [160] or on planar electrode arrays, making contact with appropriate laying ones by a subsequent lithography-based metallization. FIB deposition has been used for that purpose as well, as, for instance, on 200 nm wires with preferably <111> orientation [161]. A comparison of resistance at room temperature for platinum NWs obtained by different authors [162] shows significant differences, reaching from 61 to 5000 µOhm-cm resistivity. The need of standardized measurement procedures is evident. A stage design with fixed contacts has been demonstrated recently to enhance reliability and throughput with preformed resist trenches. Wires longer than 60 nm have been arranged in appropriate positions [163]. A NW manipulation technique for four-point measurements with individually moved tips has been presented before [164]. Obtained data are detrimental in understanding and design of future devices and are practically important already to develop sensors, based on analyte-depending properties of semiconductor materials [23, 24]. Conductivity changes of neat gold NWs have been used for ionic mercury detection [165]. To our knowledge, a systematic study of individual NWs, esp. single crystalline wires, i.e. grains along different crystal axes, is still lacking. However, it should be important for reliability issues in nanoelectronics (Chaps. 2, 3, 4 and 5) and future sensor developments.

21.10 Manipulation of Nanowires

For applications of NWs as admixtures in a composite, e.g. to manage electrostatic or magnetic properties or the conductivity of a polymer, they certainly do not have to be manipulated individually. However, if NWs have to be placed one by one and specifically to ensure the envisioned function, appropriate touchless handling techniques are necessary. The contact-free manipulation of sensitive objects like metal NWs requires the combination of different physical principles, allowing directed transport, orientation and fixation. Similar approaches have been developed successfully for single cell manipulation and measurement earlier [166, 167]. Main physical principles for contact-free handling of delicate individual components are magnetophoresis, electrophoresis, dielectrophoresis, capillary forces and interaction with focussed laser light (laser tweezers), often in combination with hydrodynamic streaming. For a review, see [168]. Dielectrophoretic field cages inside fluidic channel structures are especially suited to sort and align different types of microand nano-objects individually [169] as has been well proven for living animal cells (for review, see [170]). Positive dielectrophoresis has been used to assemble gold wires from 70 to 350 nm in diameter in electrode gaps [171-173]. Magnetic fields have been applied to arrange and to assemble large quantities of Ni NWs in parallel or, with a bit more luck, even individually [174]. Combinations with independent solution structuring, e.g. by a liquid crystal [175], can improve the alignment and ordering of large numbers of particles, important for collective interaction phenomena of NWs with external electromagnetic fields. Surfactants can be used to build assemblies of NWs [176]. Since gold can easily be modified with thiolates, gold-capped NWs can be labelled for self-assembly [177]. But placement alone does not yet yield the trick of contacting NWs.

21.11 Nanowires: Bonding and Joining

It seems as if NWs will require specialized bonding or joining techniques to be contacted reliably. Surprisingly, ultrasonic bonding in an almost conventional manner has been demonstrated to produce low contact resistance between 1-µm-long carbon nanotubes and metal electrodes, reaching 8–24 kOhm [178]. Nevertheless, it is obvious that practical applications of NWs in electronic packaging would require some paradigm shift, new approaches and technical solutions. But metal NWs arrived already at the level of practical applications: interconnect formation has been demonstrated with 30 nm nickel NWs, generated with AAO and assembled magnetically between neighbouring contact pads. The resistance of the formed contacts after annealing under reducing conditions decreased from >10 MOhm to ~800 Ohm [179]. The use of vertically aligned NWs in an adhesive interposer foil has been envisioned [180] and realized [181] independently. We could show a new technical principle of decorating flip-chip bonding pads directly with NWs, omitting external force fields for their arrangement, to be successful for joining of gold nanolawn model structures [66] (Fig. 21.4).

Deleterious effects of recrystallization phenomena (see below), crucial for single wire contacts, can obviously be overcome and can even be used if applied with intercalated NW ensembles. The observed contact formation is based on Ostwald ripening, as indicated by FIB/SEM dissections (Figs. 21.3 and 21.4). Solid phase diffusion bonding, well established in microelectronics, hence can supplement the contact formation techniques described above, even without large pressures to be applied.

However, intermetallic diffusion and corrosion have to be considered as to be crucial for interconnects between individual NWs. Four different bonding techniques for individual single 100 nm gold NWs have been compared regarding their practical feasibility and efficiency [182], still leaving the need for further research.

Concerning the wire-to-wire bonding, gold or Au-Ni-Au wires have been joined together and soldered under reflow. Resistance measurement (lithographically patterned contacts) indicated solder contact formation for 200 nm diameter wires. The resistance of individual contacts was reduced to about 13 Ohm, starting from 300 to 106 Ohm before reflow [183].



Fig. 21.4 FIB dissections of intercalated wire-decorated surfaces (all gold), using flip-chip bonding principle. Bonding at ambient temperature with pressure as indicated. (a) Close-up for 100 MPa sample. (b) Intergrain diffusion and contact formation after annealing. All scale bars, 1 µm

If the NW template can be generated directly on surfaces to be decorated with NWs, the previous discussion on manipulation and joining to connecting electrodes becomes obsolete. A technique to generate nanoporous AAO spots directly on wafer substrates has been presented recently. Copper NWs have been generated in those AAO pads and proposed for contact formation with solder pads in a flip-chip bonding approach [184, 185]. Doubtless, microinterconnects by multiple metallic NWs will be useful for fine pitch applications.

21.12 Nanowire Interaction with Electromagnetic Fields

Due to the high aspect ratio of NWs, resonance frequency shifts can be observed for structures with dimensions below one fourth of the wavelength of the external field. Non-linear interaction of NWs with light- or high-frequency electromagnetic fields, useful for generating active and passive photonic structures [186] or HF structures [187], has been described previously, e.g. for enhancing the sensitivity of Raman scattering over several magnitudes in chemical analysis (SERS) [188, 189]. The possibility to use NWs to produce stop-band filters or antenna structures [190–192] should be mentioned as well. NWs could be used in new integrated optical devices because of their negative magnetic permeability and dielectric permittivity in the visible and the near infrared if arranged into parallel pairs even randomly in a matrix [193]. Resonance phenomena of NWs in the infrared have been discussed in depth and investigated experimentally on copper and gold NWs of 100 nm diameter [194]. Significant antenna-like plasmon resonances and skin effects have to be considered for practical applications in light confinement or estimation of effective

refractive indices in the antennas surrounding. For a review of general near-field optical properties of nanostructures, see [195].

The optical parameters of nanorod dispersions are changing according to the degree of orientation in the dispersion. The degree of orientation can be externally influenced by electric fields [196]. An observed change of phase shift as well as selective absorption could be useful in preparation of shielding materials to prevent electromagnetic interference (EMI). Polymer composites of conductive CNTs [197] and of copper wires in flex have been proposed [198]. The application of carbon nanotube NWs and nanotube antenna arrays, consisting of individual wires of different length and hence different resonance frequencies has been proposed for in/out signal demultiplexing and wireless interconnection of integrated nanosystems to the microelectronic periphery. The authors point out that this approach could translate interconnection challenges from the spatial to the frequency domain, consequently eliminating a technological bottleneck [199].

Size-dependent magnetoresistance measurements of single Ni NWs (30 and 200 nm diameter) bridging Ni electrodes have been studied at 10–300 K [200]. With decreasing diameter, transverse and longitudinal magnetoresistance differ from values obtained for thin layers. Perpendicular giant magnetic resistance (GMR) studies on layered Co/Cu nanowire arrays have been undertaken, e.g. by [201]. The results obtained indicate the attractive possibilities of NW arrays for new memory device architectures.

21.13 Future Prospects

Due to the known field inhomogeneities at electrode edges and spherical vs. parallel diffusion at ultramicroelectrodes, ensembles of NWs, depicted as nanoelectrode ensembles, have been evaluated for applications in analytical chemistry [202] and for applications in wet chemistry and gas analysis.

Biophysics and cell biology are other exciting application fields for NW-decorated surfaces, since nanotopographies are known to trigger cell differentiation or even phagocytosis [203]. Traction forces generated by moving animal cells have been measured with microneedles [204] and could be accessible even more accurately on NW arrays.

In cooperation with cell biologists, we started to study the behaviour of mammalian cells on a gold nanolawn [205], especially the influence on cell-substrate adhesion. For primary mouse astroglial cells, very close cell-cell and cell-substrate contacts have been observed [79] (Fig. 21.5). Considering the growing importance of interfaces of microelectronic systems with living tissue [206], those contacts can be interesting for neuroprosthetic device development – one more area of rising importance for microelectronic packaging.



Fig. 21.5 Primary mouse astroglial cells growing on a nanolawn (Pt). (a) SEM image of cell typical spreading towards confluency (bar, 20 μ m). (b) Close-up of cell-substrate contacts (bar: 2 μ m). Cell culture and sample preparation by U. Gimsa and L. Jonas, University of Rostock, Germany

21.14 Conclusion

NWs can be regarded as promising materials to supplement existing packaging applications such as flip-chip bonding, anisotropically adhesive foils and electromagnetic shielding. Moreover they open up new vistas for future applications.

The properties of a single NW will be defined by the grains or even by the single grains it consists of. Therefore, their/its orientation and existing grain boundaries have to be taken into account for practical application and design.

The reliability of future nanostructure-based components will depend on the knowledge of the thermo-mechanical behaviour of single metal grains. To obtain the necessary data, NWs are well-suited objects to study.

The characterization and measurement of typical electrical properties like electrical conductivity or resistancy and thermo-mechanical properties require reliable techniques for electrical connection and mechanical clamping.

The sorting, manipulation and placement, i.e. assembly of individual NWs, demand touchless and contact-free handling to avoid their damage, contamination or destruction. External electromagnetic fields are well suited to generate necessary forces for doing so.

Due to high aspect ratio, i.e. the anisotropy of NW properties interacting with electromagnetic fields, NWs and NW arrays offer applications in signal processing and storage.

The collective behaviour of NWs in regular arrays or statistically arranged brushes and nanolawn opens up new applications in photonics, EMF shielding, sensorics and biomedicine.

To summarize, focussed research with NWs can pave the way for low-energy bonding techniques, high-density interconnects, high-density (spin) data storage, molecular electronics, biomedical electronics and life sciences – what promising prospects for microelectronic packaging!

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Chapter 22 Nanowire ACF for Ultrafine-Pitch Flip-Chip Interconnection



Kafil M. Razeeb, Jing Tao, and Frank Stam

22.1 Introduction

Semiconductor chip packaging has evolved from single chip packaging to 3D heterogeneous system integration using multichip stacking in a single module. One of the key challenges in 3D integration is the high-density chip interconnect. Anisotropic conductive adhesives/film (ACAs/ACF) technology is one of the low-temperature, fine-pitch interconnect methods, which has been considered as a potential replacement for solder interconnects in line with continuous scaling down of the interconnects in the IC industry.

Anisotropic conductive adhesives/films (ACAs/ACFs) consist of composite materials comprising electrically conductive fillers in a non-conductive adhesive base. There are mainly two types of ACAs [1]: (1) a homogeneous mixture of conductive fillers and the adhesive and (2) the conductive fillers distributed in an orderly fashion in the adhesive base. Commercial particle-dispersed ACAs belong to the first type of ACAs and are the most developed ACA technology with wide applicability for chip-to-substrate packaging particularly in the display industry. Extensive studies exist comparing material constituents, fabrication methods, bonding processes, conductions mechanism and applications [2]. The advantages of ACA over solder interconnect include fine-pitch capability, lower processing temperature, less environmental impact, reduced cost and decreased intermetallic (IMC) reliability concern. However, these conventional ACA/ACF materials are facing challenges to accommodate the reduced pad and pitch size due to the micron-scale particles and the particle agglomeration issue [3]. The limitations of these materials are such that the achievable pad/pitch size may not fulfil the ultrafine-pitch 3D interconnection (<50 µm) requirements. The open/short failures due to the unpredictable number of

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trapped particles in the interconnection and the occurrence of particle agglomeration in the small pad gap are limiting the specifications.

This chapter discusses the development trends of ACA technologies from commercial particle-dispersed ACAs to vertical wire ACFs and is introducing the concept of nanowire ACF. As a well-developed electrically conductive bonding agent, commercial particle-dispersed ACAs have widely been used in the display industry for more than 30 years. Vertical wire ACFs belong to the second type of ACAs, and they have been developed in a patterned adhesive matrix as a Z-axis interconnect solution for even finer-pitch size applications than achievable with solder interconnect. Compared to particle-dispersed ACAs, the vertical wire ACFs have a higher density of conductors in the interconnection and also eliminate the particle agglomeration problem [4]. However, due to the limitation of optical lithographic patterning and cost issues, high aspect ratio vertical wires with submicron diameter (<1 μ m) will be difficult to obtain [5]. Therefore, research on a new type of interconnect material - nanowire anisotropic conductive film (NW-ACF) composed of high-density metallic nanowires that are vertically distributed in a polymeric template – is carried out to tackle the constraints of the conventional ACFs and serves as an inter-chip interconnect solution for potential threedimensional (3D) applications. In this chapter, the fabrication techniques and early research on these unique nanowire-based anisotropic conductive films will be introduced. The application of the NW-ACF in chip-to-chip bonding with their electrical and mechanical properties will be discussed in detail.

22.2 Anisotropic Conductive Adhesive/Film (ACA/ACF) Technology

Anisotropic conductive adhesive (ACA) is a Z-axis interconnect material which can provide direct electrical connection between the two bonding surfaces. Conventional ACAs have spherical conductive particles of $3-15 \,\mu\text{m}$ in size, which are randomly dispersed throughout a polymer matrix with a filling ratio of 5-20%. This results in unidirectional electrical conduction when the film is compressed and when the particles form an interconnection between the bond pads. Figure 22.1 shows a



Fig. 22.1 Schematic showing the flip-chip interconnect formed by the particle-based ACA between the IC and the substrate; the spherical particles are trapped and deformed to make connections between opposite pads [6]

schematic of the flip-chip interconnects formed by the conventional particle-based ACA between the IC and the substrate. The electrical connection is formed by the trapped conductive particles between the opposite bond pads, and the electrical insulation in X-Y plane is maintained due to the highly dispersed particles in the polymer. The mechanical connection is provided by the polymer matrix due to its adhesive properties.

ACAs have been considered as a potential replacement for soldered interconnects [7] and have been widely used as a flip-chip interconnect technology for chip-tosubstrate packaging applications. The particle-dispersed ACAs have been used as packaging technologies in flat panel displays for more than 30 years [8-10]. The main technologies using ACAs include chip-on-flex [11–14], chip-on-glass [15–17] and chip-on-board [18-21], flex-on-board/glass [22, 22] and chip-on-chip [24]. The main advantages of the particle-dispersed ACAs are a low process temperature (<200 °C, which is also suitable for very thin flex substrates) and a fine-pitch capability. Meanwhile, it eliminates the need for underfill as compared to solder technology; hence, it greatly decreases the packaging cost and simplifies the processing. It also provides an acceptable electrical and thermal joint resistance and relatively easy rework/repair [9]. Microparticle-based ACAs are proposed for advanced packaging applications, such as wafer-level packages and 3D IC integration. ACAs composed of benzocyclobutene (BCB) and conductive particles can be spin- or spray-coated onto the full wafer and bonded at wafer level to realize both electrical and mechanical connections [25]. The modified ACA solution with high fluidity can be directly coated on a wafer with a blade coating method, and the singulated chip with the coated ACA can be subsequently bonded to the substrates using thermocompression bonding [26]. These approaches greatly eliminate the process steps and time compared to conventional ACF technology. Furthermore, the BCB-type ACF has also been proposed for 3D chip stacking to interconnect between TSV and MEMS dies [27].

With the trend of I/O miniaturization in the IC industry, the conventional ACF faces challenges to accommodate the reduced pad and pitch size. With decreased particle density, two problems have been reported: electrical opens due to reduced number of particles trapped between the connecting pads and electrical shorts due to the higher probability of particle agglomeration in the narrower pad gaps. New types of ACAs have been developed to solve these problems. A nanofibre-incorporated particle-based ACF was developed in order to suppress the conductive particle movement during resin/polymer flow and to improve the fine-pitch capability [28-30]. The achievable pitch size was 25 μ m with a ~1000 μ m² pad size. To improve the small pad capability, a magnetically aligned anisotropic conductive adhesive with a column structure was considered as a possible solution by applying small particles with high density [31]. For spherical particles, the particle size cannot be smaller than $2-3 \mu m$ to achieve an adequate bond line thickness. To overcome the disadvantage of non-metallurgical electrical interconnect and to provide sufficient current-carrying capacity, flux function-added solder ACFs have been proposed to form the metallurgical joints with the pads [32, 33]. By reducing the particle size to nanometre size, nano-silver (Ag)-filled anisotropic conductive adhesive [34] has
been developed with a low sintering temperature (<200 $^{\circ}$ C). By incorporating the organic self-assembly monolayer in such nano-Ag ACA, the electrical resistance is further reduced with a high current-carrying ability.

22.2.1 Limitations of ACA

Failures in ACA interconnection have been reported due to oxidation of conductive particles, coplanarity issues between the chip and substrate, thermal stress due to CTE mismatch, post-assembly residual compressive stresses, polymer expansion due to moisture absorption and degradation of the polymer at high temperatures [35]. Meanwhile, to deal with the smaller pad/pitch requirements, higher particle densities also have their limitations as particles could easily agglomerate during the bonding process and cause short-circuiting in the X-Y plane [3]. For conventional ACAs, the electrical connection is formed by physical contact of the particles with the metal surfaces, resulting in unstable contact resistances due to a loss of compressive force (e.g. due to humidity expansion) [36].

22.2.2 Vertical Wire ACFs

Vertical wire ACF is based on conductive wires orderly distributed along the z-direction in the adhesive base. Its fabrication requires a more complicated manufacturing process, with a vertical channel-based structure (like vertical through-holes), which is required before filling these channels with electrically conductive material. This novel structure, consisting of micro-/nanoscale conductive wires, allows for smaller pitches and pad areas and creates electrical pathways between pads while providing insulation in the x-y plane [37, 38].

22.2.3 Initial Patent and Concept

Fine-pitch, low porous polymer sheets have been proposed to fabricate the ultrasmall size (0.1–50 μ m) conductors along the straight-line pores to form anisotropically electrically conductive article in 1986 [39]. The vertical wire ACF concept was patented by Takayama et al. [40] in 1992, when the ACF with through-holes filled with metallic material was proposed. The through-holes were made by piercing the film in the z-direction, while the metallic substance filled in the holes formed conductive pathways. In literature, diameters of the through-holes were found to be generally from 15 to 100 μ m, and the film thickness was 5–200 μ m. The insulation film material can be thermosetting or thermoplastic resins, and the metallic substance can be various metals such as gold, silver, copper, tin, lead, nickel,

cobalt, indium and various alloys of these metals. The through-holes can be formed by a mechanical process, such as punching, dry etching, using a laser or plasma beam or chemical wet etching using chemicals or solvents through a mask or photoresist pattern. The holes can be filled by various techniques, such as sputtering, vacuum evaporation and electroplating. Because of the large hole diameter, it should have a rivet-like shape so that one end of the hole can form a bump-like projection to prevent the metals from falling off [41, 42]. The minimum pitch of these conductors was 25 µm, which was composed of 18 µm diameter Cu pillars with 70 µm height. These micro-size Cu pillar conductors stand straight to electrically conduct between the chip and board and result in a contact resistance of 20 m Ω . The interconnections also show a stable contact resistance and insulation properties under hightemperature and humidity environments. Due to the large ratio of metal conductor in this ACF, the die shear strength is be compromised in such interconnects due to the low ratio of adhesive.

The other type of the ACF composed of a plurality of minute pores of about 0.01–0.2 μ m diameter and a predetermined depth of about 1–100 μ m can be formed by anodic oxidation of Al substrate, which was firstly patented by Yoshida in 1993 [43]. The anodic oxidation film of, e.g. Al₂O₃ has a plurality of pores formed in a honeycomb pattern and each extending in the thickness direction of the film with the diameter less than 0.2 μ m and a pitch between the pores of 0.3–0.4 μ m. The conductive materials of, e.g. Ni and Au are filled in the pores by electrolytic deposition method and can have the protruding portions to provide a connection point without applying pressure.

Ishibashi et al. [4] reported the fabrication process for the ACF with a Ni bump array using photoresist patterning. The array of Ni bumps were obtained by Ni electroplating in open holes of the patterned photoresist on a substrate. The holes have a diameter of 12 μ m at 20 or 40 μ m spacing and with typical bump heights of 9–20 μ m. The ACF is prepared by laminating a 30 μ m thick epoxy adhesive film onto the metal bumps followed by peeling off process. The difficulty lies in the transferring process, which requires pressure during lamination to not let the adhesive make contact with the substrate surface and prevent the metal structure from deformation.

A research group in LETI developed the so-called Z-axis ACF with pyramidal tips for bumpless chip connection and wafer-level interconnection [37, 44, 45]. The conductors are composed of 10-µm-long Ni inserts with 10 µm diameter and 30 pm pitch by photolithographic method. With the gluing and thermocompression process, the Z-axis ACF is reported to achieve a contact resistance of 6 m Ω with 50 × 50 µm² pad and a stable contact under thermal cycling. The challenges for this technology are reported as the damage caused by the shape tips of the Ni inserts into the passivation layer on the chip and the increased contact resistance due to the effect of humidity exposure.



Fig. 22.2 Concept of nanowire ACF as compliant interconnects between the dies/substrates

22.2.4 Nanowire ACF

Despite that good process feasibility and connection properties can be achieved for vertical wire ACF, there are technical challenges in achieving an even smaller hole structure (below 1 µm diameter) with a high aspect ratio when the standard photo-lithography method is used. In addition, the micron-size metal posts or flakes are not structurally compliant, which can result in reliability issues at an elevated temperature [46]. Therefore, polymer films with the nano-hole/pore structures, which can be filled with metals, are proposed to form nanoscale conductors in the ACF. Figure 22.2 shows the schematic of the vertical nanowire-based ACF concept to connect between the dies and substrates through to the opposite electrodes as compliant interconnects.

Nanowires are mainly used for packaging-specific applications in the field of interconnect formation [47]. Yousef et al. [48] developed the vertical via interconnects in a flexible PCB with high aspect ratio (300:1) Ni nanowires. With 10% via metal fraction, the resulting electrical resistance per via is 0.07 Ω (via dimension, $26 \times 26 \ \mu\text{m}^2$, and thickness of 10 $\ \mu\text{m}$). Xu et al. [49, 50] reported copper nanowire arrays grown on conductive pads through an anodic aluminium oxide (AAO) template to form the metal nanowire bumps. By utilizing flip-chip bonding for two nanowire bumps, the nanowire to nanowire interweaving "Velcro" type contact can be formed at low temperature with a contact resistance of 0.35 Ω . Such interconnects were also reported with a bonding strength of more than 5 N cm⁻² at room temperature bonding [51]. Fiedler et al. [52] further studied the intercalated nanowires after annealing and found that with increasing annealing temperature and/or time, fusion of the nanowires can occur.

Nanowire arrays embedded in a polymer template have been proposed to form an ACF material by several research groups in the last decade. Maekawa et al. [53] studied the potential of poly(ethylene terephthalate)/Cu hydride membranes as an ACF by probing the four-terminal resistance of the film in the vertical direction, and the resultant resistance is in the range of 10^{-7} – $10^{-8} \Omega/cm^2$ for Cu wires with 12 µm height and 200 nm in diameter and wire density of 3×10^7 cm⁻². A similar feasibility study has been conducted by Sykes et al. [54] for the polycarbonate/Au hybrid membranes as anisotropic conductors. They also verified experimentally that no conduction exists between neighbouring wires despite a 25 µm spacing. The research group in ITRI [55], on the other hand, proposed fabrication of nanowire

ACFs based on AAO templates to obtain Ag/Co multilayer nanowire arrays, magnetically aligning the nanowires after the removal of AAO and then refilling with low viscous polyimide through the vertically aligned nanowire array to achieve a nanowire-polyimide ACF. The reported Z-axis resistance is less than 0.2 Ω , and X-Y insulation resistance is 4–6 G Ω for the fabricated film. Meanwhile, such a nanowire ACF was proposed for fine-pitch flip-chip bonding between the chip and substrate with the application of additional non-conductive paste (NCP) [56]. The effective properties of nanowire ACF were modelled by the rule-of-mixture (ROM) technique, and the optimization of the material- and process-related properties were carried out by finite element modelling and a quadratic regression model to minimize warpage and peeling stress and maximize contact stress for the proposed package [46]. Stam et al. [57] reported the Cu nanowire-based ACF for the electrical connection between the gold stud bump and Au layer with a resultant electrical resistance of 2.5–3 Ω . In addition, Razeeb et al. [58, 59] have explored the viability of Ag nanowire- embedded polycarbonate template as thermal interface material, which is regarded as an additional benefit to apply such nanowire composite material for an interconnection purpose with good thermal properties. Thus the concept of nanowire-embedded polymer material as an ACF material for low-temperature, finepitch interconnect applications has shown good prospects.

22.3 Fabrication of Nanowire ACF

In 2005, our group started a research activity in the area of nanowire ACF through European Union (EU)-funded project e-CUBES [60] and continued in a subsequent project e-BRAINS [61]. One of the challenges in both projects is to develop low-temperature bonding process for 3D integration of functional layers, and thereby we proposed the development of nanowire-based anisotropic conductive film (NW-ACF) as an interconnection medium.

Fabrication of the NW-ACF was achieved by using the commercially available track-etch porous membranes as templates. Templates with pore diameters, ranging from 0.01 to 30 μ m, are commercially available for the polycarbonate templates with a thickness varying from 6 to 30 μ m. As the nanowires will resemble the same shape and size of the pores, the pore diameter should be carefully considered to obtain the fine-pitch conductors and should not be too small to compromise the electrical performance. Copper was selected as the low resistivity metal to be deposited in the pores as nanowire conductors. The resistivity of copper (Cu) is reported to increase substantially, when the line width (or diameter of the nanowire) decreases below ~100 nm [62]. Therefore, templates with an average pore diameter of ~200 nm were selected from the commercially available polycarbonate membranes.

To achieve a NW-ACF, one big challenge would be to obtain a high filling ratio of pores during electrodeposition. According to the research work by H. Yosef [48], the filling ratio in the template mainly depends on the electrodeposition process parameters, the quality of the seed layer and the wetting of the template. The other



difficulty to prepare the NW-ACF is to remove all metal residues on both surfaces of the film.

Figure 22.3 illustrates the schematic of the process steps developed for NW-ACF fabrication. Firstly, a 400 nm thick Ag layer was evaporated in a Temescal FC-2000 E-beam evaporation system. This serves as the cathode and the seed laver for growing nanowires. Then the Ag-coated template was fixed in a home-made sample holder for electrodeposition. The Teflon sample holder provides a solid support, where a cut-to-shape copper foil formed a back contact to the seed layer on the template with a plastic O-ring. The geometric area exposed for deposition is $\sim 12 \text{ cm}^2$. The anode was pure copper foil (dimension of $50 \times 50 \times 2$ mm³, 99.99%, Goodfellow). The electrolyte for Cu electrodeposition consisted of 0.24 M CuSO₄·5H₂O and 1.8 M H₂SO₄. A high concentration of CuSO₄ was used to supply a sufficiently large number of ions inside the pores during the deposition, and sulfuric acid was added to increase the conductivity of the solution [63]. Meanwhile, the additives of polyethylene glycol (PEG) (300 ppm) and Cl (50 ppm) as NaCl were added in the electrolyte as stabilizers, according to the earlier work by Hasan et al. [64]. The wetting of the template was performed by immersing the template in the electrolyte for at least 30 min before deposition. For galvanostatic deposition, a constant current of 40 mA was applied between the cathode and anode using a CHI 660C instrument, and the potential-time (V-t) curves was generated to monitor the deposition process. The deposition was carried out at room temperature, and the magnetic stirring was applied at 100 rpm to improve the ion diffusion into the pores.

During the deposition, it was found that not all pores were filled up with nanowires simultaneously. A possible reason could be that not all pores in the template are aligned parallel to each other and a considerable angular distribution of $\sim 30^{\circ}$ to the surface normal was observed [65]. To achieve the complete filling of



Fig. 22.4 Optical images showing the stripping process of the Cu overgrown layer, (**a**) film with an overgrown Cu layer after electrodeposition, (**b**) separation of the Cu layer from the underneath film and (**c**) the resultant film with a residue-free surface

every pore in the template, a so-called overgrowth-stripping method was developed [66]. This method allows nanowires to grow in as many pores as possible by depositing for a longer time and thereby allowing a continuous Cu film to grow on the template surface. The next step was to mechanically strip this overgrown film from the template to leave a residue-free surface. Figure 22.4a–c show the stripping process for preparing a NW-ACF film, where (a) is the Cu-filled membrane with an overgrown layer, (b) is the half separated Cu layer from the underneath film and (c) is the stripped film with a residue-free surface. Due to the weak adhesion between the Cu and polymer layer, the overgrown layer can be readily separated from the membrane using a small peeling force. Finally, the Ag seed layer was etched in dilute $\rm NH_4OH:H_2O_2$ (1:1) solution for several seconds. The fabricated film was thoroughly rinsed in DI water and dried with a nitrogen gun.

22.4 Nanowire ACF: Fine-Pitch Interconnection

22.4.1 Daisy-Chain Test Chip Design and Fabrication

Two stacked test chips (test module) with daisy-chain, 4-point and insulation test structures were designed to electrically characterize the Z-axis interconnection resistance and X-Y direction insulation property of the fine-pitch interconnects formed by NW-ACF. Figure 22.5 shows the layout of the bottom and top chip design using CleWin software [67]. The 100 daisy-chain square bond pads are placed in the centre of both top and bottom chips with the same pad and pitch size. All the test chips have two 4-point structures and four insulating pads.

There are four variations of the daisy-chain test chips that have different bond pad size and pitch. All test modules have a bottom chip size of $5 \times 5 \times 0.5$ mm. For test module 1 and 2, with a larger pad/pitch size of 80/160 µm and 40/80 µm, it has a top die dimension of $2.5 \times 2.5 \times 0.5$ mm. While for test module 3 and 4, with a smaller



Fig. 22.5 Layout of daisy-chain test module containing 100 daisy-chain pads, two 4-point test structures and four insulating pads (die 1 is bottom die, and die 5 is corresponding top die) [68]



Fig. 22.6 Schematics showing (a) 4-point single interconnection resistance structure and (b) insulation test structure [6]

pad/pitch size of 20/40 and 10/30 $\mu m,$ it has a top chips dimension of $1.1 \times 1.1 \times 0.5$ mm.

Meanwhile, two 4-point structure and four unlinked pads are placed in the periphery of the daisy-chain pads to enable 4-point single interconnect measurement and insulation tests to be performed. The principle of the 4-point structure for single interconnect measurement is illustrated in Fig. 22.6a, where the voltage/current is applied between V_1/I_1 and V_2/I_2 and the voltage drop is measured between V_3 and V_4 . For the insulation test, the neighbouring NW-ACF interconnects with unlinked bond pads are shown in Fig. 22.6b, where the voltage/current is applied between V_1/I_1 and V_2/I_2 and the leakage current I_{leak} is measured between the two points.

The test wafer containing daisy chains and other test features was fabricated using a four-mask wafer fabrication process, as shown in Fig. 22.7. Details of the fabrication process can be found in [68].

The four-mask process includes:

- 1. Cu electroplating process with the first photoresist (PR) mask to form the base metal of pads and tracks
- 2. The In electroplating process with second PR mask to form the bond pad finish of In



Fig. 22.7 Schematic representation of the process flow of the test wafer [68]

- 3. Cu seed layer etching process with the third PR mask to remove the residue metal and insulate the structures
- 4. SiO_2 passivation process by sputtering a thin layer of SiO_2 on the whole wafer area and patterning the pad area with the fourth PR mask to open the pads by the dry etching process and to insulate the metal tracks

22.4.2 Thermocompression Bonding

The interconnections between the bottom and top chips were achieved by interposing the NW-ACF between two chips using thermocompression bonding. Due to the fine-pitch dimensions of the test chips, alignment is critical for achieving successful bonding. Otherwise, the open and shorting probability increases abruptly due to misalignment of ACF joints [69]. The other issue with ACF bonding is non-planarity, which can create an uncontacted bonding area due to an uneven distribution of the bonding force [70, 71]. Figure 22.8 shows the captured alignment images of the daisy-chain test module 1 (with the largest pad/pitch size of 80/160 μ m) and test module 4 (with the smallest pad/pitch size of 10/30 μ m) by the process camera in the bonding system. Even for the smallest pitch size, good alignment can be achieved with the bonding system before bonding. To ensure a good coplanarity between top and bottom dies, accurate calibration of the bonding tool is required. Since the die has a considerable surface topography due to the bonding



Fig. 22.8 The captured image of chip alignment during bonding, (**a**) the alignment with pad/pitch size of 80/160 μ m and (**b**) the alignment with the pad/pitch size of 10/30 μ m [72]



Fig. 22.9 SEM image of the bonding interface of the NW-ACF interconnect [68]

pads structure, the coplanarity within the bonding area is very critical and has an influence on the bonding yield.

Meanwhile, the bonding parameters, i.e. bonding temperature and force, were experimented with to understand their effects on the formed interconnects. Three bonding temperatures, 180, 200 and 220 °C, were evaluated with test module 1, and a bonding force ranging from 1.5 to 20 N was evaluated using all four test modules. The details of this study can be found in [68, 72] with optimized bonding conditions of 220 °C, 1.5–10 N (depending on pad size), 60 s for NW-ACF. Figure 22.9 shows the cross-sectional SEM image of the bonding interface of the nanowire ACF interconnect.

22.4.3 Electrical Measurement and Daisy-Chain Resistance

After flip-chip assembly, the interconnections formed by NW-ACF were subjected to full electrical characterization with 4-point Kelvin probing using a Cascade manual probe station and Agilent B1500A Semiconductor Device Analyzer. The 4-point measurement was set up by connecting four source/monitor units (SMUs) of the instrument, separately. SMU 1 and 2 were connected as voltage force, and SMU 3 and 4 were connected to sense the voltage drop. Figure 22.10 shows the schematic of the 4-point measurement for two connected daisy chains. It should be noted that with this probing structure, a small part of the track and the bond pad resistance (between SMU 3 and 4) is included in the measurement. For each measurement, the forcing voltage started from -100 to 100 mV with steps of 1 mV. The current flow from SMU 1 to SMU 2 and the voltage drop between SMU 3 and 4 were recorded to generate the I-V curve.

The measured I-V curves at the interconnect intervals of 2, 6, 8, 10, 30, 60, 96, 98, 100 daisy chains in a fully connected daisy-chain circuit are shown in Fig. 22.11. The resistances were obtained as the slope of the respective curves and increased



Fig. 22.10 Schematic showing the 4-point kelvin probing for daisy-chain resistance (two connected chains probed in this case). SMU 1 and 2 supply a voltage force and SMU 3 and 4 record the voltage drop. The resistances of the tracks and bond pads between SMU 3 and 4 are measured







with the number of interconnects increasing from 0.15 to 7.36 Ω . The resistances plotted as a function of the number of interconnects are shown in Fig. 22.12.

From the graph, it can be seen that the resistances linearly increase with the number of interconnections. The slope of the linearized line is defined as the average daisy-chain resistance per interconnection and is measured to be \sim 74 m Ω in this case.

22.4.4 Insulation Properties

For the NW-ACF, the polymer matrix acts as the insulation material between the nanowires to prevent lateral conduction. The conductivity of pure polycarbonate is about 10^{-13} S/m [73], and it has been used as the base insulation material to form CNT/polymer composites for electrical applications. On the other hand, the distribution of nanowires which is predetermined by the pore distribution in the polymer is the key factor to influence the insulation properties of the NW-ACF. Due to the random distribution of pores and the different angles of inclination of the pores, the merged pores seen in the template surface and the existence of overlapping pores inside the template account for some insulation issues between bond pads, after applying the NW-ACF material [66, 72, 74].

The insulation properties between the NW-ACF-formed interconnects were evaluated by probing any of the two neighbouring insulation pads on the bonded samples. The leakage current was measured at increased voltages from 0 to 20 V with a step size of 50 mV. The failure criterion is defined as a measured leakage current $I_{leak} > 10^{-9}$ A, which is an analogy to the failure criteria defined for the leakage characteristic of fine-pitch TSVs in a Si substrate [75]. Three pairs of the insulation pads were probed for each test module, and the voltage represents the worst-case scenario among the tested groups. It was found that for the large pitch sizes (160 and 80 µm), nearly all interconnects can maintain a small leakage current



Fig. 22.13 Typical I-V curves showing leakage current behaviours as a function of voltage, (a) insulation voltage of 20 V and (b) insulation voltage of 14 V

up to 20 V (except for the test module 2 at 5 N). For the smaller pitch size (40 and 30 μ m), there are more variations of insulation voltage from sample to sample, and one shorted interconnect was found with the test module 4 at 3 N. However, most of the insulated interconnects show a good insulation property with a small leakage current even at a small pitch size.

Figure 22.13 shows the I-V curves representing the typical leakage current behaviours of the measured NW-ACF interconnects at a pitch size of 30 µm. Figure 22.13a shows the I-V curve indicating the best-case insulation property, where the leakage current is well maintained below 10^{-11} A with an applied voltage up to 20 V. Comparatively, Fig. 22.13b shows the increase of the leakage current with the increasing voltage. This represents the typical insulation behaviour for the interconnections with an insulation voltage <20 V. In graph (b), for the applied voltage is >14 V, the leakage current below 10^{-9} A gradually increases up to 10^{-6} A. The decreased insulation voltage and the occasional insulation failures can be attributed to the random distribution of the pores in the membrane template and the existence of the overlapping pores in some small areas. If such areas are captured between two adjacent pads, the tiny conduction channels formed by the linked nanowires can be established in the X-Y direction and cause the increased leakage current and even shorts at an increased applied voltage. However, it should be noted that both the applied voltage (20 V) and the leakage current limit ($<10^{-9}$ A) have been set higher than the expected voltage (~3 V) and leakage current ($<10^{-6}$ A) requirements for most IC applications.

22.5 Comparison of Different 3D Interconnect Methods

Table 22.1 compares the different interconnection technologies for 3D stacking, including Cu/Sn µbump, Cu-Cu direct bonding, conventional ACF and NW-ACF. Among them, solder µbump and Cu-Cu direct bonding are the most prevailing

		JU MAUNING	_	
		Cu-Cu direct bonding		
	Solder µbump [76–78]	[79–81]	Particle-based ACF	NW-ACF
Applications	3D interconnect	3D interconnect	Chip-to-substrate, die-to-die	Die-to-die 3D integration
Companies/institutes	RTI International (2010), ITRI (2011)	Leti (2008), Uni. of Tokyo (2008), Zintronix (2009)	Hitachi (commercial ACF) (evaluated in this work)	Tyndall (evaluated in this work)
Interconnect methods	Cu-Ni/Au-SnAg, Cu-Sn	Cu-Cu (bumpless)	Adhesive-based, Ni/Au- coated particles	Adhesive-based, Cu-NW
Minimum pitch size (µm)	10	6	80	30
Minimum pad size (µm)	4	.0	40	10 (to date)
Process temperature	300 °C (N ₂ purging)	<200 °C or RT	190 °C	220 °C
Process time	180 s	30 s or post-annealing, 30 min	Lamination time + 5–30 s bonding time	60 s
Bonding force	5 MPa	64 MPa	20 N per die	1.5-10 N per die
Contact resistance (Ω)	0.07	0.08	0.09 (Cu-In pads, 80 µm size)	0.03 (Cu-In pads, 10 µm pad size)
Bond strength	20–30 MPa	>20 MPa	20 MPa	5-10 MPa ^a
Reliability issue	Intermetallic compound (IMC) growth	NA	Polymer degradation	Polymer delamination and degradation ^a
Specific requirements	UBM, wafer bumping, underfill	Surface treatment, CMP, vacuum environment	Lamination process	NA
Process complexity/cost	Medium	High	Low	Low

 Table 22.1
 Comparison of interconnection technologies for 3D stacking

^aValues/issues can be improved by using different polymer system

technologies which are used for 3D interconnection. The ultrafine-pitch solder μ bump interconnect with 4/10 μ m pad/pitch size has been reported by RTI International with a low contact resistance of 70 m Ω per bond [76]. However, the difficulties for this technology were reported by ITRI [77] to include the fine-pitch bumping process with bumping defects such as bridge bump, missing bumps and variations in bump height. The other challenge is the fine-gap underfill process to achieve a high dispensing yield without voids. The main reliability concern of the μ bump joints is crack propagation along the interface between solder and the formed intermetallic compounds (IMCs). Meanwhile, due to high bonding temperature (250–300 °C), thermo-mechanical stress caused by local thermal expansion coefficient (CTE) mismatch between the UBM, solder, IMC and underfill is another reliability issue of these μ bump interconnects which needs to be addressed [78].

As a low-temperature bonding method, Ziptronix have developed wafer-level direct bonding interconnect (DBI) by direct Cu-Cu and oxide bonding at room temperature using copper CMP process after the BEOL Cu damascene process, followed by 125 °C post-annealing [79]. Leti have developed a similar approach using direct hydrophilic Cu-Cu bonding at room temperature, atmospheric pressure and ambient air [80]. The main challenge presented by these processes is in the area of surface preparation, where a very flat surface with root mean square (RMS) roughness lower than 0.5 nm and particle-free hydrophilic surface have to be prepared before bonding. Researchers in the University of Tokyo have successfully applied a surface-activated bonding (SAB) method for Cu-Cu direct bonding at room temperature without any annealing steps [81]. A bumpless interconnect with 6 μ m pitch Cu electrodes has been realized at room temperature using the SAB method. However, the whole bonding process has to be carried out under an ultrahigh vacuum condition (<10⁻⁵ Pa), and this makes these processes very expensive for mass production.

Despite the ultrafine-pitch capability of the above technologies, these interconnect methods may still be limited by process complexity, yield and cost. On the other hand, ACF technologies can be recognized as a low-temperature, fine-pitch interconnection method used for chip-to-substrate and die-to-die applications. Compared to the particle-based ACF which is limited by the applicable pad size (\geq 40 µm), NW-ACF with nanowires orderly distributed in the polycarbonate matrix has shown its potential as an ultrafine-pitch interconnect (10/30 µm pad/pitch capability to date) with an even better electrical performance (30 m Ω per bond). Polycarbonate (PC) matrix is the most suitable commercially available template at present. With other polymeric templates becoming available, aspects such as interface adhesion and agglomeration of nanowires should be better controlled and consequently improve the reliability.

22.6 Conclusions

One of bottlenecks of 3D heterogeneous IC integration is the requirement for low-temperature, high-density interconnects to be formed between the stacked dice. Conventional bulk solder-based interconnects can no longer meet the cost and performance requirements with the ever-decreasing pitch size. On the other hand, ACF interconnects have been considered as a potential replacement to accommodate the reduced pad and pitch sizes. New developments of particle-dispersed ACAs such as nano-Ag or solder particles have led to new applications with finerpad/finer-pitch size. However, constraints such as particle agglomeration and lower volume fractions of particles make such ACAs not suitable for chip-to-chip applications with a low electrical resistance requirement (comparable to solder joint resistance). To avoid the particle agglomeration issue, vertical wire ACFs have been developed with orderly distributed conductors. A Z-axis ACF with vertical wire conductors have been successfully demonstrated for fine-pitch chip-/waferlevel interconnections. However, limitations of this technology are the photolithographic-based patterning process and the rigidity of the wire conductors with micro-size diameter. To obtain high aspect ratio nano-size wire conductors, the concept of nanowire ACF is proposed by fabricating nanowires in the ion tracketched membranes. The nanowires show promising results in terms of electrical, mechanical and thermal properties, which can be used as compliant conductors in an ACF. Future work needs to look into reliability and compare different polymer carriers and metallurgical versus compression interconnects for the NW-ACF.

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Chapter 23 Carbon Interconnects



Antonio Maffucci

23.1 Interconnect Challenges for Nanoelectronics

In the last four decades, the growth of the semiconductor industries has been characterized by a continuous process of dimensional scaling of silicon technology, in order to improve the performance of integrated circuits (ICs). In this period, the popular Moore's law [1] and the classical scaling rules (e.g., the pioneering work [2]) have been at the basis of the ITRS (International Technology Roadmap for Semiconductors, [3]) which has driven the industry targets.

Given the exponential increase in the number of transistors, a more and more crucial role has been played by the electrical interconnects, needed to manufacture high-performance microchips. A typical interconnect structure inside a silicon chip is depicted in Fig. 23.1: starting from the transistor level (local level), the signal is routed through the chip in horizontal (lines) and vertical (vias) interconnects, passing from the intermediate level and ending to the global level. Typical cross-section dimensions are reported in Table 23.1. The interconnect density is of the order of some km/cm².

The overall performance is strongly affected by the behavior of interconnects, which introduce power dissipation, delays, signal integrity issues, and reliability problems. All these effects worsen with dimensional scaling, and thus in the past, significant threats related to scaling were solved by replacing materials and redesigning architectures. For instance, copper (Cu) interconnects have replaced aluminum to reduce the electrical resistance and to mitigate electromigration [4]. Furthermore, the use of low-k dielectrics has lowered the capacitance [5], with the result of lowering the interconnect delay and the dynamic power dissipation. Great

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Table 23.1 Dimensions of the interconnect cross section for two technology nodes (ITRS, [3])

	22 nm node			11 nm node		
	Global	Intermediate	Local	Global	Intermediate	Local
Line width [nm]	200	70	35	100	35	17.4
Line height [nm]	400	140	65	200	70	32.5
Via diameter [nm]	200	70	35	100	35	17.4

investments in new materials and processes and in the increase in the number of layers have allowed the continuous scaling of interconnects to comply with new technology nodes, as, for instance, the 22 nm node [3]. However, when shrinking the dimensions to nanoscale, where the lateral dimension of a Cu interconnect becomes comparable or smaller than its electron mean free path, its electrical resistivity dramatically increases [6], due to surface and grain-boundary scattering mechanisms (see Fig. 23.2). Additional problems, like reduced electromigration lifetime and poor adhesion to interlayer dielectrics, along with the limits of the present dielectrics, suggest replacing the conventional Cu/low-k technology with novel solutions with innovative materials.

Besides the behavior of the materials at nanoscale, another challenge for nanointerconnects is given by the architecture or, more generally, by the design itself [7]. Interconnects are used for several purposes: they can carry signals or power, data or clock, analogue or digital, and so on. An optimal design is therefore strongly related to the final purpose of the interconnect, since there are deep differences in operating conditions and required performance. A proper design for signal interconnects, for instance, must be aware of all the signal integrity issues arising from phenomena like delay, mismatch, dispersion, crosstalk, etc. [8]. This usually dictates design strategy aimed at minimizing such phenomena, by lowering the corresponding circuit parameters (e.g., coupling capacitances, resistances, loop inductance, etc.). Speaking about power interconnects, such as those used in power delivery networks (PDNs), their reliability is strongly affected by the problem of electromigration. Therefore, in designing them, a crucial parameter to take under



Fig. 23.2 Copper resistivity versus wire width. (Reproduced from ITRS, [3])

control is the current density [9]. Indeed, the nanoscale interconnects may be required to carry on current densities of the order of MA/cm^2 , leading to a volumetric heat production of the order of 10^3-10^4 W/mm³ [3]. Furthermore, for PDNs it is essential to get the lowest value of resistance in order to minimize unwanted effects like the voltage drop.

As a consequence of the above considerations, the interconnect structure of an IC must be designed by optimizing contemporarily many performance indicators, which is a great challenge at the nanoscale, where the scaling laws may change. For instance, nanoscale effects like those associated with quantum capacitance or kinetic inductance may break the simple scaling rules used so far to mitigate the crosstalk noise between two interconnects that are based on a proper ratio between inter-wire distance and wire diameter (e.g., [10]). Finally, in the route to the nanoscale, the semiconductor industry is also investigating radical changes in interconnect technology, such as the use of optical links [11] or RF interconnects [12].

Given these premises, it is not surprising to realize that in the last decade, many companies promoted research on emerging interconnect technologies, such as those based on carbon. Indeed, due to their outstanding physical properties, carbon-based materials are promising candidates to replace copper for nano-interconnects [13–15]. To this end, extensive consideration has been so far devoted to the use of carbon nanotubes (CNTs), i.e., a 1D allotrope of graphene obtained by rolling up a graphene sheet [13]. They are denoted as "single-walled" (SWCNTs) if a single sheet is considered or as "multi-walled" (MWCNTs) if composed of several nested sheets. Alternatively, interconnects made by graphene nanoribbons (GNRs) have been also investigated. Both materials exhibit low electrical resistivity, high thermal conductivity, and high current-carrying capability, besides other excellent mechanical

properties [16, 17]. In fact, the electron mean free path is of the order of μ m in SWCNTs [18] and in GNR [19], of tens of μ m in MWCNTs [20], to be compared to the few tens of nm in Cu. The current density may reach values of 10⁹ A/cm² in CNTs [21], and of 10⁸ A/cm² in GNRs [22], whereas the maximum attainable value for Cu is about 10⁷ A/cm². As for mechanical properties, the CNTs may exhibit a Young's modulus of about 1 TPa [23], five times the value for stainless steel. The thermal conductivity of CNTs may reach values of about 3500 Wm⁻¹ K⁻¹ [24], whereas for Cu it is usually about 400 Wm⁻¹ K⁻¹.

Given such fabulous properties, carbon-based interconnects have been widely investigated for future VLSI applications: ballistic transport means reduced resistance, hence reduced delay for signal lines. The combination of mechanical strength and large current capability mitigates the electromigration issues, a highly desirable behavior for power interconnects. High thermal conductivity results in more efficient heat dissipation, which in turns allows using such interconnects in 3D architecture and/or in nanopackaging.

However, all these outstanding values may dramatically drop when real-world interconnects are fabricated, given the necessity of using bundles of CNTs or arrays of GNRs rather than isolated specimens. Controlling the quality of such bundles (e.g., in terms of density and alignment, terminal contacts, defects, and inclusions) is among the most limiting factors for the success of such a technology, along with compatibility between the CNT and the CMOS growth processes. Despite all the above limits, the recent first examples of successful integration between CNT and CMOS technologies (e.g., [25–30]) opened the possibility for carbon interconnects to move toward real practical applications. In [25], the solder bumps for flip-chip interconnects are made by CNT bundles (Fig. 23.3); in [26] high-frequency CMOS oscillators are realized by using interconnects; in [28], CNT bundles have been used to fabricate through-silicon vias; finally, in [29] an all-CNT computer with PMOS transistors is demonstrated.

In this chapter we review the state of the art of carbon-based interconnects, presenting the most relevant results in modeling, fabrication, and integration, coming to the most recent applications, where such interconnects were for the first time successfully integrated to CMOS technology.

23.2 Modeling Carbon Interconnects

23.2.1 A Generalized Ohm's Law for Nanoscale Conductors

In view of designing carbon-based nano-interconnects, accurate and efficient equivalent circuit models are needed. To this end, one of three distinct approaches to electron transport modeling can be used: classical, semiclassical, and quantum.

The *classical approach*, with the most limited validity area, is the simplest one. For example, the Drude model of conductivity in metals considers the conducting **Fig. 23.3** CNT pillar bumps for flip-chip technology: (**a**) die attached to the carrier substrate; (**b**) zoom to two CNT bumps. (Reproduced from Yap et al. [25])



Silicon CMOS integrated circuit



Carbon nanotube interconnect



Fig. 23.4 High-frequency CMOS oscillators with CNT interconnects. (Reprinted with permission from Close et al. [26]. Copyright (2008) American Chemical Society)

electron as a classical particle, which moves in the electric field while encountering inelastic collisions with a randomly vibrating ion lattice. Assuming a conducting wire with longitudinal axis *z*, the model easily leads to the classical *Ohm's law* that reads in frequency domain:

$$J_z(z,\omega) = \sigma_c(\omega) E_z(z,\omega), \qquad (23.1)$$

where J_z and E_z are the axial components of the current density and electric fields, respectively, whereas $\sigma_c(\omega)$ is e the Drude conductivity:

$$\sigma_c(\omega) = \frac{\sigma_0}{1 + i\omega/\nu},\tag{23.2}$$

 ν being the collision frequency and σ_0 the DC value of conductivity.

However, at the nanoscale the classical approach leads to low-accuracy models, since new phenomena join to classical electromagnetic interactions, such as discrete energy spectrum of charge carriers, existence of phonons, ballistic transport and tunneling, many-body correlations, interface effects, etc. [31]. The *quantum approach* based on a Maxwell-Schrödinger model is the most accurate, since it rigorously describes all quantum effects: tunneling, spin-orbit, dipole-dipole, and spin-spin interactions. This approach leads to highly cumbersome simulations that cannot be carried out in the standard circuit-based simulation tools usually adopted by IC designers.

However, the quantum approach is not always strictly necessary at the nanoscale. Taking into account the realistic operation conditions for nano-interconnects in next technology nodes [3], with operating frequencies below 1 THz and low-bias conditions (fractions of volts), a *semiclassical approach* can be used. With this approach, the particle ensemble can be modeled as a non-ideal gas or as a fluid, undergoing quantum effects, which are taken into account by replacing the real particle mass by the corresponding effective value. Indeed, in the above operating conditions, for transverse dimensions of the order of nanometers the following conditions hold:

- (i) The cross-section characteristic dimension is *electrically small*, i.e., it is much smaller than the characteristic wavelength of the signals propagating along the conductor.
- (ii) The transverse component of the electrical current may be neglected.
- (iii) Only intraband transitions are considered, while interband ones are not allowed [32].

In addition, given the low-bias conditions, the typical voltage value verifies $V < k_BT/e$, being k_B the Boltzmann constant, T the absolute temperature, and e the electron charge. For instance, CNT-based integrated circuits have been proven to work under a supply voltage as low as 0.4 V, much lower than for conventional silicon ICs, e.g. [33]. Consequently, a linear relation may be assumed between electric field and current, which may be written as the *generalized Ohm's law* in the wavenumber domain β [34, 35]:

Type/width	1 nm	10 nm	50 nm	100 nm
CNT	2.00	2.12	5.04	9.93
GNR	1.00	1.07	1.57	3.13
Cu NW	3.12	11.8	221	875

Table 23.2 Estimated number of conducting channels *M* at 300 K, for a copper NW, GNR, and CNT, for different widths (GNR) or diameters (NW and CNT), at 300 K [35]

$$[1 - \psi(\omega)\beta^2]\hat{J}_z(\beta,\omega) = \frac{\sigma_0}{1 + i\omega/\nu}\hat{E}_z(\beta,\omega), \qquad (23.3)$$

$$\Psi(\omega) = \frac{\xi(\omega)v_F^2}{\nu^2(1+i\omega/\nu)^2}, \ \ \sigma_0 = \frac{2\nu_F M}{\nu R_0 X},$$
(23.4)

where $R_0 = 12.9 \text{ k}\Omega$ is the so-called quantum resistance, *M* is the number of conducting channels, v_F is the Fermi velocity, ν is the collision frequency and the quantities *X*, and $\xi(\omega)$ depends on the material used as conductor. For a CNT, it is $X = \pi D$ and $\xi(\omega) = 1$, (being *D* its diameter), whereas for a GNR it is $X = \pi W$ (being *W* its width), with $\xi(\omega)$ expressed as in [35]. For a metallic nanowire (NW) of diameter *D*, it is $X = \pi (D/2)^2$ and $\xi(\omega)$ may be approximated as $\xi(\omega) \approx (1 + 1.8i\omega/\nu)/3(1 + i\omega/\nu)$ [34].

The left-hand side of (23.3) introduces a spatial-temporal dispersion, whereas the right-hand side introduces a frequency dispersion. This means that Ohm's law for nanoscale interconnects introduces nonlocal and long-lasting interactions. When the dispersion at the left-hand side is negligible, (23.3) is consistent with classical law (23.2), the only difference being in the values of the quantities related to quantum effects, such as the number of conducting channels M. This quantity is a measure of the number of subbands that effectively contribute to the electric conduction and plays a crucial role in the behavior of the carbon nanomaterials. Table 23.2 reports the value of M for carbon materials and copper nanowire at different transverse dimension: for carbon material the energy levels are quantized for transverse dimensions up to some hundreds of nm; hence M is always of the order of some units. For wires of conventional conducting materials like copper, there is no quantization of energy levels unless their diameters drop to the order of some tens of nm or lower [35].

23.2.2 Equivalent Circuit Models for a Single Nanointerconnect

The main advantage of semiclassical models for the electron transport is the possibility to model carbon interconnects in the common frame of the transmission line (TL) model. Alternatively, field equation models have been also explored, such as those cast in terms of integral equations to be solved numerically (e.g., [36]), but of



Fig. 23.5 A simple two-conductor nano-interconnect, with the signal conductor made by: (**a**) a carbon nanotube or a nanowire; (**b**) a graphene nanoribbon. (**c**) Equivalent transmission line model: inset is the unit cell

course such models are not so appealing to designers since they do not provide equivalent circuits.

The simplest configuration is depicted in Fig. 23.5, where the nano-interconnect is made by a signal conductor above a perfect conducting ground. The signal conductor can be either made by a CNT or a nanowire (NW), as in Fig. 23.5a, or by a GNR, as in Fig. 23.5b.

In the abovementioned operating conditions, at a given abscissa z, the distributions of surface currents and charges along the contour of a nanoscale conductor may be assumed to be uniform [36]. Thus, coupling Maxwell equations (with the charge conservation law) to the generalized Ohm's law (23.3), the following relations hold between the electrical current I(z) and the voltage U(z), defined in terms of electrochemical potential:

$$-\frac{\partial I(z)}{\partial z} = i\omega C_t U(z), \quad -\frac{\partial U(z)}{\partial z} = (R_t + i\omega L_t)I(z), \quad (23.5)$$

where the electrical parameters L_t , R_t , and C_t are the per-unit-length (pul) inductance, resistance, and capacitance, respectively, defined as:

$$L_t = L_m + L_k, \quad R_t = \nu L_k, \quad C_t^{-1} = C_e^{-1} + C_q^{-1} (1 + \nu/\omega)^{-1}.$$
(23.6)

Here, C_e and L_m are, respectively, the classical pul electrostatic capacitance and magnetic inductance for the guiding structure, whereas L_k and C_q are, respectively, the *kinetic inductance* and the *quantum capacitance*, given by:

$$L_k = \frac{R_0}{2v_F} \frac{1}{M}, C_Q = \frac{1}{v_F^2} \frac{1}{L_k}.$$
(23.7)

From the physical point of view, the kinetic inductance describes the effects of the mass inertia of the conduction electrons, while the quantum capacitance is related to the quantum pressure arising from the zero-point energy of such electrons. The collision frequency may be expressed as $v = 2v_F/l_{mfp}$, l_{mfp} being the electron mean free path.

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Equation (23.5) represents the classical TL model for a two-conductor line, written in terms of the variables (I, U); hence the pul parameters (23.6) represent the parameters of the unit RLC cell in Fig. 23.2c. Specifically, the inductance is the series combination of the classical magnetic one and the kinetic one, and the capacitance is the series combination of the classical electrostatic one and a quantum one (independent of frequency, if $\nu/\omega < 1$). This circuit model was first derived for quantum wires in the pioneering work [37] and for CNTs in the early works of Burke, [38], in the frame of the Luttinger liquid theory. In the latter case, L_k and C_a were obtained for metallic single-walled CNTs, that is, in the case obtained by assuming M = 2 in (23.7). In [39], the same TL model applicable both to CNTs and conventional metallic nanowires was derived from a semiclassical transport theory based on the Boltzmann equation. The Boltzmann transport theory was also used to obtain the circuit models for SWCNTs in [40] and MWCNTs in [41]: such an approach was proven to be equivalent to a hydrodynamic model, the so-called fluid model, where the carriers are modeled as an electron cloud, [42, 43]. Finally, firstprinciples calculations and fitting with experimental results instead form the basis of the circuit models presented in [44] for CNTs and in [45–47] for GNRs.

Another possible TL model is obtained by recasting (23.5) in terms of the voltage V(z) defined from the electrical potential, instead of the electrochemical one:

$$-\frac{\partial I(z)}{\partial z} = i\omega C_t V(z), \quad -\frac{\partial V(z)}{\partial z} = (R_t + i\omega L_t)I(z), \quad (23.8)$$

In this case, the pul parameters (23.6) would change into [40-43]:

$$L_{t} = (L_{m} + L_{k})/a_{C} \quad R_{t} = \nu L_{k}/a_{C}, \quad C_{t} = C_{e}, \quad a_{C} = 1 + \frac{C_{e}}{C_{q}(1 + \nu/\omega)}.$$
(23.9)

However, this is usually only a theoretical difference, since in practical applications, the quantum capacitance C_q is at least one order of magnitude larger than the electrostatic one C_e , and typical values for the collision frequency ν are $10^{11} \rightarrow 10^{12}$: this means that for frequencies up to 1 THz, $a_C \approx 1$.

According to (23.7) and (23.9), the pul resistance R_t , also known as the *intrinsic* resistance, may be expressed as:

$$R_t = \frac{R_0}{M} \frac{1}{l_{mfp}}.$$
 (23.10)

A great potential advantage of using carbon interconnects is their huge mean free path compared to conventional conductors, of the order of some tens of μ m, as recalled in Sect. 23.1. This means that *ballistic transport* (which means $R_t \approx 0$) is achievable for lengths comparable to those of local lines or vertical vias in on-chip interconnects.

The TL model for nanoscale interconnects (23.5), (23.6) is consistent with the classical TL model for a macroscopic line: indeed, for wire widths greater or equal to 100 nm, in conventional conductors like copper, the number of channels M becomes huge (as shown in Table 23.2), hence $L_k < < L_M$, $C_e < < C_q$, and so expressions (23.6) provide the classical TL pul parameters: $L = L_m$, $C = C_e$, and $R = 1/(\sigma_0 S_w)$, being S_w the wire section area.

To complete the circuit model in Fig. 23.5c, we should add two lumped resistances R_c at the terminations. Indeed, at the terminal contact surfaces between carbon and conventional metals, there is a barrier due to the mismatching between the band structures of the different materials [27]. This effect may be taken into account through a lumped resistor R_c :

$$R_c = \frac{R_0}{M} + R_p, \qquad (23.11)$$

where $R_0 = 12.9 \text{ k}\Omega$ and R_p is a parasitic term due to the quality of the contacts. Therefore, even in the ballistic transport regime ($R_t = 0$) and assuming ideal contacts ($R_p = 0$), the minimum value of the electrical resistance for a carbon line would be R_0/M , which means 12.9 k Ω or 6.45 k Ω for a single metallic GNR or SWCNT, respectively. The huge contact resistance arising from the metal/carbon interfaces still remains a primary issue for the practical use of carbon interconnects, and thus many efforts are devoted to contact engineering, to lower such a value [48].

Another important difference between macroscopic and nanoscale interconnects is the phase velocity: in macroscopic TLs the working mode is the *transverse electromagnetic* (TEM) wave, with phase velocity $c = 1/\sqrt{L_tC_t}$. The working mode in nano-TLs is a *surface wave* with rather large longitudinal component and phase velocity given by the Fermi velocity $v_F = 1/\sqrt{L_kC_q}$. To get an insight into this effect, let us refer to the interconnect in Fig. 23.5, assuming typical values for on-chip local level interconnect at the 14 nm node [3]: D = W = 14 nm, t = 2D and a relative permittivity of the embedding medium $\varepsilon_r = 2.2$.

Figure 23.6a shows the frequency behavior of the normalized phase velocity $c(\omega) = k_0/\beta(\omega)$, k_0 being the vacuum space wavenumber. The dispersion introduced by the generalized Ohm's law (23.3) leads to saturation in different frequency ranges. In all cases, the carbon line velocity saturates to a value that is two orders of magnitude smaller than the vacuum space velocity. This slowing effect is a well-known consequence of the role played by the kinetic inductance [33, 47]. The copper realization is not evidently affected by the quantum effects, and so its phase velocity exhibits a behavior similar to bulk copper, with saturation close to the ideal velocity. In a copper nanowire, the propagating velocity would be slowed down only for widths of the order of nanometers or fractions of nanometers, when the transverse quantization starts playing a role in reducing the conducting channels, as shown in Table 23.2. Figure 23.6b shows the dispersion for the attenuation constant $\alpha(\omega)$, therefore providing information about the frequency dependence of the losses. The attenuation introduced by CNTs is lower than those introduced by the other two



Fig. 23.6 Dispersion effect for an on-chip interconnect with width equal to 14 nm: (a) normalized phase velocity; (b) attenuation constant



Fig. 23.7 Carbon on-chip interconnects: (a) vertical vias realized with CNT bundles; (b) horizontal traces realized with CNT bundles or GNR stacks

realizations and is almost constant over the considered frequency range. As expected, the attenuation introduced by the copper NW is increasing, with frequency increasing, and is generally lower than that introduced by GNRs.

23.2.3 Equivalent Single Conductor (ESC) Model for Bundles

Isolated CNTs, GNRs, or NWs have been successfully used as electrodes in nanotransistors (e.g., [49, 50]), but are not suitable for fabricating nano-interconnects, given the huge value of the resistance introduced, and also for the presence of the contact resistance. Therefore, realistic carbon interconnects are fabricated by putting in parallel a consistent number of CNTs or GNRs, to lower such a resistance. Typical geometries for CNT interconnects are sketched in Fig. 23.7, where vertical (vias) or horizontal (lines) interconnects are supposed to be realized by bundles of

SWCNTs, MWCNTs, or mixed CNTs. Horizontal lines can be also realized by means of multilayered graphene nanoribbons (MLGNRs).

The rigorous way to model a bundle of *N* CNTs or a stack of *N* GNRs is the generalization of (23.5) or (23.8) to the case of a multiconductor transmission line (MTL). Such equations would relate the vectors of voltages and currents through per-unit-length matrix parameters, given by (formulation 23.5):

$$\mathbf{L}_{t} = \mathbf{L}_{m} + \mathbf{L}_{k}, \quad \mathbf{R}_{t} = \nu \mathbf{L}_{k}, \quad \mathbf{C}_{t}^{-1} = \mathbf{C}_{e}^{-1} + \mathbf{C}_{q}^{-1} (1 + \nu/\omega)^{-1}.$$
(23.12)

or (formulation 23.8):

$$\mathbf{L}_{t} = (\mathbf{L}_{m} + \mathbf{L}_{k})\boldsymbol{\alpha}_{c}^{-1}, \quad \mathbf{R}_{t} = \boldsymbol{\nu}\mathbf{L}_{k}\boldsymbol{\alpha}_{c}^{-1}, \quad \mathbf{C}_{t} = \mathbf{C}_{e}, \quad \boldsymbol{\alpha}_{c}^{-1} = \mathbf{I} + \mathbf{C}_{e}\mathbf{C}_{q}^{-1}(1 + \boldsymbol{\nu}/\boldsymbol{\omega})^{-1}$$
(23.13)

In (23.12), (23.13), **I** is the identity matrix, and \mathbf{L}_k , $\boldsymbol{\nu}$, and \mathbf{C}_q are diagonal matrices given by:

$$\nu = diag(\nu_n), \quad L_k = diag(L_{kn}), \quad C_q = diag(C_{qn}), \quad n = 1..N.$$
 (23.14)

The distributed terms (23.12) or (23.13) must be augmented with the terminal contact resistances for each conductor, as in Fig. 23.5c.

The above model includes the electromagnetic interactions between CNTs and GNRs, described by the off-diagonal terms of the magnetic inductance and electrostatic capacitance matrices, but neglect the inter-bundle quantum interactions.

Indeed, moving from isolated to bundles or arrays of carbon interconnects, additional effects into the electrodynamic models should be taken into account, which leads to the deformation of the energy bands for a CNT (a GNR) in a bundle (array). This deformation can, in principle, change the quantum parameters v_n , L_{kn} , and C_{qn} of the *n*-th CNT (GNR), with respect to the case where it is isolated. The main physical phenomenon is the tunneling between adjacent CNT shells or adjacent GNR layers, which gives rise to a transverse electron current and strongly affects the longitudinal electron transport [51, 52]. In particular, this effect would reduce the mean free path, with respect to the values observed for isolated CNTs or GNRs. The tunneling has a great influence on the propagation characteristics when considering antisymmetric current distributions between the shells and the ribbons [51, 52] or when investigating the THz range, where it generates additional resonances or antiresonances [53]. However, for frequencies up to 1 THz, assuming all the CNTs or GNRs are fed in parallel, we can disregard this tunneling effect [53]; hence in (23.14) we can use the quantum parameters evaluated for isolated CNTs or GNRs.

Since the CNTs or GNRs are fed in parallel, an *equivalent single conductor (ESC)* model may be derived (e.g., [54, 55]), recasting the above MTL model into a single TL one, relating the voltage $V_b(z) = V_n(z)$, n = 1. N, to the total current $I_b(z) = \sum_{n=1}^{N} I_n(z)$.

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An approximated *ESC* model may be used in cases when the kinetic inductance (quantum capacitance) matrix dominates over the magnetic inductance (electrical capacitance), and the operating frequencies are such that $\alpha_c^{-1} \approx I$. In such a case, it is:

$$L_{esc} = \left(\sum_{n=1}^{N} L_{kn}^{-1}\right)^{-1}, \ R_{esc} = \left(\sum_{n=1}^{N} \nu_n L_{kn}^{-1}\right)^{-1}, \ C_{esc} = C_{eb},$$
(23.15)

where v_n , and L_{kn} are the quantum parameters for the *n*-th isolated CNT (GNR). For carbon interconnects of practical use, densely packed bundles (arrays) are to be considered; hence the equivalent capacitance C_{eb} can be approximated by the classical electrostatic capacitance obtained for the given bundle (array), assuming the signal trace to be a bulk conductor [56]. Furthermore, the effects of the quantum capacitances are completely hidden by the electrical capacitance.

For instance, for a bundle of SWCNTs with diameter *D*, at a distance *t* from the ground (see Fig. 23.5a), the *ESC* model (23.15) reduces to:

$$L_{esc} = \frac{1}{N} \frac{3R_0}{4v_F}, \quad R_{esc} = \nu L_{esc}, \quad C_{esc} = 2\pi\varepsilon / \ln\left(\frac{2t}{D}\right).$$
(23.16)

In (23.16) only one-third of CNTs in the bundle are assumed to be metallic, which is a realistic statistical distribution.

23.2.4 Electrothermal Models for Carbon Interconnects

Designing reliable interconnects requires a self-consistent electrothermal co-simulation in order to correctly estimate the effects of temperature change on signal and power integrity [57]. Indeed, the power dissipation induces elevated temperatures, which directly impact on the interconnect RLC parameters, since the material properties such as electrical resistivity are temperature dependent. Such effects become more critical with advanced technologies, like the technology nodes beyond 14 nm, or for three-dimensional (3D) integration technology, since they require increased power density while exhibiting greater thermal resistances. The situation is particularly critical for power interconnects, characterized by high-density unidirectional currents, which introduce electromigration and limit the current-carrying capacity of switching circuits to the overall detriment of the interconnect reliability. As pointed out in Sect. 23.1, the use of CNTs could be also desirable to alleviate electromigration issues and improve their resiliency.

An accurate electrothermal model is obtained by coupling the electrical model to the thermal model describing the heat diffusion. In the general case, the thermal model is described by a second-order parabolic partial differential equation where the unknown is a nonuniform temperature profile and the source term is a nonlinear combination of electrical variables. Indeed, the source term is mainly given by the power dissipation due to the switching activity of the devices embedded in the substrate, with an additional contribution given by the Joule heating in the interconnects. The problems are then coupled via the temperature-dependent electrical resistivity of the conductors. The solution of the electrothermal problem in the general case requires a full 3D numerical simulation of the thermal problem (via FD, FEM, or BEM methods, for instance), coupled to a circuit simulation of the electrical network, usually in a relaxation approach (e.g., [57]).

A simple electrothermal model can be obtained by assuming 1D heat flux, i.e., the heat is mainly propagating along the interconnects and the heat exchange at the boundary between conductors and insulating dielectrics is negligible. A typical arrangement is depicted in Fig. 23.5, which shows the section and lateral views of an on-chip interconnect between two metal layers, with both horizontal and vertical interconnects.

Assuming steady-state conditions, the spatial distribution of temperature along an interconnect is governed by the heat equation:

$$\frac{d^2T(z)}{dz^2} - \frac{T(z)}{L_H^2} = -\frac{q(z)}{k},$$
(23.17)

where q(z) is the production term, k is the thermal conductivity of the conductor, and L_H is the thermal heating length.

The thermal conductivity for a carbon nano-interconnect usually has two components, associated with electrons and phonons, respectively, $k^{-1} = k_{el}^{-1} + k_{ph}^{-1}$. These two terms depend in different ways on temperature and size: in the simple case of isolated metallic SWCNT of length *l*, the following approximation holds [58]:

$$k(l,T) = \left(3.7 \cdot 10^{-7}T + 9.7 \cdot 10^{-10}T^2 + 9.3(1 + 0.5/l)T^{-2}\right)^{-1}, \ (l \text{ is in } \mu\text{m}).$$
(23.18)

In a more general case, the thermal conductivity of CNTs spans a very wide range of values from some tens to thousands of W/mK, as shown in Fig. 23.8, which shows the measured value of k for single and bundled MWCNTs [59].

Just like the electrical contact resistance (23.11), an important role can be played by the interface thermal resistance between CNT and metal electrodes (the so-called Kapitza resistance). Using an effective medium approach, an equivalent thermal resistance can be introduced, to include the effect of such an additional contribution. However, this contact thermal resistance may be neglected if the quality of the interface is improved, for instance, by introducing strong chemical bonds, as shown in [60].

The coupling with the electrical problem is given in (23.17) by the production term q(z), which in turn is related to the power dissipated for device activity ($\approx I_0 V_{dd}$, if I_0 is the device current and V_{dd} the bias) and to volumetric heat generated by Joule effect, $q = J^2 \rho$, being J the current density and ρ the electrical resistivity. The operating current and bias voltage of the devices can be considered independent of



temperature; hence the only temperature-dependent parameter is ρ and consequently the resistance. According to (23.10), (23.11), the resistance depends on the number of conducting channels *M* and on the mean free path l_{mfp} : both parameters depend on temperature. The mean free path in CNTs is related to acoustic phonon scattering and optical scattering, $l_{mfp}^{-1} = l_{mfp,ac}^{-1} + l_{mfp,opt}^{-1}$. [58]. The term $l_{mfp,ac}$ is proportional to 1/*T*, and $l_{mfp,opt}$ is a decreasing function as *T* increases, too. In addition, l_{mfp} is proportional to the CNT diameter *D* [47]. In the temperature range [300–600 K], the following approximation formula may be used [56] that fits the data provided in [58] and the simulations given in [44]:

$$l_{mfp} = D[k_1 + k_2T + k_3T^2]^{-1}, \qquad (23.19)$$

where $k_1 = 3.01 \cdot 10^{-3}$, $k_2 = -2.12 \cdot 10^{-5} \text{ K}^{-1}$, and $k_3 = 4.70 \cdot 10^{-8} \text{ K}^{-2}$.

For GNRs, the scattering comes from defects and acoustic and edge phonons [45]; hence the mean free path may be expressed as $l_{mfp}^{-1} = l_{mfp,D}^{-1} + l_{mfp,AC}^{-1}$. The mfp related to defects $l_{mfp,D}$ is quite insensitive to the GNR size and temperature, and its value ranges from 0.4 to 1 µm, where the minimum is attained when strong interlayer hopping mechanism is considered. The mfp related to acoustic phonons may be expressed as [56]:

$$l_{mfp,AC} = \gamma W/T, \qquad (23.20)$$

with the coefficient $\gamma \approx 9.92 \cdot 10^4$ K. Finally, a contribution due to the edges should be taken into account, which strongly depends on the edge diffusivity and the Fermi level. This contribution can be neglected, assuming the edges to be fully specular [45]. This leads to an underestimation of the total mfp and hence of the GNR performance.

As for the number of conducting channels M, it depends on the CNT or GNR size, chirality, and temperature. In particular, M is increasing with T, according to the approximate linear piecewise formula [44, 45, 56, 61]:

	Metallic SWCNT	Semicond. SWCNT	Metallic GNR	Semicond. GNR
M_0	2	0	1	0
$a_1 [\mathrm{nm}^{-1}\mathrm{K}^{-1}]$	$1.04 \cdot 10^{-4}$	$1.04 \cdot 10^{-4}$	$1.04 \cdot 10^{-4}$	$1.04 \cdot 10^{-4}$
<i>a</i> ₂	0.15	-0.20	0.02	0.02
$x_0 [\text{nm} \cdot \text{K}]$	5600	600	9000	3000

Table 23.3 Fitting coefficients for the number of conducting channels M in (23.17)

$$M(X;T) \cong \begin{cases} M_0 & \text{for } X < x_0/T \\ a_1 XT + a_2 & \text{for } X \ge x_0/T \end{cases}.$$
 (23.21)

where X is the GNR width W or the CNT circumference πD , and the fitting coefficients are given in Table 23.3. Therefore, the increase of M can counteract the decrease of l_{mfp} , leading to cases where a negative derivative of the electrical resistance with respect to T is found. Experimental evidences of this extremely favorable behavior are reported in [62] for GNRs and in [63] for MWCNTs. Further details on this behavior are discussed in paragraph 4.3.

23.3 Challenges for Fabrication and Integration of Carbon Interconnects

The effective use of carbon interconnects in future VLSI technology will be enabled only by an efficient and compatible fabrication process, able to match the following main requirements:

- (i) It has to be cheap, reliable, and easily scalable, in view of its industrialization.
- (ii) The resulting intrinsic and contact resistances of the carbon interconnects must be kept to enough low values.
- (iii) The growth temperature must be compatible with the CMOS integration in the back end of line (BEOL).

As for point (i), the best solution would be given by a monolithic CMOS-carbon interconnect integration process. However, the state of the art is still far from this achievement, due to major problems mainly related to material limitations and temperature issues. Therefore, the existing examples of circuits where CMOS were integrated with carbon interconnects have been realized by using transfer techniques: the CNT or GNR interconnects are grown at high temperature on a suitable substrate, and then they are transferred to the final substrate, with a nanoscale manipulation controlled by atomic force and/or scanning electron microscopes [64]. Several methods have been proposed to optimize the transfer techniques, such as dielectrophoresis, used to integrate CNT [26] and GNR [27] interconnects with CMOS in ICs operating up to GHz frequencies; see Fig. 23.4. Although optimized, the transfer technique ends up being too complicated and is hence characterized by too high costs and too low yields that make it unsuitable for mass production.
Requirement (ii) is strictly related to the achievable density of the CNT bundles or GNR stacks. As pointed out in Sect. 23.2, the main limiting factor for carbon interconnects is their resistance, both intrinsic (23.10) and contact (23.11). When dealing with short interconnects like vias, their typical length may be shorter than the mean free path; thus the performance is dictated by the contact resistance. On the contrary, the lengths of the horizontal traces are typically much longer than the mean free path, so for reasonable quality carbon/metal interfaces, the contact resistance can be neglected. In any case, the only way to reduce the resistance is to improve the quality of carbon/metal contacts and to increase the density of CNTs in bundles or GNRs in arrays, and this possibility is strictly related to the fabrication technology. According to the ITRS [3], the metallic SWCNT density required to be competitive with copper in terms of resistivity must be larger than 10^{13} cm⁻². Assuming all aligned and ideally close-packed SWCNTs, the maximum achievable density is about $2 \cdot 10^{14}$ cm⁻², obtained with SWCNTs with 0.4 nm diameter [65]. However, in a random distribution of SWCNTs, only 1/3 are metallic. In addition, in real bundles it is extremely hard to match the above ideal conditions. The metallic fraction may be increased by using MWCNTs, since in that case the semiconducting shells can also contribute to the electric conduction. However, to this end the inner shells must be opened to contact with electrodes [66].

As for point (iii), the compatibility with standard CMOS technology requires a process temperature that must be lower than 400 °C. Unfortunately, as shown later, the fabrication techniques suitable for a mass production of CNTs or GNRs are characterized by higher temperatures, and the possibility of lowering them has a major drawback in the increase of defects and so in the decrease of the quality of the carbon interconnect.

Summarizing, contact quality, bundle density, process temperature, and alignment [67, 68] are the main aspects to be taken into account to obtain an effective fabrication process for carbon interconnects.

23.3.1 Fabrication of Carbon Nanotube Interconnects

The fabrication of CNTs can be effectively done by means of three main techniques: *arc discharge, laser vaporization*, and *chemical vapor deposition*. The arc discharge method, based on the evaporation of graphite electrodes in electric arcs (used by lijima to synthesize the first CNT [69]), provides high crystalline quality but requires too high temperature (about 4000 °C) and introduces a high level of impurity [70]. On the other hand, the laser vaporization method, based on the laser-assisted evaporation of high-purity graphite, provides high level of purity, but it is limited by a modest yield, not suitable for mass production [71]. As for now, the most promising technique is chemical vapor deposition (CVD) or its derivatives such as *plasma-enhanced CVD* (PECVD) and *hot-filament CVD* (HFCVD). The advantages of such techniques reside in a selective growth of aligned CNTs and in their scalability [72, 73] that is essential in view of mass production.



Fig. 23.9 Mechanism for CNT growth with chemical vapor deposition. (Reproduced from Kumar [74])

In order to grow a CNT interconnect on a silicon or other substrates by CVD, a catalyst metal, such as iron (Fe) or cobalt (Co) is needed (the diameters of CNTs will almost correspond to the size of the metal catalyst islands). The growth mechanism is schematically reported in Fig. 23.9 [74]: the substrate is heated, and a carbon source gas is supplied, for instance, methane (CH₄), ethylene (C₂H₄), or acetylene (C₂H₂). The gas molecules decompose at the metal surface, then the carbon slops down through the metal, and the CNTs grow up across the metal bottom, pushing up the metal particle. Until the metal top is in contact with the gas and the excess carbon does not fully cover it, such a mechanism continues to grow the CNT longer and longer.

The quality of a bundle of single-walled or multi-walled carbon nanotubes is mainly related to the density, the absence of defects, the alignment, and the percentage of metallic tubes, all of which strongly influence the number of conducting channels, as pointed out in Sect. 23.2. By using the CVD method, the CNT density is strongly related to the size of the catalytic particles, which is in the order of nanometers. The density may be improved by reducing the catalyst nanoparticle size, which in turns leads to a reduction of the CNT diameter. The factors that limit such a reduction are given by the unwanted particle aggregation and by the interaction between the particle and the substrate. To this end, insulating substrates outperform metallic ones. The simultaneous control of the particle size and the substrate surface is difficult, and thus the maximum density achieved with standard CVD techniques is about 10^{12} cm⁻², one order of magnitude less than the targeted value [71]. However, the desired values of density may be obtained by means of costly improvement techniques, such as the use of cyclic deposition and annealing of the catalyst (achieving densities of about 10^{13} cm⁻² [75], see Fig. 23.10), the use of refractory conductive films to limit the catalyst diffusion into the support (achieving densities of about $5 \cdot 10^{12}$ cm⁻² [76]), or the use of nucleation and growth by sputtering (achieving densities of about $1.2 \cdot 10^{13} \text{ cm}^{-2}$ [77]).

As previously pointed out, a major issue for CNT/CMOS integration is the compatibility of the CNT growth temperature with typical VLSI technology temperatures. Indeed, growth occurs at temperatures between 550 and 1000 °C using

Fig. 23.10 A high-density CNT forest grown on a metallic support. (Reprinted with permission from Esconjauregui et al. [75]. Copyright (2010) American Chemical Society)



classical CVD techniques, whereas CMOS compatibility requires a maximum temperature of 400 °C. An efficient technique to lower the temperature is remote plasma CVD, where the plasma is generated far away from the substrate: in [78], MWCNT vias have been fabricated at 390 °C, whereas in [79] the synthesis of CNT bundles at 400 °C has been reported. An alternative technique is thermal CVD, based on the lower activation energy of catalysts: by means of such a technique, temperatures as low as 350 °C have been achieved in [80]. The main limiting factor in lowering the temperature with the above methods is the increase of undesired defects of the CNT structure, due to the poor diffusion of the carbon atoms placed close to the edges. Indeed, by means of PECVD, it is possible to lower the temperature to 120 °C, as demonstrated in [81], but with very low-quality CNTs.

Another important feature to control in view of fabricating good quality CNT bundles is the alignment of the tubes, which strongly impacts the electrical and thermal properties of the interconnect. Indeed, all the abovementioned techniques for mass production of CNTs lead to randomly oriented tubes in the bundles, and thus their alignment must be externally imposed. Two main approaches may be followed: the alignment can be imposed during the growth or post-growth, respectively. CNT alignment during the synthesis is obtained by placing nanoparticles of a metal catalyst on the substrate, exploiting the attitude of CNTs of growing on such particles in the normal direction with respect to the substrate. Unwanted bending may be avoided by increasing the density of catalysts, whose activity may be efficiently enhanced by the presence of water [82]. The process may be further enhanced by applying an external electrical field during the growth [83, 84]. Although this approach is easy to implement, its limit resides in the presence of metal catalyst particles in the final CNT bundle. Several post-growth techniques have been proposed, which are in general more cumbersome, but result in cleaner and welldispersed CNTs [85]. Such techniques start with isolating the CNTs through dispersion and centrifugation with a dispersant (e.g., a polymer or surfactant). The alignment is then realized by means of the action of external forces, related to electrical and magnetic fields. In view of industrial production, techniques like those based on gas flow are found to be suitable, given their scalability [86].



Fig. 23.11 Two different types of metal/CNT contact: (a) end contact; (b) side contact

The last issue to be considered is the role of the contact resistance that appears at any CNT/metal interface, since its huge value (in the order of $k\Omega$ per single tube) is one of the major limiting factors in the use of the nano-carbon interconnects. This is especially true for local interconnects, since in this case the main contribution to the overall resistance comes from the lumped term (23.11), rather than from the intrinsic distributed one (23.10). As pointed out in (23.11), the contact resistance is given by a quantum term that represents a bulk value and another term that depends on the quality of the contacts. The main problem is related to the small contact area between CNTs and metal electrodes that makes the electrical coupling between them difficult. Understanding the coupling mechanisms at the interface, both physical and chemical, is essential to effectively reduce the contact resistance. The most popular contact geometries are the so-called side contact and end contact; see Fig. 23.11. The side contact may be realized by drop-casting on electrodes the CNTs suspended in alcohol. The end contact is usually realized by bonding the metal surface atoms effectively to unsaturated C-bonds at the edge of the CNT shell. The two contacts lead to contact resistance values in the range of $k\Omega$ per single tube. To further reduce such values, several techniques are proposed, such as the use of Joule heating to induce annealing at the interface or the improvement of the wetting and of the formation of chemical bonding, for instance, by interposing a graphitic interfacial layer between CNTs and metal, as shown in [87] for a side-contacted CNT-based field-effect transistor. A comprehensive review of the results so far obtained for side and end contacts may be found in [48]. However, while the methods mentioned above are effective for isolated CNTs, they are not so effective for bundles since they are not suitable for scaling up. To improve the contact with CNT bundles, chemicalmechanical planarization is proposed, with a proper selection of the electrode material [88], or the use of an end-bonded geometry with a metallization process, as shown in [89]. A further improvement has been obtained by moving to the so-called "all-around" geometry, where the contacts occur both at the tip and at the side of the bundle [90]. Despite all these improvements, the contact resistance is still so high that the electrical resistivity of CNT bundle interconnects obtained so far falls, in the best cases, in the range 10^{-2} – 10^{-3} Ω cm, about three orders of magnitude higher than for nanoscale copper.

23.3.2 Fabrication of Graphene Interconnects

The most popular solution for graphene interconnects is the use of single or stacked graphene nanoribbons that can be fabricated with several techniques, either based on lithographic or catalytic cutting, on epitaxial methods, or on chemical assembly [91]. Indeed, GNRs have been fabricated, for instance, by means of direct CVD on metal substrates [92], of epitaxial growth on silicon carbide wafers [93], of top-down plasma etching, Fig. 23.12 [94], of exfoliation techniques [95], of on-surface polymerization with suitable molecular precursor, Fig. 23.13 [96], or by unzipping CNTs via oxidation [97].

The main challenge in fabricating GNRs is the requirement for high-quality graphene at the wafer-scale and for suitable substrates for patterning interconnect widths usually in the order of few nanometers. The choice of fabrication method and of the supporting substrate strongly influences the final performance of the interconnect: for instance, the conductivity of a GNR on a substrate may decrease orders of magnitude with respect to that of the same GNR suspended, because of the trapping effect of the substrate on the electrical charges. Indeed, mean-free-path values of about 1 μ m have been reported for suspended GNRs, whereas when they lie on SiO₂ substrate, such a value reduces to few tens of nm, comparable to that of the copper; see Fig. 23.14 [98]. Another major issue is given by the edge effects: rough edges and dangling bonds dramatically reduce the electrical properties of GNRs, because of the modification of the band structure. For this reason, if the GNR



Fig. 23.12 Fabrication of graphene nanoribbons via top-down etching

Fig. 23.13 STM image of graphene nanoribbons of different lengths obtained with a fabrication technique based on-surface polymerization. (Reproduced from Kimouche et al. [96])





Fig. 23.14 Electron mean-free-path values of GNRs versus their widths, for suspended ("bulk") GNRs (1.2 μ m line) and for GNRs on substrates. (Reprinted with permission from Rakheja et al. [98]. Copyright (2013) IEEE)

is too narrow (below 60 nm), it always behaves as a semiconductor, with a bandgap inversely proportional to its width and with strongly reduced mobility [98]. The edge scattering is therefore one of the most limiting factors for scaling down the minimum size of GNR interconnects. Finally, the fabrication method is also responsible for the final amount of defects and impurities, which is another fundamental aspect to be controlled, since it introduces additional degradation mechanisms such as Coulomb scattering.

Although many of the fabrication methods cited provide high-quality graphene on silicon substrates, such as the mechanical exfoliation, unfortunately they are unsuitable for mass production and incompatible with CMOS technology requirements. For instance, the silicon sublimation method is a promising technique able to control few layer graphene, but the requested annealing temperature is too high for CMOS compatibility. Therefore, as far as now, the most promising technique is again based on chemical vapor deposition (CVD process, as in the case of CNT interconnects (see Sect. 23.3.1)). The GNRs are grown via CVD at ambient pressure on a substrate such as nickel or copper. After the CVD growth, the graphene ribbons are transferred to the final substrate chosen for the envisaged application, via an etching process, as shown, for instance, in Fig. 23.15 where the fabrication of a GNR-based FET is shown [99]. First, graphene is grown at 1000 °C by using CVD on a copper layer and is then transferred to the final substrate. In detail, after the GNR growth, a layer of polymethyl methacrylate (PMMA) is spin-coated on top of the substrate, in order to lift off the GNR from it and to transfer to the target substrate, Fig. 23.15a. Next, the electrodes may be fabricated by depositing them by an electron-beam evaporation system, as shown in Fig. 23.15b. GNR arrays of different



Fig. 23.15 CVD-based fabrication of a GNR interconnect and its transfer to the target substrate. (a) transfer of CVD graphene onto substrates; (b) graphene patterning and contact metal deposition; (c) graphenenanoribbon patterning; (d) graphene etching; (e) final GNR array. (Reprinted with permission from Tan et al. [99]. Copyright (2013) American Chemical Society)

widths can be further fabricated using electron-beam lithography, Fig. 23.15c. Subsequently, oxygen plasma and chemical washing are used to remove the excess graphene to form nanoribbons (Fig. 23.15d) and excess PMMA (Fig. 23.15e), respectively.

This method is in principle suitable for industrial production, since it can be scaled to transferring large areas of graphene from arbitrary substrates to CMOS substrates. However, the transfer step is critical, being responsible for the final quality of the device in terms of the presence of defects and impurities [100]. Enhanced techniques may be adopted to preserve the smoothness of the GNR edges, such as the use of a gas-phase etching [101].

Other promising fabrication approaches are based on bottom-up techniques, such as controlled unwrapping of oxidized carbon nanotubes by means of sonication [97], or the use of 1D chains of carbon precursors [102]. The structure of the precursor may be tailored to obtain a good control over the GNR width and good edge smoothing. The present limits for the bottom-up approaches reside in their low applicability to substrates of interest for interconnects, such as Si or SiC, although some examples of self-growth on SiC substrate have been demonstrated [103]. An alternative bottom-up fabrication technique for graphene-based interconnects has been recently proposed in [104], where a low-cost fabrication of graphene flakes has been presented based on thermal expansion of intercalated graphite, and an interconnect on FR4 dielectric has been fabricated by a drop-cast technique. The interconnect has been created by self-assembly of graphene flakes, under the action of an external electric field.

As for carbon nanotubes, a single monolayer graphene nanoribbon cannot be used as an interconnect due to the huge value of the contact resistance, so a



Fig. 23.16 An intercalation-doped multilayer graphene nanoribbon interconnect and the achieved values of resistivity compared to a copper interconnect vs wire widths. (Reprinted with permission from Jiang et al. [106]. Copyright (2016) American Chemical Society)

configuration of practical use must exhibit a high number of GNRs fed in parallel in order to reduce the overall resistance. The most suitable solution, therefore, is that of using multilayer GNRs (MLGNRs) instead of monolayers.

As for the CNT bundles in Sect. 23.2, the MLGNR interconnects may be linked to the outer world through side or top contacts: in the first case, all GNR layers are physically connected to contacts, while in the second one, only the topmost layer is connected to the contacts. For this reason, top-contacted MLGNRs usually exhibit worse performance, although they are easier to fabricate. Anyway, simulations and experimental results on both top- and side-contacted MLGNRs have demonstrated that, with suitable doping, such interconnects may outperform copper ones, for instance, in terms of electrical resistance [105]. Indeed, stacking graphene monolayers at the van der Waals distance may lead to a structure similar to that of graphite, whose electrical properties are much worse than those of graphene due to interactions between layers. Intercalating doping molecules between the layers allows them to be electrically decoupled, so that N-stacked GNRs may behave as N parallel independent channels for electrical transport. In [106] a CVD synthesized MLGNR interconnect with FeCl₃ intercalation doping has been presented that matches copper resistivity at 20 nm width, Fig. 23.16. Furthermore, the width-dependent doping effect due to increasingly efficient FeCl₃ diffusion in scaled MLGNRs suggests that this interconnect may outperform Cu for sub-20 nm widths. A different dopant that has been considered is lithium, which has been shown to improve the conductivity by more than a factor of ten [107].

From a fabrication point of view, a challenging task is the control of the uniformity of doping on the GNR surface and at the interface with the substrate. A nonuniform accumulation of dopants close to the substrate leads to a screening effect of the innermost GNR layers, hence to their different contributions to the conduction, compared to the layers that are located far from substrate. A possible solution to this problem is the shift of the Fermi energy level of the upper layers.

23.4 Performance Analysis of Carbon Interconnects

Given their promising features, carbon materials such as carbon nanotubes and graphene nanoribbons have been included from almost a decade ago among the innovative materials for next-generation interconnects by the ITRS [3]. However, given the major issues of compatibility between their fabrication conditions and those of the standard CMOS technology discussed in Sect. 23.3, few examples of practical realizations of electronic circuits integrating carbon interconnects are so far available, such as those reported in Sect. 23.1. Therefore, many of the results related to the performance analysis of carbon interconnects are still based on simulation of models, although more and more accurate, that have been proposed in the last decade [108].

As a general result, it has been shown that, despite their huge contact resistance values, CNT and GNR interconnects may be arranged in such a way to be competitive or even better than copper ones for on-chip interconnects either at the local and at the global level [47, 108–111]. Carbon nanotube vias may also outperform copper ones, and their use has been largely investigated either as classical on-chip vias [112] and as through-silicon vias (TSVs), in the so-called 3D integration schemes [113–115, 116]. Promising results are also foreseen for carbon-based power interconnects in the chip power delivery networks [108, 117] and for the chip-to-package carbon interconnects such as pillar bumps [25].

Table 23.4, extracted from table INTC9 in [3], summarizes the current status for the use of carbon materials as interconnects, either considered as an alternative to copper or as native device interconnects.

Application	Option	Potential advantages	Primary concerns
Cu replacement	Carbon nanotube	Ballistic conduction in narrow lines, electromigration resistance	Quantum contact resistance, controlled placement, low den- sity, chirality control, substrate interactions, parametric spread
	Graphene nanoribbons	Ballistic conduction in narrow films, planar growth, electromigration resistance	Quantum contact resistance, controlled placement, control of the edges, deposition, etch stop- ping, stacking, substrate interactions
Native device interconnects	Carbon nanotube	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, fanout/branching and place- ment control
	Graphene nanoribbons	No contact resistance to device, ballistic transport over microns, support for multi- fanout	Quantum contact resistance to Cu, deposition and patterning processes

 Table 23.4
 Advantages and issues for carbon interconnects [3]

23.4.1 On-Chip Interconnects

On-chip interconnects are characterized by three main hierarchical levels, local, intermediate, and global, moving from the substrate to the package. Typical dimensions change from level to level and with the technology node considered: Table 23.1 reports the typical values of the cross-section dimensions for interconnects for two technology nodes, taken from [3]. Typical arrangements for on-chip interconnects are shown in Fig. 23.7, where they are made of bundles of CNTs or of multilayer GNRs.

Taking into account the considerations given in Sect. 23.2, if we assume wellaligned CNTs or GNR layers, without defects or irregular edges, the main aspects affecting their performance are the chirality, the density, and the contact resistance.

As for the chirality, statistically in a population of CNTs or GNRs, one-third of the population is metallic and two-third semiconducting. It is possible to increase the fraction of metallic samples, but this would increase the cost of their production. This statistic has a different impact on the different types of carbon materials: for instance, a semiconducting single-walled CNT does not contribute to the conductivity (see Table 23.3, M = 0), whereas in multi-walled CNTs, a significant contribution to the number of conducting channels can also come from semiconducting shells, depending on their diameter. Therefore, for a given cross section, the use of SWCNTs instead of MWCNTs leads to bundles with larger numbers of CNTs but with only one-third active in the electrical conduction. The choice is then related to this trade-off, along with the possibility to increase the density, i.e., to maximize the area occupied by CNTs in the bundle (filling factor). Note that putting the CNTs too close together to maximize density leads to unwanted inter-CNT interactions that result in a degradation of the electrical performance. The same happens, as pointed out in Sect. 23.3, when GNR layers are put at the minimum distance (van der Waals distance, about 0.34 nm): this condition maximizes the density, but the strong interlayer interactions lower the conductivity of the structure to values similar to graphite rather than graphene. Finally, a crucial parameter to be taken into account for performance analysis is the contact resistance, whose role has been discussed in Sect. 23.3.

Many efforts have been devoted in the recent literature to carry out a performance analysis for on-chip carbon interconnects. In particular, many works compare such interconnects to conventional ones, based on simulation results. The adopted models have been refined and improved in these years to include the realistic effects expected from the fabrication limits, as discussed in Sect. 23.3 [46, 47, 98, 108–111].

A parameter of major interest for an electrical interconnect is of course its electrical resistance or equivalently its electrical resistivity that must be as low as possible (ideally equal to zero), in order to mitigate issues like energy losses, signal delay, and Joule heating. The electrical resistance of a CNT interconnect has been predicted to be competitive with that of copper, at any hierarchical level of an integrated circuit, provided that high enough densities and low enough contact



Fig. 23.17 Electrical resistivity values predicted for Cu and CNT on-chip interconnects versus the line length, for (**a**) 14 nm node, local level; (**b**) 14 nm node, global level; (**c**) 22 nm node, local level; (**d**) 22 nm node, global level

resistances are obtained. As an example, Fig. 23.17 shows the DC electrical resistivity at room temperature obtained by assuming the resistance model (23.9)– (23.11), comparing CNT and copper interconnects at various hierarchical levels and for two different technology nodes. Here we assume a filling factor of 80% and a value for the parasitic resistance of 50 k Ω for each conduction channel. As shown, CNT interconnects exhibit lower resistivity from a given value of the line length on. For shorter length, the result is dominated by the huge values of the contact resistance. Of course, lowering the parasitic resistance would lead to a lower value for this transition length. The result is also dependent on the bundle density that must be high enough. Indeed, Table 23.5 reports the minimum density of metallic SWCNTs required to obtain the same resistivity as Cu interconnects, for the several technology nodes foreseen by the ITRS for the future.

Year	2015	2017	2019	2021
Technology node – physical gate length for HP logic (nm)		18	12	10
Copper resistivity (×10 ⁻⁸ Ω m)		5.08	5.85	6.84
SWCNT minimum density ($\times 10^{13}$ cm ⁻²)		0.96	0.81	0.66

 Table 23.5
 Minimum density of SWCNT interconnects to be competitive with copper ones



Fig. 23.18 Per-unit-length electrical resistance values predicted for GNR on-chip interconnects vs wire width (technology node). Several realizations of GNR lines are considered, differing from the edge-scattering coefficients, the Fermi level, and the mean free path, and compared to two realizations of Cu lines with two different aspect ratios, W/T. (Reprinted, with permission, from Rakheja et al. [98]. Copyright (2013) IEEE)

Another design parameter to be optimized is the CNT diameter that directly impacts the number of channels M (23.21) and hence the resistivity. A larger diameter means a higher value for M, but a smaller number of tubes for a given interconnect cross section. The impact of diameter is different from SWCNTs and MWCNTs due to the different role of the semiconducting shells in the electrical conductions; therefore a trade-off solution must be found case by case between the diameter of single CNT and density in the bundle.

As for GNR interconnects, their resistivity is usually worse than that of copper ones, as shown in Fig. 23.18, taken from [98]. The figure shows the per-unit-length electrical resistance values versus the line width, e.g., the technology node, comparing different realizations of GNR lines with Cu. In particular, different values of the edge-scattering coefficient P_{GNR} , the Fermi level E_f , and the substrate-limited mean free path λ_{SUB} are considered. As a general result, GNR resistance will become comparable to or even lower than Cu only for future technology nodes, with widths

Orientation	Cross-section dimensions, W and T or D (μ m)	Resistivity (mΩcm)	Reference
Vertical	D = 0.15	5.1	[119]
	D = 2	0.6	[120]
Horizontal	W = 0.1, T = 0.1	0.45	[121]
	W = 0.07, T = 0.07	0.5	[122]

Table 23.6 Measured electrical resistivity for on-chip CNT interconnects

lower than 6–7 nm, only assuming smooth edges and low Fermi levels and no additional scattering from the substrate. As pointed out in Sect. 23.2, for GNR interconnects to be competitive with Cu ones, intercalated MLGNR arrangements must be considered.

The available measured values for the electrical resistance or resistivity of CNT on-chip interconnects are generally far from the simulation results presented above or similar ones available in the literature [118]. The best performances obtained so far are summarized in Table 23.6, covering both vertical arrangements, such as on-chip CNT vias, and horizontal ones. As examples of the two types of interconnects, we report in Fig. 23.19 a CNT horizontal interconnect [89] and in Fig. 23.20 a CNT used to contact two transistors at different layers [119].

Another important performance indicator among the metrics to be considered for an interconnect is the propagation delay. To evaluate such a delay, we should refer to a signaling system like that schematically depicted in Fig. 23.21, where the carbon interconnect acts as a channel between a driver and a receiver. The propagation delay is of course dependent also on the equivalent circuit parameters of the devices connected to the carbon line, for instance, the equivalent capacitance of the buffer acting as the receiver. Typical results are provided in [47], where the delay associated to a circuit as that in Fig. 23.20 is studied by considering several types of CNT and GNR interconnects, assuming the ITRS [3] values for the local, intermediate, and global levels for an integrated circuit at the technology nodes of 22 and 14 nm. Carbon nanotube interconnects are supposed to be realized by means of MWCNTs or SWCNTs, and in the latter case, different metallic fractions are considered. As for the GNR ones, different values for edge-scattering coefficient p are considered. In addition, either neutral or intercalated multilayer graphene nanoribbons are considered.

Figure 23.22 shows the computed propagation delays, normalized to that predicted when assuming the interconnection to be made by copper. At the local level, carbon interconnects (except for monolayer GNR) exhibit comparable performance with respect to copper ones, due to the huge impact of the driver resistance over the propagation delay at such a level. The MWCNT solution is sensibly better for longer lines. At the intermediate level, usually the CNT lines outperform copper ones, and this behavior is much more pronounced at the global level. As for the GNR solution, Fig. 23.22 suggests that the only way to outperform copper is to realize doped GNRs with an edge-scattering coefficient p = 1, which is an ideal case, since realistic values are about 0.4–0.5. Lower propagation delays for GNR interconnects



Fig. 23.19 Horizontal CNT interconnects with two types of contact: (left) end-bonded; (right) all-around. (Reprinted from Chiodarelli et al. [89]. Copyright (2013), with permission from Elsevier)

even in cases of low values of the coefficient p are predicted in [98], where an optimal number of layers is chosen to minimize such a delay.

Figure 23.23 shows the delays obtained by considering GNR interconnects with two different values of mean free path λ_D and by considering both the side and the top contact solutions. Despite the low value of *p*, this optimized solution improves the performance at the local level, becoming better or comparable to copper, whereas at the intermediate level, the GNR solution is still worse.

Another important issue for a signaling system is signal integrity: a popular technique to check the signal integrity of a transmitting channel for high-speed digital signals is the analysis of the so-called eye diagram that is obtained by overlapping segments of a digital data stream arriving at the receiver in the same time frame [8]. The quality of the transmitting system is given by two metrics: the *eye-jitter* (related to the signal delays and responsible for synchronization errors) and the *eye-opening factor* (related to the signal distortion and responsible for false detections). To realize a good channel, the first indicator must be kept as low as possible, while the second should be as high as possible. Although the eye diagram



Fig. 23.20 A CNT-based via used to contact transistors at two different layers: (**a**) top view; (**b**) CNT via; (**c**) side view. (Reprinted from Vollebregt and Ishihara [119]. Copyright (2016), with permission from Elsevier)



features depend, of course, on the whole system given by the driver, interconnect, and receiver, the effects of the interconnect become more and more crucial as the frequencies increase and the dimensions decrease [8]. In particular, both the static and dynamic parameters of the interconnect influence the performance of the digital system.

In the following, a local-level system is analyzed, where the carbon interconnect in Fig. 23.20 is assumed to be composed by a horizontal trace at metal layer M1 and another horizontal trace at metal layer M2, with a via connecting M1 to M2. The technology node considered is 22 nm, with parameters as in Table 23.1.



Fig. 23.22 Signal delay values for the signaling system in Fig. 23.20 for different types of carbon interconnects, assuming two different technology nodes and hierarchical levels: (a) 14 nm, local level; (b) 22 nm, local level; (c) 14 nm, intermediate level; (d) 22 nm, intermediate level; (e) 14 nm, global level; (f) 22 nm, global level. The results are normalized to that of copper interconnect. Different values for the edge-scattering coefficient *p* are considered for the GNR lines that have been supposed either to be neutral (n-GNR) or intercalated (d-GNR). Different metallic fractions F_m are considered for SWCNT lines. (Reprinted, with permission, from Li et al. [47]. Copyright (2009) IEEE)

The interconnect is assumed to be made of bundles of SWCNTs of diameter 1 nm, with a metallic fraction $F_m = 0.3$. The driver is modeled as a voltage source of magnitude $V_s = 0.8V_{DD}$ and a series resistor of $2.5k\Omega$, while the receiver is modeled as a capacitor of capacitance 2 fF. Figure 23.24 shows the eye diagrams computed

Fig. 23.23 Signal delay values for different types of GNR interconnects compared to copper one, versus the technology nodes and hierarchical levels: (a) local level, with driver size line length equal to $1 \times$ and $10 \times$ gate pitches, respectively; (b) with driver size line length equal to $5 \times$ and $50 \times$ gate pitches, respectively. Different values for the mean free $\lambda_{\rm D}$ are considered, and top and side contact configurations are simulated. The edgescattering coefficient p is equal to 0.2. (Reprinted, with permission, from Rakheja et al. [98]. Copyright (2013) IEEE)



for such a system, with different values of data rate (DR) and rise time t_r . Table 23.7 summarizes the computed values for the jitter and the opening factor for different DR, showing the capability of the CNT solution to outperform the copper one.

23.4.2 Through-Silicon Vias and Pillar Bumps

As pointed out in Sect. 23.2, from a technology point of view, the fabrication of vertical bundles of CNTs has reached satisfactory levels in terms of density, direction control, CMOS compatibility, and contact resistance. Consequently, CNTs are



Fig. 23.24 Eye diagrams for the circuit in Fig. 23.20, assuming an on-chip interconnect at the local level (22 nm technology node), at different data rate (DR) values: (a) CNT case, DR = 5Gbit/s; (b) Cu case, DR = 5Gbit/s; (c) CNT case, DR = 10Gbit/s; (d) Cu case, DR = 10Gbit/s

	DR [Gbit/s]	Eye jitter [ps – rms]	Eye-opening factor
Copper	1	_	0.99
	3	1.70	0.99
	5	4.80	-
	10	11.52	0.54
	20	16.53	0.28
CNT	1	2.24	1.00
	3	_	0.90
	5	0.38	0.95
	10	1.73	0.97
	20	3.19	0.80

Table 23.7 Summary of the results of the eye diagram analysis for on-chip interconnects

proposed as serious candidates for realizing vertical interconnects like throughsilicon vias and pillar bumps.

Through-silicon vias (TSVs) are vertical interconnects passing through stacked integrated circuits (ICs), a solution that has enabled the so-called 3D-IC technology providing many benefits such as reduced delay, increased bandwidth, and energy efficiency [123, 124]. Pillar bumps are vertical interconnects used in the chip-to-package

and chip-on-chip bonding technology, to replace costly past solutions like wire bonding [125]. Both types of interconnects suffer from two main problems: the electromigration of copper atoms due to the high current density and the skin effect due to the high frequency. Therefore, in the past years, carbon nanotube interconnects have been proposed in order to mitigate such problems. As pointed out in Sect. 23.1, CNTs may carry a current density of about 10⁹ A/cm² [21], two orders of magnitude higher than the maximum value obtainable for Cu, so exhibiting a high electromigration resistance [126]. In addition, the high-frequency behavior of the CNT bundles is better than the Cu solution [127, 128], for instance, due to a lower sensitivity to the skin effect [129].

From a theoretical point of view, this is due to the role of the huge kinetic inductance which usually hides the magnetic one, as pointed out in Sect. 23.2.2. Specifically, if we realize a TSV (of cross section S_b and height l) with a bundle of N_b CNTs, and assume the equivalent single-conductor model described in Sect. 23.2.3, the relation between the total current in the bundle, $I_b = \sum_{n=1}^{N_b} I_n$, and the voltage V_b can be expressed as:

$$V_{b} = Z_{b}I_{b} = \left(\rho_{b}' + i\rho_{b}''\right)\frac{l}{S_{b}}I_{b},$$
(23.22)

where $\rho_b = \rho'_b + i\rho''_b$ may be regarded as the *bundle equivalent resistivity*. Assuming that all CNTs in the bundle are equal and that the kinetic inductance dominates over the magnetic one, the equivalent resistivity becomes [47]:

$$\rho_b' + i\rho_b'' = \rho_0 (1 + i\omega/\nu), \qquad (23.23)$$

where ν is the collision frequency and the DC value ρ_0 is given by:

$$\rho_0 = \frac{R_{CNT} S_b}{F_M N_b l},\tag{23.24}$$

being R_{CNT} the resistance of the single CNT and F_M the metal fraction. As for the resistance value, similar considerations hold as those expressed for conventional on-chip vias in Sect. 23.4.1. However, TSVs or pillar bumps are characterized by diameters of the order of μ m, hence larger dimensions with respect to on-chip vias analyzed in Sect. 23.4.1, and hence their electrical resistance values are usually higher than for the copper realization, since the copper resistivity value is in the bulk value region (see Fig. 23.2). Therefore, the use of CNT improves the reliability but usually worsens the electrical performance of such interconnects. A possible compromise is the use of Cu-CNT composite [130].

For high frequencies, also the imaginary part of resistivity (related to the inductance) plays a role. We can define an equivalent skin depth as follows [47]:

$$\delta = \sqrt{\frac{2\rho_0}{\omega\mu}} \sqrt{\left[\left(\frac{\omega}{\nu}\right)^2 + 1\right]} \left(\sqrt{\left(\frac{\omega}{\nu}\right)^2 + 1} - \frac{\omega}{\nu}\right).$$
(23.25)

Expression (23.25) reduces to the classical definition of the skin depth if $\omega/\nu < < 1$, i.e., when the mean free path is small enough (e.g., ~40 nm in copper). For CNTs, however, larger mean free path values (hundreds of μ m) induce a saturation in the skin depth as frequency increases, according to (23.25).

As an example, let us consider a TSV with the typical dimensions predicted by the ITRS [3] for the 14 nm technology, i.e., diameter equal to 1.2 μ m and height equal to 30 μ m, assuming a current of 10 mA flowing through it. Let us consider the TSV to be made either by copper (assuming the resistivity parameters given in Fig. 23.2 for bulk copper) or by a bundle of MWCNTs. Each MWCNT has outer diameter $D_{out} = 30$ nm and inner diameter $D_{in} = 0.5D_{out}$, with one-third of metallic shells. Figure 23.25 shows the distribution in the via cross section of the current density computed at room temperature at a frequency of 200 GHz. Figure 23.25a refers to the copper via, where the skin effect is evident, whereas Fig. 23.25b referring to the MWCNT case shows a quite uniform current density. To clarify the role of the kinetic term in the inductance, Fig. 23.25c shows the result obtained for the MWCNT case after removing the kinetic inductance: in this case, the skin effect is again no longer negligible.

The presence of the kinetic inductance also provides benefits in terms of EMC behavior of the interconnects, by mitigating, for instance, the proximity effect [36] and the crosstalk noise between adjacent interconnects [54, 131]. Indeed, new concepts and new solution for the EMC problems at the nanoscale arise due to the features of parameters like the kinetic inductance or the quantum capacitance, as shown in [10].

One of the reasons to use CNT bundles as pillar bumps (e.g., Fig. 23.3) is the possibility to achieve good reliability performance while implementing new heat removal technologies. Indeed, the heat management of future nanoelectronics requires new approaches: using the conventional approach, for instance, the cooler for technology solutions like the systems in package could easily become larger than the semiconductor itself. Carbon nanotubes could, for instance, be used as microchannel coolers in thermofluidic cooling approaches. In addition, they are also proposed as a thermal interface material, although the main limit is still given by the possibility of achieving high-density aligned CNTs in a polymer matrix, without degrading the thermal conductivity [15].

In order to investigate the electrical properties of CNT pillar bumps, let us refer to the scheme depicted in Fig. 23.7a: the two vertical pillars are assumed to be realized by using Cu, a bundle of SWCNTs, or a bundle of MWCNTs. As usual, we assume that only one-third of the total CNT shells are metallic. As pointed out in Sect. 23.2, since the semiconducting SWCNTs do not contribute to the conduction, very high-density bundles must be fabricated to have low-resistance CNT pillars. In MWCNTs, on the other hand, the semiconducting shells also contribute to the total number of conducting channels, and therefore the optimal density is a trade-off between the CNT diameter

Fig. 23.25 Distribution of the current density in the cross section of a TSV for the 14 nm technology at 200 GHz: (a) Cu; (b) MWCNT; (c) MWCNT without the effect of the kinetic inductance L_k (Reprinted, with permission, from Chiariello et al. [56]. Copyright (2103), IEEE)





Fig. 23.26 Equivalent resistance of pillar bumps made by carbon nanotube and copper. The solution obtained by neglecting the skin effect in the copper bump is also plotted

and its number of shells. Let us consider the pillar bumps proposed in [132], having a diameter $D = 15 \,\mu\text{m}$ and a wire bond pitch of 30 μm , assuming an operating frequency of 10 GHz. For the Cu solution, we can assume the bulk value of resistivity, i.e., $\rho_{Cu} = 1.7 \cdot 10^{-8} \,\Omega\text{m}$. The SWCNT diameters are assumed to be 2 nm, whereas for the MWCNTs, we assume an outer diameter $D_{out} = 30$ nm, inner diameter $D_{in} = 0.5 D_{out}$, and an inter-shell distance 0.34 nm. In both cases, a density of 80% and a contact resistance of 20 $k\Omega$ per shell are assumed.

In terms of electrical properties, a good packaging interconnect must be characterized by a low equivalent series impedance. For this case, the equivalent inductances are well beyond the maximum allowed of $5 - 10 \ pH$; hence we can focus on the equivalent resistance. Figure 23.26 compares the resistance values obtained for Cu and CNT bumps, for aspect ratios ranging from 1 to 5. The lowest values are obtained by using MWCNT bundles, whereas SWCNT bundles show higher resistance values, close to those related to the copper realization. Note that at the given frequency, the skin effect in the copper pillar plays a relevant role: indeed, the resistance obtained by neglecting the skin effect would be much lower, as shown in Fig. 23.26. The performance of SWCNTs can be further improved by reducing the contact resistance.

23.4.3 Power Interconnects

As already pointed out, carbon materials are considered to be promising candidates for the realization of novel power interconnects in next-generation ICs, given the possibility to match two major requirements for building resilient power delivery networks (PDNs): higher current density and efficient heat management. Indeed, future PDNs are required to carry current densities of the order of MA/cm², corresponding to a volumetric heat production of the order of 10^3-10^4 W/mm³, which would be impossible if the PDNs were fabricated out of conventional metals, like copper and aluminum.

The electrical behavior of power interconnect in terms of resistance, frequency dependence, and current density is similar to that of on-chip interconnects previously analyzed in Sect. 23.4.1. However, speaking about power interconnects, it is of interest to provide additional results about their electrothermal behavior, starting from the considerations given in Sect. 23.2.4. Taking into account electrothermal effects is, of course, also important for on-chip interconnects or TSVs [115], but it becomes a must when dealing with power interconnects. Indeed, in PDNs the power dissipation induces elevated temperatures, which directly impact interconnect parameters (i.e., R, L, and C values), since material properties such as the electrical resistivity are temperature dependent. Ultimately, any change in interconnect parameters varies both dynamic and leakage power consumption and impacts the so-called power integrity by modifying the performance indicators such as the voltage drop (a measure of the unwanted voltage fluctuations over the PDN).

The thermal impact on PDNs may be mitigated due to the favorable thermal properties of CNTs and graphene with respect to traditional materials. Specifically, it is possible to tailor the carbon interconnect characteristics in order to have an electrical resistance quite insensitive to the temperature variation or even decreasing with increasing temperature. As already mentioned in Sect. 23.2.4, this favorable behavior is the consequence of a counteracting mechanism between the increase of the number of conducting channels M (23.21) and the decrease of the mean free path l_{mfp} as the temperature increases. Both parameters influence the electrical resistance of a carbon interconnect, as shown in (23.10) and (23.11).

The temperature dependence of an electrical resistance R(T) is usually studied by means of the *temperature coefficient of the resistance* (TCR), defined as:

$$TCR = \frac{1}{R} \frac{dR}{dT}.$$
(23.26)

Conventional conducting materials always exhibit a TCR > 0, i.e., an electrical resistance that increases with increasing temperature. Let us consider the popular law for the temperature dependence of the resistance of a copper wire of length l and cross-section S:

$$R(T) = \rho_0 (1 + \alpha_0 (T - T_0)) \frac{l}{S}, \qquad (23.27)$$

where T_0 is the room temperature, ρ_0 is the resistivity at $T = T_0$, and α_0 is a temperature coefficient. Both ρ_0 and α_0 depend on the transverse dimension of the copper interconnect: for instance, for bulk conductors, it is $\rho_0 \approx 1.7 \cdot 10^{-8} \Omega m$ and $\alpha_0 = 0.0039 \text{ K}^{-1}$, whereas for nanoscale ones (for instance, at the 22 nm node), it is $\alpha_0 = 0.0012 \text{ K}^{-1}$ and $\rho_0 \approx [2 \rightarrow 6] \,\mu\Omega cm$, depending on the considered interconnect



Fig. 23.27 Temperature coefficient of the resistance versus line length, for Cu and SWCNT and MWCNT for two different sizes, at T = 300 K

level. By applying (23.26)–(23.27), we obtain $TCR = \alpha_0$, which means that for copper, this value is always positive and slightly decreasing at the nanoscale. Instead, by applying (23.26) to the resistance of a carbon interconnect (23.10)–(23.11), it is possible to obtain a much more complicated behavior of the *TCR* that depends on temperature itself but also on the line length, given the different roles played by the intrinsic and contact resistances. In particular, a more realistic model for the parasitic term R_p in (23.11) must take also into account the dependence on temperature *T*, whereas the quantum term R_0 is constant with *T*. A simple model for R_p is suggested in [63] and resembles (23.27), assuming as *S* the contact area and as *l* a characteristic length of the contact.

Taking into account also the latter consideration, the *TCR*s computed for CNT and Cu interconnects at room temperature are reported in Fig. 23.27. Here, metallic CNTs are considered, with two different diameters values: 1 and 3 nm for SWCNTs and 20 nm and 40 nm for MWCNTs. As for the parasitic resistance, here we assume $R_p(T_0) = 1 \text{ k}\Omega$ and $\alpha_0 = 10^{-4} \text{ K}^{-1}$. The TCR for SWCNTs is always positive: this is due to the fact that for such CNTs, the number of channels *M* is quite insensitive to *T*; see (23.21) and Table 23.3. Instead, TCRs close to zero or even negative may be obtained by using MWCNTs: the lengths for which the TCR is negative can be modulated by changing the dimension of the diameters or by modifying the impact of the parasitic resistance.

Experimental evidence of a negative *TCR* has been provided for isolated MWCNTs [20] and GNRs [62]. However, when the CNTs are bundled, such a behavior often disappears due to the collective effects and the degradation of the contacts. Few examples of bundled CNTs with negative TCRs are available so far: in [63] this behavior has been experimentally found for MWCNT vias with lengths up to 3 μ m, also putting on evidence the side effects due to contact resistance. A similar



Fig. 23.28 The considered power delivery network: (**a**) schematic of the two-layer structure, with the heat sink; (**b**) equivalent electrical and (**c**) thermal circuit model at each grid node (Reprinted, with permission, from Magnani et al. [117]. Copyright (2016) IEEE)

result is found in [80], again for CNT vias. Recently, a negative TCR has been obtained also in longer (hundreds of μ m) horizontal conductors, realized by CNT bundles [84].

To investigate the electrothermal performance of a carbon-based power delivery network, let us consider the simple structure sketched in Fig. 23.28, where a power and ground plane are separated by an insulation layer and connected to VDD and GND supply pins, respectively. The chip is connected to a heat sink on one side for heat dissipation. The electrical model is given by two networks corresponding to the two layers. At each grid node, the conductors are represented by means of a series impedance; see Fig. 23.28b. Each node of a grid is connected to the corresponding one on the other grid via a capacitor in parallel with a current source to represent the circuit switching activity, i.e., the current demand of a circuit connected between VDD and GND pins. The solution of the electrical problem provides the so-called voltage drop at any generic node i, namely:

$$V_d(i) = V_{DD} - (V_n(i) - V_g(i))$$
(23.28)

 $V_n(i)$ and $V_g(i)$ being the node potentials with respect to the power and ground plane references, respectively.

As for the thermal problem, the temperature distribution over the PDN is found by solution of a heat equation like (23.17). However, in PDNs it is possible to assume that the heat mainly flows along the grid conductors (grids and vias), the heat exchange between copper and dielectric being negligible. Therefore, (23.17) may be discretized with an equivalent thermal circuit whose generic node is depicted in Fig. 23.28c, R_{TH} being the thermal resistance corresponding to the generic track of the conductor and R_{HS} the heat sink resistance.

In other words, the thermal problem may be cast as an equivalent electrical one, where the heat flow plays the role of the electrical current and the temperature difference corresponds to the electrical voltage.

As pointed out in Sect. 23.2.4, the coupling between the two problems is given by the production term in (23.17): this term corresponds in Fig. 23.28c to the source P_s + P_J , being the two terms related to the switching activity and to the Joule effect in the conductors, respectively. Therefore, this term depends on the solution of the electrical problem. On the other hand, the solution of the thermal problem changes

the electrical resistance values, according to (23.27) or similar laws. A popular way to solve this coupled problem is through the so-called relaxation approach where, after giving an initial guess for the temperature, iteratively the heat equation is solved providing the temperature distribution, the temperature-dependent electrical parameters are updated, and the electrical problem is solved. Then, the heat production term is updated, until convergence is reached.

To study the performance of a carbon PDN, let us refer to a global-level interconnect at the 22 nm technology node (Table 23.1), with a chip core of dimensions 0.5×0.5 mm. The PDN grid is made of 250×250 nodes and is fed at the four corners of each elementary stamp of 25×25 nodes. The thermal resistance of the heat sink is assumed to be $100 \times$ the value of the thermal resistance of a single PDN branch. For such a case, the dynamic effects can be neglected, as shown in [117]; hence a pure resistive model can be assumed. As for the copper realization, we assume for the resistance the classical model (23.27) with the room temperature parameters typical for the 22 nm technology, namely, $\rho_0 = 2.94 \ \mu\Omega cm$ and $\alpha_0 = 0.0012 \ \text{K}^{-1}$. The copper thermal conductivity is assumed to be $k_m = 193 \ \text{W/mK}$.

As for the carbon PDNs, we consider a case where the interconnects are made by bundles of MWCNTs of 40 nm external diameters, 80% density, and metallic fraction of 1/3. For MWCNTs, a thermal conductivity of 200 W/mK was assumed. Note that this value of thermal conductivity is far from the values of above 3000 W/mK, reported, for instance, in [24]. Such outstanding values, however, correspond to favorable cases with excellent control of the CNT quality, e.g., in terms of alignment. A more realistic case must take into account the effect of intra-bundle coupling, imperfections, and misalignment, which typically lower the thermal conductivity of about one order of magnitude.

Next, a graphene realization is also considered, by assuming each track of the PDN to be made by a stack of GNRs, put at the van der Waals distance, with a metallic fraction of 1/3. As for the thermal conductivity, we assume a realistic value of 1500 W/mK. For both the CNT realizations, we neglect the contribution of the parasitic term in the contact resistance in (23.11); therefore we consider ideal contacts.

In Fig. 23.29 we report the results of the performance analysis of the considered PDNs, carried out by computing the maximum voltage drop (23.28) in Fig. 23.29a and the maximum temperature rise in Fig. 23.29b, over the PDN nodes, for different values of the switching current. The CNT realization provides the best electrical and thermal performance, with a voltage drop always lower than 0.1 V and a temperature rise not exceeding 50 K. In addition, CNT power interconnects perform well in a wide range of the switching current I_0 . The GNR realization is always worse than the CNT one, both in terms of voltage drop and of temperature rise. Given the above dimensions and parameters, the total number of channels for GNRs is lower than for MWCNTs, leading to higher electrical resistance values for GNR power interconnects. Compared to the copper realization, the GNR one provides a higher voltage drop for low values of I_0 , but for higher values, the behavior is much better. However, in terms of thermal behavior, the GNR solution outperforms the Cu one. If we include the effect of the parasitic contact resistance, we expect to have a similar behavior, but a reduced range of admissible switching current I_0 .



Fig. 23.29 Performance analysis of the PDNs, comparing Cu, CNT, and GNR cases: (a) maximum voltage drop, (b) maximum temperature rise, vs current source

23.5 Conclusions

As the electronics of the twenty-first century is approaching the end of the classical roadmap, carbon materials are serious candidates to replace conventional ones in realizing novel interconnects. The main reason for such an interest lies in the outstanding electrical, thermal, and mechanical properties of carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), suggesting that carbon-based interconnects may meet the tight requirements for the future ultra-scaled technology, in terms of current density, power consumption, signal and power integrity, heat management, mechanical stresses, reliability, and resiliency.

Given this interest, in the past decade, an intense modeling activity has provided simple although more and more accurate equivalent circuit models to describe interconnects made by CNTs or GNRs. The most common modeling approach is based on a compromise between the need for models simple enough to be integrated in the standard design flow of the IC designers and the need for an accurate inclusion of the quantum effects arising at the nanoscale. This goal has been achieved by modeling the carbon interconnects in the frame of the transmission line model, where the classical magnetic and electrical parameters are corrected by novel terms taking into account kinetic and quantum effects at nanoscale. These terms are responsible for novel behavior and phenomena that give to such interconnects many favorable properties but also set some serious limits to their practical use.

Electrical and thermal ballistic transport, reduced delay, insensitivity to skin effect, mitigation of electromigration, and thermal stability are among the fascinating properties foreseen by the simulation results. On the other hand, huge resistance due to the contacts and slow propagation velocity are some of the main expected drawbacks. Simulation results for carbon-based signal and power on-chip interconnects, through-silicon vias and pillar bumps, confirm the possibility for such interconnects to outperform the classical copper ones for scaled technologies, with typical dimensions equal to or less than tens of nanometers.

In practical applications, the promising results coming from simulations are strictly related to the possibility of realizing high-quality bundles of CNTs or stacks of GNRs, with a satisfactory control over parameters like chirality, density, alignment, defects, surface roughness, and contacts. Therefore, major efforts have been made in the last years to assess reliable design approaches and effective fabrication processes for carbon interconnects. Although technological solutions have been demonstrated to solve issues like the compatibility of the growth temperature with the standard CMOS technology, the needed density and degree of alignment, the presence of defects, and the contact quality, these solutions are still not suitable for mass production, which would require a monolithic integration of carbon interconnects into future VLSI circuits. Therefore, only limited performances have been achieved with carbon interconnects so far, and few examples of integration with CMOS technology have been demonstrated. In other words, up to now carbon materials have failed to deliver their promise of realizing better interconnects with respect to conventional materials. The most promising progress could be witnessed in the development of hybrid copper/carbon materials or in the smart use of dopants and functionalization. Novel perspectives can also be given by the rapid development of stackable technology, where the interconnects are requested to link many layers of active components. Carbon electronics using 2D materials like graphene in the active x-y layers with vertical (z-axis) CNT interconnects, at least for local connections, may be the best solution to realize an all-carbon interconnection structure.

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Chapter 24 Carbon Nanotubes for Thermal Management of Microsystems



Johan Liu and Teng Wang

24.1 Introduction

One important function of electronics packaging is to remove the heat generated by the integrated circuits (ICs). Efficient cooling requires both high heat conduction within the package and efficient heat removal from the package. Elevated temperature is damaging to the chip and its package. Material mismatch causes mechanical stress leading to fatigue, creep, and finally failure; interconnects can melt, and electromigration within the IC is speeded up. Efficient heat removal is not always the case. Plastics is a common packaging material as it is electrically insulating and cheap. The thermal conductivity is, however low, about 0.2 W/mK compared to that of metals (aluminum 220 W/mK and copper 400 W/mK). Other important factors are the heat spreading and thermal interface materials. The components are often mounted on a polymer board which is only cooled by air. The heat transfer coefficient is only 5–15 W/m² K for natural convection and 15–250 W/m² K for forced convection in gases [1].

As electronic circuits grow denser and the power consumption per unit area increases, new more efficient technologies for heat removal are necessary. Heat fluxes from the IC on the order of 100 W/cm² (1,000,000 W/m²) are not rare. A heat transfer coefficient (including a possible area enlarging factor) of 20,000 W/m² K is needed to accommodate a heat flux of 100 W/cm² at a temperature difference of 50 K. The application of nanotechnologies is considered as a revolutionary approach

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and the overall thermal performance of the package is complex.

Fig. 24.1 A model of the heat path in a component mounted with a heat sink on a PCB with a heat sink on the back

to meet the tougher requirements for thermal management of microsystems (Fig. 24.1).

There are two possible approaches to improve the cooling of microelectronic packages: the first is to improve the thermal conductivity of the packaging material and package geometry so that the thermal gradient within it becomes smaller. The second is to improve the heat removal, i.e., increasing the effect of the convective heat transfer, from the surface or from the inside of the package. Both approaches are discussed in this chapter. The first one is to make thermal interface materials (TIMs) by embedding carbon nanotubes (CNTs) or other nanoscale thermal conductive particles in nanofibers prepared by electrospinning. The second approach is to build microchannel coolers based on carbon nanotubes. A brief introduction to the physical background of heat transfer is also included in this chapter.

24.2 Physical Background

There exist three basic heat transfer mechanisms: conduction, convection, and radiation. In electronics the first two mechanisms dominate, and consequently radiation is often neglected by engineers. Therefore only conduction and convection are discussed in this section.
24.2.1 Conduction

Heat transfer by conduction Q, over a certain area A, depends on the thermal conductivity k, of the material and the temperature gradient ∇T . The law of heat conduction is also known as Fourier's law:

$$Q = k \cdot \nabla T \cdot A \tag{24.1}$$

In one dimension with temperature difference Δ , *T* over distance *l*:

$$Q = \frac{k \cdot \Delta T \cdot A}{l} \tag{24.2}$$

Heat transport in solids and fluids takes place via two effects: lattice vibration (phonons) and electron migration. Materials (metals) with high electrical conductivity are generally better thermal conductors as electrons are involved in the heat transfer. There is almost no transfer of electrons in insulators, so heat conduction must rely on lattice vibrations and is thus poorer.

24.2.1.1 Conduction in Composites

The denser and more uniform a material is the better its thermal conductivity. The conductivity of insulators is reduced by different types of phonon scattering processes. The scattering of phonons in composite materials is mainly due to acoustic mismatch between filler and matrix [2]. For a certain filler type and volume fraction, there are the following methods for increasing the thermal conductivity:

- Decreasing the number of thermally resistant junctions, e.g., by minimizing the number of polymer layers between fillers, for example, by using larger filler particles
- · Forming conducting networks by suitable packing
- Minimizing filler-matrix interfacial defects

Thermal conductivity can be estimated by the semiempirical theory of Lewis and Nielsen [3]. According to this theory, conduction of the composite is dependent on volume fraction and heat conduction of the filler, heat conduction of the matrix, and the filler shape. The basic estimate for composites can be done according to Lewis-Nielsen theory by using the following formulae:

$$k_C = k_M \frac{1 + AB\phi_F}{1 - B\psi\phi_F} \tag{24.3}$$

$$B = \frac{k_F / k_M - 1}{k_F / k_M + A}$$
(24.4)

$$\psi = 1 + \frac{1 - \phi_M}{\phi_M^2} \phi_F \tag{24.5}$$

where φ_M is the maximum filler load and *A* is a parameter depending on particle shape. Both are given in tables for different geometries (empirical and theoretical values). φ_F is the volume fraction filler; k_F , k_M , and k_C are the thermal conductivities of filler, matrix, and composite. In this theory rods or fibers increase the thermal conductivity more than spheres of the same thermal conductivity and volume fraction. However, the theory does not explicitly take into account the size of particles or deal with more than two phases. Miloh and Benveniste suggested a method for the estimation of effective thermal conductivity of three phase composites with ellipsoidal inclusions [4].

Based on the above, it is obvious that elongated and well-dispersed particles forming networks are necessary to produce composites with high thermal conductivity. Filler-matrix interfacial contact can be improved by surface treatment of the particles and addition of coupling agents [5–7]. If untreated, the filler particles will form agglomerates in the epoxy matrix, so the particles are treated to render the surfaces hydrophobic. The coupling agent can also contain a functional group to form a chemical bond to the polymer.

24.2.1.2 Thermal Resistance

Thermal resistance, R_{th} , is a common way to define the cooling capabilities of a system. R_{th} is analogous to electrical resistance with the temperature drop, ΔT , as the driving force instead of electrical potential, and is defined as the temperature drop divided by the heat flow:

$$R_{th} = \frac{\Delta T}{q} = \frac{l}{k \cdot A} \tag{24.6}$$

The cooling of electronic systems can be characterized by the thermal resistance between the heat source (the chip) and the ambient. The thermal resistance depends of the thickness, cross-sectional area, and thermal conductivity of materials around the heat source and of the heat transfer coefficient h, to surrounding fluid (e.g., air or liquid coolant). In contrast to thermal conductivity, which is an inherent material quality, thermal resistance is a geometry-dependent property specific for each system.

24.2.2 Convection

Heat transfer by convection occurs between a solid surface and adjacent moving fluid and consists of two mechanisms; random molecular motion (diffusion) and macroscopic bulk motion in the fluid. Closest to the surface, the velocity is zero due to interaction with the solid, and from there it increases to the bulk velocity, v_{∞} . The same occurs for the temperature which changes from surface temperature, T_s , to the bulk temperature, T_{∞} . These regions are caller boundary velocity layer and thermal boundary layers and do not need to be the same size.

Convective heat transfer can be by either natural convection or forced convection. The cause for natural convection is the density difference in fluids due to temperature variations. Forced convection is obtained by an external force that puts the fluid in motion. In electronics this can, for example, be achieved with a fan for air or pump for fluid. Convective heat transfer can also be classified according to the flow regime, laminar or turbulent. Laminar flow is characterized by low pressure drop, neglecting mixing. Laminar flow occurs at low flow rates and small dimensions. When the flow velocity increases, the flow becomes unstable, vortices occur, and at a certain point, the fluid pattern changes to chaotic, i.e., turbulent. The pressure drop will be much higher, but the heat transfer within the fluid will also mix much better. In electronic systems with their small dimensions and low flow rates, laminar flow is usually the case, and most engineering rules of thumb are built on this assumption.

To determine the flow regime, the Reynolds number can be used. The Reynolds number is a dimensionless number that describes the ratio of the kinematic and viscous forces in the fluid. At a certain Reynolds number, the flow will undergo a transition from laminar to turbulent. The value varies for different geometries. From the definition we see that low dimensions lead to low numbers, which is taken advantage in microfluidics. The Reynolds number is defined as:

$$\operatorname{Re} \equiv \frac{v \cdot l}{v} = \frac{\rho \cdot v \cdot l}{\eta}$$
(24.7)

Laminar flow can be described by the Navier-Stokes equations, which describe how the velocities, v, u, and w, in different direction, and pressure, p, are related.

The equations are the continuity equation:

$$\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y} + \frac{\partial w}{\partial z} = 0$$
(24.8)

and the momentum equations in the x-, y-, and z-directions:

$$\left(\rho\frac{\partial u}{\partial t} + \rho u\frac{\partial u}{\partial x} + \rho v\frac{\partial u}{\partial y} + \rho w\frac{\partial u}{\partial z}\right) = \rho g_x - \frac{\partial p}{\partial x} + \mu \left(\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 u}{\partial z^2}\right) \quad (24.9)$$

$$\left(\rho\frac{\partial v}{\partial t} + \rho u\frac{\partial v}{\partial x} + \rho v\frac{\partial v}{\partial y} + \rho w\frac{\partial v}{\partial z}\right) = \rho g_{y} - \frac{\partial p}{\partial y} + \mu \left(\frac{\partial^{2} v}{\partial x^{2}} + \frac{\partial^{2} v}{\partial y^{2}} + \frac{\partial^{2} v}{\partial z^{2}}\right) \quad (24.10)$$

$$\left(\rho\frac{\partial w}{\partial t} + \rho u\frac{\partial w}{\partial x} + \rho v\frac{\partial w}{\partial y} + \rho\frac{\partial w}{\partial z}\right) = \rho g_z - \frac{\partial p}{\partial z} + \mu \left(\frac{\partial^2 w}{\partial x^2} + \frac{\partial^2 w}{\partial y^2} + \frac{\partial^2 w}{\partial z^2}\right)$$
(24.11)

These equations are a set of coupled differential equations and in practice are extremely difficult to solve analytically. Instead, computational fluid dynamics (CFD) is used to solve flow problems. For an incompressible, Newtonian fluid with uniform viscosity and small temperature differences, the system can be described by the continuity and momentum equations. If the flow is compressible, or if heat fluxes occur, at least one extra equation is required.

24.2.2.1 Flow in Microchannels

The term "micro" can be used for channels with hydraulic diameters of ten to several hundred micrometers. Fluid mechanics in microscopic scale is different from fluid mechanics at large scale. The Navier-Stokes equations and other models of fluid mechanics are based on the fact that the fluid can be treated as a continuum. However, as the scale shrinks, the number of molecules in the system becomes fewer, and a point is reached when each molecule has larger chance to interact with surrounding walls that with another molecule of its own kind. At this situation it could be awkward to model the fluid as a continuum, and it should rather be modeled as individual molecules. According to Nguyen [8] this limit for water is reached at about 10 nm. At very small scale and high shearing, the Newtonian behavior of the fluid breaks down, and the macroscopic nonslip boundary condition (velocity is zero at interface) between fluid and surface cannot be used. According to Nguyen this limit is reached well above the shear rates which were reached in the experimental setup. Recent experiments for circular and rectangular cross-sectional microchannels [9, 10] have shown that the transition from laminar to turbulent flows occurs at about same Reynolds number for flow at micro- and macroscales.

24.3 Nano-thermal Interface Materials

Heat removal is crucial to the performance and reliability of microelectronic systems, as the heat generated by integrated circuits keeps increasing significantly. The objective of the present research work is to develop a new class of nano-thermal interface materials (nano-TIMs) using the electrospinning methodology by embedding nano-thermally conductive particles in nanofibers to enhance heat removal between the chip and the heat sink/substrate [11].

Electrospinning is the process of subjecting a polymer solution to an electric field [12–16]. The applied voltage breaks down the surface tension at the capillary tip (called Taylor's cone), and as the charged solution moves in air, the solvents



20.0kV x700 20µm ⊢

evaporate to produce nanofibers on a collector. The electrospinning setup consists mainly of a high-voltage source, a capillary tube, a needle, and a collector (Fig. 24.2).

Nanoparticles of silver, silicon carbide, and multiwall carbon nanotubes are added as thermal conductivity enhancement promoters. The developed nano-TIMs are soaked after spinning in some conducting liquids to enhance the thermal conductivity and wetting performance. To determine the maximum temperature the resins can withstand, differential scanning calorimetry (DSC) and thermogravimetric analysis (TGA) have been utilized.

Figure 24.3 shows a SEM picture of a polymer resin nano-TIM. SEM pictures of nano-TIMs embedded with nano-silver particles and CNTs soaked in some conducting fluids are shown in Fig. 24.4.

Fig. 24.4 SEM pictures of nano-TIMs embedded with nano-Ag (a) and CNTs (b)





In order to enhance the adhesion strength of the nano-TIM to the substrate, adhesives are also jetted in the same process as the formation of the nano-TIM. An example of the nano-TIM with adhesive function is shown in Fig. 24.5. By doing so, a complete nano-TIM tape is formed.

Table 24.1 summarizes the results for the various nano-TIMs in comparison with the two commercial samples, indicating that the nano-TIM with CNT and resin A can offer similar thermal conductivity, three to nine times lower thermal resistivity, similar operation temperature range and degradation behavior, two to five times better ultimate tensile strength, and much higher Young's modulus. For the nano-TIM with nano-Ag particles and resin B, similar thermal resistivity, temperature operation range, and degradation behavior as compared with the commercial samples were obtained, but the mechanical properties are about 10–20 times better in terms of ultimate tensile strength, and elasticity and Young's modulus are about 50% to three times better. By adding more nano-silver particles into this TIM, it is believed that its thermal conductivity can be further improved.

Property	Unit	Commercial sample A	Commercial sample B	Nano-TIM with CNT soaked in a conducting liquid	Nano-TIM with silver soaked in a conducting fluid
Thermal conductivity	W/mK	4.0–5.2	4.4–6.5	0.72–4.33	1.02–2.73
Film thickness	μm	1000	500	110	200
Thermal resistance	K/W	0.9–1.2	0.35–0.55	0.66–0.11	0.93–0.35
Operating temperature	°C	50-140	50-140	50-120	40–130
Degradation temperature	°C	400–500	400–500	400	300
Maximum stress during break	%	54.1	30.	15	600
E-module	MPa	0.17	0.75	3.44	0.08
Color		Gray	Gray	Black	Gray

Table 24.1 Properties of nano-TIMs in comparison with commercial materials

In conclusion, nano-TIMs with various nanoparticles have been manufactured using electrospinning. It is found that nanoparticles can improve the heat transfer characteristics of the nano-TIMs. Such improvement depends on the quality and quantity of the nanoparticles. Preliminary mechanical, thermal, and degradation characterization of the nano-TIMs has shown that these materials can potentially offer better mechanical properties with equal or better thermal properties.

24.4 Microchannel Coolers Based on Carbon Nanotubes

The challenge of developing high-performance and low-complexity cooling solutions for microelectronic systems is becoming a key factor as the overall power consumption of integrated circuits continuously rises, despite the drop of the supply voltage. Many investigations about microchannels have been undertaken in the past several decades, showing that extremely high rates of heat transfer can be obtained by applying microchannel structures [17]. Carbon nanotubes (CNTs), a new form of carbon which can be described as rolled layers of graphite with 1–100 nm diameter [18], are a very ideal choice to make this kind of microchannel cooler due to many reasons. Firstly, well-structured CNTs are believed to have very high thermal conductivity based on theoretical predictions, although the experimental results vary dramatically in different references [19–21] for both single-walled and multiwalled nanotubes (SWNTs and MWNTs). If the unusually high thermal conductivity of CNTs can be achieved by a suitable synthesis processes, the efficiency of the fins can be maximized; thus, the total heat removal capability of the cooler can be promoted. Furthermore, CNTs can be grown directly on the surface of silicon and



accurately according to predefined small-scale catalyst patterns normally transferred by standard photolithography processes. Therefore microscale channels can be fabricated, making the cooler very compact and efficient. CNTs also provide a possibility of low-cost bulk production with a potential compatibility with standard CMOS technology [22].

This section briefly introduces the latest research work on using CNTs to build microcoolers [23–25], as well as supporting simulation work [26].

The overall manufacturing procedure of this CNT microcooler is illustrated in Fig. 24.6. The catalyst pattern is firstly transferred to the silicon substrate by photolithography and evaporation and a lift-off process. The catalyst used in this application is iron, and its thickness is roughly 1 nm. By using thermal chemical vapor deposition (TCVD), CNTs are then grown on the catalyst patterns, forming the fins of the microcooler. The growth temperature is about 750 °C. The silicon substrate carrying CNT fins is then bonded with a lid to finish an entire cooler.

Carbon nanotube microcoolers of different patterns and dimensions have been successfully manufactured. Figure 24.7 shows the SEM images of a CNT cooler with 50 μ m wide channels and fins. The height of the fins is roughly 300 μ m. Each fin contains numerous vertically aligned carbon nanotubes bunched together. The overall quality of the coolers is quite acceptable in terms of the uniformity and tube density of the fins.

The measurement was performed by using a power film resistor which can generate up to 30 W power as the heat source. The coolers are mounted on the exposed ceramic heat dissipating surface of the resistor. No heat transfer paste is applied. The coolers are connected to plastic tubes on both ports, and waterproof



Fig. 24.7 SEM images of a carbon nanotube microcooler

tape seals the connections to prevent leakage of water. A micropump which can deliver up to 500 ml/min flow rate provides a continuous, stable, and controllable water flow through the channels of the coolers. The temperature of the resistor is obtained by a thermocouple glued on the heat dissipation surface of the transistor.

A CNT microchannel cooler, a silicon microchannel cooler, and a silicon cooler without fins, which are of similar dimensions, have been tested and compared under the same experimental conditions. The initial measurement results show that the cooling efficiencies of CNT and silicon microchannel coolers are roughly at the same level and much higher than that of the silicon cooler without fins.

Based on the initial experimental configuration, the power transferred from the heat source to the cooler cannot be measured or calculated precisely because an unknown portion of heat is dissipated by natural air convection. There are also some considerable thermal resistances existing between the resistor and the cooler, making accurate calculation more difficult. Therefore, some new coolers with heat resistors directly integrated onto the backside of the cooler have been designed and fabricated. The resistors are made of copper and formed in a serpentine pattern. The thermal resistance between the coolers and heat sources can thus been miniaturized. The new microcoolers are currently under test.

CFD simulation is a powerful tool to assist the study and design of microcoolers. Simulation work has also been done for CNT microchannel coolers to shorten the design cycle and lower the experimental cost.

Two types of fin arrays (1D and 2D nanotube fin arrays, respectively) have been simulated to study the relation between the cooling performance and the fin array structures, dimensions, fluid speed, and thermal conductivity of the fins. The PRC (preconditioned conjugate residual) method in the FLOTRAN CFD program in ANSYS is utilized in this case. A numerical method to solve this conjugate heat transfer problem is to treat the solid and fluid as a unitary computational domain and to solve the governing equations simultaneously. The FLUID141 element in ANSYS is selected to model the present fluid/thermal system with a fluid-solid coupling. Examples of the meshes generated in the CFD simulation of cooling assemblies for 1D and 2D fin arrays (M = 5, N = 5) are shown in Fig. 24.8.



Fig. 24.8 An example of the models and meshes generated in the CFD simulation



Fig. 24.9 An example of CFD simulation results for fins of different thermal conductivity

Simulation results have shown that the thermal conductivity of the fins does have a significant effect on the cooling efficiency of the coolers. One example with five 1D fins shows that the maximum and average temperature of the fin array can be decreased dramatically by increasing the thermal conductivity of the fins (Fig. 24.9).

Another important factor affecting the performance of the microchannel coolers is the speed of the flow. As revealed in an example shown in Fig. 24.10, very high fluid speed must be applied to achieve good cooling performance. And the high fluid speed results in a very large pressure drop, which requires much higher pumping power. To apply high fluid, speeds may also destroy the CNT fins as the nanotubes are basically bound together by weak van der Waals forces. This must be taken into account when designing the microcoolers. One possibility is to coat the CNT fins, which increases the cost and complexity of manufacturing such coolers.



Fig. 24.10 An example of CFD simulation results revealing the effect of fluid speed on the temperature and pressure drop

24.5 High Thermally Conductive Carbon Nanotube Bumps

Another important heat removal path from the chip is through the interconnects to the substrate. CNTs have also been proposed as bumps for flip chip interconnect due to their high thermal conductivity [27]. Besides the thermal conductivity, CNTs also have high mechanical strength [21] and good electrical conductivity for metallic CNTs [28]. Moreover, CNTs can be aligned according to small-scale precisely predefined patterns by common technologies, making bulk production of fine-pitch interconnects possible.

The simplified manufacturing process of patterned CNTs is illustrated in Fig. 24.11. Photolithography is used to transfer the patterns defined in the mask to





the substrate. The catalyst is then deposited onto the substrate by an electron beam evaporator. A lift-off process is performed afterward to remove the resist together with the unwanted catalyst. By using a DC-PECVD system, CNTs are grown on the catalyst patterns, forming the bumps of the chip.

In real applications, it is also necessary to grow CNTs on metal layers. The PECVD growth of carbon nanostructures can differ significantly on different metal layers, and an insertion layer between the metal and catalyst particles can play a crucial role in the process [22]. A SEM picture showing the CNT bumps grown on both silicon and copper is shown in Fig. 24.12.

An important issue regarding using CNTs as flip chip interconnects is the high synthesis temperature of CNTs, typically higher than 650 °C. Such high temperature is not compatible with certain temperature-sensitive processes and materials. Therefore transfer of CNTs by solders [29] and conductive adhesives [30] has been proposed. Figure 24.13 shows some transferred CNT bundles by imprinted isotropic conductive adhesive (ICA). This technology can successfully transfer CNT structures at a low temperatures of 150 °C, enabling the integration of CNTs into processes and materials that cannot withstand the high CNT synthesis temperatures [31].



Fig. 24.12 SEM image of CNT bumps grown on silicon and copper





24.6 Conclusions

Some new developments of applying nanotechnologies and nanomaterials in the field of thermal management of microelectronics packaging have been introduced in this chapter. These applications include nano-thermal interface materials and carbon nanotube-based microcoolers and flip chip bumps. The utilization of various nanotechnologies and nanomaterials may potentially revolutionize the electronics packaging and production industry to solve the needs of miniaturization, ultra-high density packaging, and larger power dissipation.

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Chapter 25 Synthesis and Optical Characterization of CVD Graphene



Chenglung Chung, Yuchun Chen, Yinren Chen, and Yonhua Tzeng

25.1 Introduction

Graphene is a two-dimensional, atomic-scale, sp²-hybridized carbon with unique optical, mechanical, and electric properties; therefore, graphene has attracted a lot of attention for many advanced applications. Physicists tended to believe that two-dimensional atomic structures were unstable in the ambient atmosphere because the thermal disturbance might be adequate to move atoms in a single-atom thick structure to form three-dimensional structures which are more thermodynamically stable. Since monolayer graphene was first exfoliated from highly oriented pyrolytic graphite (HOPG), graphene has been extensively characterized and studied for a wide spectrum of applications.

Graphene is the thinnest and lightest weight solid-state material in the world. The thickness of monolayer graphene is ~0.334 nm. The perfect and symmetrical band structure creates some of its unique physical and chemical properties. At room temperature, graphene has an ultrahigh electron mobility of about 15,000 cm²v⁻¹ s⁻¹ [1]. Carrier mobility in graphene is much higher than that in silicon (~1400 cm²v⁻¹ s⁻¹). The resistivity of graphene is about $10^{-6} \Omega$ -cm, which is lower than those of copper and silver. Also, the optical transmittance of graphene is about 97.7%. With its high mechanical strength and tensile strength, graphene is a good prospect as a flexible transparent electrode for applications such as touch screens.

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25.2 Fabrication of Graphene

There are several ways to produce and synthesize graphene. A.K. Geim et al. from the University of Manchester exfoliated single-layer graphene (SLG) from graphite in 2004 [2]. In their experiment, highly oriented pyrolytic graphite (HOPG) was used as the graphene source. Scotch tape was used to peel off single- or multilayers of graphene from the top of the HOPG. This method is mechanical exfoliation.

Exfoliation is a convenient means of synthesizing single or few-layer graphene films. As Fig. 25.1 shows, many researchers used scotch tape to adhere to the HOPG (highly oriented pyrolytic graphite) and mechanically exfoliated graphene films from the HOPG. This exfoliated graphene has less defects than most of its CVD counterparts [3]. Various chemical and physical means of exfoliating graphene have been developed, but the size of exfoliated graphene is not well-defined. Large-area exfoliated graphene is difficult to obtain. Therefore, many research groups are still devoted to the synthesis of large-area and high-quality graphene using chemical vapor deposition. Nevertheless, exfoliation provides a means of producing tons of graphene flakes, which can be used directly for selected applications or further processed to become customized composite materials for optimized performance for each specific application.

H. Dia et al. demonstrated a novel method of producing high-density graphene, known as the oxidation and reduction method [4]. In their work, graphite was placed inside a strong oxidant solution container and treated by vibration, centrifugation, a cleanup process, and so on. The van der Waals force between the graphene layers decreased sharply during the treatment. The graphite was then dispersed to form graphene nanoplatelets in the solution. The oxidation process then easily converts graphene to graphene oxide (GO). An efficient reducing process is required to then reduce the GO oxide back to graphene. Although this way could easily produce a large amount of graphene, high-quality graphene is not easily obtained using this method because defects of graphene produced by the process are difficult to reduce. Besides, the oxidation and reduction method cannot easily produce a large-area uniform graphene film.

One of the common methods used to synthesize large-area uniform graphene is thermal-chemical vapor deposition (thermal CVD). When this method to fabricate



Fig. 25.1 Schematic diagram of the mechanical exfoliation of graphene



Fig. 25.2 Schematic diagram of a thermal CVD system for graphene

graphene is applied, catalysts such as gold, nickel, and copper are required. Q. K. Yu et al. reported that carbon atoms could be absorbed and then segregated from nickel (Ni) [5]. The catalyst substrate and the process temperature play significant roles. However, high-quality and uniform graphene films were not easily produced by using nickel as a catalyst. In 2009, the Rudoff group demonstrated a method of synthesizing large-area and high-quality single-layer graphene (SLG). In their experiments, copper foils served as a catalyst. Because of the very low carbon solubility in copper at room temperature, the synthesis of SLG on copper is a self-limiting process [6]. Once the copper is covered by graphene, there is no further growth of a second layer of graphene on top of the first because there is no exposed copper catalyst. On the other hand, lateral growth of single-layer graphene on the exposed copper surface continues to form larger and larger SLG domain sizes [7–9]. Zheng Yan et al. controlled the CVD chamber pressure and demonstrated the growth of millimeter-sized single-domain graphene on copper substrates [9]. Figure 25.2 shows a schematic diagram of a thermal CVD apparatus.

D.A. Boyd et al. demonstrated a high-quality graphene film using plasmaenhanced chemical vapor deposition (PECVD) [10]. During the experiment, plasma-induced ions and free radicals both bombarded the target substrate. The growth temperature for graphene using PECVD is lower than that for thermal CVD. In their results, high-quality graphene can be synthesized on copper foils at a low process temperature of ~420 °C in a few minutes. The surface roughness on copper foil using the low-temperature growing process is better than for high-temperature growth processes. An electron carrier mobility of 6.0×10^4 cm²v⁻¹ s⁻¹ at room temperature has been reported.

25.3 Transferring Graphene from the Metal Catalyst to the Target Substrate

In the past decade, most of the CVD processes for high-quality graphene fabrication have still required metal catalysts. Methods for transferring graphene layers from metal catalyst substrates to substrates are needed. Rudoff et al. demonstrated a method of using PMMA to transfer large-area single-layer graphene from a metal catalyst to a target substrate [11]. During their experiment, the PMMA was first spin-coated onto a graphene/copper foil as a passivation layer, and then the sample was placed into FeCl₃ solution to remove the copper foil. After the copper was removed completely through etching, the graphene film was then transferred onto the target substrate. Finally, the PMMA was removed by using organic solvents such as chloroform and acetone. However, with this method, it is possible to contaminate the graphene surface. Therefore, a simple and efficient method for the removal of PMMA or photoresist is required.

Ce'sar J. Lockhart and de la Rosa et al. demonstrated a novel method of using hydrogen bubbles to successfully transfer graphene to a target substrate [12]. In their work, after graphene has been grown on both sides of a copper foil, the graphene on the back side of the copper foil was removed by an oxygen plasma. Afterward, PMMA was spin-coated onto the top side of the graphene/copper foil as a passivation layer, and then a flexible plastic frame was placed on the PMMA/graphene/ copper sample for protection before the sample was processed by wet etching. The plastic frame/PMMA/graphene/copper sample was placed inside a container of 0.25 M NaOH solution. The plastic frame/PMMA/graphene/copper sample was then connected to serve as a negative electrode, while platinum (Pt) was connected as a positive electrode. Because the H₂O electrolysis process generates hydrogen bubbles between graphene and the copper foil, the graphene is separated from the copper foil in a few tens of seconds. Finally, after the PMMA/graphene film was separated completely from the copper foil and transferred to a target substrate, the plastic frame/PMMA was removed by using a solvent solution. The authors also claimed that both optical and electrical characterizations of graphene using the electrochemical bubble separation method are better than those of using traditional wet-etching transfer.

Figure 25.3 shows a schematic diagram of a graphene transfer process, where a copper foil is folded and made into an enclosed structure with an inner surface as the chamber walls and an outer surface. Graphene was synthesized on both the inside and outside surfaces of the copper enclosure. Single-layer or few-layer graphene (FLG) sheets were grown on the outside surface of the copper enclosure. The outer surface is coated with PMMA followed by oxygen plasma etching of the graphene on the chamber walls and wet chemical etching of the copper foil to obtain PMMA-coated graphene, which was grown on the outside surface of the copper enclosure [13–15]. The PMMA/graphene film was transferred onto a silicon substrate, on which there was a 300 nm thick thermal oxide. The PMMA is then washed away using chloroform, acetone, and IPA. After the transfer process, as Fig. 25.4 shows,



Fig. 25.3 Schematic diagram showing a graphene transfer process



Fig. 25.4 Optical images of both single-layer and bilayer CVD graphene on a SiO2/Si substrate

we can clearly observe both single-layer and bilayer graphene on the SiO_2/Si substrate. Because of optical interference, bilayer graphene appears to be darker than single-layer graphene when they are observed by an optical microscope.

In practice, large-area single-layer or multilayer graphene is very fragile, especially during the wet-etching and transferring processes; therefore, a passivation layer is required to protect and support a graphene film during most of the transferring process. W.H. Lin et al. demonstrated a novel polymer-free method that can transfer the graphene film directly from the copper surface to a target substrate [16]. High electrical conductivity and excellent optical transmittance have been reported. The mobility of the polymer-free monolayer graphene fabricated by their method is as high as 63,000 cm² V⁻¹ s⁻¹, which is 50% higher than comparable samples transferred by conventional methods. Graphene films can also be transferred directly onto a variety of soft materials, such as organic and polymeric thin films by using their method.

D.Y. Wang et al. demonstrated a method of transferring residue-free graphene from a copper foil to target substrates [17]. In their work, the top side of the target substrate was first treated by a static electricity gun to generate static electricity. The target substrate was then rolled with the graphene/copper foil. Interaction between the graphene/copper foil and the target substrate was very strong due to the static electricity on the target substrate. Afterward, the copper foil was removed by a copper etchant solution, and the graphene film was stacked on the target substrate. Besides, no polymer passivation layer was used when using their method for transferring graphene. Therefore, the surface of graphene did not appear to have contamination. However, the static electricity is easily affected by air humidity. The efficiency of transferring graphene to another substrate by using their method might not be easy to control.

S. Bae et al. demonstrated a novel roll-to-roll process for transferring graphene from a copper foil to a flexible substrate [18]. In their work, polymer thermal release tape (TRT) was used to stick to the top surface of a graphene/copper foil. The purpose of the TRT is for graphene protection. The sample was then put into a machine with two rolls to enhance the interaction between TRT and the graphene/copper film. Afterward, the sample was placed into a copper etching solution to remove the copper foil and put into a two-roll machine again to stick the graphene film to the target substrate. Finally, the TRT was released from the top of the graphene samples by heating. By using this method, a large-area graphene film can be easily transferred onto various types of flexible substrates.

J. H. Lee et al. demonstrated a method of using a dry transfer process to place graphene on a target substrate [19]. The flat, single-crystalline monolayer graphene was first grown on a silicon wafer covered by a germanium layer. Au was then deposited on top of the graphene/Ge sample to protect the graphene from organic contamination. The polymer TRT was placed onto the Au/graphene/Ge samples. Ge was then separated from the sample by a mechanical method due to the weak interaction between graphene and the underlying hydrogen-terminated germanium surface. Afterward, the TRT/Au/graphene was transferred to the target substrate. Finally, the TRT was removed by heating to 100 °C for 2 min. Au was removed by dipping in Au etchant. By using their transfer process, high-quality graphene can be dry-transferred to a target substrate without using photoresist.

25.4 Transfer-Free Graphene

Most of the graphene transfer processes require wet-etching techniques for metal film etching. However, additional defects and undesirable impurities from contamination are easily created during the wet-etching procedure. Due to charge carrier scattering by defects, the electron mobility of graphene is easily degraded. Therefore, transfer-free methods to directly synthesize high-quality graphene on substrates have been reported in recent years. A. Ismachy et al. reported a transfer-free method to directly fabricate CVD graphene on quartz [20]. In their work, the copper film was first sputtered on a quartz substrate as catalyst. Graphene films were first synthesized on both sides of a copper film. After the copper evaporated completely, graphene was deposited directly onto quartz. However, the copper evaporation rate was not easily controlled, so copper residue was easily left on the substrate.

L.J. Li et al. demonstrated a method of using thermal CVD to grow graphene on a copper/SiO₂ substrate [21]. In their work, copper was first deposited on SiO₂ using sputtering to a thickness of a few hundred nanometers. Because carbon atoms diffuse through copper to the interface between copper and SiO₂ substrate, the graphene film not only grew on the top side of the copper film but also formed a graphene film between the copper and the underlying SiO₂ substrate. Afterward, the top-layer graphene was left on the SiO₂ substrate. By using their method, it is possible to synthesize SLG directly on a dielectric substrate in one step without a graphene transfer processes.

H. Kim et al. demonstrated a novel method of using a copper-vapor-assisted CVD process to synthesize transfer-free graphene on a substrate [22]. In their work, a piece of copper foil was suspended above the SiO₂ substrate without physical contact and then placed inside the thermal CVD furnace tube. During the process, due to the catalytic activation of copper vapor at high temperature, methane was decomposed to carbon atoms, and graphene was directly synthesized on the SiO₂ substrate. However, the copper vapor was not easily controlled during the experiment. Thus, the quality of graphene is not easily controlled. Although SLG can be directly synthesized on a dielectric substrate without transfer steps, Raman spectra show that the D-band signal strength was strong.

25.5 Characterization of CVD Graphene

In the past decade, various synthesis methods have been demonstrated and reported for the growth of high-quality graphene. Chemical vapor deposition (CVD) is one of the methods that can produce large-area, high-quality, and low-cost graphene films. By tuning the gas mixture, pressure, and temperature in the deposition chamber, the number of graphene layers can be controlled. So far, the only way to produce uniform, large-area, and high-quality graphene is using CVD techniques, with copper being the most common metallic material as catalyst for graphene synthesis. After the graphene has been synthesized on copper by CVD, graphene can be transferred to an arbitrary substrate. Besides, the quality of graphene can be assessed and identified through Raman spectroscopy, transmission electron microscopy (TEM), and so on.

Zhou et al. reported a method of depositing Ag thin films on exfoliated graphene to distinguish the quality of graphene [23]. The strong defect signal of graphene films was magnified due to the surface-enhanced Raman scattering (SERS) effect.

The quality of graphene can be distinguished by Raman spectra with a D-band signal (~1359 cm⁻¹) being commonly attributed to graphene defects. Dallas et al. also reported a method of depositing Ag thin film on SLG grown by CVD to distinguish the quality of graphene [24]. In their report, the signal of Raman spectra between 900 and 1600 cm⁻¹ can be enhanced through SERS effects.

Various methods have been reported to evaluate the quality of CVD graphene. However, those methods cannot easily distinguish the quality of large-area graphene. Here we demonstrate a simple, quick, and effective method based on wavelength-dependent optical reflection from a graphene-covered copper surface under illumination by the light of a fluorescent lamp. The graphene-covered copper is examined by optical reflection spectroscopy, either at ambient temperature or after having been heated in ambient air to accelerate oxygen diffusion through defects in the graphene and the subsequent oxidation of the copper underneath at a preset temperature for a desirable time period.

Perfect graphene is an excellent diffusion barrier for gases including oxygen. Therefore, perfect graphene grown on a copper substrate will be able to prevent the oxidation of copper in ambient air even for a long shelf time. Copper oxide formed by oxidation varies the reflectivity of visible light. The extent of oxidation of copper is used to tell high-quality graphene from poor-quality graphene grown on copper. For poor-quality graphene, after having been tarnished in ambient air, it can be discerned by the naked eye based on the color change [25]. For near equally good-quality graphene, the difference is small and difficult to be observed by the naked eye. We report the use of optical reflection spectroscopy to differentiate high-quality graphene from graphene of slightly poorer quality by measuring the extent to which graphene-covered copper is tarnished. This can be done at the ambient temperature after the samples have been exposed to the ambient air for a short period of time.

For high-quality graphene, oxidation of underlying copper in ambient air is too slow to be observed within a short period of time after the graphene is synthesized. Heating the sample to a proper temperature to accelerate the oxidation in air can be carried out. The heating process keeps the high-quality graphene from being damaged. Graphene of slightly poorer quality allows underlying copper to be oxidized to a sufficient extent and displayed by the wavelength-dependent optical reflectivity. Perfect graphene, or graphene with very few defects, can effectively block ambient oxygen from diffusing through the graphene to oxidize the copper underneath when the graphene-covered copper is subjected to heating below a threshold temperature for a shorter period of time than what takes to cause permanent damages by oxidation of the graphene [26]. This process thus allows rapid classification of manufactured graphene on copper to differentiate graphene of acceptable quality from that of poor quality without resorting to expensive and time-consuming advanced examination such as SEM, Raman scattering, etc.

Figure 25.5 shows Raman spectra for two graphene samples on copper which have been exposed to the ambient air at room temperature for 3 months. Both spectra show the full width at half maximum (FWHM) value of the Raman 2D-band being 35 cm^{-1} and the ratio of signal intensity of the 2D-band to that of the G-band being greater than one. The Raman spectrometer used for the experiments was not of a high



Fig. 25.5 Raman spectra excited by a green laser and measured from a relatively (a) "excellent" sample and a (b) "good" sample of CVD graphene grown on copper

resolution. Therefore, these spectra are used only as a comparison. Sample #2 has a higher D-band signal intensity than that of sample #1. Based on Raman spectra, sample #1 is of excellent quality, and sample #2 is of lower but reasonably good quality. Because the sample surface is not perfectly smooth and uniform, the reflection changes to some extent from spot to spot. Optical spectra measured from sample #1 and sample #2 are shown in Fig. 25.6a, b, respectively, for reflection of incident light from a fluorescence lamp. The two wavelengths which changed the most after being reflected from oxidized copper are in the green and purple color ranges.

For both the "excellent" and the "reasonably good" samples, Raman scattering shows sharp peaks of the G-band, without any D-band or with only a small D-band signal, indicating that the graphene is of excellent and reasonably good quality. It should be noted that micro-Raman scattering only measures the quality of graphene at the focused point of laser illumination. It does not show the effects of abundant defects in graphene and the domain boundaries located between different areas on graphene.

Sample surfaces are not perfectly smooth, and the light intensity is not measured at exactly the same location and the same direction for these two samples. The relative extent of the change in intensity between the reflected light and the incident light at those two wavelengths are shown in Fig. 25.6c for an "excellent" sample (#1) and a "reasonably good" sample (#2) in comparison with the incident light. The good sample #1 exhibits nearly equal ratios of reflected to incident light intensity for the green (546 nm) and the blue-purple (436 nm) color. It shows that the absorption of the incident light by the "excellent" graphene-covered copper is relatively independent of the wavelength of the incident light, i.e., the copper underneath has not been oxidized to a sufficient extent to affect the reflection of light.

By contrast, the "reasonably good" sample #2 exhibits stronger absorption of the blue-purple light than of the green light. This optical reflection response is similar to that of oxidized copper, which absorbs short-wavelength light more than long-wavelength light. Although both samples exhibit similar Raman spectra, the optical



Fig. 25.6 Optical spectra of reflected light (**a**) from sample #1 and (**b**) from sample #2. (**c**) Ratio of the intensity of light reflected from graphene-covered copper to the incident light measured at two wavelengths. Sample #1 is superior to sample #2 in quality



Fig. 25.7 Optical micrograph of (a) sample #1 and (b) sample #2

microscope images shown in Fig. 25.7a for sample #1 and Fig. 25.7b for sample #2 show that after exposing the graphene-covered copper in ambient air for 3 months, the "excellent" graphene indeed retained the capability of blocking ambient oxygen from oxidizing the copper beneath the graphene. For graphene film defects,

including incompletely merged domain boundaries or small unfilled holes, penetration of oxygen through those defects caused the copper beneath to be oxidized after being exposed to ambient air at room temperature for 3 months.

A simple and rapid means of differentiating high-quality graphene grown on copper from those of poorer quality has been demonstrated. High-quality graphene can protect copper from oxidation in ambient air at room temperature for a long period of time. Nevertheless, reasonably good-quality graphene based on Raman scattering evaluation still loses its diffusion barrier capability for oxygen after prolonged exposure to ambient air for 3 months. Oxidation of copper due to defects in graphene can be applied to categorize graphene grown on copper into different levels of quality by heating in ambient air up to 200 °C for a few minutes. Heating to temperatures lower than 200 °C can also be done, but it takes a longer period of time because it reduces the extent of oxidation damages to the graphene. The optical reflection spectroscopic results have been correlated to optical micrographs and Raman spectra of different samples to demonstrate the effectiveness of the reported method of rapid and inexpensive evaluation of the quality of mass-produced graphene on copper.

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Chapter 26 Characterization of Electronic, Electrical, Optical, and Mechanical Properties of Graphene



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26.1 Introduction

In accordance with Moore's law, the number of transistors in an integrated circuit (IC) doubles every 2 years, while the transistor price and size continue to decrease. The interconnect between transistors in an IC also becomes smaller and more difficult to fabricate. Tiny copper interconnects cause serious degradation in circuit performance due to increased RC delay times and failure to conduct properly due to electromigration. Carbon nanotubes, graphene, and related nanomaterials have been studied and have made rapid progresses in the last decade. Graphene and its derivatives have especially emerged as promising enabling materials for a wide spectrum of future applications.

Graphene is a two-dimensional material which is composed of a hexagonal honeycomb lattice of carbon atoms in a single atomic layer. It has many extraordinary properties applicable to real-world applications and even more still requiring further research and improvement before practical applications can be realized.

The electronic energy band structure of graphene and its characteristics have been investigated and predicted theoretically since 1947 by Wallace [1]. In 2004, Novoselov and Geim successfully demonstrated both few-layer and single-layer graphene nanosheets by mechanical exfoliation techniques. After that, many excellent and outstanding properties of graphene have been measured and demonstrated by reproducible and verifiable experiments [2].

Graphene has much higher electrical and thermal conductivities and a higher charge carrier mobility than commonly used semiconductors such as silicon and is therefore suitable for a wide range of electronics applications. Monolayer graphene

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conducts electricity by holes, electrons, or both which can move ballistically at speeds 100 times higher than charge carriers in common semiconductor materials at room temperature. Low electrical resistivity, high electromigration resistance, high thermal conductivity, and outstanding mechanical strength make it a promising candidate to replace copper and other conventional materials in realizing nano-interconnects. Atomically thin graphene is optically transparent to a wide spectrum of wavelengths. Moreover, graphene is an excellent diffusion barrier, desirable for many applications [3]. In this chapter, characterization of graphene's electronic, electrical, optical, and mechanical properties will be described and discussed.

26.2 Bandgap Engineering of Graphene

26.2.1 Zero Bandgap Energy of Monolayer Graphene and Methods of Opening Up the Bandgap

Graphene's conduction and valence bands meet at Dirac points, and hence it is a semimetallic material or a zero-gap semiconductor. As Fig. 26.1 shows, pristine monolayer graphene has zero bandgap energy. Unlike common semiconductors, in which only electrons with high enough energy can cross an energy barrier to become a free charge carrier for conducting electricity, the energy barrier is zero for graphene. However, transistors made of monolayer graphene with zero-energy bandgap and ballistic carrier transport are difficult to be switched from the conductive stage (on) to the nonconductive stage (off). For digital circuits, it is desirable for



Fig. 26.1 The electronic band diagram of graphene. The six points where the conduction band and valence band meet are called Dirac points. The two sets of Dirac points are labeled K and K' [3]

a transistor to conduct as little current as possible when it is in the off state in order to reduce power consumption. Opening up the energy bandgap is therefore an important goal of many research groups. For analog circuits, the high-speed electron transport is desirable for high-frequency applications while the zero energy bandgap is of less concerns.

In order to overcome the zero bandgap issue of graphene, a number of research groups have investigated methods for creating non-zero bandgap graphene. Several types of dopants have also been introduced into graphene to reduce its resistivity and make it more promising for practical applications.

26.2.2 Surface Modification and Doping of Graphene

Adsorption and termination by various foreign atoms or molecules on graphene surfaces or substituting carbon atoms in graphene with dopants such as H, P, Si, Se, O, W, etc. by chemical and physical means have been investigated in order to tailor the chemical reactivity, electrical conductivity, and a variety of properties of graphene [4–7]. For example, hydrogen-terminated graphene has been investigated for spintronics, electronics [8, 9], and surface-enhanced Raman spectroscopy (SERS) applications [10]. When graphene is fully terminated by hydrogen [11– 13], an electrically conductive monolayer of graphene is converted into electrically insulating graphane, which has a direct bandgap of $E_g = 3.5$ eV for the chair form and $E_g = 3.7$ eV for the boat form. In the chair-like conformer, the hydrogen atoms are alternatively attached to the carbon atoms on both sides of the sheet, whereas in the boat-like conformer, the carbon-bonded hydrogen atoms are alternatively attached in pairs on both sides of the sheet. Both chair-like conformation and boatlike conformation of graphene have been predicted to be promising candidates for semiconductor applications. The calculated graphane C-C bond length of 1.52 Å is similar to the sp³ bond length of 1.53 Å in a diamond crystal and is much greater than the 1.42 Å characteristic of sp^2 carbon bonds in graphene. Graphene has a 2D flat planar structure, whereas graphane has an extended 2D covalently bonded structure [14].

Graphene with tunable resistance by hydrogen termination has been demonstrated by exposing graphene to a remote microwave plasma at room temperature as shown in Fig. 26.2a [15]. After having been exposed to remote plasma species for 10 min, the graphene sample was measured for its resistance. As shown in Fig. 26.2b, the resistivity of graphene increased with the hydrogen plasma treatment time. Surface treatment of graphene by hydrogenation provides an increase in the electrical resistivity of graphene for practical electrical and electronic applications.

A novel phosphorus-doped graphene field-effect transistor (GFET) has been developed as a next-generation electronic device [16]. An inductively coupled plasma (ICP) and triphenylphosphine (TPP) were applied for substitutional doping of graphene with phosphorus. Chemical bonding between phosphorus and carbon is clearly shown by XPS spectra of phosphorus-doped graphene. The transfer



Fig. 26.2 (a) Schematic diagram showing the remote hydrogenation plasma; (b) electrical resistance of a single-layer graphene as a function of exposure time to a remote hydrogen plasma

characteristics of a phosphorus-doped graphene field-effect transistor exhibit a Dirac point voltage (VDirac) around 54 V. Moreover, excellent multifunctional applications of phosphorus-doped graphene for oxygen reduction reactions and lithium ion batteries have been demonstrated by using graphene oxide (GO) and triphenylphosphine as carbon and phosphorus sources, respectively [17].

Substitutional doping of graphene with boron or nitrogen atoms creates a bandgap and makes graphene a p-type or n-type semiconductor material suitable for charge storage, charge transfer, and many promising applications [18–22]. Kim et al. [23] demonstrated a method of producing single-layer graphene with substitutional boron doping by mechanically exfoliating graphene from boron-doped graphite. Boron atoms are spaced apart by 4.76 nm in single-layer graphene according to measurements by Raman spectroscopy. The amount of substitutional boron atoms in the graphite crystal was ~0.22% of carbon atoms, which was measured by X-ray photoelectron spectroscopy. Besides, Panchakarla et al. [24] demonstrated borondoped graphene by using an arc discharge technique. To produce the boron-doped graphene samples, boron-stuffed graphite electrodes yield boron-doped graphene of two to four layers in a gas mixture of hydrogen, helium, and diborane (B_2H_6) of a DC arc discharge. The boron-doped graphene exhibits p-type semiconductor behavior with promising properties for VLSI circuit applications. Wang et al. [25] demonstrated a scalable and tunable boron-doped graphene by using thermal exfoliation of graphene oxide in the presence of BF3 at different elevated temperatures. Different amounts of boron atoms can be introduced into the carbon lattice by tuning the composition of the gaseous atmosphere at different temperatures. However, the achieved doping level with boron was only between 23 and 590 ppm.

Substitutional doped nitrogen in graphene serves as an excellent electron donor to create an n-type semiconductor suitable for electronic applications. Nitrogen-doped graphene also has optical, magnetic, and a variety of outstanding properties which are desirable for biological [26], supercapacitor [27–29], and energy storage applications [30–32]. Li et al. [33] reported a novel method of producing nitrogen-doped

graphene by thermal annealing of graphene oxide (GO) in ammonia at temperatures ranging from 300 to 1100 °C. The highest doping level of about 5% nitrogen was achieved at 500 °C. Besides, graphene oxide annealed in NH_3 exhibits higher electrical conductivity than those annealed in H_2 atmospheres.

Chemical vapor deposition (CVD) is a promising method of producing largescale nitrogen-doped graphene. For instance, Wei et al. [34] demonstrated doped graphene with a doping level of ~9% nitrogen by means of a CVD process. Copper films on silicon serve as the catalyst in a mixture of hydrogen, methane, argon, and ammonia at a temperature of about 800°. Furthermore, doped graphene with a doping level of 2.4% nitrogen can be synthesized by using a nitrogen plasma under various conditions [35]. Mou et al. [36] demonstrated a method by heating graphene oxide with melamine or urea as the nitrogen source at different temperatures ranging from 200 to 700 °C to produce nitrogen-doped graphene.

As previously reported, single-layer graphene exhibits very high carrier mobility up to $15,000-200,000 \text{ cm}^2 \text{V}^{-1} \text{ s}^{-1} [37-39]$, which is superior to silicon by more than ten times. However, pristine graphene is known to have a zero bandgap and is not suitable for field-effect transistors for digital circuit applications.

Beidou Guo et al. demonstrated a graphene field-effect transistor based on nitrogen-doped graphene. The N-doped graphene was obtained by ammonia (NH₃) annealing after N⁺-ion irradiation of graphene and achieved electron and hole mobilities of ~6000 cm² V⁻¹ s⁻¹ [40]. Boron-doped graphene has also been demonstrated with a stable p-type behavior and carrier mobility of ~800 cm² V⁻¹ s⁻¹ at room temperature [41]. From recent reports, the carrier mobility of boron-doped graphene is lower than that of nitrogen-doped graphene. Tianru Wu et al. demonstrated B- and N-doped graphene-based back-gate FETs by chemical vapor deposition using polystyrene, urea, and boric acid. The mobility of B- and N-doped graphene is 350–550 cm² V⁻¹ s⁻¹ and 450–650 cm² V⁻¹ s⁻¹, respectively [42].

The capability for substitutional doping of graphene with different dopants is expected to significantly promote further development of graphene-based electronic, biomedical devices and many applications. Additional methods shown in Tables 26.1 and 26.2 have been employed to dope graphene with boron (Table 26.1) and nitrogen (Table 26.2).

26.2.3 Stacked Graphene

Recently, stacked layers of graphene, including bilayer and few-layer graphene structures, have attracted significant attention due to their special crystalline structures and unique properties in dependence of the twisted angle between adjacent graphene layers. For example, the bandgap of bilayer graphene is tunable by an externally applied vertical electrical field. Stacked multilayer graphene can be synthesized directly or formed by transferring one single-layer graphene at a time for multiple times on a substrate. Controlled alignment angle between consecutive layers of graphene can be achieved. Different interaction modes between two layers

Method of synthesis	Process parameters	B content (at.%)	Applications	Ref.
CVD	Cu as catalyst, B as powder, and ethanol as precursor, 950 °C, 10 min	0.5	Solar cells	[43]
CVD	Triethylborane, graphene on Ni substrate	-	-	[44]
CVD	A gaseous mixture of CH ₄ /H ₂ /B ₂ H ₆ , 1000 °C, polycrystalline, Cu foil	2.5	Electronic device	[45]
Arc discharge	A gaseous mixture of H/He/B ₂ H ₆	1–3	Electronic	[24]
	Arc discharge of boron-stuffed graphite electrode		applications	
Thermal	Graphite heated in H_3BO_3 , at 2540 °C for exfoliated graphene	0.22	-	[23]
Thermal	Graphene oxide (GO) and B ₂ O ₃ , 1200 °C, 10 min	~3.2	Electrochemical applications	[46]
Solvothermal	GO in tetrahydrofuran, ammonia borane, 3 h reflux	-	Supercapacitor	[47]
Thermal	GO and H_3BO_3 in a mixture of Ar/H ₂ , 1100 °C	1.7	Optical applications	[48]

 Table 26.1
 Methods of synthesizing boron-doped graphene

 Table 26.2
 Synthesis of nitrogen-doped graphene

		N		
Method of		content		
synthesis	Process parameters	(at.%)	Applications	Ref.
CVD	25 μm copper foil as catalyst, a mixture of H ₂ /Ar/CH ₄ /NH ₃ gas, at 850–980 °C	2.1–5.6	Graphene SERs	[<mark>49</mark>]
CVD	Nickel film on SiO ₂ /Si substrate, a mixture of NH ₃ /CH ₄ /H ₂ /Ar gas, at 1000 °C	4	Fuel cells	[<mark>50</mark>]
PE-CVD	25 μm copper foil as catalyst, a mixture of $H_2/CH_4/N_2$ gas, at 950 °C	0.5–1	-	[51]
Arc discharge	Arc discharge of graphite in NH ₃	1.2	Electronic applications	[24]
Thermal	Graphene oxide, a mixture of NH ₃ /Ar gas, GO annealed at higher temperatures $(\geq 900 \ ^{\circ}C)$	3–5	-	[33]
Thermal	Graphene oxide (GO) in NH ₃ , 300–800 °C	6–11	Electrocatalytic applications	[52]
XMicrowave treatment	Graphene oxide (GO), urea, 900 W, 30 s	13–15	Supercapacitor	[<mark>19</mark>]
Ball milling	Pristine graphite in NH ₃	4.49	Solar cells	[53]
		14.84	Fuel cells	[54]

of graphene which are stacked with different alignment angles result in varied properties of multilayer graphene.

To make different applications of bilayer or few-layer graphene possible, various production methods for high-quality multilayer graphene have been developed. For



Fig. 26.3 (a) Optical image of the top view of a back-gate FET. The scale bar is 2 μ m. (b) Transfer characteristics of a bilayer graphene back-gate FET device

example, mechanical exfoliation [2], epitaxial growth [55], and chemical vapor deposition of hydrocarbons on transition metals [56, 57] were demonstrated for producing bilayer graphene with the same stacking order as consecutive graphene layers in a graphite crystal. A commonly used thermal CVD method was also applied for the synthesis of bilayer and tri-layer graphene in our research laboratory. The CVD bilayer graphene is characterized and used for the fabrication of dual-gate FETs with a self-aligned top gate on silicon substrates using native aluminum oxide as the gate dielectric and the spacers for insulation between the gate and the source and drain.

To characterize the electrical properties of CVD bilayer graphene, electrical transport measurements were carried out using the back-gate FET in the ambient atmosphere. Electron beam lithography was applied for the fabrication of the back gate for bilayer graphene FETs. First of all, a bilayer graphene film was transferred onto a Si substrate on which e-beam-patterned alignment marks had been made. Then, the graphene channel was patterned by oxygen plasma etching in combination with e-beam lithography. The e-beam lithography was then used to pattern source/drain electrodes. Source/drain contacts were deposited using thermal evaporation (Au 50 nm/Pd 10 nm) followed by a lift-off process.

Figure 26.3a shows an optical micrograph of a back-gate FET. Figure 26.3b shows transfer characteristics of the bilayer graphene device. In particular, transfer characteristics of the bilayer graphene FET show that the Dirac point was shifted in the positive V_{BG} direction due to the doping effects by humid air in the ambient atmosphere [58–60].

26.2.4 Optical Properties of Graphene Materials

In 2012, Tzeng et al. reported controlled nucleation and growth of snowflake-like graphene on Cu foils by competitive growth and etching in hydrogen-diluted

methane [61]. In 2013, Wu et al. also reported the growth of snowflake-like graphene on liquid copper with the graphene morphology controlled by the ratio of inert gas to hydrogen [62]. Besides CVD nucleation and growth of graphene of special patterns, by the use of a proper Ar/H_2 gas ratio, it was demonstrated that monolayer graphene film can be etched to obtain graphene patterns of sixfold symmetry without needing any etch mask [63].

Due to the undesirable zero bandgap of single-layer graphene for some applications, Bernal-stacked, i.e., the same atomic alignment for two consecutive graphene planes in graphite, bilayer graphene, and rhombohedral-stacked tri-layer graphene, have been studied. Methods of preparing stacked graphene with special stacking alignments and sequences offer a new route to opening the graphene bandgap. For example, a perpendicular electrical field can modify the bandgap of Bernal-stacked bilayer graphene. Birong Luo et al. reported that different hierarchical graphene architectures could be produced with their unique electrical properties measured quantitatively. They also used equivalent circuits to explain the transport properties [64].

For optoelectronic and electronic applications, pristine single-layer graphene suffers from low on/off transistor current ratio, gain, and photoresponsivity due to its being a semimetal. Therefore, intensive research efforts have been made on heterostructures between graphene and other semiconductor materials. Charge transfer phenomena can be observed from the I–V transport property of a graphene channel. For example, P-doped graphene exhibiting transfer of holes from a harvesting material to a graphene channel causes the Dirac point to shift from the left- to the right-hand side of a I–V curve.

In recent years, a variety of absorbed materials on graphene channel have been investigated. Yuanda Liu et al. combined single-wall carbon nanotubes with highquality graphene to achieve broadband (400-1550 nm), high photoconductive gain (105), and high gain-bandwidth product $(1 \times 10^9 \text{ Hz})$ [65]. Graphene can be considered as the primary conductive path providing an excellent signal-to-noise ratio, high carrier mobility, and fast response. Pilgyu Kang et al. prepared crumpled graphene on strong bonding tape [66]. Dramatically enhanced optical extinction (1250%) was achieved by a textured surface of graphene. The stretching capability of this flexible graphene device could be 200% of its original length. They also demonstrated strain-tunable wavelength selectivity with an integrated colloidal photonic crystal. In some special situations, optoelectronic devices respond to some special wavelengths of illumination. Vinh Quang Dang et al. used zinc oxide nanorods to decorate graphene and form a hybrid UV photodetector with high photoconductive gain (10⁶) and good photoresponsivity $(3 \times 10^5 \text{ AW}^{-1})$ [67]. After illumination, electrons and holes were generated in zinc oxide. Then, electrons shifted from the zinc oxide to the graphene because of a built-in electrical field at the junction. The phenomenon for doping a graphene channel can be observed by I-V measurements. Finally, the surviving holes in the zinc oxide moved to the surface of the nanorods and reacted with oxygen molecules absorbed on the surface.

Youngbin Lee et al. hybridized methylammonium lead halide (perovskite structure) and single-layer graphene. The combined device provided a large photocurrent and an ultrahigh quantum efficiency from the photo-gating effect in the visible wavelength range [68]. By a similar means, Zhenhua Sun et al. added gold nanoparticles to form methylammonium lead halide/graphene/gold nanoparticles with sandwiched structures [69]. Plasmonic coupling effects of gold nanoparticles can penetrate through the atomically thin graphene and enhance the methylammonium lead halide to facilitate light harvesting by a near-field effect. The device offers better performance in the generated photocurrent and response time. Jinshui Miao et al. demonstrated a near-infrared photodetector by a new type of vertically stacked heterojunction of indium arsenide nanowires and graphene [70]. This device had a large on/off current ratio (5×10^2) , which was achieved by reducing the dark current by the formation of a heterojunction barrier. The Schottky barrier height at the interface can be modulated by back-gate biasing. This method can also develop rectification actions for diode applications. Similar rectification behavior has also been investigated in stacked heterojunctions of graphene and zinc oxide nanowires [71]. The gate voltage can modulate the Schottky barrier height due to the variation of the Fermi level of graphene. Golam Haider et al. combined graphene quantum dots with a graphene channel to achieve sensitivity as high as 4.06×10^9 A W⁻¹ under 325 nm UV illumination [72]. They developed graphene quantum dots/graphene structures on flexible substrates [73]. They investigated different electrically polarized substrates to show different photoconductive phenomena. By controlling an applied permanent electrical field to a substrate, the sensitivity was improved and the power range for the photoresponse was broadened. The photoresponse power range for the quantum dots/graphene optoelectronic system limits low power by a defect trap effect and high power by a carrier screening effect. The electric dipole moment induced by the substrate lets the device maintain a better performance in both low and high power ranges.

Although single-layer graphene is only one atom thick, the optical transmittance of such a graphene layer on quartz at 550 nm is $\sim 97.7\%$. The opacity of suspended graphene is defined solely by a parameter that describes coupling between light and relativistic electrons and that is traditionally associated with quantum electrodynamics rather than materials science. Despite being only one atom thick, graphene is found to absorb a significant portion ($\pi a = 2.3\%$) of the incident white light, a consequence of graphene's unique electronic structure. However, it is still transparent and useful for many applications. Besides, single-layer graphene has very high electron mobility and low resistivity [39, 74, 75]. Therefore, graphene is hailed as a potential replacement for indium tin oxide (ITO), for which the world supply of indium is finite. Sukang Bae et al., fabricated a 30 in. flexible touch screen panel by using graphene as a transparent conductive electrode. In their work, a 30 in. largescale graphene layer was grown on a roll of copper foil. Multiple roll-to-roll transfer methods have also been demonstrated. The results showed that large-scale graphenebased touch panels with sheet resistance as low as ~30 Ω /sq at ~90% transparency could be competitive with current commercial transparent electrodes such as ITO [76]. In addition, a transparent single-layer graphene touch sensor which works
under a gentle touch has been studied and reported [77]. By changing the channel conductance, the flexible characteristic of graphene, a touch event and a vertical force can be measured. In their experiments, the graphene touch sensor responds to pressure variations ranging from 1 to 14 kPa, similar to a human's lowest perception.

Graphene oxide (GO) is a promising functional material for optoelectronic applications owing to its broad spectral responses and many outstanding optical properties. Cote et al. coated different amounts of graphene oxide onto quartz substrates by using the Langmuir-Blodgett method, which allows layer-by-layer assembly control for the deposition of graphene oxide. In their results, the transparency of graphene oxide is measured to be 95% with a resistance of 19 MΩ/square [78]. Zhixing Qiao et al. demonstrated that the change in optical transmittance for monolayer graphene oxide (mGO) could be up to 24.8% using an external electrical field [79].

Although graphene has extraordinary optical characteristics for optoelectronic applications, the dilemma is that there is difficulty in achieving a compromise between the required low sheet resistance and the high optical transmittance of graphene because the sheet resistance increases with the increase of optical transmittance of graphene. Junbo Wu et al. demonstrated a transparent conductive anode for organic photovoltaic (OPV) cells based on solution-processed graphene thin films. In their work, the optical transmittance and sheet resistance of the OPV cells ranged from 85% to 95% and 100 to 500 k Ω /sq, respectively. Besides, they also indicated that the short-circuit current and fill factor of the graphene cells are lower than those for the control device using ITO owing to the high resistance of the graphene sheets [80]. Therefore, further optimization of graphene with low resistance and high transmittance is needed for future touch panel applications.

Ultrafast detectors such as GaAs, silicon, and GaN photoconductive sensors have attracted significant attention due to their potential applications in the near-infrared spectral range (690–1080 nm) [81–84]. However, it is really formidable to find a similarly fast detector for longer mid- and far-infrared wavelengths [85].

Graphene has recently emerged as a promising optoelectronic material for ultrabroadband photodetectors owing its gapless band structure and excellent electronic properties [86, 87]. Chang-Hua Liu et al. fabricated an ultra-broadband photodetector based on graphene double-layer heterostructures. The room-temperature photodetection from the visual to the mid-infrared range has been demonstrated. Besides, they reported that the detector exhibited a mid-infrared responsivity of up to 1 AW^{-1} , which can be widely used for many applications [88]. Martin Mittendorff demonstrated an ultrafast device of laser pulses over a broad range of wavelengths from a visual wavelength (780 nm) to a far-infrared wavelength (496 um). The ultrafast device is based on CVD graphene on SiC substrates. In their results, an electrical rise time of ~40 ps and a noise-equivalent power of 100 μ W·Hz^{-1/2} were demonstrated over a spectral range from 800 nm to 500 µm [89]. Cheng et al. also demonstrated a self-powered photodetector with fast photoresponse and wide spectral range from 400 to 1000 nm based on graphene/ZnO/Si triple junctions. The response of the device can be reduced to 100 µs due to the existence of built-in electrical fields across the interfaces [90].



26.2.5 Mechanical Properties of Graphene Materials

Graphene has remarkable mechanical properties with outstanding Young's modulus of ~1 Tpa and ultimate strength of 130 GPa. Because graphene exhibits the highest Young's modulus among all materials in nature, it makes a promising candidate for electrical and mechanical applications which require both excellent electrical and mechanical properties [2, 91, 92]. Lee et al. reported a systematic experimental analysis of elastic properties and strength of pristine free-standing monolayer graphene [93]. In their experiments, the graphene film was transferred to a substrate with an array of circular wells. Mechanical properties of graphene were then measured using an atomic force microscope (AFM) as shown in Fig. 26.4. The result shows that graphene has a Young's modulus of E = 1.0 TPa, third-order elastic stiffness of D = -2.0 TPa, and intrinsic strength of sigma = 130 Gpa for bulk graphite. Besides, this experiment has also established the record showing that graphene is the strongest material in the world.

Hye Jin Park et al. synthesized few-layer graphene (FLG) on Ni-coated substrates using CVD and demonstrated its novel properties. In their experiments, when the pristine polycarbonate film was covered with FLG, Young's modulus improved from 1.37 to 1.85 GPa [94]. A novel, simple, efficient, and low-cost production of SLG and FLG with high yield was demonstrated. Both monolayer and FLG can be produced by mechanical ablation of pencil lead on a harsh glass surface with simultaneous ultrasonic treatment [95]. Griep et al. demonstrated a novel method to enhance graphene properties by using ultrasmooth copper growth substrate. Mechanisms for tailoring physical, electrical, and mechanical properties of graphene at the growth stage have also been reported [96]. Because of the unique mechanical applications have been demonstrated in the past decade.

26.3 Modification of Electronic Properties of Graphene by Confinement of Carrier Transport

Graphene nanoribbons (GNRs) are strips of graphene with ultrasmall width of a few to less than 50 nm. Transport of charge carriers through a GNR is confined by two edges on two sides of the ribbon. The width of a ribbon, therefore, greatly affects the carrier transport and its electrical and electronic properties. Demonstrated outstanding electrical and mechanical properties of GNRs, including bandgap opening by quantum confinement, are promising for future electronic applications.



Many researchers have applied remarkable thermal, mechanical, and electrical properties of graphene for graphene-based transistor and IC interconnects [97]. Mitis Sutaka Fujita and co-authors reported theoretical investigations of GNRs. In their work, the electronic states of graphite ribbons with both zigzag and armchair edges were studied by using tight-binding band calculations. They found that graphite ribbons exhibited striking contrasts in their electronic state depending on the edge [98, 99]. Figure 26.5 shows the structures of (a) armchair and (b) zigzag GNRs. Graphene ribbons with both edge shapes can be made from a graphene sheet. The width of an armchair GNR is classified by the number of hexagonal carbon rings or by the number of dimer lines (N_a) across the ribbons. The width of a zigzag GNR is classified by the number of zigzag edges jointly determine the electronic structure and properties of a GNR.

Electronic properties of graphene nanoribbons functionalized by various elements such as H, O, and B and functional groups have been reported [101]. In this work, various properties of GNRs, including the electrical and magnetic properties, were modified by various elements and functional groups. GNRs are also contenders for post-VLSI interconnect applications. GNR-based interconnects can be classified into two different types including single-layer GNR (SLGNR) and multilayer GNR (MLGNR) interconnects [102]. SLGNRs are less suitable for interconnect applications because of their higher resistance than MLGNRs [103]. Narshiha Reddy et al. reported the power dissipation of MLGNRs using 32 nm technology. The power dissipation capacity was increased by increasing the number of graphene layers, and the cross talk delay was decreased as the number of graphene layers increased [104, 105]. The cross talk effect in single-layer GNR interconnect for 21 nm and 13.4 nm technology nodes was analyzed by keeping the voltage on a victim net to be zero with the aggressor nets switching simultaneously. With increasing GNR width, the cross talk noise increased as well [106, 107]. Furthermore, thermal conductivity is also very important in the development of energy dissipation and thermal management of micro- and submicron-sized devices and interconnects. Thermal conductivity of GNRs with different edge shapes as a function of length, width, and strain has been studied by using a non-equilibrium molecular dynamics method. The thermal conductivity was found to be sensitive to the edge shapes, widths, and strains [108]. GNRs have been demonstrated to be promising for interconnect applications.

26.4 Graphene-Substrate Interactions

Recently, studies of the interface between graphene and various substrates have been made by many researchers, because substrates have charged defects, phonons, and different thermal conductivities, which all affect the electrical and electronic properties of graphene. F. Hibel et al. reported graphene-substrate interactions for graphene grown on 6H-SiC using scanning tunneling microscopy (STM). Interaction between the first carbon plane of the synthesized graphene and the SiC surface is much weaker on the carbon face than on the silicon face of the SiC substrate. Interactions between CVD graphene and copper substrates have also been studied by Raman spectroscopy, X-ray diffraction techniques, and atomic force microscopy (AFM). The specific strain and doping values of graphene were found to be affected by the copper crystal orientation, and not as much by the crystalline quality or the surface topography of copper. It was also found that interactions between graphene and metallic substrates caused an exceptionally narrow 2D-band Raman signal [109]. Nevius et al. reported a novel fabrication method that made semiconducting graphene by epitaxial growth. By an improved growth method, a bandgap of greater than 0.5 eV was produced in the first graphene layer on the SiC (0001) surface [110].

Moreover, the structural and electronic properties of graphene on SiC and diamond substrates modified by various dopants and functional groups have been investigated by computation. The structural and electronic characteristics of both single- and double-layer graphene on H-, OH-, and F-passivated [111] diamond surface have also been reported. For graphene on a hydrogen-terminated diamond surface, change transfer results in n-type doping of graphene and the change transfer and doping of graphene do not occur, while graphene is on F and OH surfaces [111].

Graphene on h-BN exhibits enhanced carrier mobility and reduced doping effects in comparison with graphene on silicon oxide substrates. The carrier mobility in graphene on a SiO₂ substrate is limited by carrier scattering due to substrate roughness [112–115], surface states, impurities, and substrate phonons [116–119]. h-BN is a promising substrate for supporting graphene-based device because of its small phonon scattering cross sections for charge carrier transport in graphene. The h-BN surface is atomically smooth. It is also relatively free of dangling bonds and surface charge traps [120]. Shahriari et al. demonstrated a graphene/(h-BN)/ graphene (G/h-BN/G) sandwiched anode material for lithium ion battery applications and achieved improved electrochemical performance [121].

26.5 Summary

Single-layer graphene and multilayer graphene made of stacked single-layer graphene exhibit various desirable and excellent properties for novel applications. Exfoliation of graphene from graphite by chemical, physical, and thermal means provides means of mass production of graphene flakes of small sizes as raw materials for further processing into application-specific forms of graphene or graphene-based composite materials. Chemical vapor deposition provides means of synthesizing graphene of large domain sizes and large areas as an optically transparent and electrically conductive ultrathin film on application-specific substrates or an interfacial layer of heterogeneously integrated materials, structures, and functional devices. Quantum confinement of carrier transport in properly patterned graphene structures results in unique and excellent properties which are more desirable than those in the as-synthesized graphene films. Characterization and essential electrical, electronic, optical, mechanical, and some other selected properties have been introduced.

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Chapter 27 Graphene Applications in Advanced Thermal Management



Hoda Malekpour and Alexander A. Balandin

27.1 Introduction

In this chapter focusing on graphene laminates [1], reduced graphene oxide films [2], and magnetically functionalized graphene fillers in composite materials [3]. As the size of electronic components decreases, the dissipated power density increases, making heat removal a critical issue for many different applications, e.g., in information, communication, and energy technologies [4–9]. Development of the next generations of integrated circuits (ICs) and ultrafast high-power transistors requires efficient heat removal [6, 7]. Better thermal management technologies are needed for high-power density devices such as gallium nitride (GaN) field-effect transistors (FETs) and GaN light-emitting diodes used in solid-state lighting [10-12]. The clock speed of integrated circuits (ICs) is limited by the temperature of silicon (Si) complementary metal-oxide-semiconductor (CMOS) transistors. A reduction in the temperature rise via better heat removal would allow manufacturers to increase the clock speed. In addition to electronics, the advancement in power generation technologies, e.g., photovoltaic solar cells, also depends on the efficiency of thermal management. Modern solar cells have a light-electricity conversion efficiency of ~15% [13–15], which means that more than 70% of solar energy is lost as heat and has to be dissipated from the cell to prevent performance degradation [15-17].

Since the discovery of the exceptional thermal conduction properties of graphene, there has been significant improvement in the thermal management of electronics. Graphene [18] is known to have extremely high intrinsic thermal conductivity [19, 20]. Despite the similarities of phonon dispersion and crystal lattice inharmonicity, graphene can reveal much higher thermal conductivity than the

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basal planes of graphite. This is attributed to the specifics of the long-wavelength phonon transport in two-dimensional (2D) crystal lattices [20–22]. The first experimental measurement conducted on suspended single-layer graphene reported significantly higher values of thermal conductivity K ~ 3000–5000 W/mK compared to that of bulk graphite, with a room temperature value of K ~ 2000 W/mK [20]. The mean free path (MFP) of the long-wavelength phonons is limited by graphene's flake size despite the diffusive nature of thermal transport. This means that unlike in 3D structures, Umklapp scattering is not sufficient for restoration of thermal equilibrium in 2D lattices. This fact is responsible for the dependence of thermal conductivity of few-layer graphene (FLG) on the number of atomic planes [21]. The size-limited thermal conductivity of graphene flake converges to its intrinsic value, as the flake size increases [22, 23].

The exceptional heat conduction properties of graphene along with its excellent mechanical properties inspired researchers to use graphene and its derivatives as a filler material in composites for electronic cooling applications [24-28]. For such applications, graphene is usually produced using liquid-phase exfoliation (LPE). This method is cost-effective for mass production of graphene - a requirement for practical thermal applications. It was reported that LPE-produced graphene and FLG can be used as fillers in thermal interface materials (TIMs) [24, 25] and in thermal phase change materials (PCMs) [29]. Graphene is considered to be a more promising filler than carbon nanotubes (CNTs) owing to LPE graphene's lower cost and graphene's better coupling to matrix material. Significant increase of the thermal conductivity of composites was achieved at low loading fractions of graphene: $\sim 10\%$ in TIMs [24] and $\sim 20\%$ in PCMs [29]. A different type of graphene material that can be used for cooling applications is graphene laminate (GL) [30]. This material is made of closely packed graphene and FLG flakes derived chemically and can be applied as coating material to increase the thermal conductivity of an arbitrary substrate.

For thermal management of modern electronics, the anisotropy of thermal conductivity can also come into importance. In such cases, films with large anisotropy factors (i.e., highly conducting heat in one direction while blocking it in perpendicular direction) are desired [6]. The function of thermal pads with this property is to dissipate heat away from the hot spots in the in-plane direction while preserving electronic components beneath them from heating. High-quality bulk graphite is also well known for its anisotropic factor, ~100, having a high thermal conductivity along its basal plane, ~2000 W/mK, and much smaller values across the planes, ~20 W/mK [31, 32]. However, unprocessed graphite does not meet the industrial requirements for practical applications. Therefore, there is motivation to synthesize new materials with high anisotropy factors. In this chapter, we will describe recent developments pertinent to graphene applications in thermal management focusing on GL [1], reduced graphene oxide films [2], and magnetically functionalized graphene fillers [3].

27.2 Graphene Laminate as a Conductive Coating for Plastic

Due to the large use of plastic in electronic packaging, there is a strong practical motivation in thermally conductive coatings for various plastic materials. While being robust, lightweight, and easy-to-work with materials, plastics suffer from very low values of thermal conductivity. In this section, we describe thermal properties of GL films following research data reported by us in [1]. Graphene laminate is a type of graphene-based material that can be conveniently utilized in coating applications [30]. Graphene and FLG flakes in GL layers, which are chemically derived, are closely packed in overlapping structure. It is common to deposit ("spray on") GL films on polyethylene terephthalate (PET) substrates. Due to PET's extremely low thermal conductivity, ranging from 0.15 to 0.24 W/mK at room temperature, its applications have certain limits. Coating PET with graphene laminate can lead to new application domains.

Graphene laminate consists of overlapping graphene and FLG flakes. Due to the random nature of the graphene flakes' overlapping regions, a large distribution of the flake sizes and thicknesses, as well as presence of defects and disorder, the physics of heat conduction in such materials is nontrivial. Having the knowledge of thermal properties of GL layers and understanding material parameters that limit heat propagation facilitate optimizing GL thermal coatings for practical applications. In [1], the authors investigated the thermal conductivity of GL-on-PET on a set of as-deposited and compressed samples with different mass densities and GL thickness ranging from ~9 to 44 μ m. In the following, we will review the sample structure followed by the outline of thermal measurements and experimental results. At the end of the section, we will outline the theory of heat conduction in FLG used by authors to assist in the theoretical data analysis.

27.2.1 Preparation of Graphene Laminate on PET Substrates

In the reported study [1], GL layers were derived chemically and deposited on PET substrates. For this purpose, an aqueous dispersion of graphene nano-flakes was used as the coating ink. The dispersion of graphene flakes is assisted by the presence of surfactants for deposition of a homogenous film. A conventional PET film was used as a substrate. The PET is a plastic material widely used in various containers. First, the substrate is coated by graphene ink using a laboratory slit coater. The coated substrate is then dried at low temperature to form GL-on-PET samples. Some of the samples were roll compressed, and thus the samples were denoted "uncompressed" and "compressed." The samples were then analyzed to better understand the characteristics of the laminate. Figure 27.1 shows top view SEM micrographs of both uncompressed and compressed GL-on-PET. One should notice that the laminate is made of overlapping single-layer graphene and FLG flakes with different sizes and



Fig. 27.1 Top view SEM images of as-deposited (a, b) and compressed (c, d) samples of GL-on-PET. Graphene laminate is made of graphene and few-layer graphene with different sizes, arbitrary shapes, and random in-plane orientation, coupling each other in an overlapping structure. The number of misaligned vertical flakes, bright white areas, decreases after compression

shapes. The cross-sectional SEM of the GL-on-PET is also shown in Fig. 27.2 with the GL layer distinguished. The cross-sectional SEM is used to determine the thickness of laminate ranging from ~9 to 44 μ m. An average value among several locations was used for this analysis due to the thickness nonuniformity. Moreover, the sheet resistance of the graphene laminate was measured by the 4-point probe technique and found to be within the 1.8–6.1 Ω/Υ interval. The mass density of GL layers was found to vary from 1.0 to 1.9 g/cm³. Table 27.1 summarizes some of the GL properties used for this study.

Aside from GL characterization, an accurate statistical analysis has been done on the laminate flake size for further quantitative analysis of thermal properties. As confirmed by SEM (Fig. 27.1), the GL is made of overlapping single-layer graphene and FLG flakes with different sizes and shapes. For statistical analysis, extensive top view SEM studies have been performed to determine an average flake size *D* of a large number of flakes. The average flake size is defined as an average of three diameters of each flake. To achieve sufficient accuracy for statistical calculation of D, more than hundred flakes have been taken into consideration for each sample. It has been noticed that after almost ~50 flakes are included in the analysis the average size saturates to a particular well-defined value [1]. All the values of average flake size have been provided in Table 27.1.



Fig. 27.2 Cross-sectional SEM images on GL-on-PET for as-deposited (a, b) and compressed (c, d) samples. Two white arrows are used to indicate the GL thickness (c). Large thickness variations are clearly observed in SEM micrographs. (Reproduced from Malekpour et al. [1] with permission from American Chemical Society)

GL-on-PET	Laminate thickness [µm]	Average flake size [µm]	K [W/mK]	Note
1	44	1.10	40 ± 7.5	Uncompressed
2	14	1.15	59 ± 3.6	Uncompressed
3	13	1.24	75.5 ± 11.3	Uncompressed
4	9	1.18	90 ± 9.4	Compressed
5	24	1.07	63.5 ± 4.0	Compressed
6	30	0.96	44.5 ± 6.9	Compressed

Table 27.1 Sample nomenclature and physical and thermal characteristics

Reproduced from Malekpour et al. [1] with permission from American Chemical Society

27.2.2 Optothermal Raman Measurements of Thermal Conductivity

For thermal studies of GL, the noncontact optothermal Raman (OTR) method was used [20]. OTR is a direct steady-state measurement technique that determines the value of thermal conductivity. (Indirect techniques such as the "laser flash" technique calculate it from the thermal diffusivity data.) This technique was originally

Fig. 27.3 Optical image of the sample holder, designed for macroscale samples, for optothermal Raman measurements. The suspended GL-on-PET, shown with a black arrow, is sandwiched between two massive aluminum heat sinks, at its two ends. The laser-induced local heating occurs at the middle of the ribbon



introduced by Balandin and co-workers for measuring thermal properties of singlelayer graphene [19]. The measurement technique includes micro-Raman spectrometer, which is used as thermometer to determine the local temperature rise. The Raman excitation laser also serves as a heater to induce local heating in the sample. Owing to the clear G peak Raman band of graphene, the temperature could be accurately read. The measurement procedure involved two steps: the calibration measurement and the power-dependent Raman measurement. In the study discussed, the authors performed micro-Raman analysis with a 488 nm excitation wavelength and power level varying up to 10 mW [1]. For power-dependent Raman measurements, the GL-on-PET samples were cut into rectangular ribbons and suspended across a specially designed sample holder, shown in Fig. 27.3. The sample holder contains two massive aluminum clamps serving as ideal heat sinks and providing good thermal contact with GL layers.

The calibration measurement was performed inside a cold-hot cell. The cold-hot cell allows the temperature of the sample to be controlled externally. Low excitation power of the Raman laser (~1 mW) was maintained during the calibration measurement to avoid laser-induced heating. As a result of the calibration, the Raman G peak position is determined as a function of the temperature of the sample. Here the temperature interval of 20–200 °C was used. It has been noticed that the G peak position followed an excellent linear shift over the examined temperature range. The slope determines the temperature coefficient of G Raman peak, χ_G , for the measured temperature range. One should note that the χ_G value depends not only on the sample properties but also on the temperature range for which it was extracted.

The second part of the OTR method, power-dependent Raman measurement, includes recording the position of the Raman G peak as a function of the increasing excitation laser power using the special sample holder described earlier. The power on the sample surface was measured by replacing the sample with a photodiode power sensor. The increase in the absorbed laser power, ΔP , generates local heating

leading the Raman G peak to red shift $(\Delta \omega)$. The shift of the G peak was recorded for the uncompressed and compressed samples as the function of the absorbed power. Having the sample geometry and temperature rise, $\Delta T = \gamma_G^{-1} \Delta \omega$, in response to the absorbed power, ΔP , the thermal conductivity K can be extracted by solving the heat diffusion equation numerically. Fourier's equation was solved for the specific sample geometry. Considering the large thickness of GL layer (~9 to 44 μ m), the heat diffusion equation needs to be solved for the 3D structure. The COMSOL software package was used for numerical solution of the equation with proper boundary conditions. A Gaussian distribution of power with the standard deviation set to the laser spot size was used to simulate the laser-induced heating. The suspended GL-on-PET ribbon is connected to the heat sinks at its two ends, modeled as being at room temperature (RT). All other boundaries are defined as insulated from the environment, modeled by having a zero temperature gradient across the boundary. An iteration strategy was used to solve the heat diffusion equation. The total power and the thermal conductivity were given as the inputs to the equation, and the temperature distribution is determined as the result of simulations. The temperature rise is then compared with the measured temperature, and based on the results, the thermal conductivity is adjusted to higher or lower value.

27.2.3 Effect of the Flake Size on Thermal Conductivity of Laminate

27.2.3.1 Experimental Results

Following the procedure described in the previous section, the RT thermal conductivity was measured for different uncompressed and compressed GL-on-PET and is shown in Fig. 27.4 and summarized in Table 27.1. One can see from Fig. 27.4 that the overall thermal conductivity values for GL-on-PET are pretty high $K \approx 40-90$ W/mK. Considering the extremely low thermal conductivity of PET and related plastic materials ($K \approx 0.15$ –0.24 W/mK), coating PET with graphene laminate enhances the thermal conductivity by more than two orders of magnitude (up to $\times 600$ times). Based on the plotted results (Fig. 27.4), high thermal conductivities can be obtained in both compressed and uncompressed GL. No correlation was noticed between thermal conductivity of GL and its mass density or thickness. It was found interestingly that the thermal conductivities of both uncompressed and compressed GL scale linearly with the average flake size D. This would suggest that heat conduction in GL layers is limited by the flake boundaries rather than intrinsic properties of the graphene and FLG. Compression improves the flakes' alignment and consequently results in a higher K value at a given flake size. The better alignment between flakes was confirmed by top view SEM analysis of the flakes, which suggests the population of vertically oriented flakes is suppressed in the compressed samples. The misaligned flakes appear as bright white spots (see



Fig. 27.4 Thermal conductivity of GL-on-PET as a function of average flake size. The results are shown for both compressed and as-deposited samples in circles and squares, respectively. High values of thermal conductivity were obtained for both types of samples. However, at the same flake size, compressed samples have higher values owing to better flake alignment. (Reproduced from Malekpour et al. [1] with permission from American Chemical Society)

Fig. 27.1). The authors further applied the theory of heat transfer in FLG to theoretically interpret their experimental data, which will be discussed in the next section.

27.2.3.2 Theoretical Analysis

Heat conduction in GL-on-PET in the plane direction consists of heat distribution in individual flakes and their boundaries' conduction. Therefore, the total in-plane thermal conductivity depends on the thermal conductivity of each FLG flake as well as the strengths of their coupling to each other. Defining a theoretical thermal conductivity to GL with such a random structure is not easy due to uncertainty of parameters like the strength of individual flakes' attachment and their mutual orientation. In [1], the authors modified formulas describing heat conduction in graphite thin films [33, 34] to gain insight into the heat conduction in GL-on-PET. The specifics of graphene laminates that are entered to the model are characteristic dimensions of the flakes and concentration of defects. The thermal conductivity in a graphene laminate for its basal plane is written as [33, 35, 36]:

$$K = K_{xx} = \frac{1}{L_x L_y L_z} \sum_{s, \vec{q}} \hbar \omega_s(\vec{q}) \tau \Big(\omega_s(\vec{q}) \Big) v_{x,s} v_{x,s} \frac{\partial N_0}{\partial T},$$
(27.1)

where $\tau(\omega_s(\vec{q}))$ denotes the relaxation time of a phonon with the frequency $\omega_s(\vec{q})$ from the *s*-th acoustic phonon branch (s = LA, TA, ZA), $\vec{q}(q_{\parallel}, q_z)$ is the phonon wave vector, $v_{x,s}$ is the projection of phonon group velocity, N_0 is the Bose-Einstein distribution function, *T* is the temperature, and L_x , L_y , and L_z are the actual sample size. The terms *LA*, *TA*, and *ZA* show the longitudinal acoustic, the transverse acoustic, and the out-of-plane acoustic phonon branches, correspondingly. Following the approach described in [33], the phonon transport in GL is defined to be two-dimensional (2D) for phonons with frequencies $\omega_s > \omega_{c,s}$ and three-dimensional (3D) for phonons with $\omega_s \le \omega_{c,s}$, where ω_c is a certain low-bound cutoff frequency. Applying the equal-energy surfaces $\omega_s(\vec{q})$ approximation with the cylindrical surfaces, one can rewrite Eq. (27.1) for the 2D and 3D parts of the thermal conductivity in the following form [33]:

$$K^{3D} \equiv \frac{\hbar^2}{4\pi^2 k_B T^2} \sum_{s=TA, LA, ZA} \frac{1}{v_s^{\perp}} \int_{0}^{\omega_{c,s}} \left[\omega_s^{\parallel} \left(q_{\parallel} \right) \right]^3 \tau \left(\omega_s^{\parallel} \right) v_s^{\parallel} \left(q_{\parallel} \right) \right) \frac{\exp\left(\hbar \omega_s^{\parallel} / k_B T \right)}{\left[\exp\left(\hbar \omega_s^{\parallel} / k_B T \right) - 1 \right]^2} q_{\parallel} d\omega_s^{\parallel},$$

$$K^{2D} \equiv \frac{\hbar^2}{4\pi^2 k_B T^2} \sum_{s=LA, TA, ZA} \frac{\omega_{c,s}}{v_s^{\perp}} \int_{\omega_{c,s}}^{\omega_{max,s}} \left[\omega_s^{\parallel} \left(q_{\parallel} \right) \right]^2 \tau \left(\omega_s^{\parallel} \right) v_s^{\parallel} \left(q_{\parallel} \right) \frac{\exp\left(\hbar \omega_s^{\parallel} / k_B T \right)}{\left[\exp\left(\hbar \omega_s^{\parallel} / k_B T \right) - 1 \right]^2} q_{\parallel} d\omega_s^{\parallel}.$$

$$(27.2)$$

where $\omega_{c,s}$ is the phonon frequency of the *s*-th branch at the *A* – point of graphite's Brillouin zone and $v_s^{\perp} = \omega_{c,s}/q_{z,\max}$.

In these calculations, three mechanisms of phonon scattering were taken into consideration [34–37]: Umklapp scattering $\tau_U(\omega_s^{\parallel}) = M v_s^2 \omega_{\max,s} / \left(\gamma_s^2 k_B T \left[\omega_s^{\parallel} \right]^2 \right)$, point-defect scattering $\tau_{pd}\left(\omega_s^{\parallel}\right) = 4v_s^{\parallel}/\left(S_0\Gamma q\left[\omega_s^{\parallel}\right]^2\right)$, and scattering on the flake boundaries $\tau_b(\omega_s^{\parallel}) = D/v_s^{\parallel}$, where the average Gruneisen parameter is branch dependent and is equal to $\gamma_{LA} = 2$, $\gamma_{TA} = 1$, and $\gamma_{ZA} = -1.5$, $\omega_{max, s}$ is the maximal frequency of s-th branch, S_0 is the cross-sectional area per atom, M is the graphene unit cell mass, and Γ is a parameter showing the strength of the point-defect scattering and defined from the typical defect densities in the given material. Here τ is the total phonon relaxation time determined from the Matthiessen's rule: $1/\tau = 1/\tau$ τ_{pd} + $1/\tau_U$ + $1/\tau_b$. In this model the scattering from the boundaries of FLG was assumed to be completely diffused. The low-bound value of the Γ parameter was estimated from energy-dispersive X-ray spectroscopy (EDS). The EDS results show the characteristic material composition 92–94% of carbon, 5.7–6.5% of oxygen, 0.34% of sodium, and 0.56% of sulfur. Using these impurity compositions, the Γ parameter is calculated to be 0.02–0.03. This value does not take into account the effect of vacancies and related structural defects, which also contribute to the phonon - point-defect scattering. Therefore, the authors used larger Γ values in the range



0.05–0.2 in their calculation. This value is rather typical for semiconductor or electrically insulating technologically important materials.

The results of their calculations are shown in Fig. 27.5a, b demonstrating the dependence of the thermal conductivity $K = K^{3D} + K^{2D}$ on temperature for different values of the average flake size D and different Γ . For comparison, the experimental points have been added to the plot, depicted by the circles. A weak dependence of K on the temperature was noticed in the range of experimentally observed values of K. The same behavior was observed in polycrystalline materials, where the phonon scatterings of crystalline grains dominate [37]. One should note that increasing D or decreasing Γ leads to restoration of the strong dependence of K on the temperature (see Fig. 27.5b). This behavior is typical for crystalline semiconductors and graphene [38]. It was found that the dependence of K on D obtained from calculations is weaker than the experimental one. This inconsistency was attributed to the different orientation and coupling of flakes in experimental samples, which has not been considered in the model description. The increasing dependency of thermal conductivity with the increasing size of the graphene fillers, that was observed experimentally, was successfully confirmed by theoretical calculations. This dependency is in line with the literature reports for carbon nanotubes and other carbon allotropes [39, 40]. The values of the thermal conductivity obtained for graphene laminate at RT (K ~ 90 W/mK) are significantly lower than measured values reported for large suspended graphene layers (K ~ 3000 W/mK) [20]. This smaller value was explained by the fact that the thermal conductivity of the laminates is limited not by the lattice dynamics of the graphene flakes but by their size, flake coupling, and orientation with respect to the heat flux.

27.2.4 Practical Thermal Applications

One of the interesting facts about this study was that high thermal conductivity values of GL were achieved in both uncompressed and compressed GL-on-PET. This suggests that for practical applications, graphene coating can be beneficial for improving heat conduction properties of plastics without roll compression or any other processing steps. The plastic material used in this study, polyethylene terephthalate (PET), is widely used in the packaging industry for water or soft drink bottles. The low cost, durability, and lightweight of plastics make it beneficial for packaging industry, but in many cases, the insulating behavior of plastic is not desirable and limits many possible applications. New applications of plastic materials, e.g., for the packaging or housing of electronic components, require higher values of thermal conductivity. This is mainly due to the increasing dissipated heat densities for modern electronics and optoelectronics. The described thermal data suggests that graphene laminates could be applied as potential thermal coatings in such applications. It has been demonstrated that graphene laminate coatings could improve the thermal conductivity of plastic materials up to 600 times. Thus, a significant increase in the potential range of practical applications of plastics could be achieved, allowing them to be used in areas not feasible until now. Considering the fact that heat removal has become a crucial issue for continuing progress in the electronic industry, this could be a significant progress for improving thermal management of electronic and optoelectronic packaging.

27.3 Reduced GO Film as Anisotropic Heat Spreaders

Due to its extremely high in-plane thermal conductivity, graphene inspired a surge in experimental and theoretical studies of heat conduction in graphene and other two-dimensional (2D) materials [22, 33, 36, 41–43]. The thermal conductivity of graphene can exceed that of the basal planes of graphite [19–21, 44, 45]. Both graphene and few-layer graphene (FLG) have been proposed as fillers in the thermal interface materials [24, 46, 47]. Moreover, they can be useful as flexible heat spreaders for cooling local hot spots in electronics and optoelectronics [1, 48–50]. For this reason, researchers are trying to develop methods to scale up the production of graphene sheets. One of the possible procedures to industry-scale applications of graphene-based materials for thermal management is the reduction of

graphene oxide (GO). However, the quality of graphene sheet produced by this technique is lower compared to the theoretical potential of pristine graphene and compared to other methods such as mechanical exfoliation. This cost-effective lower-quality graphene can still be useful for applications, such as thermal management, where exploiting high intrinsic electrical and thermal properties of graphene is not critical. In this section we describe properties of temperature-treated reduced GO (rGO) films following our data reported in [2]. It has been established that a significant enhancement in the in-plane thermal conductivity of the rGO films can be achieved by applying high-temperature annealing. On the other hand, a very small value of cross-plane thermal conductivity was found in such rGO films. Therefore, an exceptionally strong anisotropy of the thermal conductivity, $K/K_{\perp} \sim 675$, was achieved for temperature-treated rGO films [2]. This anisotropy factor is much larger than that of high-quality graphite. In the following, we will first describe the reduction of graphene oxide and the techniques used to investigate the effectiveness of reduction. We will continue the chapter by reviewing the thermal and electrical analysis done on the thermally reduced GO films and finally discuss the theoretical interpretations of the results.

27.3.1 Reduction of GO as a Cost-Effective Method for Graphene Production

The reduction of GO films to obtain the reduced graphene oxide is important, mainly due to the fact that graphene oxide is strongly hydrophilic and thus the exfoliation of graphene oxide from graphite oxide is eased. Using a well-established Hummers method or its modifications [51, 52] allows one to produce GO from natural graphite in a large scale. Excellent mechanical properties have been reported for thin films on the basis of GO [53, 54]. However, very low values of thermal conductivity have been attributed to GO (K = 0.5-1 W/mK at RT) [55–57].

The reduction process of graphene oxide strongly affects the quality of the produced rGO. Different reduction techniques are being used, all aiming to restore the structure of pristine graphene. The methods are mainly based on chemical, thermal, or electrochemical means. Synthesizing reduced graphene oxide (rGO) films via conventional chemical or thermal reduction techniques does not necessarily result in increased *K* or the *K*/*K*_⊥ ratio due to residual impurities, defects, and disorder [20]. The authors of [2] studied several films including the reference free-standing GO films and the films annealed at different temperatures: 300, 600, and 1000 °C. A modified Hummers method was used to prepare the initial GO [58–60]. The prepared GO was then used to prepare a GO film by casting the GO dispersion into a mold and then drying. The next step included thermal treatments for preparing rGO films. For this purpose, the samples were placed in a tube furnace and heated up in a N₂ atmosphere. The residence time of 60 min was used for each temperature. As a result of this temperature treatment, free-standing rGO films are



Fig. 27.6 Top view (**a**, **c**) and cross-sectional view (**b**, **d**) SEM images of the GO (**a**, **b**) and 600 °Creduced GO (**c**, **d**) films. Due to the formation of air pockets, the thickness increases and the surface becomes more corrugated after reduction. (Reproduced from Renteria et al. [2] with permission from John Wiley & Sons)

obtained due to the reduction process. A scanning electron microscopy (SEM) study was done on the samples to investigate their microstructure.

Figure 27.6 shows the top (a–c) and cross-sectional (b–d) SEM micrographs of the films before and after thermal treatment. Based on the cross-sectional SEM images, the films consist of a layered structure where individual continuous sp^2 layers become larger. The thermal treatment does not change the interlayer distance

between sp² atomic planes substantially, which is in line with previous reports that used XRD analysis [61]. At the same time, due to the release of oxygen and carbon dioxide, "air pockets" develop between the layers. These "air pockets" strongly influence the cross-plane thermal conduction while not seriously affecting the in-plane thermal distribution. Moreover, the formation of "air pockets" corrugates the surface of the high-temperature annealed films. This was confirmed by morphological changes observed in SEM images and also with the measured thickness data. As a result of the high-temperature treatment at 1000 °C, the average thickness of the reference GO film increased up to almost four times its initial value ($H = 40 \,\mu$ m). For measuring the true mass density ρ , the films were compacted into the special sample container to remove the trapped air and the density was measured to be the same for all the samples (1.87 g/cm³). However, the apparent mass density, which includes the "air pockets," varies almost inversely with the increased thickness. In the next section, we will discuss possible methods used by authors to investigate the effectiveness of reduction.

27.3.2 Assessment of the Quality of the Reduction Process

In order to evaluate the effectiveness of reduction, different spectroscopy techniques can be used. Here in this study, X-ray photoelectron spectroscopy (XPS) and Raman spectroscopy were used for this purpose. In the following sections, we will discuss these two techniques and the results obtained.

27.3.2.1 X-Ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) was used to assess the quality and completeness of the reduction process [2]. Using this technique, the authors determined the chemical composition and morphology of the samples before and after thermal annealing was applied [2]. Carbon (C), oxygen (O), nitrogen (N), and sulfur (S) elements appear on all samples' XPS spectra at varying concentrations. An important XPS spectrum range, carbon (C1S), is shown in Fig. 27.7a, b. The spectrum shows that the main carbon bonds occur at ~284.6 eV, 286.8 eV, and 288.1 eV, corresponding to sp² and sp³ C, single-bonded carbon-oxygen (C-O), and double-bonded carbon-oxygen (C=O). Single and double carbon oxygen bonds, C-O and C=O, are significantly reduced after annealing at 600 °C and almost disappear after the 1000 °C treatment (see Fig. 27.7a, b). The oxygen removal caused by thermal treatment results in a rise in carbon concentration, up to 92% at 1000 °C treatment. Due to a small energy difference between C sp² and C sp³ peaks, the interpretation of these two bonds is complicated. However, the XPS results indicate that C sp² peak energy is in a range 284.1–285 eV, while the C sp³ peak



energy is in the range 284.9–286 eV which is in line with other reported data [62–67]. For a rGO film annealed at T = 1000 °C, there is only one peak centered around 284.8 eV which mostly corresponds to C sp² bonds.

27.3.2.2 Raman Spectroscopy of Carbon Materials

Raman spectroscopy is an effective tool that can be used to monitor how thermal treatment changes the structural composition of rGO films. Raman spectroscopy was performed in a backscattering configuration under visible ($\lambda = 488$ nm) and UV ($\lambda = 325$ nm) laser excitations (Fig. 27.8a, b) [2]. The Raman spectra of 300, 600, and 1000 °C treated films have been shown in Fig. 27.8a. The peaks at ~1350 cm⁻¹ and 1580 cm⁻¹ correspond to the D and G peaks, respectively. Two other bands show up in visible Raman spectra: the 2D band centered around 2700 cm⁻¹ and a S3

Fig. 27.8 Visible and UV Raman spectra of rGO films annealed at different temperatures. The peaks at $\approx 1350 \text{ and } 1580 \text{ cm}^{-1}$ correspond to the D and G bands, respectively. The spectrum of 1000 °Cannealed film shows a more pronounced separation of D and G bands. Moreover, the 2D and S3 bands become more prominent which is an indication of moving toward a more ordered material. In UV Raman the D to G band intensity ratio reduces at 1000 °C-annealed film that could be attributed to the reduction of defects and carbon sp3 bonds. (Reproduced from Renteria et al. [2] with permission from John Wiley & Sons)



peak near 2900 cm⁻¹, consistent with literature reported values [68–70]. After the higher temperature treatment was applied, the separation between the D and G peaks becomes more pronounced, as well as intensities of the 2D and S3 bands. These changes indicate that the reduction of the GO film is happening as the thermal treatment is applied. Moreover, the films are moving away from an amorphous state to a more ordered material. The results are in line with XPS data showing the disappearance of C=O and C-O bonds after high-temperature annealing. On the other hand, the UV Raman, which is known to be more sensitive to C sp3 and C-H bonds, is shown in Fig. 27.8b. The UV Raman D to G band intensity ratio underwent a significant decrease in rGO annealed at 1000 °C as compared to that annealed at 300 °C. This suggests that the amount of sp³ carbon bonds in the 1000 °C treated film is small and the reduction mostly results in sp² carbon bonds to form.

27.3.3 Thermal and Electrical Conductivity of Reduced GO Films

The in-plane and cross-plane thermal conductivity of the films described in [2] was measured using a transient "laser flash" technique (LFT). The optothermal Raman measurements [20] were performed to cross-check the in-plane thermal conductivity of the films. It is interesting to compare the changes in the in-plane thermal conductivity with those in electrical conductivity since both the phonon and electron transport can be affected by the defects and structural disorder in carbon materials. For this purpose, the authors measured the electrical sheet resistance using the van der Pauw technique [2].

27.3.3.1 Thermal Conductivity Measurements

The LFT measurements were used for investigating thermal conductivity of the films. This technique directly measures the thermal diffusivity α of the material [71], and the thermal conductivity is later calculated from diffusivity data. The samples were placed inside special stages and sample holders that fitted their size in order to perform LFT measurement. A xenon lamp with millisecond energy pulses illuminated the bottom of the stage to heat it up. An infrared detector monitors the temperature of the opposite surface of the sample [72, 73]. The time it takes for the temperature rise to reach the backside of the sample depends on the sample's thermal diffusivity value. Therefore, this value can be extracted from the measured temperature/time function on the backside of the sample. Both the in-plane and cross-plane thermal diffusivity can be measured with LFT using different sample holders and masks. A schematic of these masks and sample holders is shown in Fig. 27.9. The in-plane sample holder measures the temperature rise at the backside of the sample at the different lateral position compared to light input. This



Fig. 27.9 Cross-plane and in-plane sample holder and mask setup for laser flash measurement. In both setups a flash lamp heats the sample at one side and an IR detector reads the temperature rise at the opposite side of the sample. However, an in-plane mask is designed so that the temperature reading occurs at different lateral position compared to the heating one. Therefore, the generated heat mostly travels in the in-plane direction to produce the corresponding temperature rise

arrangement allows the input heat to travel mostly in the in-plane direction to reach the location where the temperature rise is being read [50].

Having the thermal diffusivity α , specific heat C_p , and mass density ρ of the samples, one can obtain the thermal conductivity from the equation $K = \rho \alpha C_p$. An independent measurement is needed to determine the specific heat of the samples. This could be done using a calorimeter or a separate measurement with the same apparatus using a reference sample of similar thermal properties with known tabulated C_p . Here, in this study, the latter was used with graphite as the reference sample. The mass density of the sample, which is equal to its mass *m* divided by its volume *V*, decreases after the temperature treatment is applied, based on XPS data. This is due to the removal of oxygen, nitrogen, and sulfur impurities:

$$m = \gamma m_0, \gamma = \frac{\left(M_c + f^O M_O + f^S M_S + f^N M_N\right)}{\left(M_c + f^O_0 M_O + f^S_0 M_S + f^N_0 M_N\right)}.$$
(27.3)

Here, m_0 is the mass of the untreated sample, M_i is the molar mass of the *i*-th element (i=C, O, S, N), and f_0^i and f^i are the ratios between the concentration of the *i*-th element and carbon in untreated and treated samples, respectively. Therefore, the density ratio between treated and non-treated samples is proportional to their thickness ratio as follows: $m/V = \gamma \rho_0 H_0/H$, where H is the thickness of treated samples, H_0 is the thickness of non-treated film, and ρ_0 is the true density measured independently. Finally, the cross-plane thermal conductivity is given by:

$$K_{\perp} = \gamma \rho_0 (H_0/H) \alpha_{\perp} C_p. \tag{27.4}$$

The cross-plane thermal diffusivity value is needed to extract the in-plane diffusivity when performing the in-plane LFT experiment. Therefore, α_{\perp} was entered as the input parameter to the system. In order to separate the cross-plane (axial) α_{\perp} and in-plane (radial) diffusivities α , an iterative scheme was used. The number of carbon layers participating in the in-plane heat distribution does not seriously change for untreated and treated samples, i.e., $H \approx H_0$. The small deviation between H and H_0 was attributed to negligible change of carbon interlayer distance with treatment. Using Eq. (27.4), $K = \gamma \rho \alpha C_p$, the in-plane thermal conductivity was achieved, having the in-plane α value and $H = H_0$. The authors calibrated the instrument and data extraction procedures with materials of known thermal conductivity in order to ensure accuracy. The standard deviations of the LFT measurements were estimated as 3–5%.

All the obtained cross-plane diffusivity values of K have been illustrated in Fig. 27.10 as a function of measuring temperature. Very small cross-plane thermal conductivity values (below 0.25) were obtained for all samples. It was found interestingly that K_{\perp} underwent a drastic reduction as high-temperature annealing was applied. Considering the low thermal conductivity value of air (~0.02 W/mK), the authors attributed this reduction to the direct effect of the "air pockets" formation and also to the sp² bonds restoration within the atomic planes. The softening of the



bonds between the layers may also play a role. This effect will be discussed in more details in the theoretical analysis section.

The dependence of thermal conductivity on temperature is weak. The slightly increasing thermal conductivity behavior is typical for amorphous and disordered materials. A rather disordered material was expected in the cross-plane direction owing to the film thickness nonuniformity and residue defects. This feature remains even after high-temperature treatment where a K_{\perp} value of ~0.09 W/mK was obtained. This extremely small value can be considered to be at the low bound of the amorphous limit [119]. Low cross-plane values of thermal conductivities, even below the amorphous limit, have been reported in the literature [120].

We now continue discussion of the results of in-plane thermal conductivity measurements. Figure 27.11 presents all the films' in-plane components of thermal conductivity, before and after annealing was applied, as a function of measuring temperature. As expected, by applying higher annealing temperature, higher values of thermal conductivity were obtained. The room temperature value of in-plane thermal conductivity obtained for GO film (2.9 W/mK) increases almost 20 times in 1000 °C annealed film (61 W/mK). One should note that the rGO samples annealed at 300 and 600 °C show a weak increasing dependency as temperature increases, while the film annealed at 1000 °C reveals strong decreasing behavior. This suggests that the phonon transport in samples annealed at 300 and 600 $^{\circ}$ C is still limited by disorder, while the one annealed at 1000 °C is limited by the Umklapp scattering process. This latter is more like a crystalline material's feature. Therefore, a more successful restoration of graphene was achieved by annealing at high temperature (1000 °C), although the sample still has a very large concentration of defects. One should remember that in crystalline materials the phonon thermal conductivity decreases as 1/T due to the Umklapp phonon scattering [20]. The authors explained the growing behavior of K with annealing temperature by the



Fig. 27.11 In-plane thermal conductivity obtained from laser flash measurement as a function of temperature. The thermal conductivity increases continuously as higher annealing temperature is applied. At room temperature, thermal conductivity of reference GO sample increases from 2.9 W/ mK up to 61 W/mK in the 1000 °C-annealed film. Moreover, strong temperature dependency of thermal conductivity was observed in 1000 °C-annealed film corresponding to the Umklapp scattering limits observed in ordered materials. (Reproduced from Renteria et al. [2] with permission from John Wiley & Sons)

enlargement of sp^2 grains and reduction in phonon scattering on O and other impurities (confirmed by the XPS data).

Other than laser flash technique, the authors used the optothermal Raman method, discussed in Sect 27.2.2, to cross-check their thermal conductivity values. It was found that thermal conductivity values were consistent with the "laser flash" data within 7% experimental uncertainty.

They concluded that $T \approx 1000$ °C could be considered as a useful reference annealing temperature at which O reduction and sp² bond restoration take place and high thermal conductivity values were obtained. Previously it was reported that O reduction and partial exfoliation of graphitic layers start at temperatures as low as 127 °C [61]. As a result of substantial loss of the oxygen surface groups, the process is accompanied with exfoliation. At higher annealing temperatures, $T \ge 600$ °C, the reduction improves, with a loss of O and H and a conversion of hybridized carbon atoms from sp³ into sp² [61]. It was also reported that T = 1000 °C acts as a critical temperature in GO treatment and their resulting graphene-like material contained <2% oxygen and 81.5% C sp² [61].

The high values of the in-plane thermal conductivity along with its low crossplane component lead to an unusually high K/K_{\perp} ratio to be obtained. One should note that the highest value of thermal conductivity achieved for the thermally treated rGO film (K = 61 W/mK at RT for rGO annealed at T = 1000 °C) is still much lower

Table 27.2 Electrical	Sample	Sheet resistance		
treated rGO films	GO	0.514 ± 0.236 MQ/Y		
ireated 160 mins	rGO (T = 300 °C)	$27.0 \pm 17 \ \Omega/\Upsilon$		
	rGO (T = 600 °C)	$2.01 \pm 1.6 \ \Omega/\Upsilon$		
	$rGO (T = 1000 \ ^{\circ}C)$	$2.13 \pm 1.1 \Omega/\Upsilon$		

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rGO sample: reduction method	Sheet resistance	Reference
Thermal reduction and annealing at 300-1000 °C	1–19 Ω/Υ	This work
Hydrogen and thermal treatment followed by CVD	~14 kΩ/Ύ	[74]
Hydroiodic acid (HI)	~840 Ω/Ύ	[75]
Hydrazine vapor and thermal treatment	100–1000 Ω/Υ	[76]
Thermochemical nanolithography	18–9100 Ω/Υ	[77]
Hydrogen reduction	18 Ω/Υ	[78]

Table 27.3 Comparison of electrical resistance data for rGO films

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than that in graphite or graphene (K = 2000 W/mK at RT for basal planes of graphite and can exceed this value in large graphene layers) [20, 36]. This could be explained by the presence of grains and disorders in rGO films, which cause phonon thermal transport to be limited not by intrinsic properties of graphene layers but by the grain and disorder scattering. However, the samples treated at T = 1000 °C tend to follow the intrinsic Umklapp scattering behavior (Fig. 27.11).

27.3.3.2 Electrical Conductivity Measurements

The electrical sheet resistances of GO and rGO films were determined using the van der Pauw technique [2]. For this purpose, square pieces of the samples were probed with four ohmic tungsten pins placed at each corner, and the resistance was measured at the different pairs of contacts. The sheet resistance was then calculated using the van der Pauw formula. The values obtained in [2] are presented in Table 27.2. A significant decrease in the resistivity values occurred after high-temperature annealing (from 0.5 M Ω / Υ in GO to ~1 to 19 Ω / Υ T = 1000 °C treated rGO). The increase of the electrical conductivity of rGO films was attributed to the increasing carbon sp² phase as in other carbon derivatives. It was also reported in [66] that the electrical conductivity of rGO correlates with the sp² (C-C)/sp³ (C-O, O-C-O) peak ratio in XPS spectra. For comparison, other values of resistivity of rGO films reported in literature are provided in Table 27.3.

27.3.4 Theoretical Interpretation of Measured Thermal Conductivities

To analyze the experimental thermal data in [2], one can adopt a theoretical model developed for the thermal conductivity of graphite in [33]. In this model, the authors used graphite phonon energy dispersions, obtained within the Born-von Karman model of lattice dynamics [79, 80], and applied the effect of oxygen and other impurities as point defects. Following the approach of [33], the phonon transport in rGO was treated as two-dimensional (2D) for phonons with frequencies $\omega_s > \omega_{c,s}$ and three-dimensional (3D) for phonons with $\omega_s \leq \omega_{c,s}$, where $\omega_{c,s}$ is the low-bound cutoff frequency of the *s*-th phonon branch. The in-plane thermal conductivity *K* in - plane is given by:

$$\begin{split} K^{\text{in-plane}} &= K^{3D} + K^{2D}_{\omega_{c,s}}, \\ K^{3D} &\equiv \frac{\hbar^2}{4\pi^2 k_B T^2} \sum_s \int_0^{\omega_{c,s}} q_{z,s}(\omega) \omega^2 \tau_s(\omega) v_s^{\parallel} \Big(q_{\parallel} \Big) \frac{\exp(\hbar\omega/k_B T)}{\left[\exp(\hbar\omega/k_B T) - 1\right]^2} q_{\parallel} d\omega, \\ K^{2D} &\equiv \frac{\hbar^2}{4\pi^2 k_B T^2} \sum_s \frac{\omega_{c,s}}{v_s^{\perp}} \int_{\omega_{c,s}}^{\omega_{\max,s}} \omega^2 \tau(\omega) v_s^{\parallel} \Big(q_{\parallel} \Big) \frac{\exp(\hbar\omega/k_B T)}{\left[\exp(\hbar\omega/k_B T) - 1\right]^2} q_{\parallel} d\omega. \end{split}$$

$$(27.5)$$

Here $\vec{q}\left(q_{\parallel},q_{2}\right)$ is the phonon wave vector, $\tau_{s}(\omega)$ is the relaxation time for a phonon with the frequency ω from the *s*-th acoustic phonon branch, $v_{s} = d\omega/dq^{\parallel}$ is the in-plane phonon group velocity for the *s*-th branch, *T* is the temperature, k_{B} is the Boltzmann's constant, and \hbar is Planck's constant. The six lowest phonon branches were included in the summation of Eq. (27.5): in-plane longitudinal acoustic LA_{I} , in-plane transverse acoustic TA_{I} , out-of-plane transverse acoustic ZA, in-plane longitudinal acoustic-like LA_{2} , in-plane transverse acoustic-like TA_{2} , and out-ofplane transverse acoustic-like ZO'.

Three phonon scattering processes, the Umklapp scattering (*U*), point-defect scattering (*PD*), and scattering on ordered cluster edges (*E*), were considered as the main mechanisms limiting the thermal conductivity in rGO. Therefore, the total phonon relaxation time τ was calculated using Matthiessen's rule as [32, 33, 35, 36, 81, 82]:

 $1/\tau_s = 1/\tau_{PD, s} + 1/\tau_{U, s} + 1/\tau_{E, s}$, where $\tau_{U,s}(\omega) = Mv_s^2 \omega_{\max,s} / (\gamma_s^2 k_B T[\omega]^2)$, $\tau_E(\omega) = L/v_s^{\parallel}$, and $\tau_{PD,s}(\omega) = 4v_s^{\parallel} / (S_0 \Gamma q^{\parallel} \omega^2)$. Γ is the measure of the strength of the point-defect scattering due to mass difference, *L* is the average length of ordered sp² or sp³ clusters, $\omega_{\max,s}$ is the maximum frequency of the *s*-th phonon branch, S_0 is the cross-sectional area per atom, and *M* is the graphite unit cell mass. Here the average of the Gruneisen parameters shown by γ is a parameter depending on phonon branches and is equal to $\gamma_{LA_1,LA_2} = 2$, $\gamma_{TA_1,TA_2} = 1$, and $\gamma_{ZA,ZO'} = -1.5$.

	C (%)	O (%)	S (%)	N (%)	Г
GO	65.9	29.2	3.7	1.1	1.208
rGO (T = 300 °C)	89.4	10.3	0.3	0	0.229
rGO (T = 600 °C)	90.6	8.6	0.4	0.4	0.206
rGO (T = 1000 °C)	91.9	6.7	1.0	0.4	0.213

Table 27.4Elemental composition and Γ parameter values

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The values of $\omega_{c, s}$ were determined from the phonon spectra as the highest energy of the *s*-th branch along the c-axis direction: $\omega_{c,LA_1/LA_2} = 89 \text{ cm}^{-1}$, $\omega_{c,TA_1/TA_2} = \$\89 cm^{-1} , and $\omega_{c,ZA/ZO'} = 32 \text{ cm}^{-1}$. Γ is a parameter showing the strength of the point-defect scattering and was estimated from the following formula [32]: $\Gamma = \sum_i c_i (\Delta M_i/M_C)^2$, where $\Delta M_i = M_{d, i} - M_C$ is the difference between the mass of the point-defect $M_{d, i}$ and carbon mass M_C and c_i is the ratio between the concentrations of the defects *i* and carbon atoms. Here an impurity atom attached to a carbon atom was modeled as a point-defect in the graphite lattice. Based on the XPS results (Table 27.4), the GO and rGO samples reveal three main impurity atoms: O, N, and S. Having the concentrations of these impurities, the Γ parameter can be calculated for each sample separately. Table 27.4 indicates the XPS measured defect concentrations and calculated values of Γ .

Figure 27.12 shows the dependence of the in-plane thermal conductivity, calculated from Eq. (27.5) on the average length *L* of the ordered graphitic clusters. The results were provided for different values of Γ . The authors attributed the growth of in-plane thermal conductivity caused by thermal treatments to three reasons. As the GO films undergo high-temperature treatment, (i) the density of defects reduces, (ii) the ordered clustering size increases in lateral dimensions, and (iii) the sp² fraction rises.

It is interesting to note that the concentration of oxygen atoms permanently decreases with annealing temperature (see Table 27.4). Nevertheless, due to small differences in S and N content, the parameter Γ was calculated to be almost the same ~ 0.21 for all thermally treated rGO films. This indicates that the strength of pointdefect scattering is roughly the same for all treated rGO films and is six times weaker than the one in the reference GO film. Therefore, the rise in thermal conductivity should be mainly due to increasing of the lateral dimensions of the ordered clusters, which is compatible with other reports showing that a highly ordered graphene-like lattice is restored after treatment [61, 66, 67]. The authors used both the theoretical and experimental thermal conductivities to estimate the average length of the ordered clusters. Their results show the length increases from ~3.5 nm in GO to ~500 nm in rGO (T = 1000 °C). The latter is in line with reported values in the literature for polycrystalline graphene and graphite (250 nm - 30 µm) [83, 84]. This calculation underestimates the actual average cluster length in the rGO samples due to possible additional phonon scattering on vacancies and dislocations, which was not included. For example, adding $\sim 0.5\%$ vacancies could increase the theoretical L up to 800 nm

Fig. 27.12 In-plane thermal conductivity of GO and rGO films calculated for T = 20 °C as a function of the average cluster size *L*. The experimental data are added in (a) for comparison. In (b) one can see the effect of oxygen impurity. (Reproduced from Renteria et al. [2] with permission from John Wiley & Sons)



for rGO (T = 1000 °C). It was found interestingly that the increase of cluster length with temperature was more prominent at higher annealing temperatures. For example, a three times increase in *L* was obtained as the annealing temperature increased from T = 300 to 600 °C. This increasing factor was 16 for T = 600–1000 °C. Theoretically, high thermal conductivity values, ~500 W/mK, could be obtained for rGO samples with larger grains and reduced impurities. The authors further investigated the effect of the oxygen reduction on the thermal conductivity of rGO (Fig. 27.12b). For this purpose, it was assumed that oxygen is the only impurity of rGO films. It was found that decreasing O concentration from 50% to 1% increases *K* by a factor of 4–24 depending on the average cluster size *L*. Based on the calculations, S and N impurities in rGO (T = 1000 °C) suppress *K* by 28%. High thermal conductivity values, *K* ~ 300 W/mK, could be obtained for *L* ~ 500 nm, if these impurities are removed and the O concentration is reduced to 1%.

27 Graphene Applications in Advanced Thermal Management

The cross-plane thermal conductivity was studied theoretically, and the observed decrease in thermal conductivity with treatment temperature was attributed to an increase in the number and size of the "air pockets" between rGO multilayers (see insert to Figs. 27.6b, d and 27.12a). The experimental data shows a four times increase in thickness of the 1000 °C treated film compared to that of GO, which confirms the increase in the "air pocket" volume. The formation of "air pockets" mostly impacts the cross-plane thermal transport and the in-plane thermal transport is less affected. Using Maxwell-Garnett's effective medium approximation, the cross-plane thermal conductivity can be estimated as [85]:

$$K_{rGO}^{\perp}(\varphi) = K_{GO}^{\perp} \frac{(1-\varphi) \left(K_{air} + 2K_{GO}^{\perp} \right) + 3\varphi K_{air}}{(1-\varphi) \left(K_{air} + 2K_{GO}^{\perp} \right) + 3\varphi K_{GO}^{\perp}},$$
(27.6)

where K_{GO}^{\perp} is the thermal conductivity of the untreated GO, K_{air} is the thermal conductivity of air, and φ is the volume fraction of the "air pockets." Using experimental obtained values, $K_{GO}^{\perp} \approx 0.18$ W/mK and $K_{air} \approx 0.026$ W/mK, the cross-plane thermal conductivity of ~0.075–0.09 W/mK was obtained, assuming $\varphi \sim 0.5 - 0.6$. This value is in a good agreement with the experimental value of 0.09 ± 0.01 W/mK for rGO (T = 1000 °C) at T = 20 °C. The formation of "air pockets" is also responsible for the reduction in the apparent mass density at high annealing temperatures.

The theoretical calculations in [2] successfully explain the observed variation in the two components of thermal conductivity. To summarize, the model attributed the increase of the in-plane component of thermal conductivity to restoration of C sp² bonds, as well as increased sp² grain size and decreased phonon scattering rate on impurities including O. On the other hand, the decrease of the cross-plane component was explained by the appearance of "air pockets" after high-temperature annealing, as well as softening of the restoring forces in this direction. The strongly anisotropic heat conduction properties of rGO films treated at high temperature can be useful for applications where heat removal along one direction is required while shielding is desired along the perpendicular direction. Below we will discuss some possible applications.

27.3.5 Practical Thermal Applications

We reviewed the thermal conductivity of free-standing rGO films subjected to a high-temperature treatment T = 300, 600, and $1000 \,^{\circ}$ C. It was reported that the high-temperature treatment dramatically increased the room temperature in-plane thermal conductivity, *K*, from 2.94 W/mK in the reference GO film to 61.8 W/mK in the rGO film annealed at $T = 1000 \,^{\circ}$ C [2]. On the other hand, the cross-plane thermal conductivity, K_{\perp} , indicates a decreasing trend from ~0.18 W/mK in the reference GO film to ~0.09 W/mK in the rGO film annealed at $T = 1000 \,^{\circ}$ C (2). Therefore, an exceptionally strong anisotropy factor of the thermal conductivity, $K/K_{\perp} \sim 675$, was

obtained for the rGO films, which is substantially larger even than in high-quality graphite ($K/K_{\perp} \sim 100$). Such films could be beneficial for thermal management of modern electronics where heat dissipation in one direction is desired [6]. For this purpose, thermal pads or coatings with similar anisotropic properties are being used to dissipate heat away from the hot spots in the in-plane direction while shielding the heat in the cross-plane direction to protect electronic components underneath them. High-quality bulk graphite carries a significantly large anisotropy factor, K/ $K_{\perp} \sim 100$, having high thermal conductivity along its basal planes ($K \approx 2000$ W/ mK) and low value along its cross-plane direction ($K_{\perp} \approx 20$ W/mK) at room temperature (RT) [31, 32]. However, unprocessed graphite cannot be applied for practical applications due to the lack of industry requirements such as flexibility. Chemically processed graphite, however, is used in composite-based commercial thermal pads to achieve industry applicable films with lower K and smaller K/K_{\perp} ratios. This suggests that a search for new materials with high K/K_{\perp} that can be used for thermal management is essential. The strongly anisotropic heat conduction properties of rGO films treated at high temperature can be beneficial for applications in thermal management, which requires materials which can remove excess heat (high K) along one direction and shield from heat (lower K_{\perp}) along the perpendicular direction.

27.4 Functionalized Graphene Fillers for TIMs

One of the most important and commonly used components of passive thermal management is thermal interface material (TIM). The term TIM is attributed to any material that is inserted between two parts in order to enhance the thermal coupling between these two components, mostly heat source and heat sink, aiming to improve the heat dissipation from heat source to heat sink. In this section we follow results reported by Balandin and co-workers [3] on heat conduction properties of thermal interface materials with self-aligning "magnetic graphene" fillers. In this work the authors synthesized graphene-enhanced nanocomposites using an inexpensive and scalable technique based on liquid-phase exfoliation. The process includes functionalizing graphene and few-layer graphene flakes with Fe_3O_4 nanoparticles to later align them during dispersion of the thermal paste to the connecting surfaces by using an external magnetic field. It was shown that the filler alignment strongly enhances thermal conductivity and diffusivity values through the layer of nanocomposite inserted between two metallic surfaces. In the following sections, we will first review recent developments made on TIMs and then focus on the technique used for the synthesis of a graphene-enhanced TIM. Finally, the experimental thermal analysis will be discussed in detail.

27.4.1 Thermal Interface Materials for Electronic Cooling

Due to the surface imperfections, the conduction pathway between heat source and heat sink is not qualified for proper heat dissipation of modern electronic devices with high-power densities. The main function of a TIM is to improve these surface contacts by filling the voids and grooves between the two connecting surfaces to improve their thermal coupling. Different types of TIMs have been developed, including phase change materials, cured and uncured thermal pastes, and solid heat spreaders. A TIM is typically made of a base (matrix) material treated by thermally conductive fillers to improve its thermal conductivity. Silver, aluminum oxide, and other metal or ceramic particles are the most conventional materials used as fillers. The problem with those materials is that high loading fractions, more than 50%, are needed to obtain the desired thermal conductivity of the TIM. Therefore, advancement of more efficient TIMs is crucial for developing heat removal from modern electronic devices. The improvement of TIM performance is established by finding the proper filler material that is highly thermally conductive and also able to strongly couple with the matrix and attach well to the connecting surfaces. The performance of a TIM is ultimately evaluated by studying the temperature rise reduction in a given device – heat sink assembly. However, the thermal conductivity and thermal resistance of TIM are also important characteristics of the material. Graphene and few-layer graphene (FLG) with unique heat conduction properties [19–21, 45] are ideal fillers in TIMs [24, 25, 86–88]. FLG is attributed to thin graphite piece with the thickness below seven to ten atomic planes. The Raman spectrum of FLG is different from that of bulk graphite [89]. FLG is of interest due to the fact that its thermal conductivity is still high while it deteriorates less than graphene when embedded inside the matrix material [20]. Moreover, due to the larger cross-sectional area of FLG compared to that of graphene, the higher heat flux along the length of the flake is achieved. This makes FLG beneficial for thermal management applications despite its lower thermal conductivity compared to graphene. Several studies reported significant improvement in the bulk thermal conductivity of epoxy by using an appropriate mixture of graphene and FLG and with only small loading fractions, below 10% [24, 25, 86-88]. Promising results have been achieved with other matrix materials such as paraffin wax [29, 46]. In all the mentioned studies, the matrix is filled with a random and homogeneous mixture of graphene and FLG. It has been reported that uniform dispersion of the fillers with the absence of air bubbles are essential for the improved heat conduction properties of the prepared composites [46, 86–88, 90].

However, using aligned fillers along the direction of heat flux is expected to strongly enhance the thermal conductivity of the matrix even at small loading fractions. This has been proved by theoretical considerations of graphene composites [91, 92] and experimental results for other types of filler materials. Considering the heat flux direction in the TIM, the direction of alignment should be perpendicular to the connecting surfaces to effectively ease the heat transfer from one surface (e.g., computer chip) to another (e.g., heat sink or package). A great improvement
(400 times) in thermal conductivity of common matrix materials has been reported along the direction of the graphene flake alignment and at small loading fraction (f = 5 vol. %), based on molecular dynamic simulations [91]. However, no enhancement in thermal conductivity was obtained in the direction perpendicular to the alignment. These results are in line with experimental studies performed on other fillers, such as carbon nanotubes (CNTs) [93–100]. High loading fractions of fillers are not desired since it would increase viscosity and also air gap formation and agglomeration of TIMs which all degrade heat conduction properties. Therefore, TIMs with low loading fractions of graphene and FLG are strongly favored. Moreover, a low loading fraction of graphene fillers is advantageous in order to keep the price of TIMs in the fair range. In the following section, we will discuss how functionalizing graphene and FLG with Fe₃O₄ nanoparticles can help one to achieve the goal of alignment of the fillers.

27.4.2 Synthesis of the Graphene-Enhanced TIMs

For this study the authors synthesized graphene and FLG using the scalable liquidphase exfoliation (LPE) method [101, 102]. The functionalization of these fillers was performed following the recipe previously developed for CNTs used in magnetic and biomedical applications [103, 104]. The process includes poly(sodium 4-styrene sulfonate) (PSS) as a wrapping polymer and polyelectrolyte poly(dimethyldiallylammonium chloride) (PDDA) for a homogeneous distribution of positive charges [105–112]. Due to the electrostatic interactions between positive and negative charges, the adsorption of negatively charged magnetic nanoparticles occurs onto the surface of graphene and FLG. Following this process, graphene fillers dressed with magnetic nanoparticles of ~10 nm average diameter are produced. It was also found that by performing a temperature treatment under certain conditions on a mixture of graphene, FLG flakes, and magnetic nanoparticles, the attachment of nanoparticles to graphene fillers is achieved without any intermediate chemical processing steps. The functionalization of graphene with magnetic nanoparticles followed the CNT route, which was showed for applications other than thermal management [103–114]. The method utilizes polymer wrapping technique (PWT) and layer-by-layer (LBL) self-assembly which leads to the non-covalent attachment of nanoparticles to the carbon filler and leaves their structure and thermal properties intact (see Fig. 27.13).

An important aspect of the procedure is the non-covalent bonding since it preserves the intrinsically high thermal conductivity of graphene [20, 90]. Sometimes a stronger covalent bonding is used to improve the coupling between the CNT filler and the matrix. This usually results in defect formation leading to phonon scattering and TC reduction at least at some filler loading fractions [90]. Here in this work, the authors used poly(sodium 4-styrene sulfonate) (PSS) as a wrapping polymer providing stable dispersions of carbon fillers (both CNTs and graphene). The high density of sulfonate groups on the negatively charged polyelectrolyte PSS leads



Fig. 27.13 Schematic representation of the procedures used to magnetically functionalize graphene and few-layer graphene, including addition of PSS to graphene solution to produce graphene surface coating with the "primer"; addition of PDDA, which sticks to PSS "primer" via electrostatic interactions and provides distribution of positive charges on graphene fillers; addition of the solution of magnetic nanoparticles, which attach to PDDA layer via electrostatic interaction during the stirring; mixing of the magnetically functionalized graphene fillers with the matrix material resulting in the self-aligned composite. By placing the produced composite in an external magnetic field, the filler alignment could be achieved. (Reproduced from Renteria et al. [3] with permission from Elsevier)

the PSS coating to act as a primer on the graphene surface for subsequent uniform adsorption of the cationic polyelectrolyte poly(dimethyl-diallylammonium chloride) (PDDA) through the electrostatic interactions [104, 115, 116]. The deposited PDDA layer gives a homogeneous distribution of positive charges, which leads to the efficient adsorption of negatively charged magnetic nanoparticles onto the surface of graphene by means of electrostatic interactions. The CNT's high curvature hinders the formation of dense coatings. In the case of graphene, its flat surface easily absorbs the nanoparticles with diameters ranging from ~6 to ~10 nm. The negatively charged magnetic nanoparticles prepared in solution are electrostatically engaged to the positively charged PDDA layer adsorbed on graphene fillers.

Figure 27.14 shows the steps for preparing epoxy-based TIMs with "magnetic graphene" fillers, which is similar to the method used for regular LPE graphene [24]. First the epoxy-based components were weighed with the intended loading wt % of LPE graphene powder to the resin and the hardener at the manufacturer's 10:3 ratio guideline. Then the composites were evenly mixed under vacuum conditions. With the help of a vacuum pump accessory, the development of the bubbles trapped as a result of mixing dry materials with liquids was prevented. A low mixing speed (500 rpm) and time were used owing to the high shearing of the dry graphene powder in the non-cured epoxy at high mixing speeds (>1000 rpm) that caused the epoxy to cure faster than desired. The cycles of mixing and vacuuming were repeated several times to achieve homogenously mixed composites. In order to obtain the flake ordering, the composites were exposed to the magnetic field (H = 1.2 T). The non-curing TIMs with "magnetic graphene" were synthesized following a similar process. It is important that the achieved mixture holds a smooth texture since the roughness is an indication of excessive air mixed into the composite and can strongly



Fig. 27.14 Synthesis procedure used for thermal interface materials with graphene and few-layer graphene fillers. (Reproduced from Renteria et al. [3] with permission from Elsevier)

degrade the thermal conductivity. The graphene-enhanced TIMs were sandwiched between two surfaces of interest, e.g., thin copper (Cu) foils, for later thermal testing. Finally, the flake alignment was obtained by placing the surface-TIM-surface sandwich, e.g., Cu-TIM-Cu structure, on a permanent magnet.

The structure and properties of the "magnetic graphene," i.e., graphene and few-layer graphene flakes functionalized with magnetic nanoparticles, are shown in Fig. 27.15. The attachment of magnetic nanoparticles has been confirmed using scanning electron microscopy and transmission electron microscopy (Fig. 27.15a, b). Some agglomeration was intentionally allowed for visualization of flake alignment. Owing to the recent development of strong permanent magnets [117, 118], the alignment of the functionalized graphene flakes with an external magnetic field was facilitated. In the next section, we will discuss analysis done on thermal conductivity and thermal diffusivity of the produced TIM.

27.4.3 Thermal Conductivity and Diffusivity of the Graphene Composites

27.4.3.1 Apparent Thermal Conductivity Analysis Using TIM Tester

In order to characterize the performance of TIM, one should investigate its thermal resistance, R_{TIM} , with specific bounding surfaces: $R_{TIM} \equiv H/K_A = H/K + R_{C1} + R_{C2}$, where *K* is the thermal conductivity of TIMs, *H* is the bond line thickness (BLT), R_{C1}



Fig. 27.15 Characterization of the magnetically functionalized graphene and few-layer graphene fillers. (a) Scanning electron microscopy of graphene and few-layer graphene flakes synthesized by the liquid-phase exfoliation technique. (b) Transmission electron microscopy image of the graphene flake with attached Fe₃O₄ nanoparticles. Observed agglomeration of graphene flakes did not prevent alignment and thermal applications. (c) The reaction of magnetically functionalized graphene fillers under a permanent magnet (B = 1.5 T). (d) Two copper foils with the functionalized graphene TIM between them placed on a flat permanent magnet for alignment purpose. (e) Optical microscopy image of epoxy with aligned graphene fillers. (Reproduced from Renteria et al. [3] with permission from Elsevier)

and R_{C2} are the thermal contact resistances of the TIM layer with the two bonding surfaces, and K_A defines the effective or apparent thermal conductivity of the TIM with two contact resistances. Thermal conductivity of the TIM and BLT as well as thermal contact resistances are the main factors determining the magnitude of R_{TIM} and K_A . These values in their turn depend on the surface roughness, temperature, and viscosity. Practical BLT values should be used to determine the magnitude of R_{TIM} or K_A . One can rewrite the above equation as follows: $K_A = K \times [1 + (K/H) (R_{C1} + R_{C2})]^{-1}$ This equation shows the dependence of apparent thermal conductivity, K_A , on BLT and contact resistances better. To compare TIM performance with actual bonding, K_A , is a more practical metric than the thermal conductivity, K, measured for bulk composite samples. For the proof-of-concept demonstration of the proposed approach of flake alignment, the authors investigated K_A of the composites



Fig. 27.16 Apparent thermal conductivity of a representative commercial TIM plotted as a function of temperature and for different loading fraction, f, of graphene without alignment. Note that the apparent thermal conductivity includes the thermal boundary resistance (TBR) with connecting surfaces. As the loading fraction increases, thermal conductivity increases monotonically in the examined range. The higher loadings were not practical due to the increased viscosity and reduced uniformity of graphene dispersion. (Reproduced from Renteria et al. [3] with permission from Elsevier)

with relevant connecting surfaces and temperature rise in actual devices. For this purpose, conventional curing epoxy and non-curing commercial TIMs designed for IC chip packaging were used to prepare the TIM composites. First LPE graphene fillers were added to non-curing TIMs and the apparent thermal conductivity was studied to verify that an enhancement is achieved. Two different techniques were used to measure the apparent thermal conductivity. The first technique involved the TIM Tester, which measures, K_A . The apparent value of the thermal conductivity includes the effect of thermal contact resistance with the connecting surfaces of interest (e.g., Cu to Cu or Si to aluminum). The results are shown in Fig. 27.16 where thermal conductivities of the non-curing TIMs with graphene and few-layer graphene fillers were plotted as the loading changes from 0 to 6 wt%. One should note that this value is independent of temperature, which is characteristic for disordered materials and beneficial for practical applications. A constant increase of K_A was achieved with increasing loading fraction f. However, increasing f would increase the composite viscosity and reduce the uniformity of graphene dispersion, which was not practical. It was successfully confirmed that a significant increase (two times) in the apparent thermal conductivity of non-curing TIM spread between two Al plates was achieved only by addition of a small fraction (f = 6%) of randomly oriented graphene and FLG. This improvement was obtained without any optimization of the composition of the matrix material for additional graphene fillers. In the next section, we will review the results achieved using LFT as a second measuring technique on apparent thermal conductivity of the composite.



27.4.3.2 Analysis of the Apparent Thermal Diffusivity

Here in this section, we discuss the experimental results of cross-plane thermal diffusivity of Cu-TIM-Cu "sandwich" performed using the "laser flash" technique [3]. The technique was explained in detail in Sect. 27.3.3.1. For this measurement, the samples were fitted into the LFT sample holder available for cross-plane measurements. The mixture of the graphene and FLG fillers was functionalized using the magnetic nanoparticles. The authors prepared two sample one with randomized fillers and the other with oriented ones. The alignment of fillers was performed, placing the sample on top of a flat permanent magnet. The results are shown in Fig. 27.17. It was found that the apparent thermal diffusivity of conventional TIM without any additional fillers ($\alpha \sim 0.23 \text{ mm}^2/\text{s}$) increases by a factor of 1.5 when only ~ 1 wt% of random fillers were applied. One should remember that this diffusivity value includes the effect of the contact resistance with Cu plates. A substantially larger increase - by a factor of 3.8 - was obtained for the oriented graphene fillers of the same loading fraction. For the realistic BLT, the fillers do not extend all the way from one surface to another, and thus no percolation network is formed. However, the fillers orientation along the direction of the heat flow substantially improves the heat conduction properties. In the next section, we will discuss further analysis done to investigate the effect of flake alignment.

27.4.3.3 Effects of Alignment of Graphene Fillers

To better explain the effect of oriented fillers, the authors plotted the ratio of the apparent thermal conductivity in TIMs with the graphene fillers, K_m , to that in the reference TIM without the fillers, K_o (Fig. 27.18). For these measurements TIMs with 1 wt% of graphene were inserted between two Cu films. One should note that



4.5



stronger enhancement was obtained by aligning the fillers. (Reproduced from Renteria et al. [3] with permission from Elsevier)

higher enhancement factors of thermal conductivity were achieved for the TIMs with oriented graphene fillers rather than random ones. However, an enhancement factor of 1.5 was obtained even using random graphene and FLG fillers and at low loading fraction. These data show the low loading fraction of graphene fillers reported to be beneficial for bulk samples [24, 25] is also helpful for TIM layers with small BLT squeezed between two relevant surfaces. For better heat conduction properties, one can either increase the loading of graphene fillers, within certain limits, or align the fillers to achieve the same enhancement with smaller loading. The latter would enhance heat conduction in composites with an epoxy base as well (Fig. 27.19).

As one can see in Fig. 27.19, a two times enhancement of the apparent thermal conductivity was achieved in epoxy-based composite using oriented graphene fillers

at small loading (f = 1 wt%), as compared to the random fillers. The ratio of the apparent thermal conductivity of the composite to that of the base epoxy, K_m/K_o , is \sim 3.2 for the oriented fillers and \sim 1.7 for the random fillers. The effect of contact resistance to the connecting metal surfaces is included in the apparent thermal conductivity values. The enhancement for the bulk thermal conductivity is probably more prominent. One of the interesting features that can be noticed from Figs. 27.15, 27.16, and 27.17 is that the behavior of thermal conductivity and thermal diffusivity with temperature is different for composites with oriented fillers from that of composites with random fillers. An increasing trend of thermal conductivity with temperature was achieved for composites with random fillers, which is characteristic of amorphous and disordered materials [1, 2, 20, 24, 25, 47]. A weaker increasing trend was observed in other TIMs with random graphene fillers [20, 24, 25, 86]. On the other hand, the thermal conductivity of composites with oriented graphene fillers shows a decreasing behavior with temperature. The authors attributed this contrary to the decreasing viscosity at elevated temperatures, resulting in partial loss of the filler orientation.

27.4.3.4 Oriented Graphene Fillers in Thermal PCMs

In this section we describe evaluation of the performance of oriented graphene fillers with the thermal phase change materials (PCM) [3]. Such materials are commonly used for thermal management of photovoltaic solar cells. The room temperature thermal conductivity value of 0.3 W/mK was measured for the conventional PCM sandwiched between two Cu plates. It was found that this thermal conductivity increases to 0.6 W/mK and 1.25 W/mK, for the composites with random and oriented graphene fillers, respectively. It was successfully confirmed that using graphene filler alignment at low loading fraction, an enhancement of thermal conductivity (by a factor of 2) was achieved as with other base materials. The temperature dependence of the thermal conductivity was similar to that of non-curing and epoxy composites. In addition, the authors proved that their filler orientation approach fits with a wide variety of base materials used in passive thermal management. In the next section, we will review the final analysis done by authors to practically evaluate the efficiency of their proposed alignment approach, by applying composites with oriented flakes to an actual computers and by measuring the resulting temperature rise.

27.4.4 Temperature Rise Testing in Computers

The "bulk" value of the thermal conductivity, which is mostly used as an industrial metric, does not completely characterize how well the material will perform in practice. Especially for TIMs, the apparent thermal conductivity measured for a realistic BLT is more informative. This thermal conductivity also includes the effect

of the thermal interface resistances. This metric is not usually provided in industrial products. However, another metric is used instead, to judge the suitability of TIM for a specific application. This metric includes a temperature rise in a given device or a system with specific TIM. In this work, the authors conducted experiments to measure temperature rise, ΔT , using a high-end desktop computer. The experiment allows one to assess the efficiency of TIM in transferring generated heat away from the computer processing unit (CPU). For this purpose, the conventional TIM supplied with the CPU package was replaced with the graphene-enhanced TIMs produced in this work. For alignment of the functionalized graphene fillers, the CPU assemblies were placed on a flat permanent magnet.

In the following, we review the details of the temperature rise testing in CPUs of a desktop computer. To evaluate TIM efficiency in transferring generated heat away from the CPU, a custom desktop computer system was assembled. To ensure controlled constant power output, a CPU under the stress test conditions was used for the temperature rise measurements. A liquid that passed through channels beneath the copper heat sink attached to the CPU performed the CPU cooling task. The cooling system allows a good control and thermal stability owing to large radiator area and high heat capacity of circulating liquid. In conventional air-cooled setups, ambient air is used instead, which would lead to a wide fluctuation over the test time. The selected CPU generated high thermal density power output, 84 W at maximum power consumption, during the thermally significant period while running stress test software. Thermistors were embedded inside each of the CPU's four physical cores for in situ temperature monitoring. An average value of the four temperature readings was used to obtain more reliable temperature rise data. In order to maximize the effective thermal intake area of the copper heat sink, it was placed on a maze of embedded water channels. The surface was polished to decrease the number and depth of the surface trenches, where air trapping was likely to take place, and to provide a better heat sink-to-TIM bonding. Two temperature acquisition programs were used to monitor and log the thermal state of all physical cores. More experimental details are provided in the full text paper [3]. All experimental runs were conducted over the period of 24 h at 100% CPU loading.

To evaluate the efficiency of synthesized TIMs with oriented graphene fillers, the profile curve for commercial (IceFusion) TIMs served as a base for comparison. The decrease in the height of the temperature profile with respect to the established baseline indicated lower temperatures in the cores of the CPU. The BLT was kept approximately constant for various TIMs under study, using a micrometer. A ~1.5 T permanent magnet was used to orient the "magnetic graphene" filler. The CPU heat sink assembly was placed on the magnet to achieve the alignment. Then the CPU with TIM was assembled with the liquid-cooled heat sink for stress testing and temperature rise monitoring. The results are shown in Fig. 27.20 indicating a temperature rise as a function of time inside a computer operating with a heavy computational load. Figure 27.20a shows the obtained results for TIMs with random graphene fillers. The graphene fillers used in this study were also functionalized with magnetic nanoparticles without being oriented by a magnetic field. The purpose was to obtain a preform comparison.



Fig. 27.20 The results of temperature rise test done inside a computer CPU plotted as a function of time. The data are shown for CPU packages that utilized TIMs with random graphene fillers (**a**) and oriented ones (**b**). The temperature rise in CPU package with conventional commercial TIM is also shown as a reference. The insets show the backside of a computer chip with applied TIM. (Reproduced from Renteria et al. [3] with permission from Elsevier)

The results show that at low weight fraction, f, of graphene fillers, no substantial difference in the performance of the TIM was achieved as compared to the reference one. It was found that increasing f leads to the CPU temperature rise (Δ T) decreasing. A 10 °C reduction in Δ T was obtained using $f \approx 4\%$ as compared to the reference commercial TIM (Δ T = 55 °C). Almost 5 °C decrease in Δ T was achieved with $f \approx 2\%$ of random graphene fillers. It was successfully proved that orientation of the functionalized graphene fillers drastically improved the efficiency of the TIM. Figure 27.20b shows that by applying the TIM with $f \approx 1\%$ of oriented graphene fillers, a 10 °C reduction in temperature rise was achieved after 15 h of CPU

operation. This reduction is substantial for practical applications. It is interesting to note that in some device technologies the reduction of the temperature rise by 20 °C is considered an order of magnitude increase of the device lifetime [10, 13].

27.5 Conclusions

In this chapter we reviewed recent progress in thermal management applications of graphene focusing on our results for graphene laminate as a conductive coating material [1], free-standing reduced graphene oxide as strongly anisotropic conductive pad material [2], and magnetically functionalized graphene as self-aligning fillers for thermal interface materials [3].

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Chapter 28 Design and Development of Stress-Engineered Compliant Interconnect for Microelectronic Packaging



Lunyu Ma, Suresh K. Sitaraman, Qi Zhu, Kevin Klein, and David Fork

28.1 Introduction

Power and latency are fast becoming major bottlenecks in the design of highperformance microprocessors and computers. Power relates to both consumption and dissipation, and therefore, effective power distribution design and thermal management solutions are required. Latency is caused by the global interconnects on the IC (integrated circuit) that span at least half a chip edge due to the RC (resistance-capacitance) and transmission line delay [1]. Limits to chip power dissipation and power density and limits on hyper-pipelining in microprocessors threaten to impede the exponential growth in microprocessor performance. In contrast, multi-core processors can continue to provide a historical performance growth on most consumer and business applications provided that the power efficiency of the cores stays within reasonable power budgets. To sustain the dramatic performance growth, a rapid increase in the number of cores per die and a corresponding growth in off-chip bandwidth are required [2]. Thus, it is projected by the Semiconductor Industry Association in their International Technology Roadmap for Semiconductors (ITRS) that by the year 2018, with the IC node size shrinking to 22 nm by 2016 and 14 nm by 2020, the chip-to-substrate area array input-output interconnects will require a pitch of 70 μ m [3]. Furthermore, to reduce the RC and transmission line delay, low-K dielectric/Cu and ultra-low-K dielectric/

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Year of production	2014	2015	2016	2017	2018	2019	2020
DRAM ¹ / ₂ -pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC metal 1 (M1) ¹ / ₂ -pitch	28	25	22	20	18	16	14
(nm) (contacted)							
MPU physical gate length (nm (µm))	11	10	9	8	7	6	6
Wire bond pitch – single in-line (μm)	20	20	20	20	20	20	20
Flip chip area-array pitch (µm)	80	80	80	80	70	70	70

Table 28.1 ITRS 2005 roadmap for assembly and packaging [3]

The bold highlights the pitch reduction in electronic packages, especially flip chip

Cu interconnects on silicon will become increasingly common. In such ICs, the thermomechanical stresses induced by the chip-to-substrate interconnects could crack or delaminate the dielectric material causing reliability problems (Table 28.1).

Flip chips with solder bumps are being increasingly used today to address these needs due to their several advantages: higher I/O density, shorter leads, lower inductance, higher frequency, better noise control, smaller device footprint, and lower profile [4]. Flip chips on board (FCOB) are gaining increased acceptance both for cost-performance and high-performance applications. Epoxy-based underfills are often used in such FCOB assemblies to accommodate the coefficient thermal expansion (CTE) mismatch among different materials (e.g., silicon IC on an organic substrate) and to enhance the solder joint reliability against thermomechanical fatigue failure [5, 6]. However, additional underfill process steps, material and processing costs, reworkability, delamination, and cracking are some of the concerns with the use of underfills. Also, as the pitch size decreases, the cost and the difficulties associated with underfill dispensing will increase dramatically [7, 8]. Conductive adhesives are an alternative given the move of industry to lead-free solders, but processing difficulties restrict them to low I/O density applications.

Furthermore, when low-K dielectric (ultralow-K dielectric in the future) is used in the IC and when such ICs are assembled on organic substrates, the chip-to-substrate interconnects are subjected to extensive differential displacement due to the CTE mismatch between the die and the substrate under thermal excursions. The interconnects, especially stiff solder bumps, could crack or delaminate the low-K dielectric material in the die. On the other hand, if the solder bumps are not underfilled, they will fatigue crack and fail prematurely. Therefore, it is necessary to explore alternate interconnects that are compliant so that they will not crack or delaminate the low-K dielectric, that will not fatigue fail prematurely without an underfill, that are easy to fabricate and assemble using existing infrastructure, that they are scalable, that are wafer level, and that will meet the electrical, thermal, and mechanical requirements for next-generation microsystems.

28.2 Literature Review on Compliant Interconnects

With the advent of the area array packages and the increasing concern of thermomechanical reliability, a promising solution is to increase the mechanical compliance of interconnect to accommodate more differential displacement due to the CTE mismatch. There are several different types of the first-level compliant interconnects already available in commercial market or currently under development. In this section, each of them will be briefly reviewed.

Tessera's compliant µBGA[™] technologies have been developed since 1995 [9, 10]. The fundamental structure elements of μ BGATM are shown in Table 28.2. The metal compliant interconnects (or ribbons) are formed by patterning the metal layer on a flexible organic tape. Then the compliant interconnects are bonded to the die and vertically expanded into the free-standing positions by injecting the low-modulus elastomer layer between the die and the flexible tape. The solder joints are bumped on the other side of the flexible tape. One of the advantages of this technology is that all the fabrication processes can be made on the wafer level. Therefore, the fabrication cost and time per unit can be significantly reduced. WAVETM (Wide Area Vertical Expansion) technology is the second generation of compliant package from Tessera. The low-modulus compliant layer absorbs the majority of package deformation caused by CTE mismatch. Thus, the stresses on the solder balls are reduced. This reduced stress level eliminates the need for an underfill [11]. However, since the similarity between this technology and TAB, only peripheral array can be achieved. The pitch size and the I/O density are limited. Additionally, the dispensing of elastomer layer will induce more cost and time.

MicroSpringTM interconnect has been developed by FormFactor Inc. The 3D microspring interconnects are formed in out-of-the-plane direction using wire bonding method as shown in Table 28.2. Each microspring is formed first, by placing a specially designed and shaped wire bond at the desired location and then plating up the wire bond, transforming it into a spring. The plating alloy provides the spring strength, while a finish layer of gold ensures a stable electrical contact [12]. The MicroSpringTM technology offers low normal force, fine pitch, high pin count arrays, and no underfill, all of which are needed for current and future microelectronic packaging [13]. However, due to the limits of the wire bonding process, the pitch size is limited to be in the range of 100 μ m. Another drawback is that, since the fabrication is a sequential process, therefore, the high cost and the long fabrication cycle need to be improved.

The Interconnect Focus Center (IFC), Georgia Institute of Technology, has proposed a compliant interconnect structure called Sea of Leads (SOLs) [14–16]. It enables a compliant wafer-level packaging (CWLP) at low cost. In the fabrication, a layer of overcoat polymer is deposited over a patterned sacrificial polymer. The sacrificial polymer is later thermally decomposed to form the air gaps in the overcoat polymer. The air gaps can enhance the vertical compliance of the leads. The curved Au leads are then patterned by photolithography and deposited by electroplating. The fabrication of SOLs is compatible with standard IC fabrication. It can achieve small pitch size and does not need an underfill material for thermomechanical reliability.

Helix interconnect is a spiral compliant interconnect that is under development at the Computer-Aided Simulation of Packaging Reliability (CASPaR) Lab, Georgia Institute of Technology [17–19]. The fabrication is based on the MEMS-type high aspect ratio via formation and electroplating. The structure is built up layer by layer.

Technology and company name Illustration Attributes µBGA® and WAVE® (Tessera) * S-shaped Cu/Au ribbon [9–11] solder ball bonds package + No underfill substrate interconnect + Batch fabrication layer + Reliable flexible link Elastomer encapsulating on-chip - Limited planar Al circuits compliance silicon chip MOST® (FormFactor) [12, 13] * Au wire bonds + No underfill + Good compliance Serial fabrication – Limited pitch and interconnect size Sea of Leads (SOLs) (IFC, * Electroplated Au lead Georgia Tech) [14–16] * Low-modulus polymer with air gap + No underfill + Batch fabrication - High-temperature processing - Limited in-plane compliance Helix Interconnects (CASPaR, * Electroplated Cu Georgia Tech) [17–19] interconnect * Layer-by-layer fabrication + No underfill + Batch fabrication + Good planar and out-ofplane compliance + Varying compliance designs

Table 28.2 Summary of current compliant off-chip interconnect technologies

The geometry of each layer is designed on each photolithography mask. First, the cavity of the first layer is formed in photoresist by photolithography. The metal is then grown in the cavity by electroplating. After the first layer is finished, a same process is repeated for the second layer, and so on. The solder material and its barrier layer can be deposited in the electroplating of the last layer. Finally, after all layers are formed, the photoresist is removed by dry-etching process and the structure becomes free-standing. The helix-type structures can be achieved through the wafer-level fabrication. The fabrication processes are completely compatible with the standard IC processes. Photolithography enables the control of fine pitch and small dimension during the fabrication. Due to the good mechanical compliance, the underfill material is not required to relieve the thermally induced stress/strain concentration in the structure. Both the vertical and in-plane compliance of the helix-type interconnect can be greater than 10 mm/N [17]. A modified version of the helix interconnects called *FlexConnects* that requires less number of masking steps is also under development [20].

28.3 Stress-Engineered Compliant Interconnects

This chapter presents the fabrication and design of stress-engineered compliant interconnects. The fabrication of the stress-engineered compliant interconnect is based on the standard IC fabrication and stress-engineering theory. The primary goal of stress-engineered compliant interconnects is to achieve higher compliance than the conventional C4 solder joints and obtain an improved thermomechanical reliability. The stress-engineered, compliant interconnect for high-density application, developed by a consortium of Georgia Institute of Technology, XEROX Palo Alto Research Center (PARC) and NanoNexus, Inc. [21, 22], is innovative and uses the intrinsic stress gradient induced during the DC sputtering deposition to create the compliant structure.

28.3.1 Fabrication of Stress-Engineered Compliant Interconnects

Stress-engineered compliant interconnects are fabricated using processes such as DC sputtering, photolithography, and wet etching, which are highly compatible with the front-end (IC) processes in semiconductor industry. The fabrication can be done in an area array format at the wafer level and has important advantages. First, the interconnect fabrication can be easily integrated into the standard semiconductor front-end processes. Additionally, the area array wafer-level fabrication of interconnect can greatly reduce the fabrication cost per unit and fabrication time and is highly

consistent with the wafer-level packaging (WLP). Finally, the standard IC fabrication enables the good control of interconnect geometry and pitch size.

Hoffman and Thornton [23] reported the stress-engineering process in the thinfilm metals that the intrinsic stresses can be gradually transitioned during DC magnetron sputtering by changing the sputtering condition, such as the argon (Ar) pressure. The impurities/atomic peening model and the grain boundary (GB) relaxation model were used to explain the stress-engineering effect [24]. Smith and Alimonda [21] first reported the fabrication of the stress-engineered compliant interconnects with 80 μ m pitch for microelectronic packaging applications.

A detailed description of fabrication process is given here. A schematic picture of fabrication processes is shown in Fig. 28.1. A bare wafer is used as the substrate for the compliant interconnect fabrication. A thin layer of titanium (Ti), about 0.5 μ m, is deposited on the substrate using DC sputtering. It is known that Ti has good interfacial adhesion with most of the materials used in IC fabrication, especially between the metals and ceramics. Therefore, the Ti layer can prevent the highly stressed thin-film metal layer from undesired peeling-off during the fabrication processes. The Ti layer is also called the release layer or the adhesion layer.



Fig. 28.1 Fabrication process of stress-engineered compliant interconnect

A layer of $Mo_{80}Cr_{20}$ alloy (by weight) thin film, 1.5 µm, is sputtered onto the Ti layer. During the DC sputtering process, the argon pressure is carefully manipulated to obtain the desired intrinsic stress conditions. At low argon pressure (less than 0.5 Pa), the possibility of collision between target metal atoms and argon atoms is low. The target metal atoms can be deposited in a condensed formation on the substrate due to less scattering effect. Thus, the interatomic distance between two neighboring metal atoms is smaller than the equilibrium distance. In this case, a compressive intrinsic stress is present in the sputtered metal layer. On the contrary, if the argon pressure is higher (greater than 0.5 Pa), the chance of collision between target metal atoms and argon atoms is higher. The target metal atoms are deposited in a coarse formation, and thus a tensile intrinsic stress (attractive interatomic force) is present in the deposited metal layer. The intrinsic stress magnitude can be varied from -1 GPa at the bottom of the Mo_{80} - Cr_{20} layer to +1 GPa at the top of the $Mo_{80}Cr_{20}$ layer, by gradually changing the argon pressure. The intrinsic stress gradient throughout the thickness can form an intrinsic up-bending moment.

In order to achieve a very uniform intrinsic stress gradient throughout the whole substrate, a rotational planetary system is used in the sputtering tool. The thin-film metals used in stress-engineered compliant interconnects are deposited in a sputter deposition system in which substrates travel on a planetary system. Analogous to the motion of celestial bodies, the substrates revolve around their own centers, as the substrate also orbits the center of the deposition system. The sputter gun, which holds the metal target for deposition, is typically located on the orbit of the substrate's center.

Although Mo_{80} - Cr_{20} alloy has very good mechanical property for the stressengineering application, its electrical property, like the conductivity, is not as good as the electrically conductive materials, such as gold (Au) and copper (Cu). In order to improve the conductivity of interconnect, a layer of Au, usually about 1.0 μ m, is sputtered over the Mo_{80} - Cr_{20} thin film. The lower elastic modulus and the small thickness of Au will ensure that the interconnects remain compliant.

After the DC sputtering, the geometry shape of the stress-engineered compliant interconnects is patterned using photolithography. Thus far, the stress-engineered Mo_{80} -Cr₂₀ layer is held down onto the substrate by the Ti adhesion layer. Next, the stress-engineered compliant interconnect should be released by etching the Ti layer. To prevent the stress-engineered compliant interconnects from peeling off from the substrate, one end of the interconnect structure will be anchored on the substrate by the Ti release layer while the other end is released from the substrate. To have this released structure, release windows are to be defined using a second photolithography process.

A layer of photoresist is first dispensed on the substrate wafer. The photoresist is patterned to create release windows for the stress-engineered interconnects. The anchoring end is still encapsulated in the photoresist to protect the underlying Ti layer from etching away. A selective etching solution is used to remove only the Ti layer within the release window. After the wet etching, the stress-engineered compliant interconnect is released from the substrate wafer and curls up automatically due to the relaxation of its intrinsic stress gradient, as seen in Fig. 28.1.



Fig. 28.2 Scanning electron microscopy (SEM) pictures of stress-engineered compliant interconnect arrays at 6 µm and 80 µm pitches

Following the release process, the rest of photoresist on the substrate is stripped away.

Figure 28.2 presents stress-engineered compliant interconnects fabricated at $6 \mu m$ pitch and $80 \mu m$ pitch. These interconnects are called linear or straight interconnects, as their unreleased geometry is along a straight line.

28.3.2 J-Spring Compliant Interconnects

The linear spring discussed thus far has excellent out-of-plane compliance. However, the in-plane compliance, especially along the axis of the linear spring, can be enhanced by suitable design modification. Accordingly, a new structure, called a "J-spring," is designed, with a *J*-like shape in the unreleased stage. The J-spring has both good in-plane compliance and excellent out-of-plane compliance. The J-spring compliance can be altered by changing various geometric parameters such as the length of the linear segment (*L*), the width (*W*), the inner radius of arc segment (*R*), and the subtended angle of arc segment (α), as illustrated in Fig. 28.3. An array of fabricated J-springs with a subtended arc angle of 90° is also shown in Fig. 28.4.

28.4 Compliance Analysis

The compliance of linear spring and J-spring was computed using a finite-element model. In the model, the substrate was modeled as a rigid substrate, and the released spring geometry was obtained starting with the residual stress gradient in the sputtered metal. A force load was then applied to the free end of the released spring geometry, and the compliance in the force direction was calculated as the ratio





Fig. 28.4 SEM image of released J-springs



between the displacement and the force in the same direction. Compliance analysis was carried out by changing the various geometry parameters of the spring structures. For the linear spring, the geometric parameters that can be changed are the length and the width of the spring. For the J-spring, the geometric parameters that can be changed are the length, width, arc radius, and the subtended angle. For the sake of brevity, selected results are presented here. Additional details can be found in [25]. Figure 28.5 shows the variation of compliance with the linear spring length,



Fig. 28.5 (a) In-plane and (b) out-of-plane compliance variation with length for the linear spring

and Fig. 28.6 presents J-spring compliance variation with the inner radius of the arc segment.

It is seen that the curves of the X and Y compliance are almost parallel to each other, or the magnitudes of the increase are about the same. Nevertheless, because L can also contribute to the Y compliance, thus the Y compliance is always larger than the X compliance in this case. The maximum Y compliance is about four times



Fig. 28.6 (a) In-plane and (b) out-of-plane compliance variation with radius for the J-spring

larger than its original value, while the maximum of the X compliance is about eight times larger than its initial value. This is because the Y compliance value is influenced by L and R, while the X compliance is primarily influenced by R. Although the Z compliance magnitude and rate of increase are much higher than the planar compliance, its maximum value is still approximately four times larger than its original value, similar to the Y compliance. When only R increases, it increases not only the moment arm but also the release height. Because of these effects, R also has significant influence on the J-spring compliance.

28.5 Compliant Interconnect Assembly Process

The thermomechanical reliability of compliant interconnects is assessed through accelerated thermal cycling tests. Test vehicles of stress-engineered compliant interconnect arrays were fabricated and assembled. Optoelectronic devices, such as the high-density vertical cavity surface-emitting laser (VCSEL) array, will be one of the important applications for this interconnection technology [26], so the pitch size of the stress-engineered compliant interconnects was designed to be 21 μ m in the test vehicle. The width of the linear compliant interconnects is 17 μ m. The compliant



Fig. 28.7 Test vehicle layout. (a) Zoomed-in schematic of horizontal array. (b) Zoomed-in schematic of vertical arrays

interconnects were fabricated on transparent substrates, such as quartz and glass. The test vehicle layout is given in Fig. 28.7.

In the test vehicle, there is one long horizontal array of compliant interconnects oriented along X direction in the center, and six short vertical arrays oriented along Y direction with some offset from X axis. The metal traces are fanned out from the compliant interconnects to the probing pads on the edges of the test vehicle. Between every two adjacent probing pads, the compliant interconnects form a daisy chain with the bonding pads on the die. A complete daisy chain loop between every two adjacent probing pads is called a channel. In the horizontal array, there are 11 channels with 100 compliant interconnects in each channel. Each vertical array is a channel containing about 110 compliant interconnects. Due to their small size, the compliant interconnects and bonding pads are also shown in Fig. 28.7.

The compliant interconnects were assembled on substrates using two different techniques. (1) The compliant interconnects were in sliding contact with the bonding pads, and the substrate was held in place using adhesive at the corners. (2) An underfill was used to assemble the substrate on the die. Both of these two assembly processes can be carried out at room temperature and thus can eliminate thermal expansion-induced misalignment between the interconnect and the bonding pad. The assembly processes use UV curing resulting in short assembly time.

28.5.1 Sliding Contact Package

The substrates with the released stress-engineered compliant interconnects and die are cleaned before assembly. After rinsing in acetone, methanol, and isopropyl alcohol, the substrate and die are cleaned in oxygen plasma to remove organic contamination. As shown in Fig. 28.8, the quartz substrate with the compliant interconnects is first mounted onto the stationary stage and held by the vacuum. Before the silicon die is mounted onto the movable stage, a UV-curable adhesive is applied to four corners of the rectangular silicon die. After the die is mounted, a coarse alignment is performed so the compliant interconnect tips do not contact the bonding pads. The compliant interconnects and bonding pads are registered with the aid of two alignment marks. After the coarse alignment, the substrate is moved down toward the die to make electrical contact between the compliant interconnects and the bonding pads. The movement is controlled to avoid over-flattening by observing the optical image through the microscope. At the same time, a fine alignment is performed to ensure the electrical contact. During the downward movement, the adhesive applied onto the die is also touching the substrate.

Once the fine alignment is completed, a UV light is shined over the assembly for 1-2 min to register the final position. The intensity of UV exposure is 70 mW/cm². In this assembly, the compliant interconnect tips contact the bonding pads without any encapsulation. Therefore, they can slide freely on the pads.



28.5.2 Non-soldered Underfilled Package

The second method of assembly deals with underfilling of the interconnects to make contact between the interconnects and the bonding pads. There are two methods to assemble using an underfill, capillary underfilling assembly, and no-flow assembly.

The capillary underfilling assembly is similar to the free-air sliding contact assembly. After the final registration with UV exposure, an underfill material is dispensed along one or two edges of package. Under capillary force, the underfill flows into the gap between the die and the substrate and encapsulates all compliant interconnects. A second UV exposure is done to cure the underfill.

In the no-flow assembly, a transparent UV-curable underfill is used to comply with the optical alignment. The underfill is first applied onto the die before



alignment. After the coarse alignment, the substrate is moved toward the die and the compliant interconnects are pressed into the underfill. The fine alignment is conducted as the compliant interconnects are completely immersed into the underfill. After the fine alignment, the package is exposed to UV radiation. The UV intensity is about the same as that used in the free-air sliding contact package. The exposure time is about 3 min. The assembly process is schematically shown in Fig. 28.9.

28.6 Accelerated Thermal Cycling Test of Underfilled Package

After the assembly, the packages were thermal cycled to assess their thermomechanical reliability. Prior to thermal cycling, the electrical resistance of different daisy chains was measured at room temperature. This electrical resistance was taken as the baseline resistance. The air-to-air thermal cycling test was based on JESD22-A104-B [27]. Based on the test standard guidelines, the maximum dwell temperature (T_{max}) was selected to be 125 °C, which was lower than the glass



Fig. 28.10 Resistance change with temperature during thermal cycling. (a) 30–125 °C. (b) –55 to 125 °C

transition temperature (T_g) of the underfill. Two temperature ranges were initially selected for the thermal cycling tests; one was from 30 to 125 °C, and the other was from -55 to 125 °C. The temperature ramping rate was 15 °C/min. The dwell time at the maximum and minimum temperature was 10 min each. The electrical resistance was measured as the thermal cycling test was conducted to assess the thermomechanical reliability. The resistance change in the accelerated thermal cycling tests are summarized below:

The electrical resistivity of a metal changes with temperature (T), with the thermal coefficient of resistivity (TCR) of pure metals typically about 4×10^{-3} K⁻¹, and generally lower for alloys [28]. From the data in Fig. 28.10, the TCR (α) can be estimated as

$$\alpha = \frac{\Delta R}{R_0 \cdot \Delta T} \approx 1.2 \times 10^{-3} \sim 2.0 \times 10^{-3} / \mathrm{K}$$

where

 α - thermal coefficient of resistivity (TCR)

 R_0 – the electrical resistance at room temperature in the beginning of experiment ΔR – increase in electrical resistance from the lowest to the highest temperature ΔT – temperature range of the thermal cycle

As seen, the measured TCR is within the range reported by others.

The average electrical resistance decreased gradually in the first several cycles of test. As seen in Fig. 28.11, this decrease was prominent in the first 1500 min (about 50 cycles). But as the thermal cycling test continued, the rate of decrease became less and less, and finally the electrical resistance value stabilized. This trend was observed in both the horizontal and vertical channels. There are two possible reasons to explain the initial decrease of the electrical resistance with the thermal cycling tests: (a) With thermal cycling, the underfill continues to cure further, shrink, and bring the substrate and the die together more. This can potentially increase the contact area between the compliant interconnect and the bonding pad and thus will decrease the electrical resistance. (b) Due to the differential expansion of various materials during thermal cycling, the interconnect tips flex and scratch the die pad surface to make better electrical contact between the compliant interconnect and the compliant interconnect and the die bonding pad. Therefore, the electrical resistance will be lowered. The observed resistance decrease during the first few cycles can be termed as "burn-in."

Another characteristic of the "burn-in" is that it occurs irreversibly in the thermal cycling test, even if there is an interruption. Figure 11 shows the electrical resistance change in a thermal cycling test with an intentional interruption of a few hours between the first 2500 min (80 cycles) and the next 1500 min (40 cycles). As seen, the electrical resistance remains unchanged during interruption of thermal cycling and continues to decrease once the thermal cycling is resumed during the burn-in phase.

28.7 Thermal Cycling of Free-Air Sliding Contact Packages

To prevent the deterioration of electrical connection in free-air sliding contact packages from contamination, the packages were tested in a sealed container. The test results are similar to those obtained from the non-soldered/underfilled packages. When the pads were examined after thermal cycling, scratch marks were seen on the



Fig. 28.11 "Burn-in" behavior of resistance. (a) First 80 cycles. (b) From 80 to 120 cycles after interruption at 80 cycles

gold bonding pads, as shown in Fig. 28.12. On each pad, there are two scratch marks. These marks are caused by the tips of the compliant interconnects scrubbed on the pads and have the same width as the stress-engineered compliant interconnects, located at the contact regions on the pads.

The cause of these scratch marks can be explained as the following. There were two types of mechanical loads applied along the contact interfaces between the compliant interconnects and the bonding pads. The first load is compressive in the vertical direction (normal to the bonding pad surface) caused by the compression of



Fig. 28.12 Scratch marks on Au bonding pads (by SEM)

the substrate toward the die in the assembly operation. The second load is in tangential direction, parallel to the pad surface. This load is caused by the differential displacement due to the coefficients of thermal expansion (CTE) mismatch in the packages at a temperature different from the stress-free condition. In the thermal cycling test, the tangential load is cyclic and leads to gradual degradation of contact integrity. Once the conductive material between the compliant interconnect tips and bonding pads is completely or partially worn out, the channels in the free-air sliding contact package fail.

28.8 Nanocantilever Fabrication for Sensing Applications

Thus far, we have discussed the application of stress-engineering principle to microscale interconnects. Now, we will discuss the potential extension of this to nanoscale sensing devices. In the ongoing work, we use electron-beam lithography and lift-off processes to fabricate the nanocantilever arrays. Lift-off processes have the capability to provide high-fidelity patterns with very fine features. These processes work well with unidirectional deposition methods that do not provide significant sidewall coverage, such as filament or e-beam evaporation. Sputter deposition, which is capable of providing a high internal stress gradient, is multidirectional, provides sidewall coverage, and therefore complicates the lift-off processes. The sidewall coverage in the sputter deposition process is due to the fact that the sputtered atoms deposit randomly at various angles on the rotating substrate. Two lift-off methods are being pursued for the fabrication of stress-engineered cantilevers: a single-layer resist approach and a bilayer resist approach, as illustrated in Fig. 28.13. Prior to spinning the resist, a sacrificial metal layer is deposited that will later be selectively etched to release the patterned cantilever. The bilayer process uses a thin layer of PMMA (polymethyl methacrylate) resist spun over a thicker base



layer of MMA (methyl methacrylate) resist. The single-layer process uses only a positive resist, e.g., PMMA. In both processes, the total resist height to deposited metal height is desired to be 7:1 or greater; a ratio less than 7:1 makes the lift-off process difficult [29].

As illustrated in Fig. 28.13, on a bare wafer (a), a thin layer of release metal is first deposited (b). In the single-layer process, PMMA is spun on the wafer, patterned, and developed. In the bilayer process, a thick layer of MMA is spun on the wafer, followed by a thinner layer of PMMA (c). After patterning of the bilayer with e-beam lithography tool, the MMA base layer is undercut during developing, due to greater exposure sensitivity as compared with the PMMA top layer (d). In both the single-layer and bilayer resist cases, the cantilever metal film, Cr, is deposited with intrinsic stress (e). Lift-off is performed using acetone in an ultrasonic bath. For
smaller aspect ratios, a mechanical polish, e.g., a gentle wipe with an acetone soaked wiper, is needed to complete lift-off (f). Once the spring metal deposition is complete, a second layer of resist is spun and patterned to define a release window, which allows the selective etching the release layer (g). After selectively etching the release layer, the stressed metal stack curls up to form a free-standing cantilever (h).

28.8.1 Fabrication Results

The pattern illustrated in Fig. 28.14 was investigated. The pattern consists of a series of cantilevers, 10 μ m in length, that vary in width from 10 to 100 nm in steps of 10 nm and from 100 to 1000 nm in steps of 100 nm, where each width is repeated five times. Two layers of chromium sputtered at a low and a high argon pressure were used to fabricate the cantilevers in thicknesses varying from 25 to 250 nm. In some cases, a thin gold layer <50 nm was deposited on the top surface of the cantilevers, and this gold layer could be used to increase surface's binding affinity for proteins and antibodies.

Thin-film deposition was performed using PVD-300 Unifilm[™] magnetron sputter system, which is capable of routinely and reproducibly depositing very uniform (>99%) and homogeneous films. A computer-controlled planetary system with two degrees of freedom (orbit and spin) is used in conjunction with a calibration of the deposition rate with respect to position. Calibrated intrinsic stress versus Ar pressure for Cr sputter film is shown in Fig. 28.15. Although stress is primarily dependent on the Ar pressure, stress values showed a slight variation depending on the deposition power. The stress measurements in Fig. 28.15 were performed by measuring the curvature of standard 4″ Si wafers, before and after the deposition of a stressed metal of a particular film thickness [30]. From Fig. 28.3, it can be seen that Unifilm is capable of developing only tensile stresses for Cr, and therefore, the cantilever stress gradient is developed by depositing two layers with an increasing magnitude of tensile stress.

Figure 28.16 illustrates selected images of nanocantilevers after the release layer is selectively etched. The images were taken with a video microscope, Fig. 28.16a, and SEM, Fig. 28.16b. As seen, the nanocantilevers curl up as designed.





Fig. 28.15 Intrinsic tress versus Ar pressure for sputter-deposited Cr



Fig. 28.16 Video microscope (a) and SEM (b) images of the released free-standing nanocantilevers

28.9 Summary

The stress-engineered compliant interconnect is a novel technology that is based on the thin-film metal deposition by DC magnetron sputtering with an engineered stress gradient through the thickness of the thin film. Because of its photolithographybased fabrication, the stress-engineered compliant interconnect can satisfy the finepitch requirement for high-density chip-to-next-level interconnection in the nextgeneration microelectronic packages. Additionally, its fabrication process is compatible with the front-end wafer-level IC fabrication processes. The interconnect's good mechanical compliance and high release clearance enable new packaging configurations, such as non-soldered packages and the free-air sliding package. The non-soldered and free-air sliding contact packages can greatly reduce the process time and cost. They are also consistent with the trend of environmentally friendly packaging. Another potential advantage is that the proposed process steps do not involve high temperature which might damage the IC devices and induce excessive thermal stresses.

The compliance of the interconnect is important for the thermomechanical reliability, as it can accommodate the differential displacement caused by the CTE mismatch. The linear stress-engineered compliant interconnect can provide an excellent out-of-plane compliance that can meet the compliance requirement of the first-level interconnect, while the in-plane compliance is limited and has a strong orientation dependence. In order to improve the in-plane compliance, an alternate stress-engineered compliant interconnect, called "J-spring," has been designed and fabricated. The "J-spring" has been proposed to have a spiral free-standing structure after releasing, which can provide a better in-plane compliance than the linear stressengineered compliant interconnect.

Two assembly processes have been developed for the stress-engineered compliant interconnect package without using solder: One is a non-soldered/underfilled package, and the other is a free-air sliding contact package. The assembly has been conducted on a customized optical alignment assembly station with five degrees of freedom and with submicron accuracy. Both of these two assembly processes can be conducted at room temperature, without the potential damage to the IC devices and package. The UV curing can greatly reduce the assembly time. The assembled packages have been subjected to the thermal cycling tests to assess the thermomechanical reliability.

The geometries have been scaled to nanoscale. When bio-conjugated, the nanoscale studies can be used for biosensing applications. Monoclonal antibodies have been immobilized on the nanoscale structures and are intended to detect extremely low levels of circulating antigens associated with human cancer. Thus, microscale and nanoscale structures can be fabricated using stress-engineering principle and can be used for microelectronic packaging, microelectronic probing, biosensing, and other applications.

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Chapter 29 Nanosensors for Electronics Package Reliability



James E. Morris

29.1 Introduction

A primary problem in modern packaging technology, e.g., flip-chip attachment, is thermomechanical stress and the resulting failures by loss of adhesion, solder fracture, etc. In other technologies, accumulated plastic strain in isotropic conductive adhesive joints, for example, may be the source of failure. In monitoring such effects, whether for research or in situ, the measurement is typically indirect or requires bulky apparatus in a laboratory setting. There is a need for a small-scale, high-gauge factor sensor, which can be integrated on chip or board. Such a device could be useful in many locations on or within a package, even to detect popcorning, for example.

Corrosion is another issue in many packaging applications, potentially wherever an interface between dissimilar metals is subject to humidity. The generic corrosion reaction releases hydrogen, and early onset of corrosion may be detected by a sufficiently sensitive detector of this by-product.

The concept of a specialized chip which could monitor package parameters of interest was developed some years ago by Sandia Labs [1-3]. However, the proposition here is to use nanoscale sensors which would take up negligible-on-chip real estate for production devices, even for many sensors distributed over many locations. (There may be need for on-chip sampling electronics, to provide a serial output to minimize I/O count overheads.)

The discontinuous metal thin film (DMTF) is one of the simplest sensor structures possible. It consists of an array of metal nanoparticles which conducts current between two electrodes, with resistance at absolute temperature T

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$$R = R_0 exp - \delta E/kT$$

with activation energy δE where *k* is Boltzmann's constant. The structure can be thought of as an array of multiple coulomb blocks, and indeed the simplest "array" of one island is a coulomb blockade device (which could also function as a sensor).

29.2 The Nanodot Coulomb Block and Discontinuous Metal Thin Films

Metal nanoparticle applications are proliferating, in nanoelectronics, for example, in some single-electron transistor (SET) configurations [4, 5], and in nanoelectronics packaging [6, 7]. Some applications will operate with only a single-nanoparticle island, others with a 1-D line of islands, and more in regular or random 2-D discontinuous metal thin-film (DMTF) arrays or in the 3-D "cermet" variant, where the nanoparticles are encased in polymer or ceramic. The generalized ellipsoidal shape of the nanoparticle shown in Fig. 29.1 is the minimal energy configuration of a charged island [8, 9] or can be a transient non-equilibrium form due to growth from a substrate adatom population [10]. Electronic conduction between contacts and nanoparticles, or between islands, is by quantum mechanical tunneling [11, 12], with probability proportional to

$$exp - (2m\Phi)^{\frac{1}{2}}(4\pi d/h)$$

where d is defined by Fig. 29.1, m is the electron mass, Φ is the effective tunneling barrier height, and h is Planck's constant, and with an associated electrostatic activation energy (assuming contact angle $\theta \approx 180^{\circ}$) at field E_a [8, 13]:



Fig. 29.1 The geometry of two ellipsoidal nanoparticle islands of eccentricity $\ell = (1 - (t/r)^2)^{V_2}$ [11, 13]

$$\begin{split} \delta E &= q^2/C = (q^2/4\pi\epsilon R_{rd})(2/\ell)[\sin^{-1}\ell - \sin^{-1}(\ell(1-p)/(1+p))]/(1-p) - qR_{rd}E_a\\ \text{for } E_a &< E_{amin} = (q^2/4\pi\epsilon R_{rd})4p(1+p)^{-1}\Big[(1+p)^2 - \ell^2(1-p)^2\Big]^{-\frac{1}{2}}, \end{split}$$

where q is the electronic charge, C is the island capacitance, $p = d/R_{rd}$, and $R_{rd} = 2r+d$,

and
$$\delta E = (q^2/4\pi\epsilon R_{rd})(2/\ell)[\sin^{-1}\ell - \sin^{-1}(\ell(1-p)R_{rd}/((1-p)R_{rd}+2x))]/(1-p) - qE_ax/p$$

for $E_{amin} < E_a < E_{amax} = (q^2/4\pi\epsilon R_{rd})4p(1-p)^{-2}(1-\ell^2)^{-\frac{1}{2}}$,
where $x = \frac{1}{2}R_{rd}\ell(1-p)\left\{\left[\left(\left[\left\{2qp/\pi\ell E_a(1-p)^2R_{rd}^2\ell^2\right\}^2 + 1\right]^{\frac{1}{2}} + 1\right)/2\right]^{\frac{1}{2}} - \ell^{-1}\right\}$
and $\delta E = 0$ at $E_a = E_{amax}$,

which corresponds to the 0° K coulomb block (SET) threshold condition. In a DMTF of N₀ nanodots,

$$N_0 exp - \delta E/kT$$

are randomly charged at any time at equilibrium, and a single-coulomb block (SET) nanodot is charged

$$exp - \delta E/kT$$

of the time, washing out the abrupt threshold at finite T [14]. The consistent observation of larger conductances in DMTFs than this traditional model predicts has been explained by a contact injection model [12, 15], which also accounts for the diode effect in asymmetric films [16] and for anomalous AC results [17, 18], including pseudo-inductance and switching effects [19, 20].

A great deal of past experimental work on the stability of nanodot characteristics in DMTF applications is directly applicable to more recent nanoelectronics applications.

DMTFs are readily formed in the early stages of nucleation and growth of noble or refractory metal films (Au, Ag, Pt, Pd, W, Mo,) on insulating substrates, by physical vapor deposition in vacuo, the key element being a weak atom-substrate interaction. DMTFs consist of discrete metal islands, of dimensions in the 2–10 nm range, separated by inter-island gaps of 2 nm or more. These parameters can vary considerably, especially with substrate temperature. The lack of DMTF stability and reproducibility has been an impediment to successful commercial development in the past.

29.3 Strain Effects

In all applications, the nanodot system will sit on some form of substrate, with electrical connections to the outside world. Conductance will show a strong negative temperature coefficient but will also be subject to the effects of thermomechanical



stress due to TCE mismatches. It has been shown that thermomechanical stress cannot account for the observed negative TCRs. However, if the film is strained, the increase in gap width, d, produces a significant increase in resistance, due to the exponential tunneling dependence. For a gauge factor, γ , assuming constant δE ,

$$\gamma = (\partial R/\mathbf{R})/(\partial d/\mathbf{d}) = (4\pi/\mathbf{h})(2\mathbf{m}^*\boldsymbol{\varphi})^{\frac{1}{2}}\mathbf{d},$$

order of magnitude calculation gives a gauge factor around 50 for 2 nm gaps, and in fact, gauge factors up to 200 are commonly observed. This model assumes only the tunneling gap contribution, and it has been shown that the activation energy term can have a significant impact too, and the linear variation of γ with d at low strain turns over at higher values [11, 21, 22], due to the predicted δE decrease (Fig. 29.2, [22]) for high eccentricity nanodots with substrate adhesion, as demonstrated in Fig. 29.3 [22]. Gauge factors are enhanced by islands only weakly pinned to the substrate, for which δE increases with strain, as typically observed, but negative gauge factors have also been observed.

The recent upsurge in interest in DMTF strain effects [23–32] is presumably driven by the same potential for strain gauge applications that drove much of the DMTF research in the 1970s. The technology would compete with nanowire-/nanotube-based sensors [33–36] which may be currently more reproducible and stable.

Fig. 29.2 Theoretical δE variations with strain ε , for varying island adhesion and eccentricities [22]



29.4 Ambient Gas Adsorption and the Hydrogen Sensor

The adsorption of air on the nanodot surface changes the work function Φ with time t, and hence tunneling probabilities [37, 38] with a t^{1/2} dependence indicative of substrate diffusion (Fig. 29.4). Other environmental gases have similar effects of R increasing upon exposure to a gaseous environment [39] providing a wealth of opportunities for gas sensing. But the universality of the effect means that an "electronic nose" system would be necessary to resolve detection of any or many specific gases.

The Pd/H₂ system is unique, however, in that a Pd DMTF resistance may decrease in the presence of H₂. The Pd island swells, decreasing gap width, and increasing electron tunneling conduction [40–42]. There is the usual opposite surface effect too, due to the increase of the Pd work function by hydrogen absorption, which is similar to the effect of other gases, so the islands must be designed to be large, with small gaps in order to maximize the unique Pd/H₂ effect. Example results, displaying both effects at different hydrogen concentrations/pressures, are shown in Fig. 29.5.

The importance of hydrogen detection in the packaging context is that H_2 is a by-product of corrosion processes and the H_2 sensor is de facto a corrosion sensor. As for strain gauge research, there has been developing interest in the Pd DMTF H_2 sensor [43–53] or related systems [54–57] with commercial products already on the market [58].



29.5 Postdeposition Resistance Changes, Stability, and Reproducibility

The key to DMTF formation is weak substrate adhesion, which leads to property instability as nanodots drift and coalesce. Typically, higher resistance films will increase R following deposition of a mixed island (TCR < 0) and filamentary (TCR > 0) structure as the island structure becomes dominant, while lower resistance films' resistances decrease further as the filaments grow. The goal of a zero TCR film requires balancing these two competing effects, the classical problem to balance a pencil on its point! [59]. The oblate nanodot shape may not be the stable equilibrium form and may change with time as (a) residual substrate deposited adatoms continue to migrate to the nanodot-substrate interface and (b) the nanodot eccentricity changes with surface self-diffusion away from the high curvature edge (Fig. 29.6 [10]).



Future commercial applications will require fabrication on stable sites, which may be achievable by harnessing the power of the atomic force microscope (AFM). One possible approach is to define such sites by nanoimprinting from a mold defined by AFM oxidation of dots on a Si surface. Another technique for customized



Fig. 29.7 (a) AFM Cr deposition by piezo-drive system control and (b) the deposition model

structures would define stable site locations by field evaporation of Cr dots on an insulating substrate surface, e.g., SiO₂, with subsequent growth of metal islands, e.g., Au, on the Cr sites by thermally controlling the adatom capture distance (diffusion constant.) AFM fabrication of nanoparticles requires the application of sufficient field to the emission tip, so atoms may be stripped from the end as in a field-ion microscope. The properties of Cr as an adhesion promoter for Au are well known. If one can establish small Cr nucleation sites to act as localized condensation centers in subsequent Au deposition, one may also achieve film stability along with reproducibility and structural regularity, (Fig. 29.7.) A 10 nA current (e.g., defined by the diode reverse saturation current) for 10 ns (z-axis pulse) would ideally produce an approximately 3.5 nm diameter hemispherical island. Seed islands of about this dimension on a regular grid would be very appropriate for subsequent deposition of gold or palladium for strain gauge or H₂ sensing applications. The Au or Pd deposition must be made at a temperature for which the island capture distance for adatoms exceeds half the gap between the Cr seed islands. For the H₂ sensor applications, large islands with small gaps are required, the most difficult structure for stability. Preliminary results for AFM deposition of Cr dots (Fig. 29.8 [60]) demonstrate concept feasibility, but these are µm-scale (but nm heights) without the deposition charge control.

29.6 Summary

Nanotechnology can provide the sensors needed to monitor on-chip reliability parameters in the R&D phase and also lifetime prognostics of the chip in the field. The specific examples covered here were the use of nanoparticle/island structured DMTFs for strain sensors and Pd DMTFs for H₂/corrosion sensing. For both, commercialization will require the development of reproducible stable structures, and the possible road via AFM deposition of stable nucleation sites was introduced.



Fig. 29.8 (a) AFM deposited single Cr island and (b) an array of nine Cr dots [60]

A recently developed commercial direct feedback strain sensor to control AFM cantilever bending is based on discontinuous sputtered Ag films [61]. A related family of DMTF sensors has also been demonstrated with gap sizes controlled by the incorporation of organic ligands [62]. These films may be 2D, as the films above, or 3D analogs of cermet structures. Strain sensing has been demonstrated with gauge factors, γ , to about 400 [63]. Temperature and humidity measurement and gas detection are also feasible as for the DMTFs above [64].

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Chapter 30 Application of Bio-nanotechnology to Electronic Packaging



Melinda Varga

30.1 From Bio-nanotechnology to Electronic Packaging

Within the field of electrical engineering, electronic packaging refers to a variety of technologies aiming to the assembly, connecting the components, enclosure, and protective features that assure a reliable functioning of the system or device [1]. Packaging of an electronic system must consider cooling, protection from mechanical damage, radio-frequency noise emission, protection from electrostatic discharge, maintenance, operator convenience, and cost [2]. The electronic products that emerge are similar to the human body. They have "brains" or microprocessors, and packaging provides the skeletal and the nervous system of the product. Packaging is needed for the electronic system to be interconnected, powered or fed, cooled via its circulatory system, and protected via its skeletal system. However, if we take a closer look to the human body and its components, one can state that they are composed of cells, i.e., unique, functional, self-sustaining units, each being built up of tiny structures called organelles and further down from molecules of nanometer size that perform various tasks contributing to the integrity and activity of the cell.

Nanotechnology has now evolved into a branch of science that aims at manipulating matter at very small, i.e., 1–100 nm, scale, which involves atoms and molecules with applications in the fields of electronics, medicine, material science, energy production, and even consumer products [3].

These nanometer-sized biological molecules not only inspire nanotechnology for technologies not yet created, but they are also an important source of potential templates for the production of such nanoscale structures and devices. This is how bio-nanotechnology has been born.

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Bio-nanotechnology analyzes the biological processes at nanoscale, e.g., proteins that self-assemble or mechanosensing (how cells sense and respond to a mechanical stimulus), the structure and function of nanomachines found in living cells such as the ATP synthase (a nanomotor that provides the living cells with energy), and the inherent properties of DNA and lipids to build nanodevices with applications in engineering and medicine [4–9]. Bio-nanotechnology seeks to modify, to find, as well as to create new technological uses of the biological principles and biological molecules and their properties through nanotechnology.

Now how can bio-nanotechnology relate to or aid electronic packaging?

The fundamental technologies behind today's electronic products such as computers, smartphones, automobiles, and medical devices are based on microsystems and electronic packaging technologies. Four technology waves (microelectronics, RF/wireless, photonics, and MEMS) made this possible [10]. MEMS are the fourth technology wave and the next step in the silicon revolution.

MEMS denote *microelectromechanical systems* in the USA and are integrated mechanical and electromechanical devices, structures, and elements of micrometer size produced through microfabrication techniques. In Europe, MEMS are known as *microsystems technology* (MST) and in Japan as *micromachines* [11].

MEMS technologies date back to a paper by Smith published in 1954 in the Physical Review journal. In his paper, Smith described for the first time the piezoresistive effects in silicon and germanium [12]. Starting from the first silicon diaphragm pressure sensors and strain gauges through commercialized pressure sensors in the 1960s, MEMS devices have advanced from simple structures with no moving elements to high-performance electromechanical systems with several moving parts controlled by integrated microelectronics and responding to various physical variables like pressure, motion, radiation, flow, etc. [13–15]. Examples include accelerometers, pressure and chemical flow sensors, micromirrors, gyroscopes, fluid pumps, and inkjet print heads [16-22]. Recently, biomedical or biological microelectromechanical systems (BioMEMS) have shown excellent applications in the field of medicine, biotechnology, rehabilitation, healthcare, sports science, as well as environmental sensing [23–29]. BioMEMS are highly promising from both research and industrial points of view for advanced diagnosis, therapy, and tissue engineering strategies and sensing (biomolecules like DNA and RNA, proteins, viruses, and other microorganisms) (Fig. 30.1).

MEMS devices are faster, smaller, lighter, and usually more precise and are fabricated using semiconductor device manufacturing technologies [30]. This implies techniques like bulk micromachining or surface micromachining of silicon-based MEMS, resulting, for instance, in low-cost accelerometers that are implemented in the air-bag systems of automobiles [31, 32]. Basic fabrication processes include the deposition of material layers (thin films), patterning by photolithography, and subsequent etching to obtain the desired shapes and elements [30]. In addition to silicon, metals, ceramics, and polymers are frequently used [33]. However, in most cases, MEMS components need to be electronically packaged for proper functioning. That is, the electrical and mechanical components need to be integrated into a system for a specific application in a way that it

Fig. 30.1 Optical MEMS gas sensor. (Image provided, courtesy of GasSecure)



satisfies the cost, performance, and reliability requirements. These components need to be assembled and interconnected, energy must be supplied, and adequate heat removal needs to be achieved. The MEMS package needs to provide mechanical support, protection from the environment, electrical connections, and reliable functioning [10].

MEMS packaging differs from other packaging of microsystems in a way that requires application-specific packaging. MEMS do not contain generic elements or universal building blocks. MEMS components are sensors, actuators, and electromechanical or microfluidic devices that require heterogeneous integration. All these components cannot be fabricated on a common substrate but each of them can be separately and then assembled to build up an operating MEMS.

One of the most common assembly and packaging methods is pick-and-place. This technique consists of removing a component from its packaging materials and mounting it onto a printed circuit board (PCB). The process involves the following steps: board indexing, board registration/alignment, component presentation, component pickup/extraction, component centering, component placement, and board removal [34]. Although this method has demonstrated accuracy and reliability for large component scales satisfying consumer electronics, it is challenged with a trade-off between throughput and accuracy of placements. Besides, pick-and-place functions in a serial manner, is time-consuming and expensive, and needs closed-loop control, and as device sizes shrink, stiction becomes a problem (when devices are smaller than 300μ m) [35] (Fig. 30.2).

Bottom-up nanotechnology often refers to the emerging use of self-assembly to position nanoscale structures or elements and construct multimolecular assemblies on the nanometer scale [36]. Self-assembly is a process of ordered, spontaneous organization of system components into functional structures or patterns as a consequence of the interaction between the components themselves without any external intervention [37]. It is a parallel process where the components themselves are contacted by a tool, i.e., picked up and placed, and yield and throughput are quite high. Especially biological systems are an important source of inspiration on how successfully self-assembly is implemented in nature. Consequently, bio-nanotechnology can aid or relate to electronic packaging.



Fig. 30.2 The Atoz PP-050 automated pick-and-place device. (Image provided, courtesy of Apex Factory Automation)

30.2 Application of Bio-nanotechnology to Electronic Packaging

For bio-nanotechnology, self-assembling molecules provide a toolkit. Molecules that arrange autonomously into a defined structure without any external intervention contribute to the process called molecular self-assembly. This process plays a pivotal role in living organisms as it aids in constructing molecular assemblies of different topologies and genuine machines that are important to the proper functioning of living cells. The assembly of molecules is directed through non-covalent interactions (e.g., hydrogen bonding, van der Waals forces, hydrophobic interactions, metal coordination, π - π , and electrostatic interactions) and electromagnetic interactions [38]. For instance, the planar bilayer of phospholipids in cells can self-assemble into micelles or a liposome [39]. The DNA molecule, a nucleic acid that stores the genetic information employed in the development and reproduction of viruses and all living organisms, is self-assembled from two biopolymer strands giving rise to a coiled coil structure [40]. The two strands are built up of nucleotides, which instead are connected by hydrogen bonds [41]. Only in this form, the DNA molecules become functional and able to encode information which can be translated into protein sequences. Inside cells, a typical DNA molecule can be as long as 2 m. This would indeed not fit into the cell nucleus if it would not be highly organized, i.e., packaged into structures called chromosomes [42]. Plus, it can be twisted in a process termed supercoiling [43].

Similarly, the newly formed polypeptide chains need to self-fold and accommodate distinctive patterns in order for a protein to be functional. Protein folding is dominated by the hydrophobic effect, and it is specified by the sequence pattern in their primary sequence with most of these consisting of hydrophobic or polar amino acids. For example, alternation of hydrophobic and polar amino acids in a primary



Fig. 30.3 (I) Phospholipids in cells can self-assemble into micelles. (II) Amino acids in a primary sequence might fold into α -helical structures or β -conformations. (III) The structure of a microtubule and its subunits. (**a**) Atomic structure of tubulin (PDB file 1TUB). (**b**) Tubulin dimer formed from a very tightly linked pair of α - and β -tubulin monomers. (**c**) The tubulin heterodimers self-assemble to form protofilaments. (**d**) Microtubule assembly from protofilaments. (Image modified from [45])

sequence results in β -conformations, while hydrophobic residues spaced three and four residues apart yield α -helical structures [44] (Fig. 30.3).

Furthermore, the α - and β -subunits can attach to each other and form dimers. For instance, the α - and β -subunits of the protein tubulin occur/exist as dimers. Furthermore, these dimers are able to self-assemble (polymerize) end to end and organize into linear filaments. Thirteen of these filaments associate laterally to generate a

pseudo-helical arrangement named a microtubule [46]. Microtubules are long, hollow structures implicated in a number of crucial cellular processes. They are involved in the intracellular transport and movements of organelles and vesicles inside the cells and contribute to the maintenance of the cell structure and shape as well as mitosis and meiosis (cell division) [47–50]. Microtubules aid in the motility of cells by being the major components in the cilia and flagella, protrusions, or flexible membrane extensions that propel cells achieving velocities of 1 mm/s [51]. Interestingly, motor proteins that utilize the energy from ATP hydrolysis like kinesin "walk" on microtubules, transporting vesicles and molecules from one side of the cell to another [49]. Microtubules are imperative in the development of the nervous system in higher vertebrates [52].

Surface layer proteins (S-layers), one of the most commonly observed envelope structures on the surfaces of certain bacterial cells, have as well the remarkable property of self-assembling into regularly ordered protein lattices with repetitive physicochemical properties down to the nanometer scale [53]. For instance, the S-layer of *Sporosarcina ureae* ATCC 13881 is characterized by identical protein subunits that assemble into lattices exhibiting square symmetry, meaning four monomers building up one unit cell [54]. The monomers are non-covalently linked to each other, through hydrogen bonds, salt bridges, ionic bonds, and hydrophobic interactions. Hence, by applying a chemical treatment, monomers are able to reassemble into mono- and multilayers not only in solution but also on solid substrates such as silicon wafers [55] (Fig 30.4).

Although self-assembly is an inherent property of the protein monomers, in vitro, the initial monomer concentration, the presence of Ca^{2+} ions, and substrate properties will strongly influence the shape and size of the protein layers formed [55]. Allowing an adequately long time for the recrystallization, tube formation occurs, which is hollow, open-ended, and in the case of the S-layer of *Sporosarcina ureae* ATCC 13881 measuring between 1.1 and 4.5 µm in length [55]. The folding

Fig. 30.4 On silicon wafers, the native S-layer of *Sporosarcina ureae* ATCC 13881 monomers are able to reassemble into mono- and multilayers. When the layers are large enough, due to an intrinsic curvature, they fold into a tube



Fig. 30.5 Fusion of streptavidin (another protein) to the S-layer protein of *Sporosarcina ureae* ATCC 13881 monomers does not impair self-assembly. The genetically modified protein molecules self-assemble into mono-and multilayers on silicon wafers



of the protein into tubes happens on the axis parallel to the layer edges [55]. The tubular shape is advantageous because it provides access to three contact regions: the outer and inner surfaces and to both ends.

By genetic engineering, self-assembling proteins can be enriched with additional properties, for instance, with a specific ligand (another molecule)-binding function. Modifications have to be performed at the DNA level, and the final protein is produced in a bacterial system, the most widely used being *E.coli*. But will the freshly produced and now modified protein monomers still self-assemble at all? What will be the final shape of the protein lattices? Will they be mono- or multi-layered protein layers?

Notably in the case of modifying the S-layer of *Sporosarcina ureae* ATCC 13881 by fusing streptavidin, a small biotin-binding protein to the monomers, experiments have shown that these were still able to self-assemble into mono- and multilayers with sizes ranging from 200 nm to 1 μ m [55] (Fig. 30.5). This certifies the fact that the self-assembly characteristic of the S-layer protein was not impaired by the genetic modification and upon addition of the new protein part [55].

On a plane silicon wafer, the modified S-layer protein forms mono-and multilayers [55] and by this remarkable property, the protein can be considered a functional biomolecular matrix for immobilizing biotinylated particles or molecules in a controlled manner and defined spacing since the lattice now exposes binding sites for biotin at well-defined distances on a nanometer scale. Streptavidin binds biotin strongly, and the interaction is the strongest non-covalent interaction in nature [56]. Consequently, biotinylated DNA or any other biotinylated moieties such as quantum dots can be immobilized and arranged on this biomolecular matrix. By mixing the modified protein monomers with non-modified monomers, the density of



Fig. 30.6 The genetically modified S-layer protein as a biomolecular matrix for immobilizing biotinylated molecules, e.g., biotinylated quantum dots



Fig. 30.7 Hybrid S-layer structures. The modified and non-modified S-layer monomers were co-crystallized. Afterward biotinylated quantum dots were adsorbed onto the resulting protein lattice. (Adapted from [55])

the biotin binding sites can be custom arranged and controlled according to the stoichiometry of the components (Fig 30.6).

This phenomenon, giving rise to hybrid assemblies, could have important applications, e.g., as an interface in biosensor elements or as building blocks in the fabrication of novel nanoelectronic circuits. First attempts to produce such hybrid assemblies have been encouraging. The modified S-layer monomers were mixed in a 1:1 ratio with non-modified monomers. Then biotinylated quantum dots were adsorbed onto the protein layers formed in order to analyze the distribution pattern of the two different proteins in the hybrid protein structure. Fluorescence microscopy has revealed that a mixing of the modified and non-modified proteins indeed took place on silicon wafers [55] (Fig. 30.7).

The structures resulted have a well-defined shape, and the deposition of quantum dots seems to be more accentuated laterally on the protein lattices. However, for a precise pattern elucidation, a higher-resolution method would be necessary.

In electronic packaging, interconnections are necessary between an integrated circuit (IC) and its packaging, and to this end wire bonding is a very common method used. Wire bonders are manually operated, semiautomatic, or fully



Fig. 30.8 Two-dimensional schematic representation of self-wiring of SslA-streptavidin modified protein

automated machines of size up to 18" deep \times 19" wide \times 12" high and weight at least 60 lb [57]. In the so-called thermosonic bond process, the machine uses a combination of heat, pressure, and ultrasonic energy to create a weld between the gold/copper ball and the aluminum/copper bond pad on the chip surface. The wires are as small as 15 µm in diameter. If now one would consider the S-layer protein matrix with the exposed binding sites for immobilizing biotinylated DNA at certain distances or positioned laterally so that the strands can be stretched and coupled to a gold electrode surface, a self-wiring process would occur. The DNA molecules at one end biotinylated, on the other thiolated, and in addition metallized would constitute a much thinner wire, i.e., of nanometer size (diameter of the DNA helix is 2 nm) that self-connects to an electronic surface (Fig. 30.8). Presently no tool can achieve interconnections that are nanometers in size.

As illustrated above, starting from simple building blocks like amino acids or proteins, nature successfully uses self-assembly and self-organization to build complex, functional structures, and machines and engineers can learn from it. Inspired by self-assembly or self-folding, engineers at John Hopkins University in USA have designed and fabricated surgical tools, i.e., microgrippers that enter the bloodstream and perform surgery by excising tissues [58]. The tissue retrieved with the help of the microgrippers was then used for genetic diagnostics (RNA and DNA analyses), as well as for cytologic analyses. These biocompatible, minimally invasive, and autonomous microtools that are capable of removing cells from tissue samples were designed after the joints of arthropods (meaning invertebrates like spiders, shrimp, or lobster) and fabricated from bilayers of Cr/Cu thin-film sheets subsequently patterned with Ni and a polymer trigger. Upon heating or exposure to chemicals (e.g., body fluids), self-folding or closing of the gipper occurred which was driven by the release of residual tensile stress within the metal thin film developed due to mismatch of the coefficient of thermal expansion (CTE) of the bilayer materials [59]. In order to operate in vivo, the microgrippers need magnetic resonance imaging or computed tomography for guidance and can be heated wirelessly by using electromagnetic fields. With these tether-less, metallic microgrippers, high-quality tissue samples were successfully extracted and analyzed without using any invasive surgical tools [58].

While all examples of self-assembly or self-folding enumerated here were based on the aggregation of similar parts to each other, the integration of heterogeneous microsystems involves different types of components as is often the case in MEMS packaging. Self-assembly works very well in liquid environments; however in the case of MEMS, this can be damaging, the structures often being sensitive to fluids or hygroscopic (retaining water). In order to avoid this, dry self-assembly approaches have recently emerged [60]. They imply part-to-template or part-to-part self-assembly based on stochastic assemblies; on geometrically defined and preconditioned template, the parts are fed stochastically, and the mobility of the parts is assured by vibrations of the template which are externally induced [61].

In conclusion, self-assembly proves to be an efficient and promising technology for nanoscale assembly. Involving various embodiments and driving forces, it has the potential to evolve into a technology that can be adopted in nanoelectronic packaging and eventually for integrating heterogeneous microsystems (e.g., miniature MEMS devices that cannot be integrated otherwise). A more extended knowledge and experimental information would however aid not only in more widespread applications but also in their more rapid embrace by industry.

Glossary

- **ALPHA HELICAL STRUCTURE** a common secondary structure of proteins, a right-hand-coiled or spiral conformation (helix).
- **AMINO ACID** a biologically important organic compound which is the building block of proteins.
- **ARTHROPODS** Animals having an external skeleton and a segmented body.
- **ATP** adenosine triphosphate, a molecule that transports chemical energy within cells for metabolism.
- **ATP SYNTHASE** an enzyme (biological molecule) that creates adenosine triphosphate (ATP).
- **BETA CONFORMATION** second form of secondary structure of proteins, strands are connected by hydrogen bonds.
- **BIOMEMS** Biomedical or Biological Micro-Electro-Mechanical Systems (MEMS).
- **BIOSENSOR** it is an analytical device that combines a biological component with a physicochemical detector.
- **BIOTIN** is a water-soluble B-vitamin (vitamin B₇).
- **BIOTINYLATED PARTICLES** particles conjugated to vitamin B_7 (see BIOTIN).
- **BODY FLUID** are liquids originating from inside the bodies of living humans, for example, blood and saliva.
- **CELL** the basic structural, functional, and biological unit of all known living organisms. It is the smallest unit that can replicate independently, often named also "building blocks of life."
- **CHROMOSOME** it is a packaged and organized structure containing most of the DNA (deoxyribonucleic acid, see below DNA) of a living organism.
- CILIA thick protuberances that project from the cell body (see CELL definition).

- **CYTOLOGIC ANALYSES** assessment of cells to diagnose, for instance, certain diseases.
- DIMER a chemical structure formed from two similar subunits.
- **DNA** deoxyribonucleic acid, a molecule which contains the biological instructions that make organisms unique.
- **E. coli** *Escherichia coli* (abbreviated as *E. coli*) are bacteria found in the environment, foods, and intestines of people as well as some animals.
- FLAGELLA a whip-like structure that allows a cell to move.
- **GENETIC ENGINEERING** the modification of an organism's genetic material by artificial means.
- **INVERTEBRATES** are animals that do not possess and develop a vertebral column.
- **KINESIN** a protein belonging to a class of motor proteins found in living cells. Kinesin moves along microtubule filaments being powered by the adenosine triphosphate (ATP).
- **LIGAND** in biochemistry and pharmacology, it means a substance that forms a complex with a biomolecule to serve a biological aim.
- **LIPID** a chemical substance insoluble in water but soluble in alcohol. Lipids are an important component of living cells. Cholesterol, for instance, is a lipid.
- **MEIOSIS** process by which chromosomes are copied, paired up, and separated to give rise to eggs or sperm.
- **MEMS** denote micro-electro-mechanical systems in the United States and are integrated mechanical and electro-mechanical devices, structures, and elements of micrometer size produced through microfabrication techniques.
- **MITOSIS** part of the cell cycle in which chromosomes in a cell nucleus are separated into two identical sets of chromosomes.
- **MOLECULE** the smallest particle in a chemical element or compound that has the chemical properties of that element or compound. Molecules are made up of atoms that are held together by chemical bonds.
- **MONOMER** a molecule that binds chemically to other molecules to form a polymer.
- **NERVOUS SYSTEM** part of an animal's body that coordinates its voluntary and involuntary actions and transmits signals to and from different parts of its body.
- **NON-COVALENT BOND** a type of chemical bond that occurs typically between macromolecules. It is used to bond large molecules such as proteins and nucleic acids.
- **NUCLEOTIDE** one of the structural components of DNA and RNA. A nucleotide consists of a base (one of four chemicals: adenine, thymine, guanine, and cytosine) plus a molecule of sugar and one of phosphoric acid.
- **ORGANELLE** in cell biology, an organelle is one of several structures with specialized functions.
- **PHOSPHOLIPID** consists of two hydrophobic fatty acid "tails" and a hydrophilic "head," joined by a glycerol molecule.
- **POLYMERIZATION** is a process of joining monomer molecules together in a chemical reaction to form polymer chains or three-dimensional networks.

- **PROTEIN** large biomolecules consisting of one or more long chains of amino acids.
- **RESIDUE** here refers to an amino acid within a peptide (biologically occurring short chains of amino acid monomers) chain.
- **RF** denotes radio frequency, any of the electromagnetic wave frequencies that lie in the range from around 3 kHz to 300 GHz.
- **RNA** ribonucleic acid, a molecule implicated in various biological concerning certain DNA fragments.
- STREPTAVIDIN protein purified from the bacterium Streptomyces avidinii.
- SUPERCOILING refers to the over- or underwinding of a DNA strand.
- **THIOLATION** introduction of sulfur units into a variety of structures, for example, protein or DNA.
- **TISSUE** in biology, *tissue* is a cellular organizational level between cells and a complete organ.
- **TISSUE ENGINEERING** refers to the practice of combining scaffolds, cells, and biologically active molecules into functional tissues.
- **VERTEBRATES** an animal category that includes bodies with a stiff rod running through the length of the animal named also vertebral column.
- **VESICLE** in cell biology, it refers to a small structure within a cell, consisting of fluid enclosed by a lipid bilayer.
- **VIRUS** a small infectious agent that replicates only inside the living cells of other organisms.
- **QUANTUM DOTS** semiconductor particles that confine electrons or holes in all three spatial dimensions.

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Chapter 31 Flip-Chip Packaging for Nanoscale Silicon Logic Devices: Challenges and Opportunities



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Acronyms

BGA	Ball Grid Array
BOM	Bill of Materials
BPA	Bisphenol-A
BW	Bandwidth
C4	Controlled Collapse Chip Connection
CG	Coarse-grained
CNT	Carbon Nanotube
CPI	Chip Package Interactions
CPU	Central Processing Unit
CSAM	C-Mode (Confocal) Scanning Acoustic Microscopy
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
CVFF	Consistent Valence Force Field
DEM	Discrete Element Model
DFT	Density Functional Theory
DIP	Dual Inline Package
DPD	Dissipative Particle Dynamics
DRAM	Dynamic Random Access Memory
EM	Electromagnetic
EMC	Epoxy Molding Compound

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EMIB	Embedded Multi-Die Interconnect Bridge
EPN	Epoxy Phenol Novolac
FCBGA	Flip Chip Ball Grid Array
FCC	Face-centered cubic
FCIP	Flip Chip in Package
FCLGA	Flip Chip Land Grid Array
FCPGA	Flip Chip Pin Grid Array
FET	Field Effect Transistor
FIVR	Fully Integrated Voltage Regulator
FLI	First Level Interconnect
FOPLP	Fan-Out Panel Level Package
FOWLP	Fan-Out Wafer Level Package
GPU	Graphics Processing Unit
HMC	Hybrid Memory Cube
HSIO	High Speed Input/Output
HVM	High Volume Manufacturing
IC	Integrated Circuit
IHS	Integrated Heat Spreader
ILD	Inner Layer Dielectric
I/O	Input/Output
IOT	Internet of Things
KGD	Known Good Die
LGA	Land Grid Array
LJ	Lennard-Jones
LOFP	Low-profile Quad Flat Package
MBVR	Mother Board Voltage Regulator
MCP	Multi-Chip Package
MD	molecular dynamics
MM	molecular mechanics
MMAP	Molded Matrix Array Package
MOSFET	Metal-Oxide-Semiconductor FET
NEMD	Non-Equilibrium Molecular Dynamics
NPU	Network Processing Unit
NPT	Isothermal-isobaric ensemble (conservation of substance amount N.
	pressure P and temperature T)
NVT	canonical ensemble (conservation of substance amount N, volume V
	and temperature T)
PBC	Periodic Boundary Conditions
PBGA	Plastic Ball GA
PCB	Printed Circuit Board
PCFF	Polymer Consistent Force Field
PDN	Power Delivery Network
PGA	Pin Grid Array
PoP	Package on Package
PTH	Plated Through Hole
OFJ	Ouad Flat J-Leaded Package
<u> </u>	_

QFN	Quad Flat Package No Lead
QFP	Quad Flat Package
RC	Resistance x Capacitance (time constant)
RDL	Redistribution Layer
RF	Radio Frequency
RH	Relative Humidity
RT	Room Temperature
SAC	Tin-Silver-Copper (Sn-Ag-Cu)
SAP	Semi-Additive Process
SCSP	Stacked die Chip Scale Package
SI	Signal Integrity
SiP	System in a Package
SLI	Second Level Interconnect
SoC	System on a Chip
SOJ	Small Outline J-Leaded Package
SOP	Small Outline Package
SRAM	Static Random Access Memory
SSOP	Shrink Small Outline Package
TCB	Thermo-Compression Bonding
TCP	Tape Carrier Package
TDP	Thermal Design Power
Tg	Glass Transition Temperature
TIM	Thermal Interface Material
TQFP	Thin Quad Flat Package
TSOP	Thin Small Outline Package
TSV	Through Silicon Via
UBM	Under Bump Metallization
VdW	Van der Waals
VHR	Voltage Holding Ratio
VR	Voltage Regulator
WLCSP	Wafer Level Chip Scale Package
WLP	Wafer Level Package
ZIP	Zig-Zag Inline Package

31.1 Introduction

Silicon features, which have continued to scale with Moore's law [1], reached the nanoscale in the early 2000s. In the second decade of this millennium, a number of technology innovations are helping drive these features to 10 nm and below [2, 3]. The first logic products with 90 nm transistors, using traditional silicon dioxide insulators and polysilicon gates, went into volume production in 2003. In 2007, 45 nm devices, using a revolutionary high-k metal gate transistor technology, were introduced [4, 5]; in 2012, the first 22 nm 3-D FinFETs were introduced [6], and in



Fig. 31.1 Number of connected things/devices worldwide 2015–2021. (Source: Berg Insight (from Statista https://www.statista.com/))

2014, they were followed by 14 nm devices based on the second generation of FinFET technologies [7]. These nanoscale devices enable higher performance circuits which in turn drive the need for advanced features in packaging. In addition to device performance improvements, new and emerging applications of semiconductor devices and the increased proliferation of Internet of Things (IOT) devices (Fig. 31.1) will require innovative packaging to support the demands of power delivery, high-speed signaling, efficient cooling, and variable form-factor requirements. Figure 31.2 provides a visual description of the proliferation of package types over time.

In the early days of the semiconductor integrated circuit (IC) industry, microelectronics packaging primarily provided space transformation and structural and environmental protection of the small but expensive devices so that they could be connected to relatively large electronic system boards. The role of microelectronics packaging has continued to expand over the past few decades, to include electrical and thermal performance management of semiconductor devices, as well as enabling system miniaturization. Reducing the cost of packaging and also meeting challenging new environmental regulations have been critical engineering requirements during this evolution.

In this chapter we examine the evolving importance of packaging technology and describe some of the challenges and opportunities specifically for flip-chip packaging¹ [8] of nanoscale devices. We first describe the evolution of space transformation requirements in packaging. This is followed by discussions on package-level power

¹Although there is a considerable amount of active research in non-solder-based area array interconnects, solder-based flip-chip interconnects are currently the most widely used die-to-die and die-to-package interconnects, for a variety of reasons including ease of manufacturing, interconnect compliance that reduces stress on the silicon backend layers, etc. In this chapter focus is restricted to packaging of nanoscale devices using solder-based flip-chip interconnects.


Fig. 31.2 Schematic showing the proliferation of package form factors. (Source: https://www.techsearchinc.com/)

delivery challenges, package architectures and characteristics needed to enable highbandwidth interconnects, package-level thermal management, and the impact package feature scaling has on the structural integrity of the silicon. Finally, scaling of package features to enable form-factor reductions is reviewed.

Materials technologies play a significant role in packaging. Performance requirements, such as thermal management, power delivery and signal integrity, as well as structural integrity and environmental and manufacturing considerations, have been enabled by significant improvements in materials technologies. This trend is expected to continue with progress along Moore's law and with the continued divergence of system form factors. The role and influence of materials technologies needed to meet electrical, thermal, manufacturability, reliability, and environmental requirements are discussed in the subsequent sections.



Fig. 31.3 Schematic showing the vertical interconnects within and between stacked dice. The image shows the HMC memory interconnect. (Source: Micron Corp.)

31.2 Space Transformation

One primary function of the package in an electronic system is to provide costeffective space transformation. The package transforms the high density of terminals on the small expensive IC chip to a lower density of terminals on the larger, lowercost, package body. The lower-density package terminals match the minimum feature sizes of the low-cost system board. Thus, the package becomes a key element for the interconnection between silicon ICs and components on the system board. There are other important interconnect functions in a package. Broadly, package technologies and assembly processes enable five distinct classes of interconnects:

- (a) *3D die-die interconnects*: Interconnects between stacked die² that enables vertical interconnects between multiple dice in a 3D stack (Fig. 31.3).
- (b) *Die-to-package interconnects*: Interconnects between the die and the package, typically known as the first-level interconnect (FLI)
- (c) 2D die-die interconnects: Interconnects between dice within the package that enable lateral connections, referred to as die-to-die package routing
- (d) *Within-package interconnects*: Interconnects within the package that enable lateral connections between two nodes or electrodes
- (e) *Package-board interconnects*: Interconnects between the package and the next level, which is typically the mother board, referred to as the second-level interconnect (SLI)

²Focus on this chapter will be restricted to area array interconnects and will not cover wire-bonded interconnects in 3D die stacks.

There has been continued increase in the interconnect count with every succeeding product generation. This is due to the inclusion of more functionality on the chip, higher data bandwidth between chips, and the need for smaller variation in supply voltage for the chip. The increased interconnect count leads to scaling of feature sizes across all domains of packaging [9].

31.2.1 3D Die-Die Interconnect

Projections in the 2013 edition of International Technology Roadmap for Semiconductors [10] show the pitch of the 3D die-to-die interconnect scaling down to 10 µm.³ The Hybrid Memory Cube (HMC) [12] multi-die stack, where four DRAM dies are stacked on top of a logic controller at a die-to-die interconnect pitch of 40 μ m, is shown in Fig. 31.3. Chip attach at reduced pitches⁴ in die-die interconnects is easier than the equivalent die-to-organic package attach for FLI interconnects. This is because the coefficients of thermal expansion (CTEs) of the two dice are better matched, and this leads to reduced misalignment in the attach process. Typically die-die interconnects are solder based (Fig. 31.3) since the solder compliance offers process flexibility and greater tolerance for misalignment and lack of coplanarity during interconnect formation. Interconnect formation at sub-10 µm pitches using solder has been demonstrated [14]. However, as the interconnect pitch shrinks, there is a corresponding reduction in solder volume and an increasing need for carefully chosen under-bump metallization (UBM) to minimize intermetallic formation and retain the solder compliance advantage. Intermetallic formation in solder is due to temperature exposure during the solder deposition and chip attach processes [15]. Alignment tolerances and process design are critical with fine-pitch interconnects [14]. Cu-Cu and other alternate bonding techniques are under active investigation as eventual replacements for solder-based interconnects [16].

As the interconnect pitch shrinks, the gap between bumps reduces, making it more difficult for deflux processes to clean the spaces between bumps and for epoxy underfill processes to adequately fill the chip gaps. These difficulties have spurred investigations into alternate underfill processes⁵ that use epoxy flux dispense or epoxy films integrated applied before the TCB process [17].

Underfill requirements needed to ensure continued interconnect scaling include:

(a) For capillary and mold underfill: Deflux processes that can effectively clean reduced chip gaps and developing underfill materials with (i) the right flow

 $^{^3}$ Although the source is somewhat dated, it is the last time a formal pitch scaling target was published. As of 2017, the lowest pitch in commercially available stacked memories is 40 μm [11].

⁴Thermal compression bonding (TCB) is the most common method of chip attach for fine-pitch die-die interconnects [13].

⁵These processes are also referred to as No-Flow processes. The underfill and flux materials as integrated together and the underfill and chip attach processes are integrated as well [17].



Fig. 31.4 Examples of flip-chip C4 joints. (a) High-lead die bump with eutectic Pb-Sn solder. (b) Cu die bump with SnAgCu solder

characteristics for void-free filling of small chip gaps and (ii) the right thermomechanical materials properties (modulus, CTE, T_g) that ensure joint integrity. Since fillers are used to modulate underfill viscosity and mechanical properties, there is great interest in fine-sized fillers that can be integrated in the underfill epoxy matrix to help tailor properties and ensure fine gap filling.

(b) For pre-dispensed underfill: The TCB process is a short-duration process that involves rapid changes in temperature and pressure [18]. Key challenges in integrating the underfill process with the TCB process involve tailoring the flux content, filler content, curing and viscosity characteristics of the underfill materials such that the material enables void-free joint formation without filler entrapment and then cures sufficiently to ensure joint integrity.

31.2.2 Die-to-Package Interconnects

The FLI interconnection is typically made by a process called controlled collapse chip connection, or C4 (Fig. 31.4 shows typical FLI joints). In the original version of C4, solder bumps on the die were aligned on top of corresponding metal pads of a ceramic package and were then reflowed to form joints with a controlled standoff height [8, 19]. A variation of this chip joining process (referred to as flip-chip interconnect in the literature) is predominantly used for organic packaging and connects high melting point or non-melting die bumps to re-flowable solder bumps on the package substrate. Initially, die bumps for organic packages used high-melt (non-melting) Pb-Sn solder (3-5% Sn and 97-95% Pb) with a melting temperature near 312 °C. The substrate bumps used eutectic Sn-Pb solder with a melting temperature of 183 °C (Figs. 31.4 and 31.5). Environmental considerations



Fig. 31.5 Minimum FLI pitch trend for Intel microprocessors

limiting the use of Pb resulted in the use of materials such as copper die bumps and SnAgCu (SAC) substrate solder [5].

The increased number of terminals for a given chip size requires a reduction in the FLI pitch in order to accommodate all the required bumps. Figure 31.5 shows minimum FLI bump pitch trend for Intel microprocessors. Finer bump pitch reduces C4 joint size and typically the space between the joints, creating FLI-related technology challenges. During the package assembly process, fine bump pitches require advanced equipment and material to precisely place the die and hold it in place until the C4 joints are formed. The smaller joint size reduces the solder volume and consequently the amount of solder collapse during the chip join reflow process. This requires good coplanarity for die bumps and for the mating package substrate contact area to reduce the risk of electrically open C4 joints.

Similar to the issues covered in the previous section, fine bump pitches also impact the choice of underfill material and process due to the reduction in the voided region between the C4 joints and the reduction in vertical space between the die and the package. These reduced spaces restrict the size of the filler particles, which are used in the underfill material to lower its coefficient of thermal expansion (CTE)⁶ and to increase its fracture toughness. Also, the narrow spacing reduces control over the underfill flow dynamics, since the flow speeds may become more sensitive to manufacturing and design variations. Therefore, a finer bump pitch makes optimization of underfill process and material properties more challenging. At the same time, the narrow width of the flip-chip joints makes the FLI less tolerant to any voids and other defects, which may lead to increased material migration between neighboring joints [17].

The small C4 joints need to support high current densities through them. These high current densities are a result of increasing total IC power supply current (even at

⁶Underfill CTE is modulated by filler content and tailored to minimize thermomechanical stresses.

iso-power consumption due to decreasing device voltages) and/or due to nonuniformity of on-chip current driven by variation in activity levels of devices at different locations on the die. If not addressed properly through design, material and process choices for the FLI, and the high current density, in the presence of high silicon chip temperature, may lead to electromigration-driven open failures [20].

Another important consideration for the design of the C4 joint is its influence on thermomechanical stresses in the on-chip interconnect. Over the past few generations, silicon process engineers have focused on reducing the dielectric constant of the dielectric material (low-k) used in the on-chip interconnect to help reduce power. This has also resulted in lowering the mechanical strength of the silicon chip backend layers making it more susceptible to failures induced by thermomechanical stresses due to packaging. The C4 joint needs to be compliant enough to minimize packaging-induced stresses on the silicon.

In summary, the material and process choices for the first-level interconnect need to ensure assembly process scalability to smaller dimensions while still providing compliancy between the silicon and the package, managing high current density through the joint, and being environmentally friendly.

31.2.3 2D Die-Die Interconnects

Connections between dies are a strong function of the interconnect purpose. Most interconnects carry digital signals, and the higher the bandwidth, typically the higher the density of interconnects and package wires. Low-density interconnects (~35 IO/mm and 125 IO/mm²) can be satisfied by standard FLI bumps and package wiring, while very high-bandwidth interfaces can require novel technologies like embedded multi-die interconnect bridge (EMIB) [21] or silicon interposer [22]. The corresponding FLI and package constructions to support these dense 2D multi-chip packages (MCP) create many fabrication and assembly challenges. Challenges in fine-pitch attach have been described in Sect. 31.2.2 and also apply to creating 2D die-die interconnects. Additionally the EMIB technology needs silicon embedding, and the silicon interposer process requires attention to through-silicon via (TSV) integration [23].

31.2.4 Within-Package Interconnects

FLI bump pitch scaling drives the need for finer line width and spacing in order to route the signals from the on-chip terminals to the SLI terminals. The high routing density is typically needed to escape the signal lines out of the congested area near the chip. Before discussing the trend in within-package interconnect, we briefly describe the organic flip-chip package substrate structure. Figure 31.6 shows a



Fig. 31.6 Sketch of a typical organic flip-chip package substrate

schematic of (a) the cross section of an organic flip-chip package substrate, (b) a top view of its primary routing layer, (c) additional details of local routing geometry.

The package substrate is generally built around a core layer⁷ introduced to provide structural rigidity to the package. The core is made up of glass fiberreinforced polymer with mechanically drilled plated through hole (PTH) vias and conducting copper layers fabricated by a subtractive photolithography process derived from widely used processes for printed circuit board (PCB) technology. Typical thickness of the core is in the approximate range of 800–100 µm. Buildup layers are added on both sides of the core layer, one symmetric pair at a time. A buildup layer is typically fabricated by first adding a relatively thin dielectric layer ~ (30-20) µm thick. Then, micro-vias, i.e., sub-75 µm diameter vias, are created by laser or other means. Copper patterns of $\leq 15 \,\mu m$ thickness are then added to form the interconnect layer and via connections to the underlying metal layer. The predominant process for forming the buildup layer conductors is the semi-additive process (SAP). Compared to the traditional subtractive process, SAP enables formation of finer line widths and spaces on the package layers. The buildup layer pairs are sequentially added until the desired layer count is achieved. A protective epoxy solder resist layer is then added to the outer surfaces. This is followed by finish metallization such as electroless NiAu or NiPdAu for the C4 pads on the front side and SLI pads on the backside. Finally, solder bumps are formed on the C4 pads to create an organic FCLGA (flip-chip land grid array) package substrate. To create a FCPGA (flip-chip pin grid array) substrate, pins are soldered to the SLI pads prior to

⁷The cored package technology is described here as a superset of substrate technologies. In recent years, there has been considerable focus on developing thin coreless package substrate technologies that essentially consist only of the dielectric layers [24] and wafer-level fan-out technologies that use wafer-level patterning processes to enable interconnect scaling [25].

chip assembly. For FCBGA (flip-chip ball grid array), solder balls are attached to the SLI pads after chip assembly.

Typically, the C4 pad size is relatively large when compared to routing line width and spacing. A large C4 pad diameter is used for various reasons. A large C4 pad size increases the joint size which, in turn, improves resistance to joint cracking failure. A large pad lowers current density through the joint and enables high current-carrying capability for the C4 joint by lowering electromigration. Also, a large C4 pad allows large solder volume. During the C4 joint formation process, the increased solder volume leads to higher solder collapse and helps achieve a highyielding C4 assembly process. Figure 31.6c shows a representative example of a routing scheme and dimensions for a flip-chip package. Another driver for a large C4 pad is to enable a micro-via to be placed in the center of the pad.

The bump pitch scaling has consistently driven the line width and space to get finer with time, and the trend is expected to continue [9]. Finer features on the substrate bring a host of challenges to package substrate technology. These challenges include technology to maintain adhesion of the resist and conductor materials during the photolithography process and a clean process environment to minimize foreign material related yield and reliability issues. Three different approaches are currently being pursued to get reduced line width and spaces: (a) continued fine-feature patterning of organic substrates [26, 27], (b) use of silicon backend features [21, 22], and (c) wafer- or panel-level fan-out (covered in more detail in Sect. 31.6) [25].

From a different perspective, the demand for fine line and space can be mitigated by aggressive reduction in the micro-via and C4 pad sizes. This would require innovation in substrate technology as well as assembly material and process technologies to produce mechanically robust via and C4 joints with high currentcarrying capability. Innovative design techniques can also mitigate the demand on line and space scaling to some extent. One example of this would be to optimize the bump placement as demanded by high-density routing instead of placing the bumps on a fixed grid pattern.

31.2.5 Package-Board Interconnect

The number of SLI terminals does not have to be equal to the number of FLI terminals, because package routing may combine a group of FLI terminals to a group of SLI terminals based on electrical and manufacturing considerations. There are three major SLI contact technologies in use for flip-chip logic products. These are the pin grid array (PGA), the land grid array (LGA), and the ball grid array (BGA) technologies (Fig. 31.7). The BGA package is directly surface mounted to the motherboard, whereas the PGA or LGA package is inserted in a socket which has been surface mounted to the motherboard. High-end components, like microprocessors, typically use the PGA or LGA package is electrically connected to its socket through a clamping mechanism that makes the individual socket contacts grip the



Fig. 31.7 Flip-chip package types for package-board interconnect

package pins. For the LGA package, electrical connection is made by pressing the package down on to the springlike socket contact probes. Vertical force to maintain this connection is applied by a retention mechanism.

The SLI density has been increasing over time to accommodate larger interconnect count on a given package surface area. The BGA pitch for flip-chip logic products has steadily reduced in time.⁸ This has been achieved by scaling the SLI contact pads and solder ball diameters, changes to solder metallurgy such as various formulations of SAC solder, and managing BGA joint reliability through advanced board assembly processes such as corner glue and other board-level underfill processes. Denser escape routing on the PCB, driven by finer BGA pitch, is enabled by improved design techniques, such as placing the solder balls anywhere on the package, modest reduction in feature sizes of conventional boards, or use of a highdensity board such as those with micro-vias [28] where it is affordable. Typical challenges with finer pitch BGA are board assembly yield, thermomechanical stress from power cycles and temperature cycles, and mechanical shock. Material and design choices have significant impact on BGA joint assembly yield and reliability [29, 30] and are critical to continued BGA pitch shrink.

The PGA pin pitch has reduced from 1.8 to 1.27 mm over the last decade. Further pin pitch reduction is expected to be minimal due to challenges in socket to pin contact technology. On the other hand, the LGA socket connection is more capable of achieving SLI pitch reduction (sub-1.00 mm pitches are possible) due to a simpler

⁸Large packages used in high-performance products use pitches in the 1.00 mm range to pitches in the 0.8 mm range, while smaller packages used in handheld devices have seen pitches as low as 0.4 mm.

contact probe design. Besides the board routing-driven requirements, LGA pitch reduction is generally limited by a minimum required socket contact resistance, maximum retention load capability of the system, and package-socket alignment capabilities. Innovation in material for package land surface finish and the design and material for socket contacts are critical in reducing the contact resistance and the load per contact.

31.3 Electrical Performance

31.3.1 Power Delivery

One of the key requirements for efficient operation of the IC device is to maintain a steady voltage level across the power supply rails. Too low a voltage can lead to erroneous switching of the transistor, causing failure of the entire circuit operation. Increasing the supply voltage to the power rail above the low voltage noise threshold is theoretically a way to mitigate the low voltage-related issues. However, higher input voltages cause higher power dissipation and can have a significant impact on transistor reliability. The requirement to deliver a stable supply voltage with low transient noise has driven power delivery management to become a major discipline within the packaging field, especially for packaging high-performance logic devices such as microprocessors.

The power consumption by the IC is a function of the number of transistors on die, their switching frequency and built-in capacitance, as well as the operating voltage. Even though the current consumed by each individual transistor has reduced with each process node shrink, in the overall IC, current has tended to increase due to increased transistor counts in a chip. This coupled with the increase in core frequency has resulted in a steady growth in power levels for a given chip architecture. In an effort to cap the power levels, microprocessors shifted to a multi-core architecture to improve performance without increase in the number of power rails delivered to the processor. Having a separate power supply for each core or each individual logic block at the lowest possible voltage to ensure error-free operation at the minimum operating frequency for that block. Figure 31.8 charts the increase in the number of power rails with time in Intel microprocessors for client as well as server segments.

To support the trend of increasing power rails without burdening the platform with a large number of voltage regulators (VRs), it is imperative to integrate the VRs in the microprocessor package and die. One way to do this is through the use of on-die linear regulators which was implemented on the IBM Power8[™] processor [31]. One advantage of using linear regulators is the elimination of inductors which makes it attractive for integrating the VR entirely on the chip. However, their poor conversion efficiency makes them suboptimal for all but a handful of rails which



Fig. 31.8 The number of power rails has been steadily going up for both client and server microprocessors



Fig. 31.9 Comparison of VR solutions between 3rd Generation and 4th Generation Intel ® Core ™ microprocessors

carry very little current. To address this issue, Intel[®] introduced the fully integrated voltage regulator (FIVR) [32], a high-efficiency switching regulator that is fully integrated on the microprocessor package and the die, in the 4th Generation CoreTM microprocessor. Figure 31.9 shows a comparison of the VR solutions between the 3rd and 4th Generation CoreTM microprocessors. The FIVR replaces all the platform voltage regulators with a single V_{IN} VR that provides the input supply for the FIVR.

A comparison of the motherboard VR (MBVR)-based power delivery network (PDN) and a FIVR-based PDN is shown in Fig. 31.10. In a MBVR-based design, the role of the package in the PDN is to merely provide a low-resistance path from the platform to the die and provide capacitors for mid-frequency decoupling. However, with the FIVR, the package and the die are tightly coupled as shown in the figure, and it is important for the package and silicon designers to work together to come up

Fig. 31.10 (a) PDN of a MBVR-based design and (b) PDN of a FIVR-based design





with the optimal codesign. In the FIVR, the power FETs, the control circuitry, and the high-frequency decoupling are on the die, while the inductors and the mid-frequency decoupling capacitors are on the package. In order to keep the output filter stage of the switching regulator small enough to fit on the die and package, the FIVR switches at high frequency in excess of 100 MHz. This allows the output filter inductors to be implemented only using the bottom metal layers of a standard flip-chip package, as shown in Fig. 31.11. By utilizing the bigger volume available on the packages, it is possible to design an array of air core inductors that have a high-enough-quality factor to enable efficient operation of FIVR. Aside from eliminating the cost associated with discrete magnetic inductors, package air core inductors have the additional benefit of allowing the designer to choose the precise value, location, and footprint for a given inductor.

The shift to FIVR has been a key enabler in providing the fine-grain power management that is required to improve the performance for a given power envelope. By moving all the VR integration to the die and the package, it also minimizes the platform power delivery area and bill of materials (BOM) cost. As we look ahead to the future generations, we can expect a further increase in current density as the



size of the core and other compute logic blocks get smaller due to device area scaling. As the package inductors that are used in FIVR today are nonmagnetic, the inductance that can be achieved for a given footprint will be limited. This may eventually force us to look at magnetic inductor options in the package as the current density continues to scale.

31.3.2 Signal Integrity

Another key requirement to achieve high performance of the nanoscale electronics is to provide the ICs with adequate data bandwidth to external memory or network interfaces. Increased transistor count, increased frequency, and improved designs, such as multi- and many-core architectures, have been driving the compute performance higher. With the increase in the processing capability of the central processing units (CPUs), the graphics processing units (GPUs), and the network processing units (NPUs), the bandwidth capability of the interconnect links to them needs to also scale accordingly. Figure 31.12 shows trends in display scaling that the mobile platform GPUs need to support and the corresponding increase in the associated switch bandwidth needs for datacenter NPUs [9]. Even though these two system types are on different ends of the spectrum in terms of size, power, cost, and overall performance, it is interesting to note the rapid increases in the growth of the bandwidth demand.

Regardless of application type, typically, bandwidth can be increased by either increasing the single wire data transfer rate or the total input/output (I/O) signal count or both. Going to higher data rates poses significant challenges to package



Fig. 31.12 Scaling of display size and memory bandwidth for mobile GPUs



Fig. 31.13 Scaling of compute power and switch bandwidth for datacenter NPUs

technologies. Some of the key performance metrics to assess the goodness of package signal integrity (SI) are insertion loss, return loss, cross-talk, and the variations in these parameters observed in high-volume manufacturing. At the same time, a typical package I/O net consists of three major sections: FLI which accounts for transitioning from die to package, break-out/fan-out routing in the package which is also simply referred to as routing, and SLI which represents the transition from package to board including BGA balls and socket pins where applicable. Models for the IC drivers and receivers must be paired with the package and system board electrical parameters to accurately predict system performance. The diagram in Fig. 31.14 illustrates some of the interactions between various package technology parameters and the package SI metrics. As seen in this diagram, each section of an I/O package net impacts a number of the SI performance metrics which makes package SI optimization a complex problem. In addition, different I/O



Fig. 31.14 Impact of package technology parameters on SI performance metrics

interfaces that rely on different signaling topologies such as single-endedvs. differential signaling and operate at different frequencies have different sensitivities and requirements in terms of these metrics. Finally, this problem is only exacerbated when the additional boundary conditions for the physical layout design such as x-y form factor, number of routing layers, etc. are also considered.

Tackling the SI challenge of today's complex electronic systems requires a very systematic optimization of the technology parameters outlined in Fig. 31.14 for all key I/O interfaces while considering all crucial physical layout design constraints. Some of the key directions for existing and future package technologies to improve SI performance of two major types of I/O interfaces are summarized below:

- 1. High-speed differential I/O interfaces: These interfaces rely on differential signaling to scale the signaling speed higher while utilizing relatively fewer numbers of lanes to meet the targeted I/O bandwidths. Key package SI metrics of interest are FLI cross-talk, routing loss, routing cross-talk, SLI return loss, and SLI cross-talk. FLI cross-talk is minimized by optimizing the FLI physical layout design (bump assignments, bump pitch, etc.). Routing and SLI cross-talk are also typically controlled through physical layout design optimization. The routing loss is directly correlated to the routing length. However, since the routing length depends on a number of other parameters (package and die form-factor, SLI pitch, etc.), developing lower loss materials has become a very important enabler to reduce the routing loss [33]. Finally, the SLI return loss can be improved by using either finer via/PTH dimensions or larger voiding in the metal layers adjacent to via pads in the package to mitigate the typically capacitive nature of the SLI [34].
- 2. High-speed single-ended I/O interfaces: For components that are close to the CPU such as the memory modules, larger I/O count interfaces that rely on single-ended signaling are preferred. They have the advantage of requiring fewer number of lanes to achieve a desired I/O bandwidth at a given signaling speed. However, as the signaling speeds increase, controlling cross-talk for each section

of the I/O nets becomes a key package SI challenge. The FLI, routing, and SLI cross-talk in this case are all typically controlled through physical layout design optimization. Especially at higher signaling speeds, the number of C4 ground bumps, package layers, and ground BGA balls or socket pins required to isolate different sections of the I/O nets for acceptable cross-talk performance can require a great deal of die/package real estate and thus results in ever-increasing costs. Some of the more recent proposed solutions to tackle this problem include adding cross-talk cancellation circuits to the I/O drivers [35].

For all I/O interfaces, ensuring that every net can meet a predetermined Z_o target is most often the first task that an SI engineer needs to complete. Today's package stack-up and design rules reflect the typical Z_o design targets. As examples, 50 Ω for single-ended and 100 Ω for differential interfaces are typical values. The final package SI metric in Fig. 31.14 refers to controlling of high-volume manufacturing variations. This is typically accomplished by optimizing the package dimensional and material tolerance specifications that dovetail well into the substrate manufacturing process capability.

As mentioned earlier, another key knob to improve the data bandwidth is to increase the I/O count. Even though package design rules have been steadily improving over the years to provide more FLI and SLI I/O density, some of the recent breakthroughs in this area rely on alternative packaging architectures. In addition to 3D stacking, which allows for a very large number of connections between the dies in the stack, 2.5D technologies such as silicon interposers [22] and embedded multi-die interconnect bridges (EMIB) [21] have also enabled a significant scaling in I/O bandwidth for side-by-side silicon components in multichip packages. Figure 31.15 shows the comparison of some of the recently announced 2.5D technologies to the traditional packaging technologies in terms of



Fig. 31.15 I/O routing density capabilities for packaging technologies

I/O routing density capability. A technology that can support, for example, >200 I/ Os/mm per substrate layer along the die perimeter can provide ~1 Tb/s I/O bandwidth using only ~2.5 mm of die edge, two layers of routing, and with signals running as low as ~1 Gb/s. This is a desirable design target which provides very high I/O bandwidths at favorable I/O power efficiencies [36].

Future packaging technologies need to support both long-reach very high-speed I/O interfaces where the cost of the interconnect is proportional to the number of and density of I/Os and high wire count, short-reach lower-speed I/O interfaces where efficient management of the I/O power is key. These two trends constitute the fundamental challenges for future of package signal integrity and are expected to drive further innovation in novel packaging architectures and signaling methods (i.e., optical RF).

31.4 Thermal Management

The need for thermal management is an important consideration that must be thoroughly understood for any high-performance IC. The thermal management problem for electronic components in a computer is one of transporting the steady-state thermal design power (TDP) from the die surface,⁹ where the temperature of the hottest spot on the die is maintained at or below a certain specified temperature (typically referred to as the junction temperature T_j), to the ambient air at temperature T_a . Using a simple thermal resistance model, the required thermal resistance is represented as the ratio of ($T_j - T_a$) over TDP.

The temperature difference (T_j-T_a) will trend lower if junction temperatures need to be low to contain the rising contributions of leakage power and product reliability expectations (both of which are inversely proportional to temperature) and/or if T_a is forced to be higher due to heating of the air inside the chassis caused by increased integration and shrinking system sizes. In general, the thermal problem becomes increasingly difficult to contend with due to increases in TDP, reductions in (T_j-T_a) , or a combination of both. Thus the thermal solution designer is faced with the challenge of developing a thermal solution that has a thermal resistance at or below the required thermal resistance to meet the product performance requirements.

The thermal management challenge may be described in terms of the following elements:

 Historically, increasing CPU performance meant increasing TDP and was one of the main issues in thermal management [37]. However with the transition to multi-core microprocessor architectures, dramatic increases in TDP have been

⁹Management of thermal transients is also an important consideration during testing of semiconductor devices and when they are expected to operate in burst modes; however this is beyond the scope of this chapter.



Fig. 31.16 Typical die power map and the hot spots on the corresponding die temperature map. The dark red central region represents the highest temperature spot



Fig. 31.17 Schematic of the two basic thermal architectures, illustrating their primary heat transfer path. (a) Architecture I (b) Architecture II

attenuated as processor performance increases. This has lessened the thermal design challenges somewhat.

• In addition to an increase in TDP, thermal designers need to account for areas of thermal nonuniformity (typically power densities of 300+W/cm² are possible). These high thermal flux regions are caused by a nonuniform distribution of power generation on the die. This can occur if the activity level of transistors in one particular area is much higher than in adjacent regions on a chip. The thermal impact of nonuniform power is schematically illustrated in Fig. 31.16.

The general strategy for thermal management focuses on:

- · Minimizing the impact of local hot spots by improved heat spreading
- Increasing the power-dissipation capability of the thermal solutions
- Expanding the thermal envelopes of systems (i.e., increasing T_i or lowering T_a)
- Minimizing the cost of the final thermal solution
- · Developing solutions that fit within form-factor considerations of the chassis

In this section we will focus only on package-level thermal solutions. As discussed in [38] and illustrated in Fig. 31.17, there are two thermal design architectures. Architecture I is one where a bare die interfaces to the heatsink solution through a thermal interface material (TIM), and architecture II is one where an

integrated heat spreader (IHS) is attached to the die through the use of a TIM and the heatsink interfaces to the IHS through a second TIM. Architecture I typically has a lower profile compared to Architecture II and is often used for microprocessors in mobile and handheld computers. Architecture II is typically used for microprocessors in desktop and server applications.

The goal of package-level cooling in Architecture II is to use the IHS to spread the heat laterally while transporting it from the die to the heatsink. The heatsink in turn dissipates heat to the local environment. In Architecture I, the base of the heatsink serves to spread the heat. Since Architecture II best illustrates the overall cooling strategy, it will be used it in most of the discussion in this section. The TIM between die and IHS is referred to as TIM1, and the TIM2 is the interface material between IHS and the heatsink.

To increase cooling capability, the strategy is to even out the temperature profiles due to nonuniform power distributions, as close to the source as possible, by spreading out the heat. Heat generated at the device is first conducted through the bulk silicon of the IC and then conducted through the TIM1 with a minimal amount of spreading. The focus in optimizing TIM1 thermal performance is to minimize its thermal resistance. This involves minimizing both the contact resistance and the bulk resistance of the TIM1 material. This is accomplished by managing three parameters: (a) the intrinsic thermal conductivity of TIM1, (b) the thermal contact resistance of the die/TIM1 and TIM1/IHS interfaces, and (c) the TIM1 layer thickness, also referred to as the bondline thickness. At the IHS level, the heat spreads and peaks in the power profile, and the resulting temperatures are smoothed out. The considerations in designing the IHS are to optimize two factors: the thermal conductivity of the IHS material and the thickness of the IHS, while ensuring that the physical and mechanical properties of the package are within acceptable limits. A thicker IHS of high thermal conductivity material will enhance heat spreading. Package thermal resistance is typically communicated in terms of an area-normalized resistance R_{ic} , defined as

$$R_{jc} = \left(\left(T_{jmax} - T_{case} \right) / P \right) x A_{die}$$
(31.1)

where *P* is the power dissipated uniformly on the die, T_{jmax} is the maximum die temperature, and T_{case} is a typical point on the IHS or heatsink. In the case of Architecture I, T_{case} is typically a point on the heatsink base over the center of the die, and in the case of Architecture II, it will be a point on the top surface of the IHS over the center of the die. Epoxies, phase change materials, and greases filled with thermally conductive fillers are the most commonly used TIM materials.¹⁰ Figure 31.18 shows some of the advances in R_{jc} from one silicon generation to the next accomplished by improvements in both TIM1 material and TIM1 bond-line thickness controls.

¹⁰In addition to particle-filled polymers listed, solders are also used as TIM materials. Solders have significantly higher bulk thermal conductivity (30–50 W/($m^{-\circ}K$)) compared to filled polymers (~3 W/($m^{-\circ}K$)); however they require very different and potentially expensive processing conditions.



Fig. 31.18 Advances in R_{jc} for Architecture II



Fig. 31.19 A typical flip-chip package configuration

Copper is the primary material of choice for IHS because it is abundant, has high thermal conductivity, and is a cost-effective choice. Innovative new carbon nanotube (CNT) surface treatments have demonstrated improvement in thermal contact conductance between CNT and external surfaces [39, 40].

Thermoelectric or Peltier devices offer promise to provide enhanced cooling to localized chip areas although the overall TDP will increase. A significant area of interest is in the development of nanostructured thermoelectric materials due to the promise of highly efficient thermoelectric energy conversion [41]. This interest is additionally sparked by the potential to integrate thermoelectric devices in the package or silicon to provide local on-demand cooling. However there are significant challenges that need to be overcome in order to realize the potential of these materials. Challenges exist in integrating the thermoelectric materials in energy efficient modules that can be integrated on the silicon or in the package. A key area of concern is reducing electrical parasitic resistance in the contact technology for the thermoelectrics [42, 43]. Focus is also needed to ensure that the devices operate at high efficiencies for multiple operating conditions of the electronic components. Finally, the process for integrating the devices in silicon or the package needs to be developed.

31.5 Structural Integrity

A typical flip-chip package configuration is shown in Fig. 31.19. The CTE of an organic package substrate is ~16 ppm/°K, while the CTE of the Si chip is less than 3 ppm/°K. Sn-based, lead-free solders with melting points of ~220–225 °C are used



Fig. 31.20 Cross sections showing the interconnect structures in a static RAM (SRAM)

to join the chip to the package. Since the chip is attached to the package at a high temperature and then cools down to room temperature during package assembly, significant stresses are developed in the chip, package substrate, and the interconnect between the chip and the package. The effect of such stresses on the silicon is generically referred to as chip-package interaction (CPI). In addition to the CTE mismatch, the CPI stresses are impacted by the assembly process conditions and chip and package design layouts and materials. System-level considerations such as the PCB assembly process and use conditions also affect the CPI.

Advanced microprocessors depend upon transistor scaling to get improved performance, generation over generation. The accompanying interconnect scaling on the die back end (see Fig. 31.20) causes interconnect propagation delays which impact chip performance. The transition from aluminum die backend interconnect to copper in the 1990s was a key step in reducing interconnect propagation delay by reducing the interconnect resistance. The RC delay was further reduced by lowering the capacitance in the interlayer dielectrics (ILD), through the introduction of materials with low dielectric constant, k.

A consequence of using lower k ILD materials, typically accomplished by increasing porosity, is that the ILD materials become increasingly fragile [44]. Elastic modulus and fracture toughness of these materials decrease rapidly as porosity increases. It has been observed that after the chip is assembled to the package, such ILD materials with lower adhesive and cohesive strengths can experience ILD cracking underneath the flip-chip bumps.

In addition to the ILD cracking, die cracking, as shown in Fig. 31.21, due to CPI stress and defects in wafer processing (including thinning and dicing), needs to be eliminated.



Fig. 31.21 Die crack as shown in (a) package cross section, (b) C-mode (confocal) scanning acoustic microscopy image



Fig. 31.22 (a) Springlike compliant interconnects used to minimize stress coupling between the silicon and package [45] (b) CNT interconnects on solder bumps: potential FLI solution [47]

One approach to reduce packaging stress is to make FLI solders more compliant so as to dissipate more stress through solder deformation, thereby protecting the low-k dielectrics. Another approach to reduce stress transfer to the ILD layers is through the use of geometrically compliant interconnects, an example of which is shown in Fig. 31.22a [45], where mechanical compliance in the interconnect joints is achieved by structural design of the joints. A further extension of this approach with novel materials is to consider using CNTs (Fig. 31.22b) or metallic nanowires to

а



construct the above interconnect structures. Although potentially both metallic nanostructures and CNTs can be used as building blocks for these nano-interconnects, CNTs can be a better choice because of their ballistic conductance, high electromigration (EM) resistance, as well as the excellent mechanical properties (e.g., super-compressibility) [46]. However significant challenges will need to be overcome before some of these potential opportunities can be realized. These challenges include the low-temperature growth of highly aligned and high-quality CNTs and understanding and resolving the CNT-metal interface contact resistance issues.

The FLI underfill process and polymer material choice play a significant role in enhancing the chip-package structural integrity. Typical package polymer materials require a combination of mechanical properties, e.g., CTE of <16 ppm/K, controlled mechanical modulus, high toughness, and low moisture absorption. Significant improvements in several composite material properties, such as the modulus, CTE, and toughness, may be effected by the addition of certain nanoparticles to the polymeric formulation (Fig. 31.23). These changes can be accomplished with minimal impact to manufacturing aspects of the material such as its rheology. The key challenge is to develop and integrate these materials and to achieve the required properties simultaneously. Significant research is required for designing and tailoring the nanoparticle-matrix interface, achieving the desired nanoparticle dispersion within the polymer matrix and developing an appropriate "rule of mixtures" for nanocomposites. Since the nanoparticle-matrix interface appears to control a nanocomposite's properties, novel and appropriate chemistries are needed to optimize the design of a nanoparticle-matrix interface to obtain a specified combination of composite properties. Finally, empirical "rules of mixtures" exist for only a few nanocomposite systems, but global, predictive, "rule of mixture" guidelines for nanocomposites are needed to enable designed nanomaterials with optimized sets of specified properties.



Fig. 31.24 Typical defect modes seen during surface mounting of packages [49]

Recently, warpage of the package has become one of its increasingly important attributes as the demand for thin devices, such as smartphones and wearable products, grows. Package warpage management is critical so that it can be surface mounted on to the system board using the cost-effective conventional solder reflow process. Figure 31.24 shows some of the key issues associated with poor warpage management.

The package warpage specifications depends on a number of factors such as the solder ball pitch, available solder volume and its variation, the shape and condition of the solder joint interface, dynamic shape profile of the two mating surfaces, and the board assembly process requirement at room temperature as well as at solder reflow temperature. There are industry guidelines for allowable maximum warpage [50–52]. Given the complexity of dealing with multiple package types, sizes, design, materials, processes, and cost of over rejecting usable parts based on too aggressive specifications, defining a standards specification is a challenging endeavor. Figure 31.25 is a 2015 snapshot summary of the various industry efforts for BGA package warpage targets [49].

31.6 Form-Factor Management

The long-standing trend toward smaller computing system size continues to hold true today. A projection of this trend, as a derivative of Bell's law [53], is shown by Y. Lee et al. in Fig. 31.26 [54] where the authors make the argument that current miniaturized computing systems, such as smartphones, fit on an ongoing trend and even smaller computing systems are yet to come. It is obvious that these small systems, such as the tablets, smartphones, and smart watches, will require the system board to have a very small form factor.

The need for longer battery life (i.e., relatively larger space being allocated to the battery) puts additional pressure for the system board to be even smaller and denser to make room for larger batteries. This, in turn, increases the device density on the



Fig. 31.25 High-temperature package warpage allowable for BGA package stated in various industry specifications [49]



Fig. 31.26 Bell's law predicts continuous scaling of minimal sized computing systems [54]



Fig. 31.27 (a) Historical minimum die thickness trend (Source: Prismark Partners LLC 2008). (b) Minimum die thickness roadmap. (Source: ITRS 2.0 Heterogeneous Integration)



Fig. 31.28 Wafer-level packages: WLCSP and FO-WLP

board. The demand for denser system boards also applies to many other systems like the laptops and servers due to other technology drivers.

This demand for continually smaller and/or denser system boards is supported by IC packaging innovations along two vectors: (1) miniaturization of the single-chip package and (2) integration of multiple components in a package, referred to as system-in-package (SiP).

In the early phase of package form-factor reduction, smaller body size was achieved by simply reducing the second-level interconnect pitch. Later, package thickness was also reduced by thinning the die (Fig. 31.27) and other dimensions such as thickness of mold compound over the die. This eventually led to the chip-scale package (CSP) concept, where the package area was reduced to less than $1.2 \times$ the die area [55] as compared to approximately (2–10)× times the die area with the traditional plastic ball grid array (PBGA) technology. CSP was achieved by reducing BGA pitch, wire bond lengths, and wire loop heights, thinning the die, and package (MMAP). Packaging concepts such as quad flat pack no-lead (QFN) and wafer-level package (WLP) also fall into the CSP category.

Of all the single-chip packages, the WLP has the smallest form factor for a given chip size. There are two major types of WLPs: (a) fan-in WLP, also referred to as wafer-level CSP (WLCSP) and (b) fan-out WLP (FO-WLP) as shown in Fig. 31.28.

The WLCSP uses the native silicon wafer and then adds one or two copper interconnect layers, called redistribution layers (RDL), to reposition the I/O



Fig. 31.29 Fan-out wafer-level package [56]

terminals on the chip to appropriate locations on the package for connecting to the system board. This is followed by the BGA solder ball attach process step and singulation from the wafer to create the WLCSP. Thus, the WLCSP, being the same size as the chip itself, is the smallest possible single-chip package. The redistribution layer (RDL) adds only a few 10s of microns of Z-height to the chip. Consequently, small devices, like smartphones, and wearables have been increasingly using WLCSP. Only a thin RDL polymer layer separates the WLCSP silicon from the system board. The stresses due to CTE mismatch between the chip and the system board limit the maximum WLCSP size. It becomes more challenging with finer BGA pitches where the solder joints are smaller and mechanically weaker. This issue can be managed through several techniques including the proper choice of RDL polymers, BGA solder material, and adding board-level underfill with optimized processing and material.

FO-WLP is processed in a wafer format similar to WL CSP. However, one major distinguishing feature is that it is a reconstituted wafer (Fig. 31.29) as opposed to the WLCSP's native silicon wafer. The reconstituted wafer is created by first placing individual silicon chips spaced away from each other by the amount required for fanning out the I/O routing from chip terminals to package BGA pads. The chips are then embedded in epoxy mold compound in the shape of a silicon wafer. The rest of the fabrication process is similar to that for WLCSP. The difference in structure between the two types of WLP leads to differences in their mechanical performances. The FO-WLP structure can also be created through a reconstituted panel form factor which is rectangular in shape instead of the wafer shape. This package is called fan-out panel-level package (FO-PLP).

As noted earlier, SiP is another vector for system miniaturization. The SiP allows many board-level components to be integrated in the package. And, it allows those components to be smaller in size and/or have finer pitch interconnects. They can be placed very close to each other by leveraging the advanced design rules and process



Fig. 31.30 Stacked die CSP: (a) mixed flip chip and wire bond (no TSV) and (b) 3DIC with through-silicon via (TSV) $\,$



Fig. 31.31 PoP packaging technology (a) bare die direct PoP, (b) through mold PoP interconnect, and (c) Cu Pillar PoP interconnect with WLCSP bottom package

equipment capabilities available for package assembly. This close packing of the components can be done in 3D space (i.e., on X-Y plane and through vertical stacking). Another benefit is that the resulting subsystem can be electrically tested before the board assembly.

SiP covers a large variety of package types [9]. In some cases, a SiP replaces a system-on-a-chip (SoC) because of faster time to market, lower development cost, and/or lower product cost. Only a few of the SiP types are discussed here. One very widely used SiP technology is stacking of memory on logic devices. This is done in two ways. The first is stacking of die on die in the form of stacked die CSP (SCSP), and the second is stacking of package on package (PoP). Figures 31.30 and 31.31 show a few examples of the SCSP and PoP configurations.

The SCSP and PoP configurations allow integration of chips from heterogeneous silicon processes and from multiple suppliers. These two technologies significantly reduce package XY area at the expense of Z-height. So, these technologies require very thin components and materials (i.e., die thickness, wire loop height, mold cap, package substrate thickness, FLI thickness, and BGA ball standoff) to deliver desired thinness of the final stack. Stacking of chips increases the overall power density in the package; so a special attention needs to be given to thermal management if high-power devices are integrated in such packages.

Challenges for SiP are manyfold. These include creating appropriate industry standards to manage interfaces between the SiP components such as the PoP interconnect design, material, and warpage, defining die bond pad locations, and functional assignments to efficiently interconnect the various chips inside the package. It is also important to find an affordable means of assuring known good die (KGD) before committing it to the SiP. Compounding of die test yield loss can limit the maximum number of dice that can be affordably integrated in a package [57]. Another critical challenge for SiP and other thin packages is managing technical issues associated with extremely thin die. The thin die challenges include the thinning process, stress-induced electrical property changes, and package warpage. Wafer thinning down to 40 μ m and in some cases to 10 μ m (Fig. 31.27b) would require thickness variation control, surface roughness minimization, relieving residual stresses caused by the thinning process, and protecting the die from chipping and cracking during wafer thinning and die singulation. Handling of a significantly warped thin wafer and die creates another key challenge. Improved carriers as well as pick and place equipment would be required to keep the wafer and die flat during the assembly process. It is shown that mechanical stress may induce changes in the electrical properties of the transistors [58]. The choice of die configurations, changes in material properties, and dimensions of the various components of a thin package can have significant impact on the stress level of the thin die. A thin package with thin die is prone to warpage due to its low stiffness. Future decreases in die thickness are expected to make this problem worse, impacting the board assembly yield. Solutions for these challenges would need innovation in packaging design, material, and process technologies.

31.7 Summary

In this chapter we have described some of the key drivers that have influenced the evolution of the high-performance logic packaging in consumer and business computing systems as well as in ultra-mobile devices. As the silicon features go deeper into the nanoscale, packaging technologies will be challenged to extend the trends in physical density scaling, power delivery, signal bandwidth, thermal management, structural integrity, and form-factor reduction.

Delivering innovative packaging solutions to meet these challenges will require accelerating the transition of emerging technologies, like nanotechnology, from research to affordable implementation. However, the trend of increasing complexity can increase the development cycle time and also increase the cost of packaging. Opportunities to successfully leverage emerging technologies to address complexity and cost will continue to pose significant challenges; however they will offer tremendous competitive advantages and need to be explored collaboratively by researchers in the field. **Acknowledgments** The authors would like to thank Brent Stone and Donald Tran from Intel Corporation for their help in providing background information on socket technologies. We would also like to thank Chris Matayabas and Gaurang Choksi for reviewing the chapter and providing guidance on enhancing the chapter.

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Chapter 32 Nanotechnology Health, Safety, and Environment Overview



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32.1 Overview of Nanomaterials

This chapter focuses on the environmental, health, and safety aspects of nanotechnology and nanomaterials. The fact that various nanomaterials are more reactive than their bulk counterparts creates a need to address the possible effects, which are typically unknown, in working with, handling, storing, applying, manufacturing, and creating novel combinations of nanomaterials. This chapter provides an overview of some of the characteristics of known nanomaterials, identifies known effects on people and the environment, and addresses the need and method of proper handling of nanomaterials.

Unfortunately, there is not a simple test that can produce a result that is accurate about most nanomaterials throughout the entire range of what is considered "nano." There are, however, some precautions that can be taken to minimize the possible risks that could be associated with the manufacture and handling of nanomaterials. In the resultant training material developed under a Susan Harwood OSHA (Occupational Safety and Health Administration) grant [1], the estimates for the possible combination of nanomaterials that could be created (and need to be evaluated) are greater than 10^{200} ! This is a daunting task considering that the American Society of Chemical Engineers [2] has characterized less than 10^8 .

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32.2 Understanding Nanomaterial

There is significant coverage of nano in the earlier chapters. There is a need for a review in order to properly put the issues in perspective. The traditionally accepted usage of the term "nano" when applied to materials/particles is in reference to materials/particles that have a size dimension of less than 100 nm. This is one problem. Classifying particles/materials the same in a range of sizes in this manner leads to erroneous assumptions. As the size decreases, the percentage of surface atoms increases. When that percentage gets to a certain point, the material starts to change behavior. This will be covered in the next paragraph. An example of changes which occur between materials is the van der Waals force. Normally considered a weak force, as the size of materials approaches 70 nm, the van der Waals force becomes the dominant means of holding particles to a surface (intermolecular attraction).

The differences in material properties between nano and bulk can be significant. Size is the obvious one. As the size decreases, the reactivity may increase. Aluminum nanoparticles become highly reactive when their size is in the region of 30 nm. The ability to fabricate two-dimensional materials, like one-atom-thick graphene, introduces materials with significant electrical properties. As another layer of atoms is added to the structure, the material changes its properties due to its *thickness*. It takes several layers before some of the bulk properties start to emerge. The *melting point* of materials can change. Gold (Au) has a melting point of 1064.18 °C, which has been used for centuries. Work on gold nanoparticles has shown that there are slight changes in the melting point that begins when the particle size is about 50 nm and continues to decrease with a sharper decrease starting to occur when the particles are about 15 nm in size. Traditionally accepted electrical properties have other influences that change standard values. The semiconductor industry has found that copper has decreased conductivity below 50 nm. There are two definite contributing factors. The crystal orientation and the grain boundaries inhibit the flow of electrons and decrease conductivity. Gold becomes a semiconductor under 1 nm. The color of gold nanoparticles in solution changes depending on the size of the nanoparticle. In the 1990s, there were pictures of vials with varying, different size nanoparticles that produced different colors. This is not a new phenomenon. The stained-glass windows from the Middle Ages have their red coloring due to nano gold particles embedded in the glass.

Many of the above characteristics are new but not necessarily surprising. There have been some surprises. Thirteen atoms of silver have been shown theoretically to have a magnetic moment. Thirteen atoms of platinum have been experimentally shown to have a magnetic moment. The crystal orientation of cerium oxide (CeO₂) has a size preference. CeO₂ less than 10 nm has the shape of a truncated octahedron with [100] and [111] faces. Greater than 10 nm, this orientation shifts toward [111] octahedron [3]. Transition metals can have five different states: as hydrated atom, metal complexed in a small protein, metal adsorbed to surface on 1 nm mineral particle, metal adsorbed to surface of 20 nm particle, and the same except to a 200 nm particle [4]. As additional research is completed, there are more interesting

aspects to the nanomaterials that may lead to novel devices. Medical applications have made significant progress in successfully applying nanomaterials.

There are a number of potential issues that arise from but are not unique to nanomaterials. As will be discussed in the next section, there are potential issues with possible toxicity effects. As with any material, there are possible chemical dangers. Standard procedures are available for most chemicals. Unfortunately, material safety data sheets (MSDS) are not available for most forms of nanomaterials. The potential for creating a fire is possible with certain materials. As mentioned earlier in this section, select nanomaterials can become highly reactive (explosive) as the amount of surface atoms becomes a significant percentage of the total material. Dust is always a potential problem even in the bulk state of materials. Is nanomaterial dust more or less dangerous than the bulk material? There is no specific answer, but it is reasonable to think that nanomaterial dust generally is not less dangerous than the bulk material. As with any very fine-sized bulk materials, electrostatic charges can create situations with an unwanted, accidental transport due to the material ability to statically cling to garments, gloves, shoes, equipment surfaces, and other items removed from the initial site of application. Contamination becomes an issue.

While most of the above issues are understandable, there are some that may not be as obvious. The size of the material in the nanorealm changes the properties of the material, which is somewhat understood. However, the fact that certain materials change shape as they change size is not common, but it does happen. Certain shapes tend to "excite" people. If a nanomaterial appears to be needlelike, many consider it to be dangerous. This experience comes from asbestos, where five of the six different types are needlelike, while the last is curved. This latter one has difficulty penetrating in the human body, while the others are very effective at penetration. There are some medical opinions that under 5 μ m in length, the rodlike structures (carbon nanotubes, for instance) are not as dangerous. The volume of material is another consideration. The density and concentration of the material also have an impact on the potential risk. Certain materials can accumulate in parts of the body and cause significant adverse effects. (Think lead and the Romans.) The Royal Chemical Society's web page [5] has stated: All chemicals are deadly; it only depends on the quantity. The answer to understanding nanomaterials is we know very little, know that there are a lot of areas we have not quantified, and realize that with the development of novel combinations of materials at the bottom end of the nanorealm, we have no idea of what will be coming. Consequently, we need to develop protection methodologies. There are certain things we know about nanomaterials and their effects, which are covered in the next section.

32.3 Identified Risks with Specific Nanomaterials

The question that arises is "What are the known problems with nanomaterials?" In most cases we do not know. Many issues have been brought forward, but the time for testing is significant and can take many years before it is classified. There is a word

of caution with the classification. In many cases, the decision will indicate something like "not known to be a carcinogenic to humans." This does not indicate that it is not, but only there is not enough evidence to indicate that it is. When concern arises about a material, it is always appropriate to remember the fact that all materials are potentially dangerous; it only depends upon the quantity.

In order to focus on the topic of this book, the most common materials that are being or proposed to be used will be covered. The authors are aware that this list of nanomaterials will continue to grow, but we will not attempt to guess which additional materials will be employed. Consequently, silver, carbon nanotubes, graphene, CdSe, and TiO₂ will be discussed. It is anticipated that there will be periodic updates to this book in order to keep the material current.

Nano-toxicology is the study/investigation of the toxicity of nanomaterials. The study is based on determining potentially harmful but not necessarily fatal effects. The increased reactivity of materials as their dimensions decrease creates situations that are dissimilar to the properties of the bulk materials. Nano-toxicity addresses both whether or not and to what extent these novel properties may pose dangers to people and/or the environment. There is a significant amount of research being conducted.

Testing of nanomaterials is very complex. It is possible that employing a few tests will not provide results that can give accurate guidance. Another interesting issue is that tests conducted on cells often do not match those conducted on animals. There has been significant effort toward developing tests that have a wide range of applications, but the progress has been a lot slower than desired. Consequently, there is much material that is available through the Internet that does not have scientific rigor. The length of time that it takes to conduct the full range of testing for a drug to determine possible effects on humans can range from 7 to 10 years. For the application being developed by a technology company, it is difficult to imagine a company waiting for the complete testing prior to manufacturing the product. An argument can be made for this approach because the majority of products are not planned on being inside humans. However, the concern is that nanomaterials may find paths to enter the body.

There are many routes for exposure. Inhalation can occur through inhaling airborne nanoparticles which may be deposited in the respiratory tract. From this location, the nanoparticles can enter the bloodstream and move to other organs. There are certain organs, like the liver, which are susceptible to accumulating various metals. The skin (dermal) exposure seems to be selective with no nanoscale oxides penetrating more than a few layers of the skin. Some metal particles have been shown to penetrate damaged or diseased skin. Quantum dots have been found to penetrate intact pig skin within 24 h at exposure levels that could occur in manufacturing. It is also possible to ingest the nanomaterials. Single-wall carbon nanotubes delivered into the gut for treating Alzheimer's disease were found in the liver, brain, and heart. Ingestion of colloidal silver can result in permanent blue discoloration of the skin, nails, and eyes [1]. In the following section, the safe handling of nanomaterials is explored.
Silver (Ag) Silver (Ag) was one of the first nanomaterials to be greatly studied to evaluate the impact on people and the environment. In the range of 30 nm and smaller, nanosilver has the ability to kill bacteria. An additional benefit is the diminishing of the ability of the bacteria to develop an immunity to the nanosilver, which is significantly less than the bacteria's ability against antibiotic drugs. This sounds good except for the fact that the nanosilver kills without respect to good or bad bacteria. The question that then arises is what happens when the material gets into the environment. It turns out that the material kills some lower aquatic life forms. This ability of nanosilver does not go on forever. Eventually, it combines with other materials, like Ag₂S, and becomes nontoxic. Regulations have a tendency to lag the actual situation. The EPA developed concentration limits based on mature aquatic creatures. Eventually, these were changed to recognize the fact that the immature fish were more significantly harmed by lower concentrations. There have been recent studies with flies that evaluated the 50% toxicity level concentration. After a few generations, the flies developed an immunity to the concentration and returned to normal levels of reproduction.

Silver's effect on turning human skin and nails a bluish tint after long exposures has been known for some time. But, the exposure was not fatal. The terms "blue blood" and "born with a silver spoon in his/her mouth" refer to very wealthy families in the Middle Ages, who tended to use eating utensils made of silver.

Carbon Nanotubes (CNTs) Carbon nanotubes (CNTs) are used in numerous products to increase the strength of the product while reducing its weight. Toyota was one of the first manufacturers to replace metal automotive bumpers with carbon nanotube-impregnated plastic. This produced a bumper that was at least twice as strong as steel and about 25% of steel's weight. The result was better mileage. The material has been employed in baseball bats and tennis racquets to improve performance and reduce weight. There was concern raised by people who noticed that the CNTs are needle shaped although typically less than 2.5 μ m long.

To further complicate the issue, the University of Florida published research in 2008 where an experiment was done to evaluate the effect of CNTs on a rat's intestines. The experimental results indicated that there were lesions observed and these had characteristics signs that were very similar to those seen in tests with asbestos (mesothelioma). The general press picked up on these results and promoted the premise that CNT's will cause similar health issues to those caused by asbestos. There are two issues that were not understood by the reporters. The first is that the CNTs were specially made to be $10 \times$ longer than the typical manufactured CNTs. This extended length made the experimental CNTs roughly the same size as asbestos. The second fact is that the quantity employed in the experiment was extremely high. Extreme doses do not represent typical situations and will cause abnormal results. As a side note, people have died due to consuming too much drinking water!

Carbon nanotubes have electrical properties. Depending on the chirality of the tube, it can be either a conductor or a semiconductor. Some efforts have been made in creating electrical circuits using this material.

Graphene (Carbon) Graphene (carbon) is typically called a two-dimensional material. Graphene is an unrolled carbon nanotube. In its thinnest form, it is only one atom thick. It is a good electrical conductor and also a very good heat conductor. There are applications that are looking at employing graphene and other similar 2-D materials to electronic circuits. An interesting fact is that adding oxygen to the graphene structure creates an insulator, which is called graphene.

Some concern has been raised due to its shape. A one-atom-thick material could be conceived to be an extremely sharp material capable of cutting through most tissue. At the time of this chapter, there were not any published reports on graphene testing on tissues.

Cadmium Selenide (CdSe) Cadmium selenide (CdSe)-derived nanoparticles with sizes below 10 nm exhibit a property known as quantum confinement. Quantum confinement results when the electrons in a material are confined to a very small volume. Quantum confinement is size dependent, meaning the properties of CdSe nanoparticles are tunable based on their size. One type of CdSe nanoparticle is a CdSe quantum dot. This discretization of energy states results in electronic transitions that vary by quantum dot size. Larger quantum dots have closer electronic states than smaller quantum dots which means that the energy required to excite an electron from the highest occupied molecular orbital (HOMO) to the lowest unoccupied molecular orbital (LUMO) is lower than the same electronic transition in a smaller quantum dot [6].

In general, CdSe is considered nontoxic and safe for applications. The problem arises when the material is disposed of. It has been shown that after disposal, CdSe can break down when put into landfills. The element cadmium (Cd) is toxic. So this becomes a disposal issue.

Titanium Dioxide (TiO₂) Titanium dioxide (TiO₂) is commonly used in many products due to its photocatalytic properties. There have been a number of studies about sunscreen which contains TiO₂. There has been some concern. A report [7] covers murine liver damage caused by ingestion of nano-TiO₂. The authors state that this work on TiO₂ is still in its infancy. Much more needs to be done.

There is an issue with the material itself. TiO_2 exists in different crystalline phases, sizes, and shapes. This makes it difficult to come out with definitive analysis because the material may change during the evaluation.

How to Proceed? There are regulations in place, but these are subject to change as more knowledge is gained on nanomaterials. There is a need to constantly review the regulations and keep up to date on new developments. Everyone must be proactive in addressing the nanomaterial issues as they develop. One action that must be taken is to act to protect workers and the environment. The next section covers the methodology of the safe handling and control of nanomaterials.

32.4 Control of Nanomaterials

Working with nanomaterials will always be a challenge to workers. The specifics of the material being employed will have an impact on the potential impact on the works and the environment. Consequently, the worker must address the workplace as having the potential to have hidden effects. The semiconductor industry has a long history of addressing hazardous material in a manner that minimizes the risk to the worker. The same type of approach needs to be incorporated into working with nanomaterials.

As nanomaterials advance, more research will be needed to determine the health effects to workers. What is more important is that the industry provides a manageable and safe work environment. This will depend on how proactive industry and government are to establish guidelines that will ensure sound practices to work and handle nanomaterials.

32.4.1 Safety Issues

According to the National Institute for Occupational Safety and Health (NIOSH) [8, para. 2], "Workers within nanotechnology-related industries have the potential to be exposed to uniquely engineered materials with novel sizes, shapes, and physical and chemical properties." These unique characteristics of present and future nanomaterials can present further problems if we do not have protocols or risk management processes in place. NIOSH [9] has been conducting research on low solubility nanoparticles in animal organs. Researchers have suggested that some nanoparticles can travel to the respiratory systems and then move into other organs. These research conclusions mentioned above and all other research reported bring attention to safety issues with working with nanomaterials.

Nanoparticles can enter through the eyes, nose, mouth, and skin; the high surface area and surface-to-volume ratio can make the particles reactive or catalytic. Particles that enter the body can have negative future implications. The dangers of exposure can be increased if the worker has preexisting conditions. Occupational hazards with nanoparticles can intensify safety issues in the workplace. Some of the potential risks of exposure are [10]:

- Workers who handle nanoparticles in liquid without adequate personal protective equipment (PPE), e.g., gloves and protection suits.
- Workers who are engaged in pouring and mixing operations (high presence of agitation).
- Workers who handle powders infused with nanoparticles are in risk of aerosolization.
- Workers who clean dust collection systems used to capture nanoparticles can be at risk of skin exposure.

With an increase in nanomaterial development for consumer and commercial products, more attention is needed to ensure there is transparency on disclosure of negative impacts to workers. Current and ongoing safety issues can be controlled through valid research (i.e., surface area, chemical reactions, toxicology) to convert the results into knowledgeable training material.

32.4.2 Environment for Working with Nanomaterials

The environment for working with nanomaterials must be adequate for the type of materials being employed. These environments can range from negative pressure clean benches to fully configured clean rooms with the associated protective garments and masks. In extremely specialized circumstances, self-contained breathing devices may be required. One means of controlling nanomaterials that reduces some risk is to always keep the material in some type of appropriate liquid. This minimizes the risk of airborne particles or material clinging to garments.

The semiconductor industry is well experienced in cleanroom technology, which provides control and minimization of airborne particles. Clean rooms are equipped with a high-efficiency particulate (HEPA) filters with specialized processing of the exhaust. For situations with chemical fume hoods, vented closures, and other special devices, the local exhaust ventilation (LEV) needs to be processed and not just vented to the atmosphere.

Employing HEPA filters is not necessarily sufficient. The selection of a HEPA filter must include consideration of the size of nanoparticles being used and the expected percentage of particles that can be trapped.

32.4.3 Worker Training and Protection

Worker training is paramount to health and safety for people who handle nanomaterials. Even more, worker competence is very critical to the success of nanotechnology as a whole. Workers will need to understand the real issues regarding nanomaterials and their impact on safety [11].

There have been some successful funded grants to begin the momentum of addressing worker safety on the national stage, (i.e., OSHA 2010 *Susan Harwood Grant – Technical Approach and Program Design: Lateral Diffusion of Nano-Safety Education and Training*). This grant was intended to develop basic safety training curriculum for industrial hygienists, supervisors, managers, and other key personnel who worked with nanomaterials. A group of safety experts, toxicologists, and educators developed an online short training course with a certification exam for the Association of Technology, Management, and Applied Engineering (ATMAE). The content was selected based on a critical need for managers, supervisors, research

directors, and workers to become competent in the basic knowledge of nanotechnology safety. These are the topic areas:

- · Introduction to Nanotechnology and Nanomaterials
- Assessing Nanomaterials Risks
- Hazard Communication
- Nanomaterials Exposure Management
- Spill Control and Emergency Response
- · Regulations and Standards

PPE is very critical for the well-being of the worker. However, administrative and engineering controls are first priority, and then PPE is considered the last line of defense because training is needed to know how to use the appropriate equipment. Since PPE is the last line of defense, a preventative maintenance plan is needed to ensure the worker receives the maximum protection. NIOSH and OSHA mandate worker protection when dealing with materials in the 1–100 nm realm. The most common materials used in commercial products are TiO_2 (e.g., used in paints, paper, and cosmetics) and single- and multi-wall carbon nanotubes (e.g., aerospace, material science, etc.). Advances in PPE will improve the quality of working with nanomaterials.

32.4.4 Monitoring

An issue is how does one know if there are adverse effects to personnel. It is recommended that prior to beginning work in an area that uses nanomaterials, the workers have a baseline medical profile established. This needs to include any possible physical characteristics that may be impacted by exposure to potentially hazardous materials. Periodic evaluations need to be performed and evaluated by established medical personnel in the field of negative impacts on various human systems (lungs, vascular, etc.).

A critical aspect of the monitoring is to establish a series of monitoring/recording devices both in the area of nanomaterial application/manufacturing and the surrounding environment. As a minimum, the particulate content of the air should be closely watched. If there is an increase in the particulate count, there is a need to investigate the cause. There also needs to be a baseline monitor that provides a check against external atmospheric conditions creating a false positive on the internal measurements. The development of a maintenance and calibration schedule for the monitoring equipment is also an important aspect of monitoring the environment.

Training of personnel in nanotechnology safety and evaluation of their knowledge needs to be included in the overall program for worker safety (more on available training in the next section). Records must be kept. The length of the storage is debatable. One of the authors recommends that the personnel evaluation records be kept permanently. This is due to the issues that arose with asbestos, where it was many years later before potential consequences started appearing on a large scale. The litigation is still ongoing. Without records, there is no means of evaluating the potential cause.

32.4.5 Procedures for Handling and Storage

The question that arises is how should nanomaterials be controlled. The recommendation is that the material should be treated as if it were gold. (In some cases, it is more expensive than gold.) That means the material receipt is documented and signed off by a responsible person. The material is then put into secure storage areas. Material is signed in and signed out. Location-specific storage is provided at the point of use. All material needs to be in marked containers and not left sitting in the open. Access to the materials is only permitted by trained workers. For larger quantities, the control is as appropriate for the large quantities. This may involve piping the materials or having very large containers for material usage. The point is that the material needs to be traceable throughout the time in the facility. This is all part of a risk management policy for the organization employing the nanomaterials.

32.4.5.1 General Public Safety

The issue of the safety aspects of nanotechnology for the general public is more challenging. Fiction writers can employ fictional characteristics to nanomaterials in order to develop a sense of urgency or pending doom. There have been a number of books in this category. One of the early ones was *Prey* by Michael Crichton, which provided a story of nanomaterials that developed a program to become self-aware and work together [12]. It is made for good reading but provided the nontechnical public with the potential distrust of developments using nanomaterials.

With a general concern for potential dangers on nanomaterials, which has been promoted through somewhat inaccurate reporting of nanomaterials research findings, there has been a tendency to remove the word "nano" from advertising literature or mention in corporate documents. While this may seem to be a good means of avoidance, it, by itself, is not a recommended practice.

The key to handling nanomaterials is to develop a training program that provides the workers with the needed knowledge and tools for the safe application and handling of nanomaterials. In 2016, the industry is still developing procedures and training. There are some existing places to acquire specific training for handling nanomaterials, which will be covered in the following paragraphs.

32.4.5.2 Nano-safety Education

At the time of preparing this chapter, there are four known nanotechnology safety education/training efforts. These are the 8-h training module developed under the OSHA Susan Harwood Grant, the Nanotechnology Safety Education Grant, METPHAST program, and the Nano-Safety Certification program.

The *OHSA Susan Harwood* training grant awarded to Rice University in 2010 was focused on the development and implementation of an 8-h training course that consisted of seven modules. These modules were:

- 1. Introduction to Nanotechnology and Nanomaterials
- 2. What Workers Need to Know about Nanomaterial Toxicology
- 3. Assessing Exposure to Nanomaterials in the Workplace
- 4. Controlling Exposure to Nanomaterials
- 5. Risk Management Approaches for Nanomaterial Workplaces
- 6. Regulations and Standards Relevant to Nanomaterial Workplaces
- 7. Tools and Resources for Further Study

The course was focused on educating workplace safety experts on the additional implications of nanotechnology. The content is available from OSHA but would be best employed with trainers knowledgeable in the field on nanotechnology safety.

A National Science Foundation award was given to Texas State University in 2012. The focus of this effort was the creation of two courses directed at *Nanotechnology Safety Education* [13]. The courses were created in a modular format, so elements could be inserted into existing courses, or the modules could become a stand-alone course. It was realized that adding new courses in already crowded curricula would be difficult, but providing modules to add to existing courses might be easier for some programs. The first course is *Introduction to Nanotechnology Safety*, which consists of the following modules:

- 1. What is Nanotechnology and Nano-ethics
- 2. Ethics of Science and Technology
- 3. Societal Impacts
- 4. Ethical Methods and Processes
- 5. Nanomaterials and Manufacturing
- 6. Environmental Sustainability
- 7. Nanotechnology in Health and Medicine
- 8. Military and National Security Implications
- 9. Nanotechnology Issues in the Near Future

The second course is *Principles of Risk Management for Nanoscale Materials*, which contains the following modules:

- 1. Overview of Occupational Health & Safety
- 2. Applications of Nanotechnology
- 3. Assessing Nanotechnology Health Risks
- 4. Sustainable Nanotechnology Development

- 5. Environmental Risk Assessment
- 6. Ethical and Legal Aspects of Nanotechnology
- 7. Developing a Risk Management Program
- 8. Results of Case Studies and Research Projects
- 9. Hands-on Experience in the Texas State Composites and Plastics Lab (designed specifically for handling nanomaterials)

The National Institute of Environmental Health Sciences Superfund Research Program helped fund the Midwest Emerging Technologies Public Health and Safety Training (METPHAST) program at the University of Minnesota. This effort is focused on dissemination of web-based modules to train individuals about health and safety issues related to emerging technologies. The content will be developed in two distinct courses. The first course is *Introduction to Occupational Hygiene* and is a one-credit, semester-long course with five modules. The second course is *Nanotechnology Health and Safety*, which is under development and will be a three-credit, semester-long course consisting of 15 modules. These will provide in-depth training to both students in health and safety along with those in engineering and science.

The *Nano-Safety Certification* program is under development with the Association of Technology, Management, and Applied Engineering (ATMAE) and will cover basic elements of the safety requirements for workers in nanotechnology.

32.4.5.3 Ethics in Applications

It might have seemed strange to see modules listed in nanotechnology education courses that focus on ethics. In the development of the NSF courses, the team realized that working with materials that have unknown properties requires additional consideration to aid in decision-making. Part of the education process is to provide guidance on decision-making, risk evaluation, and considerations of potential consequences. Of course, one of the consequences can be significant legal responsibilities. There are many examples of poor decision-making that end up requiring the development of the Government Super Fund to mitigate sites that have been contaminated. The purpose of the addition of ethics content is to reduce the potential for reoccurrences of situations that require massive funding to correct.

32.5 Risk Management

The management of risk requires that there is an understanding of the potential dangers and the value of the effort can be determined. In order to properly manage a situation, the risks must be known. What is risk? Risk is a combination of the probability of a harmful occurrence versus the severity of possible harm. Any large project has risk associated with it. Normally, the dangers are evaluated, and ways are developed to mitigate the harm that may be casqued. The building of the

Golden Gate Bridge is one such example. Extreme safety measures were taken including nets hanging from the underside of the bridge. In spite of all the precautions, there were numerous incidents, but there were only 11 deaths. This is a high number, but compared to other major projects during that time, it was remarkably low [14].

At the current time, there is insufficient data to create a classification of *all* nanomaterials that will guarantee there will be no hidden dangers or other surprises. Consequently, determining the risk becomes an effort in unknowns. The lack of information will not be an excuse if anything happens, and there are resulting lawsuits. So, this effort must proceed along traditional methods of (1) identifying potential hazards, (2) evaluating current regulations, and (3) developing a plan to minimize any risk. This approach is similar to the training received by firefighting personnel who are taught basic emergency analysis procedures and to approach each situation where there are potentially hazardous materials and the actual material in the emergency situation is unknown.

Doing nothing is not an option. The first part of a nanomaterial program is to address peoples' health, material control, and environmental monitoring.

People's health requires training as well as proper working conditions. Nanomaterials can cling to clothing. Nanomaterials can be airborne. Protective gear may include traditional chemical lab garments and masks, lab coats, shoe covers, and some mouth and nose covering. Depending on the materials, the size, the quantity, and the potential toxicity, clean room garments are a good starting point. If more stringent controls are required, then fully protective garments should be employed along with air locks that stream air to remove loosely adhering nanoparticles. Garments will require a specialized cleaning process.

There needs to be means to prevent workers from accidently ingesting any nanomaterials. Many people unconsciously touch their face, mouth, etc. Gloves on the workers reduce the tendency to touch one's face and prevent nanomaterial from adhering to one's skin. A face mask will prevent accidental hand-to-mouth transfers of nanomaterials. There needs to be a requirement for all workers to wash before eating and/or drinking.

The *control of the material* is critical. All materials need to be identified and plainly marked. They should be kept in a secure location with restricted access to the storage. There should be a means of recording every time someone accesses the secure storage. Ideally, this is an automatic record keeping system. The actual area where the nanomaterials are to be manufactured or used needs to have airflow designed to remove any loose particles. Normally, the area is at a negative pressure with respect to the outside area. In the nanotech area, lab hoods with negative pressure can be employed. For more dangerous situations, the lab hoods may have access only with gloves extending through the protection material, and any samples are entered through a double-door sample chamber in the hood.

Many larger companies have a baseline medical exam of any employee who would be working with the nanomaterials. This is a precaution in case there is an incident, and history is available to understand if there were changes to the person's health. *Monitoring the environment* is a good means of identifying if and when an exposure occurred. As mentioned in the previous paragraph, a person's medical baseline is available if there were to be an incident. How do you know there was an incident? By monitoring and recording the information. It can be as simple as a particle counter in the work area with nanomaterials. It is also advisable to have a baseline monitor. One small company that has excellent monitoring capability had an unusually high particle count reading in the area where nanomaterials were being produced. This caused an alarm, until the baseline monitor, which had both office and outdoor sensors, was checked. As it turned out, that day had a very high level of natural pollutants (springtime pollen). This process of providing the workers with the proper training and ensuring that the environment is being monitored does not just happen. It takes planning, training, testing, and record keeping. Eventually, we may find out that some of it is not necessary, but until then precautions must be taken.

Having taken these precautions on workers and the environment, how does one make decisions on the application of the nanomaterials? In general, this is more difficult. Some applications are easy to control. In a medical environment, like insertion of viruses with gold nanoparticles attached to inject into a person for cancer treatment, the materials are fairly well contained. Procedures are in place for the proper handling and disposal of materials. The amount of nanogold is small and will not be getting in to the environment. A more difficult choice is the handling and usage of quantum dots. Typically, these nanoparticles are considered "not proven to be carcinogenic to humans". [Notice the precautionary statement does not say "safe."] The application of quantum dots is increasing for televisions and other monitors. The issue is that some of the quantum dots are made from material that decomposes when it is discarded into a landfill. The resultant material may be toxic. Is this a wise decision to use the quantum dots? If one considers the small amount of material being used and the greater reduction in electrical usage, there will need to be a trade-off. This is a similar question to "Do you build a bridge if you know two people probably die in its construction?" Or, an even more interesting decision: "Do you clean up the radioactive material at the Bikini Atoll because there is a probability one person may die? And, in doing so, two people die!

In spite of all the preparations and all the evaluations, there will be insufficient information to make a completely informed decision. Consequently, it is necessary to provide a means of making the best decision with imperfect knowledge. Constant updates on materials and regulations are required. The answer is imperfect but the best available today.

32.6 Regulations and Restrictions

The one main problem with regulations is that they normally start late and, when they are projected forward, they mix the facts and capabilities. CNTs are a perfect example. The initial efforts were to develop/manufacture some of the material so that experiments could be conducted to understand its properties. This was a brand-new field with no history and consequently no knowledge of potential benefits or issues.

Some observers noticed a similarity in shapes between CNTs and asbestos. There were experiments developed that demonstrated a possibility of CNTs causing lesions in tissues, which were similar to those caused by asbestos. This led to concern about nanomaterials possibly being dangerous. One reaction was that the city of Berkeley, California, passed an ordinance that required any nanomaterials brought into the city were required to have a material safety data sheet (MSDS). The MSDS did not exist for CNTs or for almost all other nanomaterials. The result was that a MSDS of a very similar material (almost identical) had to be substituted. At that time, and in some cases still today, the regulations do not acknowledge the possibility that a slight difference in nanomaterial particle size totally changes the properties of the materials.

One cannot ignore the regulations, but one needs to be aware of the changes and modifications to existing regulations. There are governmental regulations that need to be periodically reviewed. One of the problems with nongovernmental sites is that these sites may not have the latest information or be taken off-line as the support funding dries up. It is unfortunate, but it is a situation that occurs on a regular basis.

It is difficult to provide a comprehensive list of US organizations involved in nanotechnology. Key ones can be identified under the National Nanotechnology Initiative, which also lists a large selection of publications. The other emphasis the US federal government has is in the health arena. Below are a listing of agencies that can be used as starting point for investigating nano-safety issues and regulations. There is no attempt in this chapter to attempt to address the individual state and local agencies that might be involved.

- National Nanotechnology Initiative http://www.nano.gov
- NIH http://www.nih.gov/research-training/nanotechnology-nih
- NIOSH http://www.cdc.gov/niosh/topics/nanotech/default.html
- EPA http://www.epa.gov/pesticides/about/intheworks/nanotechnology.htm
- FDA http://www.fda.gov/ScienceResearch/SpecialTopics/Nanotechnology/

There are both European Union organizations and local country organizations. The European Commission has recently moved their policy website and cover key enabling technologies. There is also a EU NanoSafety Cluster website, which addresses the "Safe Handling of Nanomaterials." The Organisation for Economic Co-operation and Development (OECD) has 34 member countries (as of this writing) with a possible 35th joining soon. They cover a wide number of topics.

Countries have their own organizations. Great Britain, for example, has a Health and Safety Executive, which has a website covering numerous topics. The German Federal Institute for Occupational Safety and Health (BAuA) also has a wide range of topics.

 European Commission – http://ec.europa.eu/research/industrial_technologies/pol icy_en.html

- EU NanoSafety Cluster http://www.nanosafetycluster.eu/news/116/66/World-sfirst-interactive-Nano-Platform-on-Safe-Handling-of-Nanomaterials-published. html
- OECD http://www.oecd.org/science/nanosafety/
- UK HSE http://www.hse.gov.uk/nanotechnology/publications.htm
- BAuA http://www.baua.de/en/Topics-from-A-to-Z/Hazardous-Substances/ Nanotechnology/Nanotechnology.html

This list could continue for many pages. There are organizations throughout the world that address various issues involving nanotechnology. If there are specific countries, the best way to start is to search the web of the topic of "nano-safety" and the name of the local entity. Whatever information that could be added to this chapter has a high probability of being replaced by something else by the time the book is published. This is one area that requires constant reviewing.

32.7 Summary and Mitigation of Impact

With unknowns, we must be proactive to protect people and the environment. In many cases, we do not know what we are looking for. This raises the question: How do we proceed? While we do not have all the answers, we can take a number of precautions. The end focus is to keep yourself safe, to keep your colleagues safe, to keep the general populace safe, to keep the facilities safe, and to keep the environment safe.

While this is not a simple task and there are many opportunities to overlook items, education is a key. This is the reason that the OSHA grant was awarded and the NSF education grant followed. There is a baseline established for working with and applying nanotechnology. It is imperative that all people involved with nanotechnology understand the proper handling and control of these materials with unusual and unique properties.

As pointed out above, there is no one source that will provide all the information desired. It takes an active role and constant updating of the latest sources to maintain current information. In rapidly developing technologies, this is always the challenge.

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