Generalized Parameter Extraction Method for Symbolic Analysis of Analog Circuits Containing Pathological Elements

Vladimir Filaretov, Konstantin Gorshkov, Sergey Kurganov and Maxim Nedorezov

Abstract This chapter gives a description of the extension of Generalized Parameter Extraction Method (GPEM) for symbolic analysis of large-scale analog circuits containing pathological elements. The brief overview of the parameter extraction approach is included. An algorithm implementing the concept of Higher Order Summative Cofactors (HOSC) for determinants computation of the pathological element-based circuits is proposed. In this chapter, we also present the hierarchical decomposition techniques of upward and downward analysis of electronic circuits by GPEM. The proposed techniques are used in freeware symbolic analyzer CirSym. Several examples are presented to illustrate the advantages of the GPEM applications.

Related topics of book: Analog circuits, circuit simulation, symbolic analysis of circuits containing pathological elements, controlled sources, nullor, voltage mirrors and current mirrors, symbolic Simulation CAD.

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1 Introduction

Most of the modern symbolic circuit analysis techniques are based on matrix calculus [1–10] or operations with circuit graph [3, 4, 10–15]. However, the usage of matrix representation or graph model may lead to the terms cancellations and produces some pseudo-dependencies in functions. In this chapter, we introduce the basics and advances of circuit analysis by parameter extraction approach which provides the effective symbolic calculation without constructing the circuit equations. Parameter extraction method was developed at the beginning of the XX century by Friedrich Wilhelm Feussner, one of the Kirchhoff's pupils. The formulae presented in [16, 17] provide the calculation of circuit determinant and doesn't need the circuit description as the matrix or topological graph. The determinant of *Z*-circuit (*y*-circuit) is defined by Feussner as the determinant of the corresponding loop impedance (nodal admittance) matrix. The diacoptic formulae for bisection of the circuit by one or two nodes were also proposed in [16] to improve the computational efficiency of parameter extraction method.

The parameter extraction approach was used in the various symbolic analysis techniques [5, 18–26]. Several researches were based on Feussner's publications [19, 23, 25–27]. M. E. Parten and R. H. Seacat proposed the method of network functions calculation of nullor-based circuit by extraction of all elements parameters until the residual circuits that contain only the norators and nullators is derived [23, 25, 26]. However, this method can be used only for active circuits with ideal operational amplifiers. The formula for extraction of controlled sources parameters was proposed by R. Hashemian in [19], but it deals with combinatorial enumeration. The Feussner's diacoptic formulae were used by S. M. Chang and G. M Wierzba for symbolic analysis of networks with nullors. However, the decomposition method proposed in [28, 29] is based on matrix manipulations and suffers from the tedious algorithm of determinant sign calculation. Also, some additional transformations of equivalent circuit are needed to use the bisection formulae in a matrix form.

The advantages of techniques of Feussner and his successors were implemented in GPEM [30–40]. GPEM is an effective tool for symbolic analysis, diagnosis, and synthesis of analog circuits. The parameter extraction cancellation-free method for symbolic analysis of switched capacitor circuits has been developed in [37]. The techniques of computation of the symbolic circuit functions sensitivities in Bode's form and in Hoang's form are described in [36]. The implementation of parameter extraction approach for symbolic circuit analysis by means of the Middlebrook's extra element theorem was proposed in [33]. The symbolic technique for analog fault diagnosis was introduced in [38]. Several GPEM-based circuit synthesis algorithms were developed: (1) an algorithm of automated synthesis of all existing equivalent pathological element-based circuits that correspond to the given polynomial network function [34]; (2) a design algorithm of OTA-based circuits [32]; (3) an algorithm of circuit synthesis using transformation of trees with pathological

elements [39]. Several GPEM-based computer programs for automated circuit analysis and synthesis were developed. The symbolic analyzer CirSym developed by V. Filaretov is available online: http://intersyn.net/en/cirsym.html.

GPEM can be successfully used for symbolic analysis of active circuits with pathological mirror elements. However, the technique proposed in [35] deals with the big amount of special cases of elements connections which complicate the symbolic analysis of large circuits. In this chapter, the new approach to the calculation of pathological element-based circuits by GPEM is presented.

The decomposition procedures can significantly increase the efficiency of symbolic analysis [4, 14, 15, 41–44]. In this chapter, we also present the hierarchical decomposition techniques of upward analysis and downward analysis of large-scale circuits by GPEM.

The chapter comprises three main sections. Section 2 introduces the basics of GPEM. The usage of parameter extraction formulae for circuit determinant expansion is discussed. The rules of degeneracy and simplification of the pathological element-based circuits are considered. Section 3 gives the application of GPEM to the generation of symbolic circuit functions in the case of Single-Input-Single-Output (SISO) and Multiple-Input-Single-Output (MISO) circuits. In Sect. 4 the extension of the method of residual circuits [23] by usage of GPEM and the concept of HOSC [22, 45] is presented. Section 5 focuses on hierarchical decomposition approaches to circuit analysis. The techniques of upward analysis and downward analysis by GPEM are proposed. The illustrative examples of usage of GPEM and its applications are included in this chapter. Conclusions summarize the results of the chapter.

2 The Basics of GPEM

2.1 *Feussner's Formulae for Determinant Expansion of the Passive Circuit*

Classic Feussner's formulae for extraction of impedance or admittance parameters are presented below [16, 17]:

$$\Delta = Z\Delta(Z \to \infty) + \Delta(Z = 0), \tag{1}$$

$$\Delta = y\Delta(y \to \infty) + \Delta(y = 0), \tag{2}$$

where Δ is a circuit determinant; $\Delta(z \to \infty)$ and $\Delta(y = 0)$ are the determinants of subcircuits in which extracted element is deleted; $\Delta(y \to \infty)$ and $\Delta(z = 0)$ are the determinants of subcircuits in which extracted element is short-circuited.

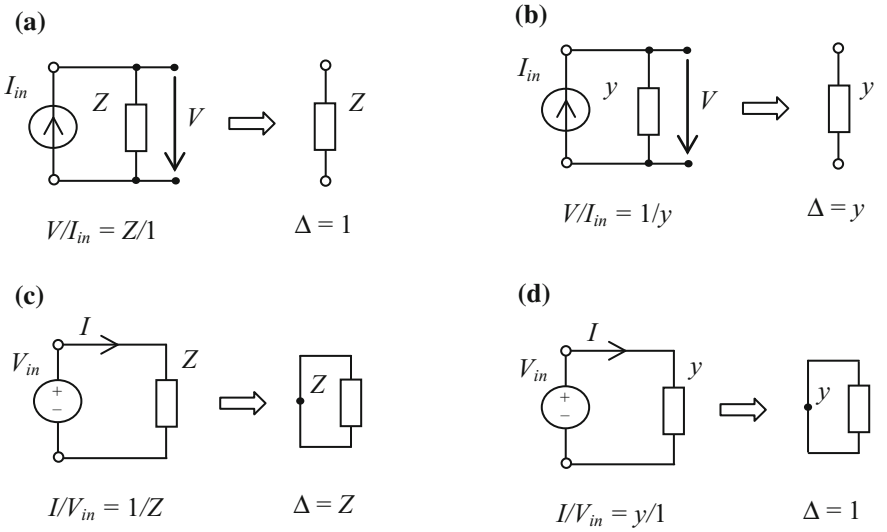
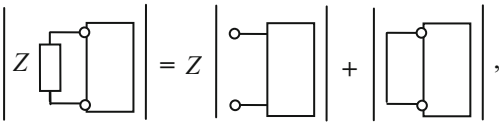


Fig. 1 The residual circuits and their determinants

Recursive usage of the formulae (1) and (2) provides the reduction of an initial circuit to several residual topologies shown in Fig. 1 which determinants can be calculated by Ohm's Law. GPEM using the complex impedance of the inductors and the complex admittance of capacitors in the Laplace domain: $Z_L = sL$ and $y_c = sC$ correspondingly.

The circuit-algebraic expressions that contain the parameters symbols, mathematical signs and derived subexpressions in the form of subcircuits, can be useful for illustration of the process of determinant expansion by parameters extraction [28]. For example, the Feussner's formulae can be expressed in the circuit-algebraic form as following:



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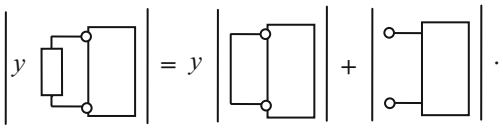

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The diacoptic approach to circuit analysis was discussed by Feussner long before the publications of G. Kron [46]. He proposed the technique of circuit decomposition

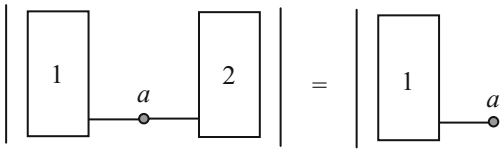
(bisection) based on following formulae for bisection of the circuit by one or two nodes correspondingly:

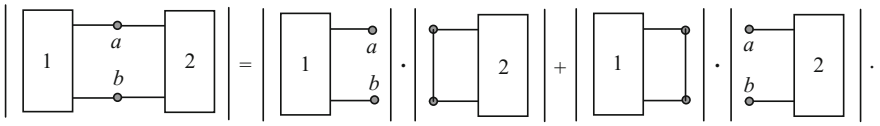
$$\Delta = \Delta_1 \Delta_2 \tag{5}$$

$$\Delta = \Delta_1 \Delta_2(a,b) + \Delta_1(a,b)\Delta_2, \tag{6}$$

where Δ_1 and Δ_2 are determinants of the first and second subcircuits in which the node a in (5) and nodes a and b in (6) are opened, $\Delta_1(a,b)$ and $\Delta_2(a,b)$ are determinants of subcircuits in which the nodes a and b are shorted.

In the circuit-algebraic form the bisection formulae by one or two nodes are shown below correspondingly:

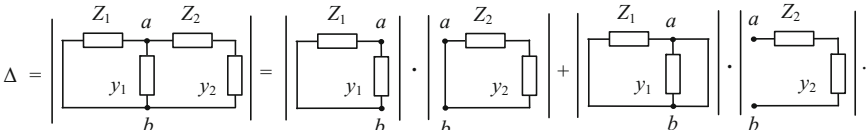




(8)

Example 1 Let's consider the determinant calculation procedure in the case of the simple two-section *LC*-ladder circuit shown in Fig. 2 to illustrate the usage of Feussner's formulae.

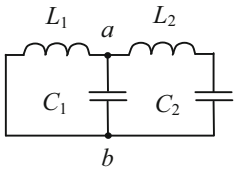
The bisection of the ladder by two nodes a and b by usage of (6) leads to the following circuit algebraic expression:

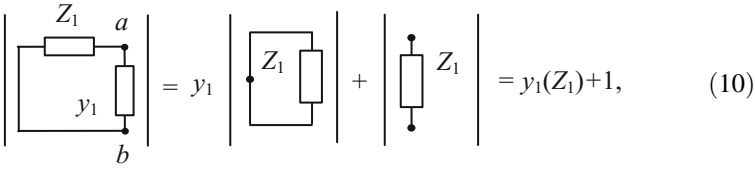


(9)

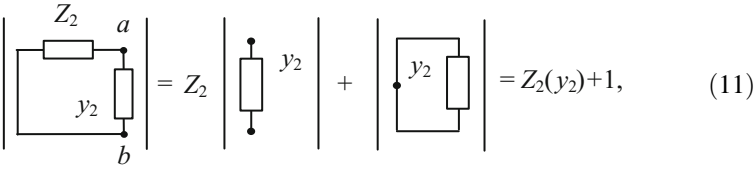
The parameter extraction procedures for determinants calculation of four subcircuits in (9) are shown below:

Fig. 2 *LC*-ladder circuit





(10)



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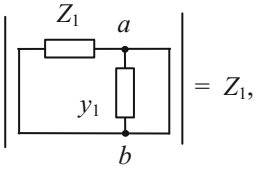

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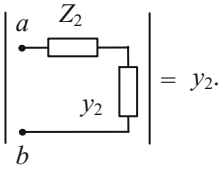


(13)

The result of the substitution of (10)–(13) into (9) can be expressed as:

$$\Delta = (y_1(Z_1) + 1)(Z_2(y_2) + 1) + Z_1 y_2. \tag{14}$$

The Feussner's formulae provide quite efficient symbolic determinant calculation of passive circuit. M. E. Parten and R. H. Seacat implemented (1) and (2) to the analysis of nullor-based circuits by extraction of all elements parameters until the residual circuits which contain only the norators and nullators [23]. The well-known equivalent transformations of parallel or series connection of norator and nullator were used for determinants computation of residual nullor circuits. However, this method can be used only for active circuits with ideal operational amplifiers. The new formula for extraction of parameters of controlled sources (CS) was needed to extend the Feussner's approach.

2.2 Extraction of Controlled Sources Parameters

The formula for the extraction of CS parameter was proposed by R. Hashemian in 1977 [19]:

$$\Delta = \chi\Delta(\chi \to \text{nullor}) + \Delta(\chi = 0), \tag{15}$$

where χ is a parameter of arbitrary CS, $\Delta(\chi \to$ nullor) is a determinant of the circuit in which a CS element is replaced by nullor, $\Delta(\chi = 0)$ is a determinant of the circuit in which the parameter of CS is equal to zero.

Hashemian has used formula (15) for simultaneous expansion of determinant by parameters of all n CS which circuit contains. Such technique leads to the enumeration of 2^n summands and cannot provides the generation of expression in the compact size.

The formula (15) was developed by V. Filaretov in 1998 irrespective of Hashemian's publication [19]. The recursive extraction of CS parameters by (15) was proposed. Also instead of original Carlin's nullor shown in Fig. 3a [47] the concept of oriented nullor, introduced in network theory by A.G. Davies [48] and J. Braun [49], is used in GPEM. The orientation of nullor provides simpler computation of the determinant expression sign of the residual nullor-based circuit as shown in Fig. 4a and b.

The oriented nullor is successfully used for calculation of network functions [49], as well as for active devices simulation [35]. For example, the equivalent circuits of voltage mirror (VM) and current mirror (CM) in which $g = 1$ are shown in Fig. 3c and Fig. 3d correspondingly. The pathological mirrors are useful ideal circuit elements for modeling active devices with voltage and current reversing [2, 7–9, 50–53].

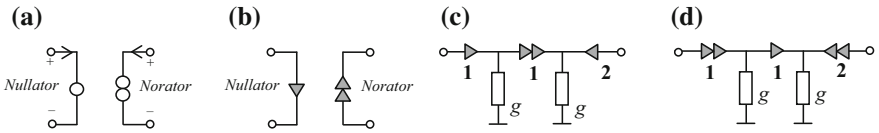


Fig. 3 Nullor symbol **a**, oriented nullor symbol **b**, the equivalent nullor circuits of pathological mirrors: VM **c** and CM **d**

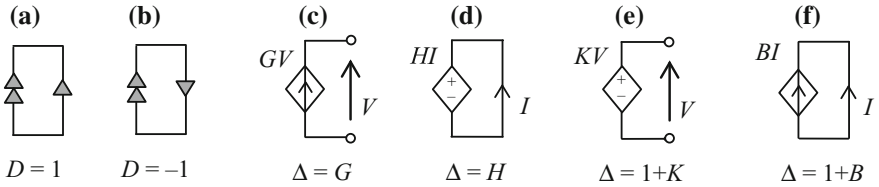
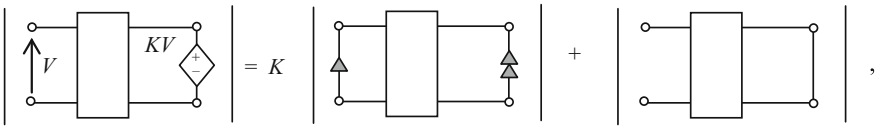


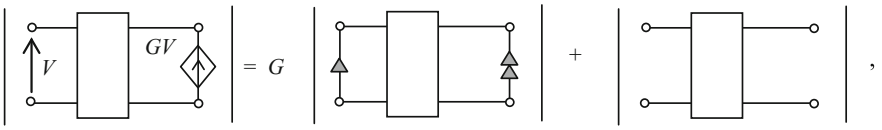
Fig. 4 The residual circuits consists of nullor **a**–**b**, controlled sources **c**–**f**

The subcircuits may include more than one oriented nullor. There are several simple rules that can help to deal with such cases: (1) enumerate the nullator-norator pairs; (2) invert the sign of determinant in the case of inversion of the norator or nullator orientation; (3) invert the sign of determinant in the case of the pair numbers interchanging between two norators or two nullators.

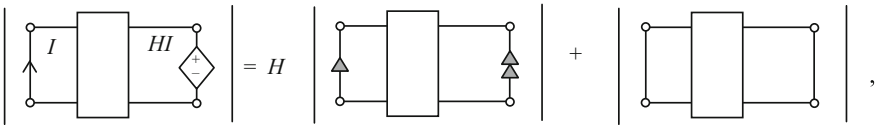
The circuit-algebraic expressions for the parameter extraction cases for each of the four depended sources, using formula (15), are shown below:



(16)



(17)



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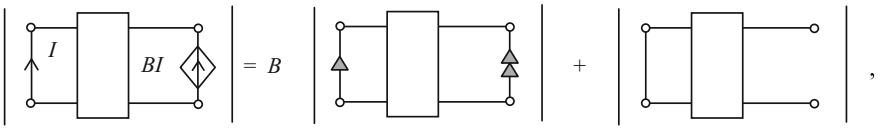


(19)

where K is a control parameter of voltage controlled voltage source (VCVS), G is a control parameter of voltage controlled current sources (VCCS), H is a control parameter of current controlled voltage source (CCVS) and B is a control parameter of current controlled current source (CCCS).

The determinant of the circuit with pathological elements can be equal to zero [28, 29, 54, 55]. Such circuits are called the degenerated circuits. The check for the degeneracy of subcircuits derived by usage of formulae (1), (2), (5), (6) and (15) is very important part of the process of symbolic analysis by GPEM.

Table 1 The circuit elements in short-circuit and in open loop

Element type	Special connection case	
	Element shorted	Element opened
Impedance	Parameter extracted – element deleted	Element shorted
Admittance	Element deleted	Parameter extracted – element shorted
Voltage source	$\Delta = 0$	Element shorted
Controlling current of CS	$\Delta = 0$	Element shorted
Current source	Element deleted	$\Delta = 0$
Controlling voltage of CS	Element deleted	$\Delta = 0$
Nullator	$\Delta = 0$	$\Delta = 0$
Norator	$\Delta = 0$	$\Delta = 0$
VM	$\Delta = 2$	$\Delta = 0$
CM	$\Delta = 2$	$\Delta = 0$

2.3 *Degeneracy and Simplification of Circuits Containing Pathological Elements*

Although topological conditions of circuit degeneracy were introduced for the first time in the mid-1970s [54, 55] the degeneracy check still can be confusing for circuit designers in the certain cases [56]. Therefore in GPEM, the generalized topological conditions are used. The determinant of circuit is equal to zero in following cases: (1) the circuit consists of several not connected subcircuits; (2) the circuit contains at least one loop consisting only of voltage sources and norators or controlling currents of CS and nullators; (3) the circuit contains at least one cross-section consisting only of the current sources and norators or controlling voltages of CS and nullators. Note that the voltage sources and current sources mentioned in topological conditions can be the input sources or depended sources as well.

The determinant of the circuit consisting only of nullors is nonzero if there is a tree which includes all of the norators while the collection of remaining branches (nullators) is the complement of such a tree and vice versa.

The degenerated circuits cannot be equivalent to each other because responses of the signal in such circuits are indeterminate. Therefore the equivalent transformation of the parallel connection of voltage source and norator into voltage source as shown in [53, 56], the transformation of the series connection of the current source and norator into current source as shown in [56], and the short-circuiting of the current source and nullator connected in series as shown in [53], are not correct.

In Tables 1 and 2 we present the special cases of elements connections derived by usage of parameter extraction formulae and topological conditions which considered above.

Table 2 The equivalent transformations of circuits containing pathological elements

	Special Case							
	In parallel with				In series with			
Element type	Norator	Nullator	VM	CM	Norator	Nullator	VM	CM
Impedance	Parameter extracted – element deleted		——	——	Element shorted			
Admittance	Element deleted		——	——	Parameter extracted – element shorted			
Voltage source	$\Delta = 0$	Nullor	——	——	Element shorted	——	——	Element shorted
Controlling current of CS	Nullor	$\Delta = 0$	——	——	——	Element shorted	Element shorted	——
Current source	Element deleted	——	——	——	$\Delta = 0$	Nullor	——	$\Delta = 0$
Controlling voltage of CS	——	Element deleted	——	——	Nullor	$\Delta = 0$	——	$\Delta = 0$
Norator	$\Delta = 0$	Nullor shorted	——	——	$\Delta = 0$	Nullor deleted	Elements deleted	$\Delta = 0$
Nullator	Nullor shorted	$\Delta = 0$	——	——	Nullor deleted	$\Delta = 0$	$\Delta = 0$	Elements deleted
VM	——	$\Delta = 2$	$\Delta = 0$	Elements shorted	Elements deleted	$\Delta = 0$	$\Delta = 0$	Elements deleted
CM	$\Delta = 2$	——	Elements shorted	$\Delta = 0$	$\Delta = 0$	Elements deleted	Elements deleted	$\Delta = 0$

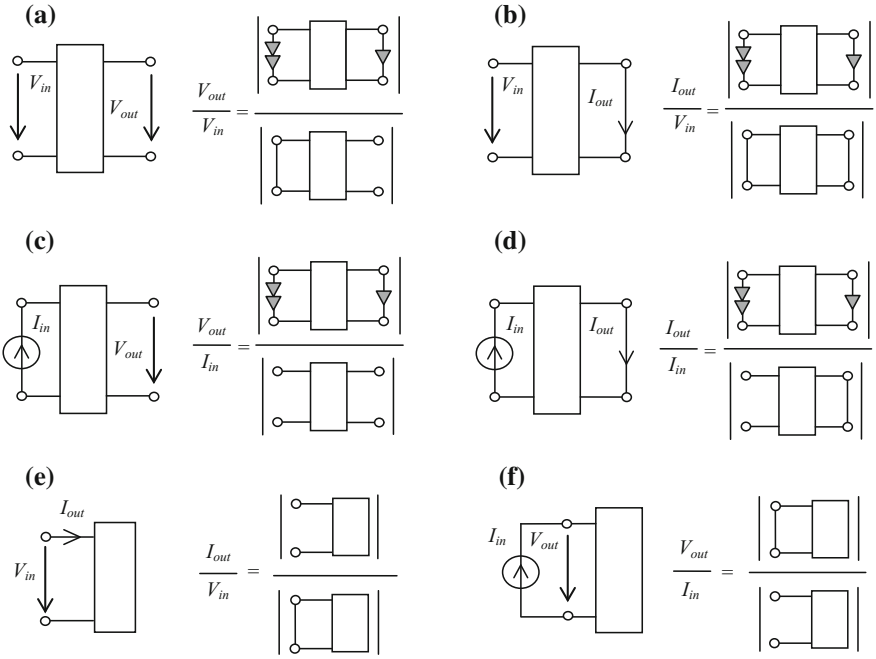


Fig. 5 The circuit-algebraic expressions of the circuit functions

3 Symbolic Circuit Analysis by GPEM

3.1 Symbolic Analysis of SISO Circuits

The network function of a linear circuit can be expressed as a ratio of two rational symbolic expressions. The numerator is the determinant of the circuit, in which the input source and response are replaced by an oriented norator and nullator correspondingly [49]. The denominator is the determinant of the circuit, in which the input and output signals are equal to zero.

The circuit-algebraic expressions for the circuit functions calculation are shown in the Fig. 5. For determinants calculation of network that contains any linear models of active circuit elements, including the controlled sources and pathological elements, the parameter extraction formulae (1), (2), (15) and bisection formulae (5)–(6) are recursively used. Each of the derived subcircuits must be checked by topological conditions for the solvability and degeneracy. As result, the residual circuits presented in Fig. 1 and Fig. 4 is obtained.

The order of parameter extraction can be chosen arbitrarily. So the calculated determinant can be presented as the rational polynomial expression if the reactive elements is extracted first.

The GPEM-based symbolic analyzer CirSym is developed by V. Filaretov. The program is freeware available in two versions: offline and online http://intersyn.net/en/cirsym.html. The input data is a slightly modified Spice-compatible netlist, which can be entered online or loaded as a cir-file. Circuit nodes should be numbered as integers. The passive impedance and admittance elements are identified by uppercase and lowercase characters correspondingly: R, L, C and g, l, c. Controlled sources are identified by following symbols: K is a parameter of VCVS, G is a parameter of VCCS, H is a parameter of CCVS and B is a parameter of CCCS. Pathological elements are identified as follows: N is a nullor, M is a VM-CM pair, T is a CM-nullator pair and Q is a norator-VM pair. Note that the input voltage source should be defined as EMF source and described by symbol E. CirSym-online provides the calculation of several circuits at once. The end of the netlist for each circuit and the end of the whole of input data are notified by strings « .end » and « .total » correspondingly.

Example 2 Let's consider the simple high-pass filter circuit containing the non-ideal OpAmp that modeled by VCVS as shown in Fig. 6. For the sake of clarity, we calculate the numerator and denominator of voltage transfer function separately.

Numerator calculation. The parameter sC_1 can be extracted from the numerator subcircuit in accordance with Table 2 due to the series connection of admittance and norator:

$$\Delta_3 = \left| \begin{array}{ccc} & g_2 & \\ sC_1 & & K_1V_1 \\ & g_1 & \end{array} \right| = sC_1 \left| \begin{array}{ccc} & g_2 & \\ sC_2 & & K_1V_1 \\ & g_1 & \end{array} \right| . \tag{20}$$

Parallel connection of voltage source of VCVS also provides simplified extraction of parameter K_1. There are two nullors in the circuit now and they must be enumerated. The interchanging of numbers between two norators leads to inversion of expression sign and provides the usage of the equivalent transformation of nullor as shown in Fig. 4a. The admittance g_2 is deleted in accordance with Table 2. The sign of determinant is changed again in the consequence of the equivalent transformation of norator and nullator which are labeled by « 2 » in accordance with Fig. 4b.

$$\Delta_3 = s^2C_1C_2K_1 \left| \begin{array}{ccc} & g_2 & \\ \mathbf{2} & & \mathbf{2} \\ \mathbf{1} & & \mathbf{1} \end{array} \right| = -s^2C_1C_2K_1 \left| \begin{array}{ccc} & & \\ g_2 & \mathbf{2} & \\ & & \mathbf{2} \end{array} \right| = s^2C_1C_2K_1. \tag{21}$$

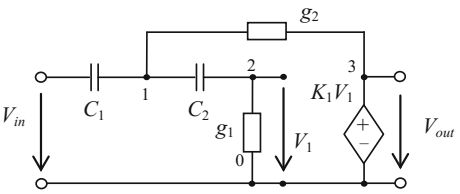
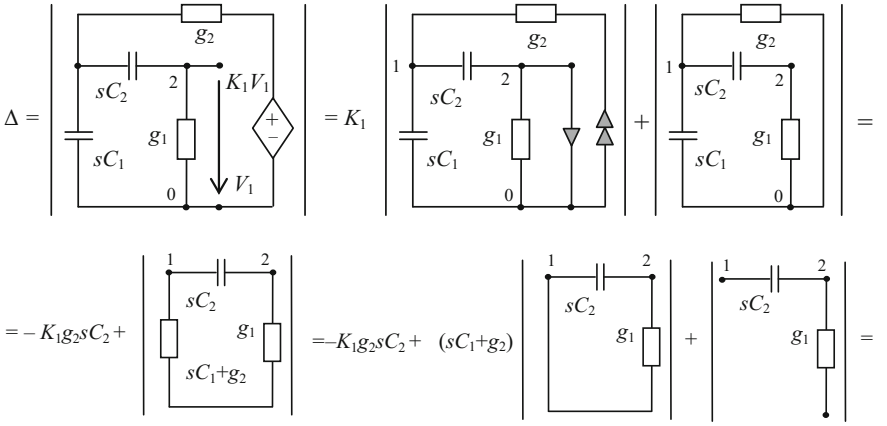


Fig. 6 VSSC-based equivalent circuit of high-pass filter

Denominator calculation. Two subcircuits that correspond to the determinants $\Delta(K_1 \rightarrow \text{nullor})$ and $\Delta(K_1 = 0)$ is derived as result of the VCVS parameter extraction by formula (15). The first subcircuit can be easily reduced to expression $-K_1 g_2 sC_2$ by usage of Tables 1 and 2. Note that the negative sign is the consequence of orientation of norator and nullator as shown in Fig. 4b. The second subcircuit can be expanded by extraction of the multibranch parameter $(sC_1 + g_2)$.



(22)

The resulting transfer function can be expressed as follows:

$$H = \frac{\Delta_3}{\Delta} = \frac{s^2 C_1 C_2 K_1}{-K_1 g_2 sC_2 + (sC_1 + g_2)(sC_2 + g_1) + sC_2 g_1}. \tag{23}$$

3.2 Symbolic Circuit Analysis of MISO Circuits

The nullator controlled multidimensional source [31] can be used for calculation of response function V_{out} of arbitrary MISO circuit that consists of n voltage sources and m current sources as shown in Fig. 7a. In that case, all of the input sources is transformed into controlled sources which will be oriented opposite [18]. All of the sources is controlled by the same nullator as shown in Fig. 7b. Parameters of input

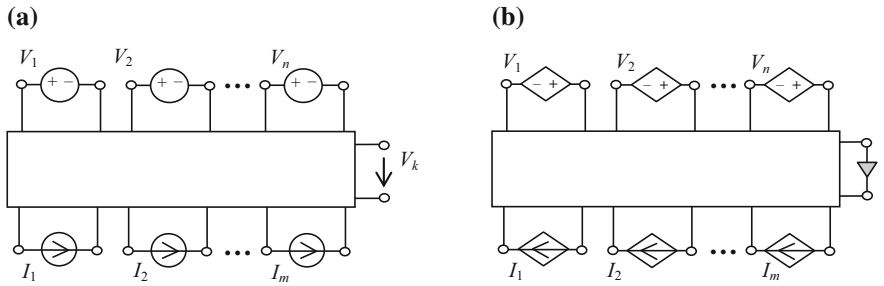


Fig. 7 The circuit with n input voltage sources and m input current sources **a**, circuit with nullator controlled multidimensional source **b**

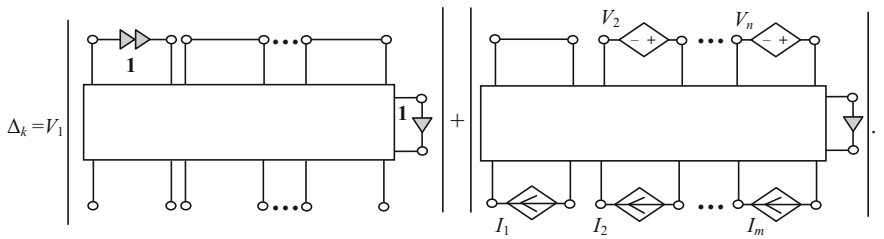
sources V_1, V_2, …, V_n and I_1, I_2, …, I_n is used as parameters of the nullator controlled multidimensional source. The properties of a nullator of a multidimensional source are the same as the properties of a standard nullator. Thus, all known operations with nullators are still valid. Obviously, the network can include only one nullator controlled multidimensional source.

The following recursive formula was proposed in [31] to calculate the numerator of k-th voltage or current function of MISO circuit:

$$\Delta_k = p_i \Delta_1 + \Delta_2. \tag{24}$$

where p_i is a source parameter V_i or I_i, Δ_1 is the determinant of network in which the source with parameter p_i corresponding to V_i or I_i is replaced by a norator, the nullator of the multidimensional source is replaced by a standard nullator, and parameters of all other sources are equal to zero; Δ_2 is the determinant of network in which the parameter of extracted source is equal to zero. Note that Δ_2 is equal to zero if all $m + n$ parameters of sources have been extracted.

Let's use the formula (15) to extract parameter V_1 in numerator circuit which is presented in Fig. 7b. As result we obtained the circuit-algebraic expression that shown below:



(25)

As can be seen from (25), the extracted voltage source in the first subcircuit is transformed into norator while parameters of others sources are equal to null. Therefore the first subcircuit contains only one nullor and can be calculated by

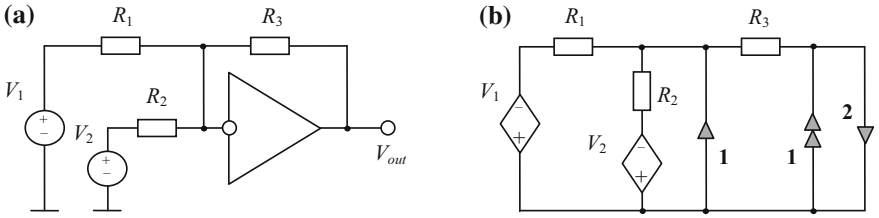
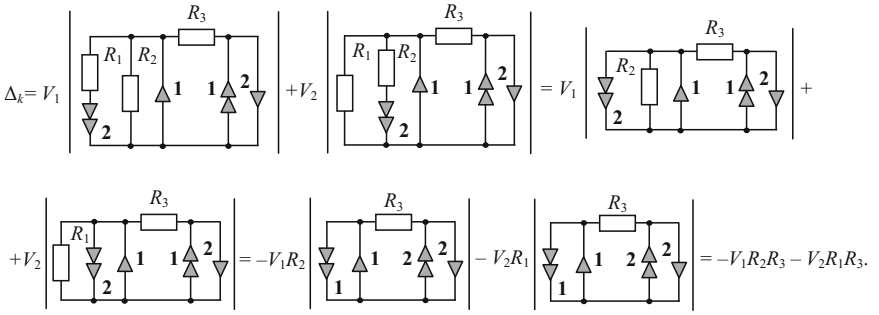


Fig. 8 **a** The summing amplifier circuit, **b** equivalent circuit with nullator controlled multidimensional source

formulae (1), (2), (15). Others sources parameters can be extracted from the second subcircuit in a similar way.

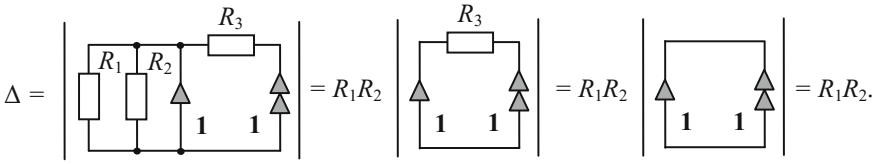
Example 3 The usage of the concept of nullator controlled multidimensional source can be explained by means of the symbolic analysis example of the summing amplifier circuit with $V_{out} = \Delta_{\underline{k}}/\Delta$ shown in Fig. 8a.

Numerator calculation. The equivalent circuit shown in Fig. 8b is used for calculation of voltage function numerator $\Delta_{\underline{k}}$ by formula (24). There are two nullor-based subcircuits as result of the extraction of parameters V_1 and V_2. The determinant expressions can be easily derived by using simplification conditions in Table 2 as follows:



(26)

Denominator calculation. The voltages of both sources V_1 and V_2 are equal to null. There is only one regular nullor in the subcircuit. The determinant expansion by using Table 2 is trivial:



(27)

4 The Technique of Determinant Expansion of Pathological Element-Based Residual Circuits

As seen from examples in previous subsections, the usage of formulae (1), (2), (5), (6) and (15) along with the conditions of circuit degradation and simplification from Tables 1 and 2 is easy, intuitive and effective especially in the case of relatively small circuits. However, the big amount of special connections of elements complicates the symbolic analysis of large subcircuits that contain only of pathological elements which are the result of extraction of all impedances, admittances, and CS. A more simple technique of determinants computation of the pathological element-based residual circuits is needed.

4.1 Expansion of Determinants of Pathological Element-Based Residual Circuits

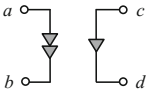
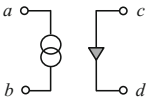
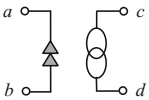
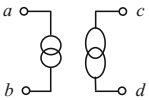
The main idea of the new approach is that the determinant of the residual circuit, which contains only the pathological elements, can be calculated by usage of matrix algebra operations instead of simplification by conditions presented in Tables 1 and 2. The connection of norator or nullator (VM or CM) to the circuit leads to the summation (subtraction) of rows or columns in circuit the admittance matrix. The rows or columns numbers correspond to the nodes numbers of the circuit. The concept of HOSC [22, 45] can be useful to represent the matrices in such operations.

The higher order cofactor is a cofactor of a cofactor. The n-th order cofactor can be identified by a symbol $\Delta_{r1,k1,r2,k2,\ldots rn,\ kn}$, where r_1, r_2, …, r_n and k_1, k_2,…, k_n are the numbers of deleted rows and columns respectively. If at least one deletion in the higher order cofactor has a summative form, then cofactor is called a higher order summative cofactor.

For example, the first-order HOSC can be described as $\Delta_{(a\pm b)(c\pm d)}$, where a and b are the numbers of rows, c and d are the numbers of columns. In the case of summation of numbers $(a + b)$ or $(c + d)$ the row a is added to row b or the column c is added to column d. In the case of subtraction of numbers $(a–b)$ or $(c–d)$ the entries of the row a or the column c is inverted before addition to the row b or to the column d correspondingly. Note, that the added row a or column c is deleted from the matrix. The following notation $\Delta_{(a+0)(c+0)}$, where zero is the number of grounded node in the circuit, means the deletion operation of the row a and column c. Obviously, $\Delta_{(a-0)(c-0)} = \Delta_{(a+0)(c+0)}$.

The matrices of pathological elements are presented in Table 3, where N is a symbol of the norator-nullator pair, Q is a symbol of the VM-norator pair, T is a symbol of the nullator-CM pair, M is a symbol of the VM-CM pair. If one of the matrix entries is null the determinant of pathological element matrix is equal to zero. In Table 3 the matrix identities for all four pathological elements in the form

Table 3 The equivalent HOSC and matrices of pathological elements

	Element type	Matrix identity in form of HOSC	Matrix elements
1	*N* (norator-nullator pair) 	$\Delta_{(a+b)(c+d)} = \Delta_{(a+0)(c+0)} + \Delta_{(b+0)(d+0)} - \Delta_{(a+0)(d+0)} - \Delta_{(b+0)(c+0)}$	| | **c** | **d** | |---|---|---| | **a** | *N* | *–N* | | **b** | *–N* | *N* |
2	*T* (nullator-CM pair) 	$\Delta_{(a-b)(c+d)} = \Delta_{(a+0)(c+0)} - \Delta_{(b+0)(d+0)} - \Delta_{(a+0)(d+0)} + \Delta_{(b+0)(c+0)}$	| | **c** | **d** | |---|---|---| | **a** | *T* | *–T* | | **b** | *T* | *–T* |
3	*Q* (VM-norator pair) 	$\Delta_{(a+b)(c-d)} = \Delta_{(a+0)(c+0)} - \Delta_{(b+0)(d+0)} + \Delta_{(a+0)(d+0)} - \Delta_{(b+0)(c+0)}$	| | **c** | **d** | |---|---|---| | **a** | *Q* | *Q* | | **b** | *–Q* | *–Q* |
4	*M* (VM-CM pair) 	$\Delta_{(a-b)(c-d)} = \Delta_{(a+0)(c+0)} + \Delta_{(b+0)(d+0)} + \Delta_{(a+0)(d+0)} + \Delta_{(b+0)(c+0)}$	| | **c** | **d** | |---|---|---| | **a** | *M* | *M* | | **b** | *M* | *M* |

of HOSC are proposed. To prove the matrix identities presented in Table 3 one can apply the Laplace's cofactor expansion.

Matrix representation of pathological elements provides the way to reduce the matrix of the residual circuit by extraction of virtual parameters that are equal in absolute values:

$$\Delta = \begin{cases} X \cdot \Delta_{(a\pm b)(c\pm d)}, & a = c \\ -X \cdot \Delta_{(a\pm b)(c\pm d)}, & a \neq c \end{cases}, \tag{28}$$

where X is a symbol of pathological element written at the intersection of rows a and b and columns c and d of the circuit matrix, $\Delta_{(a\pm b)(c\pm d)}$ is the circuit matrix transformed in accordance with Table 3.

The recursive usage of the formula (28) provides the calculation of determinant of the matrix of the residual circuit. The determinant of the non-degenerated nullor-based residual circuit can take on values $\Delta = 1$ or $\Delta = -1$. The determinant value of non-degenerated residual circuit containing pathological mirrors can be multiple of 2.

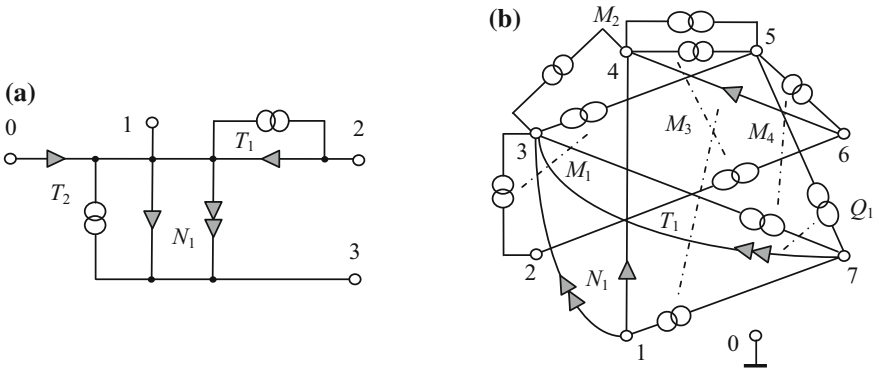


Fig. 9 The pathologic element-based residual circuits

Example 4 Suppose that the pathologic element-based circuit shown in Fig. 9a is a residual circuit of a certain network in which all of the impedances, admittances, and CS were extracted.

The HOSC list and its representation in the form of circuit matrix can be expressed as follows:

$$\Delta_{(1-2)(2+1),(1-3)(0+1),(1+3)(1+3),} \tag{29}$$

	1	2	3
1	$-T_1-T_2+N_1$	T_1	$-N_1$
2	$-T_1$	T_1	
3	$-T_2-N_1$		N_1

(30)

Let's extract T_1 from the matrix by formula (28). The symbol of the first nullator-CM pair is deleted as shown below:

	1	2	3
1	$-T_2+N_1$		$-N_1$
2			
3	$-T_2-N_1$		N_1

(31)

The subtraction of entries at rows 1 and 2 leads to inversion of the entries of row 1:

	1	2	3
2	T_2-N_1		N_1
3	$-T_2-N_1$		N_1

(32)

The result of the addition of entries in columns 2 and 1 is shown below:

	1	3
2	T_2-N_1	N_1
3	$-T_2-N_1$	N_1

(33)

Now let's rearrange the numbers of columns and rows as follows:

	2	3
2	T_2–N_1	N_1
3	$-T_2$–N_1	N_1

(34)

The number of the row a is not equal to the number of the column c ($1 \neq 2$), so in accordance with (28):

	2	3
2	$-T_2$+N_1	$-N_1$
3	T_2+N_1	$-N_1$

(35)

As seen from (35), the types of non-extracted pathological elements is changed as following $T_2 \rightarrow N_2$ and $N_1 \rightarrow T_3$:

	2	3
2	N_2+T_3	$-T_3$
3	$-N_2$+T_3	$-T_3$

(36)

Now let's extract the symbol of nullor N_2:

	2	3
2	T_3	$-T_3$
3	T_3	$-T_3$

(37)

The result of the addition of the entries in rows 2 and 3 is shown below:

	2	3
3	$2T_3$	$-2T_3$

(38)

The last step is the addition of columns 0 and 2 which leads to deletion of column 2:

	3
3	$-2T_3$

(39)

The value of the determinant is $\Delta = -2$.

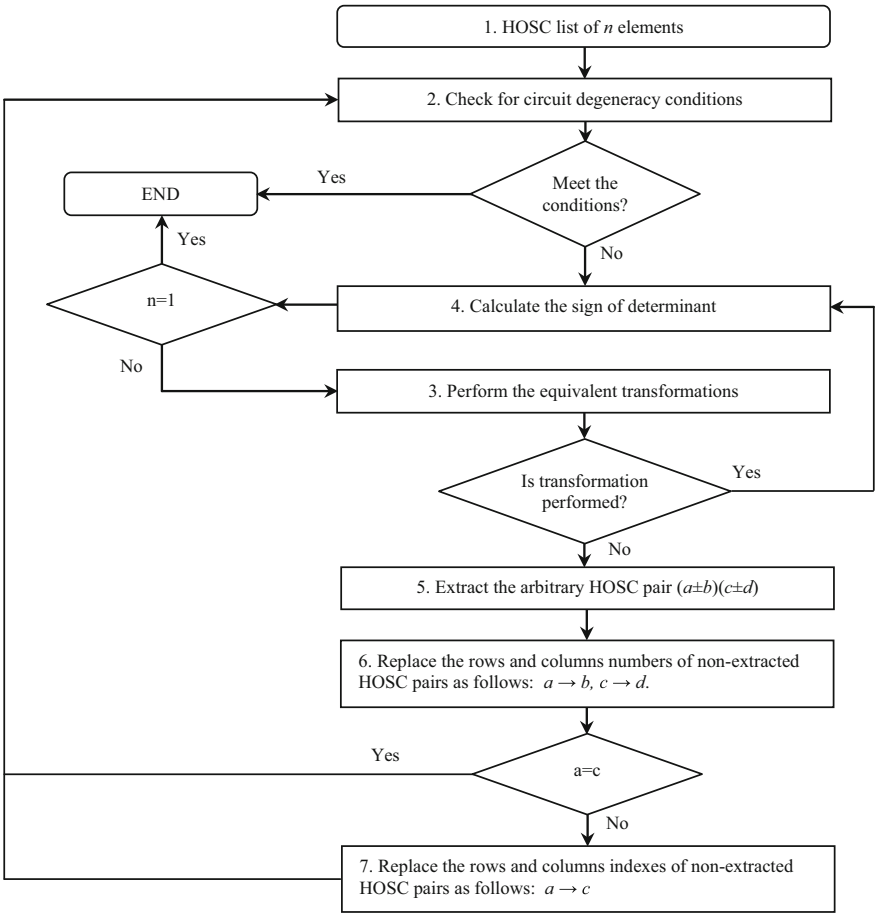


Fig. 10 The flow chart of algorithm

4.2 *The Algorithm of Determinant Expansion Directly from HOSC of Residual Circuits*

The HOCS pairs $(a \pm b)(c \pm d)$ can be extracted instead of the pathological elements symbols. The determinant expansion of residual circuits directly from HOSC is more appropriate for automatic calculation. The algorithm proposed is shown in Fig. 10. The input data is the HOSC list of a certain circuit in which all of the elements except the pathological mirrors and nullors were extracted by formulae (1), (2) and (15).

The individual aspects of analysis stages are detailed below:

1. The netlist of the residual circuit is transformed into the HOSC list.

2. At the beginning of computation process and after every extraction iteration the HOSC list must be checked for circuit degeneracy conditions. If the HOSC list includes more than one element then determinant is equal to zero in following cases:

$$(\mathrm{a}+\mathrm{a}) \rightarrow \Delta = 0; \tag{40}$$

$$(\mathrm{c}+\mathrm{c}) \rightarrow \Delta = 0. \tag{41}$$

If the HOSC list includes only one element that differs from $\Delta_{(a+b)(a+b)} = 1$ and $\Delta_{(a+b)(b+a)} = -1$, then determinant is equal to zero. For example: $\Delta_{(a+b)(c+d)} = 0$.

3. Several equivalent transformations must be performed in the HOSC list:

I. Determinant doubling (2Δ):

$$(\mathrm{a}-\mathrm{a}) \rightarrow (\mathrm{a}+0), \tag{42}$$

$$(\mathrm{c}-\mathrm{c}) \rightarrow (\mathrm{c}+0). \tag{43}$$

II. The transformations of the HOSC list elements with null summand:

$$(\mathrm{a}-0) \rightarrow (\mathrm{a}+0); \tag{44}$$

$$(\mathrm{c}-0) \rightarrow (\mathrm{c}+0); \tag{45}$$

$$(0-\mathrm{a}) \rightarrow (\mathrm{a}+0); \tag{46}$$

$$(0+\mathrm{a}) \rightarrow -(\mathrm{a}+0); \tag{47}$$

$$(0-\mathrm{c}) \rightarrow (\mathrm{c}+0); \tag{48}$$

$$(0+\mathrm{c}) \rightarrow -(\mathrm{c}+0). \tag{49}$$

III. The transformations of the HOSC list elements with the first negative number:

$$((-a)+b) \rightarrow -(b+(-a)) \rightarrow -(b-a) \rightarrow -(a-b), \tag{50}$$

$$((-a)-b) \rightarrow (b-(-a)) \rightarrow (b+a) \rightarrow -(a+b), \tag{51}$$

$$((-c)+d) \rightarrow -(d+(-c)) \rightarrow -(d-c) \rightarrow -(c-d), \tag{52}$$

$$((-c)-d) \rightarrow (d-(-c)) \rightarrow (d+c) \rightarrow -(c+d). \tag{53}$$

4. The default positive sign of determinant must be inverted in the case of transformations (47), (49), (50)–(53) or extraction of the HOCS pair $(a + b)$ $(c + d)$ in which $a \neq c$ (see step 7).

Table 4 The expansion of HOSC list (29)

Operation		HOSC list	Determinant
1	Extraction of (1, 2)(2 + 1)	$\Delta_{(1-3)(0+1),(1+3)(1+3)}$	Δ
2	Rows: 1 → –2; Col.: 2 → 1	$\Delta_{(-2-3)(0+1),(-2+3)(1+3)}$	
3	Rows and Col.:1 → 2	$\Delta_{(-2-3)(0+2),(-2+3)(2+3)}$	
4	Changing sign 1 ≠ 2	$\Delta_{(-2-3)(0+2),(-2+3)(2+3)}$	–Δ
5	Transformation by (51)	$\Delta_{(2+3)(0+2),(-2+3)(2+3)}$	Δ
6	Transformation by (50)	$\Delta_{(2+3)(0+2),(2,3)(2+3)}$	–Δ
7	Transformation by (49)	$\Delta_{(2+3)(2+0),(2,3)(2+3)}$	Δ
8	Extraction of (2 + 3)(2 + 0)	$\Delta_{(2,3)(2+3)}$	Δ
9	Rows: 2 → 3; Col.: 2 → 0	$\Delta_{(3)(0+3)}$	
10	Saving sign 2 = 2	$\Delta_{(3)(0+3)}$	Δ
11	Doubling by (42)	$\Delta_{(3+0)(0+3)}$	2Δ
12	Transformation by (49)	$\Delta_{(3+0)(3+0)}$	–2Δ
Result			**–2Δ**

5. The extraction of arbitrary HOSC pair $(a + b)(c + d)$ decreases HOSC list by one.
6. After extraction of HOCS pair $(a \pm b)(c \pm d)$ the numbers of rows of non-extracted HOSC pairs will be replaced as follow: $a \rightarrow b$. The numbers of columns is replaced in a similar way: $c \rightarrow d$. If $a = c$ the analysis procedure repeats from degeneracy checking. In the opposite case, the next step must be performed.
7. If $a \neq c$ the rows and columns numbers of non-extracted HOSC pairs is replaced as follows: $a \rightarrow c$. This operation is inverting of the sign of the determinant.

The algorithm of calculation of determinant of the residual circuit consisting of pathological elements only is implemented in circuit analyzer CirSym.

Example 5 The sequence of operations of determinant calculation of the pathologic element-based residual circuit which is shown in Fig. 9a is presented in Table 4 in accordance with the algorithm proposed.

As can be seen, the result of calculation by the expansion of HOSC list is the same as result of matrix expansion in Example 4.

Example 6 Suppose that pathologic element-based circuit shown in Fig. 9b is a residual circuit of a certain active network in which all of the impedances, admittances, and CS were extracted. The HOSC list of pathological elements is written below in the following order: N_1, M_1, M_2, M_3, M_4, Q_1, T_1.

Table 5 The expansion of HOSC list (54)

Operation		HOSC list	Determinant
1	Extraction of (1 + 3)(1 + 4)	$\Delta_{(2-3)(3-5),(3-4)(4-5),(4-5)(2-6),(5-6)(3-7),(7+3)(5-7),(7-1)(6+4)}$	Δ
2	Rows: 1 → 3; Col.: 1 → 4	$\Delta_{(2-3)(3-5),(3-4)(4-5),(4-5)(2-6),(5-6)(3-7),(7+3)(5-7),(7-3)(6+4)}$	
3	Extraction of (2, 3)(3–5)	$\Delta_{(3-4)(4-5),(4-5)(2-6),(5-6)(3-7),(7+3)(5-7),(7-3)(6+4)}$	
4	Rows: 2 → –3; Col.: 3 → –5	$\Delta_{(3-4)(4-5),(4-5)(2-6),(5-6)(-5-7),(7+3)(5-7),(7-3)(6+4)}$	$-\Delta$
5	Changing sign 2 ≠ 3		
6	Rows and Col.:2 → 3	$\Delta_{(3-4)(4-5),(4-5)(3-6),(5-6)(-5-7),(7+3)(5-7),(7-3)(6+4)}$	
7	Transformation by (53)	$\Delta_{(3-4)(4-5),(4-5)(3-6),(5-6)(5+7),(7+3)(5-7),(7-3)(6+4)}$	Δ
8	Extraction of (3, 4)(4, 5)	$\Delta_{(4-5)(3-6),(5-6)(5+7),(7-4)(5-7),(7+4)(6-5)}$	
9	Rows: 3 → –4; Col.: 4 → –5	$\Delta_{(4-5)(3-6),(5-6)(5+7),(7-4)(5-7),(7+4)(6-5)}$	$-\Delta$
10	Changing sign 3 ≠ 4		
11	Rows and Col.:3 → 4	$\Delta_{(4-5)(4-6),(5-6)(5+7),(7-4)(5-7),(7+4)(6-5)}$	
12	Extraction of (4, 5)(4–6)	$\Delta_{(5-6)(5+7),(7-4)(5-7),(7+4)(6-5)}$	
13	Rows: 4 → –5; Col.: 4 → –6	$\Delta_{(5-6)(5+7),(7+5)(5-7),(7-5)(6-5)}$	
14	Extraction of (5, 6)(5 + 7)	$\Delta_{(7+5)(5-7),(7-5)(6-5)}$	
15	Rows: 5 → –6; Col.: 5 → 7	$\Delta_{(7-6)(7-7),(7+6)(6-7)}$	
16	Doubling by (43)	$\Delta_{(7-6)(7+0),(7+6)(6-7)}$	-2Δ
17	Extraction of (7–6)(7 + 0)	$\Delta_{(7-6)(7+0),(7+6)(6-7)}$	
18	Rows: 7 → –6; Col.: 7 → 0	$\Delta_{(-6+6)(6-0)}$	
19	Transformation by (50)	$\Delta_{(6-6)(6-0)}$	2Δ
20	Doubling by (42)	$\Delta_{(6+0)(6-0)}$	4Δ
21	Transformation by (45)	$\Delta_{(6+0)(6+0)}$	
Result			**4Δ**

$$\Delta_{(1+3)(1+4),(2-3)(3-5),(3-4)(4-5),(4-5)(2-6),(5-6)(3-7),(7+3)(5-7),(7-1)(6+4)}. \quad (54)$$

The sequence of operations of determinant calculation is presented in Table 5.

The obtained results of examples which considered above are confirmed by usage of CirSym.

5 Circuit Decomposition in GPEM

There are two hierarchical decomposition approaches to circuit analysis. The first one is called upward analysis and it is based on the combination of subcircuits [44]. The downward analysis deals with recursive usage of circuit bisection. Both of decomposition approaches are implemented in GPEM. The upward analysis provides the generation of circuit function in the form of sequence of expressions (SoE). Many symbolic circuit analysis techniques provide the solution in the form of SoE [1, 5, 6, 44, 57–59] and the sequence can be made very compact [59]. The single nested expression of circuit function can be obtained by downward analysis.

5.1 The Downward Analysis

In this section, we present the generalized topological approach to circuit bisection which can be explained by matrix decomposition procedures. Let's consider the arbitrary fully populated matrices **A**, **B**, and **C = A+B** of the same order $n = 3$. The determinant of **C** can be expressed as shown below:

$$\det(\mathbf{C}) = \begin{vmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{vmatrix} = \begin{vmatrix} a_{11}+b_{11} & a_{12}+b_{12} & a_{13}+b_{13} \\ a_{21}+b_{21} & a_{22}+b_{22} & a_{23}+b_{23} \\ a_{31}+b_{31} & a_{32}+b_{32} & a_{33}+b_{33} \end{vmatrix}. \quad (55)$$

The expression (55) can be transformed in consequence of linearity of the determinant as follows:

$$\begin{aligned} \det(\mathbf{C}) = &\begin{vmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{vmatrix} + \begin{vmatrix} a_{11} & a_{12} & b_{13} \\ a_{21} & a_{22} & b_{23} \\ a_{31} & a_{32} & b_{33} \end{vmatrix} + \begin{vmatrix} a_{11} & b_{12} & a_{13} \\ a_{21} & b_{22} & a_{23} \\ a_{31} & b_{32} & a_{33} \end{vmatrix} + \begin{vmatrix} b_{11} & a_{12} & a_{13} \\ b_{21} & a_{22} & a_{23} \\ b_{31} & a_{32} & a_{33} \end{vmatrix} + \\ + &\begin{vmatrix} a_{11} & b_{12} & b_{13} \\ a_{21} & b_{22} & b_{23} \\ a_{31} & b_{32} & b_{33} \end{vmatrix} + \begin{vmatrix} b_{11} & a_{12} & b_{13} \\ b_{21} & a_{22} & b_{23} \\ b_{31} & a_{32} & b_{33} \end{vmatrix} + \begin{vmatrix} b_{11} & b_{12} & a_{13} \\ b_{21} & b_{22} & a_{23} \\ b_{31} & b_{32} & a_{33} \end{vmatrix} + \begin{vmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \end{vmatrix}, \end{aligned} \quad (56)$$

or more briefly as

$$\det(\mathbf{C}) = \det(\mathbf{A}+\mathbf{B}) = \det\mathbf{A} + \sum\Delta(1) + \sum\Delta(2) + \ldots + \sum\Delta(k) + \ldots + \sum\Delta(n-1) + \det\mathbf{B}, \quad (57)$$

where $\Delta(k)$ is the determinant derived by operation of replacement of all the entries of k columns of matrix $\mathbf{A}$ by the entries of corresponding columns of matrix $\mathbf{B}$. The sum in (57) is the sum over all possible combinations of k columns in $\mathbf{A}$ and $\mathbf{B}$.

In accordance with Laplace theorem if we are given a selection of k rows i_1, i_2, …, i_k of a square n-order matrix $\mathbf{M}$ the determinant can be characterized as the sum [60]:

$$\Delta = (-1)^{\sum_{z=0}^{k} i_z + \sum_{z=0}^{k} j_z} M_{j_1,j_2,\ldots,j_k}^{i_1,i_2,\ldots,i_k} \overline{M}_{j_1,j_2,\ldots,j_k}^{i_1,i_2,\ldots,i_k}, \quad (58)$$

where $j_1, j_2, \ldots, j_k$ specify the columns of $\mathbf{M}$, $\overline{M}_{j_1,j_2,\ldots,j_k}^{i_1,i_2,\ldots,i_k}$ is the complementary minor of the minor $M_{j_1,j_2,\ldots,j_k}^{i_1,i_2,\ldots,i_k}$. Note that the columns vary over all possible combinations of k columns.

The Eq. (57) can be expressed by usage of (58) as following [61]:

$$\det(\mathbf{C}) = \det(\mathbf{A}+\mathbf{B}) = \det\mathbf{A} + \sum_{k=1}^{n-1} \sum (-1)^{\sum_{z=0}^{k} i_z + \sum_{z=0}^{k} j_z} B_k \overline{A_k} + \det\mathbf{B}, \quad (59)$$

where B_k is the minor of order k of matrix $\mathbf{B}$, $\overline{A_k}$ is the complementary minor of (n–k) order formed by the determinant of the matrix $\mathbf{A}$ from which k rows and columns associated with minor B_k have been removed.

The expression (59) seems not quite effective for determinant expansion of the fully populated matrix. But the circuit matrix usually is sparse. Thereby the formula (59) can be quite useful for the symbolic circuit analysis by hierarchical decomposition. Let's consider the graphical models of arbitrary circuit matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C} = \mathbf{A}+\mathbf{B}$ of the same order n which are presented in Fig. 11. The parameters of circuits' elements are written in the entries in the shaded areas of matrices $\mathbf{A}$ and $\mathbf{B}$. The values of the entries in the non-shaded areas are equal to null. The intersection of the rows and columns, which corresponds to the common nodes of

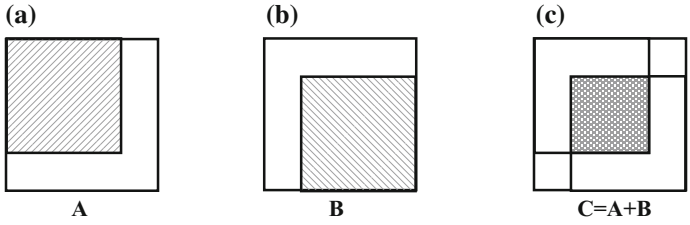


Fig. 11 The graphical models of arbitrary circuit matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C} = \mathbf{A}+\mathbf{B}$

circuits is shown as the double-shaded area in matrix **C**. Suppose that the set of common nodes includes the grounded node. Thereby for determinant calculation of circuit matrix **C** by (59), we can use only the minors and cofactors that correspond to the common nodes of subcircuits. The other minors and cofactors are equal to zero.

The Feussner's diacoptic formulae (5) and (6) represent the particular cases of circuit bisection. The operation of short-circuiting of the nodes a and b in bisection formula (6) is equivalent to a parallel connection of norator and nullator into those nodes, which causes the deletion of the correspondent column and the row of subcircuit matrix [62]. Therefore, the derived subcircuit may be called a «minor of circuit» by analogy with the term «minor of matrix». The symbolic expression of minor of the circuit can be calculated using formulae (1), (2) and (15).

The binary arrays represent the minors of the circuit with m number of external nodes; one of which is considered as a grounded node. The dimension of an array is $2n$, where $n = (m–1)$. The first n elements of the binary array form the norator vector and the last n elements form the nullator vector. There are two possible values for each element of vector: 0 or 1. The unity value of some entry of norator (nullator) vector means that norator (nullator) is inserted into the circuit between the correspondent node and grounded node. The norator and nullator of the inserted nullor are oriented in the same direction. In the case of zero value, the node is in open loop. The positions of entries in the vector can be presented by the tuple that consists of labels of a subcircuit external nodes excluding the basic node.

The number of binary arrays for an arbitrary subcircuit can be calculated by the formula:

$$v = \sum_{i=0}^{n} \binom{i}{n}^2, \tag{60}$$

where $\binom{i}{n}$ is a binomial coefficient.

The bisection formula (59) can be transformed by usage of the binary arrays concept for decomposition of the circuit by m nodes as follows:

$$\sum_{i=1}^{v} \delta_i \Delta_1(b_i) \Delta_2(\overline{b_i}), \tag{61}$$

where $\Delta_1(b_i)$ is a first subcircuit minor which corresponds to the binary array b_i; $\Delta_2(\overline{b_i})$ is a second subcircuit minor which corresponds to the binary array $\overline{b_i}$.

The norators and nullators that are inserted into the circuit minors can be enumerated in accordance with the values of the entries in the corresponding binary array. The binary array that corresponds to the circuit minors with enumerated

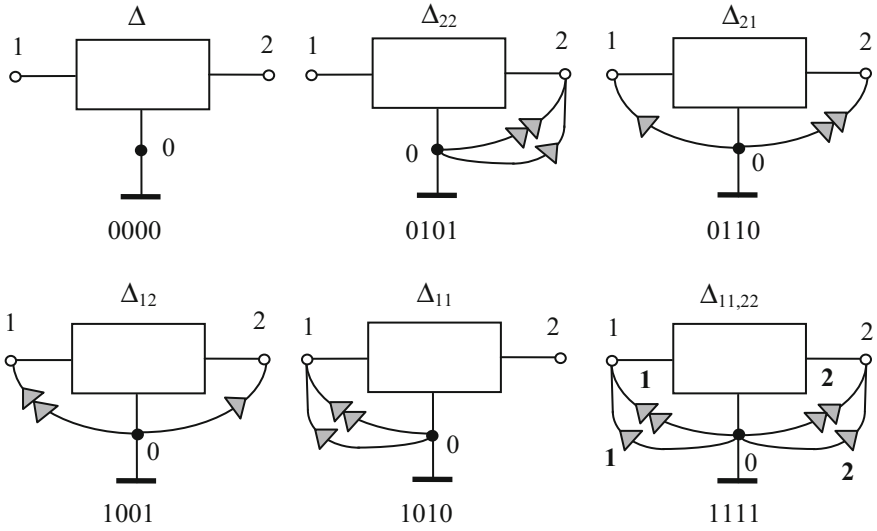


Fig. 12 The circuit minors and binary arrays of three-node subcircuit

nullors is called the enumerated binary array. Instead of nullator and norator connection information, this array contains nullor number which particular nullator and norator belong to. For example, the binary array $b = 110101$ of some circuit minor includes the two nullors labeled by « 1 » and « 2»; using those numbers binary array can be transformed into the following enumerated binary array: $b' = 120102$.

The nullor circuit that corresponds to the sum of two enumerated binary arrays, is consist of n norator-nullator pairs, connected in parallel. Norator-nullator pairs must be labeled by the same number to use the nullor simplification. If the labels of a norator and nullator of certain nullor are different the permutation of labels in the sum result of two enumerated binary arrays is needed. The determinant of nullor circuit is $\delta = 1$ if the amount of such permutations is even. In the opposite case, the sign of the product of $\Delta_1(b_i)$ and $\Delta_2(\overline{b}_i)$ in (61) is negative.

In the case of circuit bisection by three nodes ($n = 2$) the dimension of binary arrays is $2n = 4$. The six binary arrays which are presented in Fig. 12 can be derived as the result of bisection. They are corresponding to the circuit minors of

Table 6 The binary arrays, the enumerated binary arrays, the sum results of enumerated binary arrays and the determinants values in the case of circuit bisection by 3 nodes

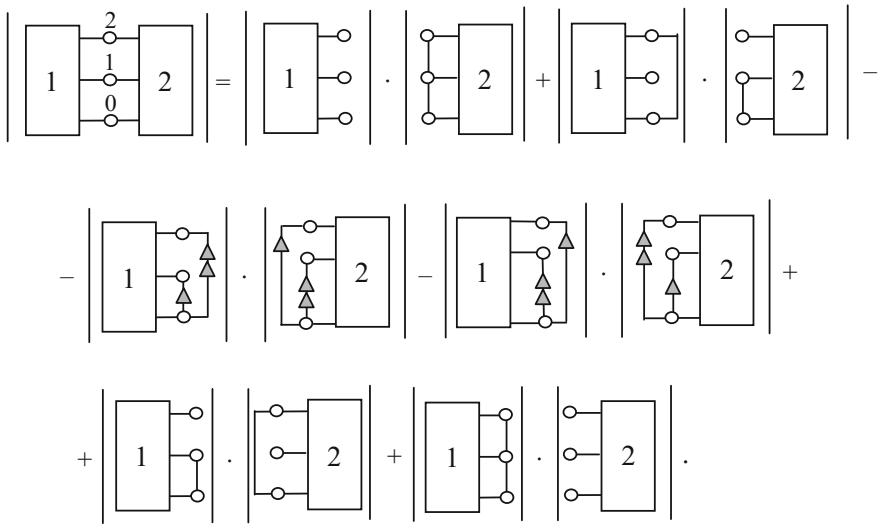
i	b_i	$\overline{b_i}$	b_i'	$\overline{b_i'}$	$b_i' + \overline{b_i'}$	δ_i
1	0000	1111	0000	1212	1212	1
2	0101	1010	0101	2020	2121	1
3	0110	1001	0110	2002	2112	–1
4	1001	0110	1001	0220	1221	–1
5	1010	0101	1010	0202	1212	1
6	1111	0000	1212	0000	1212	1

the first subcircuit in (61). The binary arrays of the second subcircuit can be obtained by operation of the one's complement of the binary number. The tuple of common (or external) nodes of subcircuits can be written as 1212. The binary arrays, their enumerated forms, the sum results of two enumerated binary arrays and the determinants values of corresponding nullor circuits are presented in Table 6.

The decomposition formula (61) in the case of bisection by three nodes can be expressed as follows:

$$\begin{aligned}\Delta = {} & \Delta_1(b_1)\Delta_2(\overline{b}_1) + \Delta_1(b_2)\Delta_2(\overline{b}_2) - \Delta_1(b_3)\Delta_2(\overline{b}_3) - \\ & - \Delta_1(b_4)\Delta_2(\overline{b}_4) + \Delta_1(b_5)\Delta_2(\overline{b}_5) + \Delta_1(b_6)\Delta_2(\overline{b}_6).\end{aligned} \tag{62}$$

The circuit-algebraic form of (62) is presented below:



(63)

Let's consider the case of circuit bisection by four nodes ($n = 3$) as shown in Fig. 13a. The dimension of binary arrays is $2n = 6$. The binary arrays in which the number of unities in norator vector differs from a number of unities in nullator

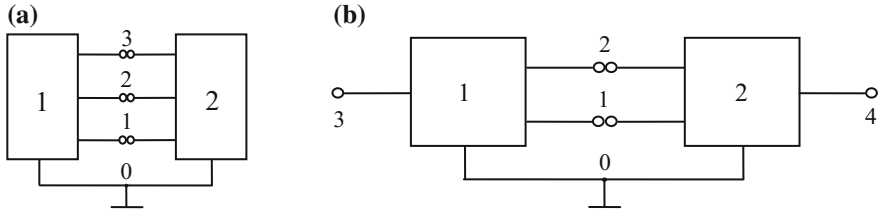


Fig. 13 The model of circuit bisection by four nodes **a**, the model of combination of two subcircuits **b**

vector are excluded from search space 000000 to 111111 in accordance with (60). Thereby twenty binary arrays for each of subcircuit are presented in Table 7, as well as their enumerated forms, the sum results of two enumerated binary arrays and the determinants values of corresponding nullor circuits.

The decomposition formula (61) in the case of bisection by four nodes can be expressed as follows:

$$\Delta = \Delta_1(b_1)\Delta_2(\overline{b}_1) + \Delta_1(b_2)\Delta_2(\overline{b}_2) - \Delta_1(b_3)\Delta_2(\overline{b}_3) + \Delta_1(b_4)\Delta_2(\overline{b}_4) - \Delta_1(b_5)\Delta_2(\overline{b}_5) + \Delta_1(b_6)\Delta_2(\overline{b}_6) - \Delta_1(b_7)\Delta_2(\overline{b}_7) + \Delta_1(b_8)\Delta_2(\overline{b}_8) - \Delta_1(b_9)\Delta_2(\overline{b}_9) + \Delta_1(b_{10})\Delta_2(\overline{b}_{10}) + \Delta_1(b_{11})\Delta_2(\overline{b}_{11}) - \Delta_1(b_{12})\Delta_2(\overline{b}_{12}) + \Delta_1(b_{13})\Delta_2(\overline{b}_{13}) - \Delta_1(b_{14})\Delta_2() + \Delta_1(b_{15})\Delta_2(\overline{b}_{15}) - \Delta_1(b_{16})\Delta_2(\overline{b}_{16}) + \Delta_1(b_{17})\Delta_2(\overline{b}_{17}) - \Delta_1(b_{18})\Delta_2(\overline{b}_{18}) + \Delta_1(b_{19})\Delta_2(\overline{b}_{19}) + \Delta_1(b_{20})\Delta_2(\overline{b}_{20}). \quad (64)$$

The bisection operation by the proposed formula (61) can be used for every derived circuit minors provides the downward hierarchical decomposition of the circuit for closed-form determinant expressions calculation. Note, that the input-port and output-port of certain CS, nullor or pathological mirrors pair, cannot be included separately in different subcircuits.

5.2 The Upward Hierarchical Analysis

The upward hierarchical analysis by GPEM starts from the decomposition of the circuit by bisection formula (61) and follows by the pairwise combination of subcircuits. The binary arrays and corresponding circuit minors are used for the representation of subcircuits. Suppose two n-port circuits combined into one circuit by m ports, which may be called the common nodes. Let's consider the input and output ports of the circuit as external nodes. Some of the common nodes of the combined circuit can be also the external nodes.

The following algorithm is used for the combination of two subcircuits:

1. Generate the set of binary arrays for each of subcircuits.
2. Perform the pairwise comparison of binary arrays using the entries that correspond to common nodes of subcircuits to find the pairs of joint binary arrays. Two binary arrays are called jointed if the entries values that correspond to the common nodes are complementary and the sum of those values is not equal to zero.
3. Generate the set of binary arrays of the combined circuit using joint binary arrays. The values of binary arrays must be written in accordance with circuit tuple in the following order: firstly, the values of binary arrays which correspond to the non-common external nodes of the first subcircuit, next, the values of the binary arrays which correspond to the common nodes, and, finally, the values of the binary arrays which correspond to the non-common external nodes of the second subcircuit. The unity must be written into binary array

entries that correspond to the common external nodes of the combined circuit if there are the unity values in the corresponding entries of the joint binary arrays.
4. Calculate the sign of circuit minors product represented by joint binary arrays according to (61). The sign is positive if the number of permutations in the enumerated joint binary arrays is even and vice versa. If the values of entries that correspond to the common external nodes are equal to unity in both joint binary arrays then the unity values of such entries in one of the binary arrays must be replaced by zero.
5. Summarize the circuit minors products that correspond to the pairs of joint binary arrays for each of combined circuit minors.

Let's consider the following example to illustrate the usage of the proposed algorithm. The circuit with three nodes labeled by 3, 4 and 0 shown in Fig. 13b is obtained by combining two subcircuits 1 and 2 with four external nodes. Thereby the dimension of binary arrays is equal to 6 in the case of the separated subcircuits and to 4 in the case of the combined circuit.

A number of external nodes is the same in both subcircuits, therefore we can use the set of binary arrays from the second column in Table 7. The tuples of binary arrays of first and second subcircuits can be expressed as 312312 and 124124

Table 7 The binary arrays, the enumerated binary arrays, the sum results of enumerated binary arrays and the determinants values in the case of circuit bisection by 4 nodes

i	b_i	$\overline{b}_i$	$b_i^{'}$	$\overline{b_i^{'}}$	$b_i^{'}+\overline{b_i^{'}}$	δ_i
1	000000	111111	000000	123123	123123	1
2	001001	110110	001001	230230	231231	1
3	001010	110101	001010	230203	231213	–1
4	001100	110011	001100	230023	231123	1
5	010001	101110	010001	203230	213231	–1
6	010010	101101	010010	203203	213213	1
7	010100	101011	010100	203023	213123	–1
8	011011	100100	012012	300300	312312	1
9	011101	100010	012102	300030	312132	–1
10	011110	100001	012120	300003	312123	1
11	100001	011110	100001	023230	123231	1
12	100010	011101	100010	023203	123213	–1
13	100100	011011	100100	023023	123123	1
14	101011	010100	102012	030300	132312	–1
15	101101	010010	102102	030030	132132	1
16	101110	010001	102120	030003	132123	–1
17	110011	001100	120012	003300	123312	1
18	110101	001010	120102	003030	123132	–1
19	110110	001001	120120	003003	123123	1
20	111111	000000	123123	000000	123123	1

correspondingly. Obviously, we need to take into account only the entries 1212 that correspond to the common nodes of subcircuits to find the set of joint binary arrays pairs and their signs. For example, two binary arrays $b_2 = 001001$ and $b_{13} = 100100$ are jointed because their values at the entries 1212 are mutually complementary: 0101 and 1010. The sign can be calculated by summation of values at the entries of the binary arrays 1212 in the enumerated form: 0101 + 2020 = 2121. Thereby the sign of the product of two circuit minors $D_1(b_2)$ $\bullet D_2(b_{13})$ is positive.

Let's consider another pair of joint binary arrays $b_5 = 010001$ and $b_9 = 011101$. The values at the entries 1212 are 1001 and 0110 correspondingly. The sum result of entries in the enumerated form is 1221, therefore the sign of the product of two circuit minors $D_1(b_5)\bullet D_2(b_9)$ is negative.

The tuple of binary arrays of the combined circuit consists of labels of non-common external nodes: 3434. The values at such entries in the joint binary arrays are used to generate the combined circuit binary arrays. For example, the values of b_2 and b_{13} at the entries 3434 are 0000. The binary array 0101 of the combined circuit corresponds to the combination of the pair: b_5 and b_9. The binary arrays of combined circuit and corresponding joint binary arrays are presented in Table 8.

The circuit minors of combined circuit can be calculated in accordance with Table 8 as following:

$$\begin{gathered}
\Delta(0000) = \Delta_1(b_1)\Delta_2(b_{19}) + \Delta_1(b_2)\Delta_2(b_{13}) - \Delta_1(b_3)\Delta_2(b_{12}) - \Delta_1(b_5)\Delta_2(b_9) + \Delta_1(b_6)\Delta_2(b_8) + \Delta_1(b_8)\Delta_2(b_2),\\
\Delta(0101) = \Delta_1(b_1)\Delta_2(b_{20}) + \Delta_1(b_2)\Delta_2(b_{15}) - \Delta_1(b_3)\Delta_2(b_{14}) - \Delta_1(b_5)\Delta_2(b_9) + \Delta_1(b_6)\Delta_2(b_8) + \Delta_1(b_8)\Delta_2(b_2),\\
\Delta(0110) = \Delta_1(b_4)\Delta_2(b_{16}) - \Delta_1(b_7)\Delta_2(b_{10}) + \Delta_1(b_9)\Delta_2(b_4) - \Delta_1(b_{10})\Delta_2(b_3),\\
\Delta(1001) = \Delta_1(b_{11})\Delta_2(b_{18}) - \Delta_1(b_{12})\Delta_2(b_{17}) + \Delta_1(b_{14})\Delta_2(b_{11}) - \Delta_1(b_{17})\Delta_2(b_5),\\
\Delta(1010) = \Delta_1(b_{13})\Delta_2(b_{17}) + \Delta_1(b_{15})\Delta_2(b_{13}) - \Delta_1(b_{16})\Delta_2(b_{12}) - \Delta_1(b_{18})\Delta_2(b_7) + \Delta_1(b_{19})\Delta_2(b_6) + \Delta_1(b_{20})\Delta_2(b_1),\\
\Delta(1111) = \Delta_1(b_{13})\Delta_2(b_{20}) + \Delta_1(b_{15})\Delta_2(b_{15}) - \Delta_1(b_{16})\Delta_2(b_{14}) - \Delta_1(b_{18})\Delta_2(b_9) + \Delta_1(b_{19})\Delta_2(b_8) + \Delta_1(b_{20})\Delta_2(b_2).
\end{gathered} \tag{65}$$

As seen from (65), generation of SoE by proposed algorithm involves a large number of calculations of circuit minors. However, decomposition of the circuit with nullors can be simplified by using degeneracy conditions [29]. Thereby the number of circuit minors can be significantly reduced by using the following rules:

1. The zero value must be written in norator vector of subcircuit binary array at the entry that corresponds to the external node a if there is a norator of certain nullor or VM between nodes a and 0 in the subcircuit.
2. The unity value must be written in norator vector of subcircuit binary array at the entry that corresponds to the common external node a if there is a norator of certain nullor or VM between nodes a and 0 in the second subcircuit.
3. The zero value must be written in nullator vector of subcircuit binary array at the entry which corresponds to the external node a if there is a nullator of certain nullor or CM is connected between nodes a and 0 in the subcircuit.

Table 8 The joint binary arrays of subcircuits 1 and 2 and binary arrays of combined circuit

The binary arrays of combined circuit (tuple 3434)	The joint binary arrays of subcircuits 1 and 2		δ
	The tuple 312312	The tuple 124124	
0000	$b_1 = 000000$	$b_{19} = 110110$	1
	$b_2 = 001001$	$b_{13} = 100100$	1
	$b_3 = 001010$	$b_{12} = 100010$	–1
	$b_5 = 010001$	$b_7 = 010100$	–1
	$b_6 = 010010$	$b_6 = 010010$	1
	$b_8 = 011011$	$b_1 = 100100$	1
0101	$b_1 = 000000$	$b_{20} = 000000$	1
	$b_2 = 001001$	$b_{15} = 101101$	1
	$b_3 = 001010$	$b_{14} = 101011$	–1
	$b_5 = 010001$	$b_9 = 011101$	–1
	$b_6 = 010010$	$b_8 = 011011$	1
	$b_8 = 011011$	$b_2 = 001001$	1
0110	$b_4 = 001100$	$b_{16} = 101110$	1
	$b_7 = 010100$	$b_{10} = 011110$	–1
	$b_9 = 011101$	$b_4 = 001100$	1
	$b_{10} = 011110$	$b_3 = 001010$	–1
1001	$b_{11} = 100001$	$b_{18} = 110101$	1
	$b_{12} = 100010$	$b_{17} = 110011$	–1
	$b_{14} = 101011$	$b_{11} = 100001$	1
	$b_{17} = 110011$	$b_5 = 010001$	1
1010	$b_{13} = 100100$	$b_{19} = 110110$	1
	$b_{15} = 101101$	$b_{13} = 100100$	1
	$b_{16} = 101110$	$b_{12} = 100010$	–1
	$b_{18} = 110101$	$b_7 = 010100$	–1
	$b_{19} = 110110$	$b_6 = 010010$	1
	$b_{20} = 000000$	$b_1 = 000000$	1
1111	$b_{13} = 100100$	$b_{20} = 000000$	1
	$b_{15} = 101101$	$b_{15} = 101101$	1
	$b_{16} = 101110$	$b_{14} = 101011$	–1
	$b_{18} = 110101$	$b_9 = 011101$	–1
	$b_{19} = 110110$	$b_8 = 011011$	1
	$b_{20} = 000000$	$b_2 = 001001$	1

4. The unity value must be written in nullator vector of subcircuit binary array at the entry that corresponds to the common external node a if there is a norator of certain nullor or CM between nodes a and 0 in the second subcircuit.

For example, suppose that in three-node nullor-equivalent subcircuit there is norator which is connected between nodes 2 and 0. In accordance with proposed

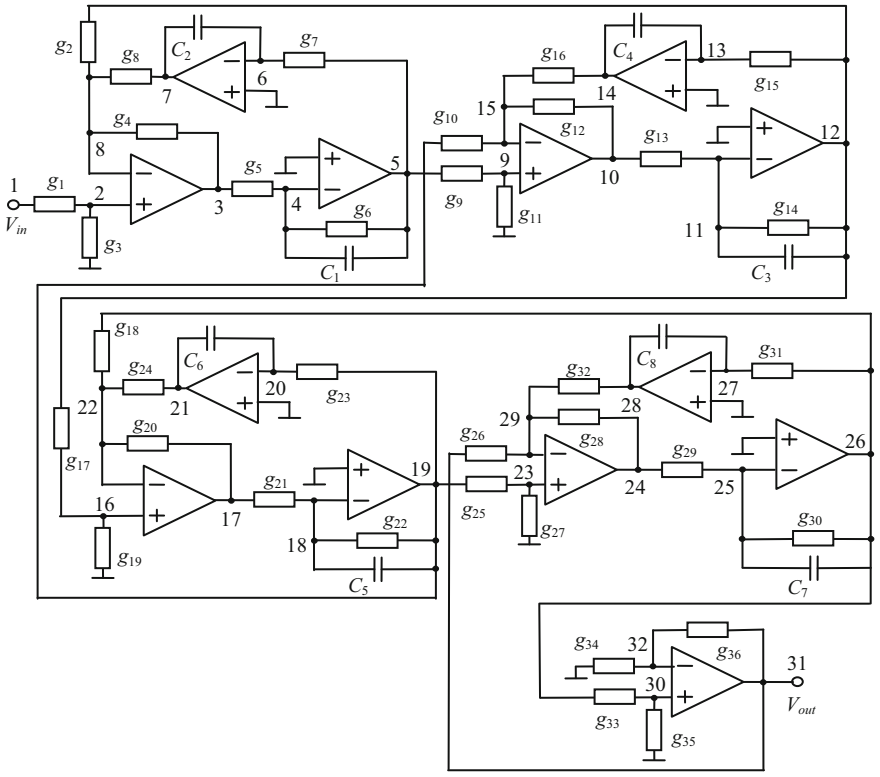


Fig. 14 The band-pass filter [44]

rules, only three binary arrays is generated instead of six which presented in Table 6: 0000, 1001, 1010.

Example 7 Let's consider the band-pass filter shown in Fig. 14, which was firstly symbolically calculated in the paper [44] by J. A. Starzyk and A. Konczykowska. This is a well-known test circuit for symbolic analysis methods. It contains 13

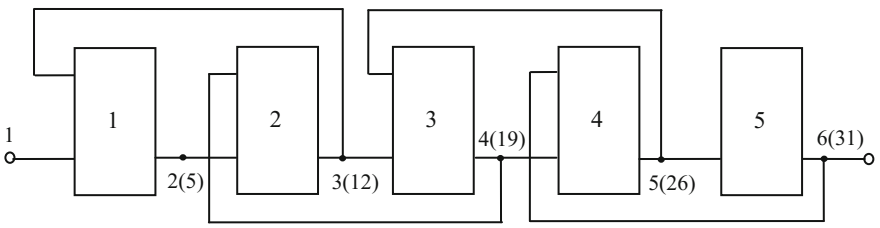


Fig. 15 The subcircuit-level model of band-pass filter

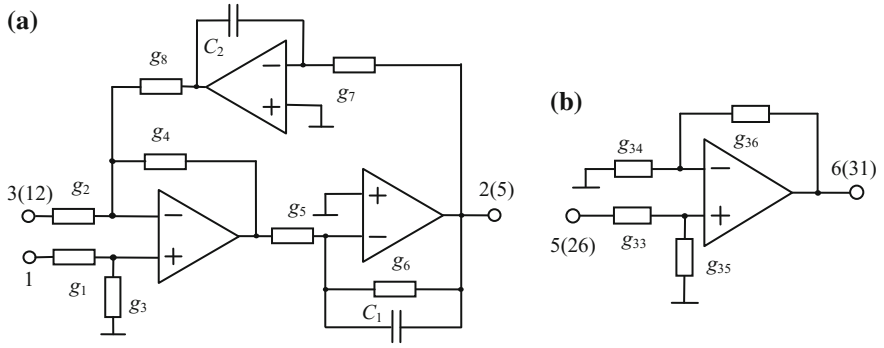


Fig. 16 The first **a** and fifth **b** subcircuits of band-pass filter

OpAmps modeled by nullors, and 36 resistors and 8 capacitors modeled by admittances.

The filter can be decomposed into the five subcircuits as shown in Fig. 15. Note that for the sake of clarity the common nodes of subcircuits are renumbered. The original nodes labels are shown in brackets in Fig. 15. The subcircuit 1 presented in Fig. 16 is topologically identical to the subcircuits 2–4. Therefore the subcircuits 2–4 can be easily derived from Fig. 16 by substitution of identification numbers of symbols of resistors and capacitors correspondingly by the following formulae:

$$N_R = i + 8(j-1), \tag{66}$$

$$N_C = i + 2(j-1), \tag{67}$$

where i is an identification number in subcircuit 1, $j = \{2,3,4\}$ is a number of one of the subcircuits 2–4.

There are four external nodes in subcircuits 1–4. In this case, 20 binary arrays can be derived. However the equivalent circuit of filter includes the 13 nullor, therefore, the number of binary arrays can be greatly reduced by usage of Rules I and II: $b_1 = 101011$, $b_2 = 101101$, $b_3 = 101110$. The tuples of binary arrays for the subcircuits 1–4 can be expressed as follows: 123123, 234234, 345345, 456456.

In the case of subcircuit 5 in Fig. 16b which includes three external nodes the number of binary arrays can be reduced to the two: $b_1 = 1001$, $b_2 = 1010$. The tuple of these binary arrays is following: 5656.

The expressions of circuit minors of subcircuits 1 and 5 calculated by GPEM are presented below:

$$\begin{gathered}
\Delta_1(b_1) = -g_1 g_5 s C_2 (g_2 + g_4 + g_8), \\
\Delta_1(b_2) = (g_1 + g_3)[(g_6 + sC_1) g_4 p C_2 + g_5 g_7 g_8], \\
\Delta_1(b_3) = g_2 g_5 s C_2 (g_1 + g_3), \\
\Delta_5(b_1) = g_{33}(g_{34} + g_{36}), \\
\Delta_5(b_2) = g_{36}(g_{33} + g_{35}).
\end{gathered} \tag{68}$$

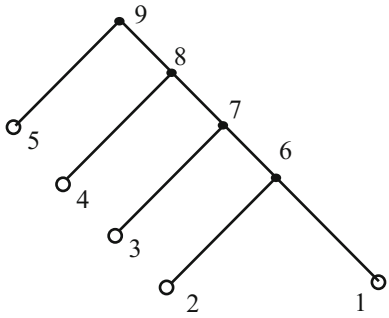


Fig. 17 The hierarchical tree for combination of circuit minors of band-pass filter

The expressions of circuit minors of subcircuits 2–4 can be derived from (68) by renumbering of symbols numbers in accordance with (66) and (67):

$$\begin{gathered}
\Delta_2(b_1) = -g_9 g_{13} sC_4 (g_{10} + g_{12} + g_{16}), \\
\Delta_2(b_2) = (g_9 + g_{11})[(g_{14} + sC_3) g_{12} sC_2 + g_{13} g_{15} g_{16}], \\
\Delta_2(b_3) = g_{10} g_{13} sC_4 (g_9 + g_{11}), \\
\Delta_3(b_1) = -g_{17} g_{21} sC_6 (g_{18} + g_{20} + g_{24}), \\
\Delta_3(b_2) = (g_{17} + g_{19})[(g_{22} + sC_5) g_{20} sC_6 + g_{21} g_{23} g_{24}], \\
\Delta_3(b_3) = g_{18} g_{21} sC_6 (g_{17} + g_{19}), \\
\Delta_4(b_1) = -g_{25} g_{29} sC_8 (g_{26} + g_{28} + g_{32}), \\
\Delta_4(b_2) = (g_{25} + g_{27})[(g_{30} + sC_7) g_{28} sC_8 + g_{29} g_{31} g_{32}], \\
\Delta_4(b_3) = g_{26} g_{29} sC_8 (g_{25} + g_{27}).
\end{gathered} \tag{69}$$

The transfer function of the filter can be expressed as result of the combination of circuit minors (68) and (69) by using the hierarchical tree presented in Fig. 17. The labels of vertices 1–5 are corresponding to the numbers of subcircuits 1–5 in Fig. 15. The labels of vertices 6–9 are corresponding to the numbers of new subcircuits which are obtained by the bottom-up combination of subcircuits. Obviously, the original filter circuit which corresponds to the vertex 9 is the final result of subcircuits combination.

Let's consider the combination of subcircuits 1 and 2 by nodes 0, 2 and 3. The entries 2323 must be taken into account to find the set of joint binary arrays pairs and their signs. Note that the values at the entries which correspond to the common non-external node 2 must be mutually complementary, while the value in the entries which correspond to the common external node 3 cannot be equal to zero. The pairs of joint binary arrays, binary arrays of combined subcircuit 6 are presented in Table 9.

The combination of other subcircuits can be performed in a similar way. Thereby the final quite compact SoE of filter transfer function is expressed as following:

Table 9 The joint binary arrays of subcircuits 1 and 2 and binary arrays of combined circuit

The binary arrays of combined subcircuit 6 (tuple 134134)		The joint binary arrays of subcircuits 1 and 2		δ
		The tuple 123123	The tuple 234234	
1	101011	2 $b_1 = 101011$	1 $b_1 = 101011$	1
2	101101	$b_2 = 101101$	$b_2 = 101101$	1
		$b_2 = 101101$	$b_3 = 101110$	–1
3	101110	$b_3 = 101110$	$b_1 = 101011$	1

$$\begin{gathered}\Delta_6(b_1)=\Delta_1(b_1)\Delta_2(b_1),\ \Delta_6(b_2)=\Delta_1(b_2)\Delta_2(b_2)-\Delta_1(b_3)\Delta_2(b_1),\\ \Delta_6(b_3)=\Delta_1(b_2)\Delta_2(b_3),\quad \Delta_7(b_1)=\Delta_6(b_1)\Delta_3(b_1),\\ \Delta_7(b_2)=\Delta_6(b_2)\Delta_3(b_2)-\Delta_6(b_3)\Delta_3(b_1),\ \Delta_7(b_3)=\Delta_6(b_2)\Delta_3(b_3),\\ \Delta_8(b_1)=\Delta_7(b_1)\Delta_4(b_1),\ \Delta_8(b_2)=\Delta_7(b_2)\Delta_4(b_2)-\Delta_7(b_3)\Delta_4(b_1),\\ \Delta_8(b_3)=\Delta_7(b_2)\Delta_4(b_3),\ \Delta_9(b_1)=\Delta_8(b_1)\Delta_5(b_1),\\ \Delta_9(b_2)=\Delta_8(b_2)\Delta_5(b_2)-\Delta_8(b_3)\Delta_5(b_1),\quad H=\Delta_9(b_1)/\Delta_9(b_2).\end{gathered} \tag{70}$$

The obtained result (70) can be verified by numerical simulation or exact comparison with the symbolic solution presented in [44].

6 Conclusion

In this chapter, we briefly review the basics of GPEM and its applications for symbolic analysis of large circuits with pathological element-based active device models. The method can be used for analysis of circuits containing all linear circuit elements, including nullors, four types of controlled sources, and pathological mirrors. We start with the parameter extraction formulae and circuit degeneracy conditions. Then we introduce an algorithm to improve the efficiency of determinants calculation of residual circuits containing pathological elements only. Such circuits can be derived from active networks in which all of the impedances, admittances, and CS were extracted. The algorithm proposed is based on the concept of HOSC and provides the determinant calculation by usage of simple matrix algebra operations instead of topological simplifications. Further, the hierarchical decomposition procedures for symbolic analysis of large circuits by GPEM have been introduced. The techniques proposed of upward analysis and downward analysis provide the calculation of a circuit function in the form of a single nested expression or in the form of sequence of expressions correspondingly. All described algorithms were implemented in the computer program for circuit analysis CirSym.

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