Symbolic Analysis and Synthesis of Analog Circuits Using Nullors and Pathological Mirror Elements

Miguel A. Duarte-Villaseñor, Esteban Tlelo-Cuautle, Luis Gerardo de la Fraga and Carlos Sánchez-López

Abstract It has been demonstrated that symbolic circuit analysis of analog circuits modeled by nullors and pathological mirror elements leads us to deal with the nodal admittance (NA) matrix that is more compact than by using traditional modified nodal analysis (MNA). This chapter reviews such a theory and details the inclusion of pathological voltage mirrors and current mirrors into the NA formulation. In this manner, from a circuit topology consisting of nullors and mirrors we show how to perform symbolic circuit analysis and then how to synthesize those circuit elements using MOS transistors. It is also highlighted that from such kind of circuit modeling, one can transform a voltage-mode circuit into a current-mode one and vice versa. We show the design of both modes of operation at the transistor level of design, for which we also provide details on the synthesis approach where each nullator, norator, voltage mirror and current mirror can have multiple options to be implemented with MOS transistors. Several examples are provided to appreciate the advantages of the NA formulation from analog circuits modeled by nullors and mirrors, the symbolic circuit analysis, the transformation from voltage-mode to current-mode and vice versa, and the synthesis of pathological circuits by using MOS transistors. The synthesized circuits are unity-gain-cells, a current conveyor, a current-feedback operational amplifier, and an operational transconductance amplifier, which are designed with standard CMOS integrated circuit technology, and they are applied to implement active filters and oscillators.

M. A. Duarte-Villaseñor
CONACyT-Instituto Tecnológico de Tijuana, Tijuana, Baja California, Mexico

E. Tlelo-Cuautle (✉)
Instituto Nacional de Astrofísica, Óptica y Electrónica, Puebla, Mexico
e-mail: etlelo@inaoep.mx

E. Tlelo-Cuautle · L. G. de la Fraga
Centro de Investigación y de Estudios Avanzados del IPN, Ciudad de México, Mexico

C. Sánchez-López
Universidad Autónoma de Tlaxcala, Apizaco, Tlaxcala, Mexico

M. Fakhfakh and M. Pierzchala (eds.), *Pathological Elements in Analog Circuit Design*, Lecture Notes in Electrical Engineering 479,
https://doi.org/10.1007/978-3-319-75157-3_1

1 Introduction

By April 23 in 1954, during the Seminario Matematico e Fisico di Milano, B. D. H. Tellegen stated that [1]: The nullator (the linear time-invariant one-port with $v = i = 0$) and the norator (the linear time-invariant one-port with v and i arbitrary), which are shown in Fig. 1a, both are singular elements. Ten years later, Carlin published the article entitled "singular network elements" [2], where he discussed the physical realizability of the singular linear network elements: the nullator (simultaneously an open and a short circuit), and the norator (the unique nonreciprocal one-port with arbitrary port voltage and current). Carlin modeled the nullor as a two-port network consisting of one nullator and one norator as shown in Fig. 1a. The nullor can also be modeled by two nullators and two norators as shown in Fig. 1b, because from the properties of the nullator, the current at the output port remains through the norators while the voltage across the nullators remains equal to zero. Carlin also predicted that the nullor would be amenable for use in practical electronic systems, as highlighted in the rest of this chapter.

Using the nullor, the ideal model of the bipolar junction transistor (BJT) was introduced in [3], where the base (B), collector (C) and emitter (E) terminals are denoted as shown in Fig. 2a. As one sees, the voltage between BE is the sum of the voltage across the nullator and the resistor, however, since the voltage across the nullator beings zero, then the input voltage drops across terminals AB where a resistor is connected. Also, since the current through the nullator beings zero, then the current through the resistor goes to the output through the collector. In a similar way, nowadays the model in Fig. 2a can be used to describe the MOSFET whose terminals are gate (G), drain (D) and source (S). In both models for the BJT and MOSFET, the output current is proportional to the inverse of the resistance value, which for amplifier design it is known as the transconductance denoted by g_m. In an extended version like the topology shown in Fig. 2b, the output is also a current that is proportional to the transconductance g_m in which the input voltage drops because the voltage across the nullators being zero, so that $i_o = g_m v_{in}$ and the direction is imposed by the polarities of the nullators, i.e. the negative input goes to terminal A and the positive input goes to B, so that the polarity of the transconductance g_m goes

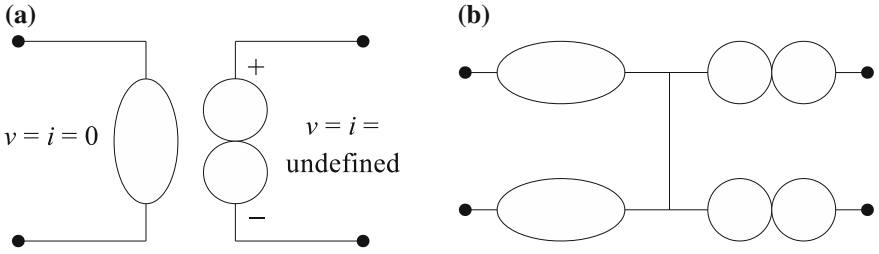

Fig. 1 Nullor representation using: **a** One nullator and one norator, and **b** two nullors and two norators

from B(+) to A(−), as denoted by the arrows in the norators at the output port, and as shown in Fig. 2b. It is also possible to joint a nullator-norator pair to model a negative-type second-generation current conveyor, as shown in Fig. 2c, where the equations $v_x = v_y$, $i_y = 0$ and $i_z = -i_x$ are accomplished. These models will be used in the next sections to show how to perform symbolic analysis and synthesis of nullor and pathological mirror networks.

The authors in [4] also introduced a nullor model of the transistor, but they pointed out that the use of T parameters permit certain advantages over the nullor-based model in the design of transistor networks. Later, in [5] the nodal admittance matrix formulation was introduced for the ideal amplifier or circuits consisting of nullors and passive circuit elements. This contribution was quite useful to perform computer analysis of nullor networks, as highlighted in [6], where a nullor version of a generalized immittance convertor (GIC) was analyzed, and where the nullator was labeled as Z and the norator as A. The program was implemented in Fortran IV, the maximum number of nodes was 20 and maximum numbers of branches 40, but those limits were only restricted by the size of the computer's core store.

The term pathological was introduced in 1976 [7], it was referred to nullor circuits for circuit analysis. The usefulness of the nullor for circuit analysis established a challenge for circuit design, so that the first monolithic implementation of the nullor, which was also referred as a universal active device, was introduced in 1977. That way, the authors in [8] claimed that if the floating nullor (having both the input and output port independently floating) is used, then all kinds of transfer functions could be fixed by using the minimum number of external passive and precision components. Up to now, still the design of the monolithic integrated nullor is a challenge because of the need to provide large internal gain. The integrated design presented in 1977 was developed by using bipolar technology and the floating nullor consisted of a differential input stage, a symmetrical level shift stage, and a differential output stage.

It was until 2010 that the authors in [9] introduced the concepts of the pathological voltage mirror (VM) and current mirror (CM) elements. Both pathological mirrors could also be used as a pair to model a universal active element, as it was

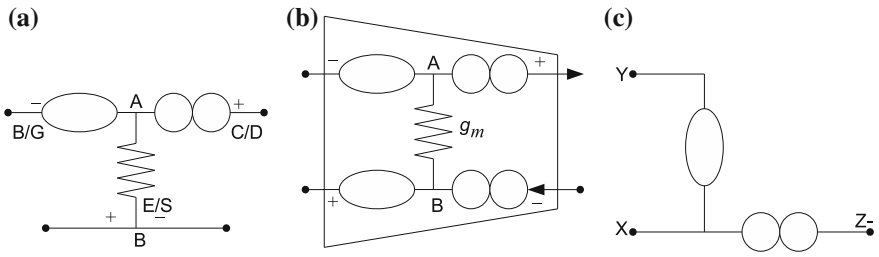

Fig. 2 Ideal model of: **a** The bipolar junction transistor (BJT) (or metal-oxide-semiconductor field-effect-transistor (MOSFET)), **b** the operational transconductance amplifier (OTA), and **c** negative-type second-generation current conveyor (CCII-)

done for the nullor. The work in [9] showed that the pathological VM-CM pair provides two alternative realizations for the nullor, and it is also capable of realizing the traditional operational amplifier and the four types of the second-generation current conveyors (CCII), namely: the negative-type CCII-, the positive-type CCII +, the inverting CCII- (ICCII-), and the inverting CCII+ (ICCII+), as shown in Figs. 3 and 4, respectively. The VM and CM are connected in a special way to accomplish the equations modeling each kind of current conveyor, for example: $v_x = v_y$, $i_y = 0$ and $i_z = -i_x$ for the CCII-; $v_x = v_y$, $i_y = 0$ and $i_z = +i_x$ for the CCII +; $v_x = -v_y$, $i_y = 0$ and $i_z = -i_x$ for the ICCII-; and $v_x = -v_y$, $i_y = 0$ and $i_z = +i_x$ for the ICCII+.

In a high level of abstraction, the nullor can also be implemented by joining two CCIIs as already shown in [10], however the CCII has a parasitic resistance at its X-port terminal and then the equivalent circuit looks like an OTA, as shown in Fig. 2b. The authors in [10] compared their CMOS design of a fully balanced four-terminal floating nullor (FBFTFN) with other integrated realizations. Those authors highlighted that their FBFTFN was superior providing suitability for ultra-low-voltage and low-power applications. The FBFTFN was designed with TSMC 0.18 μm n-well CMOS technology with supply voltage of 0.5 V and dissipation power of 9.4 μW, and it employed the bulk-driven quasi-floating-gate (BD-QFG) metal–oxide–semiconductor transistor technique to provide the capability of ultra-low-voltage, low-power operations as well as extended input voltage range. To demonstrate the usefulness of the CMOS FBFTFN, it was tested by implementing fully balanced filters, such as: band-pass Sallen–Key filter, voltage-mode universal biquadratic filter and current-mode sixth-order low-pass filter. However, this novel integrated design has also parasitic impedances that for direct current it also can be modeled as parasitic resistance as shown in Fig. 2b.

As one can infer, by using nullators, norators, VMs and CMs one can model all kinds of active devices, as already shown in [11–24], where in some cases they are called pathological circuit elements. Their usefulness in computing symbolic

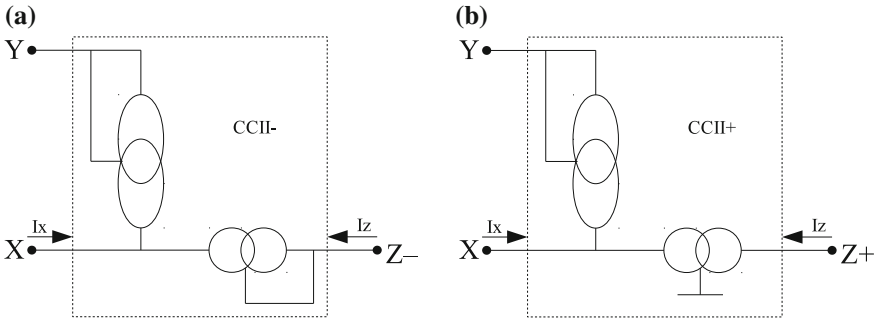

Fig. 3 Pathological VM-CM pair used to model the **a** negative-type second-generation current conveyor (CCII-) and the **b** positive-type second-generation current conveyor (CCII+), taken from [9]

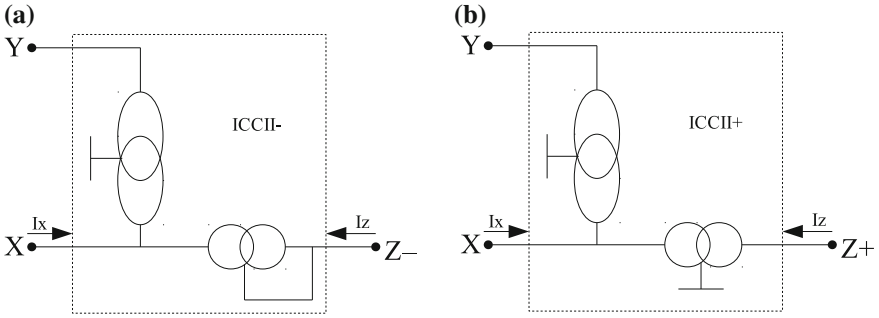

Fig. 4 Pathological VM-CM pair used to model the **a** inverting CCII- and the **b** inverting CCII+, taken from [9]

expressions have also been demonstrated in various recent works, where the main goal is to get insights into the effect of each circuit element in the biasing and sizing of analog integrated circuits to enhance performances in alternate and direct current, and time domains. As already mentioned in [11], very efficient symbolic analysis methods, such as nodal analysis, Coates flow graphs, and two-graphs are widely used. The works in [11, 12] used ICCII-based circuits to show the usefulness of performing graph operations to compute symbolic expressions. A more general modeling approach for current conveyors is given in [13], where one can find models of single and multiple outputs (MO) for the first, second and third generation current conveyors, their inverting topologies and their positive and negative types denoted as (MO)(I)CCI(II)(III)±. In [13], the authors showed how to include parasitic elements to the current conveyors, as done in [14]. Other active devices are modeled by using pathological elements trying to capture the dominant behavior, as shown in [15], and including differencing voltage and current characteristics, as highlighted in [16]. As one sees, the pathological VM-CM pair is quite useful to increase the modeling capabilities of active devices because they can provide multi-outputs (MO) [17], as it is quite common in integrated circuit design using current mirror topologies at the transistor level of abstraction.

A very complete list of pathological equivalents of fully differential active devices is given in [18], where some examples are provided to show how to perform symbolic nodal analysis. Other nullor equivalents and pathological realizations for application to symbolic circuit analysis are given in [19–24]. If one performs symbolic analysis of only nullor networks, the VM-CM pair can be modeled using nullor equivalents as shown in [25], which allows including parasitic elements to the MO versions. The next section shows some examples of performing symbolic nodal analysis of analog integrated circuits modeled by nullators, norators, VMs and CMs. Afterwards, we show how to transform a circuit working in voltage-mode to a circuit working in current-mode and vice versa. In such a case the adjoint and duality properties are applied, as already shown in [26], where some examples show their

usefulness to solve the problems such as the inflexible positions of the port variables, and inability for the conditions that both circuit and voltage of a port are independent (or dependent) variables.

The symbolic analysis tools are quite useful to analyze all kinds of analog integrated circuits modeled by nullators, norators, VMs and CMs, and working in either voltage or current modes. In fact, in the synthesis of analog circuits, a symbolic analysis tool can be used in the loop for verifying the desired transfer function and then to test the frequency response. Among the synthesis approaches based on nodal analysis, some key references are [27–29]. In such cases, every nullator, norator, VM and CM can be implemented with transistors, as demonstrated in [30], where the nullator is synthesized by a voltage follower (VF), the norator is synthesized by a current follower (CF), and the VM and CM by their corresponding CMOS topologies. All of them can be extended to provide multiple outputs, as shown in the rest of this chapter. Section 2 summarizes the recent advances in symbolic analysis techniques for design automation of nanometer VLSI systems [31]. Section 3 shows the transformation of voltage-mode circuits to current-mode ones and vice versa. Section 4 shows the synthesis of the pathological nullator, norator, VM and CM elements by using CMOS integrated circuit technology. Section 5 shows some integrated circuit designs of unity-gain cells, current conveyors, current-feedback operational amplifier and OTA, which are optimized by metaheuristics like in [32], and they are applied to implement active filters and oscillators. Finally, the conclusions are listed in Sect. 6.

2 Symbolic Nodal Analysis of Circuits Modeled by Nullors and Mirrors

Symbolic circuit analysis is a complement to numerical simulation, and it is a systematic approach to obtaining the knowledge of analog building blocks in analytic form. The history of symbolic circuit analysis is given in [31], in which is mentioned that this field gained real momentum in the 1950s when electric computers were introduced and used for circuit analysis, while the first general-purpose circuit analysis programs emerged in the early 1960s, when a basic goal behind computer-aided design and analysis of analog circuits was to formulate network equations by matrix algebraic or topological techniques. In the frequency domain, the circuit equations of a lumped linear or linearized time-invariant analog circuit can be formulated by applying nodal analysis in the general matrix form given by (1), where $\boldsymbol{A}$ is an $n \times n$ sparse admittance matrix (n as the rank of the matrix), $\boldsymbol{b}$ is a vector of external sources, and $\boldsymbol{x}$ the vector of unknowns.

$$Ax = b \tag{1}$$

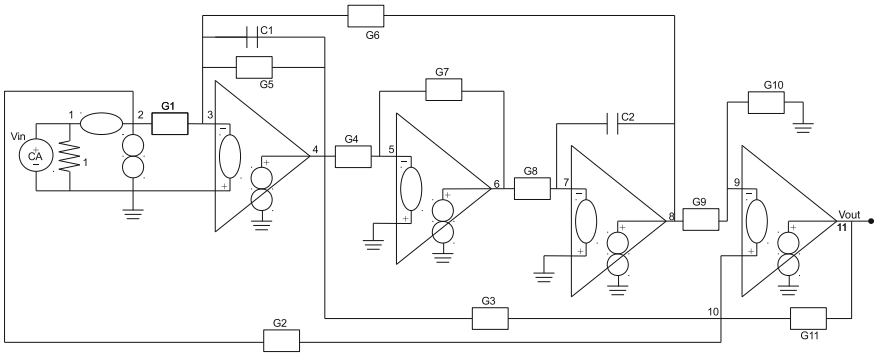

Fig. 5 RC filter consisting of operational amplifiers modeled by nullors

Symbolic analysis of analog integrated circuits solves (1) in which the matrix elements a_{ij} can be real numbers, rationals in the frequency domain s, semi-symbolic or fully symbolic expressions. Reference [31] provides graph and matrix-based methods to solve (1). For example, the RC filter shown in Fig. 5 consists of operational amplifiers (opamps) that are modeled using the nullor and the independent voltage source is transformed to an independent current source among nodes 1 and 2. As already shown in [13–19, 23–25], the order of the nodal admittance matrix must be equal to the number of nodes minus the number of nullors, so that the resulting system of equations has the form like in (1), and it is given by (2). The reduced matrix was obtained by applying the nullator and norator properties, which are summarized as follows:

1. If a nullator is connected between node i and ground, from its voltage property node i has the same potential as ground, and therefore the voltage variable associated to node i is eliminated, thus reducing one column in the admittance matrix.
2. If a nullator is floating, e.g. connected between nodes i and j, from its voltage property both nodes i and j are virtually connected, so that a single voltage-node variable $v_{i,\,j}$ is associated to both nodes i and j, thus reducing one column in the admittance matrix.
3. If a norator is connected between node k and ground, from its current property node k should be grounded and therefore eliminated as current variable, thus reducing one row in the admittance matrix.
4. If a norator is floating, e.g. connected between nodes k and l, from its current property both nodes k and l are virtually connected, so that a single current-branch variable $i_{k,\,l}$ is associated to both nodes k and l, thus reducing one row in the admittance matrix.

$$\begin{bmatrix} v_{in} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ -G_1 & -G_5 - sC_1 & 0 & -G_6 & 0 & 0 \\ 0 & -G_4 & -G_7 & 0 & 0 & 0 \\ 0 & 0 & -G_8 & -sC_2 & 0 & 0 \\ 0 & 0 & 0 & -G_9 & G_9 + G_{10} & 0 \\ -G_2 & -G_3 & 0 & 0 & G_2 + G_3 + G_{11} & -G_{11} \end{bmatrix} \begin{bmatrix} v_{1,2} \\ v_4 \\ v_6 \\ v_8 \\ v_{9,10} \\ v_{11} \end{bmatrix} \tag{2}$$

In the previous RC filter, the opamps are modeled by nullors and avoid non-idealities but the models can also include parasitic elements, as shown in [13]. The solution to (2) can be obtained by applying the methods given in [31].

As one can infer, to take advantage on performing computer-aided analysis all active devices should be modeled with the appropriate pathological elements. Figure 2a shows the ideal model of the BJT or MOS transistor, and Fig. 2b shows an extended version to model the OTA and which can also be associated to modeling the voltage-controlled current source (VCCS). Figure 6 shows the nullor equivalents of the four controlled sources, voltage-controlled voltage source (VCVS), VCCS, current-controlled voltage source (CCVS), and current-controlled current source (CCCS), which can be used to model any kind of active devices. For example: Fig. 7 shows the four terminals MOSFET including parasitic resistances at the drain, gate, source and bulk terminals, the output conductance g_o, and parasitic capacitors among two terminals. The conventional model consists of two VCCSs that have been implemented by one nullor and one resistor because one nullator-norator pair is in parallel and it is equivalent to a short circuit.

The current mirror is quite useful in designing active devices like the OTA Miller shown in Fig. 8a, in which two current mirrors are embedded, one by M3–M4 and the other by M5–M6–M7. Those current mirrors can be modeled using nullors to obtain the nullor equivalent shown in Fig. 8b, where one can count 15 nodes (node 5 is already grounded but labeled to appreciate de joint connection of a nullator-norator pair associated to MOSFET M5 in Fig. 8a) and Fig. 9 nullors or nullator-norator pairs. In this manner, the system of equations formulates an admittance matrix having an order equal to the number of nodes (15), minus the number of nullors (9): 15 – 9 = 6. One can also perform sensitivity analysis after solving the system of equations and noise analysis, as already detailed in Chap. 9 in [31].

The pathological VM and CM elements can also be used to model active devices with multiple-outputs. For instance, Fig. 9 shows the nullor-CM equivalent of a current mirror with one negative current-output i_{z-} and one positive current-output i_{z+}. Such an equivalent can be used to analyze the current-mode filter that consists of one current follower (CF) labeled as 2 in Fig. 10a, one 2-outputs current mirror labeled as 1, one 3-outputs current mirror labeled as 3, 2 resistors R_1 and R_2, and 2 capacitors C_1 and C_2. Those current mirrors can be modeled by using the equivalent from Fig. 9 leading to the pathological equivalent shown in Fig. 10b, where it can be appreciated that 3 resistors are added to the outputs to measure the currents for the

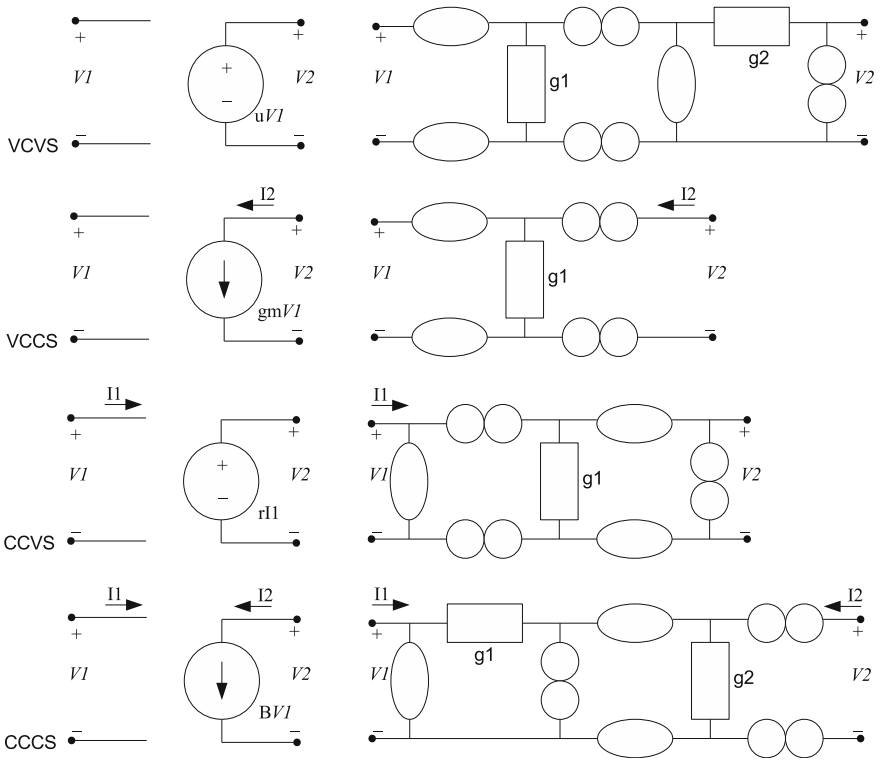

Fig. 6 Nullor equivalents of the four controlled sources

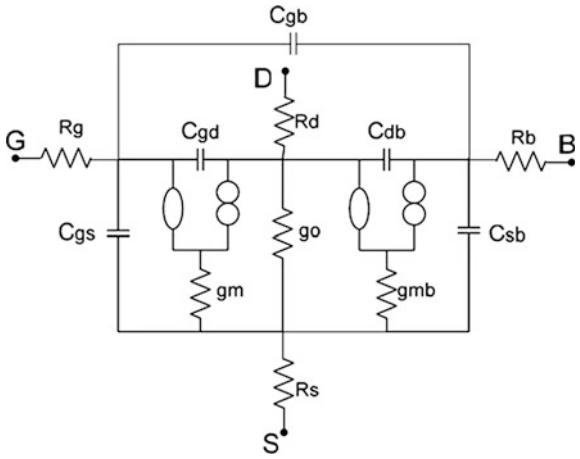

Fig. 7 Small-signal model of the four terminals MOSFET including parasitic elements

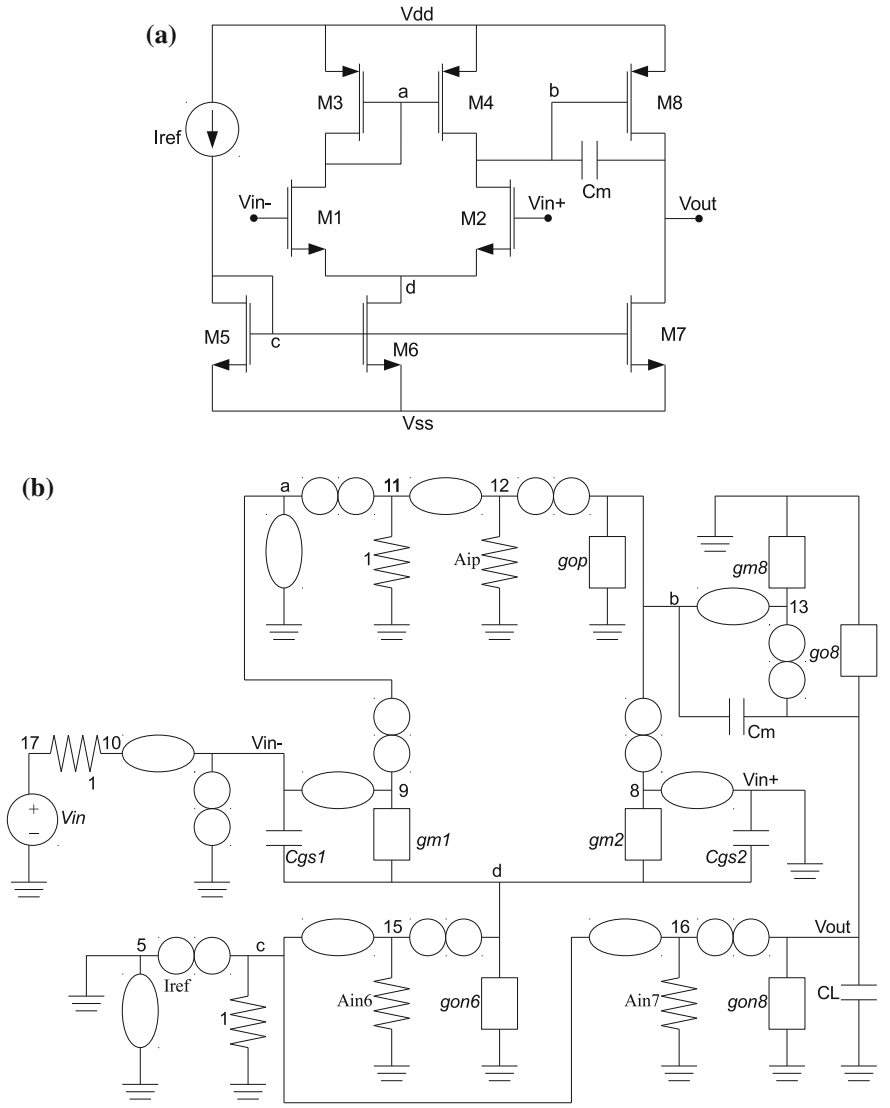

Fig. 8 Miller amplifier: **a** MOSFET circuit and its **b** nullor equivalent taken from [31]

band-pass (BP), high-pass (HP) and low-pass (LP) filter responses. After performing nodal analysis of this pathological equivalent, the symbolic expressions are given by,

$$\frac{I_{BP}}{I_{in}} = \frac{s\frac{g_1}{C_1}}{s^2 + s\frac{g_1}{C_1} + \frac{g_1 g_2}{C_1 C_2}}, \frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + s\frac{g_1}{C_1} + \frac{g_1 g_2}{C_1 C_2}}, \frac{I_{LP}}{I_{in}} = \frac{\frac{g_1 g_2}{C_1 C_2}}{s^2 + s\frac{g_1}{C_1} + \frac{g_1 g_2}{C_1 C_2}} \quad (3)$$

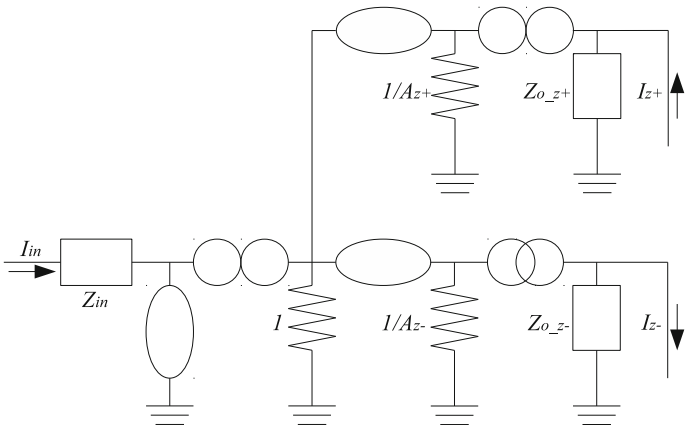

Fig. 9 Two-outputs current mirror modeled by three nullators, two norators and one CM

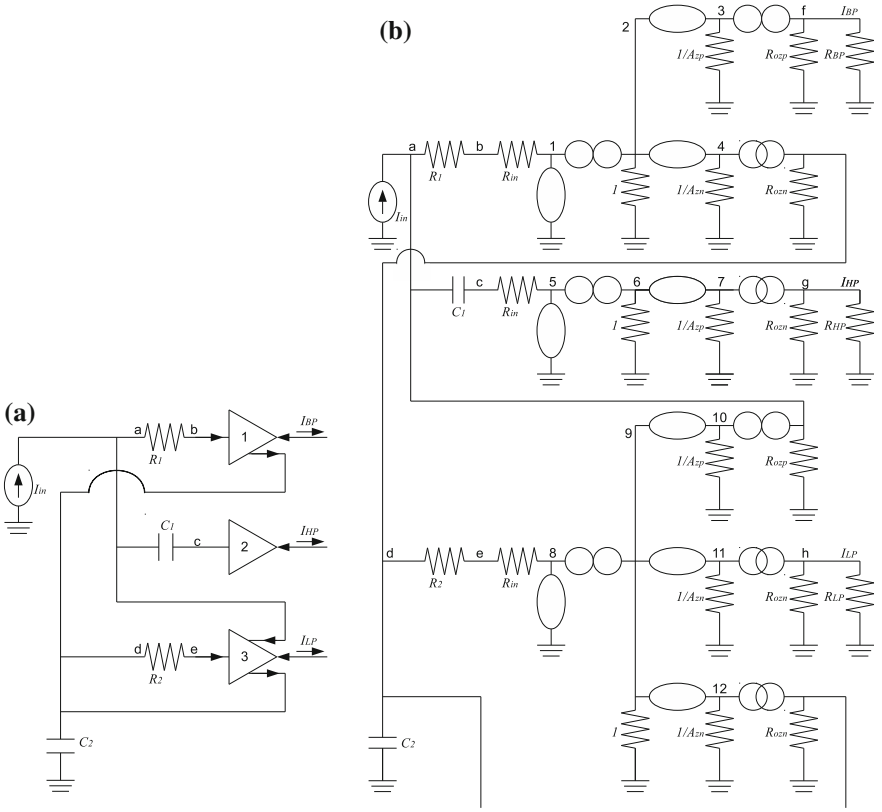

Fig. 10 **a** Current-mode universal filter taken from [33], and **b** its pathological equivalent using the current mirror equivalent shown in Fig. 9

This example highlights the usefulness of using the pathological current mirror element to model active devices with the goal of computing analytical expressions. That way, the main advantage of the derived pathological models relies on the application of symbolic nodal analysis (NA) to formulate smaller matrices compared to traditional modified nodal analysis (MNA) formulation. As pointed out, the pathological equivalents also allow including parasitic elements, so that the derived behavioral models capture the real behavior of the active devices.

3 Adjoint Transformations of Circuits Containing Nullors and Mirrors

Current-mode circuits like the examples given above are quite useful in some analog signal processing applications. However, since the majority of analog integrated circuit designers are quite familiar with voltage-mode circuits, it is quite convenient to know how to convert the voltage-mode designs into their current-mode versions. As highlighted in [26], the main idea is replacing the elements in the voltage-mode circuits by their adjoints, and this task is pretty simple when nullators, norators, CM and VMs, model the voltage-mode circuits. In this manner, this section shows some examples of converting voltage-mode circuits that are modeled by pathological elements, to current-mode ones. The main steps are associated to interchange nullators and voltage mirrors with norators and current mirrors, respectively.

Lets us consider the voltage follower shown on the left of Fig. 11. It consists of a nullator connected between nodes AB and a norator connected between node B and ground. As one sees, the input port drives a voltage input v_{in} connected between node A and ground, while the output is measured at node B with respect to ground. Interchanging the nullator/norator by the norator/nullator but keeping the nodes intact are the main operations to obtain the adjoint equivalent. In this manner, now the norator is connected between nodes AB as shown on the right of Fig. 11, and the nullator is connected between node B and ground. The input/output port from the voltage follower now becomes the output/input port of the current follower, as

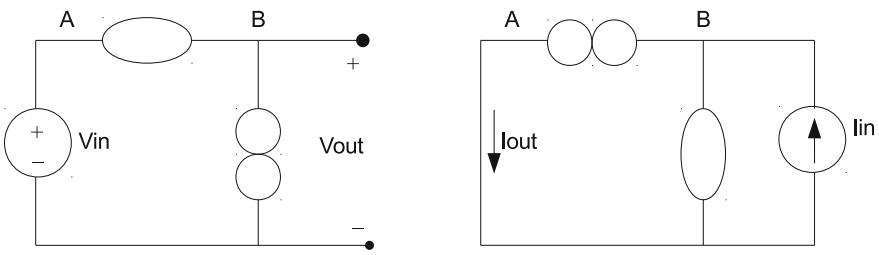

Fig. 11 Transforming a voltage follower into a current follower

highlighted in Fig. 11. It is trivial to obtain the voltage follower from the current follower by performing the same operations on interchanging the nullor/norator by the norator/nullator and converting the input/output port from the current follower to become the output/input port of the voltage follower. In both cases the transfer function equals to 1, i.e. $V_{out}/V_{in} = 1$ and $I_{out}/I_{in} = 1$.

A more elaborated example consists on transforming the OTA-based filter shown in Fig. 12a, which is working in voltage-mode, into its current-mode version. In this case one must set references to the four nullator-norator pairs, and to the input and output ports. Each nullator-norator pair is joined by one of their terminals that are connected to the transconductance g_m. The capacitor practically remains intact and the nullators are interchanged by the norators, the input/output port in Fig. 12a will become the output/input port of the current-mode OTA-based filter in Fig. 12b. By computing the symbolic transfer functions applying the nodal analysis method described in the previous section, both analytical expressions in voltage-mode and current-mode are the same,

$$\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = \frac{g_m}{sC + g_m} \tag{4}$$

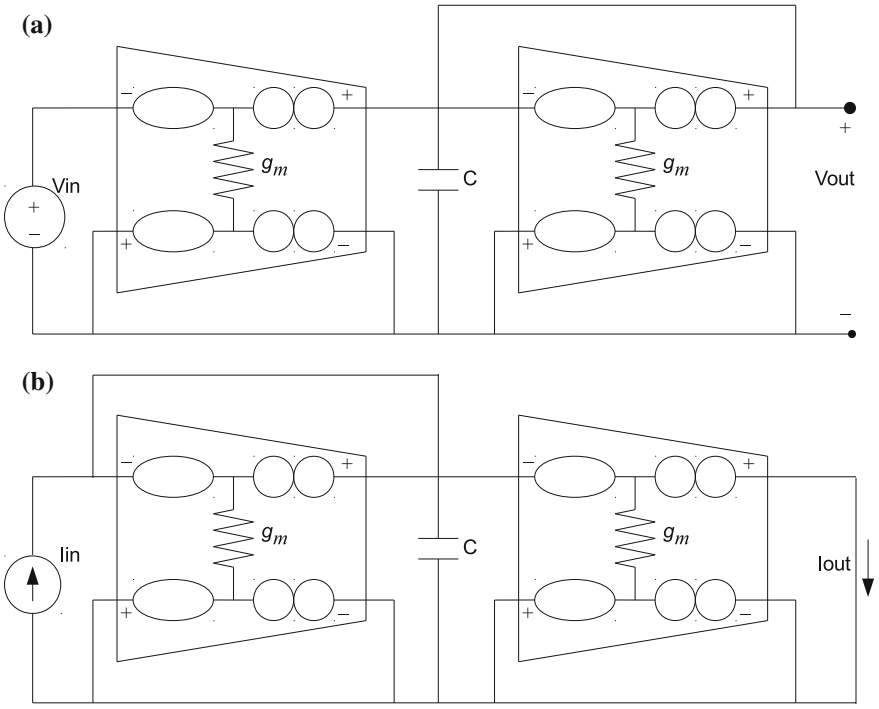

Fig. 12 Transforming the **a** voltage-mode OTA-based filter, into **b** the current-mode one

The same operations apply for VM-CM pairs; they must be interchanged when transforming a voltage-mode circuit into a current-mode one and vice versa. The difficulty arises when either the nullator or norator is associated to a VM or CM, in such a case; one must find the adjoint of each element independently of its associated pair.

4 Synthesis of Nullators, Norators, Voltage Mirrors and Current Mirrors

The singular or pathological elements can be synthesized by transistors if each nullator has its corresponding norator pair as already modeled in Fig. 2a and in Fig. 11, where the voltage follower is modeled by the nullator but a norator is required to fix the output, and where the current follower is modeled by the norator but it needs a nullator to fix the input. For instance, in [34] the nullator is synthesized by MOS transistors when it is modeled as a voltage follower, for which several cases arises because the voltage follower can be modeled by a single, two or four nullators, as shown in Fig. 13, and then each nullator must be accompanied by a norator that can be connected in different ways.

Taking the voltage follower from Fig. 13a, there are several possibilities to add a norator (labeled as P in Fig. 14) to the nullator (labeled as O in Fig. 14), as shown in Fig. 14, the norator can be added to node 1, node 2 or in parallel to the nullator between nodes 1–2. All these nullator-norator (O-P) pairs can be synthesized by the MOS transistor, from Fig. 2a with the resistance equal to zero. Another problem arises when the O-P pairs are in parallel because the source terminal is associated to the node that joints both singular elements, and from Fig. 14c, the source can be associated to node 1 or node 2. All these combinations lead to different topologies, which will require voltage and current biases, as shown in Fig. 15, where one can see some possibilities of adding biases to one O-P pair. Finally, the implementation by using MOS transistors for synthesizing O-P pairs and by using MOS current mirrors to implement the current sources (I_{bias1} and I_{bias2} shown in Fig. 15) is given in Fig. 16, where only three CMOS topologies are shown, and they were synthesized by beginning from Fig. 13a. As one can infer, by beginning the synthesis

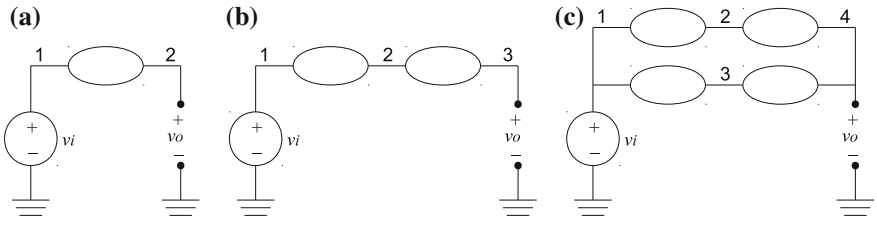

Fig. 13 Nullator equivalents for modeling the voltage follower

process from Fig. 13c, more O-P combinations arises than those shown in Fig. 14, more possibilities of adding voltage and current biases, and more possibilities of synthesizing each O-P pair and current biases by MOS transistors. The authors in [35] improved the work in [34] by applying genetic algorithms to synthesize the voltage follower. Therefore, a chromosome consisting of four genes was proposed, as shown in (5), where the small signal gene (genSS) includes O-P pairs which connections from Fig. 14 can be encoded by two bits (in (5) there are 8 bits associated to the voltage follower modeled by four nullators as in Fig. 13c), the synthesis of each O-P pair can be done by using the P-channel or N-channel MOS transistor, so that one bit is required to encode each O-P pair leading to genSMos. The possibilities of adding current biases can be encoded by two bits for each O-P pair leading to genBias, and finally, the current biases (like I_{bias1} and I_{bias2} shown in Fig. 15) can be synthesized by MOS current mirrors for which many topologies already exist in the literature (for example: simple current mirror, Widlar current mirror, cascode current mirror and so on), in (5) genCM consists of two bits meaning that each current bias can be replaced by any of the four MOS current mirrors. As one can infer, the chromosome in (5) leads us to deal with $8 + 4 + 8 + 2 = 22$ bits that in decimal notation equals to 4,194,304 combinations!, thus this problem is quite suitable for applying metaheuristics.

$$\text{Chromosome}_{VF} = \underbrace{00100010}_{\text{genSS}}\ \underbrace{0011}_{\text{genSMos}}\ \underbrace{10101111}_{\text{genBias}}\ \underbrace{00}_{\text{genCM}} \tag{5}$$

The synthesis of the norator can be associated to the current follower, as the one shown on the right side of Fig. 11. The synthesis process can be performed quite similar as for the synthesis of the nullor but the biases are now majorly voltage sources than current ones, it is an open problem that has been partially solved in [30], where several new topologies synthesized by MOS transistors are provided.

The synthesis of the voltage mirror (VM) can be seen as an extended case of the voltage follower (VF). Lets us consider Fig. 17 that embeds a VF that can be connected in two combinations. Basically, the chromosome in (5) can be

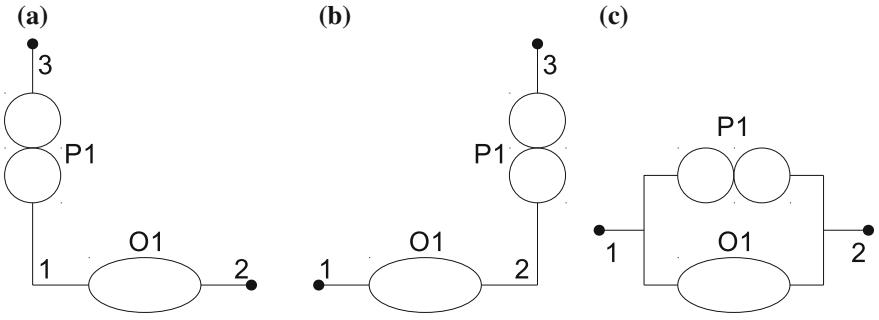

Fig. 14 Adding a norator to the nullator from Fig. 13a

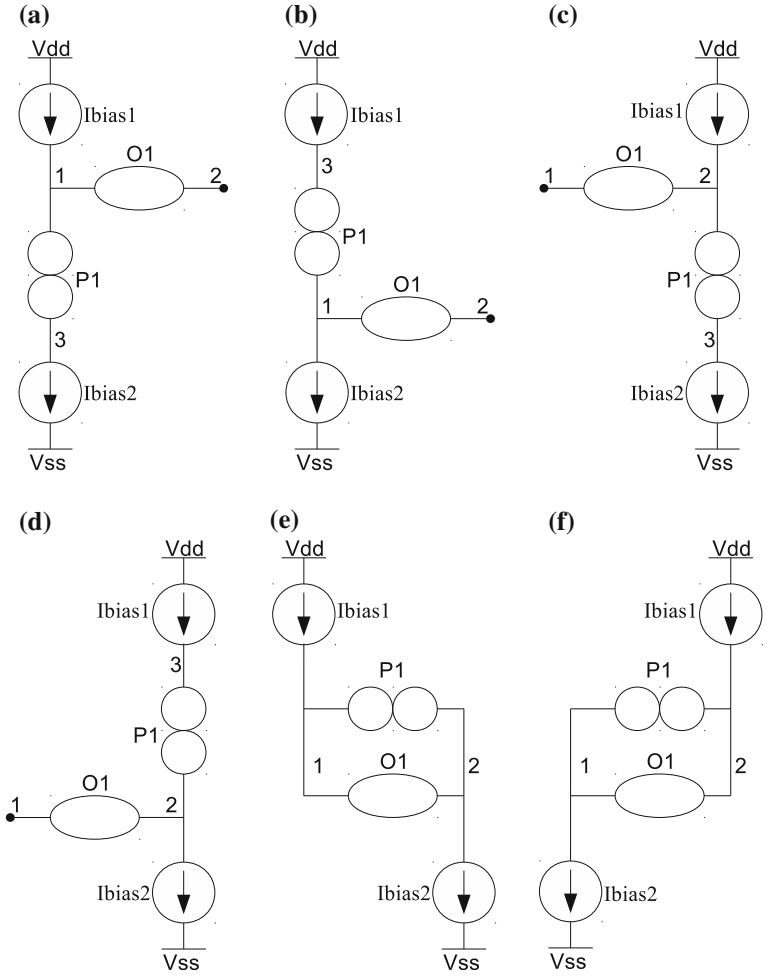

Fig. 15 Adding voltage and current biases to the nullator-norator (O-P) pairs from Fig. 14

augmented by one bit associated to the kind of connection of the output of the VF, e.g. to the P-channel or N-channel MOS transistor. From this reasoning, the synthesis of the VM by MOS transistors can be performed by beginning with the synthesis of the voltage follower (VF) and adding two complementary MOS transistors, as shown in Fig. 17, therefore the chromosome is like in (5) but adding one bit to encode the P-channel (MINV2) or N-channel (MINV1) MOS transistors. The authors in [35] provide details of this synthesis approach.

The synthesis of current mirrors with single or multiple outputs can be associated to the model given in Fig. 9, where it can be appreciated the association of O-P pairs but the pathological CM can be implemented with MOS transistors as already shown in [30], and where one can find new MOS topologies.

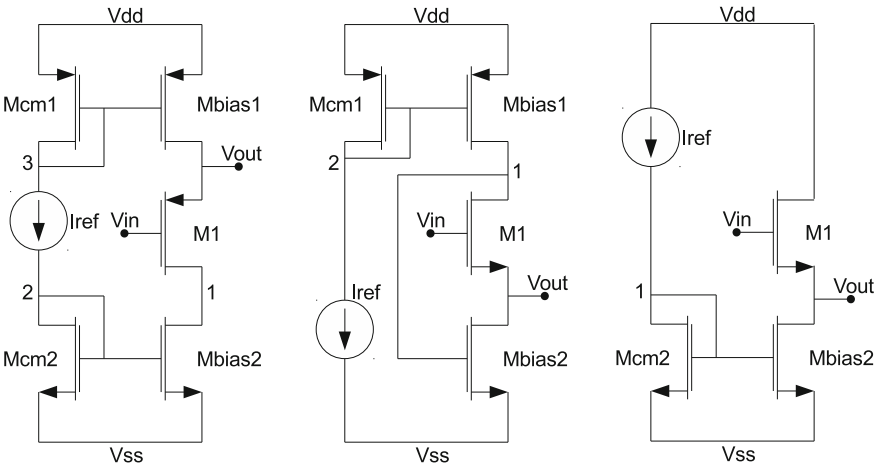

Fig. 16 Three CMOS topologies of the voltage follower synthesized by beginning from Fig. 13a

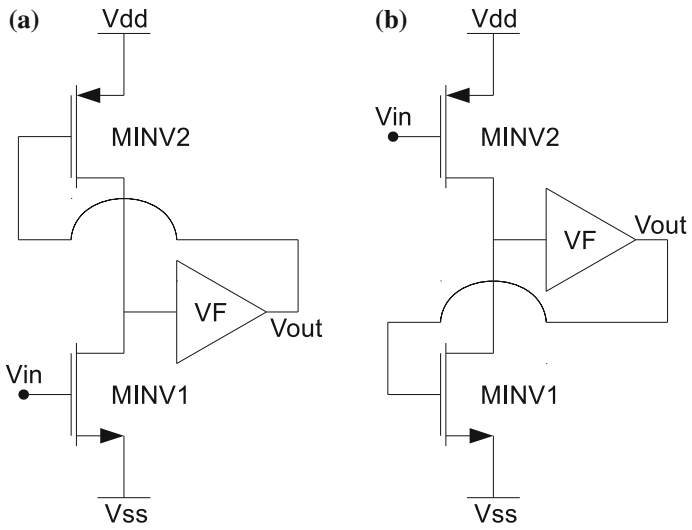

Fig. 17 Synthesis of the voltage mirror (VM) by beginning with the synthesis of the voltage follower (VF) and adding two complementary MOS transistors

5 CMOS Implementation of Unity-Gain-Cells and Mixed-Mode Analog Circuits

This section shows the implementation of synthesized circuits like unity-gain-cells, a current conveyor, a current-feedback operational amplifier, and an operational transconductance amplifier, which are designed with standard CMOS integrated circuit technology, and they are applied to implement active filters and oscillators.

The four unity-gain cells are the voltage follower (VF), current follower (CF), voltage mirror (VM) and current mirror (CM). A well-known VF is shown in Fig. 18, it is synthesized from Fig. 13c: Fig. 18a shows ideal current biases that are synthesized by simple current mirrors in Fig. 18b. Those ideal current biases can also be synthesized by other kinds of current mirrors. The voltage mirror can be synthesized by embedding a VF as shown in Fig. 19a, and the whole CMOS implementation is shown in Fig. 19b.

The current mirror can be implemented as shown in Fig. 20, which is based on the cascode topology. The current mirror is embedded between the input and output ports labeled as i_{in} and $i_{out}+$, respectively. The third column of MOS transistors replicates the current output $i_{out}+$ that is inverted with another current mirror to provide the current-outputs $i_{out}-$ that are associated to a current follower because they go out. In this topology, the input current i_{in} is mirrored by the output $i_{out}+$, and is copied twice by the embedded current followers by the outputs $i_{out}-$.

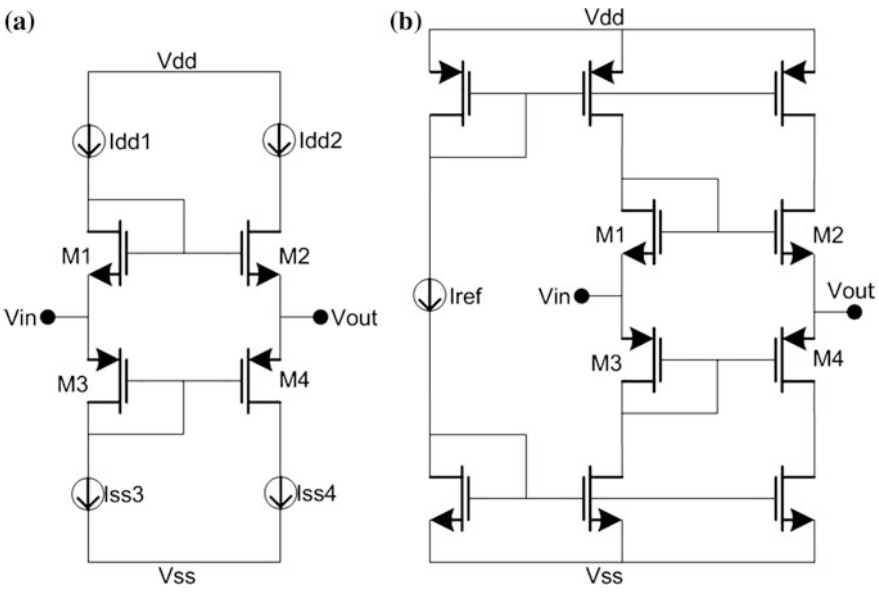

Fig. 18 Voltage follower synthesized from Fig. 13c

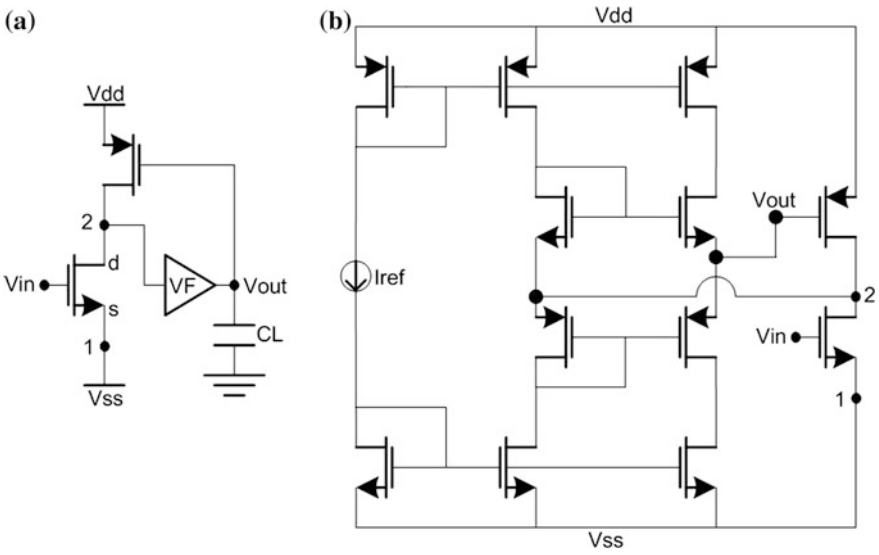

Fig. 19 Voltage mirror consisting of: **a** An inverting topology and a voltage follower (VF), and synthesizing the VF by Fig. 18b

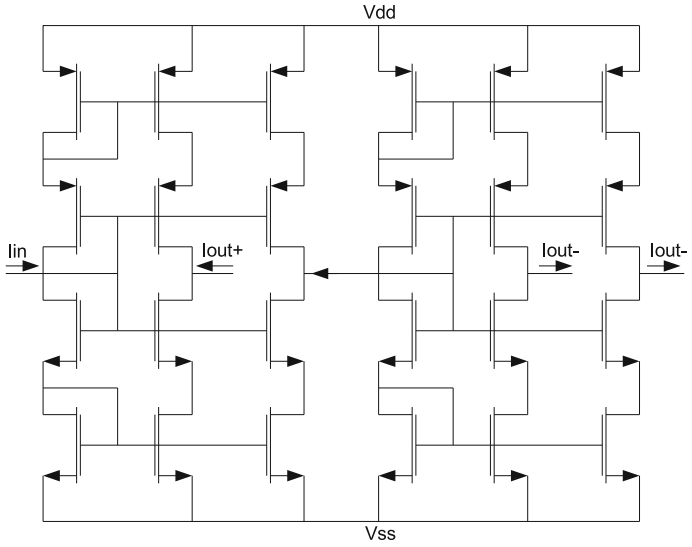

Fig. 20 CMOS implementation of the current follower and current mirror

The four UGCs, namely: VF, VM, CF and CM can be superimposed or interconnected to provide different kinds of amplifiers like current conveyors and current feedback operational amplifiers. For example, Fig. 21f shows the interconnection of a VF with a CM to synthesize a positive-type second-generation current conveyor (CCII+). It can be done by using the VF from Fig. 18a, where: if the current biases are synthesized by simple current mirrors it leads to the VF shown in Fig. 22a, but if the current biases are independently synthesized, e.g. I_{dd1} and I_{ss3} by CMs mirroring the current reference I_{ref} and if I_{dd2} and I_{ss4} are synthesized by cascode CMs providing another port, one gets the CCII+ shown in Fig. 22b. It is easy to see that the ICCII+ can be synthesized by using the VM shown in Fig. 19b. In general, similar interconnections can be performed between two UGCs from Fig. 21 to find novel three terminals amplifiers that work in mixed-mode because they process both voltage and current signals.

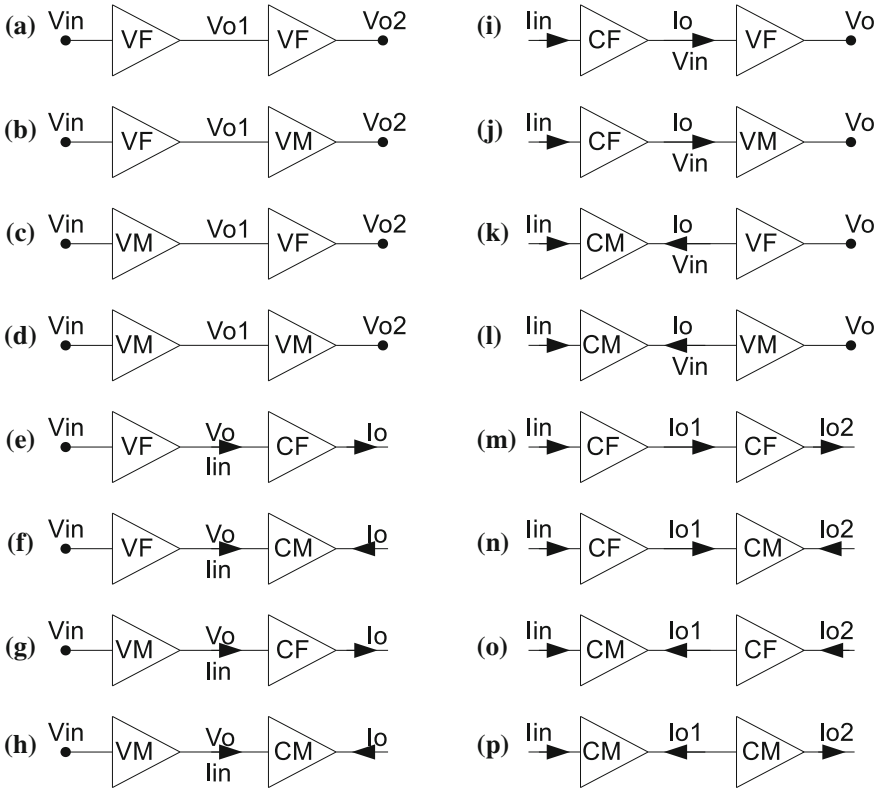

Fig. 21 Examples on interconnecting two UGCs to synthesize three terminals amplifiers

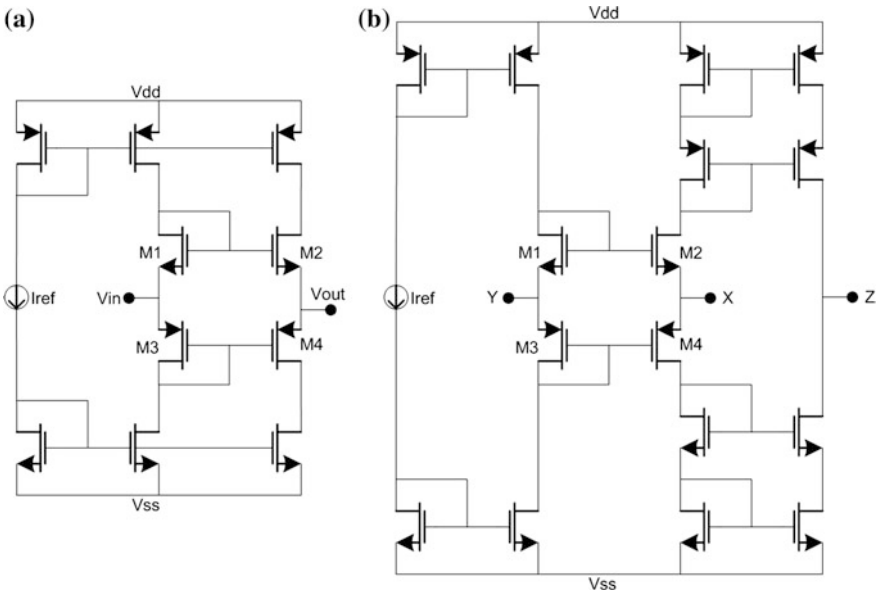

Fig. 22 VF that is superimposed with CMs to synthesize a CCII+

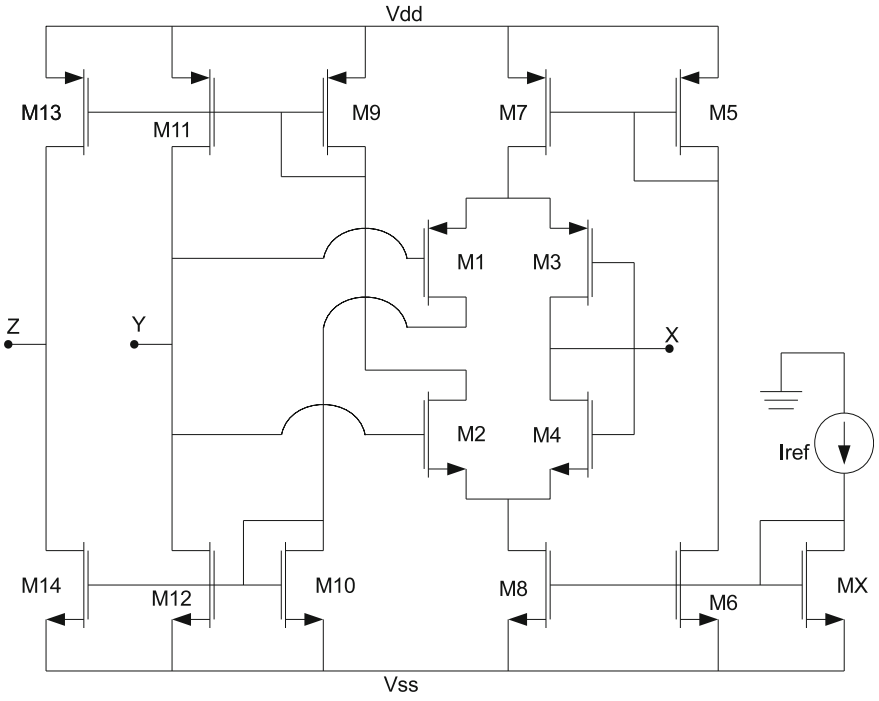

Fig. 23 CCI that is synthesized by a VF and a two-outputs CM, taken from [36]

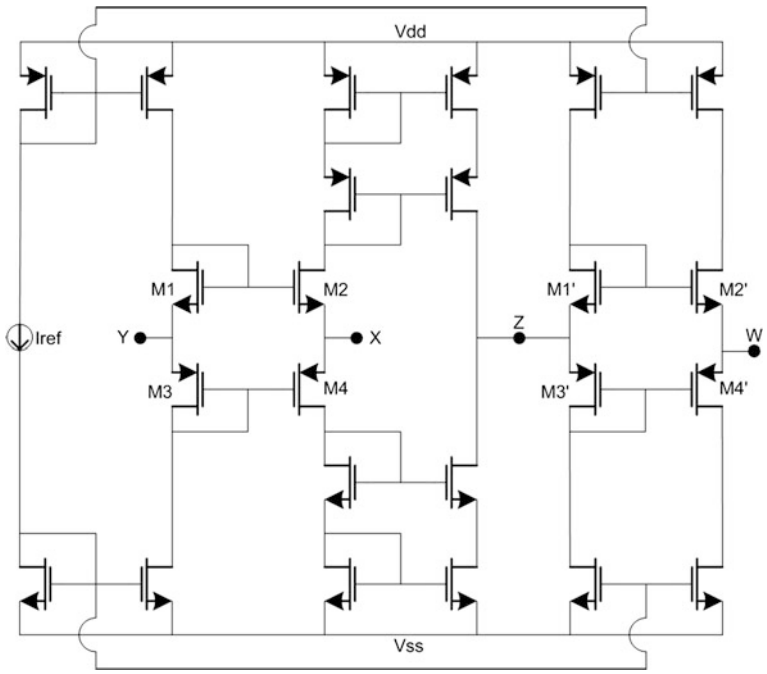

Fig. 24 CCII+ that is connected to another VF to synthesize a CFOA

The UGCs can also provide multiple outputs like the current mirror topologies. They are useful for implementing the first-generation current conveyor (CCI) that must accomplish Vx = Vy, Iy = Ix, and Iz = Ix. From these equations it is easy to see that the currents at ports Y and Z mirror the input current at port X, leading to the CMOS circuit shown in Fig. 23, where the VF is different from the previous circuits and the simple CM provides two outputs. For this and the previous circuits, symbolic analysis can be performed to get insights on their behaviors when synthesizing with different CMOS topologies. For instance, current conveyors present parasitic resistances at their ports that can be minimized by searching for new topologies or by performing circuit optimization [32].

One can also interconnect more than two UGCs, for example: the current-feedback operational amplifier (CFOA) is basically composed of a CM sandwiched by two VFs. Again, by using the VF shown in Fig. 18 and the cascode CM, the resulting CMOS CFOA is shown in Fig. 24, which is also the connection of a CCII+ with a VF. Other VF and CM topologies can also be used to synthesize the CFOA, those topologies will provide different performances that can be compared to choose the most suitable design to accomplish target design specifications.

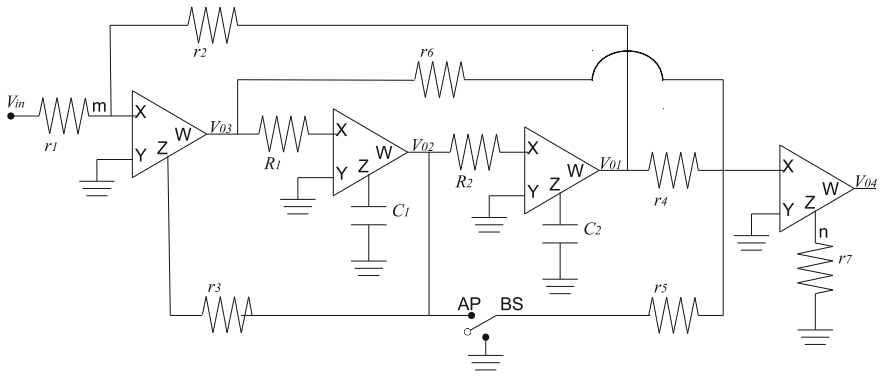

Fig. 25 CFOA-based universal biquadratic filter, taken from [37]

For example, the implementation of the CFOA-based universal mixed-mode filter shown in Fig. 25 requires CFOAs with minimum parasitic impedance at port X and high bandwidth response to improve the design introduced in [37], where the cut-off frequency is low as 100 kHz. Symbolic nodal analysis can be applied to know the effect of the parasitic resistances and capacitances of the CFOA and then to enhance the frequency response of the filter.

The synthesis of the operational transcoductance amplifier (OTA) is more difficult than for mixed-mode circuits by interconnecting UGCs. OTAs are based on a differential pair implemented by two MOSFETs and then more stages are added to increase the gain on the whole amplifier. The gains consist of MOSFETs acting as amplifiers and current mirrors to bias those stages. As the OTA provides current at its output port, then one can use multiple-outputs current mirrors to bias and provide outputs. See for example the OTA designed in [38] and shown in Fig. 26 that has N-channel MOSFETs at its input and simple current mirrors to provide multi-outputs. This OTA has been used in [38] to implement the first-order all-pass filter that consists of two OTAs, one grounded resistor and one grounded capacitor, as shown in Fig. 27. By performing symbolic analysis, the transfer function of this filter is given by (6). Furthermore, this filter can be used to synthesize the current-mode multi-phase sinusoidal oscillator (MSO) shown in Fig. 28, for which the condition of oscillation (CO) and the frequency of oscillation (FO) are given by (7) and (8), respectively, where n is related to the number of stages or first-order all-pass filter sections.

In [38], the sinusoidal outputs provided by the MSO was set up to $n = 5$, and the OTA realization was compared with the one implemented with current-differencing

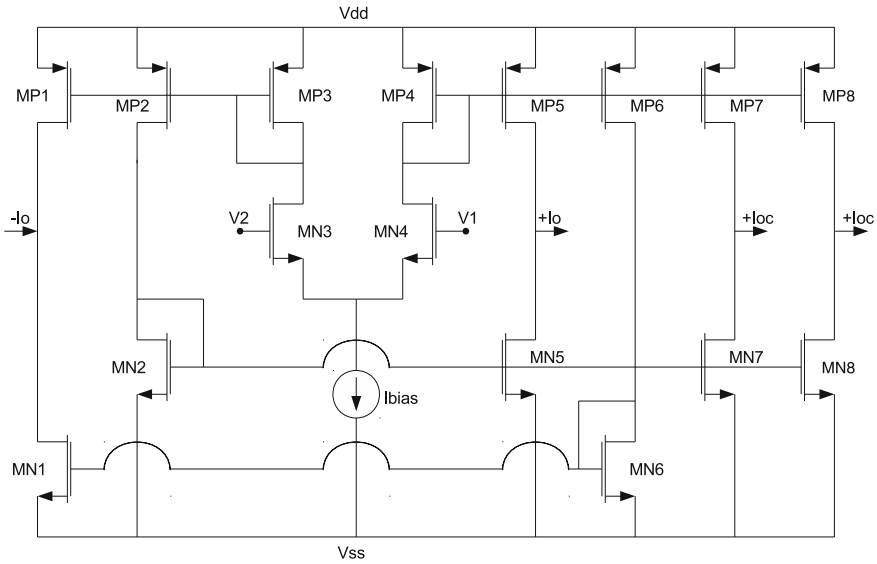

Fig. 26 OTA providing one negative output (−Io), and three positive outputs (+Ioc)

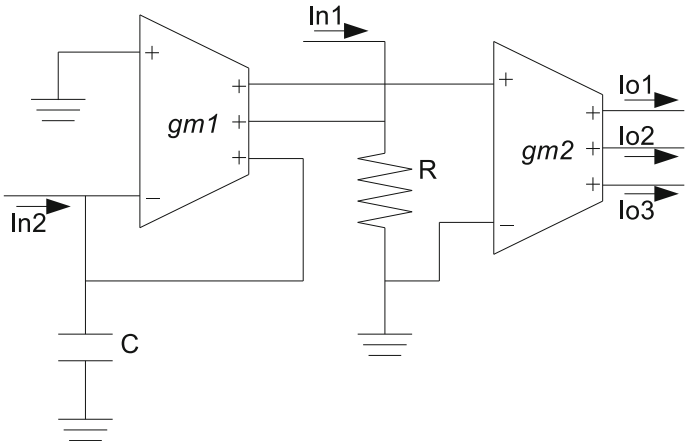

Fig. 27 OTA-based first order all-pass filter

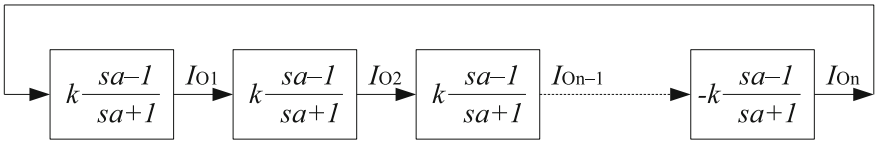

Fig. 28 MSO realized by the cascade connection of first order all-pass filter sections

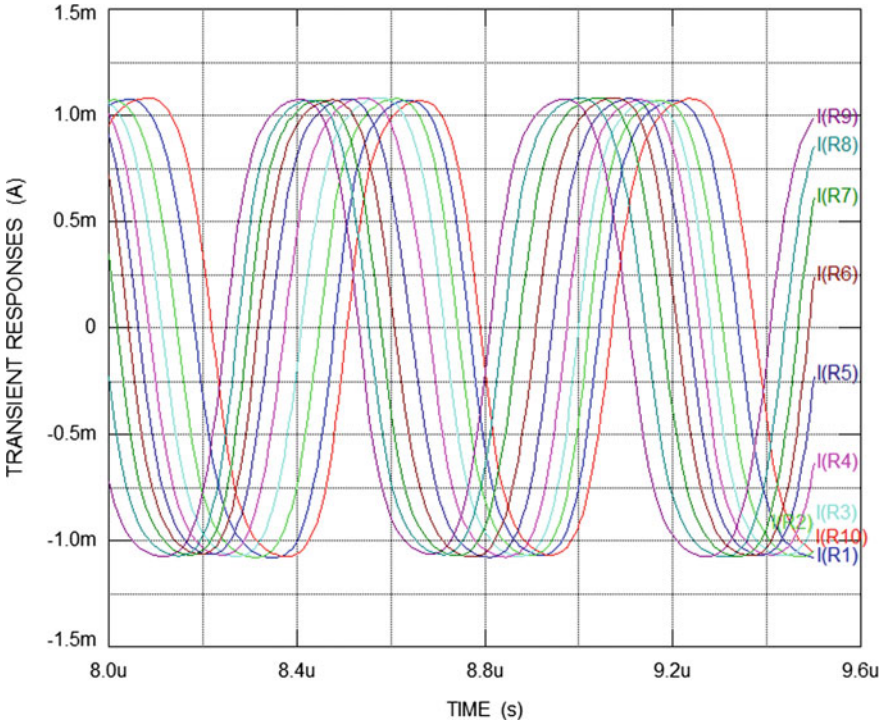

Fig. 29 MSO with $n = 10$ and C = 2 nF to work at FO = 1.71 MHz with g_m = 21.59 I/V

cascaded transconductance amplifiers (CDCTAs), concluding on the suitability of OTAs with multiple-outputs to implement the MSO. In this chapter we show the oscillations with $n = 10$ and $n = 20$ in Figs. 29 and 30, respectively.

$$\frac{I_{01}}{I_{in1}} = g_{m2}R\left(\frac{s\frac{C}{g_{m1}} - 1}{s\frac{C}{g_{m1}} + 1}\right) \tag{6}$$

$$CO : g_{m2}R = 1 \tag{7}$$

$$FO : w_{osc} = \frac{g_{m1}}{c}\tan\left(\frac{\pi}{2n}\right) \tag{8}$$

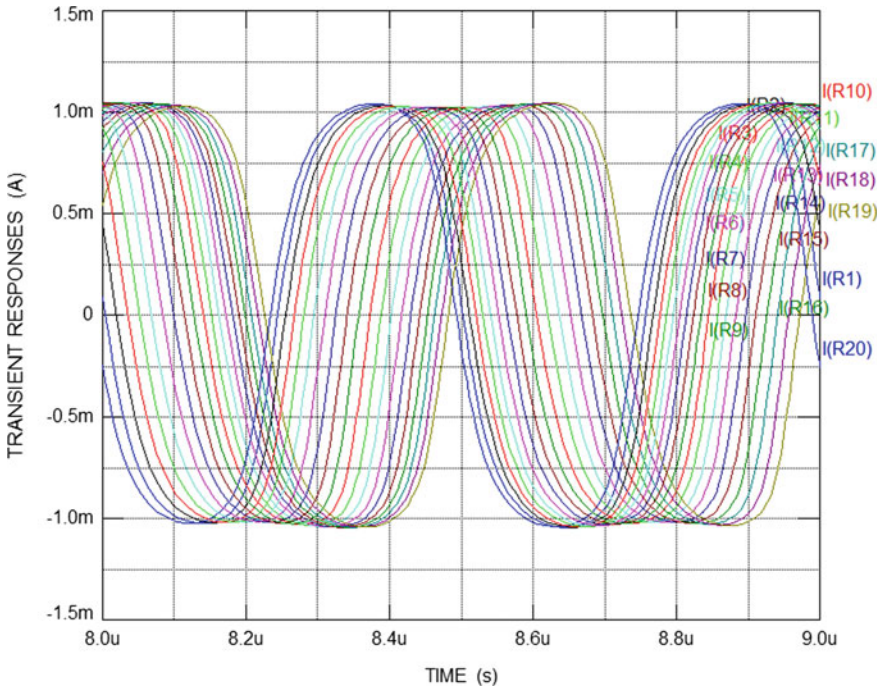

Fig. 30 MSO with $n = 20$ and C = 3.4 nF to work at FO = 2 MHz with $g_m = 86.40$ I/V

6 Conclusions

This chapter discussed the application of symbolic analysis to analog circuits that can be modeled by nullors and pathological current and voltage mirrors. Several related references were provided to highlight that the symbolic analysis of analog circuits modeled by nullors and pathological mirror elements leads us to deal with the nodal admittance (NA) matrix that is more compact than by using traditional modified nodal analysis (MNA).

The second part was devoted to the synthesis of nullor and pathological networks by MOSFETs. It was shown how to synthesize unity-gain cells (UGCs) and mixed-mode amplifiers from nullator, norator and pathological descriptions. Several examples showed that mixed-mode amplifiers can be synthesized from the interconnections of UGCs, and also that operational amplifiers like the OTA can be synthesized by multiple-output current mirrors, differential pairs and so on. Although not shown by examples, a circuit modeled by nullors or pathological elements that is working in voltage-mode can be transformed a current-mode one and vice versa.

The application of UGCs and mixed-mode amplifiers can be found in recent literature. In this chapter the reader can infer that still one can find novel topologies

when synthesizing analog circuits from nullor and pathological element descriptions. In addition, symbolic analysis can be performed to get insights on the behavior of the topologies to mitigate undesired parasitic elements and then to improve their performances.

Acknowledgements This work is partially supported by CONACyT-Mexico under grant 237991.

References

1. Tellegen BDH (1954) La recherche pour una série compléte d'éléments de circuit ideaux non-linéaires. Rendiconti del Seminario Matematico e Fisico di Milano: Conferenza tenuta il. 25(1):134–144. https://doi.org/10.1007/bf02923815
2. Carlin HJ (1964) Singular network elements. IEEE Trans Circuit Theory CT 11(1):67–72. https://doi.org/10.1109/tct.1964.1082264
3. Martinelli G (1965) On nullor. Proc Inst Electr Electron Eng 53(3):332. https://doi.org/10.1109/PROC.1965.3733
4. Myers BR, Martinelli G (1965) Nullor model of transistor. Proc Inst Electr Electron Eng 53 (7):758–759. https://doi.org/10.1109/PROC.1965.4035
5. Roedler D (1971) Node-admittance matrix of an ideal amplifier (Nullor). NTZ Nachrichtentechnische Zeitschrift 24(9):465–466
6. Coldham D, Bruton LT (1973) Computer analysis of nullor networks. Electron Lett 9(4):80–82
7. Hien VH, Mesnard G (1976) Pathological circuits. Int J Electron 40(1):25–36. https://doi.org/10.1080/00207217608920540
8. Huijsing JH, Dekorte J (1977) Monolithic nullor–Universal active network element. IEEE J Solid State Circuits 12(1):59–64
9. Soliman AM, Saad RA (2010) The voltage mirror-current mirror pair as a universal element. Int J Circuit Theory Appl 38(8):787–795
10. Kumngern M, Khateb F, Kulej T (2017) Fully-balanced four-terminal floating nullor for ultra-low voltage analogue filter design. IET Circuits Devices Syst 11(2):173–182
11. Pierzchala M, Fakhfakh M (2014) Symbolic analysis of nullor-based circuits with the two-graph technique. Circuits Syst Signal Process 33(4):1053–1066
12. Shi G (2015) Two-graph analysis of pathological equivalent networks. Int J Circuit Theory Appl 43(9):1127–1146
13. Tlelo-Cuautle E, Sanchez-Lopez C, Moro-Frias D (2010) Symbolic analysis of (MO)(I)CCI (II)(III)-based analog circuits. Int J Circuit Theory Appl 38(6):649–659
14. Nguyen Q-M, Chiang N-H, Tran H-D (2015) Symbolic nodal analysis of conveyor-based circuits considering non-ideal active devices. AEU Int J Electron Commun 69(11):1635–1640
15. Tan L, Liu K, Bai Y (2013) Construction of CDBA and CDTA behavioral models and the applications in symbolic circuits analysis. Analog Integr Circuits Signal Process 75(3):517–523
16. Lin W-C, Wang Hung-Yu, Liu C-Y (2013) Symbolic analysis of active device containing differencing voltage or current characteristics. Microelectron J 44(4):354–358
17. Sanchez-Lopez C, Cante-Michcol B, Morales-Lopez FE (2013) Pathological equivalents of CMs and VMs with multi-outputs. Analog Integr Circuits Signal Process 75(1):75–83
18. Sanchez-Lopez C (2013) Pathological equivalents of fully-differential active devices for symbolic nodal analysis. IEEE Trans Circuits Syst I Regul Pap 60(3):603–615
19. Huang W-C, Wang Hung-Yu, Cheng P-S (2012) Nullor equivalents of active devices for symbolic circuit analysis. Circuits Syst Signal Process 31(3):865–875

20. Soliman AM (2012) Pathological realizations of BOTA and FDDTA using grounded resistors. J Circuits Syst Comput 21(3). Article Number: 1250025
21. Soliman AM (2012) Classification and pathological realizations of transconductance amplifiers. J Circuits Syst Comput 21(1), Article Number: 1250010
22. Soliman AM (2011) Pathological representation of the two-output CCII and ICCII family and application. Int J Circuit Theory Appl 39(6):589–606
23. Sanchez-Lopez C, Fernandez FV, Tlelo-Cuautle E, Tan SX-D (2011) Pathological element-based active device models and their application to symbolic analysis. IEEE Trans Circuits Syst I Regul Pap 58(6):1382–1395
24. Wang Hung-Yu, Huang W-C, Chiang N-H (2010) Symbolic nodal analysis of circuits using pathological elements. IEEE Trans Circuits Syst II Express Briefs 57(11):874–877
25. Tlelo-Cuautle E, Sanchez-Lopez C, Martinez-Romero E, Tan SX-D (2010) Symbolic analysis of analog circuits containing voltage mirrors and current mirrors. Analog Integr Circuits Signal Process 65(1):89–95
26. Liang G, Ma L (2015) Adjoint of a linear multiport element based on generalized duality. IEEE Trans Circuits Syst II Express Briefs 62(1):21–25
27. Lingling Tan Yu, Bai JT (2013) Trans-impedance filter synthesis based on nodal admittance matrix expansion. Circuits Syst Signal Process 32(3):1467–1476
28. Tran H-D, Wang Hung-Yu, Nguyen Q-M (2015) High-Q biquadratic notch filter synthesis using nodal admittance matrix expansion. AEU Int J Electron Commun 69(7):981–987
29. YongAn Li (2015) Systematic derivation for quadrature oscillators using CCCCTAs. Radioengineering 24(2):535–543. (Part: 2)
30. Duarte-Villasenor MA, Tlelo-Cuautle E, Gerardo de la Fraga L (2012) Binary genetic encoding for the synthesis of mixed-mode circuit topologies. Circuits Syst Signal Process 31 (3):849–863
31. Shi G, Tan S, Tlelo-Cuautle E (2014) Advanced symbolic analysis for VLSI systems: methods and applications. Springer
32. Sanabria-Borbón AC, Tlelo-Cuautle E (2017) Sizing analogue integrated circuits by integer encoding and NSGA-II. IETE Techn Rev, 1–7. https://doi.org/10.1080/02564602.2016.1276869. (Published online 2017)
33. Senani R, Gupta SS (2011) Current-mode universal biquad using current followers: a minimal realization. Radioengineering 20(4):898–904
34. Tlelo-Cuautle E, Torres-Muñoz D, Torres-Papaqui L (2005) On the computational synthesis of CMOS voltage followers. IEICE Trans Fundam Electron Commun Comput Sci 88 (12):3479–3484
35. Tlelo-Cuautle E, Duarte-Villaseñor MA, Guerra-Gómez L (2008) Automatic synthesis of VFs and VMs by applying genetic algorithms. Circuits Syst Signal Process 27(3):391–403
36. Tlelo-Cuautle E, Moro-Frías D, Sánchez-López C, Fakhfakh M (2011) Design of current conveyors and their applications in universal filters. In: IEEE 8th international conference on electrical engineering computing science and automatic control (CCE), pp. 1–6
37. Singh VK, Singh AK, Bhaskar DR, Senani R (2005) Novel mixed-mode universal Biquad configuration. IEICE Electron Express 2(22):548–553
38. Tlelo-Cuautle E, de la Fraga LG, Phanrattanachai K, Pitaksuttayaprot K (2015) CDCTA and OTA realizations of a multi-phase sinusoidal oscillator. IETE Techn Rev 32(6):(497–504) (2015)