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Pathological Elements in Analog Circuit Design

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Pathological Elements in Analog Circuit Design

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Foreword

This book focuses on some kind of mystery circuit elements, namely norator, nullator, nullor, current mirror, and voltage mirror, all of them known as pathological elements. As you will see along the chapters of this book, the mystery of those pathological elements relies on its usefulness to perform circuit modeling, symbolic circuit analysis, circuit synthesis, circuit design and to develop applications that involve modern active devices. The nullor concept was introduced to model the ideal behavior of the operational amplifier, and since the works of B. D. H. Tellegen and H. J. Carlin in the 60s, nowadays many researchers introduced contributions on analysis, synthesis, and design of active circuits. More recently, Prof. A. M. Soliman and co-authors have introduced contributions in this new millennium by using the current mirror and voltage mirror, which as a pair they form a universal element, as the nullor does, and they are useful to analyze and discover new designs of active devices.

The editors are active researchers that have already published works on these topics, and they have included a Preface that lists detailed statistics on publications and contributions associated with pathological elements. Personally, I met Prof. Mourad at the SMACD conference held at Gammarth, Tunisia, in 2012. From that time, I have followed his research not only on topics involving pathological elements, but also on circuit optimization. Professor Marian has also published several works using pathological elements in analysis and synthesis of analog circuits. Both editors have been organized eleven chapters in this book entitled: *Pathological Elements in Analog Circuit Design*, which is divided into two parts where you can find details to infer the significance of the pathological elements and of the fixator in analysis, synthesis, design and applications. The chapters highlight the use of the pathological elements to model transistors, voltage amplifiers, current amplifiers, impedance converters, current conveyors, inverting conveyors, operational transconductance amplifiers, operational transresistance amplifiers, and other modern active devices.

Without a doubt, this book will make your imagination to explore new challenges in the application of pathological elements for the modeling, analysis, synthesis, and applications of analog circuits, and we will be happy reading your contributions in these topics.

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Preface

Prior to 1960, electronic circuits and systems were produced by connecting discrete component to discrete devices. Each component or device was packaged separately and connected by means of conducting wires. So, the procedures for analysis, synthesis, and design of electronic circuits were relatively simple. Some network theory and basic techniques were used for such purpose. Circuits were most often analyzed using a combination of *Kirchhoff*'s voltage and current laws. Models of active devices invariably involved resistors, capacitors, inductors, and dependent sources.

In the 1960s, the integrated circuit was developed. This device created entire electronic circuits on or in a silicon wafer. The devices are interconnected through the silicon material or by very small conducting metal strips, deposited on the wafer. Since then, thousands of devices and components can be created on a very small wafer to produce very complex circuits. Although the integrated circuit is technically a circuit composed of thousands of components and devices, it is referred to as an electronic device. Many types of integrated circuits are available, for example, operational amplifiers, current conveyors, transconductance amplifiers, and so on. Due to their complexity, such new elements cannot be analyzed by the conventional simple laws of network theory. The development of new integrated circuits and the complexity of their constructions had stimulated the network theorists to consider new basic elements which allow the circuit designer to analyze and synthesize integrated circuits in more simpler and effective ways. Among various basic elements proposed so far, *nullors*, which are the combinations of nullators and norators, have been regarded to be universal building blocks since all existing analog circuit building blocks can be represented using these elements.

Although the origin of the *nullor* concept itself was advanced as early as 1961–1964, for many years this element was largely regarded as theoretical concept with singular properties. Nowadays, this singular element is considered as a very useful and powerful "tool-kit" as it can be argued by the increasing large number of published papers dealing with the use of such a particular element in analog circuit design (see Fig. 1).

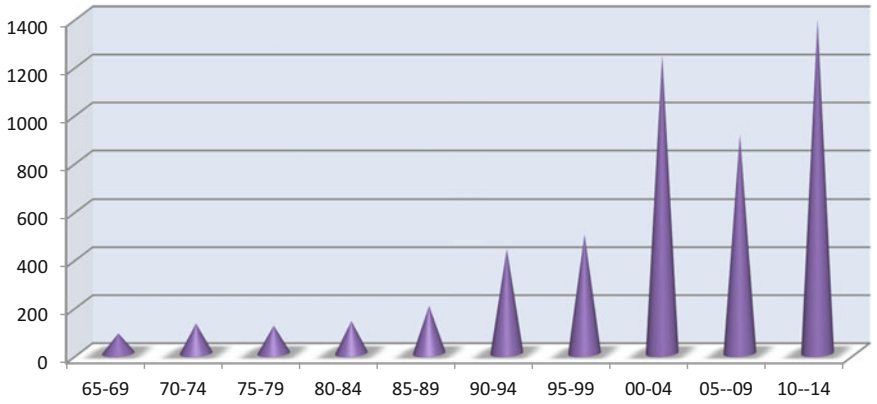

Fig. 1 Quinquennal evolution (since 1965) of the number of papers on *Google Scholar*. (Keywords: *Nullor analog circuit*)

The *mirror* is another singular element which provides a framework not only for analysis, synthesis, and design of integrated circuits but also for interrelating between different network elements. It is a relatively newly known *singular element* (when compared to the *nullor*). It was proposed in 1999.

Nullors and *mirrors* are also called "***pathological elements***" because they do not possess the classical and the conventional obvious properties. Such *pathological elements* are used in a large spectrum of applications in the modern circuit and system theory, as well as in the design practice. Figure 2 shows the evolution of the use of these *pathological elements* in analog circuit design and synthesis (the source of these statistics is "Google Scholar" with the keywords "*pathological elements*", "*analog*", "*circuit*").

In view of the above, therefore, it clearly appears timely to propose a book on these *pathological elements* and their applications in analog circuit modeling, analysis, and synthesis.

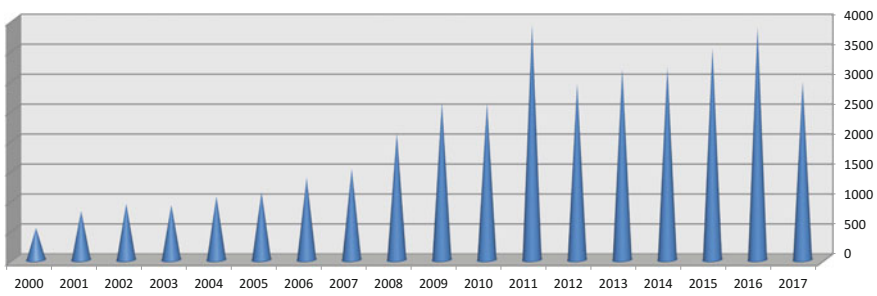

Fig. 2 Annual evolution (since 2000) of the number of papers on *Google Scholar*. (Keywords: *pathological elements analog circuit*)—updated on December 17, 2017

As far as is known, no book has so far been published on this topic yet. This book will fill this void.

The editors have invited some experts from related disciplines involved in the synthesis and design of analog circuits using pathological elements to contribute and give a comprehensive overview of their particular field. In addition, an open call for chapters was launched. A large number of interesting proposals were submitted. Few of them were selected for inclusion in the book.

The book is divided into two parts:

Part I is entitled "Pathological Elements in the Analysis and the Synthesis of Analog Circuits." It encompasses six chapters.

Part II has the title "Pathological Elements in the Design of Analog Circuits." It contains five chapters.

Hereafter, the eleven chapters are succinctly introduced.

Chapter 1 is entitled "Symbolic Analysis and Synthesis of Analog Circuits Using Nullors and Pathological Mirror Elements" and is proposed by *Miguel A. Duarte-Villaseñor, Esteban Tlelo-Cuautle, Luis Gerardo de la Fraga,* and *Carlos Sánchez-López*. It reviews advantages of the (Modified) Nodal Analysis ((M)NA) theory and details the inclusion of pathological voltage mirrors and current mirrors into the NA formulation.

It shows how to perform symbolic circuit analysis and then how to synthesize those circuit elements using MOS transistors. It is also highlighted that from such kind of circuit modeling, one can transform a voltage-mode circuit into a current-mode one and vice-versa. The authors show the design of both modes of operation at the transistor level of design, for which they also provide details on the synthesis approach where each nullator, norator, voltage mirror, and current mirror can have multiple options to be implemented with MOS transistors. Several examples are provided to appreciate the advantages of the NA formulation from analog circuits modeled by nullors and mirrors, the symbolic circuit analysis, the transformation from voltage-mode to current-mode and vice-versa, and the synthesis of pathological circuits by using MOS transistors.

Chapter 2, "Generalized Parameter Extraction Method for Symbolic Analysis of Analog Circuits Containing Pathological Elements", authored by *Vladimir Filaretov, Konstantin Gorshkov, Sergey Kurganov,* and *Maxim Nedorezov* deals with a description of the extension of Generalized Parameter Extraction Method (GPEM) for symbolic analysis of large-scale analog circuits containing pathological elements. A brief overview of the parameter extraction approach is offered. An algorithm implementing the concept of Higher Order Summative Cofactors (HOSCs) for determinants computation of the pathological elements-based circuits is also proposed. Furthermore, the hierarchical decomposition techniques of upward and downward analysis of electronic circuits by GPEM are presented.

Chapter 3, entitled "Two-Graph-Based Semi-topological Analysis of Electronic Circuits with Nullors and Pathological Mirrors" and proposed by *Marian Pierzchala* and *Mourad Fakhfakh*, deals with the abstraction level elements such as nullator, norator, current mirrors, and voltage mirrors that have been very useful in the analysis of linear circuits. In this chapter, the authors propose a method for the

analysis of linear circuits with the pathological elements which are based on the two-graph representation of these elements and the semi-topological procedure of calculations of the network functions. For completeness, the method has been extended to encompass RLC-elements, all types of controlled sources, voltage, and current independent sources. The procedure of calculation is based on the product matrices and on a numerical formula of evaluation of unimodular determinants. No sign rule is required for their evaluations, and canceling terms are extracted during their evaluations.

Chapter 4, "Circuit Analyses with Nullors" authored by *Mihai Iordache, Lucia Dumitriu, Dragos Niculae, Marilena Stanculescu, Victor Bucata,* and *Georgiana Rezmerita*, is dedicated to the analysis of the circuit with nullors using the topological approach for transfer function generation by two-graph tree enumeration. The nullor-based modeling of active devices from the circuit level of abstraction is described in detail, and the generalized topological formula with homogeneous parameters is proved for all the circuit functions. The simple representation of the four types of controlled sources by admittances allows a uniform treatment of the entire circuit in terms of admittances. Rules to automatically generate the two graphs and to enumerate the common spanning trees are presented, and a discussion considering the known conversion techniques of the controlled sources is offered.

Chapter 5 that is entitled "Symbolic Sensitivity Analysis Enhanced by Nullor Model and Modified Coates Flow Graph" and proposed by *Irina Asenova* and *Franciszek Balik* shows how pathological elements like nullors can be exploited to symbolic sensitivity analysis enhancement. A method of first-, second-order, and multiparameter symbolic sensitivity determination based on the nullor model of active devices and modified Coates flow graph is presented. The method performs symbolic sensitivity analysis with respect to various circuit parameters appeared not only at one location in the nullor model. Illustrative examples on symbolic sensitivity analysis are given. Advantages of the proposed Coates graph-based method are stressed. Comparison results for the multiparameter sensitivity calculations of the voltage transfer function are presented via application examples.

Chapter 6 titled "Synthesis of Electronic Circuits Structures on the Basis of *Active Switches*", which is authored by *Marian Pierzchala* and *Mourad Fakhfakh*, presents a novel idea for the synthesis of electronic circuits' structures. It is based on the use of "*active switches*" which can be considered as circuit implementation of the pathological elements since they connect and/or disconnect different elements in the circuits and thus impose on their terminals specific voltages and currents in a similar way as nullors and mirrors. Furthermore, the authors shows that this new technique allows not only demystifying the process of finding new circuits structures but also opens large research areas for proposing new ones.

Chapter 7 "Applications of the Voltage Mirror-Current Mirror in Realizing Active Building Blocks" by *Ahmed M. Soliman* highlights four alternative realizations of the nullator using a single voltage mirror (VM) or two VMs. Similarly four alternative realizations of the norator using a single current mirror (CM) or two CMs are also demonstrated. It is also shown that the VM-CM pair can be used to realize a nullor and many other analog basic building blocks without the use of any

external resistors. The use of the VM-CM pair with additional resistors to realize the family of controlled sources, transconductance amplifiers, and other active building blocks using NAM expansion is included. Moreover, it is shown that the Nullator-CM pair as well as its adjoint which is the VM-Norator pair can also be used as universal building blocks.

Chapter 8, "Circuit Biasing Using Fixator-Norator Pairs—A Tutorial" by *Reza Hashemian*, describes a procedure based on local biasing. This procedure initiates from port nullification and extends to nonlinear device nullification. It is shown that when a device internally powered but is nullified through its ports, it is locally biased. The difference between locally biased devices with full supplies or with reduced number of supplies is discussed. It is presented the technique of biasing through the use of fixator norator pairs (FNPs) that allow fixing each circuit transistor to its designated operating point, just like local biasing, while the power supplies remain in their normal location in the circuit (global biasing). Properties on fixators and norators are discussed, and component modeling using FNPs are introduced.

Chapter 9 titled "Fixator-Norator Pair Based Design of Analog Circuits" authored by *R. Rohith Krishnan* and *S. Krishnakumar* focuses on an approach toward the design and analysis of analog circuits via the use of fixator-norator pairs (FNPs). A brief explanation about the possible realizations of FNPs is introduced, and then the use of FNPs in source allocation, source transformation, and biasing design are presented. The proposed chapter also deals with the design of analog integrated circuits based on FNPs. In addition, the chapter considers a complete AC performance design case. All the proposed techniques are proved via some example circuits.

Chapter 10 entitled "Application of Fixator-Norator Pairs in Analog Circuit Design" by *Reza Hashemian* introduces fixator norator pairs (FNPs) as powerful tools for designing analog circuits. It stresses the application of FNPs in analog circuit designs, including biasing, gain, input and output impedances, and frequency responses. It also highlights the use of FNPs in designing active loads and current mirrors in IC circuits. The author shows the utility and the necessity of using a model circuit for designing a circuit with a specific bandwidth and frequency profile. This model circuit provides the frequency response needed, and FNP is used to force the original circuit to follow the model circuit on its bandwidth.

Chapter 11, "Nullor-Based Negative-Feedback Memristive Amplifiers: Symbolic-Oriented Modelling and Design", by *Arturo Sarmiento-Reyes* and *José Balaam Alarcón-Angulo* deals with a new strategy for the design of nullor-based memristive amplifiers with memistor realization of the nullor. This strategy allows the implementation of the amplifier in a full memristive circuit. Moreover, a fully symbolic memristor model is introduced, and the most important fingerprints are highlighted. This model is used along the analysis and design steps. The model has been recast as a behavioral model in Verilog-A. In the first stage, the memristive amplifiers are composed by the nullor and a memristive feedback network. Noise and harmonic analyses are carried out with symbolic and numerical simulations. In

the second stage, the nullor is implemented by a memistor. Special attention has been devoted to the noise contribution of the memistor. Finally, a transmemristance amplifier has been used as case study for the memistor implementation of the nullor, and noise and harmonic analyses are also offered.

Finally, the editors wish to use this opportunity to thank all the authors for their valuable contributions, and the reviewers for their help for improving the contributions' qualities.

The editors are also very thankful to Thomas Ditzinger, Springer Executive Editor, for his valuable support. Our thanks go also to all the Springer team, especially to Ramya Chandran, Springer Project Coordinator, for her continued assistance throughout the preparation of the book.

Enjoy reading the book.

Sfax, Tunisia — Mourad Fakhfakh
Wrocław, Poland — Marian Pierzchala

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Part I
Pathological Elements in the Analysis and the Synthesis of Analog Circuits

Symbolic Analysis and Synthesis of Analog Circuits Using Nullors and Pathological Mirror Elements

Miguel A. Duarte-Villaseñor, Esteban Tlelo-Cuautle, Luis Gerardo de la Fraga and Carlos Sánchez-López

Abstract It has been demonstrated that symbolic circuit analysis of analog circuits modeled by nullors and pathological mirror elements leads us to deal with the nodal admittance (NA) matrix that is more compact than by using traditional modified nodal analysis (MNA). This chapter reviews such a theory and details the inclusion of pathological voltage mirrors and current mirrors into the NA formulation. In this manner, from a circuit topology consisting of nullors and mirrors we show how to perform symbolic circuit analysis and then how to synthesize those circuit elements using MOS transistors. It is also highlighted that from such kind of circuit modeling, one can transform a voltage-mode circuit into a current-mode one and vice versa. We show the design of both modes of operation at the transistor level of design, for which we also provide details on the synthesis approach where each nullator, norator, voltage mirror and current mirror can have multiple options to be implemented with MOS transistors. Several examples are provided to appreciate the advantages of the NA formulation from analog circuits modeled by nullors and mirrors, the symbolic circuit analysis, the transformation from voltage-mode to current-mode and vice versa, and the synthesis of pathological circuits by using MOS transistors. The synthesized circuits are unity-gain-cells, a current conveyor, a current-feedback operational amplifier, and an operational transconductance amplifier, which are designed with standard CMOS integrated circuit technology, and they are applied to implement active filters and oscillators.

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1 Introduction

By April 23 in 1954, during the Seminario Matematico e Fisico di Milano, B. D. H. Tellegen stated that [1]: The nullator (the linear time-invariant one-port with $v = i = 0$) and the norator (the linear time-invariant one-port with v and i arbitrary), which are shown in Fig. 1a, both are singular elements. Ten years later, Carlin published the article entitled "singular network elements" [2], where he discussed the physical realizability of the singular linear network elements: the nullator (simultaneously an open and a short circuit), and the norator (the unique nonreciprocal one-port with arbitrary port voltage and current). Carlin modeled the nullor as a two-port network consisting of one nullator and one norator as shown in Fig. 1a. The nullor can also be modeled by two nullators and two norators as shown in Fig. 1b, because from the properties of the nullator, the current at the output port remains through the norators while the voltage across the nullators remains equal to zero. Carlin also predicted that the nullor would be amenable for use in practical electronic systems, as highlighted in the rest of this chapter.

Using the nullor, the ideal model of the bipolar junction transistor (BJT) was introduced in [3], where the base (B), collector (C) and emitter (E) terminals are denoted as shown in Fig. 2a. As one sees, the voltage between BE is the sum of the voltage across the nullator and the resistor, however, since the voltage across the nullator beings zero, then the input voltage drops across terminals AB where a resistor is connected. Also, since the current through the nullator beings zero, then the current through the resistor goes to the output through the collector. In a similar way, nowadays the model in Fig. 2a can be used to describe the MOSFET whose terminals are gate (G), drain (D) and source (S). In both models for the BJT and MOSFET, the output current is proportional to the inverse of the resistance value, which for amplifier design it is known as the transconductance denoted by g_m. In an extended version like the topology shown in Fig. 2b, the output is also a current that is proportional to the transconductance g_m in which the input voltage drops because the voltage across the nullators being zero, so that $i_o = g_m v_{in}$ and the direction is imposed by the polarities of the nullators, i.e. the negative input goes to terminal A and the positive input goes to B, so that the polarity of the transconductance g_m goes

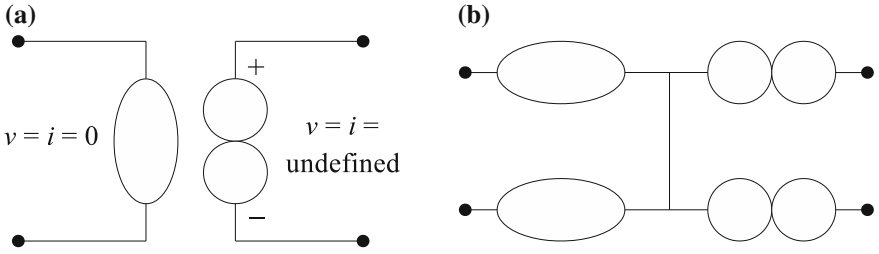

Fig. 1 Nullor representation using: **a** One nullator and one norator, and **b** two nullors and two norators

from B(+) to A(−), as denoted by the arrows in the norators at the output port, and as shown in Fig. 2b. It is also possible to joint a nullator-norator pair to model a negative-type second-generation current conveyor, as shown in Fig. 2c, where the equations $v_x = v_y$, $i_y = 0$ and $i_z = -i_x$ are accomplished. These models will be used in the next sections to show how to perform symbolic analysis and synthesis of nullor and pathological mirror networks.

The authors in [4] also introduced a nullor model of the transistor, but they pointed out that the use of T parameters permit certain advantages over the nullor-based model in the design of transistor networks. Later, in [5] the nodal admittance matrix formulation was introduced for the ideal amplifier or circuits consisting of nullors and passive circuit elements. This contribution was quite useful to perform computer analysis of nullor networks, as highlighted in [6], where a nullor version of a generalized immittance convertor (GIC) was analyzed, and where the nullator was labeled as Z and the norator as A. The program was implemented in Fortran IV, the maximum number of nodes was 20 and maximum numbers of branches 40, but those limits were only restricted by the size of the computer's core store.

The term pathological was introduced in 1976 [7], it was referred to nullor circuits for circuit analysis. The usefulness of the nullor for circuit analysis established a challenge for circuit design, so that the first monolithic implementation of the nullor, which was also referred as a universal active device, was introduced in 1977. That way, the authors in [8] claimed that if the floating nullor (having both the input and output port independently floating) is used, then all kinds of transfer functions could be fixed by using the minimum number of external passive and precision components. Up to now, still the design of the monolithic integrated nullor is a challenge because of the need to provide large internal gain. The integrated design presented in 1977 was developed by using bipolar technology and the floating nullor consisted of a differential input stage, a symmetrical level shift stage, and a differential output stage.

It was until 2010 that the authors in [9] introduced the concepts of the pathological voltage mirror (VM) and current mirror (CM) elements. Both pathological mirrors could also be used as a pair to model a universal active element, as it was

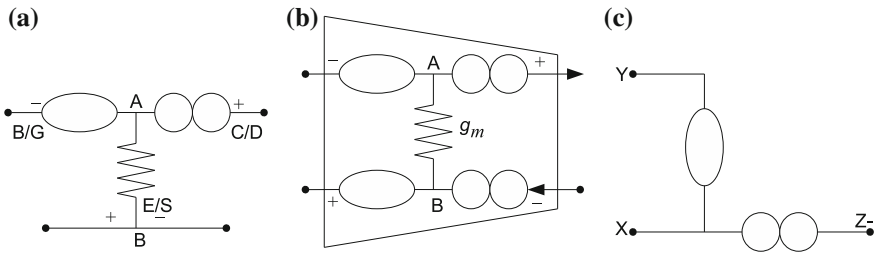

Fig. 2 Ideal model of: **a** The bipolar junction transistor (BJT) (or metal-oxide-semiconductor field-effect-transistor (MOSFET)), **b** the operational transconductance amplifier (OTA), and **c** negative-type second-generation current conveyor (CCII-)

done for the nullor. The work in [9] showed that the pathological VM-CM pair provides two alternative realizations for the nullor, and it is also capable of realizing the traditional operational amplifier and the four types of the second-generation current conveyors (CCII), namely: the negative-type CCII-, the positive-type CCII +, the inverting CCII- (ICCII-), and the inverting CCII+ (ICCII+), as shown in Figs. 3 and 4, respectively. The VM and CM are connected in a special way to accomplish the equations modeling each kind of current conveyor, for example: $v_x = v_y$, $i_y = 0$ and $i_z = -i_x$ for the CCII-; $v_x = v_y$, $i_y = 0$ and $i_z = +i_x$ for the CCII +; $v_x = -v_y$, $i_y = 0$ and $i_z = -i_x$ for the ICCII-; and $v_x = -v_y$, $i_y = 0$ and $i_z = +i_x$ for the ICCII+.

In a high level of abstraction, the nullor can also be implemented by joining two CCIIs as already shown in [10], however the CCII has a parasitic resistance at its X-port terminal and then the equivalent circuit looks like an OTA, as shown in Fig. 2b. The authors in [10] compared their CMOS design of a fully balanced four-terminal floating nullor (FBFTFN) with other integrated realizations. Those authors highlighted that their FBFTFN was superior providing suitability for ultra-low-voltage and low-power applications. The FBFTFN was designed with TSMC 0.18 μm n-well CMOS technology with supply voltage of 0.5 V and dissipation power of 9.4 μW, and it employed the bulk-driven quasi-floating-gate (BD-QFG) metal–oxide–semiconductor transistor technique to provide the capability of ultra-low-voltage, low-power operations as well as extended input voltage range. To demonstrate the usefulness of the CMOS FBFTFN, it was tested by implementing fully balanced filters, such as: band-pass Sallen–Key filter, voltage-mode universal biquadratic filter and current-mode sixth-order low-pass filter. However, this novel integrated design has also parasitic impedances that for direct current it also can be modeled as parasitic resistance as shown in Fig. 2b.

As one can infer, by using nullators, norators, VMs and CMs one can model all kinds of active devices, as already shown in [11–24], where in some cases they are called pathological circuit elements. Their usefulness in computing symbolic

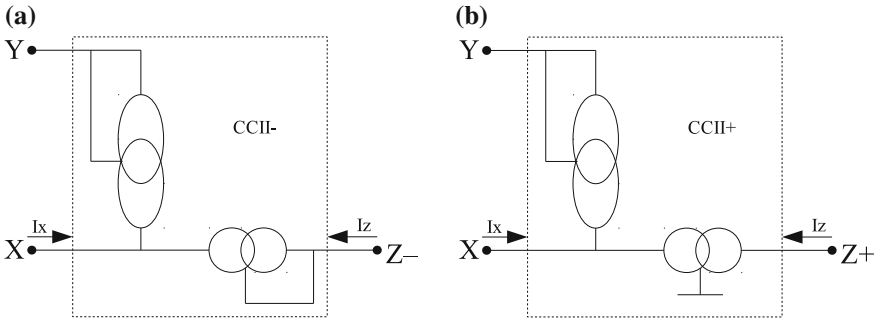

Fig. 3 Pathological VM-CM pair used to model the **a** negative-type second-generation current conveyor (CCII-) and the **b** positive-type second-generation current conveyor (CCII+), taken from [9]

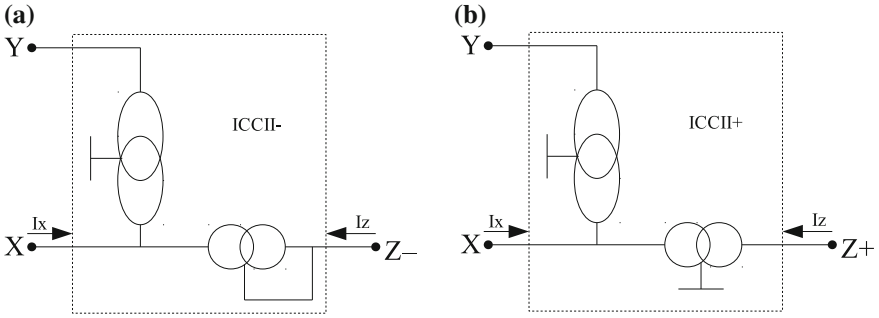

Fig. 4 Pathological VM-CM pair used to model the **a** inverting CCII- and the **b** inverting CCII+, taken from [9]

expressions have also been demonstrated in various recent works, where the main goal is to get insights into the effect of each circuit element in the biasing and sizing of analog integrated circuits to enhance performances in alternate and direct current, and time domains. As already mentioned in [11], very efficient symbolic analysis methods, such as nodal analysis, Coates flow graphs, and two-graphs are widely used. The works in [11, 12] used ICCII-based circuits to show the usefulness of performing graph operations to compute symbolic expressions. A more general modeling approach for current conveyors is given in [13], where one can find models of single and multiple outputs (MO) for the first, second and third generation current conveyors, their inverting topologies and their positive and negative types denoted as (MO)(I)CCI(II)(III)±. In [13], the authors showed how to include parasitic elements to the current conveyors, as done in [14]. Other active devices are modeled by using pathological elements trying to capture the dominant behavior, as shown in [15], and including differencing voltage and current characteristics, as highlighted in [16]. As one sees, the pathological VM-CM pair is quite useful to increase the modeling capabilities of active devices because they can provide multi-outputs (MO) [17], as it is quite common in integrated circuit design using current mirror topologies at the transistor level of abstraction.

A very complete list of pathological equivalents of fully differential active devices is given in [18], where some examples are provided to show how to perform symbolic nodal analysis. Other nullor equivalents and pathological realizations for application to symbolic circuit analysis are given in [19–24]. If one performs symbolic analysis of only nullor networks, the VM-CM pair can be modeled using nullor equivalents as shown in [25], which allows including parasitic elements to the MO versions. The next section shows some examples of performing symbolic nodal analysis of analog integrated circuits modeled by nullators, norators, VMs and CMs. Afterwards, we show how to transform a circuit working in voltage-mode to a circuit working in current-mode and vice versa. In such a case the adjoint and duality properties are applied, as already shown in [26], where some examples show their

usefulness to solve the problems such as the inflexible positions of the port variables, and inability for the conditions that both circuit and voltage of a port are independent (or dependent) variables.

The symbolic analysis tools are quite useful to analyze all kinds of analog integrated circuits modeled by nullators, norators, VMs and CMs, and working in either voltage or current modes. In fact, in the synthesis of analog circuits, a symbolic analysis tool can be used in the loop for verifying the desired transfer function and then to test the frequency response. Among the synthesis approaches based on nodal analysis, some key references are [27–29]. In such cases, every nullator, norator, VM and CM can be implemented with transistors, as demonstrated in [30], where the nullator is synthesized by a voltage follower (VF), the norator is synthesized by a current follower (CF), and the VM and CM by their corresponding CMOS topologies. All of them can be extended to provide multiple outputs, as shown in the rest of this chapter. Section 2 summarizes the recent advances in symbolic analysis techniques for design automation of nanometer VLSI systems [31]. Section 3 shows the transformation of voltage-mode circuits to current-mode ones and vice versa. Section 4 shows the synthesis of the pathological nullator, norator, VM and CM elements by using CMOS integrated circuit technology. Section 5 shows some integrated circuit designs of unity-gain cells, current conveyors, current-feedback operational amplifier and OTA, which are optimized by metaheuristics like in [32], and they are applied to implement active filters and oscillators. Finally, the conclusions are listed in Sect. 6.

2 Symbolic Nodal Analysis of Circuits Modeled by Nullors and Mirrors

Symbolic circuit analysis is a complement to numerical simulation, and it is a systematic approach to obtaining the knowledge of analog building blocks in analytic form. The history of symbolic circuit analysis is given in [31], in which is mentioned that this field gained real momentum in the 1950s when electric computers were introduced and used for circuit analysis, while the first general-purpose circuit analysis programs emerged in the early 1960s, when a basic goal behind computer-aided design and analysis of analog circuits was to formulate network equations by matrix algebraic or topological techniques. In the frequency domain, the circuit equations of a lumped linear or linearized time-invariant analog circuit can be formulated by applying nodal analysis in the general matrix form given by (1), where $\boldsymbol{A}$ is an $n \times n$ sparse admittance matrix (n as the rank of the matrix), $\boldsymbol{b}$ is a vector of external sources, and $\boldsymbol{x}$ the vector of unknowns.

$$Ax = b \tag{1}$$

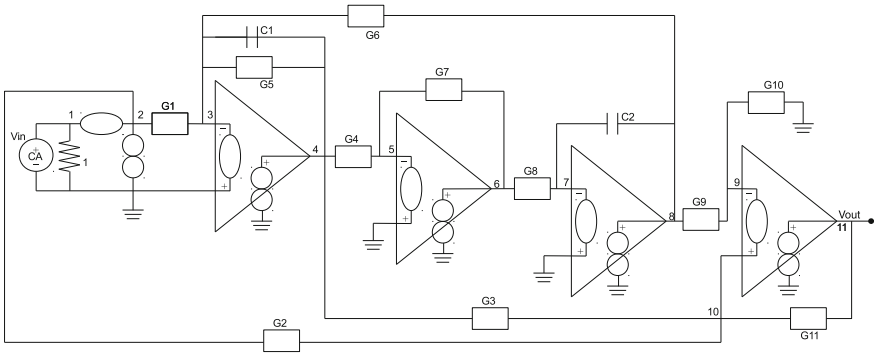

Fig. 5 RC filter consisting of operational amplifiers modeled by nullors

Symbolic analysis of analog integrated circuits solves (1) in which the matrix elements a_{ij} can be real numbers, rationals in the frequency domain s, semi-symbolic or fully symbolic expressions. Reference [31] provides graph and matrix-based methods to solve (1). For example, the RC filter shown in Fig. 5 consists of operational amplifiers (opamps) that are modeled using the nullor and the independent voltage source is transformed to an independent current source among nodes 1 and 2. As already shown in [13–19, 23–25], the order of the nodal admittance matrix must be equal to the number of nodes minus the number of nullors, so that the resulting system of equations has the form like in (1), and it is given by (2). The reduced matrix was obtained by applying the nullator and norator properties, which are summarized as follows:

1. If a nullator is connected between node i and ground, from its voltage property node i has the same potential as ground, and therefore the voltage variable associated to node i is eliminated, thus reducing one column in the admittance matrix.
2. If a nullator is floating, e.g. connected between nodes i and j, from its voltage property both nodes i and j are virtually connected, so that a single voltage-node variable $v_{i,\,j}$ is associated to both nodes i and j, thus reducing one column in the admittance matrix.
3. If a norator is connected between node k and ground, from its current property node k should be grounded and therefore eliminated as current variable, thus reducing one row in the admittance matrix.
4. If a norator is floating, e.g. connected between nodes k and l, from its current property both nodes k and l are virtually connected, so that a single current-branch variable $i_{k,\,l}$ is associated to both nodes k and l, thus reducing one row in the admittance matrix.

$$\begin{bmatrix} v_{in} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ -G_1 & -G_5 - sC_1 & 0 & -G_6 & 0 & 0 \\ 0 & -G_4 & -G_7 & 0 & 0 & 0 \\ 0 & 0 & -G_8 & -sC_2 & 0 & 0 \\ 0 & 0 & 0 & -G_9 & G_9 + G_{10} & 0 \\ -G_2 & -G_3 & 0 & 0 & G_2 + G_3 + G_{11} & -G_{11} \end{bmatrix} \begin{bmatrix} v_{1,2} \\ v_4 \\ v_6 \\ v_8 \\ v_{9,10} \\ v_{11} \end{bmatrix} \tag{2}$$

In the previous RC filter, the opamps are modeled by nullors and avoid non-idealities but the models can also include parasitic elements, as shown in [13]. The solution to (2) can be obtained by applying the methods given in [31].

As one can infer, to take advantage on performing computer-aided analysis all active devices should be modeled with the appropriate pathological elements. Figure 2a shows the ideal model of the BJT or MOS transistor, and Fig. 2b shows an extended version to model the OTA and which can also be associated to modeling the voltage-controlled current source (VCCS). Figure 6 shows the nullor equivalents of the four controlled sources, voltage-controlled voltage source (VCVS), VCCS, current-controlled voltage source (CCVS), and current-controlled current source (CCCS), which can be used to model any kind of active devices. For example: Fig. 7 shows the four terminals MOSFET including parasitic resistances at the drain, gate, source and bulk terminals, the output conductance g_o, and parasitic capacitors among two terminals. The conventional model consists of two VCCSs that have been implemented by one nullor and one resistor because one nullator-norator pair is in parallel and it is equivalent to a short circuit.

The current mirror is quite useful in designing active devices like the OTA Miller shown in Fig. 8a, in which two current mirrors are embedded, one by M3–M4 and the other by M5–M6–M7. Those current mirrors can be modeled using nullors to obtain the nullor equivalent shown in Fig. 8b, where one can count 15 nodes (node 5 is already grounded but labeled to appreciate de joint connection of a nullator-norator pair associated to MOSFET M5 in Fig. 8a) and Fig. 9 nullors or nullator-norator pairs. In this manner, the system of equations formulates an admittance matrix having an order equal to the number of nodes (15), minus the number of nullors (9): 15 – 9 = 6. One can also perform sensitivity analysis after solving the system of equations and noise analysis, as already detailed in Chap. 9 in [31].

The pathological VM and CM elements can also be used to model active devices with multiple-outputs. For instance, Fig. 9 shows the nullor-CM equivalent of a current mirror with one negative current-output i_{z-} and one positive current-output i_{z+}. Such an equivalent can be used to analyze the current-mode filter that consists of one current follower (CF) labeled as 2 in Fig. 10a, one 2-outputs current mirror labeled as 1, one 3-outputs current mirror labeled as 3, 2 resistors R_1 and R_2, and 2 capacitors C_1 and C_2. Those current mirrors can be modeled by using the equivalent from Fig. 9 leading to the pathological equivalent shown in Fig. 10b, where it can be appreciated that 3 resistors are added to the outputs to measure the currents for the

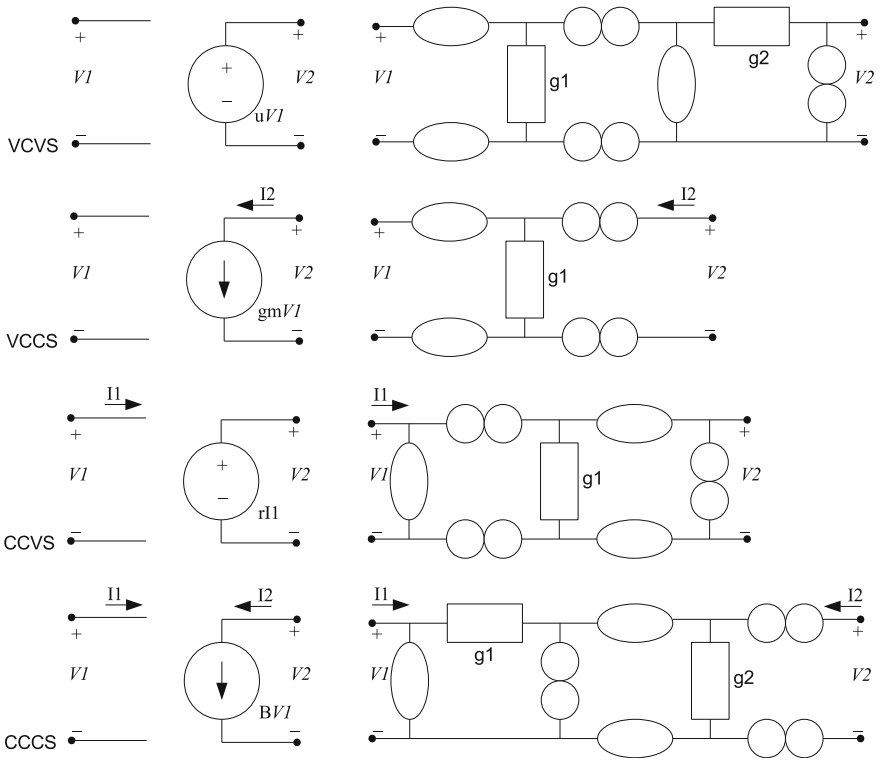

Fig. 6 Nullor equivalents of the four controlled sources

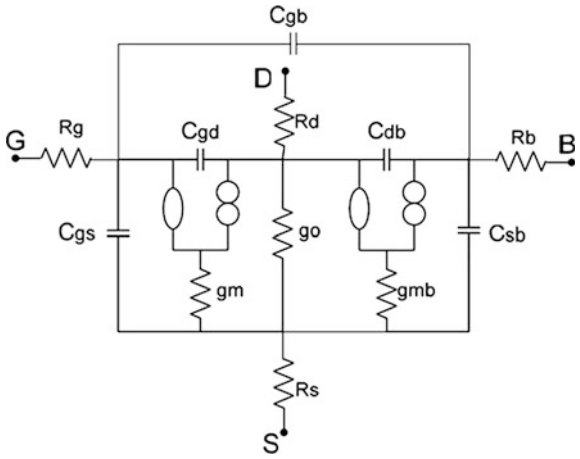

Fig. 7 Small-signal model of the four terminals MOSFET including parasitic elements

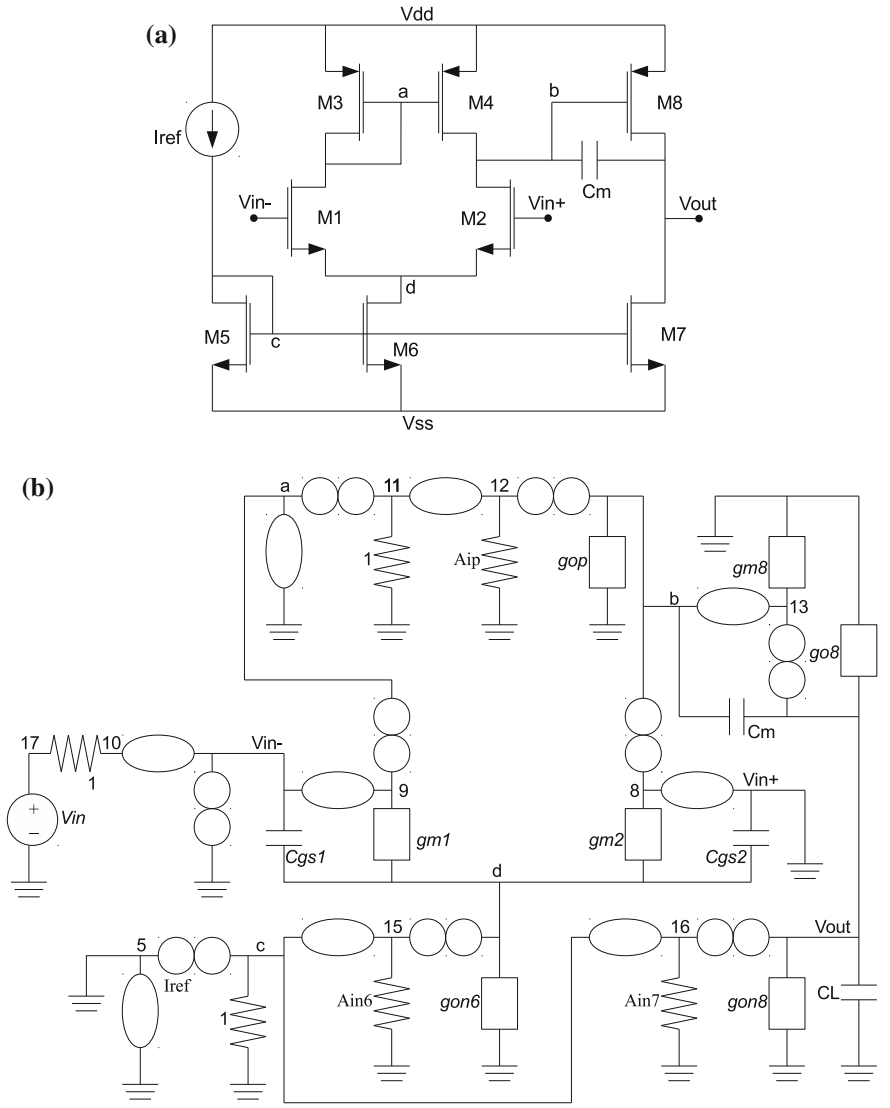

Fig. 8 Miller amplifier: **a** MOSFET circuit and its **b** nullor equivalent taken from [31]

band-pass (BP), high-pass (HP) and low-pass (LP) filter responses. After performing nodal analysis of this pathological equivalent, the symbolic expressions are given by,

$$\frac{I_{BP}}{I_{in}} = \frac{s\frac{g_1}{C_1}}{s^2 + s\frac{g_1}{C_1} + \frac{g_1 g_2}{C_1 C_2}}, \frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + s\frac{g_1}{C_1} + \frac{g_1 g_2}{C_1 C_2}}, \frac{I_{LP}}{I_{in}} = \frac{\frac{g_1 g_2}{C_1 C_2}}{s^2 + s\frac{g_1}{C_1} + \frac{g_1 g_2}{C_1 C_2}} \quad (3)$$

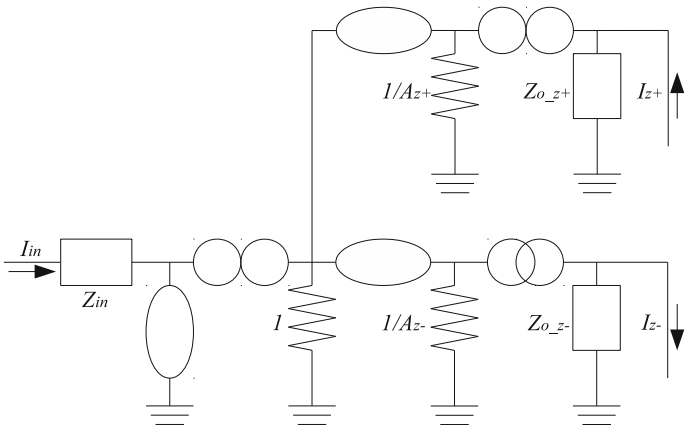

Fig. 9 Two-outputs current mirror modeled by three nullators, two norators and one CM

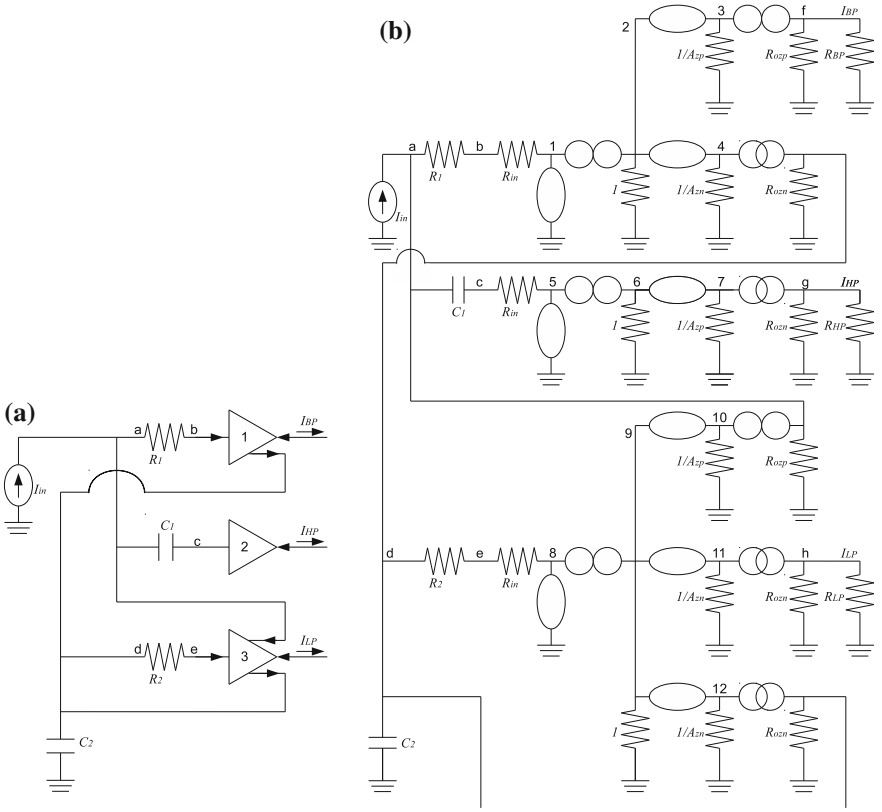

Fig. 10 **a** Current-mode universal filter taken from [33], and **b** its pathological equivalent using the current mirror equivalent shown in Fig. 9

This example highlights the usefulness of using the pathological current mirror element to model active devices with the goal of computing analytical expressions. That way, the main advantage of the derived pathological models relies on the application of symbolic nodal analysis (NA) to formulate smaller matrices compared to traditional modified nodal analysis (MNA) formulation. As pointed out, the pathological equivalents also allow including parasitic elements, so that the derived behavioral models capture the real behavior of the active devices.

3 Adjoint Transformations of Circuits Containing Nullors and Mirrors

Current-mode circuits like the examples given above are quite useful in some analog signal processing applications. However, since the majority of analog integrated circuit designers are quite familiar with voltage-mode circuits, it is quite convenient to know how to convert the voltage-mode designs into their current-mode versions. As highlighted in [26], the main idea is replacing the elements in the voltage-mode circuits by their adjoints, and this task is pretty simple when nullators, norators, CM and VMs, model the voltage-mode circuits. In this manner, this section shows some examples of converting voltage-mode circuits that are modeled by pathological elements, to current-mode ones. The main steps are associated to interchange nullators and voltage mirrors with norators and current mirrors, respectively.

Lets us consider the voltage follower shown on the left of Fig. 11. It consists of a nullator connected between nodes AB and a norator connected between node B and ground. As one sees, the input port drives a voltage input v_{in} connected between node A and ground, while the output is measured at node B with respect to ground. Interchanging the nullator/norator by the norator/nullator but keeping the nodes intact are the main operations to obtain the adjoint equivalent. In this manner, now the norator is connected between nodes AB as shown on the right of Fig. 11, and the nullator is connected between node B and ground. The input/output port from the voltage follower now becomes the output/input port of the current follower, as

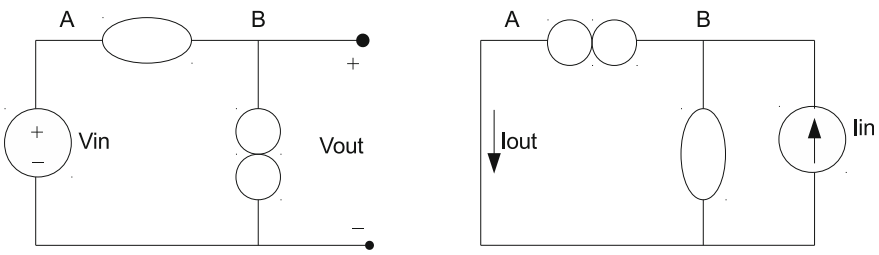

Fig. 11 Transforming a voltage follower into a current follower

highlighted in Fig. 11. It is trivial to obtain the voltage follower from the current follower by performing the same operations on interchanging the nullor/norator by the norator/nullator and converting the input/output port from the current follower to become the output/input port of the voltage follower. In both cases the transfer function equals to 1, i.e. $V_{out}/V_{in} = 1$ and $I_{out}/I_{in} = 1$.

A more elaborated example consists on transforming the OTA-based filter shown in Fig. 12a, which is working in voltage-mode, into its current-mode version. In this case one must set references to the four nullator-norator pairs, and to the input and output ports. Each nullator-norator pair is joined by one of their terminals that are connected to the transconductance g_m. The capacitor practically remains intact and the nullators are interchanged by the norators, the input/output port in Fig. 12a will become the output/input port of the current-mode OTA-based filter in Fig. 12b. By computing the symbolic transfer functions applying the nodal analysis method described in the previous section, both analytical expressions in voltage-mode and current-mode are the same,

$$\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = \frac{g_m}{sC + g_m} \tag{4}$$

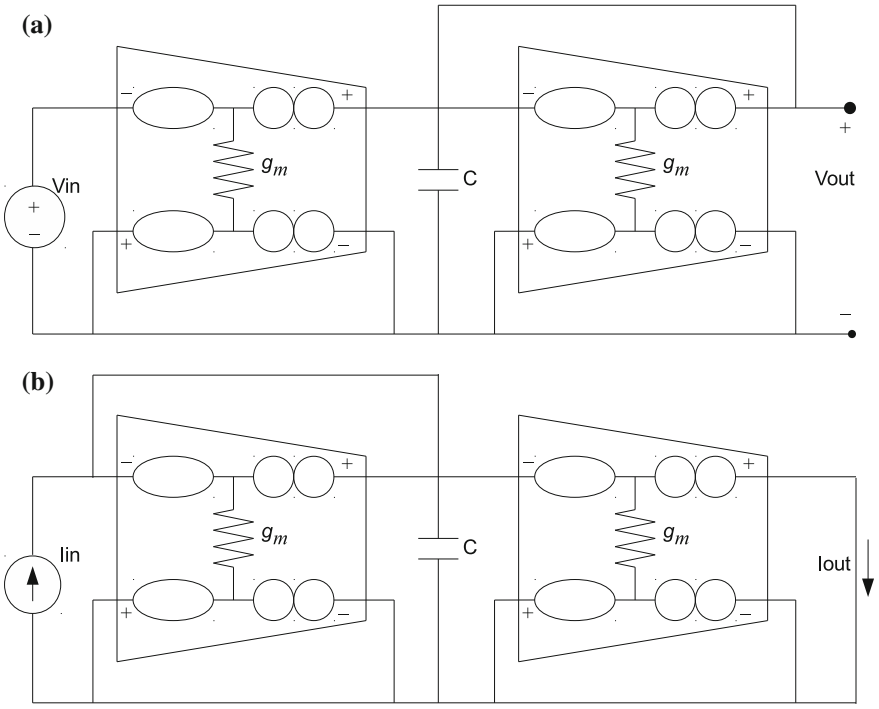

Fig. 12 Transforming the **a** voltage-mode OTA-based filter, into **b** the current-mode one

The same operations apply for VM-CM pairs; they must be interchanged when transforming a voltage-mode circuit into a current-mode one and vice versa. The difficulty arises when either the nullator or norator is associated to a VM or CM, in such a case; one must find the adjoint of each element independently of its associated pair.

4 Synthesis of Nullators, Norators, Voltage Mirrors and Current Mirrors

The singular or pathological elements can be synthesized by transistors if each nullator has its corresponding norator pair as already modeled in Fig. 2a and in Fig. 11, where the voltage follower is modeled by the nullator but a norator is required to fix the output, and where the current follower is modeled by the norator but it needs a nullator to fix the input. For instance, in [34] the nullator is synthesized by MOS transistors when it is modeled as a voltage follower, for which several cases arises because the voltage follower can be modeled by a single, two or four nullators, as shown in Fig. 13, and then each nullator must be accompanied by a norator that can be connected in different ways.

Taking the voltage follower from Fig. 13a, there are several possibilities to add a norator (labeled as P in Fig. 14) to the nullator (labeled as O in Fig. 14), as shown in Fig. 14, the norator can be added to node 1, node 2 or in parallel to the nullator between nodes 1–2. All these nullator-norator (O-P) pairs can be synthesized by the MOS transistor, from Fig. 2a with the resistance equal to zero. Another problem arises when the O-P pairs are in parallel because the source terminal is associated to the node that joints both singular elements, and from Fig. 14c, the source can be associated to node 1 or node 2. All these combinations lead to different topologies, which will require voltage and current biases, as shown in Fig. 15, where one can see some possibilities of adding biases to one O-P pair. Finally, the implementation by using MOS transistors for synthesizing O-P pairs and by using MOS current mirrors to implement the current sources (I_{bias1} and I_{bias2} shown in Fig. 15) is given in Fig. 16, where only three CMOS topologies are shown, and they were synthesized by beginning from Fig. 13a. As one can infer, by beginning the synthesis

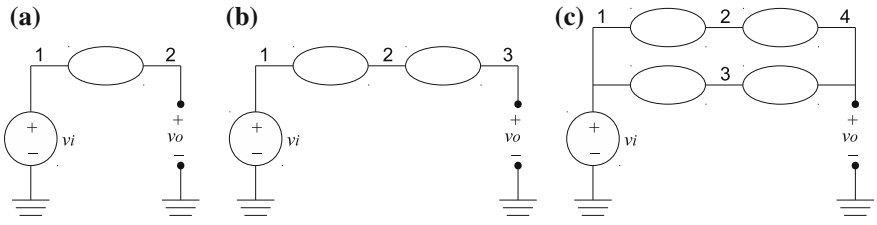

Fig. 13 Nullator equivalents for modeling the voltage follower

process from Fig. 13c, more O-P combinations arises than those shown in Fig. 14, more possibilities of adding voltage and current biases, and more possibilities of synthesizing each O-P pair and current biases by MOS transistors. The authors in [35] improved the work in [34] by applying genetic algorithms to synthesize the voltage follower. Therefore, a chromosome consisting of four genes was proposed, as shown in (5), where the small signal gene (genSS) includes O-P pairs which connections from Fig. 14 can be encoded by two bits (in (5) there are 8 bits associated to the voltage follower modeled by four nullators as in Fig. 13c), the synthesis of each O-P pair can be done by using the P-channel or N-channel MOS transistor, so that one bit is required to encode each O-P pair leading to genSMos. The possibilities of adding current biases can be encoded by two bits for each O-P pair leading to genBias, and finally, the current biases (like I_{bias1} and I_{bias2} shown in Fig. 15) can be synthesized by MOS current mirrors for which many topologies already exist in the literature (for example: simple current mirror, Widlar current mirror, cascode current mirror and so on), in (5) genCM consists of two bits meaning that each current bias can be replaced by any of the four MOS current mirrors. As one can infer, the chromosome in (5) leads us to deal with $8 + 4 + 8 + 2 = 22$ bits that in decimal notation equals to 4,194,304 combinations!, thus this problem is quite suitable for applying metaheuristics.

$$\text{Chromosome}_{VF} = \underbrace{00100010}_{\text{genSS}}\ \underbrace{0011}_{\text{genSMos}}\ \underbrace{10101111}_{\text{genBias}}\ \underbrace{00}_{\text{genCM}} \tag{5}$$

The synthesis of the norator can be associated to the current follower, as the one shown on the right side of Fig. 11. The synthesis process can be performed quite similar as for the synthesis of the nullor but the biases are now majorly voltage sources than current ones, it is an open problem that has been partially solved in [30], where several new topologies synthesized by MOS transistors are provided.

The synthesis of the voltage mirror (VM) can be seen as an extended case of the voltage follower (VF). Lets us consider Fig. 17 that embeds a VF that can be connected in two combinations. Basically, the chromosome in (5) can be

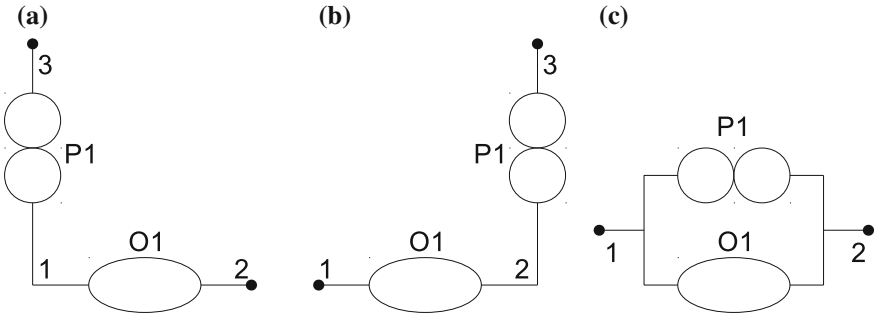

Fig. 14 Adding a norator to the nullator from Fig. 13a

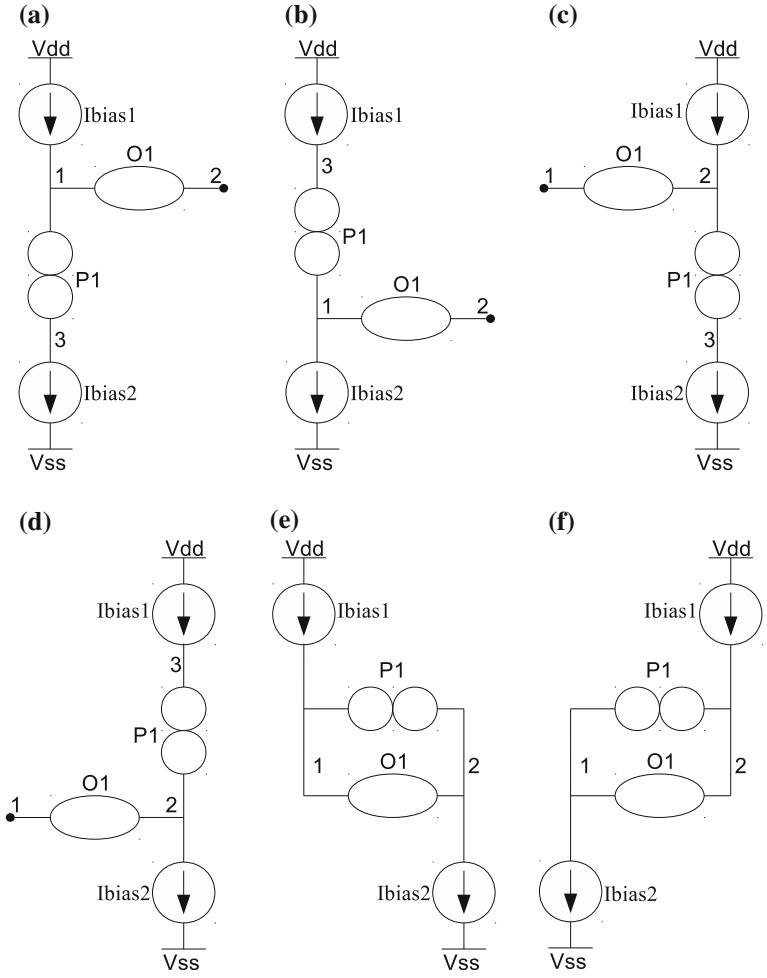

Fig. 15 Adding voltage and current biases to the nullator-norator (O-P) pairs from Fig. 14

augmented by one bit associated to the kind of connection of the output of the VF, e.g. to the P-channel or N-channel MOS transistor. From this reasoning, the synthesis of the VM by MOS transistors can be performed by beginning with the synthesis of the voltage follower (VF) and adding two complementary MOS transistors, as shown in Fig. 17, therefore the chromosome is like in (5) but adding one bit to encode the P-channel (MINV2) or N-channel (MINV1) MOS transistors. The authors in [35] provide details of this synthesis approach.

The synthesis of current mirrors with single or multiple outputs can be associated to the model given in Fig. 9, where it can be appreciated the association of O-P pairs but the pathological CM can be implemented with MOS transistors as already shown in [30], and where one can find new MOS topologies.

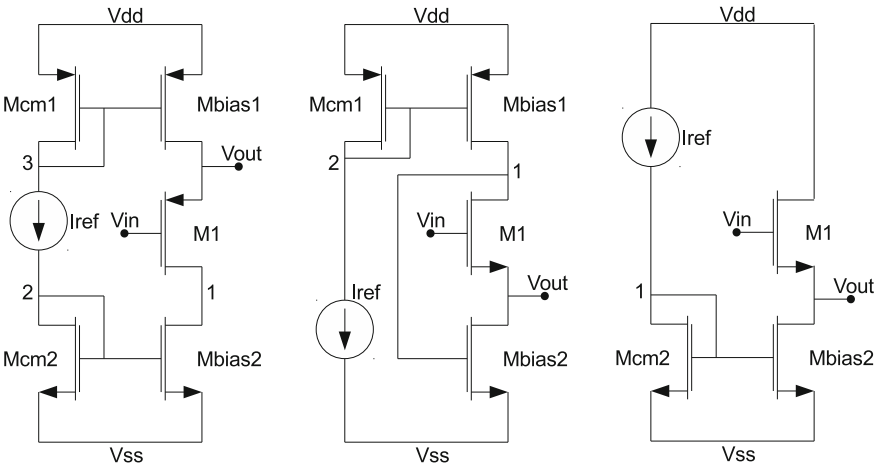

Fig. 16 Three CMOS topologies of the voltage follower synthesized by beginning from Fig. 13a

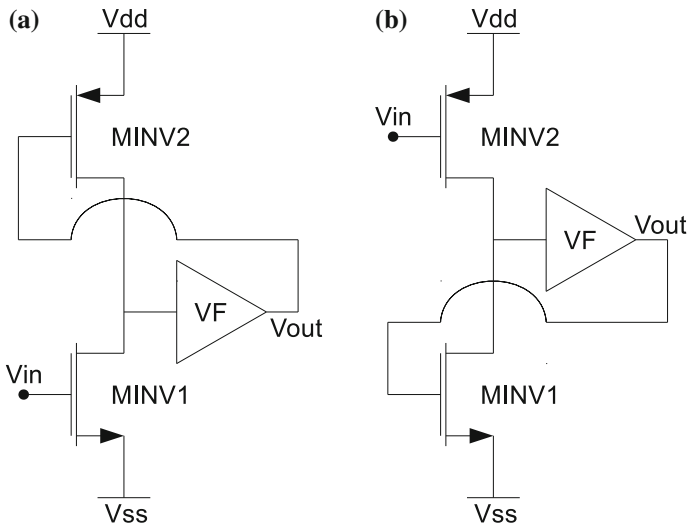

Fig. 17 Synthesis of the voltage mirror (VM) by beginning with the synthesis of the voltage follower (VF) and adding two complementary MOS transistors

5 CMOS Implementation of Unity-Gain-Cells and Mixed-Mode Analog Circuits

This section shows the implementation of synthesized circuits like unity-gain-cells, a current conveyor, a current-feedback operational amplifier, and an operational transconductance amplifier, which are designed with standard CMOS integrated circuit technology, and they are applied to implement active filters and oscillators.

The four unity-gain cells are the voltage follower (VF), current follower (CF), voltage mirror (VM) and current mirror (CM). A well-known VF is shown in Fig. 18, it is synthesized from Fig. 13c: Fig. 18a shows ideal current biases that are synthesized by simple current mirrors in Fig. 18b. Those ideal current biases can also be synthesized by other kinds of current mirrors. The voltage mirror can be synthesized by embedding a VF as shown in Fig. 19a, and the whole CMOS implementation is shown in Fig. 19b.

The current mirror can be implemented as shown in Fig. 20, which is based on the cascode topology. The current mirror is embedded between the input and output ports labeled as i_{in} and $i_{out}+$, respectively. The third column of MOS transistors replicates the current output $i_{out}+$ that is inverted with another current mirror to provide the current-outputs $i_{out}-$ that are associated to a current follower because they go out. In this topology, the input current i_{in} is mirrored by the output $i_{out}+$, and is copied twice by the embedded current followers by the outputs $i_{out}-$.

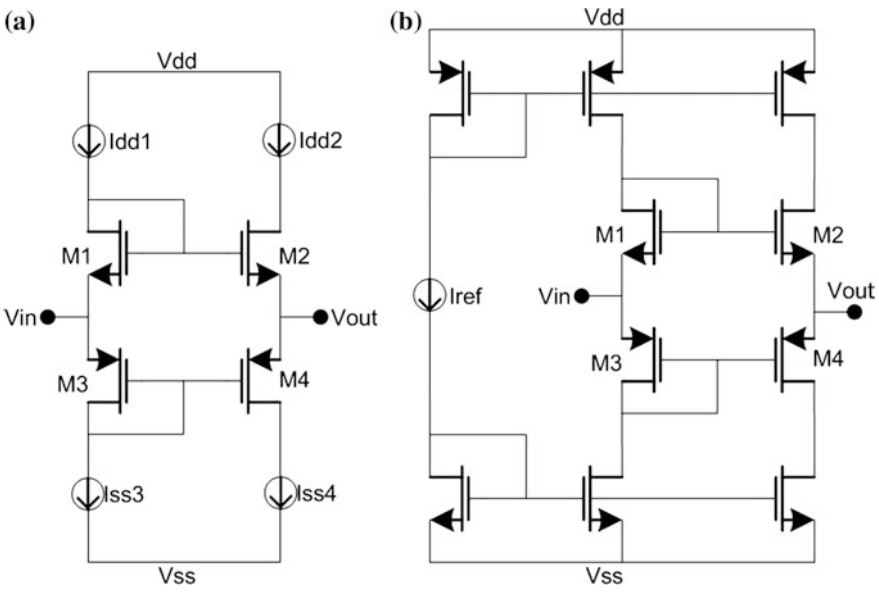

Fig. 18 Voltage follower synthesized from Fig. 13c

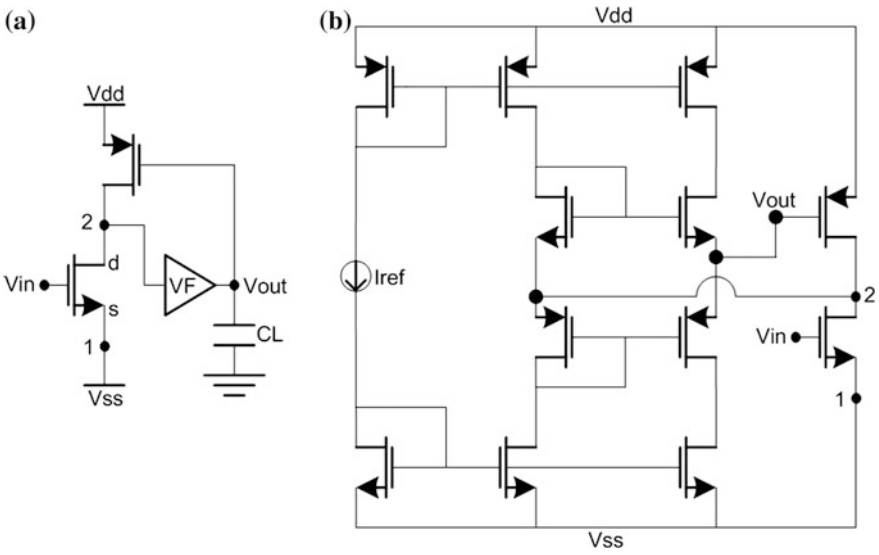

Fig. 19 Voltage mirror consisting of: **a** An inverting topology and a voltage follower (VF), and synthesizing the VF by Fig. 18b

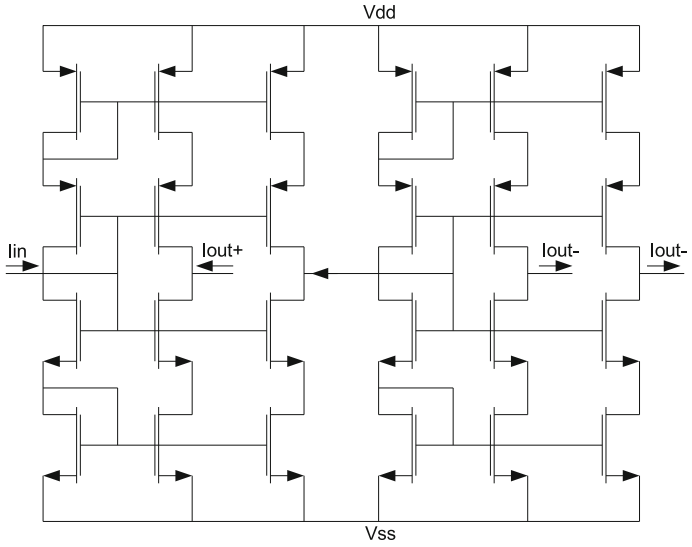

Fig. 20 CMOS implementation of the current follower and current mirror

The four UGCs, namely: VF, VM, CF and CM can be superimposed or interconnected to provide different kinds of amplifiers like current conveyors and current feedback operational amplifiers. For example, Fig. 21f shows the interconnection of a VF with a CM to synthesize a positive-type second-generation current conveyor (CCII+). It can be done by using the VF from Fig. 18a, where: if the current biases are synthesized by simple current mirrors it leads to the VF shown in Fig. 22a, but if the current biases are independently synthesized, e.g. I_{dd1} and I_{ss3} by CMs mirroring the current reference I_{ref} and if I_{dd2} and I_{ss4} are synthesized by cascode CMs providing another port, one gets the CCII+ shown in Fig. 22b. It is easy to see that the ICCII+ can be synthesized by using the VM shown in Fig. 19b. In general, similar interconnections can be performed between two UGCs from Fig. 21 to find novel three terminals amplifiers that work in mixed-mode because they process both voltage and current signals.

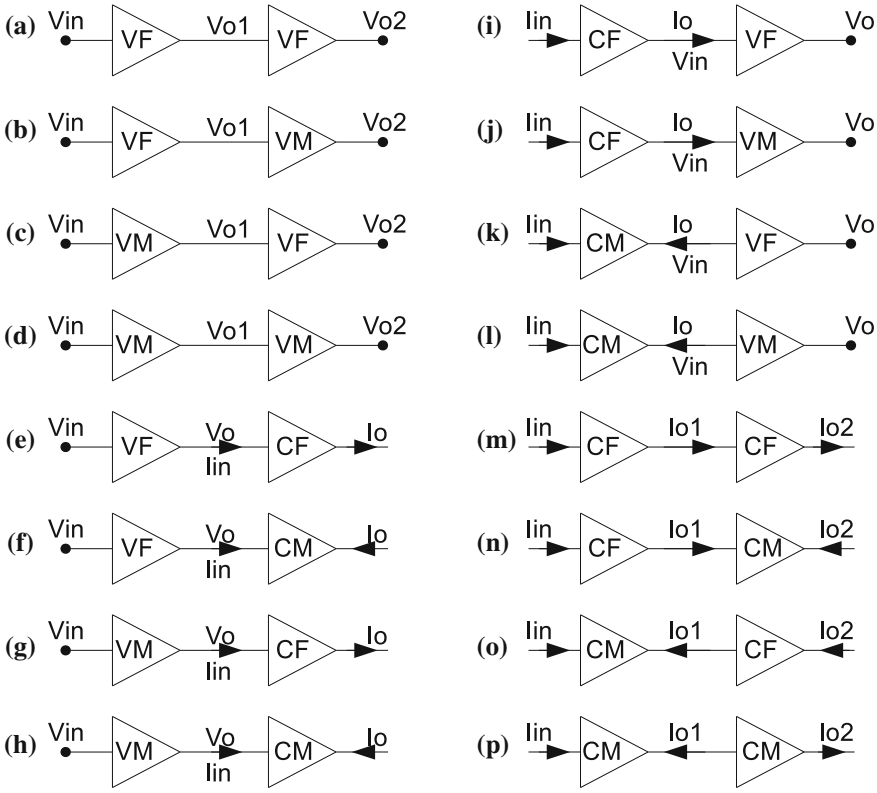

Fig. 21 Examples on interconnecting two UGCs to synthesize three terminals amplifiers

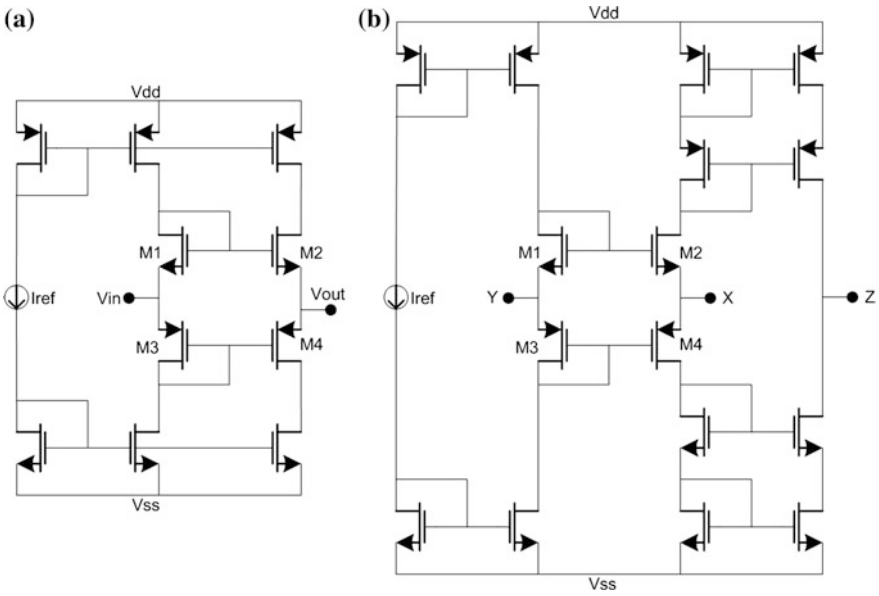

Fig. 22 VF that is superimposed with CMs to synthesize a CCII+

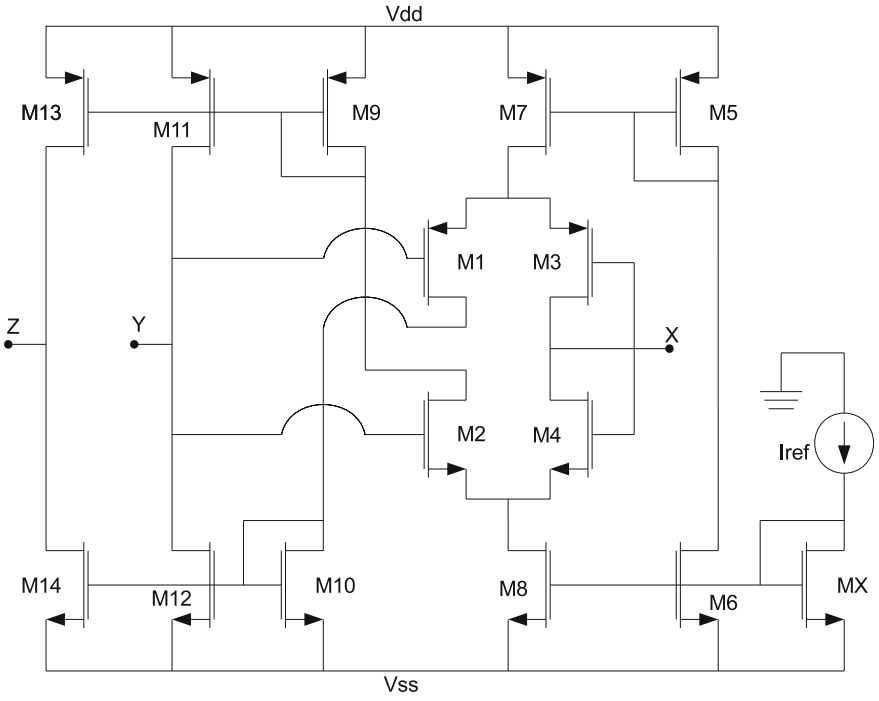

Fig. 23 CCI that is synthesized by a VF and a two-outputs CM, taken from [36]

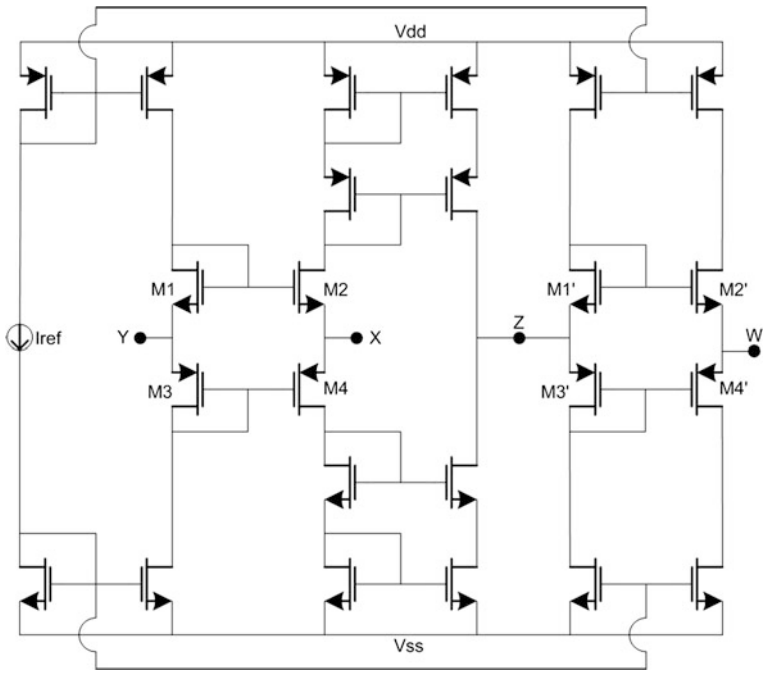

Fig. 24 CCII+ that is connected to another VF to synthesize a CFOA

The UGCs can also provide multiple outputs like the current mirror topologies. They are useful for implementing the first-generation current conveyor (CCI) that must accomplish Vx = Vy, Iy = Ix, and Iz = Ix. From these equations it is easy to see that the currents at ports Y and Z mirror the input current at port X, leading to the CMOS circuit shown in Fig. 23, where the VF is different from the previous circuits and the simple CM provides two outputs. For this and the previous circuits, symbolic analysis can be performed to get insights on their behaviors when synthesizing with different CMOS topologies. For instance, current conveyors present parasitic resistances at their ports that can be minimized by searching for new topologies or by performing circuit optimization [32].

One can also interconnect more than two UGCs, for example: the current-feedback operational amplifier (CFOA) is basically composed of a CM sandwiched by two VFs. Again, by using the VF shown in Fig. 18 and the cascode CM, the resulting CMOS CFOA is shown in Fig. 24, which is also the connection of a CCII+ with a VF. Other VF and CM topologies can also be used to synthesize the CFOA, those topologies will provide different performances that can be compared to choose the most suitable design to accomplish target design specifications.

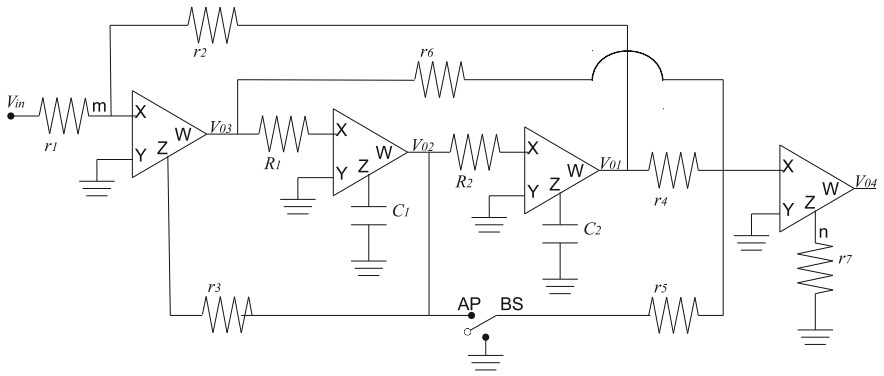

Fig. 25 CFOA-based universal biquadratic filter, taken from [37]

For example, the implementation of the CFOA-based universal mixed-mode filter shown in Fig. 25 requires CFOAs with minimum parasitic impedance at port X and high bandwidth response to improve the design introduced in [37], where the cut-off frequency is low as 100 kHz. Symbolic nodal analysis can be applied to know the effect of the parasitic resistances and capacitances of the CFOA and then to enhance the frequency response of the filter.

The synthesis of the operational transcoductance amplifier (OTA) is more difficult than for mixed-mode circuits by interconnecting UGCs. OTAs are based on a differential pair implemented by two MOSFETs and then more stages are added to increase the gain on the whole amplifier. The gains consist of MOSFETs acting as amplifiers and current mirrors to bias those stages. As the OTA provides current at its output port, then one can use multiple-outputs current mirrors to bias and provide outputs. See for example the OTA designed in [38] and shown in Fig. 26 that has N-channel MOSFETs at its input and simple current mirrors to provide multi-outputs. This OTA has been used in [38] to implement the first-order all-pass filter that consists of two OTAs, one grounded resistor and one grounded capacitor, as shown in Fig. 27. By performing symbolic analysis, the transfer function of this filter is given by (6). Furthermore, this filter can be used to synthesize the current-mode multi-phase sinusoidal oscillator (MSO) shown in Fig. 28, for which the condition of oscillation (CO) and the frequency of oscillation (FO) are given by (7) and (8), respectively, where n is related to the number of stages or first-order all-pass filter sections.

In [38], the sinusoidal outputs provided by the MSO was set up to $n = 5$, and the OTA realization was compared with the one implemented with current-differencing

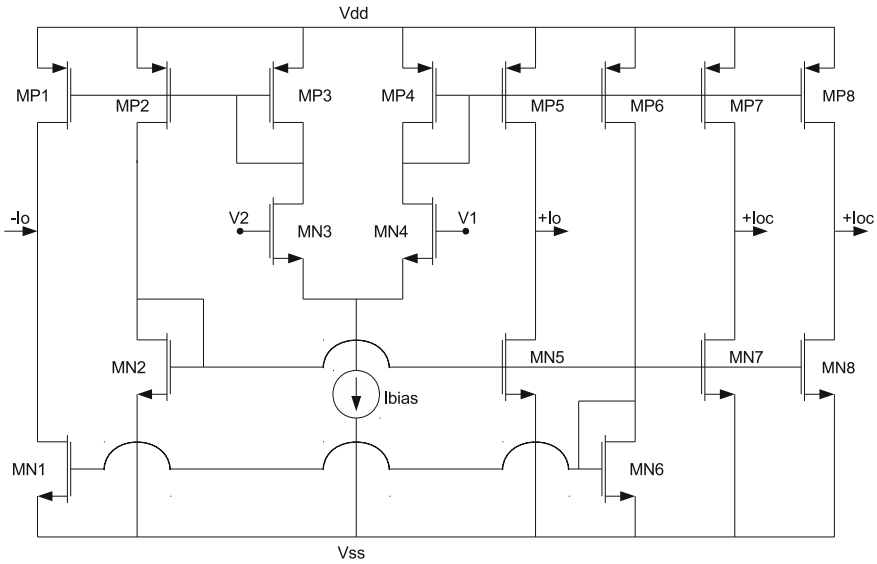

Fig. 26 OTA providing one negative output (−Io), and three positive outputs (+Ioc)

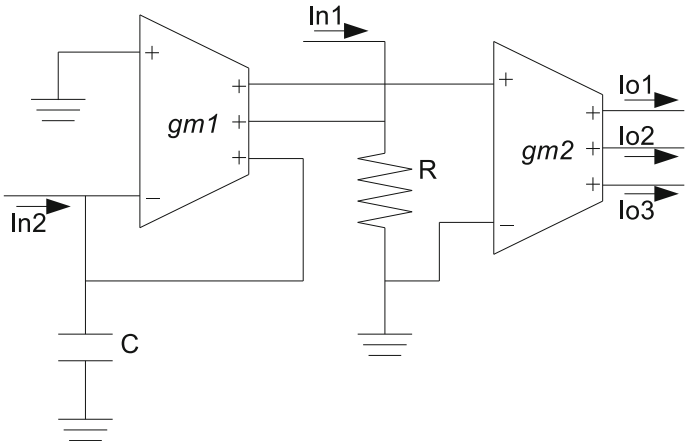

Fig. 27 OTA-based first order all-pass filter

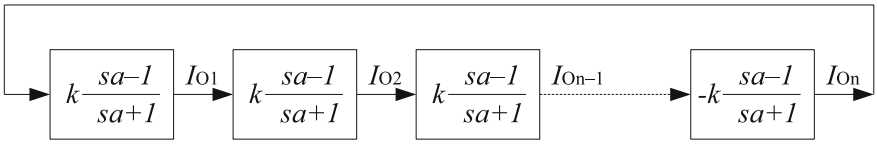

Fig. 28 MSO realized by the cascade connection of first order all-pass filter sections

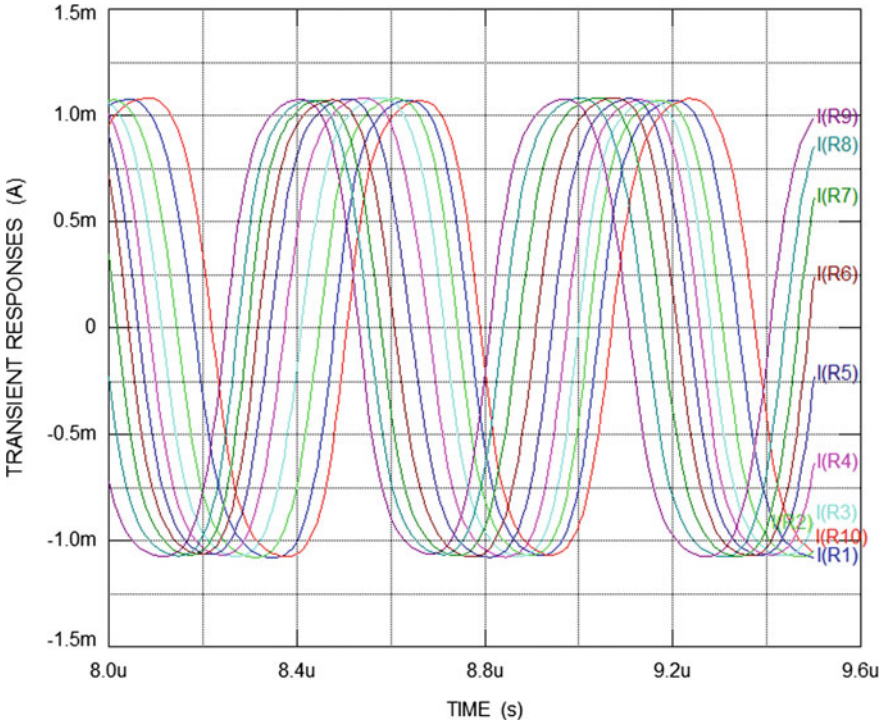

Fig. 29 MSO with $n = 10$ and C = 2 nF to work at FO = 1.71 MHz with g_m = 21.59 I/V

cascaded transconductance amplifiers (CDCTAs), concluding on the suitability of OTAs with multiple-outputs to implement the MSO. In this chapter we show the oscillations with $n = 10$ and $n = 20$ in Figs. 29 and 30, respectively.

$$\frac{I_{01}}{I_{in1}} = g_{m2}R\left(\frac{s\frac{C}{g_{m1}} - 1}{s\frac{C}{g_{m1}} + 1}\right) \tag{6}$$

$$CO : g_{m2}R = 1 \tag{7}$$

$$FO : w_{osc} = \frac{g_{m1}}{c}\tan\left(\frac{\pi}{2n}\right) \tag{8}$$

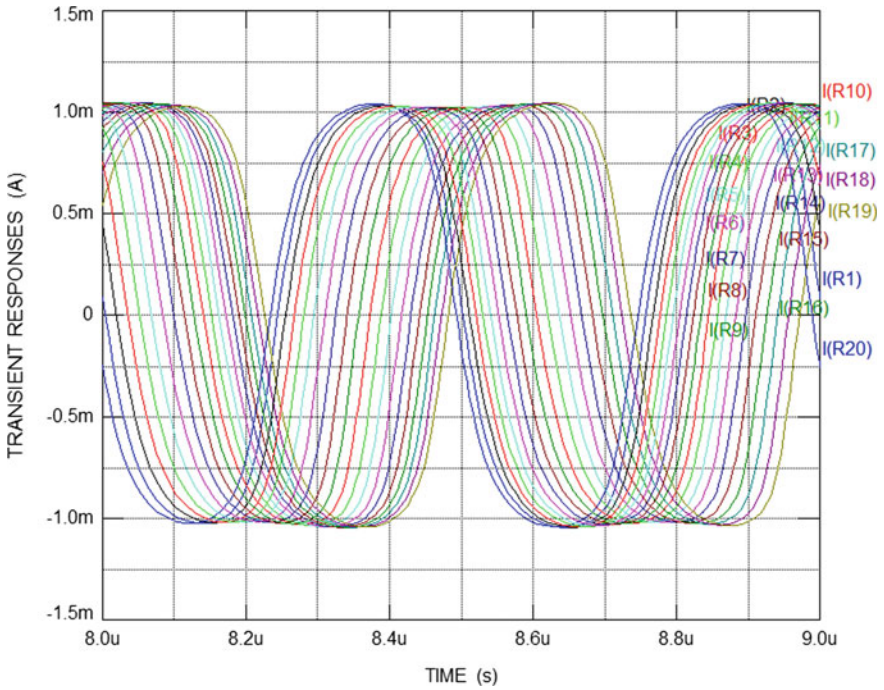

Fig. 30 MSO with $n = 20$ and C = 3.4 nF to work at FO = 2 MHz with $g_m = 86.40$ I/V

6 Conclusions

This chapter discussed the application of symbolic analysis to analog circuits that can be modeled by nullors and pathological current and voltage mirrors. Several related references were provided to highlight that the symbolic analysis of analog circuits modeled by nullors and pathological mirror elements leads us to deal with the nodal admittance (NA) matrix that is more compact than by using traditional modified nodal analysis (MNA).

The second part was devoted to the synthesis of nullor and pathological networks by MOSFETs. It was shown how to synthesize unity-gain cells (UGCs) and mixed-mode amplifiers from nullator, norator and pathological descriptions. Several examples showed that mixed-mode amplifiers can be synthesized from the interconnections of UGCs, and also that operational amplifiers like the OTA can be synthesized by multiple-output current mirrors, differential pairs and so on. Although not shown by examples, a circuit modeled by nullors or pathological elements that is working in voltage-mode can be transformed a current-mode one and vice versa.

The application of UGCs and mixed-mode amplifiers can be found in recent literature. In this chapter the reader can infer that still one can find novel topologies

when synthesizing analog circuits from nullor and pathological element descriptions. In addition, symbolic analysis can be performed to get insights on the behavior of the topologies to mitigate undesired parasitic elements and then to improve their performances.

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Generalized Parameter Extraction Method for Symbolic Analysis of Analog Circuits Containing Pathological Elements

Vladimir Filaretov, Konstantin Gorshkov, Sergey Kurganov and Maxim Nedorezov

Abstract This chapter gives a description of the extension of Generalized Parameter Extraction Method (GPEM) for symbolic analysis of large-scale analog circuits containing pathological elements. The brief overview of the parameter extraction approach is included. An algorithm implementing the concept of Higher Order Summative Cofactors (HOSC) for determinants computation of the pathological element-based circuits is proposed. In this chapter, we also present the hierarchical decomposition techniques of upward and downward analysis of electronic circuits by GPEM. The proposed techniques are used in freeware symbolic analyzer CirSym. Several examples are presented to illustrate the advantages of the GPEM applications.

Related topics of book: Analog circuits, circuit simulation, symbolic analysis of circuits containing pathological elements, controlled sources, nullor, voltage mirrors and current mirrors, symbolic Simulation CAD.

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1 Introduction

Most of the modern symbolic circuit analysis techniques are based on matrix calculus [1–10] or operations with circuit graph [3, 4, 10–15]. However, the usage of matrix representation or graph model may lead to the terms cancellations and produces some pseudo-dependencies in functions. In this chapter, we introduce the basics and advances of circuit analysis by parameter extraction approach which provides the effective symbolic calculation without constructing the circuit equations. Parameter extraction method was developed at the beginning of the XX century by Friedrich Wilhelm Feussner, one of the Kirchhoff's pupils. The formulae presented in [16, 17] provide the calculation of circuit determinant and doesn't need the circuit description as the matrix or topological graph. The determinant of *Z*-circuit (*y*-circuit) is defined by Feussner as the determinant of the corresponding loop impedance (nodal admittance) matrix. The diacoptic formulae for bisection of the circuit by one or two nodes were also proposed in [16] to improve the computational efficiency of parameter extraction method.

The parameter extraction approach was used in the various symbolic analysis techniques [5, 18–26]. Several researches were based on Feussner's publications [19, 23, 25–27]. M. E. Parten and R. H. Seacat proposed the method of network functions calculation of nullor-based circuit by extraction of all elements parameters until the residual circuits that contain only the norators and nullators is derived [23, 25, 26]. However, this method can be used only for active circuits with ideal operational amplifiers. The formula for extraction of controlled sources parameters was proposed by R. Hashemian in [19], but it deals with combinatorial enumeration. The Feussner's diacoptic formulae were used by S. M. Chang and G. M Wierzba for symbolic analysis of networks with nullors. However, the decomposition method proposed in [28, 29] is based on matrix manipulations and suffers from the tedious algorithm of determinant sign calculation. Also, some additional transformations of equivalent circuit are needed to use the bisection formulae in a matrix form.

The advantages of techniques of Feussner and his successors were implemented in GPEM [30–40]. GPEM is an effective tool for symbolic analysis, diagnosis, and synthesis of analog circuits. The parameter extraction cancellation-free method for symbolic analysis of switched capacitor circuits has been developed in [37]. The techniques of computation of the symbolic circuit functions sensitivities in Bode's form and in Hoang's form are described in [36]. The implementation of parameter extraction approach for symbolic circuit analysis by means of the Middlebrook's extra element theorem was proposed in [33]. The symbolic technique for analog fault diagnosis was introduced in [38]. Several GPEM-based circuit synthesis algorithms were developed: (1) an algorithm of automated synthesis of all existing equivalent pathological element-based circuits that correspond to the given polynomial network function [34]; (2) a design algorithm of OTA-based circuits [32]; (3) an algorithm of circuit synthesis using transformation of trees with pathological

elements [39]. Several GPEM-based computer programs for automated circuit analysis and synthesis were developed. The symbolic analyzer CirSym developed by V. Filaretov is available online: http://intersyn.net/en/cirsym.html.

GPEM can be successfully used for symbolic analysis of active circuits with pathological mirror elements. However, the technique proposed in [35] deals with the big amount of special cases of elements connections which complicate the symbolic analysis of large circuits. In this chapter, the new approach to the calculation of pathological element-based circuits by GPEM is presented.

The decomposition procedures can significantly increase the efficiency of symbolic analysis [4, 14, 15, 41–44]. In this chapter, we also present the hierarchical decomposition techniques of upward analysis and downward analysis of large-scale circuits by GPEM.

The chapter comprises three main sections. Section 2 introduces the basics of GPEM. The usage of parameter extraction formulae for circuit determinant expansion is discussed. The rules of degeneracy and simplification of the pathological element-based circuits are considered. Section 3 gives the application of GPEM to the generation of symbolic circuit functions in the case of Single-Input-Single-Output (SISO) and Multiple-Input-Single-Output (MISO) circuits. In Sect. 4 the extension of the method of residual circuits [23] by usage of GPEM and the concept of HOSC [22, 45] is presented. Section 5 focuses on hierarchical decomposition approaches to circuit analysis. The techniques of upward analysis and downward analysis by GPEM are proposed. The illustrative examples of usage of GPEM and its applications are included in this chapter. Conclusions summarize the results of the chapter.

2 The Basics of GPEM

2.1 *Feussner's Formulae for Determinant Expansion of the Passive Circuit*

Classic Feussner's formulae for extraction of impedance or admittance parameters are presented below [16, 17]:

$$\Delta = Z\Delta(Z \to \infty) + \Delta(Z = 0), \tag{1}$$

$$\Delta = y\Delta(y \to \infty) + \Delta(y = 0), \tag{2}$$

where Δ is a circuit determinant; $\Delta(z \to \infty)$ and $\Delta(y = 0)$ are the determinants of subcircuits in which extracted element is deleted; $\Delta(y \to \infty)$ and $\Delta(z = 0)$ are the determinants of subcircuits in which extracted element is short-circuited.

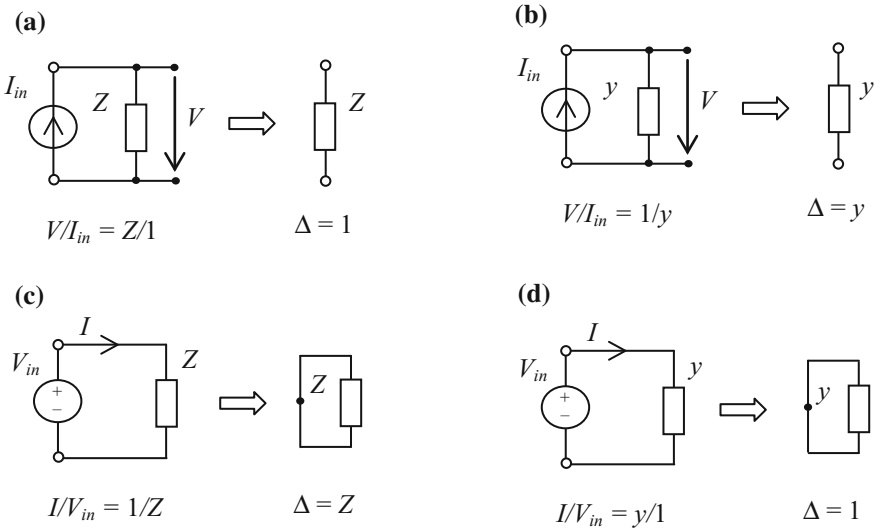
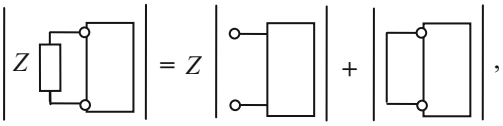


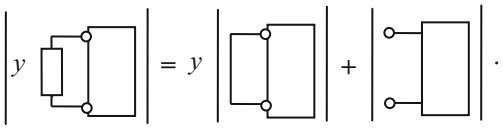
Fig. 1 The residual circuits and their determinants

Recursive usage of the formulae (1) and (2) provides the reduction of an initial circuit to several residual topologies shown in Fig. 1 which determinants can be calculated by Ohm's Law. GPEM using the complex impedance of the inductors and the complex admittance of capacitors in the Laplace domain: $Z_L = sL$ and $y_c = sC$ correspondingly.

The circuit-algebraic expressions that contain the parameters symbols, mathematical signs and derived subexpressions in the form of subcircuits, can be useful for illustration of the process of determinant expansion by parameters extraction [28]. For example, the Feussner's formulae can be expressed in the circuit-algebraic form as following:



(3)



(4)

The diacoptic approach to circuit analysis was discussed by Feussner long before the publications of G. Kron [46]. He proposed the technique of circuit decomposition

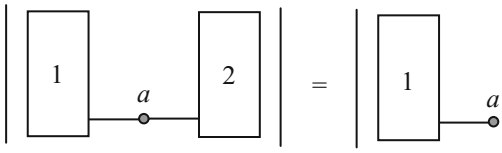
(bisection) based on following formulae for bisection of the circuit by one or two nodes correspondingly:

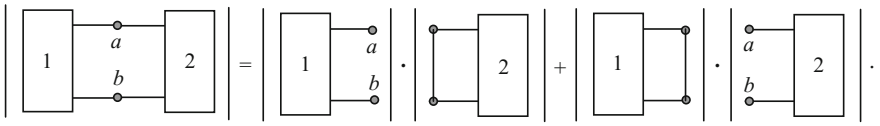
$$\Delta = \Delta_1 \Delta_2 \tag{5}$$

$$\Delta = \Delta_1 \Delta_2(a,b) + \Delta_1(a,b)\Delta_2, \tag{6}$$

where Δ_1 and Δ_2 are determinants of the first and second subcircuits in which the node a in (5) and nodes a and b in (6) are opened, $\Delta_1(a,b)$ and $\Delta_2(a,b)$ are determinants of subcircuits in which the nodes a and b are shorted.

In the circuit-algebraic form the bisection formulae by one or two nodes are shown below correspondingly:

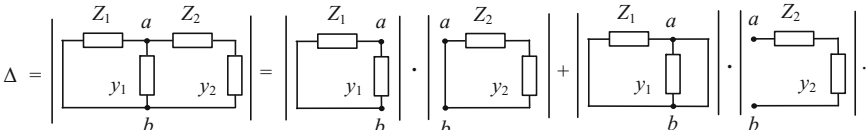




(8)

Example 1 Let's consider the determinant calculation procedure in the case of the simple two-section *LC*-ladder circuit shown in Fig. 2 to illustrate the usage of Feussner's formulae.

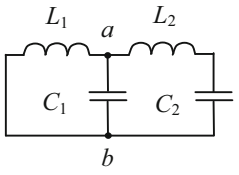
The bisection of the ladder by two nodes a and b by usage of (6) leads to the following circuit algebraic expression:

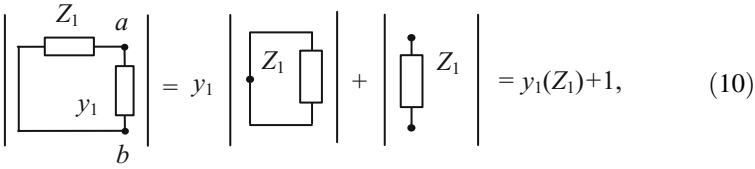


(9)

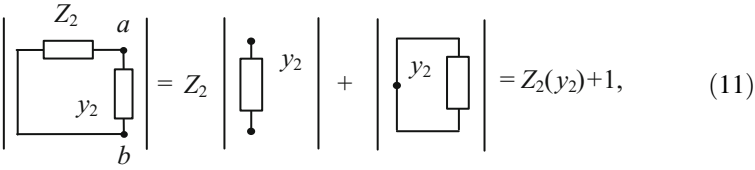
The parameter extraction procedures for determinants calculation of four subcircuits in (9) are shown below:

Fig. 2 *LC*-ladder circuit

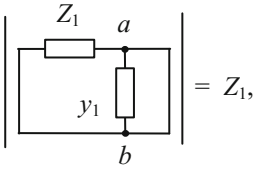




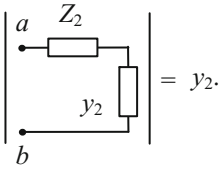
(10)



(11)



(12)



(13)

The result of the substitution of (10)–(13) into (9) can be expressed as:

$$\Delta = (y_1(Z_1) + 1)(Z_2(y_2) + 1) + Z_1 y_2. \tag{14}$$

The Feussner's formulae provide quite efficient symbolic determinant calculation of passive circuit. M. E. Parten and R. H. Seacat implemented (1) and (2) to the analysis of nullor-based circuits by extraction of all elements parameters until the residual circuits which contain only the norators and nullators [23]. The well-known equivalent transformations of parallel or series connection of norator and nullator were used for determinants computation of residual nullor circuits. However, this method can be used only for active circuits with ideal operational amplifiers. The new formula for extraction of parameters of controlled sources (CS) was needed to extend the Feussner's approach.

2.2 Extraction of Controlled Sources Parameters

The formula for the extraction of CS parameter was proposed by R. Hashemian in 1977 [19]:

$$\Delta = \chi\Delta(\chi \to \text{nullor}) + \Delta(\chi = 0), \tag{15}$$

where χ is a parameter of arbitrary CS, $\Delta(\chi \to$ nullor) is a determinant of the circuit in which a CS element is replaced by nullor, $\Delta(\chi = 0)$ is a determinant of the circuit in which the parameter of CS is equal to zero.

Hashemian has used formula (15) for simultaneous expansion of determinant by parameters of all n CS which circuit contains. Such technique leads to the enumeration of 2^n summands and cannot provides the generation of expression in the compact size.

The formula (15) was developed by V. Filaretov in 1998 irrespective of Hashemian's publication [19]. The recursive extraction of CS parameters by (15) was proposed. Also instead of original Carlin's nullor shown in Fig. 3a [47] the concept of oriented nullor, introduced in network theory by A.G. Davies [48] and J. Braun [49], is used in GPEM. The orientation of nullor provides simpler computation of the determinant expression sign of the residual nullor-based circuit as shown in Fig. 4a and b.

The oriented nullor is successfully used for calculation of network functions [49], as well as for active devices simulation [35]. For example, the equivalent circuits of voltage mirror (VM) and current mirror (CM) in which $g = 1$ are shown in Fig. 3c and Fig. 3d correspondingly. The pathological mirrors are useful ideal circuit elements for modeling active devices with voltage and current reversing [2, 7–9, 50–53].

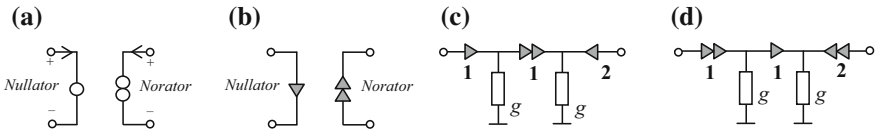


Fig. 3 Nullor symbol **a**, oriented nullor symbol **b**, the equivalent nullor circuits of pathological mirrors: VM **c** and CM **d**

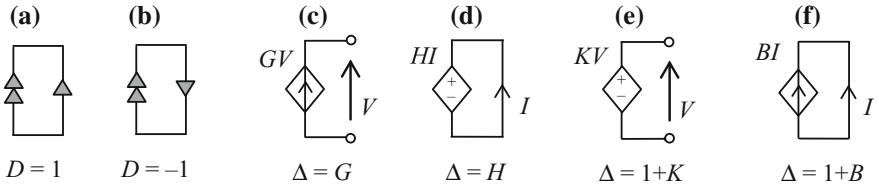
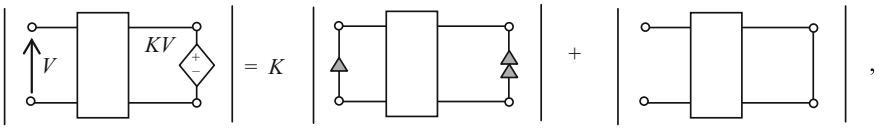


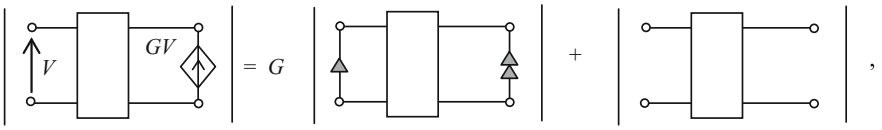
Fig. 4 The residual circuits consists of nullor **a**–**b**, controlled sources **c**–**f**

The subcircuits may include more than one oriented nullor. There are several simple rules that can help to deal with such cases: (1) enumerate the nullator-norator pairs; (2) invert the sign of determinant in the case of inversion of the norator or nullator orientation; (3) invert the sign of determinant in the case of the pair numbers interchanging between two norators or two nullators.

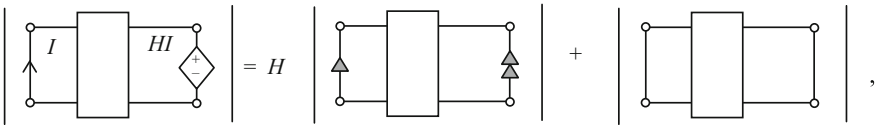
The circuit-algebraic expressions for the parameter extraction cases for each of the four depended sources, using formula (15), are shown below:



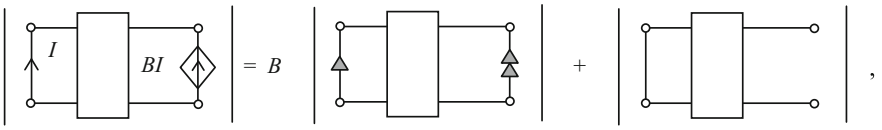
(16)



(17)



(18)



(19)

where K is a control parameter of voltage controlled voltage source (VCVS), G is a control parameter of voltage controlled current sources (VCCS), H is a control parameter of current controlled voltage source (CCVS) and B is a control parameter of current controlled current source (CCCS).

The determinant of the circuit with pathological elements can be equal to zero [28, 29, 54, 55]. Such circuits are called the degenerated circuits. The check for the degeneracy of subcircuits derived by usage of formulae (1), (2), (5), (6) and (15) is very important part of the process of symbolic analysis by GPEM.

Table 1 The circuit elements in short-circuit and in open loop

Element type	Special connection case	
	Element shorted	Element opened
Impedance	Parameter extracted – element deleted	Element shorted
Admittance	Element deleted	Parameter extracted – element shorted
Voltage source	$\Delta = 0$	Element shorted
Controlling current of CS	$\Delta = 0$	Element shorted
Current source	Element deleted	$\Delta = 0$
Controlling voltage of CS	Element deleted	$\Delta = 0$
Nullator	$\Delta = 0$	$\Delta = 0$
Norator	$\Delta = 0$	$\Delta = 0$
VM	$\Delta = 2$	$\Delta = 0$
CM	$\Delta = 2$	$\Delta = 0$

2.3 *Degeneracy and Simplification of Circuits Containing Pathological Elements*

Although topological conditions of circuit degeneracy were introduced for the first time in the mid-1970s [54, 55] the degeneracy check still can be confusing for circuit designers in the certain cases [56]. Therefore in GPEM, the generalized topological conditions are used. The determinant of circuit is equal to zero in following cases: (1) the circuit consists of several not connected subcircuits; (2) the circuit contains at least one loop consisting only of voltage sources and norators or controlling currents of CS and nullators; (3) the circuit contains at least one cross-section consisting only of the current sources and norators or controlling voltages of CS and nullators. Note that the voltage sources and current sources mentioned in topological conditions can be the input sources or depended sources as well.

The determinant of the circuit consisting only of nullors is nonzero if there is a tree which includes all of the norators while the collection of remaining branches (nullators) is the complement of such a tree and vice versa.

The degenerated circuits cannot be equivalent to each other because responses of the signal in such circuits are indeterminate. Therefore the equivalent transformation of the parallel connection of voltage source and norator into voltage source as shown in [53, 56], the transformation of the series connection of the current source and norator into current source as shown in [56], and the short-circuiting of the current source and nullator connected in series as shown in [53], are not correct.

In Tables 1 and 2 we present the special cases of elements connections derived by usage of parameter extraction formulae and topological conditions which considered above.

Table 2 The equivalent transformations of circuits containing pathological elements

	Special Case							
	In parallel with				In series with			
Element type	Norator	Nullator	VM	CM	Norator	Nullator	VM	CM
Impedance	Parameter extracted – element deleted		——	——	Element shorted			
Admittance	Element deleted		——	——	Parameter extracted – element shorted			
Voltage source	$\Delta = 0$	Nullor	——	——	Element shorted	——	——	Element shorted
Controlling current of CS	Nullor	$\Delta = 0$	——	——	——	Element shorted	Element shorted	——
Current source	Element deleted	——	——	——	$\Delta = 0$	Nullor	——	$\Delta = 0$
Controlling voltage of CS	——	Element deleted	——	——	Nullor	$\Delta = 0$	——	$\Delta = 0$
Norator	$\Delta = 0$	Nullor shorted	——	——	$\Delta = 0$	Nullor deleted	Elements deleted	$\Delta = 0$
Nullator	Nullor shorted	$\Delta = 0$	——	——	Nullor deleted	$\Delta = 0$	$\Delta = 0$	Elements deleted
VM	——	$\Delta = 2$	$\Delta = 0$	Elements shorted	Elements deleted	$\Delta = 0$	$\Delta = 0$	Elements deleted
CM	$\Delta = 2$	——	Elements shorted	$\Delta = 0$	$\Delta = 0$	Elements deleted	Elements deleted	$\Delta = 0$

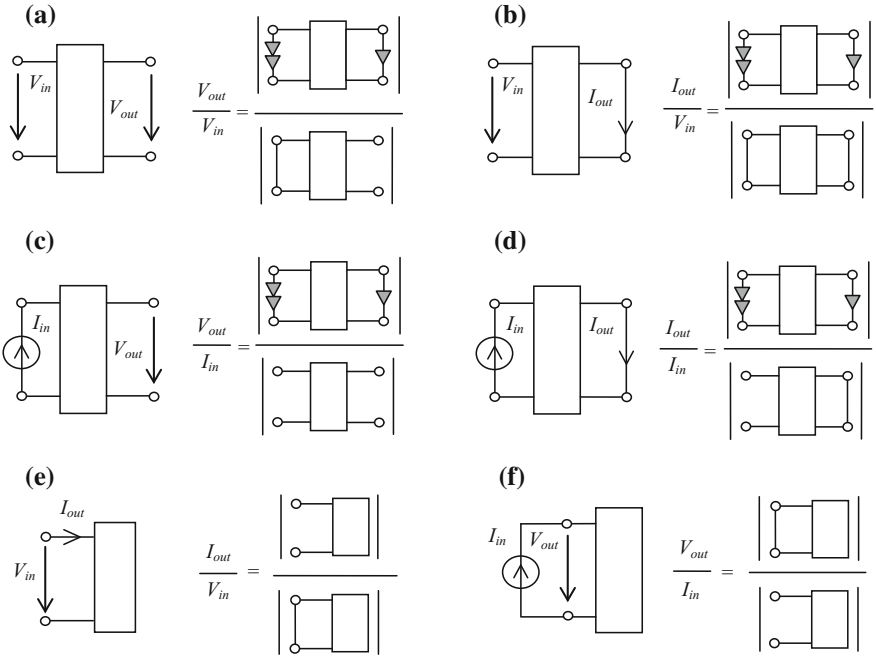


Fig. 5 The circuit-algebraic expressions of the circuit functions

3 Symbolic Circuit Analysis by GPEM

3.1 Symbolic Analysis of SISO Circuits

The network function of a linear circuit can be expressed as a ratio of two rational symbolic expressions. The numerator is the determinant of the circuit, in which the input source and response are replaced by an oriented norator and nullator correspondingly [49]. The denominator is the determinant of the circuit, in which the input and output signals are equal to zero.

The circuit-algebraic expressions for the circuit functions calculation are shown in the Fig. 5. For determinants calculation of network that contains any linear models of active circuit elements, including the controlled sources and pathological elements, the parameter extraction formulae (1), (2), (15) and bisection formulae (5)–(6) are recursively used. Each of the derived subcircuits must be checked by topological conditions for the solvability and degeneracy. As result, the residual circuits presented in Fig. 1 and Fig. 4 is obtained.

The order of parameter extraction can be chosen arbitrarily. So the calculated determinant can be presented as the rational polynomial expression if the reactive elements is extracted first.

The GPEM-based symbolic analyzer CirSym is developed by V. Filaretov. The program is freeware available in two versions: offline and online http://intersyn.net/en/cirsym.html. The input data is a slightly modified Spice-compatible netlist, which can be entered online or loaded as a cir-file. Circuit nodes should be numbered as integers. The passive impedance and admittance elements are identified by uppercase and lowercase characters correspondingly: R, L, C and g, l, c. Controlled sources are identified by following symbols: K is a parameter of VCVS, G is a parameter of VCCS, H is a parameter of CCVS and B is a parameter of CCCS. Pathological elements are identified as follows: N is a nullor, M is a VM-CM pair, T is a CM-nullator pair and Q is a norator-VM pair. Note that the input voltage source should be defined as EMF source and described by symbol E. CirSym-online provides the calculation of several circuits at once. The end of the netlist for each circuit and the end of the whole of input data are notified by strings « .end » and « .total » correspondingly.

Example 2 Let's consider the simple high-pass filter circuit containing the non-ideal OpAmp that modeled by VCVS as shown in Fig. 6. For the sake of clarity, we calculate the numerator and denominator of voltage transfer function separately.

Numerator calculation. The parameter sC_1 can be extracted from the numerator subcircuit in accordance with Table 2 due to the series connection of admittance and norator:

$$\Delta_3 = \left| \begin{array}{ccc} & g_2 & \\ sC_1 & & K_1V_1 \\ & g_1 & \end{array} \right| = sC_1 \left| \begin{array}{ccc} & g_2 & \\ sC_2 & & K_1V_1 \\ & g_1 & \end{array} \right| . \tag{20}$$

Parallel connection of voltage source of VCVS also provides simplified extraction of parameter K_1. There are two nullors in the circuit now and they must be enumerated. The interchanging of numbers between two norators leads to inversion of expression sign and provides the usage of the equivalent transformation of nullor as shown in Fig. 4a. The admittance g_2 is deleted in accordance with Table 2. The sign of determinant is changed again in the consequence of the equivalent transformation of norator and nullator which are labeled by « 2 » in accordance with Fig. 4b.

$$\Delta_3 = s^2C_1C_2K_1 \left| \begin{array}{ccc} & g_2 & \\ \mathbf{2} & & \mathbf{2} \\ \mathbf{1} & & \mathbf{1} \end{array} \right| = -s^2C_1C_2K_1 \left| \begin{array}{ccc} & & \\ g_2 & \mathbf{2} & \\ & & \mathbf{2} \end{array} \right| = s^2C_1C_2K_1. \tag{21}$$

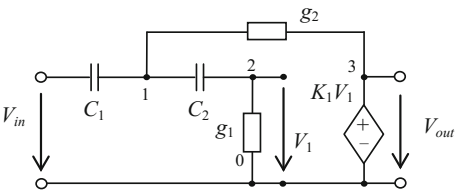
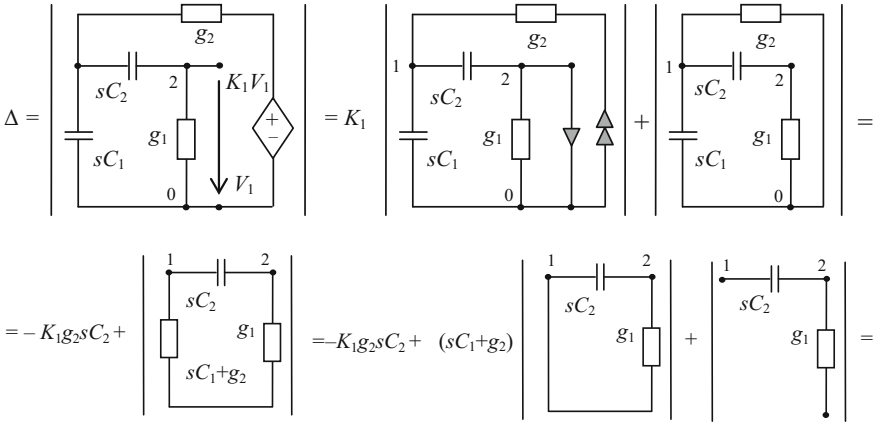


Fig. 6 VSSC-based equivalent circuit of high-pass filter

Denominator calculation. Two subcircuits that correspond to the determinants $\Delta(K_1 \rightarrow \text{nullor})$ and $\Delta(K_1 = 0)$ is derived as result of the VCVS parameter extraction by formula (15). The first subcircuit can be easily reduced to expression $-K_1 g_2 sC_2$ by usage of Tables 1 and 2. Note that the negative sign is the consequence of orientation of norator and nullator as shown in Fig. 4b. The second subcircuit can be expanded by extraction of the multibranch parameter $(sC_1 + g_2)$.



(22)

The resulting transfer function can be expressed as follows:

$$H = \frac{\Delta_3}{\Delta} = \frac{s^2 C_1 C_2 K_1}{-K_1 g_2 sC_2 + (sC_1 + g_2)(sC_2 + g_1) + sC_2 g_1}. \tag{23}$$

3.2 Symbolic Circuit Analysis of MISO Circuits

The nullator controlled multidimensional source [31] can be used for calculation of response function V_{out} of arbitrary MISO circuit that consists of n voltage sources and m current sources as shown in Fig. 7a. In that case, all of the input sources is transformed into controlled sources which will be oriented opposite [18]. All of the sources is controlled by the same nullator as shown in Fig. 7b. Parameters of input

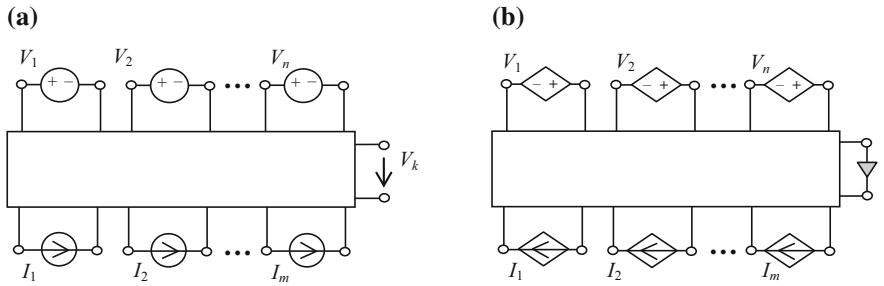


Fig. 7 The circuit with n input voltage sources and m input current sources **a**, circuit with nullator controlled multidimensional source **b**

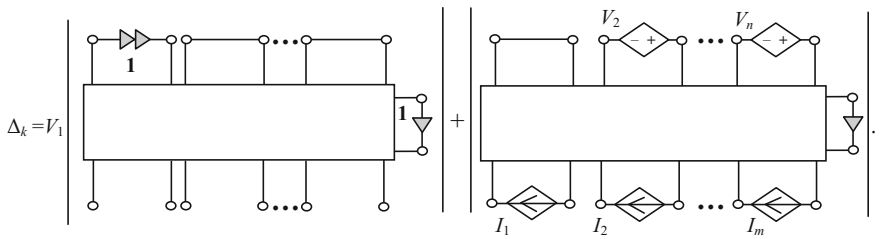
sources V_1, V_2, …, V_n and I_1, I_2, …, I_n is used as parameters of the nullator controlled multidimensional source. The properties of a nullator of a multidimensional source are the same as the properties of a standard nullator. Thus, all known operations with nullators are still valid. Obviously, the network can include only one nullator controlled multidimensional source.

The following recursive formula was proposed in [31] to calculate the numerator of k-th voltage or current function of MISO circuit:

$$\Delta_k = p_i \Delta_1 + \Delta_2. \tag{24}$$

where p_i is a source parameter V_i or I_i, Δ_1 is the determinant of network in which the source with parameter p_i corresponding to V_i or I_i is replaced by a norator, the nullator of the multidimensional source is replaced by a standard nullator, and parameters of all other sources are equal to zero; Δ_2 is the determinant of network in which the parameter of extracted source is equal to zero. Note that Δ_2 is equal to zero if all $m + n$ parameters of sources have been extracted.

Let's use the formula (15) to extract parameter V_1 in numerator circuit which is presented in Fig. 7b. As result we obtained the circuit-algebraic expression that shown below:



(25)

As can be seen from (25), the extracted voltage source in the first subcircuit is transformed into norator while parameters of others sources are equal to null. Therefore the first subcircuit contains only one nullor and can be calculated by

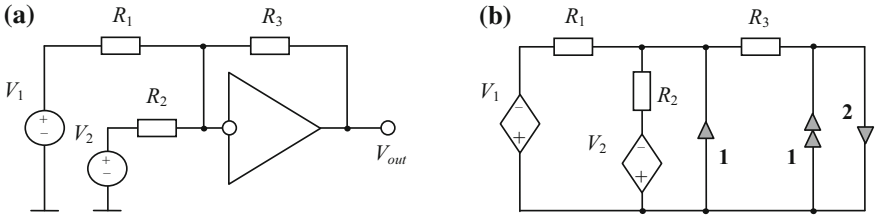
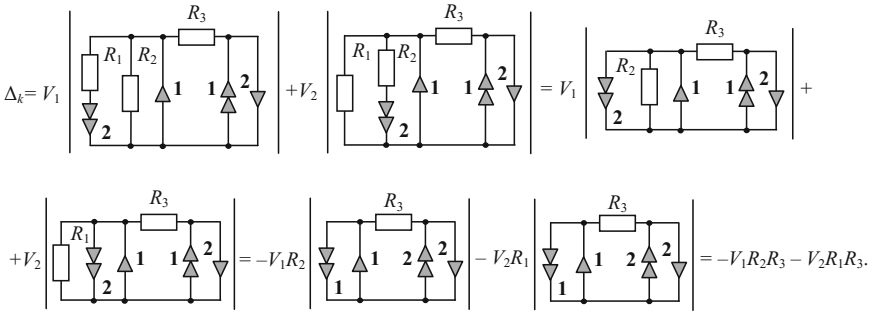


Fig. 8 **a** The summing amplifier circuit, **b** equivalent circuit with nullator controlled multidimensional source

formulae (1), (2), (15). Others sources parameters can be extracted from the second subcircuit in a similar way.

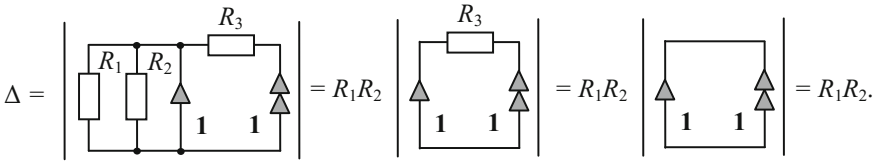
Example 3 The usage of the concept of nullator controlled multidimensional source can be explained by means of the symbolic analysis example of the summing amplifier circuit with $V_{out} = \Delta_{\underline{k}}/\Delta$ shown in Fig. 8a.

Numerator calculation. The equivalent circuit shown in Fig. 8b is used for calculation of voltage function numerator $\Delta_{\underline{k}}$ by formula (24). There are two nullor-based subcircuits as result of the extraction of parameters V_1 and V_2. The determinant expressions can be easily derived by using simplification conditions in Table 2 as follows:



(26)

Denominator calculation. The voltages of both sources V_1 and V_2 are equal to null. There is only one regular nullor in the subcircuit. The determinant expansion by using Table 2 is trivial:



(27)

4 The Technique of Determinant Expansion of Pathological Element-Based Residual Circuits

As seen from examples in previous subsections, the usage of formulae (1), (2), (5), (6) and (15) along with the conditions of circuit degradation and simplification from Tables 1 and 2 is easy, intuitive and effective especially in the case of relatively small circuits. However, the big amount of special connections of elements complicates the symbolic analysis of large subcircuits that contain only of pathological elements which are the result of extraction of all impedances, admittances, and CS. A more simple technique of determinants computation of the pathological element-based residual circuits is needed.

4.1 Expansion of Determinants of Pathological Element-Based Residual Circuits

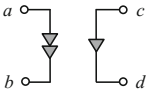
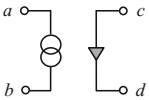
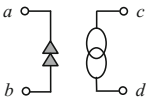
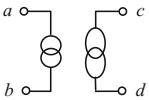
The main idea of the new approach is that the determinant of the residual circuit, which contains only the pathological elements, can be calculated by usage of matrix algebra operations instead of simplification by conditions presented in Tables 1 and 2. The connection of norator or nullator (VM or CM) to the circuit leads to the summation (subtraction) of rows or columns in circuit the admittance matrix. The rows or columns numbers correspond to the nodes numbers of the circuit. The concept of HOSC [22, 45] can be useful to represent the matrices in such operations.

The higher order cofactor is a cofactor of a cofactor. The n-th order cofactor can be identified by a symbol $\Delta_{r1,k1,r2,k2,\ldots rn,\ kn}$, where r_1, r_2, …, r_n and k_1, k_2,…, k_n are the numbers of deleted rows and columns respectively. If at least one deletion in the higher order cofactor has a summative form, then cofactor is called a higher order summative cofactor.

For example, the first-order HOSC can be described as $\Delta_{(a\pm b)(c\pm d)}$, where a and b are the numbers of rows, c and d are the numbers of columns. In the case of summation of numbers $(a + b)$ or $(c + d)$ the row a is added to row b or the column c is added to column d. In the case of subtraction of numbers $(a–b)$ or $(c–d)$ the entries of the row a or the column c is inverted before addition to the row b or to the column d correspondingly. Note, that the added row a or column c is deleted from the matrix. The following notation $\Delta_{(a+0)(c+0)}$, where zero is the number of grounded node in the circuit, means the deletion operation of the row a and column c. Obviously, $\Delta_{(a-0)(c-0)} = \Delta_{(a+0)(c+0)}$.

The matrices of pathological elements are presented in Table 3, where N is a symbol of the norator-nullator pair, Q is a symbol of the VM-norator pair, T is a symbol of the nullator-CM pair, M is a symbol of the VM-CM pair. If one of the matrix entries is null the determinant of pathological element matrix is equal to zero. In Table 3 the matrix identities for all four pathological elements in the form

Table 3 The equivalent HOSC and matrices of pathological elements

	Element type	Matrix identity in form of HOSC	Matrix elements
1	*N* (norator-nullator pair) 	$\Delta_{(a+b)(c+d)} = \Delta_{(a+0)(c+0)} + \Delta_{(b+0)(d+0)} - \Delta_{(a+0)(d+0)} - \Delta_{(b+0)(c+0)}$	| | **c** | **d** | |---|---|---| | **a** | *N* | *–N* | | **b** | *–N* | *N* |
2	*T* (nullator-CM pair) 	$\Delta_{(a-b)(c+d)} = \Delta_{(a+0)(c+0)} - \Delta_{(b+0)(d+0)} - \Delta_{(a+0)(d+0)} + \Delta_{(b+0)(c+0)}$	| | **c** | **d** | |---|---|---| | **a** | *T* | *–T* | | **b** | *T* | *–T* |
3	*Q* (VM-norator pair) 	$\Delta_{(a+b)(c-d)} = \Delta_{(a+0)(c+0)} - \Delta_{(b+0)(d+0)} + \Delta_{(a+0)(d+0)} - \Delta_{(b+0)(c+0)}$	| | **c** | **d** | |---|---|---| | **a** | *Q* | *Q* | | **b** | *–Q* | *–Q* |
4	*M* (VM-CM pair) 	$\Delta_{(a-b)(c-d)} = \Delta_{(a+0)(c+0)} + \Delta_{(b+0)(d+0)} + \Delta_{(a+0)(d+0)} + \Delta_{(b+0)(c+0)}$	| | **c** | **d** | |---|---|---| | **a** | *M* | *M* | | **b** | *M* | *M* |

of HOSC are proposed. To prove the matrix identities presented in Table 3 one can apply the Laplace's cofactor expansion.

Matrix representation of pathological elements provides the way to reduce the matrix of the residual circuit by extraction of virtual parameters that are equal in absolute values:

$$\Delta = \begin{cases} X \cdot \Delta_{(a\pm b)(c\pm d)}, & a = c \\ -X \cdot \Delta_{(a\pm b)(c\pm d)}, & a \neq c \end{cases}, \tag{28}$$

where X is a symbol of pathological element written at the intersection of rows a and b and columns c and d of the circuit matrix, $\Delta_{(a\pm b)(c\pm d)}$ is the circuit matrix transformed in accordance with Table 3.

The recursive usage of the formula (28) provides the calculation of determinant of the matrix of the residual circuit. The determinant of the non-degenerated nullor-based residual circuit can take on values $\Delta = 1$ or $\Delta = -1$. The determinant value of non-degenerated residual circuit containing pathological mirrors can be multiple of 2.

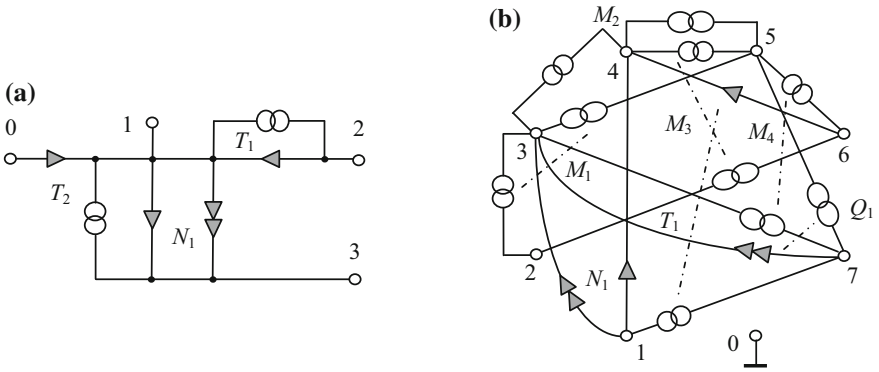


Fig. 9 The pathologic element-based residual circuits

Example 4 Suppose that the pathologic element-based circuit shown in Fig. 9a is a residual circuit of a certain network in which all of the impedances, admittances, and CS were extracted.

The HOSC list and its representation in the form of circuit matrix can be expressed as follows:

$$\Delta_{(1-2)(2+1),(1-3)(0+1),(1+3)(1+3),} \tag{29}$$

	1	2	3
1	$-T_1-T_2+N_1$	T_1	$-N_1$
2	$-T_1$	T_1	
3	$-T_2-N_1$		N_1

(30)

Let's extract T_1 from the matrix by formula (28). The symbol of the first nullator-CM pair is deleted as shown below:

	1	2	3
1	$-T_2+N_1$		$-N_1$
2			
3	$-T_2-N_1$		N_1

(31)

The subtraction of entries at rows 1 and 2 leads to inversion of the entries of row 1:

	1	2	3
2	T_2-N_1		N_1
3	$-T_2-N_1$		N_1

(32)

The result of the addition of entries in columns 2 and 1 is shown below:

	1	3
2	T_2-N_1	N_1
3	$-T_2-N_1$	N_1

(33)

Now let's rearrange the numbers of columns and rows as follows:

	2	3
2	T_2–N_1	N_1
3	$-T_2$–N_1	N_1

(34)

The number of the row a is not equal to the number of the column c ($1 \neq 2$), so in accordance with (28):

	2	3
2	$-T_2$+N_1	$-N_1$
3	T_2+N_1	$-N_1$

(35)

As seen from (35), the types of non-extracted pathological elements is changed as following $T_2 \rightarrow N_2$ and $N_1 \rightarrow T_3$:

	2	3
2	N_2+T_3	$-T_3$
3	$-N_2$+T_3	$-T_3$

(36)

Now let's extract the symbol of nullor N_2:

	2	3
2	T_3	$-T_3$
3	T_3	$-T_3$

(37)

The result of the addition of the entries in rows 2 and 3 is shown below:

	2	3
3	$2T_3$	$-2T_3$

(38)

The last step is the addition of columns 0 and 2 which leads to deletion of column 2:

	3
3	$-2T_3$

(39)

The value of the determinant is $\Delta = -2$.

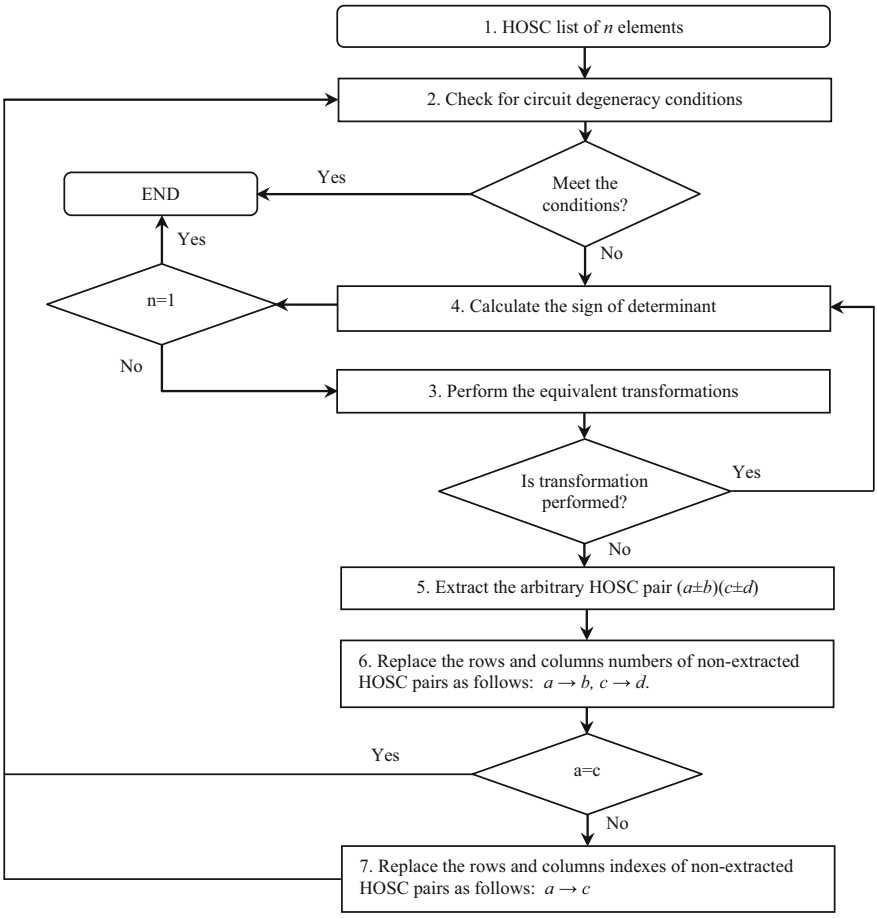


Fig. 10 The flow chart of algorithm

4.2 *The Algorithm of Determinant Expansion Directly from HOSC of Residual Circuits*

The HOCS pairs $(a \pm b)(c \pm d)$ can be extracted instead of the pathological elements symbols. The determinant expansion of residual circuits directly from HOSC is more appropriate for automatic calculation. The algorithm proposed is shown in Fig. 10. The input data is the HOSC list of a certain circuit in which all of the elements except the pathological mirrors and nullors were extracted by formulae (1), (2) and (15).

The individual aspects of analysis stages are detailed below:

1. The netlist of the residual circuit is transformed into the HOSC list.

2. At the beginning of computation process and after every extraction iteration the HOSC list must be checked for circuit degeneracy conditions. If the HOSC list includes more than one element then determinant is equal to zero in following cases:

$$(\mathrm{a}+\mathrm{a}) \rightarrow \Delta = 0; \tag{40}$$

$$(\mathrm{c}+\mathrm{c}) \rightarrow \Delta = 0. \tag{41}$$

If the HOSC list includes only one element that differs from $\Delta_{(a+b)(a+b)} = 1$ and $\Delta_{(a+b)(b+a)} = -1$, then determinant is equal to zero. For example: $\Delta_{(a+b)(c+d)} = 0$.

3. Several equivalent transformations must be performed in the HOSC list:

I. Determinant doubling (2Δ):

$$(\mathrm{a}-\mathrm{a}) \rightarrow (\mathrm{a}+0), \tag{42}$$

$$(\mathrm{c}-\mathrm{c}) \rightarrow (\mathrm{c}+0). \tag{43}$$

II. The transformations of the HOSC list elements with null summand:

$$(\mathrm{a}-0) \rightarrow (\mathrm{a}+0); \tag{44}$$

$$(\mathrm{c}-0) \rightarrow (\mathrm{c}+0); \tag{45}$$

$$(0-\mathrm{a}) \rightarrow (\mathrm{a}+0); \tag{46}$$

$$(0+\mathrm{a}) \rightarrow -(\mathrm{a}+0); \tag{47}$$

$$(0-\mathrm{c}) \rightarrow (\mathrm{c}+0); \tag{48}$$

$$(0+\mathrm{c}) \rightarrow -(\mathrm{c}+0). \tag{49}$$

III. The transformations of the HOSC list elements with the first negative number:

$$((-a)+b) \rightarrow -(b+(-a)) \rightarrow -(b-a) \rightarrow -(a-b), \tag{50}$$

$$((-a)-b) \rightarrow (b-(-a)) \rightarrow (b+a) \rightarrow -(a+b), \tag{51}$$

$$((-c)+d) \rightarrow -(d+(-c)) \rightarrow -(d-c) \rightarrow -(c-d), \tag{52}$$

$$((-c)-d) \rightarrow (d-(-c)) \rightarrow (d+c) \rightarrow -(c+d). \tag{53}$$

4. The default positive sign of determinant must be inverted in the case of transformations (47), (49), (50)–(53) or extraction of the HOCS pair $(a + b)$ $(c + d)$ in which $a \neq c$ (see step 7).

Table 4 The expansion of HOSC list (29)

Operation		HOSC list	Determinant
1	Extraction of (1, 2)(2 + 1)	$\Delta_{(1-3)(0+1),(1+3)(1+3)}$	Δ
2	Rows: 1 → –2; Col.: 2 → 1	$\Delta_{(-2-3)(0+1),(-2+3)(1+3)}$	
3	Rows and Col.:1 → 2	$\Delta_{(-2-3)(0+2),(-2+3)(2+3)}$	
4	Changing sign 1 ≠ 2	$\Delta_{(-2-3)(0+2),(-2+3)(2+3)}$	–Δ
5	Transformation by (51)	$\Delta_{(2+3)(0+2),(-2+3)(2+3)}$	Δ
6	Transformation by (50)	$\Delta_{(2+3)(0+2),(2,3)(2+3)}$	–Δ
7	Transformation by (49)	$\Delta_{(2+3)(2+0),(2,3)(2+3)}$	Δ
8	Extraction of (2 + 3)(2 + 0)	$\Delta_{(2,3)(2+3)}$	Δ
9	Rows: 2 → 3; Col.: 2 → 0	$\Delta_{(3)(0+3)}$	
10	Saving sign 2 = 2	$\Delta_{(3)(0+3)}$	Δ
11	Doubling by (42)	$\Delta_{(3+0)(0+3)}$	2Δ
12	Transformation by (49)	$\Delta_{(3+0)(3+0)}$	–2Δ
Result			**–2Δ**

5. The extraction of arbitrary HOSC pair $(a + b)(c + d)$ decreases HOSC list by one.
6. After extraction of HOCS pair $(a \pm b)(c \pm d)$ the numbers of rows of non-extracted HOSC pairs will be replaced as follow: $a \rightarrow b$. The numbers of columns is replaced in a similar way: $c \rightarrow d$. If $a = c$ the analysis procedure repeats from degeneracy checking. In the opposite case, the next step must be performed.
7. If $a \neq c$ the rows and columns numbers of non-extracted HOSC pairs is replaced as follows: $a \rightarrow c$. This operation is inverting of the sign of the determinant.

The algorithm of calculation of determinant of the residual circuit consisting of pathological elements only is implemented in circuit analyzer CirSym.

Example 5 The sequence of operations of determinant calculation of the pathologic element-based residual circuit which is shown in Fig. 9a is presented in Table 4 in accordance with the algorithm proposed.

As can be seen, the result of calculation by the expansion of HOSC list is the same as result of matrix expansion in Example 4.

Example 6 Suppose that pathologic element-based circuit shown in Fig. 9b is a residual circuit of a certain active network in which all of the impedances, admittances, and CS were extracted. The HOSC list of pathological elements is written below in the following order: N_1, M_1, M_2, M_3, M_4, Q_1, T_1.

Table 5 The expansion of HOSC list (54)

Operation		HOSC list	Determinant
1	Extraction of (1 + 3)(1 + 4)	$\Delta_{(2-3)(3-5),(3-4)(4-5),(4-5)(2-6),(5-6)(3-7),(7+3)(5-7),(7-1)(6+4)}$	Δ
2	Rows: 1 → 3; Col.: 1 → 4	$\Delta_{(2-3)(3-5),(3-4)(4-5),(4-5)(2-6),(5-6)(3-7),(7+3)(5-7),(7-3)(6+4)}$	
3	Extraction of (2, 3)(3–5)	$\Delta_{(3-4)(4-5),(4-5)(2-6),(5-6)(3-7),(7+3)(5-7),(7-3)(6+4)}$	
4	Rows: 2 → –3; Col.: 3 → –5	$\Delta_{(3-4)(4-5),(4-5)(2-6),(5-6)(-5-7),(7+3)(5-7),(7-3)(6+4)}$	$-\Delta$
5	Changing sign 2 ≠ 3		
6	Rows and Col.:2 → 3	$\Delta_{(3-4)(4-5),(4-5)(3-6),(5-6)(-5-7),(7+3)(5-7),(7-3)(6+4)}$	
7	Transformation by (53)	$\Delta_{(3-4)(4-5),(4-5)(3-6),(5-6)(5+7),(7+3)(5-7),(7-3)(6+4)}$	Δ
8	Extraction of (3, 4)(4, 5)	$\Delta_{(4-5)(3-6),(5-6)(5+7),(7-4)(5-7),(7+4)(6-5)}$	
9	Rows: 3 → –4; Col.: 4 → –5	$\Delta_{(4-5)(3-6),(5-6)(5+7),(7-4)(5-7),(7+4)(6-5)}$	$-\Delta$
10	Changing sign 3 ≠ 4		
11	Rows and Col.:3 → 4	$\Delta_{(4-5)(4-6),(5-6)(5+7),(7-4)(5-7),(7+4)(6-5)}$	
12	Extraction of (4, 5)(4–6)	$\Delta_{(5-6)(5+7),(7-4)(5-7),(7+4)(6-5)}$	
13	Rows: 4 → –5; Col.: 4 → –6	$\Delta_{(5-6)(5+7),(7+5)(5-7),(7-5)(6-5)}$	
14	Extraction of (5, 6)(5 + 7)	$\Delta_{(7+5)(5-7),(7-5)(6-5)}$	
15	Rows: 5 → –6; Col.: 5 → 7	$\Delta_{(7-6)(7-7),(7+6)(6-7)}$	
16	Doubling by (43)	$\Delta_{(7-6)(7+0),(7+6)(6-7)}$	-2Δ
17	Extraction of (7–6)(7 + 0)	$\Delta_{(7-6)(7+0),(7+6)(6-7)}$	
18	Rows: 7 → –6; Col.: 7 → 0	$\Delta_{(-6+6)(6-0)}$	
19	Transformation by (50)	$\Delta_{(6-6)(6-0)}$	2Δ
20	Doubling by (42)	$\Delta_{(6+0)(6-0)}$	4Δ
21	Transformation by (45)	$\Delta_{(6+0)(6+0)}$	
Result			**4Δ**

$$\Delta_{(1+3)(1+4),(2-3)(3-5),(3-4)(4-5),(4-5)(2-6),(5-6)(3-7),(7+3)(5-7),(7-1)(6+4)}. \quad (54)$$

The sequence of operations of determinant calculation is presented in Table 5.

The obtained results of examples which considered above are confirmed by usage of CirSym.

5 Circuit Decomposition in GPEM

There are two hierarchical decomposition approaches to circuit analysis. The first one is called upward analysis and it is based on the combination of subcircuits [44]. The downward analysis deals with recursive usage of circuit bisection. Both of decomposition approaches are implemented in GPEM. The upward analysis provides the generation of circuit function in the form of sequence of expressions (SoE). Many symbolic circuit analysis techniques provide the solution in the form of SoE [1, 5, 6, 44, 57–59] and the sequence can be made very compact [59]. The single nested expression of circuit function can be obtained by downward analysis.

5.1 The Downward Analysis

In this section, we present the generalized topological approach to circuit bisection which can be explained by matrix decomposition procedures. Let's consider the arbitrary fully populated matrices **A**, **B**, and **C = A+B** of the same order $n = 3$. The determinant of **C** can be expressed as shown below:

$$\det(\mathbf{C}) = \begin{vmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{vmatrix} = \begin{vmatrix} a_{11}+b_{11} & a_{12}+b_{12} & a_{13}+b_{13} \\ a_{21}+b_{21} & a_{22}+b_{22} & a_{23}+b_{23} \\ a_{31}+b_{31} & a_{32}+b_{32} & a_{33}+b_{33} \end{vmatrix}. \quad (55)$$

The expression (55) can be transformed in consequence of linearity of the determinant as follows:

$$\begin{aligned} \det(\mathbf{C}) = &\begin{vmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{vmatrix} + \begin{vmatrix} a_{11} & a_{12} & b_{13} \\ a_{21} & a_{22} & b_{23} \\ a_{31} & a_{32} & b_{33} \end{vmatrix} + \begin{vmatrix} a_{11} & b_{12} & a_{13} \\ a_{21} & b_{22} & a_{23} \\ a_{31} & b_{32} & a_{33} \end{vmatrix} + \begin{vmatrix} b_{11} & a_{12} & a_{13} \\ b_{21} & a_{22} & a_{23} \\ b_{31} & a_{32} & a_{33} \end{vmatrix} + \\ + &\begin{vmatrix} a_{11} & b_{12} & b_{13} \\ a_{21} & b_{22} & b_{23} \\ a_{31} & b_{32} & b_{33} \end{vmatrix} + \begin{vmatrix} b_{11} & a_{12} & b_{13} \\ b_{21} & a_{22} & b_{23} \\ b_{31} & a_{32} & b_{33} \end{vmatrix} + \begin{vmatrix} b_{11} & b_{12} & a_{13} \\ b_{21} & b_{22} & a_{23} \\ b_{31} & b_{32} & a_{33} \end{vmatrix} + \begin{vmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \end{vmatrix}, \end{aligned} \quad (56)$$

or more briefly as

$$\det(\mathbf{C}) = \det(\mathbf{A}+\mathbf{B}) = \det\mathbf{A} + \sum\Delta(1) + \sum\Delta(2) + \ldots + \sum\Delta(k) + \ldots + \sum\Delta(n-1) + \det\mathbf{B}, \quad (57)$$

where $\Delta(k)$ is the determinant derived by operation of replacement of all the entries of k columns of matrix $\mathbf{A}$ by the entries of corresponding columns of matrix $\mathbf{B}$. The sum in (57) is the sum over all possible combinations of k columns in $\mathbf{A}$ and $\mathbf{B}$.

In accordance with Laplace theorem if we are given a selection of k rows i_1, i_2, …, i_k of a square n-order matrix $\mathbf{M}$ the determinant can be characterized as the sum [60]:

$$\Delta = (-1)^{\sum_{z=0}^{k} i_z + \sum_{z=0}^{k} j_z} M_{j_1,j_2,\ldots,j_k}^{i_1,i_2,\ldots,i_k} \overline{M}_{j_1,j_2,\ldots,j_k}^{i_1,i_2,\ldots,i_k}, \quad (58)$$

where $j_1, j_2, \ldots, j_k$ specify the columns of $\mathbf{M}$, $\overline{M}_{j_1,j_2,\ldots,j_k}^{i_1,i_2,\ldots,i_k}$ is the complementary minor of the minor $M_{j_1,j_2,\ldots,j_k}^{i_1,i_2,\ldots,i_k}$. Note that the columns vary over all possible combinations of k columns.

The Eq. (57) can be expressed by usage of (58) as following [61]:

$$\det(\mathbf{C}) = \det(\mathbf{A}+\mathbf{B}) = \det\mathbf{A} + \sum_{k=1}^{n-1} \sum (-1)^{\sum_{z=0}^{k} i_z + \sum_{z=0}^{k} j_z} B_k \overline{A_k} + \det\mathbf{B}, \quad (59)$$

where B_k is the minor of order k of matrix $\mathbf{B}$, $\overline{A_k}$ is the complementary minor of (n–k) order formed by the determinant of the matrix $\mathbf{A}$ from which k rows and columns associated with minor B_k have been removed.

The expression (59) seems not quite effective for determinant expansion of the fully populated matrix. But the circuit matrix usually is sparse. Thereby the formula (59) can be quite useful for the symbolic circuit analysis by hierarchical decomposition. Let's consider the graphical models of arbitrary circuit matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C} = \mathbf{A}+\mathbf{B}$ of the same order n which are presented in Fig. 11. The parameters of circuits' elements are written in the entries in the shaded areas of matrices $\mathbf{A}$ and $\mathbf{B}$. The values of the entries in the non-shaded areas are equal to null. The intersection of the rows and columns, which corresponds to the common nodes of

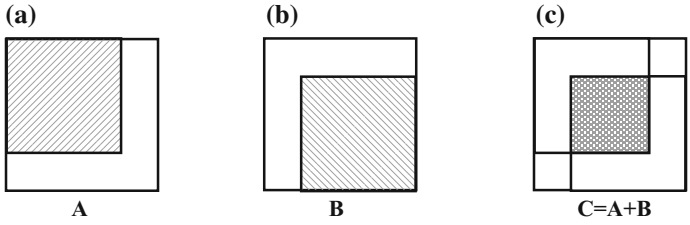


Fig. 11 The graphical models of arbitrary circuit matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C} = \mathbf{A}+\mathbf{B}$

circuits is shown as the double-shaded area in matrix **C**. Suppose that the set of common nodes includes the grounded node. Thereby for determinant calculation of circuit matrix **C** by (59), we can use only the minors and cofactors that correspond to the common nodes of subcircuits. The other minors and cofactors are equal to zero.

The Feussner's diacoptic formulae (5) and (6) represent the particular cases of circuit bisection. The operation of short-circuiting of the nodes a and b in bisection formula (6) is equivalent to a parallel connection of norator and nullator into those nodes, which causes the deletion of the correspondent column and the row of subcircuit matrix [62]. Therefore, the derived subcircuit may be called a «minor of circuit» by analogy with the term «minor of matrix». The symbolic expression of minor of the circuit can be calculated using formulae (1), (2) and (15).

The binary arrays represent the minors of the circuit with m number of external nodes; one of which is considered as a grounded node. The dimension of an array is $2n$, where $n = (m–1)$. The first n elements of the binary array form the norator vector and the last n elements form the nullator vector. There are two possible values for each element of vector: 0 or 1. The unity value of some entry of norator (nullator) vector means that norator (nullator) is inserted into the circuit between the correspondent node and grounded node. The norator and nullator of the inserted nullor are oriented in the same direction. In the case of zero value, the node is in open loop. The positions of entries in the vector can be presented by the tuple that consists of labels of a subcircuit external nodes excluding the basic node.

The number of binary arrays for an arbitrary subcircuit can be calculated by the formula:

$$v = \sum_{i=0}^{n} \binom{i}{n}^2, \tag{60}$$

where $\binom{i}{n}$ is a binomial coefficient.

The bisection formula (59) can be transformed by usage of the binary arrays concept for decomposition of the circuit by m nodes as follows:

$$\sum_{i=1}^{v} \delta_i \Delta_1(b_i) \Delta_2(\overline{b_i}), \tag{61}$$

where $\Delta_1(b_i)$ is a first subcircuit minor which corresponds to the binary array b_i; $\Delta_2(\overline{b_i})$ is a second subcircuit minor which corresponds to the binary array $\overline{b_i}$.

The norators and nullators that are inserted into the circuit minors can be enumerated in accordance with the values of the entries in the corresponding binary array. The binary array that corresponds to the circuit minors with enumerated

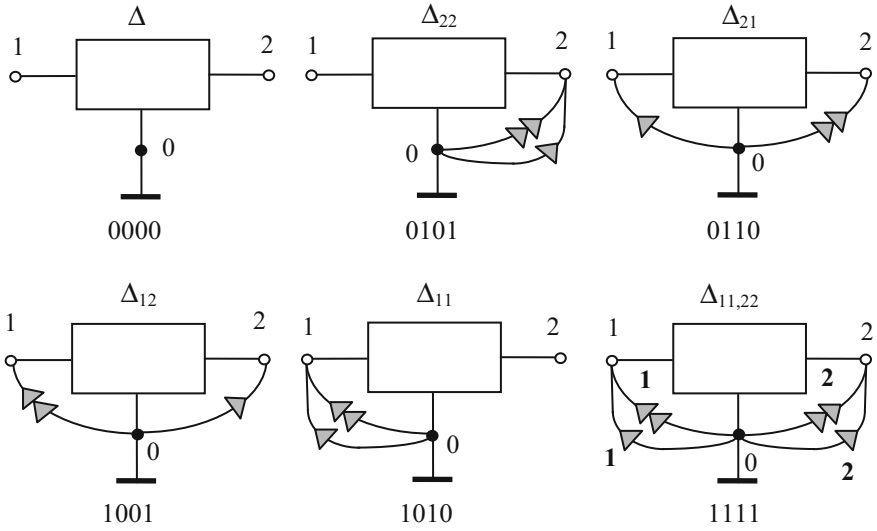


Fig. 12 The circuit minors and binary arrays of three-node subcircuit

nullors is called the enumerated binary array. Instead of nullator and norator connection information, this array contains nullor number which particular nullator and norator belong to. For example, the binary array $b = 110101$ of some circuit minor includes the two nullors labeled by « 1 » and « 2»; using those numbers binary array can be transformed into the following enumerated binary array: $b' = 120102$.

The nullor circuit that corresponds to the sum of two enumerated binary arrays, is consist of n norator-nullator pairs, connected in parallel. Norator-nullator pairs must be labeled by the same number to use the nullor simplification. If the labels of a norator and nullator of certain nullor are different the permutation of labels in the sum result of two enumerated binary arrays is needed. The determinant of nullor circuit is $\delta = 1$ if the amount of such permutations is even. In the opposite case, the sign of the product of $\Delta_1(b_i)$ and $\Delta_2(\overline{b}_i)$ in (61) is negative.

In the case of circuit bisection by three nodes ($n = 2$) the dimension of binary arrays is $2n = 4$. The six binary arrays which are presented in Fig. 12 can be derived as the result of bisection. They are corresponding to the circuit minors of

Table 6 The binary arrays, the enumerated binary arrays, the sum results of enumerated binary arrays and the determinants values in the case of circuit bisection by 3 nodes

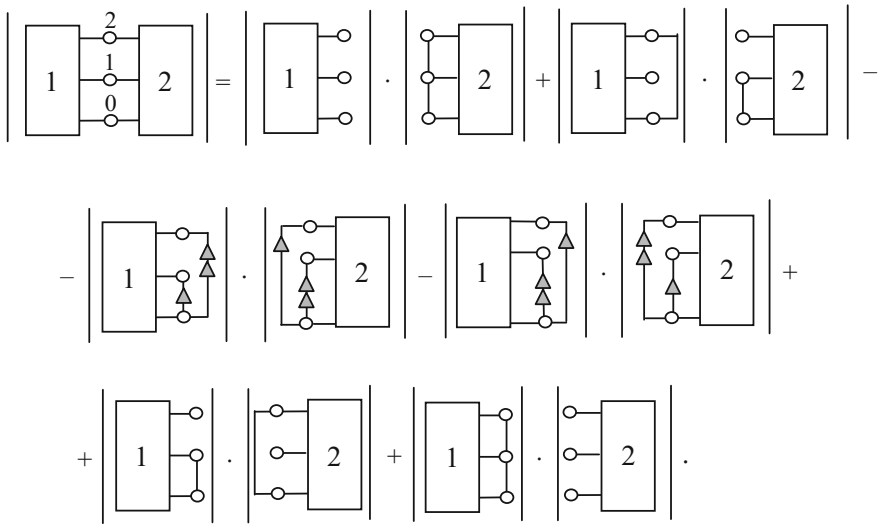
i	b_i	$\overline{b_i}$	b_i'	$\overline{b_i'}$	$b_i' + \overline{b_i'}$	δ_i
1	0000	1111	0000	1212	1212	1
2	0101	1010	0101	2020	2121	1
3	0110	1001	0110	2002	2112	–1
4	1001	0110	1001	0220	1221	–1
5	1010	0101	1010	0202	1212	1
6	1111	0000	1212	0000	1212	1

the first subcircuit in (61). The binary arrays of the second subcircuit can be obtained by operation of the one's complement of the binary number. The tuple of common (or external) nodes of subcircuits can be written as 1212. The binary arrays, their enumerated forms, the sum results of two enumerated binary arrays and the determinants values of corresponding nullor circuits are presented in Table 6.

The decomposition formula (61) in the case of bisection by three nodes can be expressed as follows:

$$\begin{aligned}\Delta = {} & \Delta_1(b_1)\Delta_2(\overline{b}_1) + \Delta_1(b_2)\Delta_2(\overline{b}_2) - \Delta_1(b_3)\Delta_2(\overline{b}_3) - \\ & - \Delta_1(b_4)\Delta_2(\overline{b}_4) + \Delta_1(b_5)\Delta_2(\overline{b}_5) + \Delta_1(b_6)\Delta_2(\overline{b}_6).\end{aligned} \tag{62}$$

The circuit-algebraic form of (62) is presented below:



(63)

Let's consider the case of circuit bisection by four nodes ($n = 3$) as shown in Fig. 13a. The dimension of binary arrays is $2n = 6$. The binary arrays in which the number of unities in norator vector differs from a number of unities in nullator

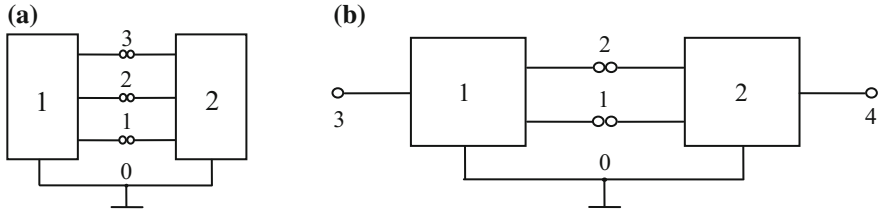


Fig. 13 The model of circuit bisection by four nodes **a**, the model of combination of two subcircuits **b**

vector are excluded from search space 000000 to 111111 in accordance with (60). Thereby twenty binary arrays for each of subcircuit are presented in Table 7, as well as their enumerated forms, the sum results of two enumerated binary arrays and the determinants values of corresponding nullor circuits.

The decomposition formula (61) in the case of bisection by four nodes can be expressed as follows:

$$\Delta = \Delta_1(b_1)\Delta_2(\overline{b}_1) + \Delta_1(b_2)\Delta_2(\overline{b}_2) - \Delta_1(b_3)\Delta_2(\overline{b}_3) + \Delta_1(b_4)\Delta_2(\overline{b}_4) - \Delta_1(b_5)\Delta_2(\overline{b}_5) + \Delta_1(b_6)\Delta_2(\overline{b}_6) - \Delta_1(b_7)\Delta_2(\overline{b}_7) + \Delta_1(b_8)\Delta_2(\overline{b}_8) - \Delta_1(b_9)\Delta_2(\overline{b}_9) + \Delta_1(b_{10})\Delta_2(\overline{b}_{10}) + \Delta_1(b_{11})\Delta_2(\overline{b}_{11}) - \Delta_1(b_{12})\Delta_2(\overline{b}_{12}) + \Delta_1(b_{13})\Delta_2(\overline{b}_{13}) - \Delta_1(b_{14})\Delta_2() + \Delta_1(b_{15})\Delta_2(\overline{b}_{15}) - \Delta_1(b_{16})\Delta_2(\overline{b}_{16}) + \Delta_1(b_{17})\Delta_2(\overline{b}_{17}) - \Delta_1(b_{18})\Delta_2(\overline{b}_{18}) + \Delta_1(b_{19})\Delta_2(\overline{b}_{19}) + \Delta_1(b_{20})\Delta_2(\overline{b}_{20}). \quad (64)$$

The bisection operation by the proposed formula (61) can be used for every derived circuit minors provides the downward hierarchical decomposition of the circuit for closed-form determinant expressions calculation. Note, that the input-port and output-port of certain CS, nullor or pathological mirrors pair, cannot be included separately in different subcircuits.

5.2 The Upward Hierarchical Analysis

The upward hierarchical analysis by GPEM starts from the decomposition of the circuit by bisection formula (61) and follows by the pairwise combination of subcircuits. The binary arrays and corresponding circuit minors are used for the representation of subcircuits. Suppose two n-port circuits combined into one circuit by m ports, which may be called the common nodes. Let's consider the input and output ports of the circuit as external nodes. Some of the common nodes of the combined circuit can be also the external nodes.

The following algorithm is used for the combination of two subcircuits:

1. Generate the set of binary arrays for each of subcircuits.
2. Perform the pairwise comparison of binary arrays using the entries that correspond to common nodes of subcircuits to find the pairs of joint binary arrays. Two binary arrays are called jointed if the entries values that correspond to the common nodes are complementary and the sum of those values is not equal to zero.
3. Generate the set of binary arrays of the combined circuit using joint binary arrays. The values of binary arrays must be written in accordance with circuit tuple in the following order: firstly, the values of binary arrays which correspond to the non-common external nodes of the first subcircuit, next, the values of the binary arrays which correspond to the common nodes, and, finally, the values of the binary arrays which correspond to the non-common external nodes of the second subcircuit. The unity must be written into binary array

entries that correspond to the common external nodes of the combined circuit if there are the unity values in the corresponding entries of the joint binary arrays.
4. Calculate the sign of circuit minors product represented by joint binary arrays according to (61). The sign is positive if the number of permutations in the enumerated joint binary arrays is even and vice versa. If the values of entries that correspond to the common external nodes are equal to unity in both joint binary arrays then the unity values of such entries in one of the binary arrays must be replaced by zero.
5. Summarize the circuit minors products that correspond to the pairs of joint binary arrays for each of combined circuit minors.

Let's consider the following example to illustrate the usage of the proposed algorithm. The circuit with three nodes labeled by 3, 4 and 0 shown in Fig. 13b is obtained by combining two subcircuits 1 and 2 with four external nodes. Thereby the dimension of binary arrays is equal to 6 in the case of the separated subcircuits and to 4 in the case of the combined circuit.

A number of external nodes is the same in both subcircuits, therefore we can use the set of binary arrays from the second column in Table 7. The tuples of binary arrays of first and second subcircuits can be expressed as 312312 and 124124

Table 7 The binary arrays, the enumerated binary arrays, the sum results of enumerated binary arrays and the determinants values in the case of circuit bisection by 4 nodes

i	b_i	$\overline{b}_i$	$b_i^{'}$	$\overline{b_i^{'}}$	$b_i^{'}+\overline{b_i^{'}}$	δ_i
1	000000	111111	000000	123123	123123	1
2	001001	110110	001001	230230	231231	1
3	001010	110101	001010	230203	231213	–1
4	001100	110011	001100	230023	231123	1
5	010001	101110	010001	203230	213231	–1
6	010010	101101	010010	203203	213213	1
7	010100	101011	010100	203023	213123	–1
8	011011	100100	012012	300300	312312	1
9	011101	100010	012102	300030	312132	–1
10	011110	100001	012120	300003	312123	1
11	100001	011110	100001	023230	123231	1
12	100010	011101	100010	023203	123213	–1
13	100100	011011	100100	023023	123123	1
14	101011	010100	102012	030300	132312	–1
15	101101	010010	102102	030030	132132	1
16	101110	010001	102120	030003	132123	–1
17	110011	001100	120012	003300	123312	1
18	110101	001010	120102	003030	123132	–1
19	110110	001001	120120	003003	123123	1
20	111111	000000	123123	000000	123123	1

correspondingly. Obviously, we need to take into account only the entries 1212 that correspond to the common nodes of subcircuits to find the set of joint binary arrays pairs and their signs. For example, two binary arrays $b_2 = 001001$ and $b_{13} = 100100$ are jointed because their values at the entries 1212 are mutually complementary: 0101 and 1010. The sign can be calculated by summation of values at the entries of the binary arrays 1212 in the enumerated form: 0101 + 2020 = 2121. Thereby the sign of the product of two circuit minors $D_1(b_2)$ $\bullet D_2(b_{13})$ is positive.

Let's consider another pair of joint binary arrays $b_5 = 010001$ and $b_9 = 011101$. The values at the entries 1212 are 1001 and 0110 correspondingly. The sum result of entries in the enumerated form is 1221, therefore the sign of the product of two circuit minors $D_1(b_5)\bullet D_2(b_9)$ is negative.

The tuple of binary arrays of the combined circuit consists of labels of non-common external nodes: 3434. The values at such entries in the joint binary arrays are used to generate the combined circuit binary arrays. For example, the values of b_2 and b_{13} at the entries 3434 are 0000. The binary array 0101 of the combined circuit corresponds to the combination of the pair: b_5 and b_9. The binary arrays of combined circuit and corresponding joint binary arrays are presented in Table 8.

The circuit minors of combined circuit can be calculated in accordance with Table 8 as following:

$$\begin{gathered}
\Delta(0000) = \Delta_1(b_1)\Delta_2(b_{19}) + \Delta_1(b_2)\Delta_2(b_{13}) - \Delta_1(b_3)\Delta_2(b_{12}) - \Delta_1(b_5)\Delta_2(b_9) + \Delta_1(b_6)\Delta_2(b_8) + \Delta_1(b_8)\Delta_2(b_2),\\
\Delta(0101) = \Delta_1(b_1)\Delta_2(b_{20}) + \Delta_1(b_2)\Delta_2(b_{15}) - \Delta_1(b_3)\Delta_2(b_{14}) - \Delta_1(b_5)\Delta_2(b_9) + \Delta_1(b_6)\Delta_2(b_8) + \Delta_1(b_8)\Delta_2(b_2),\\
\Delta(0110) = \Delta_1(b_4)\Delta_2(b_{16}) - \Delta_1(b_7)\Delta_2(b_{10}) + \Delta_1(b_9)\Delta_2(b_4) - \Delta_1(b_{10})\Delta_2(b_3),\\
\Delta(1001) = \Delta_1(b_{11})\Delta_2(b_{18}) - \Delta_1(b_{12})\Delta_2(b_{17}) + \Delta_1(b_{14})\Delta_2(b_{11}) - \Delta_1(b_{17})\Delta_2(b_5),\\
\Delta(1010) = \Delta_1(b_{13})\Delta_2(b_{17}) + \Delta_1(b_{15})\Delta_2(b_{13}) - \Delta_1(b_{16})\Delta_2(b_{12}) - \Delta_1(b_{18})\Delta_2(b_7) + \Delta_1(b_{19})\Delta_2(b_6) + \Delta_1(b_{20})\Delta_2(b_1),\\
\Delta(1111) = \Delta_1(b_{13})\Delta_2(b_{20}) + \Delta_1(b_{15})\Delta_2(b_{15}) - \Delta_1(b_{16})\Delta_2(b_{14}) - \Delta_1(b_{18})\Delta_2(b_9) + \Delta_1(b_{19})\Delta_2(b_8) + \Delta_1(b_{20})\Delta_2(b_2).
\end{gathered} \tag{65}$$

As seen from (65), generation of SoE by proposed algorithm involves a large number of calculations of circuit minors. However, decomposition of the circuit with nullors can be simplified by using degeneracy conditions [29]. Thereby the number of circuit minors can be significantly reduced by using the following rules:

1. The zero value must be written in norator vector of subcircuit binary array at the entry that corresponds to the external node a if there is a norator of certain nullor or VM between nodes a and 0 in the subcircuit.
2. The unity value must be written in norator vector of subcircuit binary array at the entry that corresponds to the common external node a if there is a norator of certain nullor or VM between nodes a and 0 in the second subcircuit.
3. The zero value must be written in nullator vector of subcircuit binary array at the entry which corresponds to the external node a if there is a nullator of certain nullor or CM is connected between nodes a and 0 in the subcircuit.

Table 8 The joint binary arrays of subcircuits 1 and 2 and binary arrays of combined circuit

The binary arrays of combined circuit (tuple 3434)	The joint binary arrays of subcircuits 1 and 2		δ
	The tuple 312312	The tuple 124124	
0000	$b_1 = 000000$	$b_{19} = 110110$	1
	$b_2 = 001001$	$b_{13} = 100100$	1
	$b_3 = 001010$	$b_{12} = 100010$	–1
	$b_5 = 010001$	$b_7 = 010100$	–1
	$b_6 = 010010$	$b_6 = 010010$	1
	$b_8 = 011011$	$b_1 = 100100$	1
0101	$b_1 = 000000$	$b_{20} = 000000$	1
	$b_2 = 001001$	$b_{15} = 101101$	1
	$b_3 = 001010$	$b_{14} = 101011$	–1
	$b_5 = 010001$	$b_9 = 011101$	–1
	$b_6 = 010010$	$b_8 = 011011$	1
	$b_8 = 011011$	$b_2 = 001001$	1
0110	$b_4 = 001100$	$b_{16} = 101110$	1
	$b_7 = 010100$	$b_{10} = 011110$	–1
	$b_9 = 011101$	$b_4 = 001100$	1
	$b_{10} = 011110$	$b_3 = 001010$	–1
1001	$b_{11} = 100001$	$b_{18} = 110101$	1
	$b_{12} = 100010$	$b_{17} = 110011$	–1
	$b_{14} = 101011$	$b_{11} = 100001$	1
	$b_{17} = 110011$	$b_5 = 010001$	1
1010	$b_{13} = 100100$	$b_{19} = 110110$	1
	$b_{15} = 101101$	$b_{13} = 100100$	1
	$b_{16} = 101110$	$b_{12} = 100010$	–1
	$b_{18} = 110101$	$b_7 = 010100$	–1
	$b_{19} = 110110$	$b_6 = 010010$	1
	$b_{20} = 000000$	$b_1 = 000000$	1
1111	$b_{13} = 100100$	$b_{20} = 000000$	1
	$b_{15} = 101101$	$b_{15} = 101101$	1
	$b_{16} = 101110$	$b_{14} = 101011$	–1
	$b_{18} = 110101$	$b_9 = 011101$	–1
	$b_{19} = 110110$	$b_8 = 011011$	1
	$b_{20} = 000000$	$b_2 = 001001$	1

4. The unity value must be written in nullator vector of subcircuit binary array at the entry that corresponds to the common external node a if there is a norator of certain nullor or CM between nodes a and 0 in the second subcircuit.

For example, suppose that in three-node nullor-equivalent subcircuit there is norator which is connected between nodes 2 and 0. In accordance with proposed

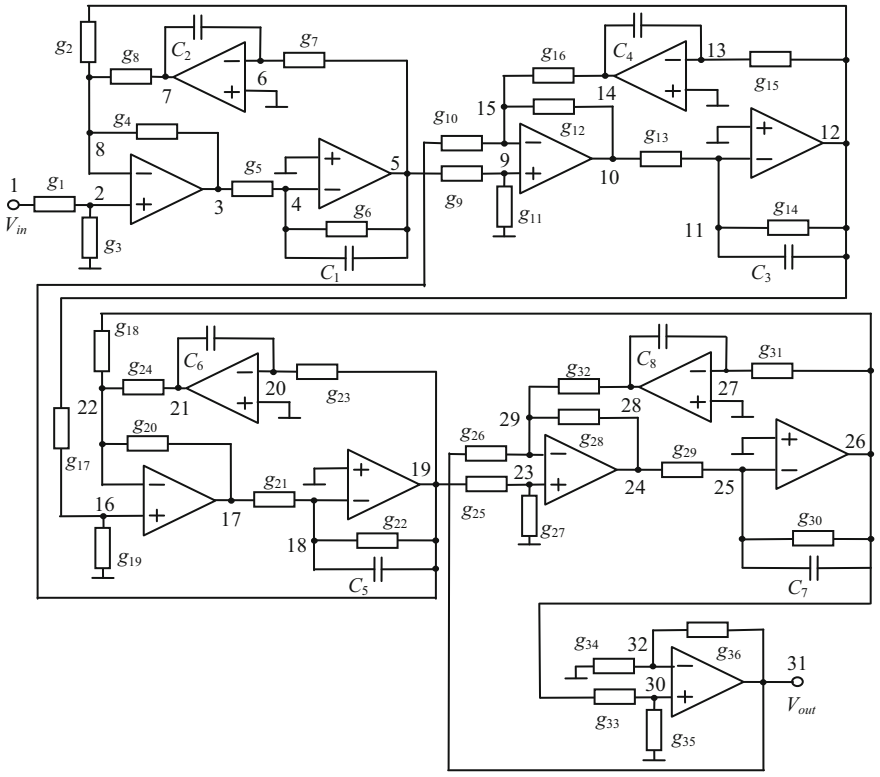


Fig. 14 The band-pass filter [44]

rules, only three binary arrays is generated instead of six which presented in Table 6: 0000, 1001, 1010.

Example 7 Let's consider the band-pass filter shown in Fig. 14, which was firstly symbolically calculated in the paper [44] by J. A. Starzyk and A. Konczykowska. This is a well-known test circuit for symbolic analysis methods. It contains 13

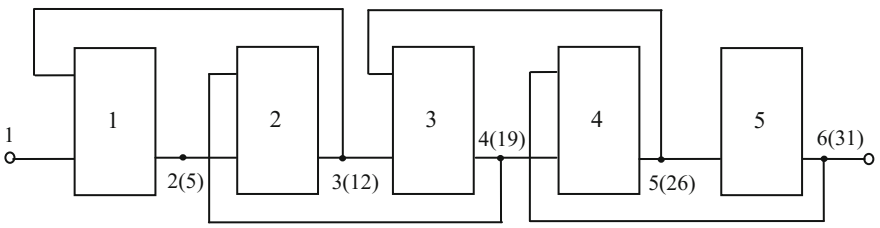


Fig. 15 The subcircuit-level model of band-pass filter

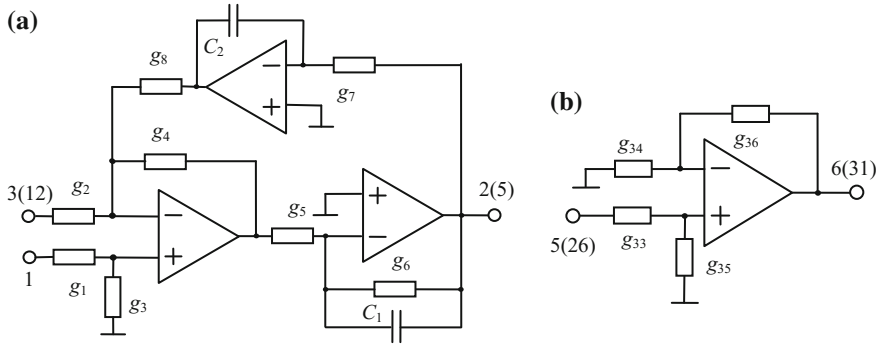


Fig. 16 The first **a** and fifth **b** subcircuits of band-pass filter

OpAmps modeled by nullors, and 36 resistors and 8 capacitors modeled by admittances.

The filter can be decomposed into the five subcircuits as shown in Fig. 15. Note that for the sake of clarity the common nodes of subcircuits are renumbered. The original nodes labels are shown in brackets in Fig. 15. The subcircuit 1 presented in Fig. 16 is topologically identical to the subcircuits 2–4. Therefore the subcircuits 2–4 can be easily derived from Fig. 16 by substitution of identification numbers of symbols of resistors and capacitors correspondingly by the following formulae:

$$N_R = i + 8(j-1), \tag{66}$$

$$N_C = i + 2(j-1), \tag{67}$$

where i is an identification number in subcircuit 1, $j = \{2,3,4\}$ is a number of one of the subcircuits 2–4.

There are four external nodes in subcircuits 1–4. In this case, 20 binary arrays can be derived. However the equivalent circuit of filter includes the 13 nullor, therefore, the number of binary arrays can be greatly reduced by usage of Rules I and II: $b_1 = 101011$, $b_2 = 101101$, $b_3 = 101110$. The tuples of binary arrays for the subcircuits 1–4 can be expressed as follows: 123123, 234234, 345345, 456456.

In the case of subcircuit 5 in Fig. 16b which includes three external nodes the number of binary arrays can be reduced to the two: $b_1 = 1001$, $b_2 = 1010$. The tuple of these binary arrays is following: 5656.

The expressions of circuit minors of subcircuits 1 and 5 calculated by GPEM are presented below:

$$\begin{gathered}
\Delta_1(b_1) = -g_1 g_5 s C_2 (g_2 + g_4 + g_8), \\
\Delta_1(b_2) = (g_1 + g_3)[(g_6 + sC_1) g_4 p C_2 + g_5 g_7 g_8], \\
\Delta_1(b_3) = g_2 g_5 s C_2 (g_1 + g_3), \\
\Delta_5(b_1) = g_{33}(g_{34} + g_{36}), \\
\Delta_5(b_2) = g_{36}(g_{33} + g_{35}).
\end{gathered} \tag{68}$$

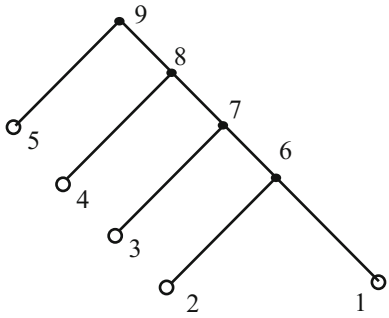


Fig. 17 The hierarchical tree for combination of circuit minors of band-pass filter

The expressions of circuit minors of subcircuits 2–4 can be derived from (68) by renumbering of symbols numbers in accordance with (66) and (67):

$$\begin{gathered}
\Delta_2(b_1) = -g_9 g_{13} sC_4 (g_{10} + g_{12} + g_{16}), \\
\Delta_2(b_2) = (g_9 + g_{11})[(g_{14} + sC_3) g_{12} sC_2 + g_{13} g_{15} g_{16}], \\
\Delta_2(b_3) = g_{10} g_{13} sC_4 (g_9 + g_{11}), \\
\Delta_3(b_1) = -g_{17} g_{21} sC_6 (g_{18} + g_{20} + g_{24}), \\
\Delta_3(b_2) = (g_{17} + g_{19})[(g_{22} + sC_5) g_{20} sC_6 + g_{21} g_{23} g_{24}], \\
\Delta_3(b_3) = g_{18} g_{21} sC_6 (g_{17} + g_{19}), \\
\Delta_4(b_1) = -g_{25} g_{29} sC_8 (g_{26} + g_{28} + g_{32}), \\
\Delta_4(b_2) = (g_{25} + g_{27})[(g_{30} + sC_7) g_{28} sC_8 + g_{29} g_{31} g_{32}], \\
\Delta_4(b_3) = g_{26} g_{29} sC_8 (g_{25} + g_{27}).
\end{gathered} \tag{69}$$

The transfer function of the filter can be expressed as result of the combination of circuit minors (68) and (69) by using the hierarchical tree presented in Fig. 17. The labels of vertices 1–5 are corresponding to the numbers of subcircuits 1–5 in Fig. 15. The labels of vertices 6–9 are corresponding to the numbers of new subcircuits which are obtained by the bottom-up combination of subcircuits. Obviously, the original filter circuit which corresponds to the vertex 9 is the final result of subcircuits combination.

Let's consider the combination of subcircuits 1 and 2 by nodes 0, 2 and 3. The entries 2323 must be taken into account to find the set of joint binary arrays pairs and their signs. Note that the values at the entries which correspond to the common non-external node 2 must be mutually complementary, while the value in the entries which correspond to the common external node 3 cannot be equal to zero. The pairs of joint binary arrays, binary arrays of combined subcircuit 6 are presented in Table 9.

The combination of other subcircuits can be performed in a similar way. Thereby the final quite compact SoE of filter transfer function is expressed as following:

Table 9 The joint binary arrays of subcircuits 1 and 2 and binary arrays of combined circuit

The binary arrays of combined subcircuit 6 (tuple 134134)		The joint binary arrays of subcircuits 1 and 2		δ
		The tuple 123123	The tuple 234234	
1	101011	2 $b_1 = 101011$	1 $b_1 = 101011$	1
2	101101	$b_2 = 101101$	$b_2 = 101101$	1
		$b_2 = 101101$	$b_3 = 101110$	–1
3	101110	$b_3 = 101110$	$b_1 = 101011$	1

$$\begin{gathered}\Delta_6(b_1)=\Delta_1(b_1)\Delta_2(b_1),\ \Delta_6(b_2)=\Delta_1(b_2)\Delta_2(b_2)-\Delta_1(b_3)\Delta_2(b_1),\\ \Delta_6(b_3)=\Delta_1(b_2)\Delta_2(b_3),\quad \Delta_7(b_1)=\Delta_6(b_1)\Delta_3(b_1),\\ \Delta_7(b_2)=\Delta_6(b_2)\Delta_3(b_2)-\Delta_6(b_3)\Delta_3(b_1),\ \Delta_7(b_3)=\Delta_6(b_2)\Delta_3(b_3),\\ \Delta_8(b_1)=\Delta_7(b_1)\Delta_4(b_1),\ \Delta_8(b_2)=\Delta_7(b_2)\Delta_4(b_2)-\Delta_7(b_3)\Delta_4(b_1),\\ \Delta_8(b_3)=\Delta_7(b_2)\Delta_4(b_3),\ \Delta_9(b_1)=\Delta_8(b_1)\Delta_5(b_1),\\ \Delta_9(b_2)=\Delta_8(b_2)\Delta_5(b_2)-\Delta_8(b_3)\Delta_5(b_1),\quad H=\Delta_9(b_1)/\Delta_9(b_2).\end{gathered} \tag{70}$$

The obtained result (70) can be verified by numerical simulation or exact comparison with the symbolic solution presented in [44].

6 Conclusion

In this chapter, we briefly review the basics of GPEM and its applications for symbolic analysis of large circuits with pathological element-based active device models. The method can be used for analysis of circuits containing all linear circuit elements, including nullors, four types of controlled sources, and pathological mirrors. We start with the parameter extraction formulae and circuit degeneracy conditions. Then we introduce an algorithm to improve the efficiency of determinants calculation of residual circuits containing pathological elements only. Such circuits can be derived from active networks in which all of the impedances, admittances, and CS were extracted. The algorithm proposed is based on the concept of HOSC and provides the determinant calculation by usage of simple matrix algebra operations instead of topological simplifications. Further, the hierarchical decomposition procedures for symbolic analysis of large circuits by GPEM have been introduced. The techniques proposed of upward analysis and downward analysis provide the calculation of a circuit function in the form of a single nested expression or in the form of sequence of expressions correspondingly. All described algorithms were implemented in the computer program for circuit analysis CirSym.

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Two-Graph Based Semi-topological Analysis of Electronic Circuits with Nullors and Pathological Mirrors

Marian Pierzchala and Mourad Fakhfakh

Abstract Abstraction level elements such as nulattor, norator, current mirrors and voltage mirrors have been very useful in the analysis of linear circuits. In this chapter, we proposed a method for the analysis of linear circuits with the pathological elements which is based on the two-graph representation of these elements and the semi-topological procedure of calculations of the network functions. For completeness, the method has been extended to encompass RLC–elements, all types of controlled sources, voltage and current independent sources. The procedure of calculation is based on the product matrices and on a numerical formula of evaluation of unimodular determinants. No sign rule is required for their evaluations, and canceling terms are extracted during their evaluations. In this chapter the symbolic analysis is preferred because symbolic expressions give good insight on the behavior of the circuit and can also be used in the optimization procedures.

1 Introduction

Nullors and mirrors are often used to model active devices. They are named pathological or singular because they possess ideal characteristics and are specified according to the constraints they impose on their terminal voltages and currents. Pathological elements are very useful in modeling and analysis of analog circuits [1–10]. In this chapter we advocates deal with the symbolic analysis because symbolic expressions give good insight on the behavior of the circuit and can also be used within optimization procedures. Actually, the literature offers a large number of publications dealing with the symbolic analysis of analog circuits using the above-mentioned pathological elements. These publications can be divided into

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two groups: in the first one the authors analyze the RLC–nullor circuits, i.e. the circuits in which the mirrors are replaced by their nullor equivalents (see for example [11, 12]) and the second one, in which the authors analyze the RLC, nullor-mirror circuits, i.e. the circuits without replacing the mirror elements with their nullor equivalents (for example [13, 14]). Regarding the formulation methods we can distinguish the following ones: the modified nodal analysis [15, 11, 13], the generalized parameter extraction method [12] and the two-graph method [14]. In this chapter we propose a new method which analyzes the RLC, nullor-mirror circuits on the base of signal-flow graph in the two-graph version. The method is semi-topological in the sense that the matrices (loop and cutset) are formulated using voltage and current graphs and the calculation of the network functions is realized numerically.

2 Primitive Signal-Flow Graphs as a Base of Semi-topological Analysis of Electronic Circuits with Nullors and Mirrors

Consider first the simpler case of network consisting of immittance (impedance or admittance) elements and independent sources only. We assume that the independent voltage sources contain no loops, and the independent current sources contain no cut-sets. Then, it is always possible to select a tree T such that all voltage sources are tree branches, and all current sources are links (cotree branches). The network branches are divided into four sets (each set may be empty) indicated by subscript as follows:

E: independent voltage sources
I: independent current sources,
$\mathbf{Z_T}$: impedance branches in the tree,
$\mathbf{Y_C}$: admittance branches in the cotree.

For such network [16] a unique signal-flow graph can be constructed, as illustrated in Fig. 1. In Fig. 1, $\boldsymbol{B_{YE}}$, $\boldsymbol{B_{YZ}}$ denote the fundamental loop matrices and $\boldsymbol{Q_{ZI}}$, $\boldsymbol{Q_{ZY}}$ denote the fundamental cut-set matrices. For the passive networks $\boldsymbol{Q_{ZY}} = -(\boldsymbol{B_{YZ}})^{t}$ and the matrices $\boldsymbol{Y_Y}$ and $\boldsymbol{Z_Z}$ have a diagonal form.

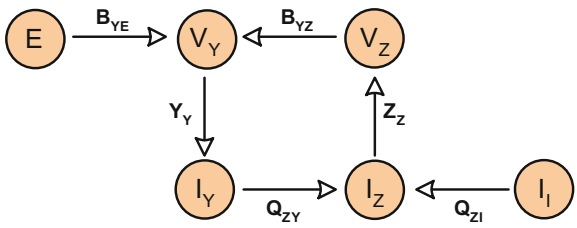
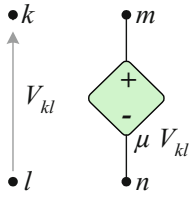
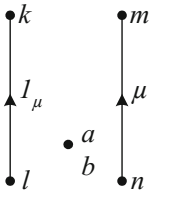
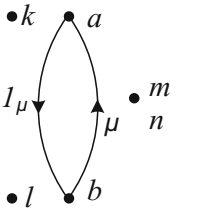
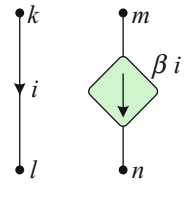
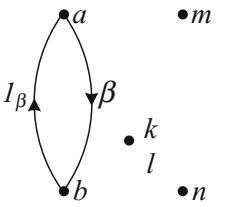
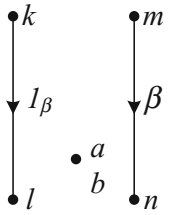
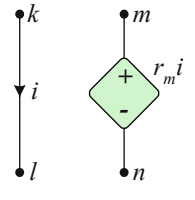
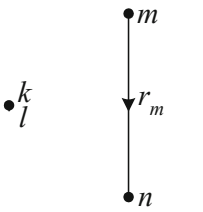
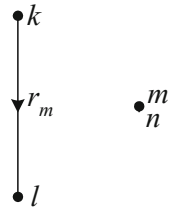
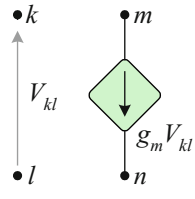
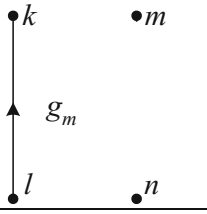
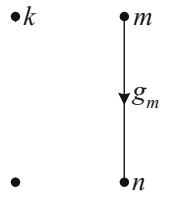


Fig. 1 The *SFG* of passive networks

Table 1 Two-graph stamps for controlled sources

	Symbol	*V-graph*	*I-graph*
VCVS			
CCCS			
CCVS			
VCCS			

For the active networks, i.e. networks with controlled sources, matrices $\boldsymbol{Y_Y}$ and $\boldsymbol{Z_Z}$ are no longer diagonal. Few methods have been proposed in the literature to overcome this problem. The two-graph method was the first to appear in the literature [17]. Since the matrices of two different graphs, namely the current graph $\boldsymbol{G_I}$ and the voltage graph $\boldsymbol{G_V}$, have been used to formulate the equations, the matrices $\boldsymbol{B_{YE}}$, $\boldsymbol{B_{YZ}}$ and $\boldsymbol{Q_{ZI}}$, $\boldsymbol{Q_{ZY}}$ should be calculated individually, i.e. $\boldsymbol{Q_{ZY}} \neq -(\boldsymbol{B_{YZ}})^{t}$. In the original method only voltage controlled current sources can be used. Two-graph stamps of the other linear controlled sources were proposed in [18], they are given in Table 1. With these stamps matrices $\boldsymbol{Z_Z}$ and $\boldsymbol{Y_Y}$ will have diagonal forms.

VCVS, *CCCS*, *CCVS* and *VCCS* refer respectively to voltage controlled current sources, current controlled voltage sources, current controlled current sources and voltage controlled current sources.

In the classical signal flow-graph method, the *transmission* from the source node X_s to the dependent node X_j is obtained by the *Mason*'s formula [19].

$$T_{js} = \frac{X_j}{X_s} = \frac{\sum P_k \Delta_k}{\Delta} \tag{1}$$

where

$\Delta = 1 -$ (the sum of all loop weights) + (the sum of all second-order loop weights) − (the sum of all third-order loop weights) + ⋯

$P_k =$ weight of the kth path from the source node X_s to the dependent node X_j,

$\Delta_k =$ the sum of those terms in Δ without any constituent loops touching the path P_k.

The summation is taken over all paths from X_s to X_j.

The calculation of the *Mason*'s formula is reduced to that of enumerating some subgraphs in the SFG. In this sense the SFG method with *Mason*'s formula is called a *topological method*.

Mason's formula for computing the transfer functions, as given by Eq. (1) has two distinct sets of topological rules: one for the denominator Δ, and the other for the numerator $\sum P_k \Delta_k$. From the practical point of view, it would be very convenient to evaluate both the denominator and numerator numerically. This is made possible by the use of the *semi-topological method.* The semi-topological formulas are based on the topological method. But once the basic matrices are determined from the voltage and current graphs, the remainder will depend only on the matrices, and the flow graphs are not required for their evaluations. Furthermore, the evaluating procedure is indirect and purely numerical. The procedure consists of using the new matrices, named the product matrices [20], which are based on the product graph [21]. In the following, we will apply (see Eqs. (2a, 2b) such formula for the analysis of connected, linear, time-invariant active or passive networks modeled with *RLC* elements, voltage controlled current sources and independent current and voltage sources [22]. Later, these formulae will be generalized to the networks containing all types of controlled sources, nullors, mirrors, voltage and current independent sources.

Theorem

Let T^v_{qp} (T^i_{qp}) denote the voltage (current) transmission (or gain) from the voltage source V_{sp} (the current source I_{sp}) to the voltage V_q across (the current source I_q through) the tree (cotree) branch Z_q (Y_q) in the nonreciprocal network N^n. Then, we have:

$$T_{qp}^{v} = \frac{\sum_{k=1}^{h} \sum_{m(iq)} \left[\left(\prod_{m=1}^{k} Z_{im} Y_{jm} \right) (\det P_k^{vs1}) (\det P_k^{i}) \right]}{1 + \sum_{k=1}^{h} \sum_{m} \left[\left(\prod_{m=1}^{k} Z_{im} Y_{jm} \right) (\det P_k^{v}) (\det P_k^{i}) \right]} \tag{2a}$$

$$T_{qp}^{i} = \frac{-\sum_{k=1}^{h} \sum_{m(jq)} \left[\left(\prod_{m=1}^{k} Z_{im} Y_{jm} \right) (\det P_k^{v}) (\det P_k^{is1}) \right]}{1 + \sum_{k=1}^{h} \sum_{m} \left[\left(\prod_{m=1}^{k} Z_{im} Y_{jm} \right) (\det P_k^{v}) (\det P_k^{i}) \right]} \tag{2b}$$

In (2a, 2b), Σ_m means the summation of all possible i_m*'s* and j_m*'s*. $\Sigma_{m(iq)}$ is the summation of all possible i_m*'s* including i_q in and all possible j_m*'s*. $\Sigma_{m(jq)}$ is the summation of all possible i_m*'s* including i_q in j_m*'s*, and $\prod_{m=1}^{k} Z_{im} Y_{jm}$ is the product of k impedances and k admittances of the (k *x* k) submatrix P_k^v, P_k^{vs1}, P_k^i, P_k^{is1}. The subscript q of i_q and j_q is borrowed from the measuring branch immitance Z_q *(*Y_q*)* to denote the corresponding row and column.

Definitions

Let N_n be a *nonreciprocal* network with n nodes N_1, …, N_n, b branches B_1, …, B_b, s sources (v voltage sources V_{s1}, …, V_{sv} and i current sources I_{sv+1}, …, I_{ss}) and c voltage controlled current sources.

Definition 1. [22] **V–substituted Voltage Product Matrix P^{vs1} (I–substituted Current Product Matrix P^{is1})**

The V- substituted voltage (I-substituted current Product Matrix) P^{vs1} (P^{is1}) is obtained from Voltage (Current) Product Matrix P^v (P^i) as follows:

(i) Substitute 0 for every element of the row (column) named as Z_q (Y_q) of P^v (P^i),
(ii) For the elements of this row (column)

(a) Substitute +1, if the tree (cotree) branch of the voltage source V_{sp} (current source I_{sp}*)* has the same arrow orientation as the cotree branch (tree branch) in the voltage (current) graph G^{vs} (G^{is}) when cuttsetting,
(b) Substitute −1, if the tree (cotree) branch of the voltage source V_{sp} (current source I_{sp}*)* has the opposite arrow orientation as the cotree branch (tree branch) in G^{vs} (G^{is}) when cuttsetting,
(c) Keep 0, otherwise.

Definition 2. [20] **Voltage Product Matrix P^v (Current Product Matrix P^i)**

The voltage (current) product matrix P^v (P^i) is defined as the product matrix of the voltage (current) graph G^v (G^i). In P^v or P^i, we give the name Z_i to the ith row; Y_j to the jth column, when $r + 1 \leq j \leq r + \mu = b$, and Y_{ci} to the jth column, when $b + 1 \leq j \leq b + c$, $j = b + 1$.

Example

A nonreciprocal network [22] is shown in Fig. 2, where it is desired to obtain the voltage transmission T_{21}^v.

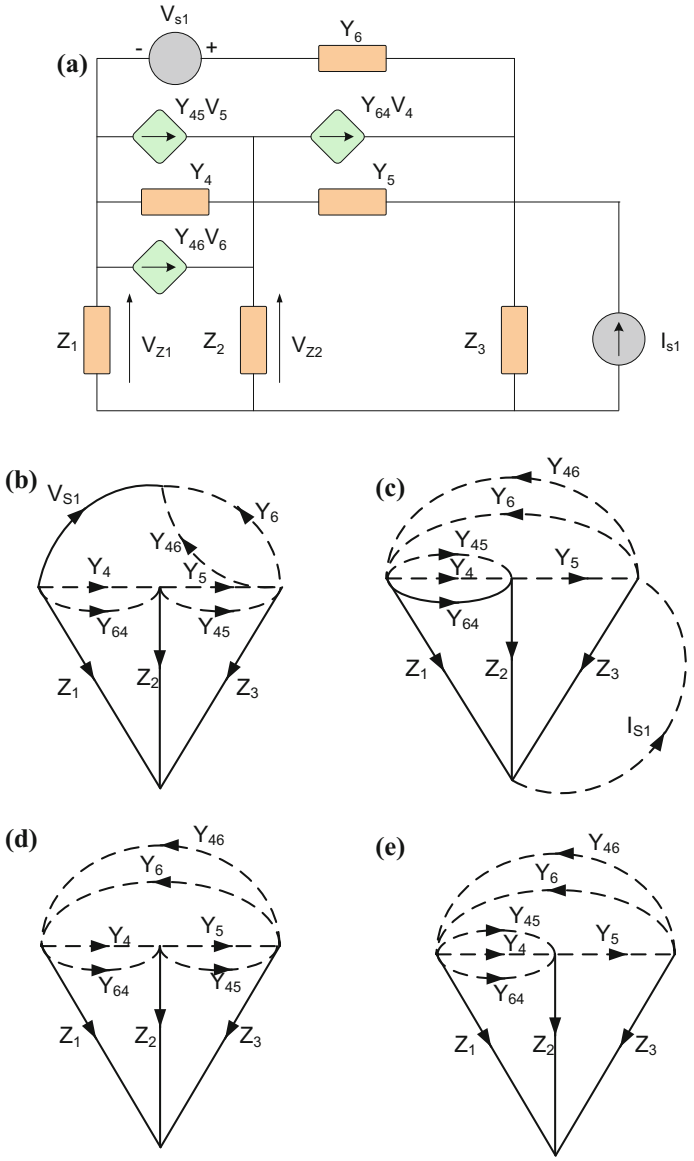


Fig. 2 **a** A nonreciprocal network, **b** G^{vs}, **c** G^{is}, **d** G^{v}, **e** G^{i}

From Fig. 2 we have:

$P^v =$		Y_4	Y_5	Y_6	Y_{45}	Y_{46}	Y_{64}
	Z_1	1	0	−1	0	−1	1
	Z_2	−1	−1	0	−1	0	−1
	Z_3	0	1	1	1	1	0

$P^i =$		Y_4	Y_5	Y_6	Y_{45}	Y_{46}	Y_{64}
	Z_1	1	0	−1	1	1	−1
	Z_2	−1	−1	0	−1	−1	0
	Z_3	0	1	1	0	0	1

$P^{vs} =$		Y_4	Y_5	Y_6	Y_{45}	Y_{46}	Y_{64}
	Z_1	1	0	−1	0	−1	1
	Z_2	0	0	1	0	1	0
	Z_3	0	1	1	1	1	0

$P^{is} =$		Y_4	Y_5	Y_6	Y_{45}	Y_{46}	Y_{64}
	Z_1	1	0	−1	1	1	−1
	Z_2	−1	0	0	−1	−1	0
	Z_3	0	−1	1	0	0	1

All possible combinations for the evaluation of the nominator of the voltage transmission T_{21}^v from the voltage source V_{s1} to the voltage V_2 across the tree branch Z_2 are given in Table 2.

Finally, from formula (2a) we obtain:

$$T_{21}^v = \frac{-Z_2Y_{46} - Z_1Z_2Y_4Y_6 + Z_1Z_2Y_{46}Y_{64} + Z_2Z_3Y_5Y_6 - Z_2Z_3Y_5Y_{46} + Z_2Z_3Y_6Y_{45}}{\Delta} \tag{3a}$$

where the denominator Δ is the same as in [20].

All possible combinations for the evaluation of the nominator of the current transmission T_{52}^i from the current source I_{s2} to the voltage I_5 throw the cotree branch Y_5 are given in Table 3.

Finally, from formula (2b) we obtain:

$$T_{52}^i = \frac{Z_3Y_5 + Z_1Z_3Y_4Y_5 + Z_2Z_3Y_4Y_5 + Z_1Z_3Y_5Y_6 - Z_1Z_3Y_5Y_{46} - Z_2Z_3Y_5Y_{46} - Z_1Z_3Y_5Y_{64}}{\Delta} \tag{3b}$$

where the denominator Δ is the same as in [20].

Table 2 Combinations for the evaluation of the nominator of the voltage transmission from V_{s1} to V_2 across the tree branch Z_2

k	$\begin{pmatrix} i'_m s \\ j'_m s \end{pmatrix}$	P_k^{vs}	P_k^i	det P_k^{vs}	$detP_k^i$	Product
1	$\begin{pmatrix} 2 \\ 6 \end{pmatrix}$	1	0	1	0	0
2	$\begin{pmatrix} 2 \\ 46 \end{pmatrix}$	1	−1	1	−1	$-Z_2Y_{46}$
2	$\begin{bmatrix} 1 & 2 \\ 4 & 6 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 \\ -1 & 0 \end{bmatrix}$	1	−1	$-Z_1Z_2Y_4Y_6$
2	$\begin{bmatrix} 1 & 2 \\ 4 & 46 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 \\ -1 & -1 \end{bmatrix}$	1	0	0
2	$\begin{bmatrix} 1 & 2 \\ 5 & 6 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix}$	0	−1	0
2	$\begin{bmatrix} 1 & 2 \\ 5 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix}$	0	1	0
2	$\begin{bmatrix} 1 & 2 \\ 6 & 45 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 \\ 1 & 0 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 \\ 0 & -1 \end{bmatrix}$	0	1	0
2	$\begin{bmatrix} 1 & 2 \\ 6 & 46 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 \\ 0 & -1 \end{bmatrix}$	0	1	0
2	$\begin{bmatrix} 1 & 2 \\ 6 & 64 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 \\ 1 & 0 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 \\ 0 & 0 \end{bmatrix}$	−1	0	0
2	$\begin{bmatrix} 1 & 2 \\ 46 & 64 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 \\ 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 \\ -1 & 0 \end{bmatrix}$	−1	−1	$Z_1Z_2Y_{46}Y_{64}$
2	$\begin{bmatrix} 2 & 3 \\ 4 & 6 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix}$	0	−1	0
2	$\begin{bmatrix} 2 & 3 \\ 4 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 \\ 0 & 0 \end{bmatrix}$	0	0	0
2	$\begin{bmatrix} 2 & 3 \\ 5 & 6 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 \\ 1 & 1 \end{bmatrix}$	−1	−1	$Z_2Z_3Y_5Y_6$
2	$\begin{bmatrix} 2 & 3 \\ 5 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 \\ 1 & 0 \end{bmatrix}$	−1	1	$-Z_2Z_3Y_5Y_{46}$
2	$\begin{bmatrix} 2 & 3 \\ 6 & 45 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$	1	1	$Z_2Z_3Y_6Y_{45}$
2	$\begin{bmatrix} 2 & 3 \\ 6 & 46 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$	0	1	0
2	$\begin{bmatrix} 2 & 3 \\ 6 & 64 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix}$	0	0	0
2	$\begin{bmatrix} 2 & 3 \\ 45 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 \\ 0 & 0 \end{bmatrix}$	−1	0	0

(continued)

Table 2 (continued)

k	$\begin{pmatrix} i'_m s \\ j'_m s \end{pmatrix}$	P_k^{vs}	P_k^i	det P_k^{vs}	$detP_k^i$	Product
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 5 & 6 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & -1 \\ 0 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & -1 \\ -1 & -1 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	−1	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 5 & 46 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & -1 \\ 0 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 1 \\ -1 & -1 & -1 \\ 0 & 1 & 0 \end{bmatrix}$	−1	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 6 & 45 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & -1 \\ -1 & 0 & -1 \\ 0 & 1 & 0 \end{bmatrix}$	1	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 6 & 46 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & -1 \\ 0 & 1 & 1 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & 1 \\ -1 & 0 & -1 \\ 0 & 1 & 0 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 6 & 64 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & -1 \\ -1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 45 & 46 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & -1 \\ 0 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & 1 \\ -1 & -1 & -1 \\ 0 & 0 & 0 \end{bmatrix}$	−1	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 46 & 64 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & -1 \\ -1 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 6 & 45 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & 0 \\ 0 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & 1 \\ -1 & 0 & -1 \\ 1 & 1 & 0 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 6 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & -1 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & 1 \\ -1 & 0 & -1 \\ 1 & 1 & 0 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 6 & 64 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & 1 \\ 0 & 1 & 0 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & -1 \\ -1 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix}$	−1	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 45 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & 1 \\ 1 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 & 1 \\ -1 & -1 & -1 \\ 1 & 0 & 0 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 46 & 64 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & 1 \\ 0 & 1 & 0 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 & -1 \\ -1 & -1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	−1	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 6 & 45 & 46 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 & -1 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 & 1 \\ 0 & -1 & -1 \\ 1 & 0 & 0 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 6 & 45 & 64 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 & 1 \\ 1 & 0 & 0 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 & -1 \\ 0 & -1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	1	0	0

(continued)

Table 2 (continued)

k	$\begin{pmatrix} i'_m s \\ j'_m s \end{pmatrix}$	P_k^{vs}	P_k^i	$\det P_k^{vs}$	$detP_k^i$	Product
3	$\begin{bmatrix} 1 & 2 & 3 \\ 6 & 46 & 64 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 & -1 \\ 0 & -1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 45 & 46 & 64 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & 1 \\ 0 & 1 & 0 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & -1 \\ -1 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	−1	0	0

Table 3 Combinations for the evaluation of the nominator of the current transmission from I_{s2} to I_5 throw the cotree branch Y_5

k	$\begin{pmatrix} i'_m s \\ j'_m s \end{pmatrix}$	P_k^v	P_k^{is}	$\det P_k^v$	$detP_k^{is}$	Product
1	$\begin{pmatrix} 3 \\ 5 \end{pmatrix}$	1	−1	1	−1	$-Z_3Y_5$
2	$\begin{bmatrix} 1 & 3 \\ 4 & 5 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$	1	−1	$-Z_1Z_3Y_4Y_5$
2	$\begin{bmatrix} 1 & 3 \\ 5 & 6 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ -1 & 1 \end{bmatrix}$	1	−1	$-Z_1Z_3Y_5Y_6$
2	$\begin{bmatrix} 1 & 3 \\ 5 & 45 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$	0	1	0
2	$\begin{bmatrix} 1 & 3 \\ 5 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$	1	1	$Z_1Z_3Y_5Y_{46}$
2	$\begin{bmatrix} 1 & 3 \\ 5 & 64 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ -1 & 1 \end{bmatrix}$	−1	−1	$Z_1Z_3Y_5Y_{64}$
2	$\begin{bmatrix} 2 & 3 \\ 4 & 5 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}$	−1	1	$-Z_2Z_3Y_4Y_5$
2	$\begin{bmatrix} 2 & 3 \\ 5 & 6 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ -1 & 1 \end{bmatrix}$	−1	0	0
2	$\begin{bmatrix} 2 & 3 \\ 5 & 45 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$	0	1	0
2	$\begin{bmatrix} 2 & 3 \\ 5 & 46 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 \\ 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix}$	−1	−1	$Z_2Z_3Y_5Y_{46}$
2	$\begin{bmatrix} 2 & 3 \\ 5 & 64 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 \\ 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ -1 & 1 \end{bmatrix}$	1	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 5 & 6 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & -1 \\ -1 & -1 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & -1 \\ -1 & 0 & 0 \\ 0 & -1 & 1 \end{bmatrix}$	0	−1	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 5 & 45 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 0 \\ -1 & -1 & -1 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 1 \\ -1 & 0 & -1 \\ 0 & -1 & 0 \end{bmatrix}$	0	0	0

(continued)

Table 3 (continued)

k	$\begin{pmatrix} i'_m s \\ j'_m s \end{pmatrix}$	P_k^v	P_k^{is}	$\det P_k^v$	$detP_k^{is}$	Product
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 5 & 46 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & -1 \\ -1 & -1 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 1 \\ -1 & 0 & -1 \\ 0 & -1 & 0 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 5 & 64 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & 1 \\ -1 & -1 & -1 \\ 0 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & -1 \\ -1 & 0 & 0 \\ 0 & -1 & 1 \end{bmatrix}$	0	−1	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 6 & 45 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 0 \\ -1 & -1 & -1 \\ 1 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & 1 \\ 0 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix}$	0	−1	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 6 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & -1 \\ -1 & -1 & 0 \\ 1 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & 1 \\ -1 & -1 & -1 \\ 0 & 0 & 0 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 6 & 64 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 1 \\ -1 & -1 & -1 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & -1 \\ -1 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 45 & 46 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & -1 \\ -1 & -1 & 0 \\ 1 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 & 1 \\ -1 & -1 & -1 \\ 1 & 0 & 0 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 45 & 64 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 1 \\ -1 & -1 & -1 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 & -1 \\ -1 & -1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	0	0	0
3	$\begin{bmatrix} 1 & 2 & 3 \\ 5 & 46 & 64 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & 1 \\ -1 & 0 & -1 \\ 1 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 & -1 \\ -1 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix}$	0	0	0

3 Two-Graph Models of Nullors and Mirrors

In order to deal with circuits containing nullors and mirrors, it is necessary to employ a network formalism which can be applied to all varieties of linear networks.

An analysis method for circuits with nullors was first proposed by Carlin [23], and it was very well explained by Bruton [24]. These earlier works are based on the use of nodal equations. Many efforts have been made to improve this method. One formulation based on indefinite admittance matrices that leads to a simpler procedure was described by Lin in [16]. This procedure has overcome the problem related to the fact that one end of a norator (or a nullator) must be connected to the reference node. However, this method makes the matrix reduction process more complex by manipulating and deleting one column and one row for each nullator and norator, respectively. Another method uses the modified nodal approach (MNA), in which additional columns and rows are incorporated into the standard admittance matrix [16, 25]. However, for the MNA, the dimensions of the matrix and the basis for the

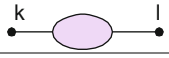
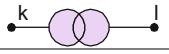
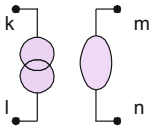
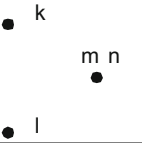
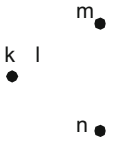
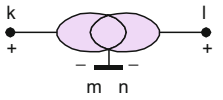
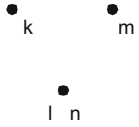
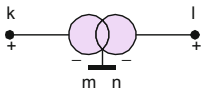
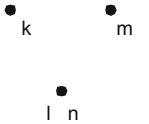
representation are dependent on the type of elements contained in the circuit. This problem does not exist in the method which uses the nodal admittance matrix (NAM), as the dimensions of this matrix are determined by the number of nodes in the circuit, but the problem of infinite matrix elements, such as for nullors, remains. A symbolic representation of a nullor in a circuit in the NAM has recently been proposed using a form of a limit variable, called an infinity-variable, or ∞-variable [26, 27]. The NAM may be then transformed into a port matrix by a process of matrix reduction and the transfer function may be obtained from the port matrix. Although the NAM improves the MNA, it creates a complex matrix reduction process by manipulating and deleting columns and rows. To improve the computation of fully symbolic expression in analog circuits with nullors, other methods have been proposed in [28–31]. These methods use standard nodal analysis, and according to the nullor properties, the corresponding procedure adds or substrates the values of the appropriate columns or rows to generate the final nodal matrix. Next, by applying Laplace expansion it is possible to calculate the transfer functions. These methods are universal, because they allow the analysis of fully differential active devices [29] and are relatively simple, but they suffer from the well-known limitations of the nodal analysis technique, i.e. it is possible to directly handle only voltage-controlled current sources and independent current sources. The other controlled sources and voltage independent sources must be modeled by equivalent circuits. Additionally, when coefficients of the NAM or modified nodal matrix have different weights, which is the most general case in the analysis of active networks, then the *Laplace* expansion of any determinant or cofactor will generate the cancellation terms [16]. Thus, even in the new formulation method using pathological element based active device models that is proposed in [28], the number of cancellation terms is just curtailed, and not reduced to zero.

Nowadays two methods of computation the network functions for the circuits with nullors and mirrors [12, 14] without the excess terms were presented. One of these methods is based on the generalized parameter extraction method [12] and the second on the topological two-graph method [14]. In this work we propose a novel technique that is semi-topological and is based on the two-graph method [17]. Basically, the two-graph method consists of constructing a voltage graph G_V and a current graph G_I. Actually, G_V and G_I constructed from an inspection of the circuit in which nullators and mirrors are replaced by appropriate two-graph stamps (see Table 4).

3.1 Two-Graph Stamps of Nullators and Mirrors

A nullator is defined as having its voltage and current simultaneously equal to zero. A norator has an arbitrary voltage and current. The models of nullator and norator have their representation in the current and voltage graph [32], the so called two-graph ‘stamps’, shown in Table 4.

Table 4 Two-graph stamps for norators and mirrors

	Symbol	I-Graph	V-Graph
Nullator			
Norator			
Nullor			
V-mirror			
I-mirror			

The voltage mirror imposes two constraints on its voltage and current, $V_k = V_m =$ arbitrary [33, 34] and $I_k = I_m = 0$, then the voltage mirror may be represented in the circuit for deriving KVL and in the circuit for deriving KCL by two different equivalent circuits. The nodes k and l may be considered as equipotential. So, we can shortcut the nodes k and m and introduce a new node k,m in the circuit for calculating KVL. Of course, for the calculation of KCL, we have two nodes k and m (see Table 4).

The current mirror imposes two constraints on its voltage and current, V_k, $V_m =$ arbitrary and $I_k = -I_m =$ arbitrary [33, 34] than the current mirror may be represented in the circuit for deriving KVL and in the circuit for deriving KCL by two different equivalent circuits. So, because of the fact that the currents in nodes k and m are the same, we can shortcut the nodes k and m and introduce new node k, m in the circuit for the calculation of KCL. Of course, for the calculation of KVL we have two nodes k and m (see Table 4).

Therefore, if we have circuits with norators, mirrors and controlled sources, than we have to calculated the fundamental loop and cutset matrices on the base two different graphs.

3.2 Examples

3.2.1 The ICCII+-Base Inverting Low-Pass Filter

To illustrate the method of formulation of the network functions for linear, analog circuits with mirrors, consider the ICCII+-based inverting low-pass filter (see Fig. 3). This example is taken from [11, (Fig. 8a)]. The mirror-based circuit is

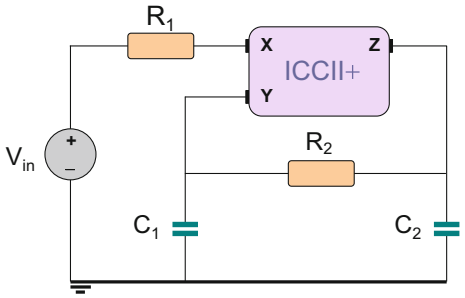


Fig. 3 The ICCII+-base inverting low-pass filter

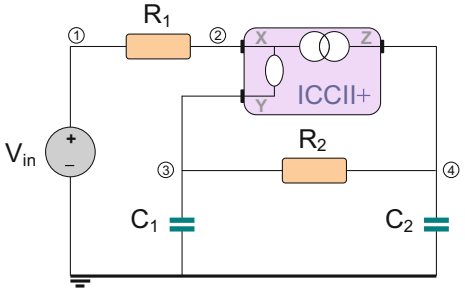


Fig. 4 The mirror-based circuit of the ICCII+-base inverting low-pass filter

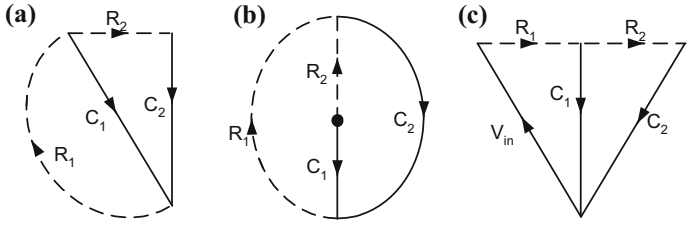


Fig. 5 The graphs of the circuit: **a** the cold voltage graph (G^v), **b** the cold current graph (G^i), **c** the voltage graph with the independent voltage source (G^{vs})

shown in Fig. 4. (In this Figure we do not use an equivalent circuit for the independent voltage source as it was done in [11, Fig. 8c] because in the proposed method we can use both independent voltage sources as independent current sources). If we use the two-graph stamps for the mirrors (given in Table 4), we can draw the voltage (G^v) and the current (G^i) cold graphs (see Fig. 5, where the cold graph means the graph with all the independent sources removed) [17]. Additionally, we draw the voltage graph (G^{vs}) with the independent voltage source [22].

On the basis of Fig. 5 we can directly obtain the product matrices $P^v = Q_{La}$, and $P^i = Q_{Lb}$, where Q_{Lx} ($x = a, b$ denote the graphs from Fig. 5a, b) is the submatrix of the fundamental cutset matrix $Q_f = [I_r\ Q_L]$ and P^{vs} is the V-substituted Voltage Product Matrix.

P^v =		$Y_1 = G_1$	$Y_2 = G_2$
	$Z_1 = 1/sC_1$	−1	1
	$Z_2 = 1/sC_2$	0	−1

P^i =		$Y_1 = G_1$	$Y_2 = G_2$
	$Z_1 = 1/sC_1$	0	1
	$Z_2 = 1/sC_2$	−1	−1

P^{vs} =		$Y_1 = G_1$	$Y_2 = G_2$
	$Z_1 = 1/sC_1$	−1	0
	$Z_2 = 1/sC_2$	0	−1

All the possible combinations for evaluation of the nominator of the voltage transmission from the voltage source V_{sp} to the voltage V_q across the tree branch $Z_1 = 1/sC_1$ are given in Table 5.

All the possible combinations for evaluation of the denominator of the voltage transmission from the voltage source V_{sp} to the voltage V_q across the tree branch $Z_1 = 1/sC_1$ are given in Table 6.

Table 5 Combinations for evaluation of the nominator of the voltage transmission from V_{sp} to the V_q across the tree branch

k	$\begin{pmatrix} i_q \\ j_q \end{pmatrix}$	P_k^{vs}	P_k^i	det P_k^{vs}	$detP_k^i$	Product
1	$\begin{pmatrix} 1 \\ 1 \end{pmatrix}$	−1	0	−1	0	0
1	$\begin{pmatrix} 1 \\ 2 \end{pmatrix}$	0	1	0	1	0
2	$\begin{bmatrix} 1 & 2 \\ 1 & 2 \end{bmatrix}$	$\begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix}$	1	1	$G_1G_2/(s^2C_1C_2)$

Table 6 Possible combinations for evaluation of the denominator of the voltage transmission from V_{sp} to V_q across the tree branch

k	$\begin{pmatrix} i_q \\ j_q \end{pmatrix}$	P_k^v	P_k^i	$\det P_k^v$	$detP_k^i$	Product
1	$\begin{pmatrix} 1 \\ 1 \end{pmatrix}$	-1	0	-1	0	0
1	$\begin{pmatrix} 1 \\ 2 \end{pmatrix}$	1	1	1	1	G_2/sC_1
1	$\begin{pmatrix} 2 \\ 1 \end{pmatrix}$	0	-1	0	-1	0
1	$\begin{pmatrix} 2 \\ 2 \end{pmatrix}$	-1	-1	-1	-1	G_2/sC_2
2	$\begin{bmatrix} 1 & 2 \\ 1 & 2 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 \\ 0 & -1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix}$	1	1	$G_1G_2/(s^2C_1C_2)$

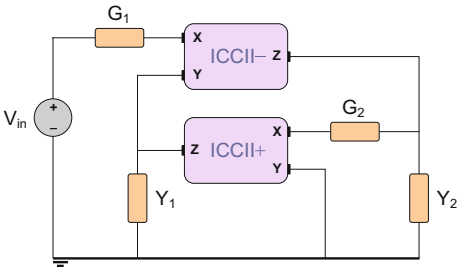


Fig. 6 ICCII-based voltage mode filter

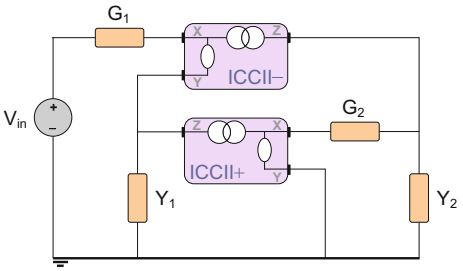


Fig. 7 An equivalent circuit of the ICCII-based voltage mode filter

Finally, we obtain from formula (2a)

$$T_{C1,In}^v = \frac{G_1G_2/(s^2C_1C_2)}{1 + G_2/sC_1 + G_2/(sC_2) + G_1G_2/(s^2C_1C_2)} = \frac{1}{s^2C_1C_2R_1R_2 + s(C_1 + C_2)R_1 + 1} \tag{4}$$

And this result is the same as in [11].

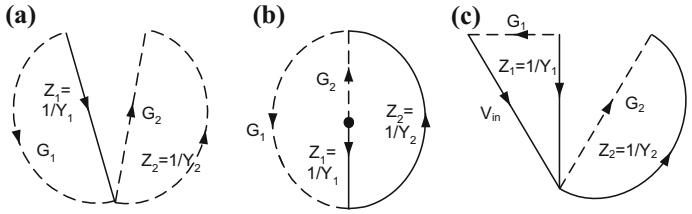


Fig. 8 The graphs of the circuit: **a** the cold voltage graph ($G^{v)}$, **b** the cold current graph (G^{i}), the voltage graph with the independent voltage source (G^{vs})

3.2.2 The Filter with Second Generation Current Conveyor

The next example presents a filter with a second generation current conveyor (see Fig. 6). This circuit is borrowed from [14, (Fig. 9)], which also was used in [11, 13, 35]. It is composed of two ICC (second generation current conveyor) blocks, a positive type (ICCII+) and a negative type (ICCII−). An equivalent circuit is shown in Fig. 7. If we use the two-graph stamps for the mirrors (Table 6), we can draw (Fig. 8) the voltage (G^{v}) and current (G^{i}) cold graphs. Additionally, we draw the voltage graph (G^{vs}) with the independent voltage source.

If we use the two-graph stamps for the mirrors (Table 4), we can draw (Fig. 8) the voltage (G^{v}) and current (G^{i}) cold graphs (where the cold graph means the graph with all the independent sources removed) [17]. Additionally, we draw the voltage graph (G^{vs}) with the independent source [22].

On the basis of Fig. 8 we can obtain directly the product matrices: $P^{v} = Q_{La}$, $P^{i} = Q_{Lb}$, where Q_{Lx} ($x = a, b$ denote the graphs from Fig. 8a, b) is the submatrix of the fundamental cutset matrix $Q_f = [I_r\ Q_L]$, and P^{vs} is the V-substituted Voltage Product Matrix.

P^{v} =		G_1	G_2
	$Z_1 = 1/Y_1$	1	0
	$Z_2 = 1/Y_2$	0	1

P^{i} =		G_1	G_2
	$Z_1 = 1/Y_1$	0	1
	$Z_2 = 1/Y_2$	−1	1

P^{vs} =		G_1	G_2
	$Z_1 = 1/sC_1$	1	0
	$Z_2 = 1/sC_2$	0	1

All the possible combinations for evaluation of the nominator of the voltage transmission from the voltage source V_{sp} to the voltage V_q across the tree branch $Z_2 = 1/Y_2$ are given in Table 7.

Table 7 Combinations for evaluation of the nominator of the voltage transmission from the voltage source V_{sp} to the voltage V_q across the tree branch Z_2

k	$\begin{pmatrix} i_q \\ j_q \end{pmatrix}$	P_k^{vs}	P_k^i	det P_k^{vs}	$detP_k^i$	Product
1	$\begin{pmatrix} 1 \\ 1 \end{pmatrix}$	1	0	1	0	0
1	$\begin{pmatrix} 1 \\ 2 \end{pmatrix}$	0	1	0	1	0
2	$\begin{bmatrix} 1 & 2 \\ 1 & 2 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & 1 \end{bmatrix}$	1	1	$G_1G_2Z_1Z_2$

All the possible combinations for evaluation of the denominator of the voltage transmission from the voltage source V_{sp} to the voltage V_q across the tree branch $Z_2 = 1/Y_2$ are given in Table 8.

Finally, from formula (2a) we obtain:

$$T_{Z,In}^{v} = \frac{G_1 Z_2}{1 + G_2 Z_2 + G_1 G_2 Z_1 Z_2} = \frac{G_1 Y_1}{Y_1 Y_2 + Y_1 G_2 + G_1 G_2} \tag{5}$$

this result is the same as in [14].

Table 8 Combinations for evaluation of the denominator of the voltage transmission from V_{sp} to V_q across the tree branch

k	$\begin{pmatrix} i_q \\ j_q \end{pmatrix}$	P_k^{v}	P_k^i	det P_k^{v}	$detP_k^i$	Product
1	$\begin{pmatrix} 1 \\ 1 \end{pmatrix}$	1	0	1	0	0
1	$\begin{pmatrix} 1 \\ 2 \end{pmatrix}$	0	1	0	1	0
1	$\begin{pmatrix} 2 \\ 1 \end{pmatrix}$	0	−1	0	−1	0
1	$\begin{pmatrix} 2 \\ 2 \end{pmatrix}$	1	1	1	1	G_2Z_2
2	$\begin{bmatrix} 1 & 2 \\ 1 & 2 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & 1 \end{bmatrix}$	1	1	$G_1G_2Z_1Z_2$

4 Conclusions

In this chapter, we proposed a method for analysis of liner circuits with RLC elements, all type of controlled sources, nullors-mirrors circuits, i.e. the circuits without the replacing the mirror elements with their nullor equivalents. It is based on the two-graph representation of these elements and semi-topological procedure of calculations of the network functions. The procedure of calculations is based on the product matrices and a numerical formula for the evaluation of unimodular determinants. The evaluating procedure is systematic, purely numerical and no sign rule is required. The formulas do not hold the terms that can be canceled and no extra attention is required for canceling terms.

In this chapter we advocate the symbolic analysis because symbolic expressions give good insight on the behavior of the circuit and can also be used in optimization procedures.

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Circuit Analyses with Nullors

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Abstract This chapter describes the nullor-based modelling of active devices from the circuit level of abstraction. After a brief overview on the nullor concept and its properties, the modelling of active devices not only at the voltage-mode but also at the current-mode and the mixed-mode of operation from two-port and four-terminal network point of view are described in details. The circuit analysis with nullors and the topological approach for transfer function generation by two-graph tree enumeration as well are presented. The generalized topological formula with homogeneous parameters is proved for all the circuit functions, and a simple representation of the four types of controlled sources by admittances is proposed, that allows a uniform treatment of the entire circuit in terms of admittances. In order to implement the procedure, the rules to automatically generate the two graphs and to enumerate the common spanning trees are presented. Some simplifications in the circuit and in the two graph structure before tree generation and a graph representation on levels, improve the efficiency of the tree enumeration procedure. The original approach, in which each edge is labelled with an admittance term, could handle only one type of active element, namely VCCS (voltage controlled current source), but the method was further developed by many researchers for general linear circuits to include virtually all active elements. Some techniques to convert the CCVSs (current controlled voltage sources), VCVSs (voltage controlled voltage sources) and CCCSs (current controlled current sources) in equivalent schemes containing only VCCSs together with admittances and the inductance modelling proposed in the literature are discussed.

1 Introduction

According to the symbolic analysis principles, the Nodal Analysis Method (NAM) is restrictive because the admittance matrix must contain only the elements compatible with the Nodal Analysis (NA). The problem can be easily resolved

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through the Modified Nodal Analysis Method (MNAM), adding a row and a column for each element which is not compatible with the classic Nodal Analysis Method [1–7]. One of the problems generated by this kind of approach is related to the size of the admittance matrix. This matrix will become bigger, according to the structure of the circuit and types of its elements.

Regarding the models to be used in the analogue circuit analysis, the requirement of a high accuracy could lead to complicated calculations and then compact models are preferred mainly for the use of much more simple equations [3–7]. These models are more effective for the optimization of design and simulation time during the analysis process. From this point of view, the nullors proved already their efficiency in the active devices modelling. In the models based on nullors, the parasitic elements can be included to analyze their contribution to the analogue circuit response. All the four controlled sources can also be represented with equivalent circuits using nullor elements. Consequently, the nullors are very useful for the analogue circuits modelling because the circuit topology can be described using only two-terminal components like resistors, capacitors, nullators, norators, independent and controlled sources. Considering that the model should be developed in the simplest manner and the accuracy of the circuit behaviour simulation must be in acceptable limits, this chapter will show the problems related to the small-signal models of the active devices modelled with nullors.

The nullator is an ideal circuit with two terminals (Table 2.1a), which is characterized by null values for the current and voltage at the terminals. It has two equations: $i = 0$, $v = 0$.

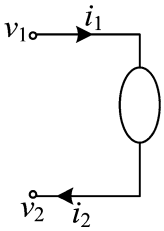
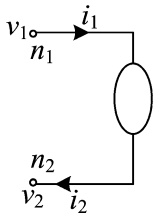
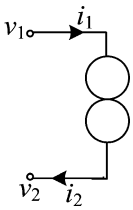
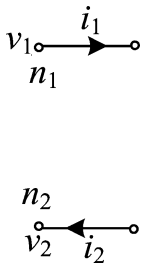
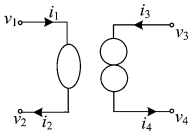
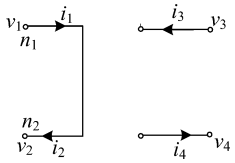
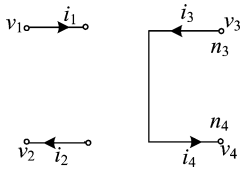
The norator is an ideal circuit with two terminals (Table 1b), which is characterized by random values for the current (i) and voltage (v) at the terminals. In other words, the norator does not have any equation. The current and the voltage values of this element are affected only by the external circuit connected to its terminals.

These two circuit elements can be used only in norator-nullator pairs called nullors (Table 1c), which has the number of equations equal to the number of gates. The nullor can be considered as an idealized operational amplifier, which has at the input gate null voltage and current and at the output gate an undetermined voltage and current (obtained by multiplying the null inputs by an infinite factor gain). In Fig. 1d, e is presented the symbol for the current (voltage) mirror.

Techniques for the analysis of linear/linearized circuit have been performed using the nullator and norator as theoretical active devices, [6–14]. Tellegen was the first who presented the ideal operational amplifier theory and later, in 1964, Carlin considered nullators and norators as single active devices in the circuit analysis—called nullor [5]. He thought that these active devices cannot be built physically. Tellegen also took in consideration that these devices must be seen only as mathematical models without any physical support. Table 1 presents the behaviour of the nullators, norators and nullors from the point of view of the voltage, respectively of the current, in G^v—the voltage graph and, respectively G^i—the current graph, [1–9].

The input port of the nullor is modelled by the nullator which is characterized by two equations:

Table 1 The behaviour of the nullators, norators and nullors

Symbol	Definitions	Voltage graph G^v	Current graph G^i
 Nullator (a)	$v_1 = v_2$ $i_1 = i_2 = 0$	 $v_1 = v_2 \Rightarrow n_1 \equiv n_2$ any $i_1 = i_2$	 any v_1, v_2 $i_1 = i_2 = 0$
 Norator (b)	any v_1, v_2 any $i_1 = i_2$	 any v_1, v_2 $i_1 = i_2 = 0$	 $v_1 = v_2 \Rightarrow n_1 \equiv n_2$ any $i_1 = i_2$
 Nullor (c)	$i_1 = i_2 = 0$ $v_1 = v_2$ any v_3, v_4 any $i_3 = i_4$	 $v_1 = v_2 =$ arbitrary $\Rightarrow n_1 \equiv n_2$, any $i_1 = i_2$, $i_3 = i_4 = 0$, any $v_3 \neq v_4$	 any $v_1 \neq v_2$ v_1, $i_1 = i_2 = 0$; $v_3 = v_4 \Rightarrow n_3 \equiv n_4$ any $i_3 = i_4$

$$v_1 = v_2 = \text{arbitrary},\ i_1 = i_2 = 0. \tag{1}$$

So, the nullator is simultaneously an open-circuit in G^i current graph and a short-circuit in G^v voltage graph. The output port of the nullor is modelled by the norator where both, the voltage and the current have arbitrary values:

$$v_1 \neq v_2 = \text{arbitrary},\ i_1 = i_2 = \text{arbitrary} \tag{2}$$

With these properties the nullor is a two-port element accepted as a universal active element [1–16, 30–34]. This concept means that the nullor along with capacitors and resistors can be used to design a maximum number of functions with the minimum number of active devices. If a suitable set of linear and nonlinear

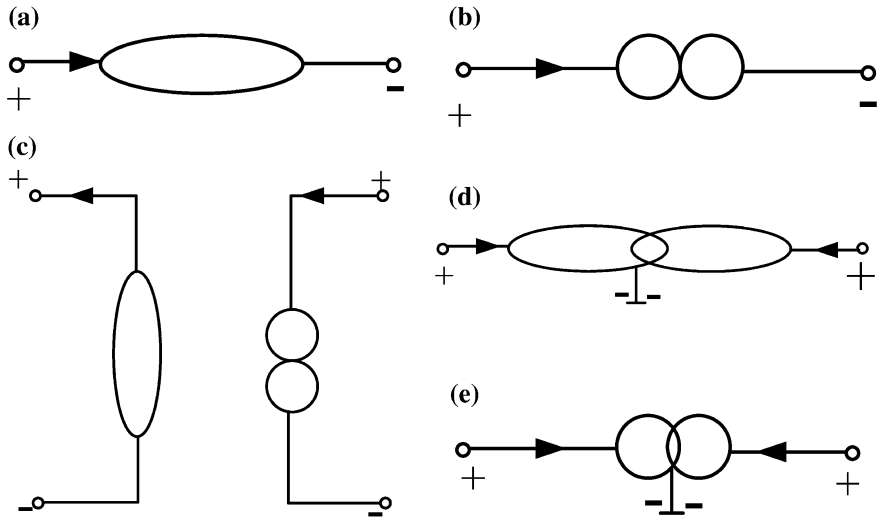


Fig. 1 **a** Nullator symbol; **b** Norator symbol; **c** Nullor symbol; **d** Current mirror; **e** Voltage mirror

passive elements is available, then no active element other than nullors are needed to implement any linear or nonlinear circuit function. So nullators, norators, resistances, along with capacitances can synthesize a complete set of linear or linearized equations.

2 Nullor Equivalences

From the beginning, the nullor circuit has been considered very efficient for the analog circuit analysis, modelling and synthesis. Therefore, there are many records regarding methods and algorithms based on nullor circuits, used for the active devices analysis and modelling [19–34]. Because any analog network can be modelled with nullators, norators and impedances, it is useful to mention the equivalence between some connections. These are shown in Fig. 2. For instance, in Fig. 2a, a current cannot flow from a to b since the current through the nullator is zero, so a series connection of the nullator and norator is equivalent to an open-circuit. In Fig. 2b, the current can flow from a to b through the norator, also the voltage across a and b becomes zero according to the property of the nullator, so a parallel connection of the nullator and norator is equivalent to a short-circuit. The remaining connections have equivalences according to the nullator and norator $i-v$ characteristics.

In another approach, the nullors along with grounded resistors can be manipulated in order to obtain inverting properties, features that the nullator and the norator

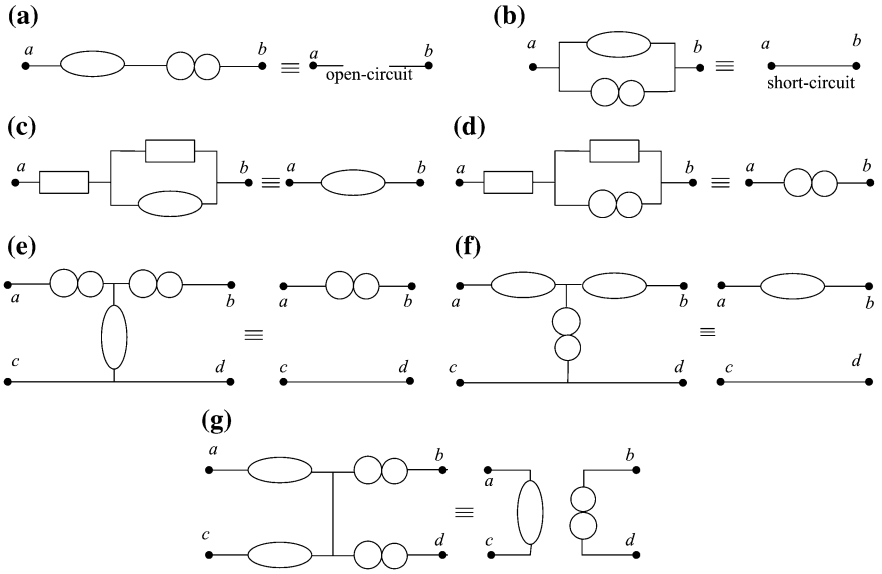


Fig. 2 Nullator and norator equivalences

cannot model by themselves [30, 31]. The main purpose of the introduction of the inverting properties is that the behaviour of some active devices involves inverting the voltage and current input-signals. In this sense, the Current-Mirror (CM) and the Voltage-Mirror (VM), both as active devices, can perform this task and their behaviour also should be modelled with nullors, [30–34]. Thus, by manipulating the nullor along with grounded resistors, the behaviour of a CM or of a VM, both with ideal unity-gain can easily be obtained, as shown in Fig. 3, [1].

Therefore, by analyzing the equivalent circuits, one can see that the VM, shown in Fig. 3a, is characterized by:

$$v_2 = -v_1 = \text{ arbitrary}, \; i_1 = i_2 = 0. \tag{3}$$

and the CM, shown in Fig. 2b, is characterized by:

$$v_2 \neq v_1 = \text{arbitrary}, \; i_1 = i_2 = \text{arbitrary} \tag{4}$$

At the end, the inverting behaviour of the nullator and norator is achieved. In [24, 31, 32], the nullor—based models of the VM and CM include parasitic elements. In the same manner as for the nullor, equivalences between the combinations of nullators, norators, CMs, VMs and impedances can be obtained. Note, however, that if v_1 or v_2 terminal from Fig. 3a is grounded and by applying the equivalences shown in Fig. 1, the VM is reduced to a nullator. In the same manner, if any terminal in Fig. 3b is grounded by applying the equivalences shown in Fig. 2, then a norator is obtained.

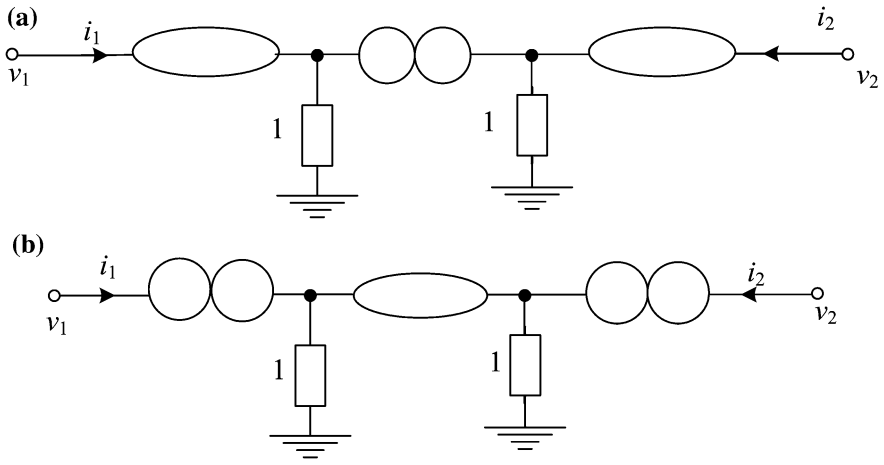


Fig. 3 Nullor and grounded resistor-based VM (**a**) and CM (**b**)

3 Loop Current Method for Circuits with Nullors

As it is well-known, the loop current method is based on introducing the loop currents as intermediary quantities which satisfy the first Kirchhoff's current law (KCL) and which can be determined by applying the Kirchhoff's voltage law (KVL) on the independent loops of the electric circuit.

Taking into account the definition of the nullator as a circuit element through which the current does not flow, it is useful and recommended to choose loop currents such that they do not flow through the branches that contain nullators. In order to respect such a condition, the branches containing the nullators should be eliminated by introducing an open-circuit between the terminals at which a nullator is connected. This leads to a decrease of the number of independent loops (l_i) with the nullator number (n_n)

$$l_i = b - n + 1 - n_n, \tag{5}$$

where: b—is the number of the circuit branches and n—is the number of the circuit nodes.

Applying KVL on the independent loops l_i a system of independent equations results from which we further can determine the loop currents.

The branch currents are expressed as an algebraic sum of the loop currents that flow through the respective branch.

If the electric circuit contains current sources, the branches which contain such sources cannot belong to a tree; a single loop current will be chosen to flow through such branch. The loop current value will be given by the source current.

In order that the system of l_i equations does not contain as unknowns the norator voltages, the l_i independent loops must not contain branches with norators.

The norator branches are replaced by open-circuits while the branches with nullators are kept.

The loop current equations corresponding to a number of l_i loops become:

$$\sum_{j=1}^{l_i}\left(\sum_{h\in[l_j]\cap[l_k]} R_h\right) I_{l_j} = \sum_{h\in[l_k]} E_h, \tag{6}$$

where: I_{l_j}—is the loop current corresponding to the l_j loop and E_h—is the *e.m.f* of b_h branch.

If we consider the current and voltage graphs with their loop-branch incidence matrices $\mathbf{B}^i$ and $\mathbf{B}^v$(see Table 1), then the matrix form of the loop current equations, [7, 9–14], can be written as follows:

$$\left(B^v R_b \left(B^i\right)^t\right) I_b^i = B^v (E_b + R_b J_b), \tag{7}$$

where, for example, $\mathbf{I}_b^i$ ($\boldsymbol{R}_b$) is the loop current vector in the current graph G^i (the diagonal matrix of the branch resistances).

Example 1 See (Figs. 4 and 5).

The loop current equations are obtained by applying the KVL on the independent loops from the voltage graph (Fig. 6) and taking the currents from attached to the loops from the current graph (Fig. 5). Proceeding in this manner, it results the following system of Eqs. (8a) and (8b)

$$\begin{cases} R_3 \cdot I_{l_1} + R_5 \cdot I_{l_1} + R_4 \cdot I_{l_1} - R_5 \cdot I_{l_2} = 0 \\ R_5 \cdot I_{l_2} + R_2 \cdot I_{l_2} - R_5 \cdot I_{l_1} = -E_2 \end{cases}. \tag{8a, b}$$

From Eq. 8b it results:

$$I_{l_2} = \frac{-E_2 + J_1 \cdot R_5}{R_2 + R_5}. \tag{9}$$

From Eq. 8a it results:

$$I_{l_3} = \frac{-J_1 \cdot (R_3 + R_5) + R_5 \cdot \left(\frac{-E_2 + J_1 \cdot R_5}{R_2 + R_5}\right)}{R_4}. \tag{10}$$

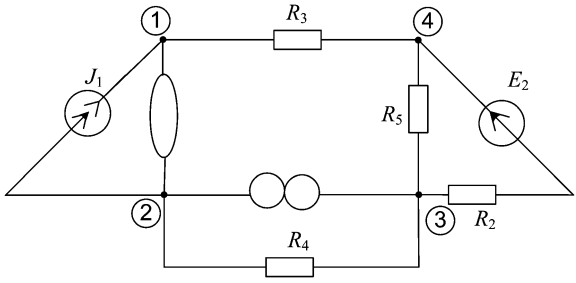


Fig. 4 Initial circuit to be analyzed using loop current method

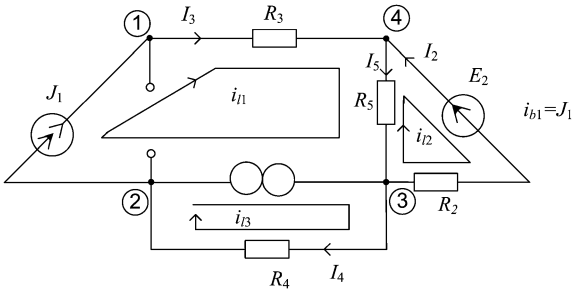


Fig. 5 Choosing of the loop currents

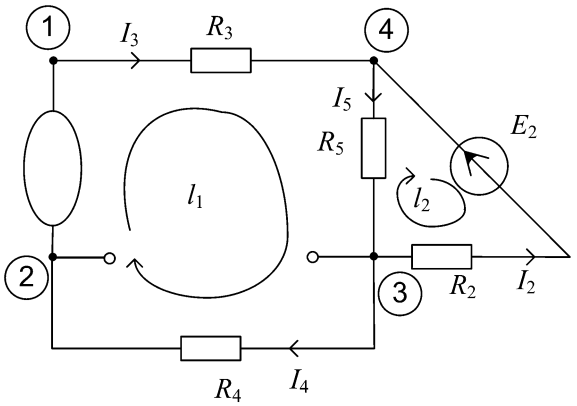


Fig. 6 Loops for KVL writing

4 Nodal Analysis Method for Circuits with Nullors

The unknown variables of this method are represented by the $n - 1$ electric potentials corresponding to the circuit nodes, excepting the nth node whose potential is the reference potential and it is considered to be zero. These unknowns satisfy KVL for any circuit loop. The computation of these unknowns is based on KCL written in $n - 1$ nodes and on the generalized Ohm's law to express each branch current depending on the node potentials.

The equations of the node potentials for the circuits containing nullators will have a different form taking into account that the voltage at the nullator terminals is equal to zero, which results in a decrease of the number of the unknown potentials (Fig. 7).

If the circuit contains norators, the norator currents should not be present in the system of equations. This is why we choose sections that do not include the branches with norators.

$$\sum_{j=1}^{N-1}\left(\sum_{h\in[l_j]\cap[l_k]} G_h\right)V_j = -\sum_{h\in[l_k]}\left(J_h + \frac{E_h}{R_h}\right). \tag{11}$$

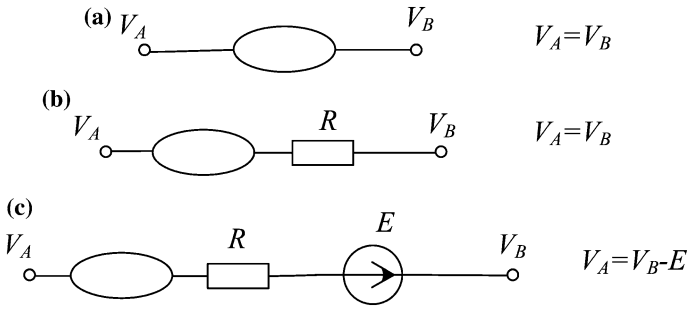


Fig. 7 The equations of the node potentials for the branches containing nullators

Considering the current and voltage graphs with their reduced node-branch incidence matrices $\mathbf{A}^i$ and $\mathbf{B}^v$(see Table 1) the matrix form of the nodal equations, [7, 9–14], is:

$$\left(\mathbf{A}^i\mathbf{G}_b(\mathbf{A}^v)^t\right)\mathbf{V}^v_{n-1} = -\mathbf{A}^i(\mathbf{G}_b\mathbf{E}_b + \mathbf{J}_b), \tag{12}$$

where, for example, $\mathbf{V}^v_{n-1}$ $(\boldsymbol{G}_b)$ is the potential vector of the $n-1$ independent nodes from the voltage graph G^v (the diagonal matrix of the branch conductances).

Example 2 The nodal analysis method for the circuits containing nullors can be applied as follows: KCT is written in the independent nodes of the current graph and there are used the potentials associated to the $n-1$ independent nodes from the voltage graph. Applying the Nodal analysis method, we obtain the following Eqs. (13)–(18) (Fig. 8):

Appling the KCL in the node (n_1) it results:

$$\frac{V_1}{R_3} = J_1. \tag{13}$$

According to the KCL on the cut-set (S_2) to obtain:

$$\frac{V_2}{R_5} + \frac{V_2}{R_2} = -J_1 - \frac{E_2}{R_2}. \tag{14}$$

From Eq. (13) it results:

$$V_1 = R_3 \cdot J_1. \tag{15}$$

From (14) we can obtain:

$$V_2 = \frac{R_5 \cdot R_2 \cdot \left(-J_1 - \frac{E_2}{R_2}\right)}{R_2 + R_5}, \tag{16}$$

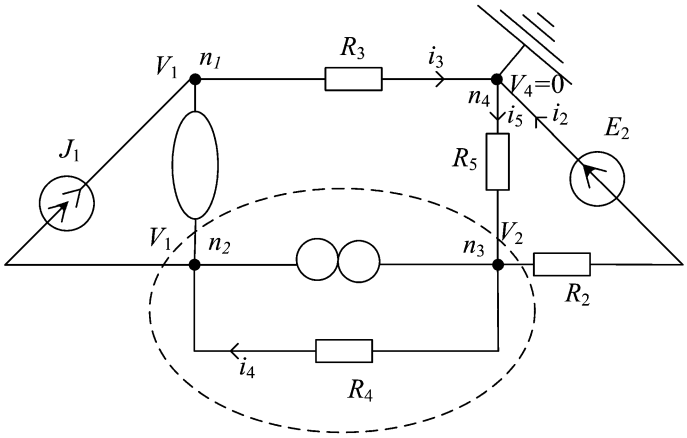


Fig. 8 Initial circuit to be analyzed using Nodal Analysis Method

$$I_4 = \frac{V_2 - V_1}{R_4} = \frac{\dfrac{R_5 \cdot R_2 \cdot \left(-J_1 - \frac{E_2}{R_2}\right)}{R_2 + R_5} - R_3 J_1}{R_4}, \tag{17}$$

$$I_2 = \frac{V_2 - V_4 + E_2}{R_2} = \frac{\dfrac{R_5 \cdot R_2 \cdot \left(-J_1 - \frac{E_2}{R_2}\right)}{R_2 + R_5} + E_2}{R_2}. \tag{18}$$

The values obtained for I_2 and I_4 are the same as those obtained by using the loop method.

5 The Generalized Topological Formula for Transfer Function Generation by Two-Graph Tree Enumeration

5.1 Introduction

One of the most important approaches for nonreciprocal circuit analysis is the two-graph tree enumeration method, mainly due to Mayeda and Seshu [16]. The original approach, in which each edge is labelled with an admittance term, could handle only one type of active element, namely VCCS, but the method was further developed by many researchers for general linear circuits to include virtually all active elements. In [17] some techniques to convert the CCVSs, VCVSs and CCCSs in equivalent schemes containing only VCCSs and admittances are introduced, and some techniques to model an inductance proposed in the literature are discussed. The resulted models have a bigger number of branches in the two graphs and some supplementary nodes are introduced in the original circuit. The method

based on a two-graph representation using a unity gyrator to model the non-admittance components was implemented [18] in order to obtain symbolic network function expressions in other terms than admittances. The price paid by all these approaches consists in the increase of the circuit complexity leading to a bigger number of common spanning trees.

Topological formulas for transfer functions of active networks using tree enumeration method have been derived firstly by Mayeda and Seshu, but their procedure for determining the sign factor is tedious. In [15] the main results in this direction up to that date are presented, and similar formulas are obtained while modelling all the controlled sources by equivalent schemes containing only two terminal elements and VCCSs. A sorting scheme is preferred to obtain symbolic network functions from the node determinant of an augmented network.

Based on the original concepts of the two-graph tree enumeration method a modelling technique of the four types of controlled sources has been elaborated and a topological formula with homogeneous parameters for the transfer admittance has been proved using the nodal approach [7]. Some innovative approaches to symbolic generation of the transfer functions have been developed: an algorithm using systematic loop opening and closing, a diakoptic approach, and a procedure based on graph decomposition on levels [7–14].

In this chapter, a set of rules for generating and using the two graphs is stated, and the generalization of the topological formula to generate all network functions is proved. These rules are applicable to a linear circuit containing: all four types of linear controlled sources, resistors, inductors, capacitors, nullors (for ideal opamps operating in the linear mode), and any multi-terminal or multiport circuit element having an equivalent scheme made up only by two-terminal elements and controlled sources. The generalized topological formula with homogeneous parameters that we propose to generate the transfer functions, can handle our models for the four types of controlled sources in a very efficient manner. Performing some reductions in the structure of the two graphs and representing them on levels we obtain an important improvement of the common tree enumeration process.

In Sect. 5.2 of this chapter we obtain the equivalent schemas in admittances that model in the two graphs the four types of controlled sources starting from the functional schemas with nullors. This representation makes possible the proof of the generalized topological formula with homogeneous parameters, valid for any transfer function of a lumped, linear and time-invariant circuit. Section 5.3 is dedicated to this proof. It is shown that the numerators of all the four types of transfer functions are identical and the treatment of the input/output ports according to the transfer function to be generated is given.

Section 5.4 is dedicated to a very efficient algorithm for tree enumeration in a graph represented on levels, which was implemented for network function generation, and Sect. 5.5 describes an efficient algorithm for sign factor generation. In Sect. 5.6 the rules for automatic generation of the network functions are introduced, and some techniques to increase the efficiency of the common spanning tree enumeration are discussed. The entire procedure of network function generation including simplification after generation is illustrated in Sect. 5.7.

5.2 Controlled Source Modelling in the Two Graphs

Consider two-port containing only linear passive two-terminal elements (resistors, capacitors, and inductors). It is well known that any circuit function can be written as a ratio of admittance polynomials using Kirchhoff's topological formula. Each monomial in these polynomials corresponds to the admittance value of a tree. This property leads to a circuit graph whose edges have the admittances as their weights.

Kirchhoff's type topological formulas have been developed by Mayeda and Seshu [16] for circuits containing linear passive two-terminal elements and voltage controlled current sources (VCCS) only. In these formulas each monomial corresponds to a common tree in the current graph G^i and the voltage graph G^v in which each passive element is represented by an edge having the admittance as its weight; a VCCS is modelled by an edge with the same weight (the control admittance) but with different positions in the two graphs: the position of the controlling branch in G^i and the position of the controlled branch in G^v. G^i is used to write the Kirchhoff's current law while G^v is used for the Kirchhoff's voltage law. The constitutive equations of all circuit elements are written as relationships between the G^i currents and G^v voltages.

Consider now a circuit containing two terminal elements and control sources of any type. In order to extend the abovementioned formulas to circuits with passive two-terminal elements and any type of controlled sources we build equivalent schemes of these sources using nullators and norators (nullors). A nullor equivalent scheme of a controlled source leads to its G^v and G^i representations considering the following properties: from the current point of view the nullator is an open-circuit while the norator is a short-circuit, and from the voltage point of view the nullator is a short-circuit while the norator is an open-circuit.

Starting from the equivalent schemes with nullors in Fig. 9, the two graph models of the controlled sources using only two terminal admittances can be built as it is shown in Fig. 9. The parameters associated with the controlled and the controlling branches are presented in Table 3. The subscript C is used for the controlling branch and the subscript c for the controlled one.

As it is shown in Fig. 9 the four types of controlled sources are modelled in the two graphs as follows:

- CCVS is modelled by a branch having the transfer impedance subscript identical with the controlled branch $Z_c = Z_{cC}$, having as parameter $Y_c = 1/Z_{cC}$, and which takes distinct positions in the two graphs:
  - In G^i it is connected to the controlling port, and it is oriented like the controlling current, the controlled branch being short-circuited;
  - In G^v this branch is connected to the controlled port, having the same direction with the voltage across this branch, the controlling branch being short-circuited.

In this way, a CCVS leads to a node contraction in each graph: in G^i the nodes of the controlled branch coincide, while in G^v the nodes of the controlling branch coincide. In order to keep the numbering of nodes in natural order (that is especially

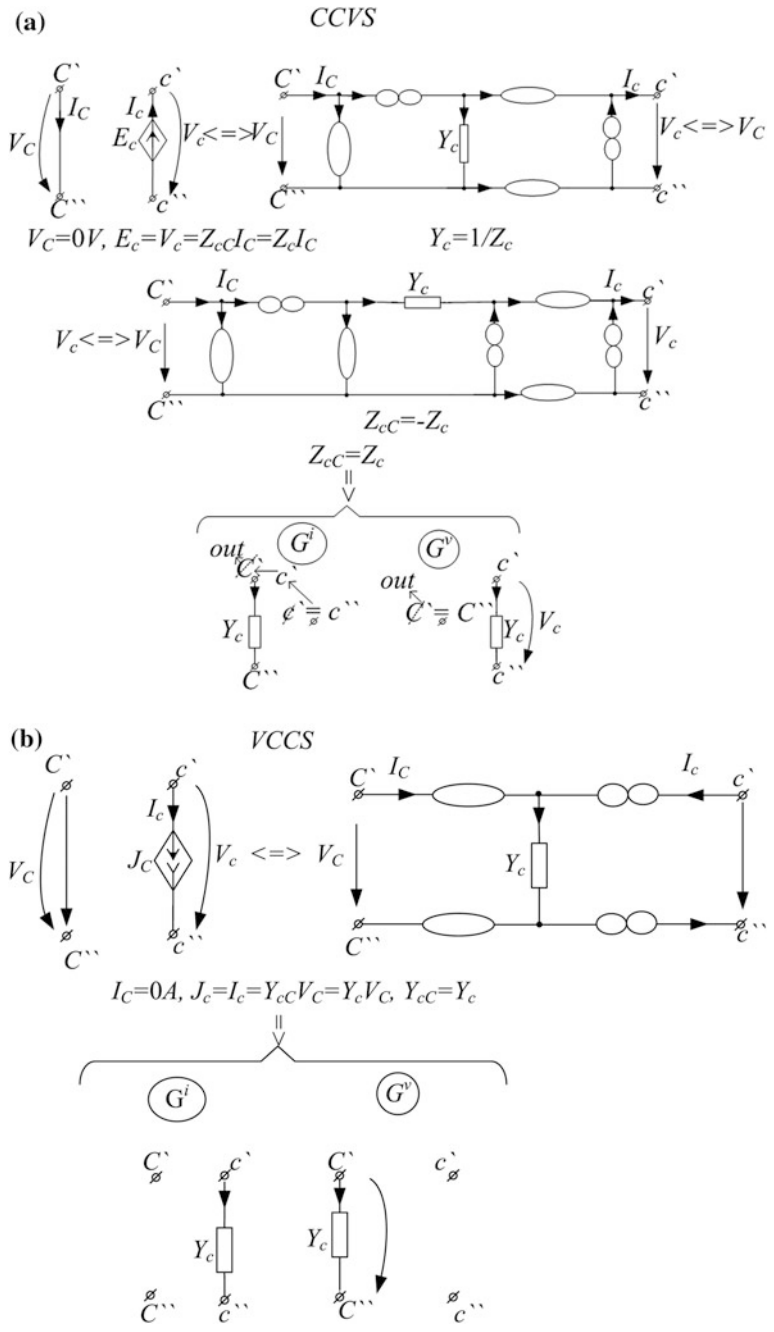


Fig. 9 Controlled source modelling in the two graphs

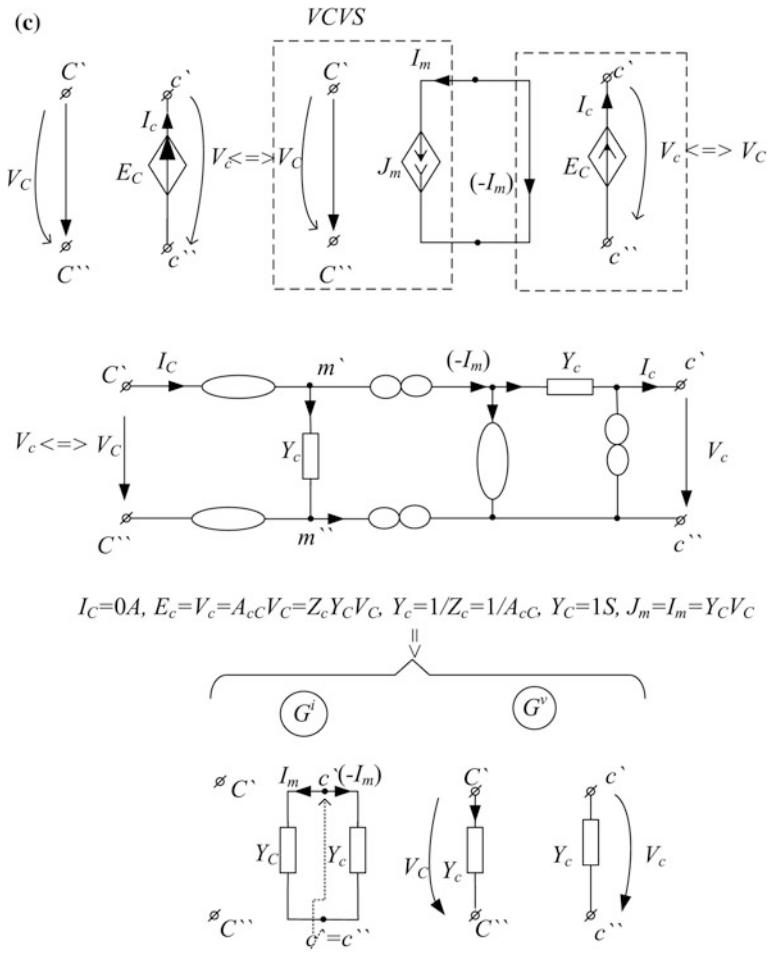


Fig. 9 (continued)

useful in tree enumeration and in the sign factor computation), we reduce by one all node numbers greater than the number of the eliminated node.

For programming needs we keep in G^i the node towards the voltage across the controlled branch is oriented (c'') the other node number (c') being allocated to the new node introduced to identify the controlling branch.

- VCCS is modelled by a branch having the transfer admittance subscript identical with the controlled branch $Y_c = Y_{cC}$, and which takes distinct positions in the two graphs:
  - In G^i it is connected to the controlled port, and it is oriented like the controlled current, the controlling branch being open;

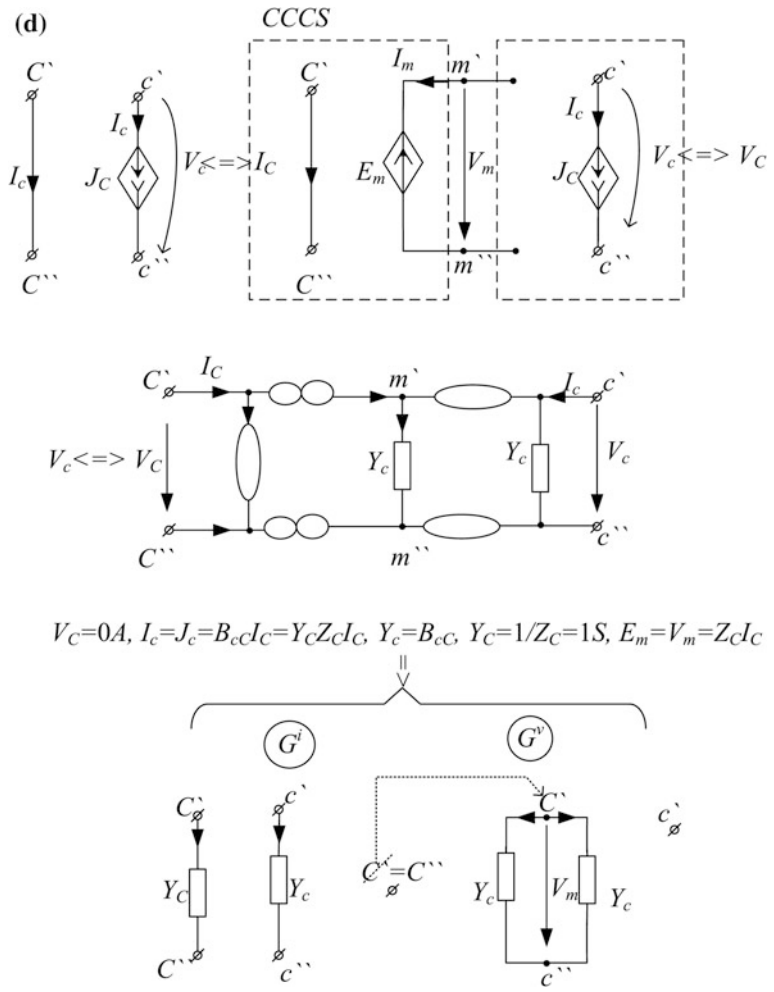


Fig. 9 (continued)

– In G^v this branch is connected to the controlling port, having the same direction with the controlling voltage, the controlled branch being open.

This controlled source does not modify the number of the two graph nodes.

- A VCVS is equivalent with a VCCS $(J_m = I_m = Y_C V_C)$, in cascade with a CCVS with negative trans-impedance $(E_c = (-Z_c) \cdot (-I_m))$, and it is modelled
  – In G^v by two branches having the controlled branch number respectively that of the controlling branch, and the parameters presented in the Table 2; they are connected to the controlled branch, respectively to the controlling one,

having the direction of the voltage across the controlled source, and respectively of the controlling voltage;
- In G^i the two branches are connected in series, having the nodes m' and m'' that are supplementary nodes. In order to keep the current graph node numbering, the number of the node m'' will be that towards the voltage across the controlled branch is oriented ($c'' \equiv m''$); the number of the eliminated node (c') will be attached to the other one ($c' \equiv m'$). The controlled branch is oriented from c'' to c', and the controlling one from c' to c''.

- A CCCS is equivalent with a CCVS connected in cascade with a VCCS, being modelled
  - In G^i by two branches having the controlled branch number and respectively those of the controlling branch, and the parameters presented in the Table 2; these branches are connected to the controlled port, respectively to the controlling one, having the direction of the controlled current, respectively of the controlling one;
  - In G^v the two branches are connected in parallel and they have two common nodes, namely the node in which the controlled current goes in (c'') and the other one having the number of the node eliminated by short-circuiting of the controlling branch in G^v (C'). The two branches have the same direction in respect of their terminals.

Remarks

1. The other circuit elements (resistors, uncoupled inductors, capacitors) keep in the two graphs the same position as in the initial circuit, and are represented by their admittances.
2. The magnetic couplings are modelled by inductors and CCVSs [10].
3. The above modelling technique of the four controlled sources leads to two directed graphs having admittance branches only.
4. The two graphs have the same number of nodes, branches and loops. They differ only by the location of the controlling and controlled branches of the four types of controlled sources.
5. Because any branch contraction in the two graphs causes the elimination of one node, the number of nodes in G^i and G^v is smaller than in the initial circuit with the number of CCVSs: $n_{G^i} = n_{G^v} = n - n_{CCVS}$.

In Table 3 is given a comparison with some reported techniques taking into account the number of branches used to model the circuit elements in both graphs and the supplementary node number.

Table 2 Controlled source equations

Controlled	Equations	Associated	Parameter
Source		Controlled branch	Controlling branch
CCVS	$V_C = 0$;	$Y_c = 1/Z_c$	$Y_c = 1/Z_c$
VCCS	$I_C = 0$;	Y_c	Y_c
VCVS	$I_C = 0$; $E_c = V_c = A_{cC} V_C = Z_c Y_C V_C$	$Y_c = 1/Z_c = 1/A_{cC}$	$Y_C = 1$ S
CCCS	$V_C = 0$;	$Y_c = B_{cC}$	$Y_C = 1/Z_C = 1$ S

Table 3 Comparison with some reported techniques

	Lin's	Models [17]	Rodanski's	Models [18]	Our	Models
Controlled source	Branches in the two graphs	Extra nodes	Branches in the two graphs	Extra nodes	Branches in the two graphs	Extra nodes
Resistor inductor capacitor	3	1	3	1	1	0
CCVS	4	1	5	2	1	−1
VCVS	3	1	3	1	2	0
CCCS	2 or 4	0 or 2	3	1	2	0

5.3 *Generalized Topological Formula for Network Function Generation*

Let us consider a linear nonreciprocal circuit (LNC) with null initial (i.c.) state and without independent sources and its associated model for operational calculus (Laplace). If we add to the input port an independent current source (Fig. 10), we can define the transfer impedance

$$Z_{oi} =^{d} \left. \frac{V_o}{J_i} \right|_{I_o = 0}. \tag{19}$$

The nodal equations of the circuit take the matrix form:

$$\mathbf{Y}_{n-1} \mathbf{V}_{n-1} = J_i, \tag{20}$$

where J_i can be expressed as

$$J_i = Y(V_{o'} - V_{o''}), \tag{21}$$

with

$$Y =^{d} \frac{1}{Z_{oi}}. \tag{22}$$

The Eq. (21) is equivalent to the substitution of J_i by a VCCS. Substituting Eq. (21) in (20) and rearranging we obtain:

$$\mathbf{Y}'_{n-1}\mathbf{V}_{n-1} = 0. \tag{23}$$

Consider the current and voltage graphs with their reduced node-branch incidence matrices $\mathbf{A}^i$ and $\mathbf{A}^v$.

Writing the Kirchhoff's current law in the current graph we obtain:

$$\mathbf{A}^i\mathbf{I}^i_b = 0, \tag{24}$$

where the branch currents can be expressed as:

$$\mathbf{I}^i_b = \mathbf{Y}_b\mathbf{V}^v_b. \tag{25}$$

The branch voltages in the voltage graph are:

$$\mathbf{V}^v_b = (\mathbf{A}^v)^{\mathrm{t}}\mathbf{V}^v_{n-1}. \tag{26}$$

Substituting (26) in (25) and the last one in (24) we obtain:

$$\mathbf{A}^i\mathbf{Y}_b(\mathbf{A}^v)^{\mathrm{t}}\mathbf{V}^v_{n-1} = 0. \tag{27}$$

If we denote

$$\mathbf{A}^i\mathbf{Y}_b(\mathbf{A}^v)^{\mathrm{t}} = \mathbf{Y}'_{n-1}, \tag{28}$$

we obtain (23).

Because the system (27) contains linear dependent equations it follows:

$$\det(\mathbf{A}^i\mathbf{Y}_b(\mathbf{A}^v)^{\mathrm{t}}) = 0. \tag{29}$$

$\boldsymbol{Y}_b$ being a symmetrical matrix, applying Binet-Cauchy theorem [6, 7] it results:

$$\det(\mathbf{A}^i\mathbf{Y}_b(\mathbf{A}^v)^{\mathrm{t}}) = \sum_{k=1}^{n_c}\Delta^i_k\Delta^v_k P_k, \tag{30}$$

where: Δ^i_k and Δ^v_k are determinants of order $n-1$, made up with elements of $\boldsymbol{A}^i$ and $(\boldsymbol{A}^v)^{\mathrm{t}}$ matrices, taking the k-th group of $n-1$ columns of $\boldsymbol{A}^i$ and respectively $n-1$ rows of $(\boldsymbol{A}^v)^{\mathrm{t}}$; P_k is the product of the operational branch admittances of $\boldsymbol{A}^i$ columns, respectively of $(\boldsymbol{A}^v)^{\mathrm{t}}$ rows that make up the k-th group; $n_c = C_b^{n-1}$.

Because Δ^i_k and Δ^v_k are nonzero if and only if the k-th groups of branches corresponding to the $n-1$ columns (rows) of $\boldsymbol{A}^i$ ($(\boldsymbol{A}^v)^{\mathrm{t}}$) form trees in G^i (G^v) [7], (30) may be written as:

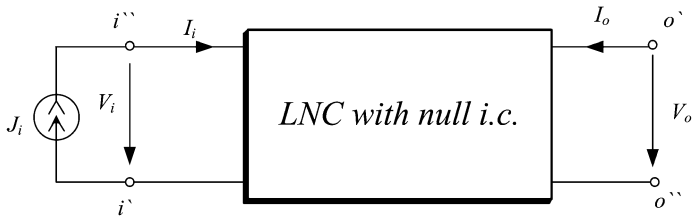


Fig. 10 The LNC transfer impedance definition

$$\det(\mathbf{A}^{i}\mathbf{Y}_{b}(\mathbf{A}^{v})^{\mathrm{t}}) = \sum_{k=1}^{t_c} \Delta_k^i \Delta_k^v P_k = \sum_{k=1}^{t_c} \varepsilon_k P_k = 0, \tag{31}$$

where: t_c is the total number of common trees of G^i and G^v; P_k is the operational admittance product of the common tree T_k branches; ε_k represents the sign factor of the pair k of common trees.

In the expression (31) there are two kinds of terms: terms that contain the admittance Y, and the others that do not contain it, so that it follows:

$$\det(\mathbf{Y}'_{n-1}) = \sum_{k=1}^{t_c} \varepsilon_k P_k = YT_1(s) + T_p(s) = 0, \tag{32}$$

where:

$$T_1(s) = \sum_{k \in (T_{1c})} \varepsilon_k t_k, \tag{33}$$

$$T_p(s) = \sum_{k \in (T_{pc})} \varepsilon_k t_k, \tag{34}$$

and $\varepsilon_k = \pm 1$—is the sign factor for each common spanning tree of the pairs (G_1^i, G_1^v), respectively (G_p^i, G_p^v), where G_1^i (G_1^v) is the current (voltage) graph containing a unit weight branch at the input (output) port, and G_p^i (G_p^v) represents the current (voltage) graph in which the input/output ports are in short-circuit or open according to the generated network function (see Table 4); $T_{1c}(T_{pc})$ is the set of the common

Table 4 Treatment of the input/output ports

The circuit	The circuit port	
Function	Input	Output
Z_{oi}	Open	Open
Y_{oi}	Short-circuit	Short-circuit
A_{oi}	Short-circuit	Open
B_{oi}	Open	Short-circuit

spanning trees of G_1^i,G_1^v (G_p^i,G_p^v); t_k is the product term equal to the product of branch admittances of the common spanning tree k.

From Eq. (32) we obtain:

$$Y = -\frac{T_p(s)}{T_1(s)}. \tag{35}$$

According to (22) it results that

$$Z_{oi} = -\frac{T_1(s)}{T_p(s)}. \tag{36}$$

In the following we shall prove that, according to this approach, any transfer function of a lumped, linear, and time-invariant circuit, can be expressed in the form:

$$F_{oi} = -\frac{T_1(s)}{T_p(s)}, \tag{37}$$

all the four transfer functions having the same numerator, the denominator being different depending on the way the input and the output ports of the circuit are treated. From the above it results that the problem of generating all product terms in the irreducible expression of the transfer function is converted to the problem of finding all common spanning trees of the two graphs.

Let us consider a two-port circuit, containing any linear multi-terminal circuit elements that have an equivalent scheme made up only by two-terminal circuit elements and controlled sources. Modelling the controlled sources in the two graphs by two terminal circuit elements as in Fig. 9 allows a uniform treatment in admittances of the entire linear nonreciprocal circuit (*LNC*).

1. **Transfer impedance**

Using the circuit represented in Fig. 11, we define its transfer impedance as

$$Z'_{oi} = \frac{V'_o}{J_i}, \tag{38}$$

from which we can obtain the LNC transfer impedance:

$$Z_{oi} = \lim_{\substack{Y_i \to 0 \\ Yo \to 0}} Z'_{oi} = -\frac{T_1(s)}{T_p(s)}, \tag{39}$$

where:

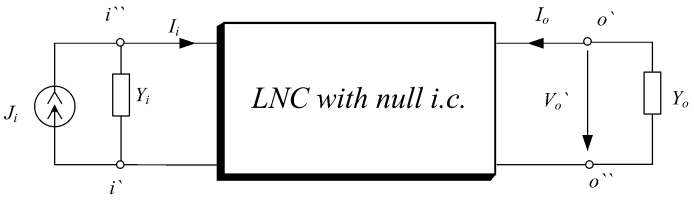


Fig. 11 The general scheme for transfer impedance definition

- T_1 is the sum of the algebraic values of the common trees in the graphs that contain the unity branch at the input (in G^i) respectively at the output (in G^v);
- T_p is the sum of the algebraic values of the common trees in G^i and G^v obtained by opening the input and output ports.

2. **Transfer admittance**

The transfer admittance of the circuit in Fig. 12 is:

$$Y'_{oi} = \frac{I'_o}{E_i} = \frac{Y_o V'_o}{J_i/Y_i} = Y_i Y_o Z'_{oi}, \tag{40}$$

and those of the LNC results as:

$$Y_{oi} = \lim_{\substack{Y_i \to \infty \\ Yo \to \infty}} Y'_{oi} = \lim_{\substack{Y_i \to \infty \\ Yo \to \infty}} Y_i Y_o Z'_{oi}. \tag{41}$$

Using the generalized Feussner formula for two branches we obtain:

$$\begin{aligned} Y_{oi} &= \lim_{\substack{Y_i \to \infty \\ Yo \to \infty}} Y_i Y_o Z'_{oi} = \\ &= -\lim_{\substack{Y_i \to \infty \\ Yo \to \infty}} Y_i Y_o \frac{T_1}{Y_i Y_o T'_{Y_{i,sc} Y_{o,sc}} + Y_i T'_{Y_{i,sc} Y_{o,op}} + Y_o T'_{Y_{i,op} Y_{o,sc}} + T'_{Y_{i,op} Y_{o,op}}} = \\ &= -\frac{T_1}{T'_{Y_{i,sc} Y_{o,sc}}} = -\frac{T_1}{T_p^Y}, \end{aligned} \tag{42}$$

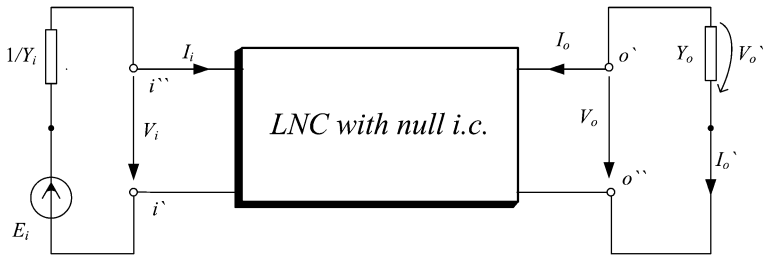


Fig. 12 The general scheme for transfer admittance definition

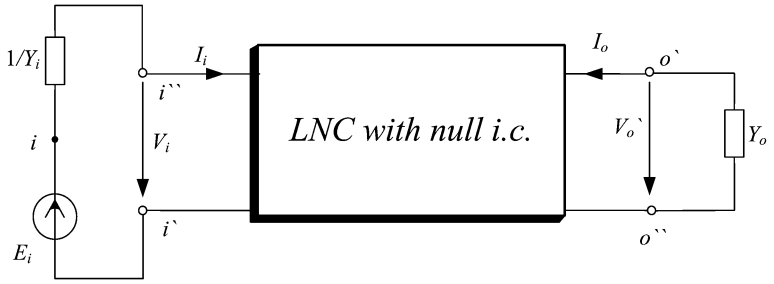


Fig. 13 The general scheme for voltage gain definition

where: T_1 is the same as in the case of Z_{oi}, and $T_p^Y = T'_{Y_{i,sc}Y_{o,sc}}$ is the sum of the algebraic values of the trees that are common to the G^i and G^v obtained by short-circuiting the input and output ports.

3. **Voltage Gain**
   Using the circuit in Fig. 13 we define the voltage gain as:

$$A'_{oi} = \frac{V'_o}{E_i} = \frac{V'_o}{J_i/Y_i} = \frac{Y_i V'_o}{J_i} = Y_i Z'_{oi}, \tag{43}$$

   from which we obtain the LNC transfer function

$$A_{oi} = \lim_{\substack{Y_i \to \infty \\ Yo \to 0}} A'_{oi} = \lim_{\substack{Y_i \to \infty \\ Yo \to 0}} Y_i Z'_{oi}. \tag{44}$$

   Applying the generalized Feussner formula we obtain:

$$\begin{aligned} A_{oi} &= \lim_{\substack{Y_i \to \infty \\ Yo \to 0}} Y_i Z'_{oi} = \\ &= -\lim_{\substack{Y_i \to \infty \\ Yo \to 0}} Y_i \frac{T_1}{Y_i Y_o T'_{Y_{i,sc}Y_{o,sc}} + Y_i T'_{Y_{i,sc}Y_{o,op}} + Y_o T'_{Y_{i,op}Y_{o,sc}} + T'_{Y_{i,op}Y_{o,op}}} = \\ &= -\frac{T_1}{T'_{Y_{i,sc}Y_{o,op}}} = -\frac{T_1}{T_p^A}, \end{aligned} \tag{45}$$

   where: T_1 is the same as in the case of Z_{oi} and Y_{oi}, and T_p^A is the sum of the algebraic values of the trees that are common to the G^i and G^v obtained by short-circuiting the input port and opening the output port.
4. **Current gain**
   For the circuit in Fig. 14 the current gain is:

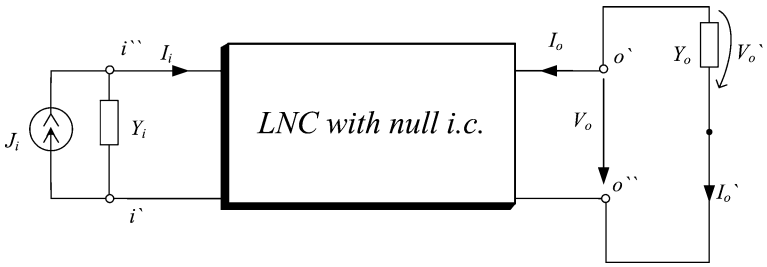


Fig. 14 The general scheme for current gain definition

$$B'_{oi} = \frac{I'_o}{J_i} = \frac{Y_o V'_o}{J_i} = Y_o Z'_{oi}, \tag{46}$$

and for the LNC we obtain

$$B_{oi} = \lim_{\substack{Y_i \to 0 \\ Y_o \to \infty}} B'_{oi} = \lim_{\substack{Y_i \to 0 \\ Y_o \to \infty}} Y_o Z'_{oi}, \tag{47}$$

that means

$$\begin{aligned} B_{oi} &= \lim_{\substack{Y_i \to 0 \\ Yo \to \infty}} Y_o Z'_{oi} = \\ &= - \lim_{\substack{Y_i \to 0 \\ Yo \to \infty}} Y_o \frac{T_1}{Y_i Y_o T'_{Y_{i,sc} Y_{o,sc}} + Y_i T'_{Y_{i,sc} Y_{o,op}} + Y_o T'_{Y_{i,op} Y_{o,sc}} + T'_{Y_{i,op} Y_{o,op}}} = \\ &= - \frac{T_1}{T'_{Y_{i,op} Y_{o,sc}}} = - \frac{T_1}{T_p^B}, \end{aligned} \tag{48}$$

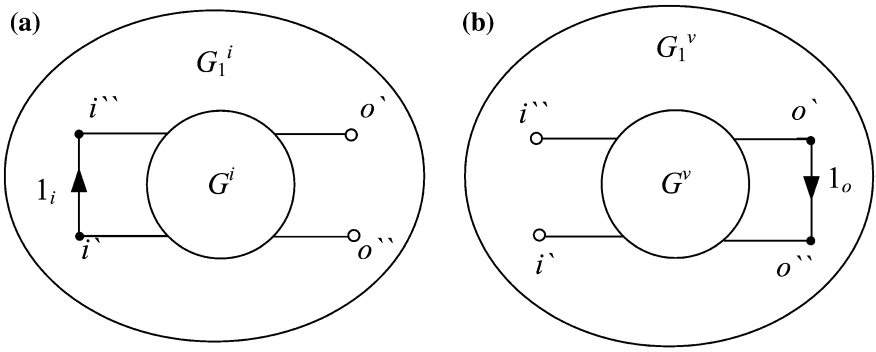


Fig. 15 Current and voltage graphs that contain the unit branch

where: T_1 is the same as in the above three cases, and T_p^B is the sum of the algebraic values of the trees that are common to the G^i and G^v obtained by opening the input port and short-circuiting the output port.

From the above analysis, we can conclude that to obtain all the transfer functions the input/output ports must be treated as in Table 4.

For the automatic generation of the graphs G_1^i and G_1^v the input gate of the analyzed circuit is connected to a current source that is controlled by the output gate voltage, which has the transfer admittance equal to the unit [27]. According to the Sect. 5.2 it will be represented in the two graphs as in Fig. 15.

5.4 Algorithm for Tree Enumeration in a Graph Represented on Levels

We have proved that the network functions generation by the topological method of tree enumeration, in the case of nonreciprocal circuits, means the generation of all common spanning trees. Since the number of graph trees increases rapidly with the graph size, a highly efficient algorithm is needed. This problem was widely studied and several algorithms of varying efficiency have been proposed in the literature. Ones of the well-known are Minty's algorithm which has the complexity $O(b + n + bt)$, and the algorithm due to Gabow and Myers having the complexity $O(b + n + nt)$, where b is the number of branches, n is the number of graph nodes, and t is the number of spanning trees.

The most used is, however, Char's algorithm, that some studies [23] show it to be superior to the other ones. This algorithm generates for the beginning an initial spanning tree which needs $O(b + n)$ operations, and starting from this one it enumerates all the spanning trees of the graph. During this enumeration, the algorithm generates also certain sequences which are not trees, called *non-tree sequences*. The original algorithm has the complexity $O(b + n + n(t + t_0))$, where t_0 is the number of non-tree sequences.

An implementation, called MOD-CHAR, of Char's spanning tree enumeration algorithm, introduces several heuristics for the selection of the initial spanning tree and for decreasing the number of the non-tree sequences. With these improvements for almost all graphs, the complexity of MOD-CHAR is $O(nt)$ [21–23]. It seems that for large dense graphs the complexity of MOD-CHAR algorithm is $O(t)$, being superior to Char's original algorithm, while for sparse graphs, it seems that Char's original implementation is superior to MOD-CHAR [22].

In the following we present an efficient algorithm for the enumeration of all the common spanning trees based on a representation on levels of the two graphs, and on a sequential computation (by substituting a branch in the previous common spanning tree), which has the complexity $O(t)$ for all kinds of graphs [13].

Let us consider the connected graph represented in Fig. 16a, and described on levels as in Fig. 16b, where:

n, b, l—represent the number of nodes, branches, and levels, respectively;

b[i] = (xi, y_i)—is the branch i, connected between the nodes x_i and y_i; the node set is ordered so that

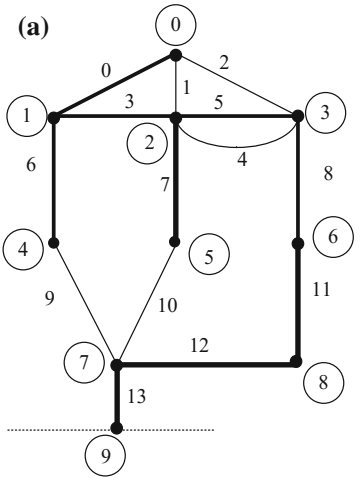
- level (x_i) $\leq$ level (y_i);
- $\forall\ 0 \leq i \leq b-1$, level ($x_i$) $\leq$ level (x_i+1) and level (y_i) $\leq$ level (y_i+1);

$niv[j]$ is the first node of level j, with $0 \leq j \leq l$;

$bet[k]$ is the first branch which connects the levels k and $k+1$, where $0 \leq k \leq l-1$;

$inter[m]$ is the first branch which connects two nodes from the level m, where $1 \leq m \leq l-1$;

The algorithm for tree enumeration is the following:



(b)

$n = 10$
$b = 14$
$l = 5$
$niv = (0,1,4,7,9)$
$bet = (0,6,9,13)$
$inter = (3,12)$

b[0]=[0,1] b[1]=[0,2]
b[2]=[0,3] b[3]=[1,2]
b[4]=[2,3] b[5]=[2,3]
b[6]=[1,4] b[7]=[2,5]
b[8]=[3,6] b[9]=[4,7]
b[10]=[5,7]
b[11]=[6,8]
b[12]=[7,8]
b[13]=[7,9]

Fig. 16 Graph representation on levels

```
place inside (level, k)
        if (level=0) {write tree; output of procedure}
        place between (level, niv[level])
        for i=k to bet[level]-1 do
                        {
                        save the colors on the stack
                        put in the tree (i)
                        place inside (level, i+1)
                        take off from the tree the last registration
                        restore the colors from the stack
                        }
place between (level, col)
        OK=1
        for C=col to niv[level+1]-1 do
              if exist the color C
                 for i=bet[level-1] to inv[level]-1 do
                     if color[b[i].y]=C
                         {
                         OK=0
                         save the colors on the stack
                         put in the tree (i)
                         place rest (level, C, i+1)
                         take off from the tree the last registration
                         restore the colors from the stack
                         }
        if (OK=1) place inside (level-1, inv[level-1]);

      place rest (level,col,k)
         place between (level, col+1)
         for i=k to inv[level]-1 do
               if color[b[i].y]=col
                 if do not make a cycle ⇔ if color [b[i].x]≠col
                    {
                    save the colors on the stack
                    put in the tree (i)
                    place rest (level, col, i+1)
                    take off from the tree the last registration
                    restore the colors from the stack
                    }
```

Remarks

1. The representation of any graph in level form is equivalent with node sorting. If a heap-sort procedure is used, the time complexity is $O(b\lg b + n\lg n)$ while using an array technique it will be $O(2b + 2n)$ [12].
2. The algorithm does not generate any non-tree sequence.
3. Any branch that obeys the algorithm rules, when is introduced in the sequence, leads to a tree.
4. The time complexity of the tree enumeration algorithm is proportional to the number of trees, $O(kt)$, where k is, statistically, about 1, when the time allocated for the level decomposition of the graph is neglected.
5. The space complexity is $O(n + n^2)$, when the necessary of memory for preserving the graph structure (which is insignificant) is neglected.

Testing the algorithm for many graphs, to make a comparison with Char's algorithm, we obtained the results presented in Table 5, and in Fig. 17.

We can see that the efficiency of our algorithm rises rapidly with the number of trees.

5.5 Algorithm for Sequential Generation of the Sign Factor

For all the terms of the numerator and of the denominator the sign factor must be computed. The sign of the tree admittance product can be found using Mayeda and Seshu's algorithm [8] or performing a depth-first or breadth-first traversal on both the G^i and G^v trees [2]. In [10, 11] an original method for the sign factor determination is presented. The tree admittance product sign ε_k is defined as:

$$\varepsilon_k = M_{T_k^i} \cdot M_{T_k^v}, \tag{49}$$

where $M_{T_k^i}, M_{T_k^v}$ are major determinants from the branch-node incidence matrices $\mathbf{A}^i$ and $\mathbf{A}^v$ corresponding to the common spanning trees T_k^i and T_k^v, respectively. To describe the current (voltage) spanning tree T_k^i (T_k^v) we use a matrix with two rows

Table 5 Comparison between the proposed algorithm and Char's algorithm

Number of the trees	Time [s]	
	Char's algorithm	Algorithm on levels
107512	0.53	0.56
9877412	14.1	8.66
61314527	82	55
103472385	154	103
220581744	235	156
1182369421	7920	1860

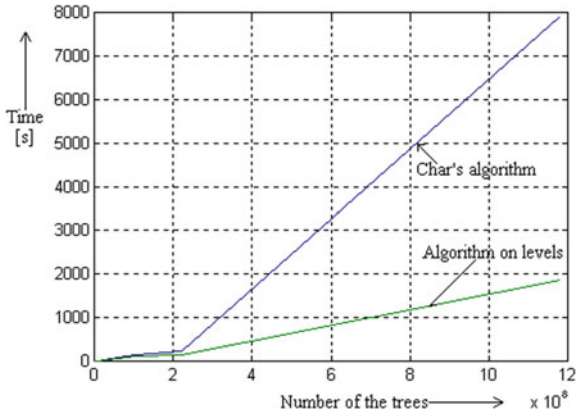


Fig. 17 Comparison with Char's algorithm

and $n-1$ columns (n being the node number of the graph)—called the *current* (*voltage*) *tree description matrix* CTDM (VTDM). Each column of this matrix contains the initial node and the final node of the tree branch corresponding to this column. For example, the tree description matrix (TDM) corresponding to the spanning tree shown in Fig. 18 has the following form:

$$\mathrm{TDM} = \begin{bmatrix} 1 & 2 & 4 & 4 & 6 & 7 & 5 & 6 \\ 2 & 4 & 3 & 6 & 7 & 5 & 8 & 9 \end{bmatrix}. \tag{50}$$

The determinants $M_{T_k^i}$ and $M_{T_k^v}$ are computed by performing simple operations on the rows of the tree description matrices. In Fig. 18 is described the computing algorithm of the determinant M_T corresponding to the spanning tree $T = \{b_1, b_2, b_3, b_4, b_5, b_6, b_7, b_8\}$.

Let B, N be two finite sets B, $N \subset \mathbf{N}$. The directed graph is, by definition, the triplet $G = (B, N, f)$, in which $f: B \to N \times N$. Let $x = (x_1, x_2)$ be an element of the set $N \times N$. We define:

$$p_1: N \times N \to N, \quad p_1(x) = x_1; \quad p_2: N \times N \to N, \quad p_2(x) = x_2, \tag{51}$$

the projections of an element in $N \times N$. Let $T = \{b_1, b_2, \ldots, b_{n-1}\}$, with $b_j \in B$, $1 \le j \le n-1$, be a spanning tree and let

$$\mathbf{P} = \begin{bmatrix} p_1(f(b_1)) & p_1(f(b_2)) & \ldots & p_1(f(b_{n-1})) \\ p_2(f(b_1)) & p_2(f(b_2)) & \ldots & p_2(f(b_{n-1})) \end{bmatrix}, \tag{52}$$

be the matrix built with the rows 1 and 2 of TDM corresponding to the spanning tree T.

The algorithm for the determinant M_T calculation has the following steps:

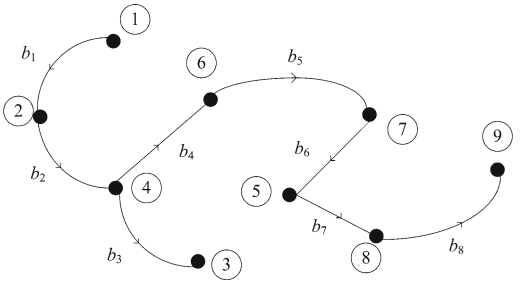


Fig. 18 Algorithm of the sign factor determination

$$b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8$$

$$\begin{bmatrix} 1\ 2\ 4\ 4\ 6\ 7\ 5\ 8 \\ 2\ 4\ 3\ 6\ 7\ 5\ 8\ 9 \end{bmatrix} = P \ \ for \ T = \{b_1, b_2, b_3, b_4, b_5, b_6, b_7, b_8\}$$

$$\begin{bmatrix} 1\ 2\ 4\ 4\ 6\ 7\ 5\ 8 \\ 2\ 4\ 3\ 6\ 7\ 5\ 8\ 9 \end{bmatrix} = P_0 \Rightarrow (-1)^{1+1}$$

$$\begin{bmatrix} 1\ 3\ 3\ 5\ 6\ 4\ 7 \\ 3\ 2\ 5\ 6\ 4\ 7\ 0 \end{bmatrix} = P_1 \Rightarrow (-1)^{1+1}$$

$$\begin{bmatrix} 2\ 2\ 4\ 5\ 3\ 6 \\ 1\ 4\ 5\ 3\ 6\ 0 \end{bmatrix} = P_2 \Rightarrow (-1)^{1+1+1}$$

$$\begin{bmatrix} 1\ 3\ 4\ 2\ 5 \\ 3\ 4\ 2\ 5\ 0 \end{bmatrix} = P_3 \Rightarrow (-1)^{1+1}$$

$$\begin{bmatrix} 2\ 3\ 1\ 4 \\ 3\ 1\ 4\ 0 \end{bmatrix} = P_4 \Rightarrow (-1)^{2+1}$$

$$\begin{bmatrix} 2\ 1\ 3 \\ 1\ 3\ 0 \end{bmatrix} = P_5 \Rightarrow (-1)^{2+1}$$

$$\begin{bmatrix} 1\ 2 \\ 2\ 0 \end{bmatrix} = P_6 \Rightarrow (-1)^{1+1}$$

$$\begin{bmatrix} 1 \\ 0 \end{bmatrix} = P_7 \Rightarrow (-1)^{1+1}$$

$$M_T = (-1)^{2+2+3+2+3+3+2+2} = -1$$

1. In the matrix $\boldsymbol{P}$, we assign zero value to the node with the greatest index (e.g. n_9 in Fig. 18). In this way, we obtain a matrix which is denoted by $\boldsymbol{P}_0$;
2. We are looking for the node which exists only once in the matrix $\boldsymbol{P}_0$, beginning with the node having the smallest index. Let this be $n_j = p_k(b_j)$, with $k = 1$ or $k = 2$ (e.g. n_1 in Fig. 18);
3. We develop the determinant M_T on the row corresponding to the node n_j, namely

$$M_T = (-1)^{n_j + j} M_T^j, \tag{53}$$

if $k = 1$, and

$$M_T = (-1)^{n_j + j + 1} M_T^j, \tag{54}$$

if $k = 2$, where j is the column of the matrix $\boldsymbol{P}_0$ corresponding to the node n_j, and M_T^j represents the determinant obtained from M_T after the elimination of the row n_j and of the column j;
4. If the node number n_j, found in step 2, is less than the greatest node number in $\boldsymbol{P}_0$ (if $n_j < n - 1$), then all elements of $\boldsymbol{P}_0$ having the values greater than n_j are reduced by a unit, and all columns of the matrix $\boldsymbol{P}_0$, which are on the right side of the column j, change the places with a column to the left side. Thus, we obtain a matrix $\boldsymbol{P}_m$, $m \leftarrow m + 1$ (initially $m \leftarrow 0$), having the column number less than $\boldsymbol{P}_0$ with a unit;
5. If $n_j \geq 1$ and if the column number of the matrix $\boldsymbol{P}_m$ is greater than one, go to step 2, where the matrix $\boldsymbol{P}_m$ takes the place of the matrix $\boldsymbol{P}_0$. If the $n_j = 1$ and if the matrix $\boldsymbol{P}_m$ has a single column, the determinant M_T^j is developed on the row corresponding to the node n_1 and go to step 6;
6. Check up if the exponent of (-1) is an even or odd number.

In order to reduce the time needed to generate the circuit functions, a very fast algorithm for calculating the sign factor was developed and implemented. It is based on sequential computation, because knowing the sign of a term we can find the sign of the following by performing simple elementary operations (permutations) in a vector with n elements, representing the number of the graph nodes. These permutations aim to preserve the summations between lines of the reduced node-branch incidence matrix, without having to store it in the memory.

The algorithm pseudocode has the following structure:

```
ordine (x)
j=0
for I=1 to x do if rel[I]=I then inc(j)
if odd[j] return 1
          else return −1

add edge
while x≠rel[x] x=rel[x]
if (x=nv)
          while y≠rel[y] y=rel[y];
          rel[y]=nv;
          s= −s·ordine(y)
else s= s·ordine(y)

compute sign
s=1, for I=1 to nv do rel[I]=I
for I=1 to nv−1 do add edge(I)
return(j)
```

5.6 Automatic Generation of the Transfer Functions

As it has been shown in Sect. 5.6, in order to compute a transfer function, we have to use two pairs of graphs: $\left(G_1^i, G_1^v\right)$, for the numerator product terms, and $\left(G_p^i, G_p^v\right)$ (in accordance with Table 4), for the denominator product terms.

For the automatic generation of $\left(G_1^i, G_1^v\right)$, we must connect at the input port of the circuit a VCCS having as controlling variable the output voltage, the transfer admittance being 1. For this source, the controlled branch number is 1, while the controlling branch number is 2 (Fig. 19, *LNC—Linear Nonreciprocal Circuit*).

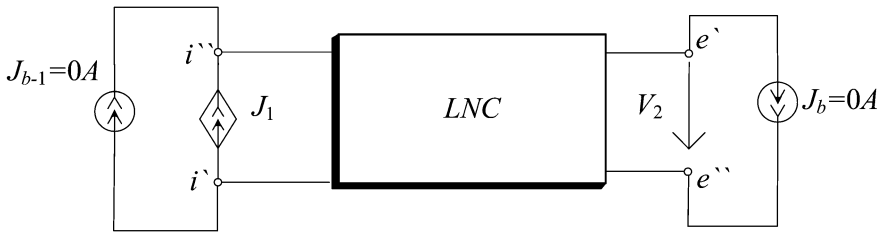


Fig. 19 Automatic generation of $\left(G_1^i, G_1^v\right)$ and $\left(G_p^i, G_p^v\right)$

For the automatic generation of $\left(G_p^i, G_p^v\right)$ we must connect at the input/output ports some ideal independent current sources having null currents and the last branch numbers: $b-1$, respectively b (Fig. 19).

The algorithm for transfer impedance Z_{oi} generation involves the following steps:

1. Gyrator circuits, voltage or current inverters, magnetic couplings, operational amplifiers and, in general, the multipole or multiport circuit elements contained in the analyzed circuit are replaced by equivalent schemes consisting of bipolar circuit elements and controlled sources only;
2. Controlled sources are simulated by passive two terminals elements that have distinct positions in G^i and G^v graphs (see Table 4);
3. Graphs G_1^i and G_1^v are generated (Figs. 15a and b). In G_1^i the branch with the unit weight connects the input port terminals, having the same sense as the sense of the input variable corresponding to the transfer function to be generated and the output port is open. In G_1^v, the branch with unit weight connects the output port terminals in the same sense as the sense of the output variable corresponding to the transfer function to be generated, the input port being open;
4. Graphs G_p^i and G_p^v are generated. In these graphs, the entry-exit ports are treated as in Table 4;
5. Determine the array of trees common to the graphs G_1^i and G_1^v that contains the branch with the unit weight

$$A_{1c} = A_1^i \cap A_1^v \tag{55}$$

where $A_1^i \left(A_1^v\right)$ is the array of the trees that contain the branch with the unit weight in the graph $G_1^i \left(G_1^v\right)$;

6. Determine the array of trees common to the graphs G_p^i and G_p^v

$$A_{pc} = A_p^i \cap A_p^v, \tag{56}$$

with $A_p^i \left(A_p^v\right)$, the array of the trees from the graph $G_p^i \left(G_p^v\right)$;

7. For each pair of common trees k, generated at steps P5 or P6, the sign factor ε_k is calculated with one of the algorithms described in Sect. 5;
8. Calculate the algebraic sum of tree values $\varepsilon_k P_k$ for the A_{1c} set and then for the set A_{pc}, P_k being the product of the weights (of operational admittances) of the common tree k branches;
9. With formula (37) calculate the transfer impedance Z_{oi};

If the numerator and the denominator of the relation (37) are multiplied by the product of the operational impedances of all branches of the circuit, it results:

$$Z_{ei} = -\frac{C_1}{C_p}, \tag{57}$$

where:

$$C_1 = \sum_{k \in C_{1c}} \varepsilon_k P_{ck}, \tag{58}$$

is the algebraic sum of the values (in impedances) of the co-trees common to the graphs G_1^i and G_1^v corresponding to the common trees that contain the branch with the unit weight and:

$$C_p = \sum_{k \in C_{pc}} \varepsilon_k P_{ck}, \tag{59}$$

is the algebraic sum of the values (in impedances) of the co-trees common to the graphs G_p^i and G_p^v.

It is easily to show [14, 21] that formula (55) can be used to generate any circuit function corresponding to the input-output ports treated as in Table 4.

Therefore

$$F_{oi} = -\frac{C_1}{C_p}, \tag{60}$$

where the function F_{oi} may be: the transfer impedance (either input or output), the transfer admittance (either input or output), the voltage transfer (gain) factor or the current transfer (gain) factor.

The algorithm for generating any of the above mentioned circuit functions is identical to the one presented for the transfer impedance Z_{oi}, the only difference being the treatment of the input-output ports (Table 4). To define input impedance (admittance), the input-output structure of the port is defined in Fig. 20a, b) by using a passive linear circuit (***PLC***). Analog is defined also the input-output structure of the two-port circuit for the calculation of the output impedance (the output admittance).

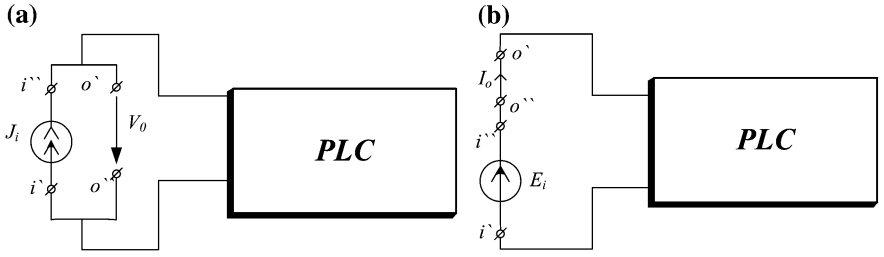


Fig. 20 The input-output structure of the two-port circuit for the calculation of the input impedance (**a**) and input admittance (**b**)

Before generating the transfer function in symbolic form, by tree enumeration in the two graphs, we must do some simplifications either in the circuit or in the structure of the two graphs called approximation-before-computation (ABC).

Firstly, for each parameter x, we perform a numerical computation of the transfer function sensitivity in the frequency range of interest.

This information could give us the reason to eliminate some branches either by element removal or by contraction of its terminal nodes that simplify the circuit structure. In order to control the accuracy of the computational process, we have to evaluate the errors in the transfer function magnitude and in the transfer function argument due to these operations in the frequency range of interest. Once the circuit structure was simplified, we can generate the two pairs of graphs: $\left(G_1^i, G_1^v\right)$ and $\left(G_p^i, G_p^v\right)$. In order to simplify the generation of all their common spanning trees, we perform some operations in the structure of these graphs, namely:

- Contraction of the unity weight branches;
- Substitution of the parallel branches in these graphs by an equivalent branch having the admittance equal to the sum of the parallel admittances;
- Contraction of all branches having a node of degree one.

After the generation of the spanning trees in the reduced graphs, we must add successively all the branches eliminated in the first step. This procedure increases the enumeration efficiency of the common spanning tree in the two pairs of graphs —$\left(G_1^i, G_1^v\right)$, and $\left(G_p^i, G_p^v\right)$.

To obtain the symbolic transfer function in a form to be easily interpreted, two approximation strategies are possible: approximation-during-computation (ADC) that produces the approximate expression without knowledge of the exact symbolic expression, and approximation-after-computation (AAC) that firstly generates the exact symbolic expression and operating on it produces an approximated one. The simplified form can be obtained because only a small number of the terms in the irreducible expanded expression of the transfer function have an important contribution in the numerator or in the denominator value. Of course, the most efficient method is to generate only the significant common trees (whose tree admittance value is not negligible) in an ADC process. To this end the common spanning trees must be generated in decreasing order of magnitude until the generated set is a good approximation of the exact network function value. Also, the generation of the common spanning trees in decreasing order of magnitude must be performed for each frequency of interest. Some techniques for ADC were reported [16, 23–26], based on a sensitivity simplification scheme, a 2-, respectively 3-matroid-intersection algorithm and on the determinant decision diagram (DDD) representation of the system determinant. Although it is not easy to compare the implementations of these algorithms because of the different simplification before generation performed, and because of the different error criteria, it seems [24] that ADC based on DDD yields better results concerning the time needed to generate a term in comparison with the other techniques.

In this chapter, an AAC procedure to obtain a network function in reduced symbolic form is adopted. To this end the numerator and the denominator expressions must be ordered in the decreasing order of the complex frequency powers. The coefficients of each complex frequency power must be ordered in the decreasing order of their values as well, and then the terms with the smallest value will be eliminated one by one if the magnitude and phase errors are kept within imposed limits in the frequency range of interest.

A very fast program for the network function generation in reduced symbolic form has been obtained by implementing the modelling technique of the controlled sources associated with the generalized topological formula and with the algorithm for common tree enumeration and sign factor computation.

5.7 *Description of the Software Application SATE—Symbolic Analisys by Trees Enumeration*

The symbolic generation algorithm of circuit functions for analogue linear and/or nonlinear (piecewise-linear approximation) circuits described in Sect. 5.6 have been implemented in a program called SATE—*S*imbolic *A*nalysis by *T*ree *E*numeration [28]. Starting from the description of the circuit through a netlist input file (*cir.* file extension), SATE generates symbolically, partial symbolically or numerically form any circuit function with respect to the user-specified input/output ports for the linear and/or non-linear (piecewise-linear approximation around a point of operation) electrical circuits.

The input data for the software application are:

nnode, *nb*, *pulsation*

where: *nnode*—is the number of circuit nodes, *nb*—is the branch number, and *pulsation (angular frequency)* is the pulsation value.

Follows a set of *nb* lines describing the branches of the circuit. The circuit elements are assigned as type numbers: **1**—for resistors; **2**—for capacitors; **3**—for inductors; **8**—for controlled sources $e_c(i_C)$; **9**—for controlled sources $j_c(v_C)$; **10**—for controlled sources $e_c(v_C)$; **11**—for controlled sources $j_c(i_C)$ and **12**—for the description of input-output ports.

For RLC circuit passive elements, the description statement has the form:

element_type parameter_real_value initial_node final_node

For a controlled source, the description statement has the following structure:

source_type parameter_real_value parameter_imaginary_value initial_node_c final_node_c initial_node_C final_node_C

where

initial_node_c final_node_c (initial_node_C final_node_C) represent the initial and final nodes for the controlled branch (controlling branch).

The last line of the input file describes the input/output ports and it has the following format:

12 initial_node_i final_node_i initial_node_o final_node_o

Remarks

1. The program gives to the branches numbers from 0 to b;
2. The last numbered branch, corresponding to the last line in the input file list, represents the branch weighting 1 in the current graph G_1^i and in the voltage graph G_1^v;
3. In the case of the current-controlled sources, $e_c(i_C)$ and $j_c(i_C)$, the controlling ports are simulated by resistors with a very low resistance value ($<10^{-8}\Omega$);
4. In the case of the homogeneous controlled sources ($e(v)$ and $j(i)$), the program assigns two branches to each source (in the following sequence: the controlled branch, the controlling branch), taking into account the modelling of these sources in the current graph or the voltage graph [20, 27]. Parameters corresponding to the two branches are assigned as follows:
   $A_{j\_k} = \frac{Y_k}{Y_j}$, where $Y_k = 1$ S and $Y_j = \frac{1}{A_{j\_k}}$, for the source e_c (v_C),
   $B_{j\_k} = \frac{Y_j}{Y_k}$, where $Y_k = 1$ S and $Y_j = B_{j\_k}$, for the source $j_c(i_C)$;
5. Magnetically coupled inductors are simulated by current-controlled voltage sources [20, 27, 28].

The main program **compute.bat** coordinates the entire process of generating the circuit function by successively calling the following subprograms:

- **cv_graph.exe**—it determines the current and voltage graphs;
- **tree.exe**—it generates the trees common to the two graphs;
- **comp_fix.exe**—it calculates the numerator and denominator terms of the circuit function;
- **getfunc.exe**—it factories the numerator and denominator expressions according to the chosen parameter;
- **draw.exe**—it draws the amplitude–frequency and phase–frequency characteristics of the generated circuit function.

The SATE program command line is:
compute input_file_name x
where:

- **input_file_name**—is the input file name with the extension *cir* (on the call the file extension is not written)
- and **x** represents the type of the circuit function that will be generated, as follows:

- **1**—the transfer impedance $Z_{ei}(s)$;
- **2**—the transfer admittance $Y_{ei}(s)$;
- **3**—the voltage transfer (gain) factor $A_{ei}(s)$;
- **4**—the current transfer (gain) factor $B_{ei}(s)$.

The SATE program generates the following output files:

- **file_name.gr1**—it contains the required information about the current graph;
- **file_name.gr(x + 1)—**it contains the required information about the voltage graph;
- **file_name.ar1**—it symbolically displays the numerator of the circuit function (A_1 from formula (19));
- **file_name.ar(x + 1)**—it symbolically displays the denominator of the circuit function (A_p from formula (19));
- a file containing numeric information about the value of the circuit function: the real part, the imaginary part, the module and the argument.

6 Examples

Example 3 Let us consider the linear circuit with lumped parameters represented in Fig. 21a. We want to determine the operational transfer admittance Y_{oi} from the input port *i'–i"* to the output port *o'–o"*, assuming that all the other parameters of the circuit are known.
In Fig. 21, additional sources were also represented $J_1 = 1.V_2$, $J_{13} = 0\text{A}$ and $J_{14} = 0\text{A}$, which aim to facilitate the automatic generation of graphs G_1^i, G_1^v (source $J_1 = 1.V_2$) and G_p^i, G_p^v (sources $J_{13} = 0\text{A}$ and $J_{14} = 0\text{A}$). The numbering of additional sources was done as indicated above.

In Fig. 21b–e the graphs G_1^i and G_1^v (G_p^i and G_p^v) are represented. The loops resulting by connecting in short-circuit of certain pairs of nodes in the graphs G_1^i, G_1^v, G_p^i and G_p^v have not been drawn in Fig. 21b–e (the branches of these loops cannot belong to the trees of these graphs).

The set of trees common to the graphs G_1^i and G_1^v (Figs. 21b and c), which contains the branch 1_i in G_1^i and, respectively, branch 1_o in G_1^v is:

$$A_{1c} = \{(1_i, 6, 9, 12; 1_o, 6, 9, 12), (1_i, 4, 10, 11; 1_o, 4, 10, 11)\}. \tag{61}$$

The set of trees common to the graphs G_p^i and G_p^v (Figs. 21d and e) has the following structure:

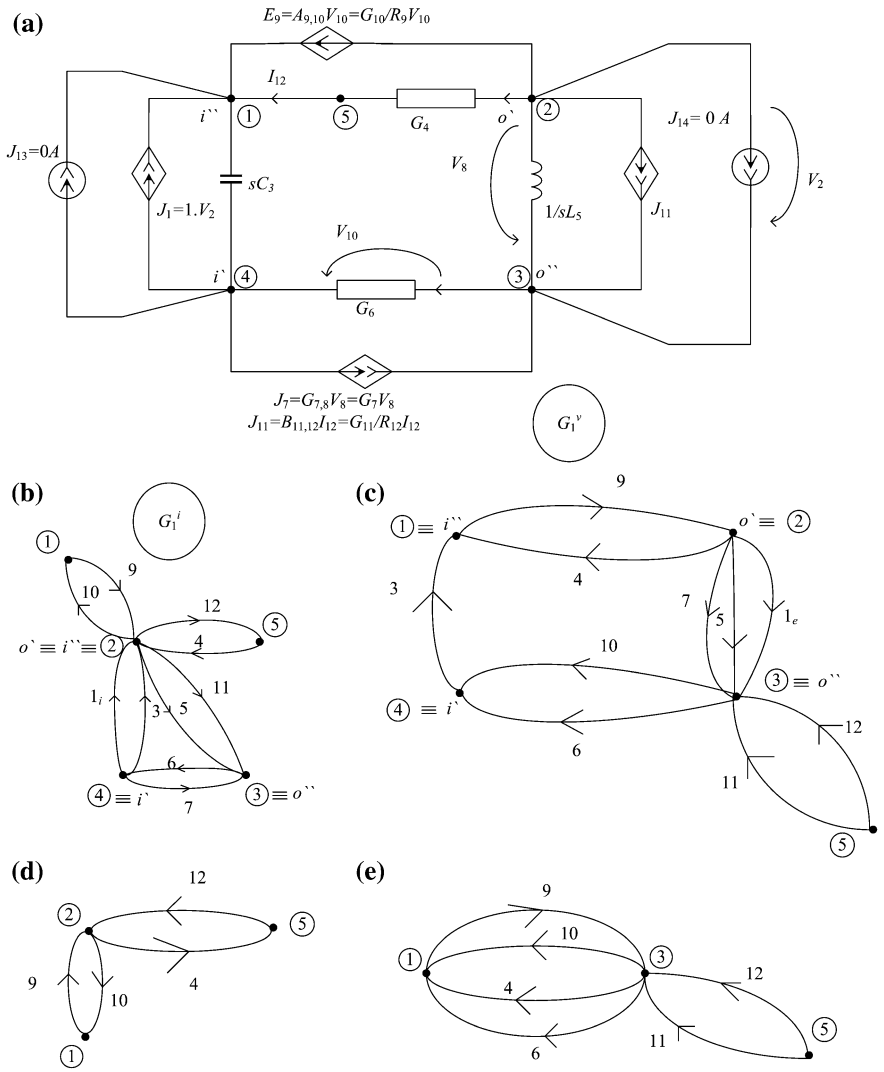


Fig. 21 A linear circuit and its pairs of graphs G_1^i and G_1^v, respectively G_p^i and $G_p^{v`}$

$$A_{pc} = \{(9,12);(10,12)\}, \tag{62}$$

Applying the above algorithm we obtain:

$$Y_{oi} = \frac{G_6G_9G_{12} + G_4G_{10}G_{11}}{(G_9 + G_{10})G_{12}} \tag{63}$$

or

$$Y_{oi} = \frac{R_4 R_{10} R_{11} + R_6 R_9 R_{12}}{R_4 R_6 R_{11} (R_9 + R_{10})}. \tag{64}$$

Expressions (61) and (62) have been compared with those obtained with the programs *TFSYG—Transfer Function SYmbolic Generation* and *CSAP—Circuit Symbolic Analysis Program*, [28, 29], and it has been observed that these are identical.

Remarks

1. The trees common to the graphs G_1^i and G_1^v, that contain the common branch of weight 1, are identical with the trees common to the graphs $G^i_{1,\,1_{i,\,sc}}$ and $G^v_{1,\,1_{o,\,sc}}$, obtained from the graphs G_1^i and G_1^v, in which the branches 1_i and 1_o are short-circuited.
2. In the case of the nonlinear circuits, any of the four transfer functions of the circuit can be calculated with formula (35) or (58), at every time moment $t_{n+1} = t_n + 1$, by making the circuit passive and by linearization around the operating point at this time moment.

Example 4 Let be the small signal equivalent circuit of a three-stage CMOS transistor amplifier, represented in Fig. 22. The voltage transfer (gain) factor has to be generated symbolically, in relation to the input-output ports, 1–5 and 4–5, respectively.

Using the algorithm based on the graph decomposition on levels, respectively of the SATE (Symbolic Analysis by Tree Enumeration) software [14, 21], we can proceed as follows:

1. The input file, ex2.cir, has to be edited with the following structure:

   5 13 314.00000000000000E + 0001 *(nodes number, branches number, pulsation)*
   1 1000.0 1 5 *(branch type, parameter value, initial node, final node)*

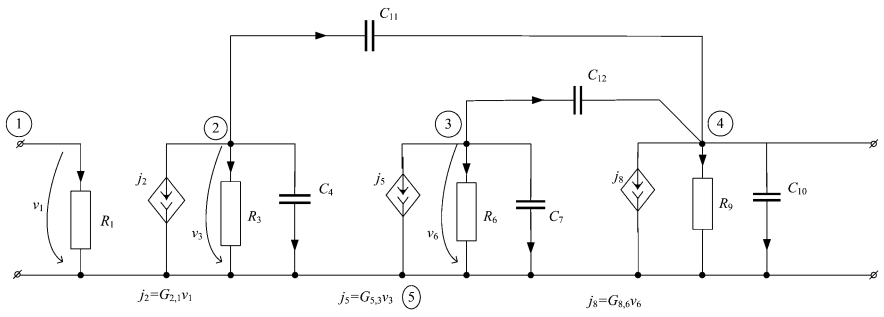


Fig. 22 Equivalent scheme of a small signal amplifier

9 0.001 0.0 2 5 1 5 *(9-source j(u), real value, imaginary value, initial node, final node for the controlled variable, initial node, final node for the controlling variable)*
1 1000.0 2 5
2 0.1e−08 2 5
9 0.001 0.0 3 5 2 5
1 1000.0 3 5
2 0.1e−08 3 5
9 0.001 0.0 4 5 3 5
1 20000.0 4 5
2 0.1e−08 4 5
2 0.1e−08 2 4
2 0.1e−08 3 4
12 1 5 4 5 (input and output ports)

1. After SATE program running, the following results are obtained:

Terms of the circuit function counter	
Sign factor	The value of common trees (in admittances)
1	$C_7C_{11}G_{2\_1}s^2$
1	$G_{2\_1}G_{5\_3}G_{8\_6}$
−1	$C_{12}G_{5\_3}G_{2\_1}s$
1	$C_{11}C_{12}G_{2\_1}s^2$
1	$C_{11}G_6G_{2\_1}s$

Terms of the circuit function denominator			
Sign factor	The value of common trees (in admittances)	Sign factor	The value of common trees (in admittances)
1	$C_{11}G_3G_6s$	1	$C_7C_{10}C_{11}s^3$
1	$C_4C_{11}G_6s^2$	1	$C_7C_{12}G_3s^2$
1	$G_3G_6G_9$	1	$C_4C_7C_{12}s^3$
1	$C_4G_6G_9s$	1	$C_7C_{11}C_{12}s^3$
1	$C_{11}G_6G_9s$	−1	$G_{5\_3}G_{8\_6}C_{11}s$
1	$C_{10}G_3G_6s$	1	$C_{11}C_{12}G_{5\_3}s^2$
1	$C_4C_{10}G_6s^2$	1	$C_{11}C_{12}G_3s^2$
1	$C_{10}C_{11}G_6s^2$	1	$C_4C_{11}C_{12}s^3$
1	$C_{12}G_3G_6s$	1	$C_{12}G_3G_{8\_6}s$
1	$C_4C_{12}G_6s^2$	1	$C_4C_{12}G_{8\_6}s^2$
1	$C_{11}C_{11}G_6s^2$	1	$C_{11}C_{12}G_{8\_6}s^2$
1	$C_4C_7G_3s^2$	1	$C_{12}G_3G_9s$
1	$C_4C_7C_{11}s^3$	1	$C_4C_{12}G_9s^2$
1	$C_7G_3G_9s$	1	$C_{11}C_{12}G_9s^2$
1	$C_4C_7G_9s^2$	1	$C_{10}C_{12}G_3s^2$

(continued)

(continued)

1	$C_7C_{11}G_9s^2$	1	$C_4C_{10}C_{12}s^3$
1	$C_7C_{10}G_3s^2$	1	$C_{10}C_{11}C_{12}s^3$
1	$C_4C_7C_{10}s^3$		

If

$$G_1 = G_3 = G_6 = G, C_4 = C_7 = C_{10} = C_{11} = C_{12} = C, G_{2\_1} = G_{5\_3} = G_{8\_6} = G_m$$

then the voltage transfer gain becomes:

$$A_{oi} = -\frac{G_m\left[C^2s^2 + C(G - G_m)s + G_m^2\right]}{8C^3s^3 + C^2(3G_m + 10G + 4G_9)s^2 + C\left(GG_m + 3G^2 + 4G_mG_9 - G_m^2\right)s + G^2G_9}$$

The sensitivity of the voltage transfer gain in relation to the parameter G_m, $S_{G_m}^{A_{0i}} = \frac{\partial A_{0i}}{\partial G_m} \cdot \frac{G_m}{A_{oi}}$, has the expression:

```
Sei =(-16*C^4*s^4*Gm+28*C^4*s^4*G+8*C^4*s^4*G9+16*C^3*s^3*G^2+
+3*C^2*s^2*G^3+21*C^3*s^3*Gm^2+6*Gm^3*C^2*s^2+3*Gm^2*G^2*G9+
+16*C^5*s^5-20*C^3*s^3*G*Gm-8*C^3*s^3*Gm*G9+2*C^2*s^2*G^2*G9+
+4*C^3*s^3*G*G9-6*C^2*s^2*G^2*Gm+C*s*G^3*G9+
+29*C^2*s^2*Gm^2*G+8*C^2*s^2*Gm^2*G9+
+2*Gm^3*C*s*G+9*Gm^2*C*s*G^2+8*Gm^3*C*s*G9-
-2*C*s*Gm*G^2*G9)/((2*C^2*s^2+C*s*G-C*s*Gm+Gm^2)*(8*C^3*s^3+
+3*C^2*s^2*Gm+10*C^2*s^2*G+4*C^2*s^2*G9+C*s*G*Gm+3*C*s*G^2+
+4*C*s*Gm*G9+G^2*G9)).
```

For the numeric values $C = 1$ nF, $G = 0.001$ S, $G_m = 0.001$ S, $G_9 = 0.00005$ S and replacing s with $j\omega$, the voltage gain expression $A_{ei}(j\omega)$ becomes:

$$A_{oi}(j\omega) = -\frac{125000 \cdot (\omega^2 - 0.1 \cdot 10^{13})}{j\omega^3 + 0.165 \cdot 10^7\omega^2 - 4 \cdot 10^{11}j\omega - 625.10^{13}}.$$

Figure 23 shows the Bode diagram, and Fig. 24 presents the distribution of poles and zeros in the complex plane.

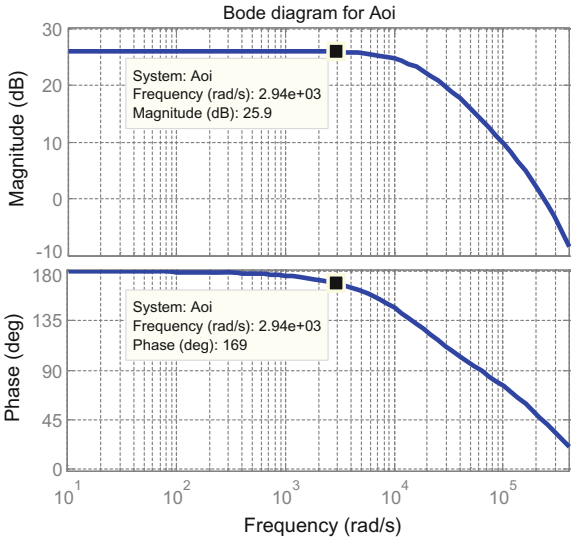


Fig. 23 Bode diagram for Aoi

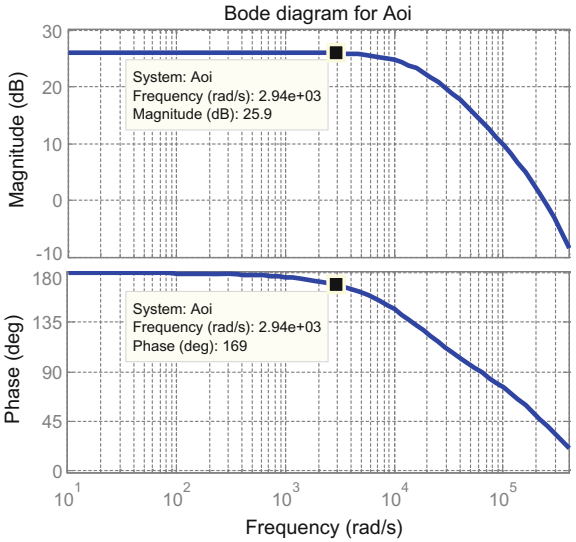


Fig. 24 Pole and zero locations of small signal amplifier

For the above numeric values, the output file provides the following data about the required circuit function:

Real part: +1.999243e + 01	Imaginary part: 4.022459e + 01
Module: 1.999648e + 01	Argument: 3.121475e + 00

Example 5 The circuit in Fig. 25a, contains two operational amplifiers and passive circuit elements R, C. This circuit operates in a permanent harmonic regime as a capacitance multiplier with respect to the input terminals (4−5). By replacing the operational amplifiers with the equivalent scheme of Fig. 25b, the equivalent circuit represented in Fig. 25c, is obtained. The complex input impedance $\underline{Z}_{ii}(\omega)$ (with respect to the input terminals 4−7) has to be calculated with SATE.

For the case when the resistances $R_5 = R_7 = 0\,\Omega; R_4 = R_6 = 1$ Meg; $C_3 = 10$ pF (node 6 becomes 1, node 5 becomes 3, node 7 becomes 5, and the resistance R_6 becomes R_5) and the voltage gains $a_{8\_4} = a_{9\_6} = 2 \cdot 10^5$, the input file required by the SATE software, *ex3.cir*, has the following structure:

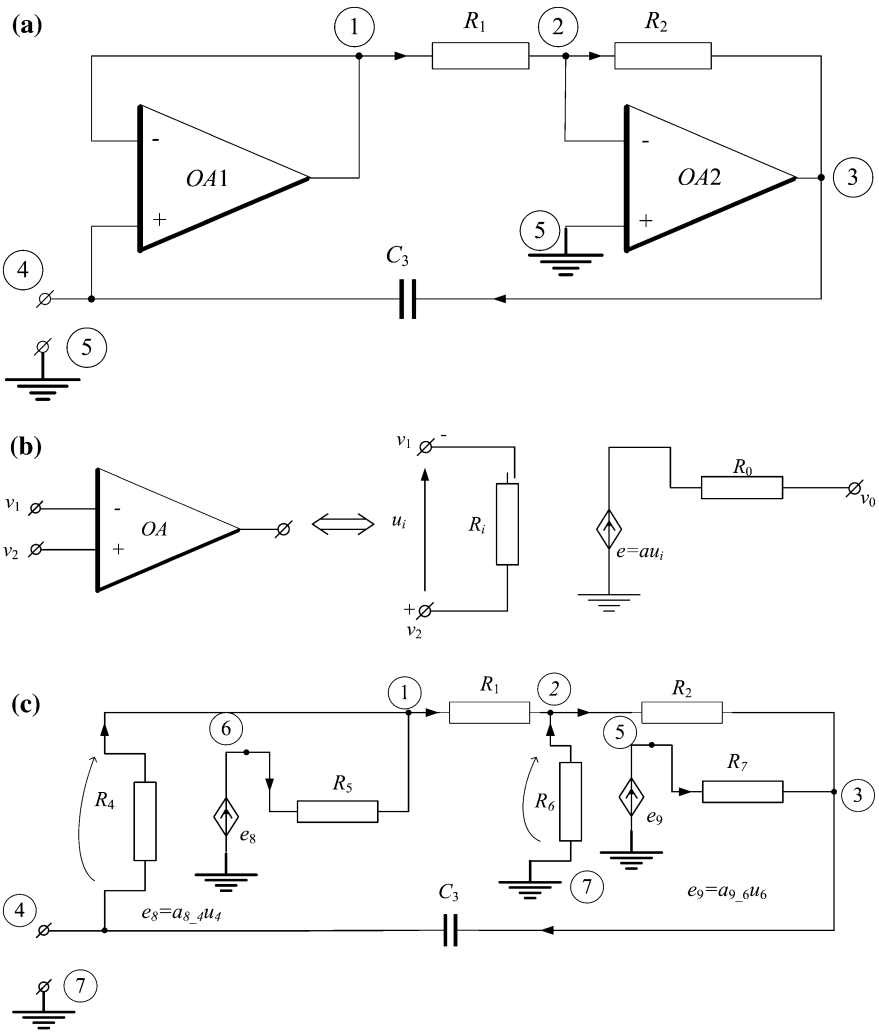


Fig. 25 Capacitance multiplier

```
5 8 314.0
1 100.0 1 2
1 1e + 05 2 3
2 1e−11 3 4
1 1e + 06 4 1
1 1e + 06 5 2
10 2e + 05 0.0 5 1 4 1
10 2e + 05 0.0 5 3 5 2
12 4 5 4 5
```

For homogeneous controlled sources ($e_c(v_C)$ and $j_c(i_C)$), the program assigns two branches to each source (in this sequence: the controlled branch, the controlling branch). For the considered circuit, in the above simplified situation, where e_8 becomes e_6 with the controlling branch l_7 and e_9 becomes e_8 with the controlling branch l_9, the corresponding voltage gains have the expressions:

$$a_{6\_7} = \frac{G_7}{G_6} \text{ şi } a_{8\_9} = \frac{G_9}{G_8},$$

where: $G_7 = 1$ S and $G_9 = 1$ S, and $G_6 = G_8 = 1/2 \cdot 10^5$ S.

Results from the output file are as follows:

Terms of the circuit function numerator		Terms of the circuit function denominator	
Sign factor	The value of common trees (in admittances)	Sign factor	The value of common trees (in admittances)
1	$G_1G_6G_8$	−1	$j\omega C_3G_5G_6G_8$
1	$G_1G_7G_8$	−1	$j\omega C_3G_5G_7G_8$
1	$G_2G_6G_8$	−1	$G_4G_5G_6G_8$
1	$G_2G_6G_9$	−1	$G_1j\omega C_3G_6G_8$
1	$G_2G_7G_8$	−1	$G_1j\omega C_3G_7G_8$
1	$G_2G_7G_9$	−1	$G_1j\omega C_3G_7G_9$
1	$G_5G_6G_8$	−1	$G_1G_4G_6G_8$
1	$G_5G_7G_8$	−1	$G_2j\omega C_3G_6G_8$
		−1	$G_2j\omega C_3G_6G_9$
		−1	$G_2j\omega C_3G_7G_8$
		−1	$G_2j\omega C_3G_7G_9$
		−1	$G_2G_4G_6G_8$
		−1	$G_2G_4G_6G_9$

For the numeric values, the output file of the program provides the following data about the required circuit function:

Real part: 5.010559e−001	Imaginary part: −3.165607e + 005
Module: 3.165607e + 005	Argument: −1.570795e + 000

If the two operational amplifiers are considered identical ($a_{6\_7} = a_{8\_9} = A$) and the resistances $R_4 = R_6 \to \infty$, while R_5, $R_7 = 0\,\Omega$, then the input complex impedance expression becomes

$$Z_{ii}(\omega) = \frac{(1+A)\cdot[A(G_1+G_2)+G_2](G_2)}{j\omega C_3[A^2(G_1+G_2)+A(G_1+2G_2)+G_1+G_2]}$$

Assuming that the operational amplifiers are ideal $(A \to \infty)$ we obtain:

$$\underline{Z}_{ii}(\omega) = \frac{G_2}{j\omega C_3(G_1+G_2)} = \frac{1}{j\omega C_3\left(1+\frac{R_2}{R_1}\right)}.$$

The input impedance sensitivity, in respect of the conductance G_1, has the expression:

$$S_{G_1}^{\underline{Z}_{ii}(\omega)} = -\frac{G_1}{G_1+G_2}.$$

From the last expression of the complex input impedance an equivalent capacity results as:

$$C_e = C_3\left(1+\frac{R_2}{R_1}\right) = 10.10^{-12}\left(1+\frac{10^5}{10^2}\right) = 10.01.10^{-9}\ \text{F} = 10.01\ \text{nF}.$$

This capacitance is about a thousand times greater than capacity C_3. This circuit is used in integrated circuits technology to achieve high capacities. Due to miniaturization, integrated circuit technology usually produces capacitors with low capacities. The multiplication effect of the capacity is called *the Miller effect* for capacities [20, 27].

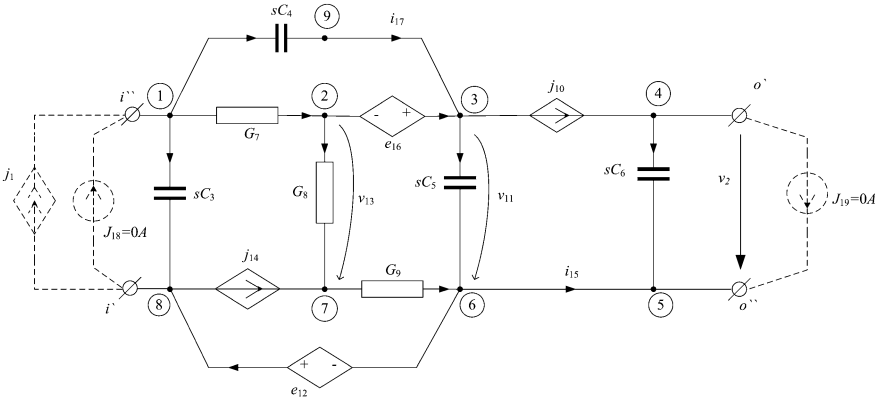


Fig. 26 A circuit containing all types of controlled sources

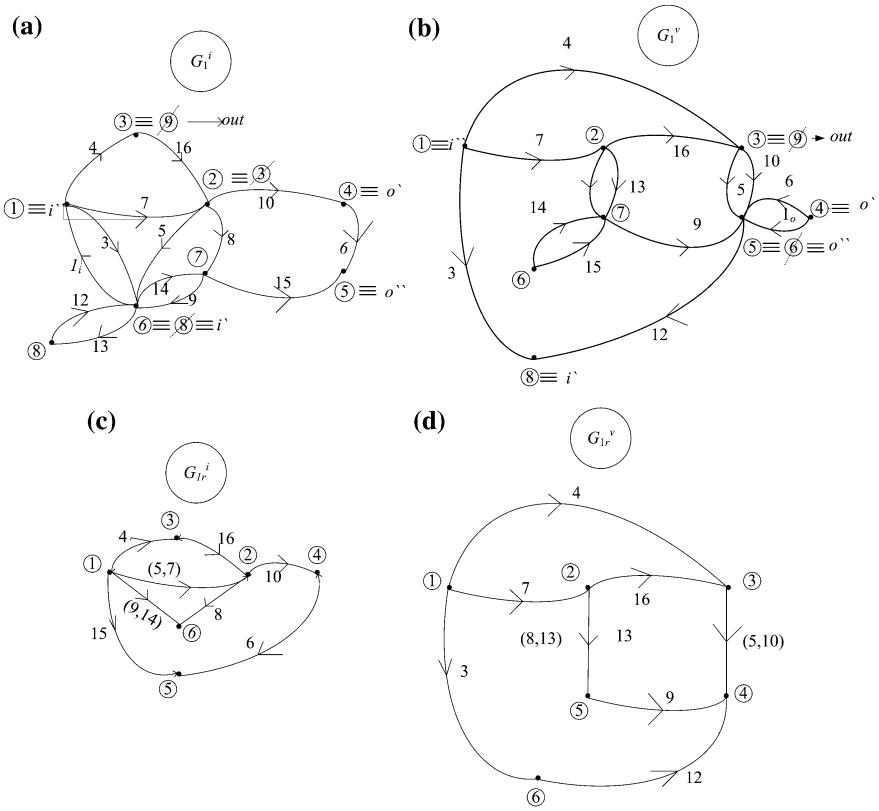


Fig. 27 The complete graphs $\left(G_1^i, G_1^v\right)$ and the reduced ones $\left(G_{1r}^i, G_{1r}^v\right)$

Example 6 The circuit containing all the types of controlled sources shown in Fig. 26, has the graphs $\left(G_1^i, G_1^v\right)$ shown in Fig. 27a and b. By performing the contractions presented in paragraph 6, we obtain the reduced graphs $\left(G_{1r}^i, G_{1r}^v\right)$ shown in Fig. 27c and d.

After operating the simplifications, the number of spanning trees in the two reduced graphs becomes much smaller. If we make similar simplifications in the graphs $\left(G_p^i, G_p^v\right)$, shown in Fig. 28a and b, we get the reduced graphs $\left(G_{pr}^i, G_{pr}^v\right)$ from Fig. 28c and d. The results of these simplifications are shown in Table 6. The number of trees in a graph has been calculated as it is presented in [20, 27].

We can observe a significant reduction in the number of trees in this simplification phase.

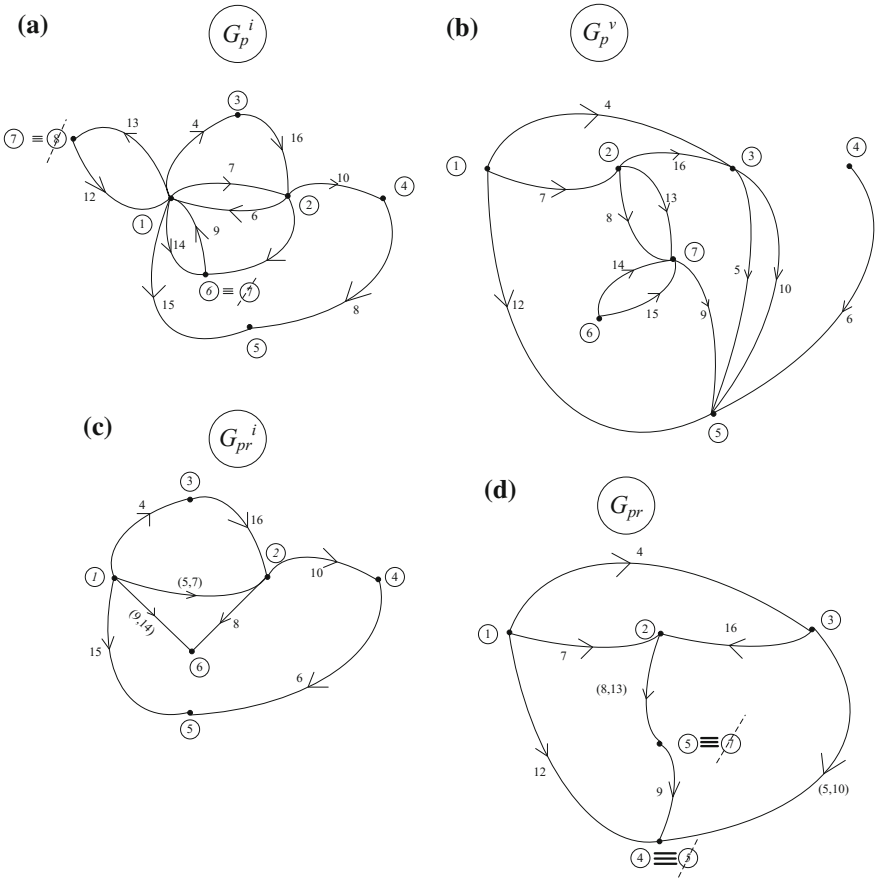


Fig. 28 The complete graphs $\left(G_p^i, G_p^v\right)$ and the reduced ones $\left(G_{pr}^i, G_{pr}^v\right)$

Table 6 The results of the simplification procedure

$n_{t,G_1^i} = 360 \Rightarrow n_{t,G_{1r}^i} = 28$	$n_{t,G_p^i} = 126 \Rightarrow n_{t,G_{pr}^i} = 28$
$n_{t,G_1^v} = 360 \Rightarrow n_{t,G_{1r}^v} = 28$	$n_{t,G_p^v} = 122 \Rightarrow n_{t,G_{pr}^v} = 24$

The command equations of the controlled sources are as follows:

$$j_1 = 1 \cdot v_2, e_{12} = a_{12,13} v_{13} = R_{12} G_{13} v_{13} = \frac{G_{13}}{G_{12}} v_{13},$$

$$j_{14} = b_{14,15} i_{15} = G_{14} R_{15} i_{15} = \frac{G_{14}}{G_{15}} \mathrm{i}_{15}, e_{16} = R_{16} i_{17} = \frac{1}{G_{16}} i_{15}.$$

The above simplifications do not affect the accuracy of the calculation, because they are operated in the graphs structure, which simplifies it, maintaining their equivalence.

If we consider $C_3 = C_4 = C_5 = C_6 = C$; $G_7 = G_8 = G_9 = G$, then the voltage gain factor Aoi has the following expression:

$$Aoi := G12\,G15\,G10\,((2.\,G16\,C\,G + 3.\,C\,G^2)\,s + 2.\,G16\,G^2)\,/\,(\\ (3.\,G15\,C^2\,G12\,G^2 - 3.\,G15\,C^2\,G13\,G^2 + 4.\,C^2\,G16\,G12\,G15\,G - 2.\,C^2\,G16\,G13\,G15\,G)\,s^2 + (2.\,C\,G10\,G15\,G12\,G16\,G \\ + 3.\,C\,G12\,G15\,G16\,G^2 + 3.\,G15\,C\,G10\,G13\,G^2 - 2.\,C\,G16\,G13\,G15\,G^2 + C\,G10\,G14\,G12\,G16\,G \\ + 2.\,G16\,C\,G13\,G10\,G15\,G)\,s + 2.\,G16\,G13\,G10\,G15\,G^2)$$

For the numeric values of the parameters

$$C = 1.0\text{e}04\ \text{F};\ G = 0.0001\ \text{S};\ G_{10} = 0.0002\ \text{S};\ G_{16} = 0.0001\ \text{S};$$
$$G_{14} = 2.0\ \text{S};\ G_{15} = 1.0\ \text{S};\ G_{13} = 4.0\ \text{S and}\ \ \text{G}_{12} = 1.0\ \text{S}.$$

Figure 29 shows the Bode diagram, and Fig. 30 presents the distribution of poles and zeros in the complex plane.

Example 7 The analog circuit shown in Fig. 31 contains all four types of linear controlled sources. The graph pairs $\left(G_1^i, G_1^v\right)$, and $\left(G_p^i, G_p^v\right)$, generated according to the rules presented in Sect. 5, are given in Figs. 32 and 33, respectively.

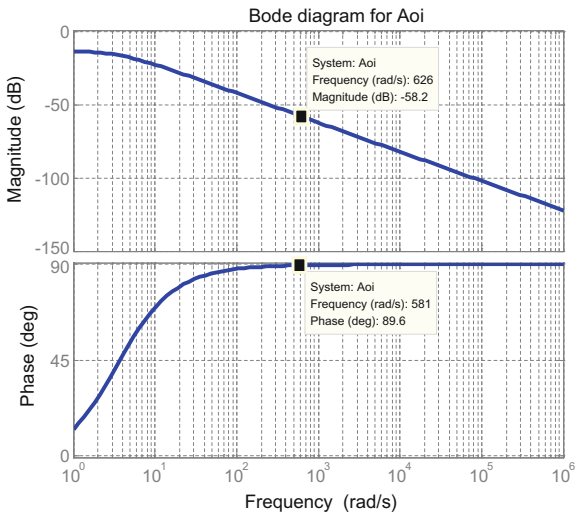


Fig. 29 Bode diagram for A_{oi}

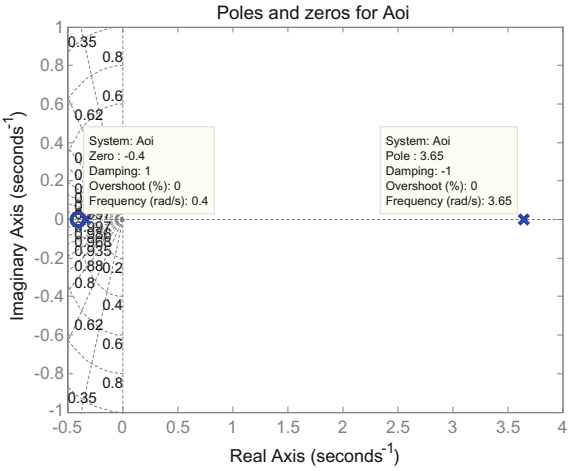


Fig. 30 Pole and zero locations of small signal amplifier

At the beginning, we generate the voltage gain $A_{oi\_ex}(s)$, and we evaluate it at the nominal parameter values, keeping only the complex frequency s as a symbol. Then we compute the transfer function sensitivity A_{oi_ex} (s, x) in respect of each parameter x. The analysis is performed considering an initial sampling in the frequency range of interest and checking the error in some intermediate points. The circuit elements that have a small value of the relative sensitivity in this frequency range can be eliminated. To this end both zero-admittance (element removal) and a zero-impedance (contraction of the terminal nodes) can be used. The value of the voltage gain in which some nodes/branches have been contracted/eliminated, $A_{oi\_ap}(s)$, is computed.

The magnitude and phase errors are given by:

$$\varepsilon_{|A_{oi}|} = \frac{|A_{oi\_ex}(j\omega)| - |A_{oi\_ap}(j\omega)|}{|A_{oi\_ex}(j\omega)|}, \tag{65}$$

$$\Delta\phi_{A_{oi}} = \frac{\arg(A_{oi\_ex}(j\omega)) - \arg(A_{oi\_ap}(j\omega))}{\arg(A_{oi\_ex}(j\omega))}. \tag{66}$$

For the circuit in Fig. 31 we find that only the capacitor C_{22} can be eliminated by contraction of its nodes, because the voltage gain sensitivity is small in the frequency range of interest, as it is shown in Fig. 34. In Fig. 35 the error variations in the same frequency range of the transfer function magnitude and of the transfer function phase are represented.

After the capacitor C_{22} removal, and applying the above procedure we obtain the reduced graphs $\left(G^i_{1r}, G^v_{1r}\right)$ and $\left(G^i_p, G^v_p\right)$. The tree number reduction of these graphs is shown in Table 7.

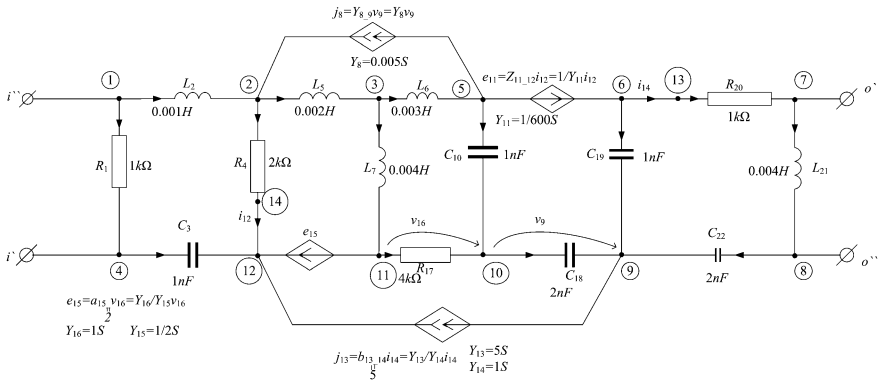


Fig. 31 Circuit diagram

If the representation of the inductors and controlled sources based on the unity gyrator model [3, 4], is used, the number of trees in the current graph increases at least at 2821968 (612 times bigger than with our models). The running time to enumerate these trees on an AMD XP 2700, 2.16 GHz, 512 MB of RAM is presented by comparison in Table 8.

The next step is to generate the numerator and the denominator expressions of the transfer function in the decreasing order of the complex frequency powers, and the coefficients of each complex frequency power in the decreasing order of their values. In this way we can eliminate one by one, the terms with the smallest values, if an error criteria for the magnitude and phase is verified over the frequency range.

The numerator of the voltage gain for the analog circuit in Fig. 31 has the following full symbolic expression:

$$\begin{aligned} numerator :=\ & C3\ C18\ L21\ Y14\ (L6\ C10\ L7\ Y15 + L5\ L6\ C10\ Y15 + L5\ C10\ L7\ Y15)\ s^4 \\ & + C3\ C18\ L21\ Y14\ (L7\ C10\ R17\ Y15 + C10\ L7\ R17\ Y16 + L5\ C10\ Y15\ R17)\ s^3 \\ & + C3\ C18\ L21\ Y14\ (L5\ Y15 + L7\ Y15 + Y11\ R4\ L7\ Y15)\ s^2 \end{aligned} ,$$

and the denominator contains 387 terms.

According to the above procedure of elimination we obtain finally a reduction in the transfer function denominator from 387 to 31 terms.

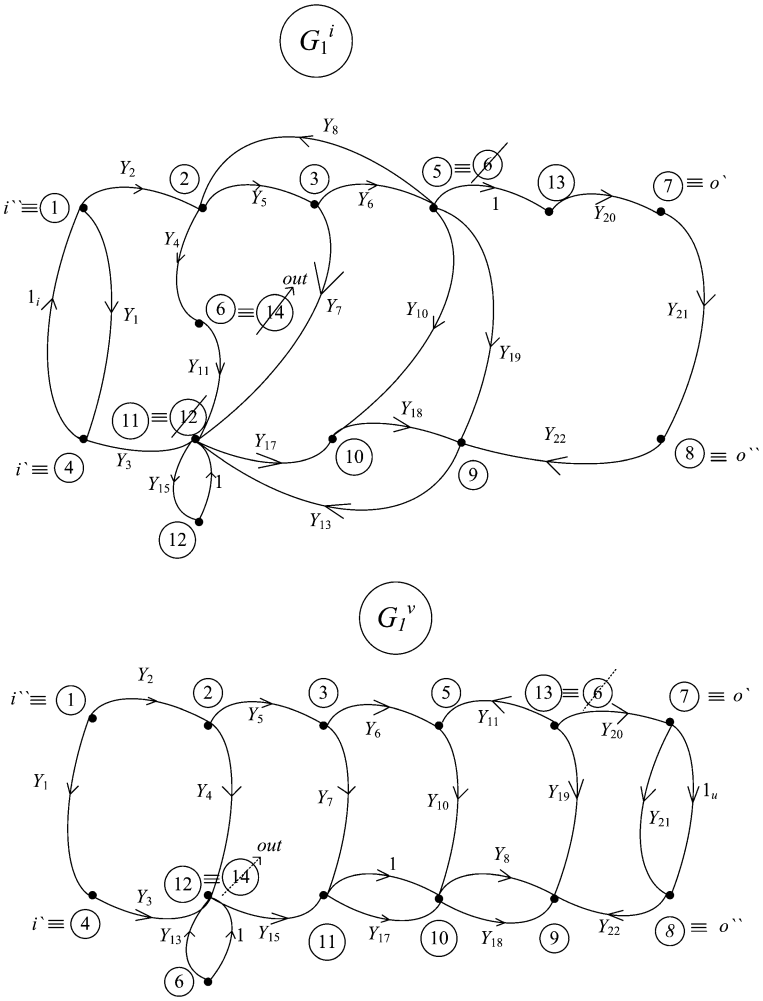


Fig. 32 $\left(G_1^i, G_1^v\right)$ graphs

In Fig. 36 the exact magnitude curve (502 terms in the denominator), that without C_{22} (387 terms in the denominator), and the approximated magnitude (31 terms in the denominator) are represented, and in Fig. 37 we can see the phase variation in the three cases. The maximum error of the transfer function magnitude is 1.6%.

A new method to formulate the system of equations in order to compute fully-symbolic small-signal characteristics of analog circuits by applying standard NA and/or loop current method has been presented.

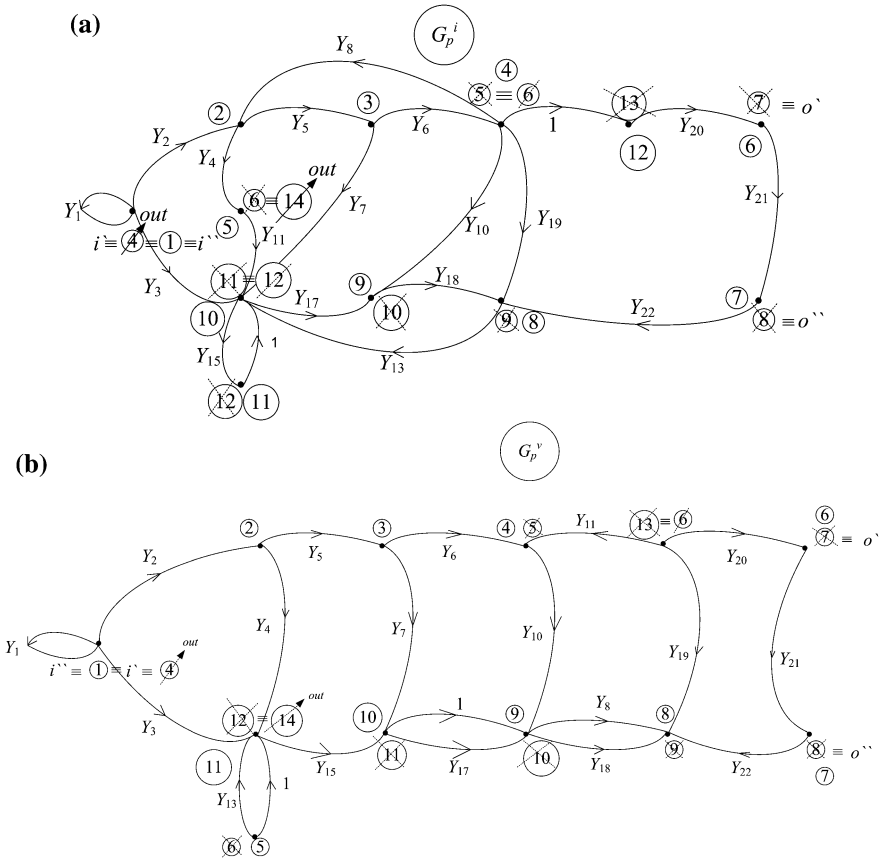


Fig. 33 $\left(G_p^i, G_p^v\right)$ graphs

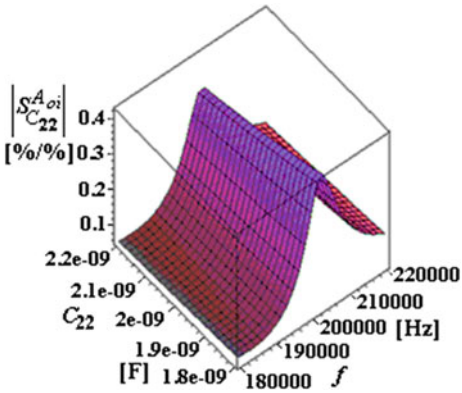


Fig. 34 Sensitivity magnitude function of C_{22} and frequency f

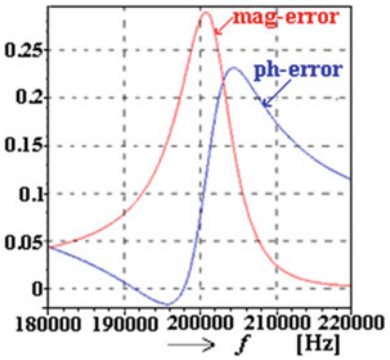


Fig. 35 Errors in voltage gain magnitude and in voltage gain phase

Table 7 Tree number reduction of the graphs from Figs. 32 and 33

$t_{G_1^i} = 4608$	$t_{G_1^v} = 3326$	$t_{G_p^i} = 4608$	$t_{G_p^v} = 3340$
$t_{G_{1r}^i} = 1792$	$t_{G_{1r}^v} = 209$	$t_{G_{pr}^i} = 1792$	$t_{G_{pr}^v} = 358$

Table 8 Comparison of running time for enumerating the trees corresponding to the graphs from Figs. 32 and 33

Number of trees	Time for tree	Enumeration [seconds]
	Algorithm on level	Char's algorithm
4608	≤ 1 μs	≤ 1 μs
2821968	1,781	4

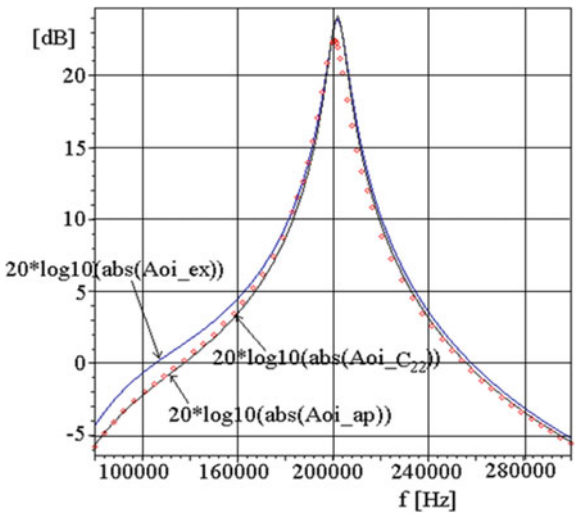


Fig. 36 Variation of the voltage gain magnitude in the frequency range

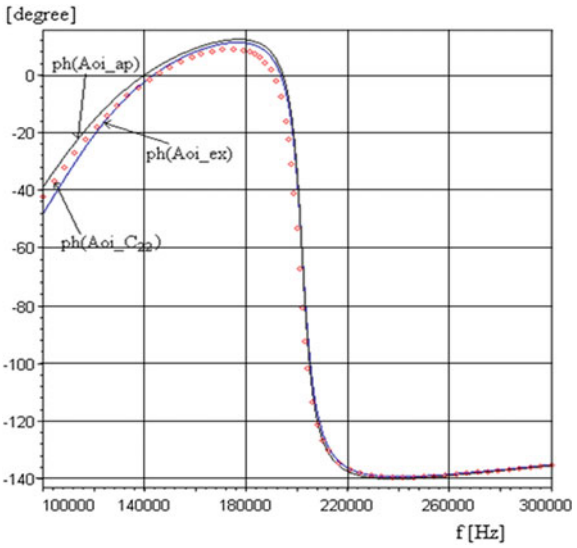


Fig. 37 Phase variation in the frequency range

7 Conclusions

By modelling electronic devices with equivalent circuits containing nullors and by associating to the analyzed circuit two graphs: one corresponding to the current one —G^i, necessary to formulate the KCL, and one corresponding to the voltage one— G^v, necessary to formulate the KVL, the nodal equations and the loop current equations can be formulated very simple for any non-reciprocal circuit. The two graphs have the same number of branches, nodes and independent loops, but they differ by their different positions they occupy in the two graphs, by the branches used to simulate the controlled sources and, in general, by the branches corresponding to the equivalent circuits containing nullors used to model the electronic devices. The characteristics of the branches are written using the voltages from the voltage graph and the currents from the current graph.

In this chapter, we propose a simple modelling procedure of the controlled sources in the two graphs. The equivalent circuits based on the functional schemes with nullors model both the controlling port and the controlled one by admittances placed in different positions in the two graphs. The two graphs obtained in this way have the same number of branches, nodes, and loops. A new method to formulate the system of equations in order to compute fully-symbolic small-signal characteristics of analog circuits by applying standard NA and/or loop current method has been presented.

A set of rules for generating and using the two graphs is stated, and the generalization of the topological formula to generate all network functions is proved. These rules are applicable to a linear circuit containing: all four types of linear controlled sources, resistors, inductors, capacitors, nullors (for ideal opamps

operating in the linear mode), and any multi-terminal or multiport circuit element having an equivalent scheme made up only by two-terminal elements and controlled sources.

The models with nullors for all active electronic devices are more effective for the optimization of design and simulation time during the analysis process. From this point of view, the nullors proved already their efficiency in the active devices modelling. In the models based on nullors, the parasitic elements can be included to analyze their contribution to the analog circuit response. All the four controlled sources can also be represented with equivalent circuits using nullor elements. Consequently, the nullors are very useful for the analog circuits modelling because the circuit topology can be described using only two-terminal components like resistors, capacitors, nullators, norators, independent and controlled sources. Considering that the model should be developed in the simplest manner and the accuracy of the circuit behaviour simulation must be in acceptable limits, this chapter will show the problems related to the small-signal models of the active devices modelled with nullors.

Unlike other similar approaches our approach does not introduce supplementary branches and nodes with respect to initial circuit. Moreover, the number of nodes in the two graphs is smaller than in the initial circuit with the number of CCVS. Modelling the controlled sources by admittances allows an efficient generation of the network functions via the generalized topological formula with homogeneous parameters. This formula works for linear nonreciprocal networks containing any type of controlled sources. The rules for the automated generation of the two graph pairs using the controlled source models proposed in this chapter and a representation on levels of the graphs were implemented in a very fast program for the symbolic transfer function computation.

The generalized topological formula can generate any network function in a full symbolic form for very large-scale analog circuits because the numerator and the denominator terms are generated one by one and stored as lists. This gives the superiority of the topological approach in contrast to the determinant method that cannot provide a full symbolic form because of the symbolic manipulator that cannot solve huge systems of algebraic equations.

The list form in which the numerator and the denominator are obtained also allows performing the simplification after generation in a simple manner.

Examples have been introduced to show the usefulness of the nullor-based models and the potential of the proposed approach for the analysis and design of the analog linear/nonlinear circuits.

From two-port and four-terminal network point of view, all the proposed models have been generated by taking into account the impedance levels associated to the input-output terminals along with the gain-equations of the active devices. As one can see throughout the chapter, the nullor-based models are not complex and they can quickly be included into symbolic analyzers. Further, nullor-based active device models by including parasitic elements, has also been introduced. Furthermore, a novel method to formulate the system of equations in order to compute fully-symbolic small-signal characteristics of analog circuits by applying only

standard NA has been presented. Thus, by using the relationships of nullators and norators and by manipulating their data-structures, the admittance matrix can quickly be constructed, avoiding waste of CPU-time and memory in the formulation process. Examples have been introduced to show the usefulness of the nullor-based models and the potentiality of the proposed formulation method

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Symbolic Sensitivity Analysis Enhanced by Nullor Model and Modified Coates Flow Graph

Irina Asenova and Franciszek Balik

Abstract In this chapter it was shown, how such the pathological elements like nullors can be exploited to symbolic sensitivity analysis enhancement. A method of first-, second-order and multiparameter symbolic sensitivity determination based on the nullor model of active devices and modified Coates flow graph is presented. The method performs symbolic sensitivity analysis with respect to various circuit parameters appeared not only at one location in the nullor model, respectively in the modified Coates flow graph. Illustrative examples on symbolic sensitivity analysis are given. In symbolic sensitivity analysis very important role plays the number of additionally generated expressions and in consequence additional number of arithmetical operations. The main drawback of some methods based on the adjoint graph or on the two-graph technique, i.e. the necessity to multiply analyze the corresponding graph, is avoided. Advantages of the method suggested are that, the matrix inversion is not required and due to the modified Coates graph this method is significantly simplified. Simplifications of the method introduced lead to the significant reduction of the final symbolic expressions without violation of accuracy. This simplification method can be considered as SBG–type (Simplification Before Generation) and has an important impact on symbolic analysis. In the chapter, it was shown that the presented method is more effective than the transimpedance method taking the number of arithmetical operations and the circuit insight into consideration. Comparison results for the multiparameter sensitivity calculations of the voltage transfer function for a fourth-order low pass filter and a second-order high pass filter are presented.

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1 Introduction

Sensitivity analysis plays an important role in determining the critical design variables in analog circuit analysis and synthesis [1, 2]. Symbolic analysis opens up new possibilities for the development of computer-aided design tools that can analyze an analog circuit topology and automatically size the components for a given set of specifications. Symbolic circuit analysis, its advantages and differences with numerical methods and first symbolic simulation is describes in [3]. A symbolic simulator performs the same function as the designers traditionally do by hand analysis. The difference is that the analysis is now much faster done by a computer, and does not make many errors [4]. Sensitivity analysis is used in a wide range of areas such as prediction and evaluation of change in the characteristics of a network due to the change in the parameters, and optimization design of the network [5]. The Modified Coates Flow Graph (MCFG) [6] allows to simplify the analysis of first-order sensitivity on the base of some network partial transfer functions [7, 8]. According to the classical formulae, the calculation of the first- and second-order transfer function sensitivities needs in the first place to find the corresponding derivatives. This is the main problem sensitivity analysis and its investigation is an object of some special methods, described in the literature [9, 10]. Once the circuit equations are derived, the relevant derivatives of each equation can be computed symbolically and then the differential sensitivity can be calculated using the chain rule of differentiation. This solution was proposed first in [11] and was extended in [12, 13] by representing a sequence of expressions (SoE) as directed acyclic graph (DAG) and providing an algorithm for analyzing the DAG. Although the method is conceptually simple it does not always generate the optimal sequence [13]. This is due to the fact that the number of additional expressions, required for sensitivity calculations, heavily depends on the position of the symbol with respect to which the derivatives are calculated. The Transimpedance (TI) method overcomes these drawbacks [2]. Another additional property of the Transimpedance method is that it can be easily used in symbolic large-change multiparameter sensitivity analysis [14]. The main drawback of some methods based on the adjoint graph is the necessity to analyze the corresponding graph twice [15] and the suggested method gets over it. Coates flow graph (CFG) is useful and often used in the network theory and in the linear system theory [16]. On the other hand, the main factor that plays important meaning during the analysis of an active electrical network is offering a simplified basis that must present all its active elements. Authors in the paper [17] proved a theorem that determinates the basis consisted by passive elements and only one active element, i.e. a nullor. It is used as a universal active element for an equivalent representation of active networks [18–21] for instance two-ports active networks, depended sources, transistors, amplifiers and etc. However, the input-output resistance and capacitance, gain, input offset voltage or current and the frequency response are all finite. This is the reason to include these effects in the nullor-based models [22], chap. 3. In this manner, any analog network can be modeled with nullors and impedances, and the equivalence between them is

introduced in [22–24]. The nullor equivalents of the pathological elements voltage mirror and current mirror and their application to symbolic analysis were introduced in [25]. In this chapter, the equivalent nullor model of the active circuit is a starting point for the sensitivity analysis. On the base of nullor models using some network partial transfer functions, a method for the first-order sensitivity analysis of active networks is describe in [26]. This method is improved and simplified in [27, 28] using the modified Coates flow graph [29]. An algorithm and a computer program "HoneySen" illustrate the method proposed [28]. The symbolic equations generated by symbolic analysis help not only understand the first-order functional behavioral of an analog circuit, but also provide insight into second-order effects in the circuit. In some network optimization schemes, it is desirable to know the dependence of first-order sensitivity on the elements of the network [6, 30]. In [31–33] the nullor model is combined with the MCFG aiming at the calculation of the multiparameter sensitivity (MS) in a symbolic form. The sequence of numbering the nodes in the equivalent nullor model is very important for the symbolic sensitivity analysis and for the input data of the special software developed. Sometimes after the nullor equivalent transformations a nullor model with some particular connections between its elements can be gotten. In the presented chapter they are considered and the right sequence of numbering of the nodes in the nullor model is presented, for instance:

- when a nullator or more nullators are connected with the source vertex, i.e. the source vertex is an isolated one in the equivalent nullor model;
- when a norator is connected between two nullators;
- when a norator or more norators are connected with the source vertex;
- when a norator and a nullator are connected with the source vertex;
- when norators have a common node in the equivalent nullor network.

2 Nullor-Modified Coates Flow Graph Symbolic Sensitivity Analysis Method

The nullator and norator [20] are elements that could facilitate the symbolic sensitivity analysis of active circuits by applying nodal analysis (NA). As a result of the combination between nullor representation and modified Coates flow graph (FG), an expression for a first-, second order and multiparameter symbolic sensitivity analysis is obtained.

2.1 Composing of an Equivalent Nullor Model

This section analyses a case when more than one parameter is likely to vary in a given circuit. Suppose that p parameters exist having very small fractional perturbations from their nominal values. According to [22–25] an equivalent nullor model N is composed by a designer. Let us assume that there are $m + n + R + 1$ nodes, where R is the number of the nullors in N. In accordance with [26, 28] the nodes, numbered from 1 to m represent network sources, nodes from $m + 1$ to $m + n$ are inner nodes, that all or some of them can be considered as outgoing nodes, and the node $m + n + 1$ is the common node for the nullor model. The sequence of the nodes in the nullor model is determined as follows:

- Incoming (sources) nodes—1,…, m;
- Outgoing nodes as follows:
  - p nodes, connected to edges with passive elements;
  - N_e nodes, connected with the ground by a norator;
  - 2 N_f nodes, connected with N_f norators;
  - N_{fr} nodes, connected with a norator that is situated between 2 nodes, one of them is connected with a nullator;
  - $n_f^{'}$ nodes that are one of the two nodes, connected with the nullators;
- $R = n_f + n_e$ nodes that are removed as follows:
  - n_f nodes, corresponding to the second node, connected with the nullators;
  - n_e nodes, connected with the nullators grounded.

Once the nullor model is established, a modification of the initial modified Coates flow graph, representing the equivalent nullor model, is implemented. This modification, performed according to the algorithm described in [27], reflects the nullor influence on the network transfer functions, reduces the nullor model complexity, and the admittance matrix respectively. Due to this modification, R vertices from the initial modified Coates flow graph are removed. These vertices (nodes in the nullor model) correspond to the number of nullators and they are strictly determined, i.e. they are the last ones in the sequence of the numbering. In this manner, it is very clear between which two nodes (vertices) the transfer function is determined after the reduction of the nullor model complexity.

The reduction is implemented, and some transformations of the initial modified Coates flow graph are performed due to the rules described in [22] chap. 5.

The validity of the rules for modification of the initial flow graph is verified by comparison of the reduced admittance matrix with the one obtained using the nullor properties described in [20].

Sometimes after the nullor equivalent transformations [18] a nullor model with some special connections between its elements can be gotten. In the presented section they are considered and the right sequence of numbering of the nodes in the nullor model is shown.

2.1.1 A Nullator or More Nullators Are Connected with the Source Node

In this case the source node is appeared as an isolated one in the equivalent nullor model.

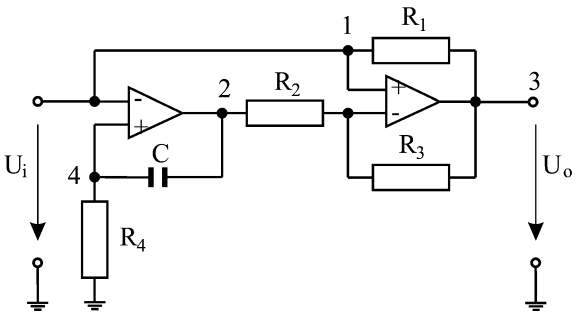
The sequence of the numbering of the nodes in ***N*** is determined as follows:

- incoming(sources) nodes—*1,…, m*;
- outgoing nodes—*m + 1,…, m + n* as follows:
  - p nodes, connected to edges with passive elements;
  - N_e nodes, connected to the ground by means of a norator;
  - 2 N_f nodes, connected *only* with N_f norators;
  - N_{fr} nodes, connected to a norator that is situated between two nodes, one of them is connected to a nullator;
  - $n_f^{'}$ nodes (that is one of the two nodes) connected with the nullators. *When a nullator or more nullators are connected with the source node, this node is missed at that point, because the source node is already numbered*;
- $R = n_f + n_e$ nodes that are removed, as follows:
  - n_f nodes, corresponding to the second node, connected to a nullator;
  - n_e nodes, connected to grounded nullators.
    When a nullator or more nullators are connected with the source node in the equivalent nullor model, then in the income data for the algorithm and for the computer program "HoneySen" the source node has to be connected with itself.

Example 2.1.1 Let us show the numbering of the nodes for the impedance converter shown in Fig. 1 and find its MCFG. The nodes, corresponding to the vertices in the initial CFG that dropout, have numbers 4 and 5. An equivalent nullor model *N* can be composed and it is shown in Fig. 2.

An initial form of the modified Coates signal flow graph for the passive part of the model is presented in Fig. 3. Following the sequence of modification in [22] Chap. 5, and the notes written in Sect. 2.1.1, we obtain MCFG shown in Fig. 4.

Fig. 1 Impedance converter



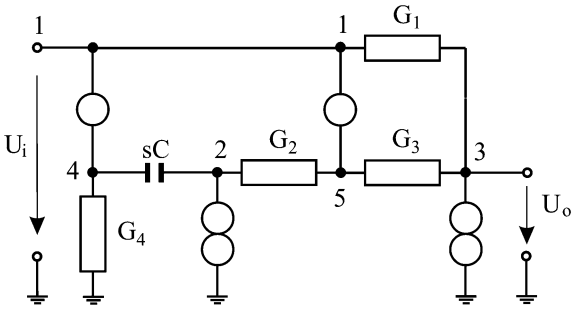


Fig. 2 Equivalent nullor model *N*

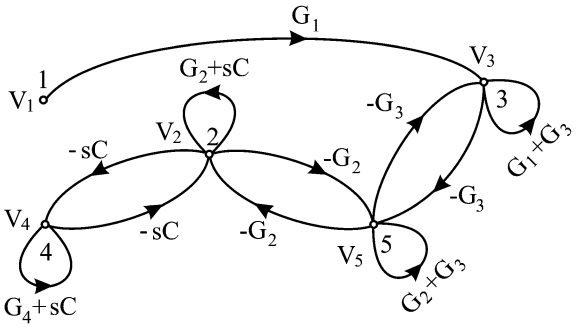


Fig. 3 Initial Coates flow graph

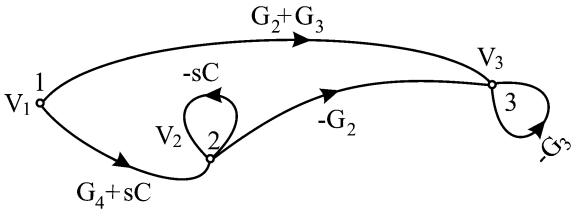


Fig. 4 Modified Coates flow graph

2.1.2 A Norator Is Connected Between Two Nullators in the Equivalent Nullor Model

The sequence of the numbering of the nodes in ***N*** is determined as the above sequence with the additional difference, namely:

– n_f' outgoing nodes, connected with the norator situated between two nodes, connected with nullators. This connection is considered only as two nullators in the equivalent nullor model. Then the common nodes between the norator and both of the nullators are chosen for outgoing ones.

Example 2.1.2 Let us find the Modified Coates flow graph for the equivalent nullor model shown in Fig. 5.

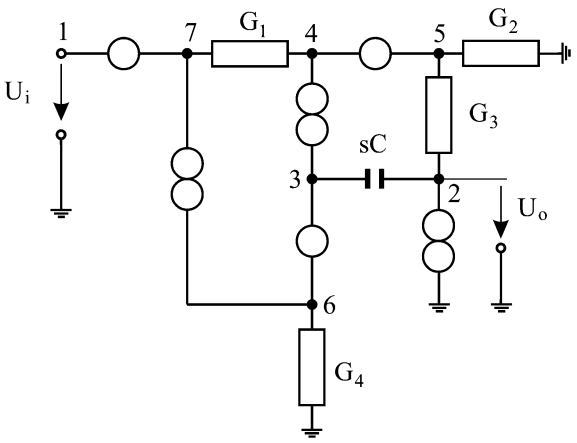


Fig. 5 Equivalent nullor model

According to the sequence of numbering, for the this special case, $m = 1, p = 0$, $N_e = 1, 2N_f = 0, N_{fr} = 0, n_f^{'} = 2$. As can be seen there are four outgoing nodes and three nodes, 5, 6 and 7, corresponding to the vertices in the initial Coates flow graph, that dropout.

The initial Coates flow graph for the passive part of the network follows from Fig. 5. It is shown in Fig. 6. Following the sequence of modification given in [22] we obtain equivalently transformed MCFG presented in Fig. 7.

2.1.3 A Norator or More Norators Are Connected with the Source Node

Example 2.1.3 Let us consider a converter of negative immitances (Fig. 8) with its equivalent nullor model ***N***, shown in Fig. 9.

As can be seen a norator is connected with the source vertex in ***N***. Important and at the same time, very simple act for the sensitivity determination is that the source

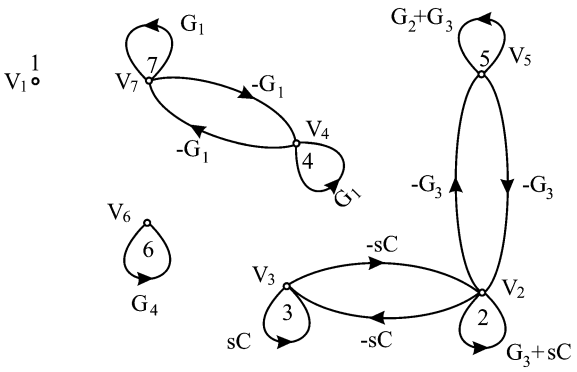


Fig. 6 Initial Coates flow graph

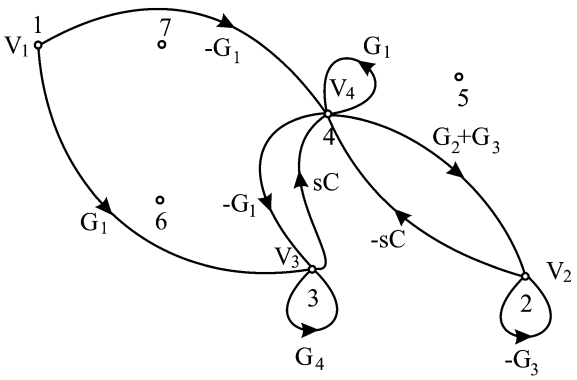


Fig. 7 Modified Coates flow graph

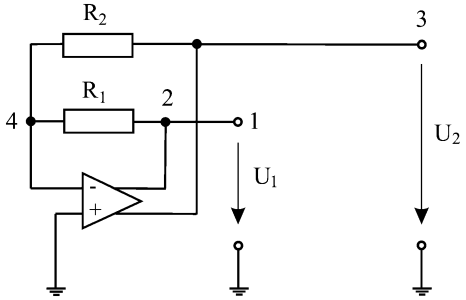


Fig. 8 Converter of negative immitances

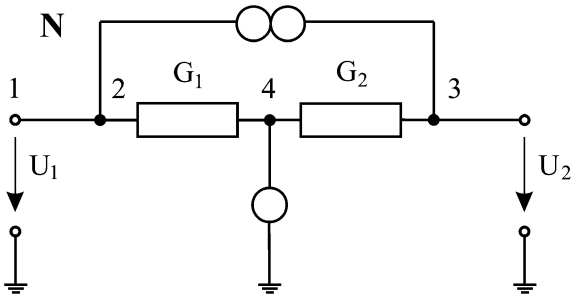


Fig. 9 Equivalent nullor model

vertex in the initial CFG, shown in Fig. 10, *has to be divided* [23] to two vertices (Fig. 11), connected with a transmission coefficient $t_{21} = G_3 = 1$. Later the sequence of the nodes is determined as it is defined in [26] (Fig. 12).

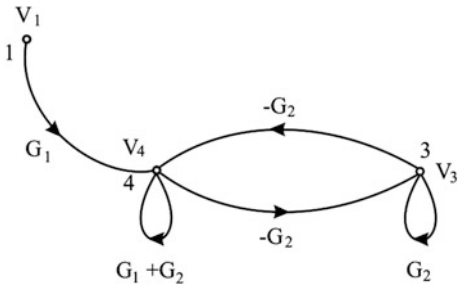


Fig. 10 Initial Coates FG

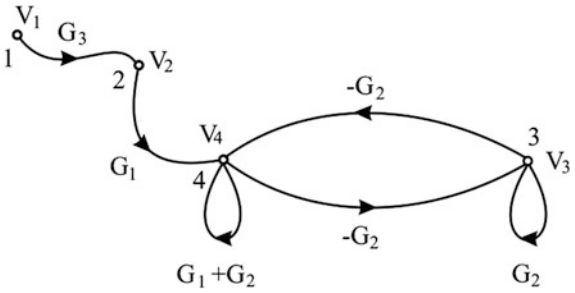


Fig. 11 Initial Coates FG with a source-vertex divided

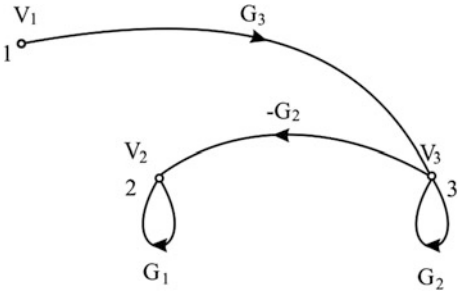


Fig. 12 Modified Coates flow graph

2.1.4 A Norator and a Nullator Are Connected with the Source Node

Then:

- the nullator is considered as one, connected between a pair nodes;
- the norator is considered as a norator, connected between a pair nodes in the nullor model, when one of the nodes is incident of the nullator.

Example 2.1.4 For an equivalent nullor model presented in Fig. 13, in the income data for the algorithm and the computer program according to [26] has to be written:

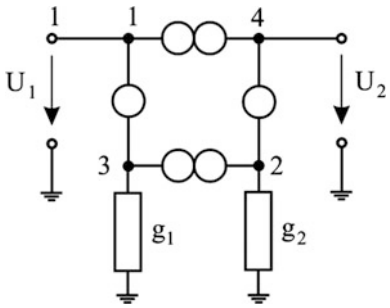


Fig. 13 Equivalent nullor model

- a number of the outgoing nodes: 2 nodes, as follows—1, 2;
- pairs nodes, connected with a nullator: 2 pairs, as follows (1, 3) and (2, 4);
- a norator between pair nodes, one of them is connected with a nullator: 2 norators between two pair nodes, as follows (1, 4) and (2, 3).

Then, $m = 1$, $p = 0$, $N_e = 0$, $2N_f = 0$, $N_{fr} = 2$, $n_f^{'} = 2$.

According to the Sect. 2.1.1 the source vertex has to be connected with itself. Both of Coates FG's, the initial and the modified one, are shown in Fig. 14a, b, respectively.

2.1.5 Norators Have a Common Node in the Equivalent Nullor Model

For this case has to be taken into account: i. a norator connected with the source node, considered in Sect. 2.1.3; ii. the pairs of the nodes connected with the norators must be written in *ascending order* in the income data.

Example 2.1.5 For this case an equivalent nullor model **N** of a converter of positive immitances is considered and shown in Fig. 15.

The initial form of the MCFG for the passive part of the network is shown in Fig. 16.

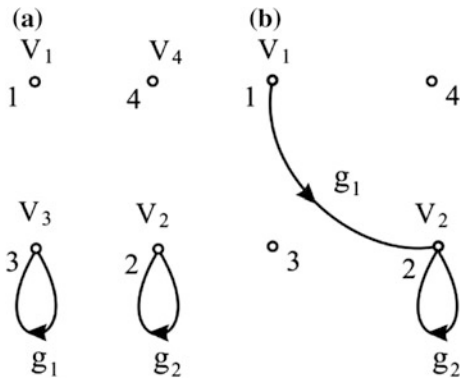


Fig. 14 Initial and modified Coates FG

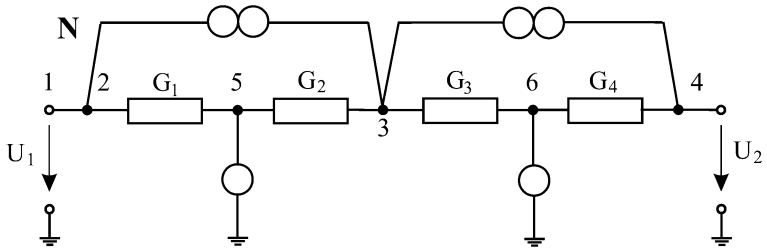
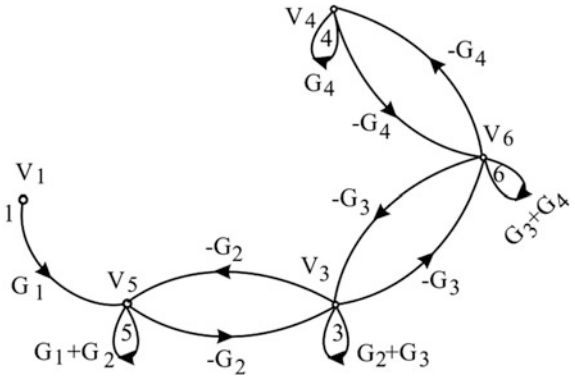


Fig. 15 Equivalent nullor model of a converter of positive immitances

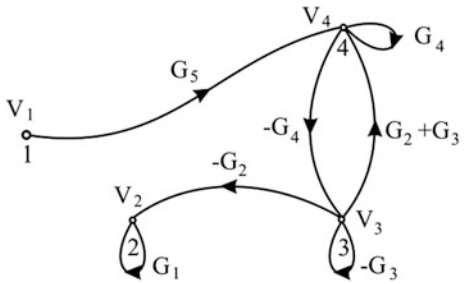
Fig. 16 Initial Coates FG



According to Sect. 2.1.3 for $t_{31} = 1$ and following the sequence of modification given in [22] chap. 5, we obtain MCFG in Fig. 17.

The *correctness* of the method considered is confirmed by *comparison of the symbolic results* for transfer function sensitivity analysis *obtained by the method described in* [20].

Fig. 17 Modified Coates FG



2.2 Determination of the Partial Transfer Functions and the First-, Second-Order and Multiparameter Symbolic Sensitivity by Nullor Model

Voltage transfer function $T_{ba}(s)$ is under consideration. Then normalized first- and second-order sensitivity, $S_{Y_1}^{T_{ba}}$ and $S_{Y_1Y_2}^{T_{ba}}$, of rational transfer function $T_{ba}(s)$ with respect to circuit parameters $Y_1(s)$ and $Y_2(s)$ are respectively [7, 8]:

$$S_{Y_1(S)}^{T_{ba}(S)} = \frac{Y_1(s)}{T_{ba}(s)} \frac{\partial T_{ba}(S)}{\partial Y_{ji}(S)} \frac{dY_{ji}(S)}{dY_1(S)} \tag{1}$$

$$S_{Y_1(S)Y_2(S)}^{T_{ba}(S)} = \frac{Y_1(s)Y_2(s)}{T_{ba}(s)} \frac{\partial^2 T_{ba}(S)}{\partial Y_1(S)\partial Y_2(S)}, \tag{2}$$

where

$$\frac{\partial^2 T_{ba}(S)}{\partial Y_1(S)\partial Y_2(S)} = \frac{\partial T_{ia}(S)}{\partial Y_{kl}(S)} \frac{dY_{kl}(S)}{dY_2(S)} T_{bj}(S) + \frac{\partial T_{bj}(S)}{\partial Y_{kl}(S)} \frac{dY_{kl}(S)}{dY_2(S)} T_{ia}(S), \tag{3}$$

$Y_{ji}(s) = a_{ji}(s) + Y_1(s)$ and $Y_{kl}(s) = a_{kl}(s) + Y_2(s)$ are edges of the MCFG and elements of reduced admittance matrix $\mathbf{Y}$(s); $a_{ji}(S)$ and $a_{kl}(S)$ contain other network parameters, for $a, i, l = 1, \ldots, m+n$; $b, j, k = m+1, \ldots, m+n$.

The MCFG allows us to simplify the sensitivity analysis on the base of certain network partial transfer functions. According to [7, 8] derivatives $\partial T_{ba}(S)/\partial Y_{ji}(S)$ in (1), $\partial T_{ia}(S)/\partial Y_{kl}(S)$ and $\partial T_{bj}(S)/\partial Y_{kl}(S)$ in (3) are as follow:

$$\begin{aligned} \partial T_{ba}(S)/\partial Y_{ji}(S) &= T_{ia}(S)T_{bj}(S) \\ \partial T_{ia}(S)/\partial Y_{kl}(S) &= T_{la}(S)T_{ik}(S) \\ \partial T_{bj}(S)/\partial Y_{kl}(S) &= T_{lj}(S)T_{bk}(S). \end{aligned} \tag{4}$$

When parameters $Y_1(S)$ and $Y_2(S)$ simultaneously participate in more then one edge in the modified Coates flow graph, respectively in the reduced admittance matrix $\mathbf{Y}$(s), the first- and second-order symbolic sensitivities are respectively:

$$S_{Y_1(S)}^{T_{ba}(S)} = \frac{Y_1(s)}{T_{ba}(s)} \sum_{ji} T_{ia}(S)T_{bj}(S) \frac{dY_{ji}(S)}{dY_1(S)} \tag{5}$$

$$S_{Y_1(S)Y_2(S)}^{T_{ba}(S)} = \frac{Y_1(s)Y_2(s)}{T_{ba}(s)} \left[\sum_{ji} T_{bj} \sum_{kl} T_{la}T_{ik} \frac{dY_{kl}(S)}{dY_2(S)} + \sum_{ji} T_{ia} \sum_{kl} T_{lj}T_{bk} \frac{dY_{kl}(S)}{dY_2(S)} \right] \tag{6}$$

or

$$S_{Y_1(S)}^{T_{ba}(S)} = \frac{Y_1(s)}{\Delta_{ba}\Delta} \sum_{j,i} \Delta_{ia}\Delta_{bj} \frac{dY_{ji}(S)}{dY_1(S)} \tag{7}$$

$$S_{Y_1(S)Y_2(S)}^{T_{ba}(S)} = \frac{Y_1(s)Y_2(s)}{\Delta_{ba}\Delta^2} \cdot \left[\sum_{ji} \Delta_{bj} \sum_{kl} \Delta_{la}\Delta_{ik} \frac{dY_{kl}(S)}{dY_2(S)} + \sum_{ji} \Delta_{ia} \sum_{kl} \Delta_{lj}\Delta_{bk} \frac{dY_{kl}(S)}{dY_2(S)} \right]. \tag{8}$$

Determinants Δ_{ba}, Δ_{ia}, Δ_{la}, and Δ_{bj}, Δ_{bk}, Δ_{ik}, Δ_{lj}, and Δ can be obtained by the modified Coates flow graph and its sub-graphs $\mathbf{G}_{kl}^{MC}$, $\mathbf{G}_{kj}^{MC}$ and $\mathbf{G}_{0}^{MC}$, respectively, as follows:

- $\mathbf{G}_{0}^{MC}$ is obtained by $\mathbf{G}^{MC}$ due to the removal of all outgoing edges from the vertex-source;
- $\mathbf{G}_{k1}^{MC}$, for $k = 2, \ldots, n$, is obtained from $\mathbf{G}^{MC}$ due to the removal of all outgoing edges, including the self-loop in the vertex k with a signal $V_k(S)$ and moving the vertex-source into the vertex k. As a result follows $Y_{jk} = 0$, $Y_{kk} = 0$ and the originals of the outgoing edges from the vertex-source are moved toward the vertex k;
- $\mathbf{G}_{kj}^{MC}$ is obtained from $\mathbf{G}_{0}^{MC}$ by removing all outgoing edges, including the self-loop, from the vertex k, as well as by removing all incoming edges, including the self-loop, from the vertex j and must be added an edge $Y_{jk} = -1$.

Consequently

$$\Delta_{kq} = \sum_{Q=1}^{R} (-1)^{N_Q} P_Q \tag{9}$$

where

N_Q—is the number of the loops in the Q-th separation of loops in the sub-graph;
R—the number of separations from loops in the sub-graph;

P_Q—the product of loop transmission coefficients in Q-th separation of loops in the sub-graph. Every separation of loops must be incident to all graph vertices and every one vertex must be incident with *only* one incoming edge and one outgoing edge.

The method suggested in this chapter performs multiparameter sensitivity analysis with respect to various circuit parameters too [31]. Suppose that p parameters exist having very small fractional perturbations from their nominal values. Magnitude of multiparameter symbolic sensitivity MS^T of transfer function $T_{ba}(S)$ is

$$MS^T = \sum_{i=1}^{p} \left| S^T_{Y_i(S)} \right| \tag{10}$$

The sequence of the main steps of the suggested method of first-, second-order and multiparameter symbolic sensitivity analysis is as follows:

1. Compose the equivalent nullor circuit of the active network.
2. Get the information about the network function required and the elements with respect to which the sensitivities are to be calculated. Determine the location of the nullators and norators [31].
3. Perform symbolic reduction of nullor circuit complexity (initial modified Coates flow graph) using the rules for transformation in order to reflect the nullor effect [22], chap. 5.
4. Calculate the partial transfer functions and the relevant determinants of the sub-graphs.
5. Calculate the first-order symbolic sensitivity of the transfer function by applying (7).
6. Calculate the second-order symbolic sensitivity of the transfer function by applying (8).
7. Calculate the multiparameter symbolic sensitivity of the transfer function by applying (10).
   The method suggested automatically performs the rules of modification, generates the symbolic admittance reduced matrix, determinants, partial transfer functions, first-, second-order and multiparameter symbolic sensitivity with respect to parameters in the circuit.

2.3 Examples

In this section, examples concerning the symbolic analysis of analog circuits are presented to show that the proposed symbolic method is applicable to first-, second order and multiparameter sensitivity analysis.

Example 2.3.1 A circuit example, taken from [9] is shown in Fig. 18 to illustrate the proposed method. The first- and second-order symbolic sensitivities of the transfer function $T(S) = U_3/U_1$ with respect to parameters G_4 and sC_2 are calculated. Multiparameter symbolic sensitivity $MS^{T_{31}}$ is obtained too. The equivalent nullor model $\boldsymbol{N}$ is composed and shown in Fig. 19.

An initial form of the MCFG for the passive part of the network is shown in Fig. 20a. The node corresponding to the vertex in the initial flow graph that is removed has number 5.

After applying the rules of modification, the modified Coates flow graph follows. It is represented in Fig. 20b.

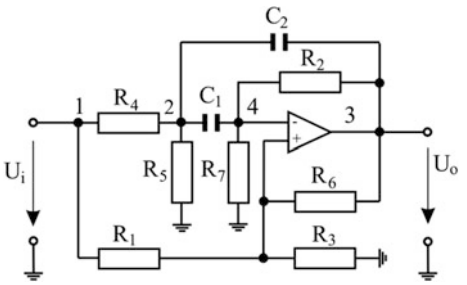


Fig. 18 The STAR network

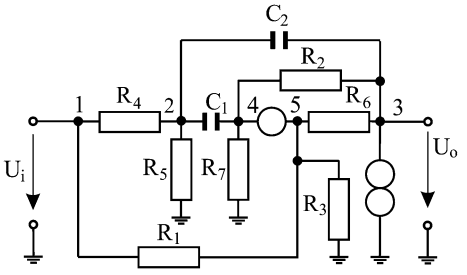


Fig. 19 The nullor model of the STAR network

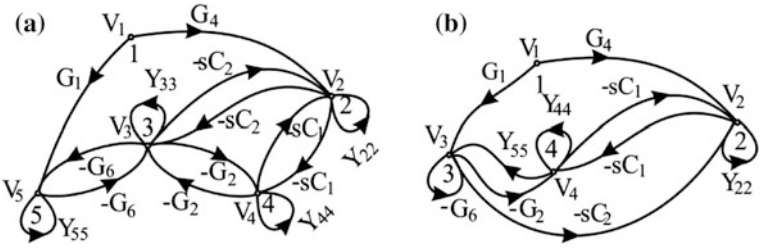
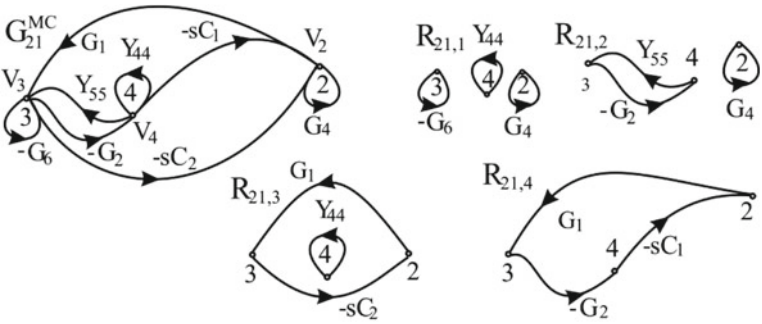


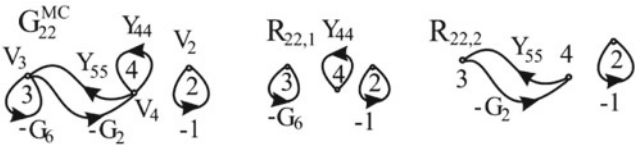
Fig. 20 Initial and modified Coates flow graphs

We suppose that voltage transfer function T_{31} is under consideration. When $Y_1(S) = G_4$ and $Y_2(S) = sC_2$ from the MCFG (Fig. 20b) follows: $Y_{21} = G_4$, $Y_{22} = G_4 + sC_2 + a_{22}$, $Y_{23} = -sC_2$, for $a_{22} = G_2 + sC_1$.

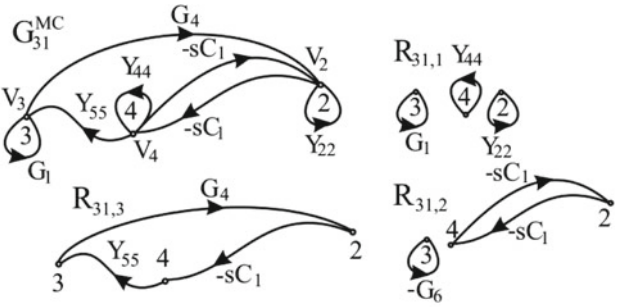
For determination of the first-order sensitivities four sub-graphs and their solutions are required: Δ_{21}, Δ_{31}, Δ_{32} are obtained using sub-graphs G_{21}^{MC}, G_{31}^{MC} and G_{32}^{MC}, respectively, shown in Fig. 21. The determinant Δ together with the possible combinations of loops (1F's) and their products are obtained using sub-graph G_0^{MC}, shown in Fig. 22.



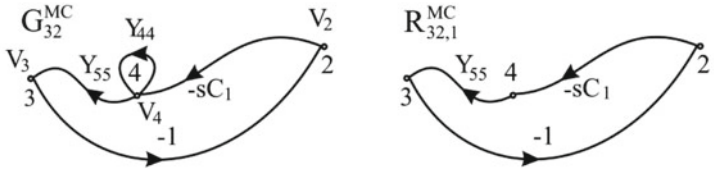
D21=Y44*(G4*G6-G1*sC2)-G2*G4*Y55-G2*G1*sC1,
where Y44=G2+G7+sC1; Y55=G1+G3+G6



D22=-Y44*G6+Y55*G2

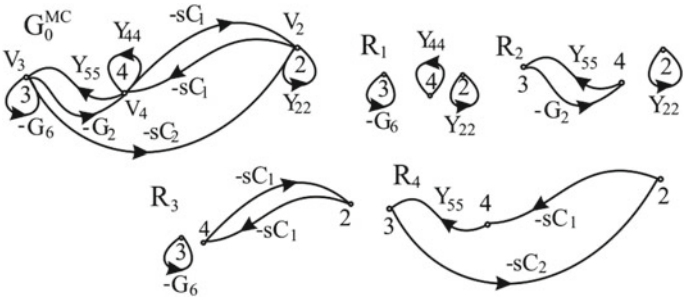


D31= -Y22*G1*Y44+sC1*sC1*G1+sC1*Y55*G4



D32=-sC1*Y55

Fig. 21 Sub-graphs G_{21}^{MC}, G_{22}^{MC}, G_{31}^{MC}, G_{32}^{MC} and their 1F's



D=Y22*G6*Y44-Y22*G2*Y55-sC1*sC1*G6-sC1*sC2*Y55

Fig. 22 Sub-graph $\mathbf{G}_0^{MC}$ and its 1F's

Taking into account (5) the first-order symbolic sensitivities $S_{G_4}^{T_{31}}$ and $S_{sC_2}^{T_{31}}$ are respectively:

$$\begin{aligned} S_{G_4}^{T_{31}} &= \frac{G_4}{T_{31}}\frac{\partial T_{31}}{\partial G_4} = \frac{G_4}{T_{31}}\left(\frac{\partial T_{31}}{\partial Y_{21}}\frac{dY_{21}}{dG_4} + \frac{\partial T_{31}}{\partial Y_{22}}\frac{dY_{22}}{dG_4}\right) \\ &= \frac{G_4}{T_{31}}(T_{11}T_{32} + T_{21}T_{32}) = \frac{G_4}{\Delta_{31}}\left(1 + \frac{\Delta_{21}}{\Delta}\right)\Delta_{32} \end{aligned} \tag{11}$$

$$\begin{aligned} S_{sC_2}^{T_{31}} &= \frac{sC_2}{T_{31}}\frac{\partial T_{31}}{\partial sC_2} = \frac{sC_2}{T_{31}}\left(\frac{\partial T_{31}}{\partial Y_{22}}\frac{dY_{22}}{dsC_2} + \frac{\partial T_{31}}{\partial Y_{23}}\frac{dY_{23}}{dsC_2}\right) \\ &= \frac{sC_2}{T_{31}}(T_{21}T_{32} - T_{31}T_{32}) = \frac{sC_2}{\Delta_{31}\Delta}(\Delta_{21} - \Delta_{31})\Delta_{32}. \end{aligned} \tag{12}$$

Taking into account (6) and (8) the second-order symbolic sensitivity $S_{G_4,sC_2}^{T_{31}}$ is respectively:

$$\begin{aligned} S_{G_4sC_2}^{T_{31}} &= \frac{G_4sC_2}{T_{31}} \\ &.[(T_{21}T_{22} - T_{31}T_{22})T_{32} + (T_{22}T_{32} - T_{32}T_{32})(T_{11} + T_{21})] \end{aligned} \tag{13}$$

$$\begin{aligned} S_{G_4sC_2}^{T_{31}} &= \frac{G_4sC_2}{\Delta_{31}\Delta} \\ &.\left[\frac{(\Delta_{21} - \Delta_{31})\Delta_{22}\Delta_{32}}{\Delta} + (\Delta_{22} - \Delta_{32})\Delta_{32}\left(1 + \frac{\Delta_{21}}{\Delta}\right)\right]. \end{aligned} \tag{14}$$

For determination of the second-order sensitivity is required only one sub-graph G_{22}^{MC} more, shown in Fig. 21.

According to (10) the method suggested calculates the magnitude of multiparameter sensitivity $MS^{T_{31}}$ of transfer function T_{31} with respect to all parameters:

$$MS^{T_{31}} = \sum_{i=1}^{7} \left| S_{G_i}^{T_{31}} \right| + \sum_{i=1}^{2} \left| S_{sC_i}^{T_{31}} \right| \tag{15}$$

where

$$\begin{aligned}
S_{G_1}^{T_{31}} &= \frac{G_1}{T_{31}} \frac{\partial T_{31}}{\partial G_1} = \frac{G_1}{\Delta_{31}} \left(1 + \frac{\Delta_{41}}{\Delta} \right) \Delta_{33} \\
S_{G_2}^{T_{31}} &= \frac{G_2}{T_{31}} \frac{\partial T_{31}}{\partial G_2} = \frac{G_1}{\Delta_{31}\Delta} (\Delta_{41} - \Delta_{31}) \Delta_{33} \\
S_{G_3}^{T_{31}} &= \frac{G_3}{T_{31}} \frac{\partial T_{31}}{\partial G_3} = \frac{G_3}{\Delta_{31}\Delta} \Delta_{41} \Delta_{33} \\
S_{G_6}^{T_{31}} &= \frac{G_6}{T_{31}} \frac{\partial T_{31}}{\partial G_6} = \frac{G_6}{\Delta_{31}\Delta} (\Delta_{41} - \Delta_{31}) \Delta_{33} \\
S_{G_7}^{T_{31}} &= \frac{G_7}{T_{31}} \frac{\partial T_{31}}{\partial G_7} = \frac{G_7}{\Delta_{31}\Delta} \Delta_{41} \Delta_{34} \\
S_{sC_1}^{T_{31}} &= \frac{sC_1}{T_{31}} \frac{\partial T_{31}}{\partial sC_1} = \frac{sC_1}{\Delta_{31}\Delta} (\Delta_{21} - \Delta_{41})(\Delta_{32} - \Delta_{34}).
\end{aligned} \tag{16}$$

For determination of multiparameter sensitivity are required seven sub-graphs (G_{21}^{MC}, G_{31}^{MC}, G_{41}^{MC}, G_{32}^{MC},G_{33}^{MC}, G_{34}^{MC} and $\mathbf{G}_0^{MC}$).

Example 2.3.2 Let us find the multiparameter sensitivity of the voltage transfer function $T_{51}(s) = U_o(s)/U_i(s) = U_5/U_1$ for the fourth-order low-pass filter, shown in Fig. 23a. Its equivalent nullor model is presented in Fig. 23b. The initial form of the MCFG is given in Fig. 24a. Considering the sequence of numbering [31], vertices (nodes) 8 and 9 in the initial flow graph (equivalent nullor model) are removed. These nodes are *strictly* determined in the input data. They correspond to the last ones in the sequence of numbering the nodes. According to rules 1, 3 and 5 of transformation of the initial flow graph described in [22], chap. 5, MCFG follows and it is shown in Fig. 24b.

Having in mind (10) $MS^T = \sum_{i=1}^{p} S_{Y_i(s)}^T$ the algebraic value of multiparameter symbolic sensitivity is

$$MS^{T_{51}} = S_g^{T_{51}} + S_G^{T_{51}} + \sum_{i=1}^{2} S_{G_i}^{T_{51}} + \sum_{i=1}^{2} S_{sC_i}^{T_{51}}, \tag{17}$$

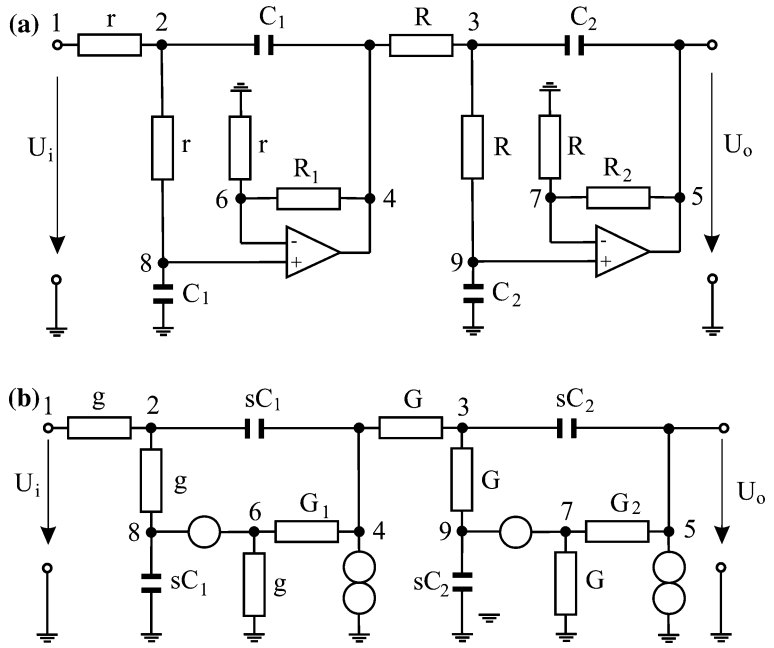


Fig. 23 Fourth-order low-pass filter (**a**) its equivalent nullor model (**b**)

where

$$
\begin{aligned}
S_g^{T_{51}} &= \frac{g}{T_{51}}\frac{\partial T_{51}}{\partial g} = \frac{g}{T_{51}}\left(T_{11}T_{52} + 2T_{21}T_{52} - T_{21}T_{54} - T_{61}T_{52} + T_{61}T_{54} + T_{61}T_{56}\right)\\
S_G^{T_{51}} &= \frac{G}{T_{51}}\frac{\partial T_{51}}{\partial G} = \frac{G}{T_{51}}\left(T_{31}T_{53} - T_{41}T_{53} - T_{71}T_{53} - T_{31}T_{55} + T_{71}T_{55} + T_{71}T_{57}\right)\\
S_{G_1}^{T_{51}} &= \frac{G_1}{T_{51}}\frac{\partial T_{51}}{\partial G_1} = \frac{G_1}{T_{51}}\left(-T_{41}T_{56} + T_{61}T_{56}\right)\\
S_{G_2}^{T_{51}} &= \frac{G_2}{T_{51}}\frac{\partial T_{51}}{\partial G_2} = \frac{G_2}{T_{51}}\left(-T_{51}T_{57} + T_{71}T_{57}\right)\\
S_{sC_1}^{T_{51}} &= \frac{sC_1}{T_{51}}\frac{\partial T_{51}}{\partial sC_1} = \frac{sC_1}{T_{51}}\left(T_{21}T_{52} + T_{41}T_{52} + T_{61}T_{54}\right)\\
S_{sC_2}^{T_{51}} &= \frac{sC_2}{T_{51}}\frac{\partial T_{51}}{\partial sC_2} = \frac{sC_2}{T_{51}}\left(T_{31}T_{53} + T_{51}T_{53} + T_{71}T_{55}\right)
\end{aligned}
\tag{18}
$$

Partial transfer functions T_{21}, T_{31}, T_{41}, T_{51}, T_{61}, T_{71}, T_{52}, T_{53}, T_{54}, T_{55}, T_{56}, T_{57} and determinants D21, D31, D41, DT51, D61, D71, D52, D53, D54, D55, D56, D57 are obtained using sub-graphs $\mathbf{G}_{21}^{MC}$, $\mathbf{G}_{31}^{MC}$, $\mathbf{G}_{41}^{MC}$, $\mathbf{G}_{51}^{MC}$, $\mathbf{G}_{61}^{MC}$, $\mathbf{G}_{71}^{MC}$, $\mathbf{G}_{52}^{MC}$, $\mathbf{G}_{53}^{MC}$, $\mathbf{G}_{54}^{MC}$, $\mathbf{G}_{55}^{MC}$, $\mathbf{G}_{56}^{MC}$, $\mathbf{G}_{57}^{MC}$ and $\mathbf{G}_{0}^{MC}$, respectively.

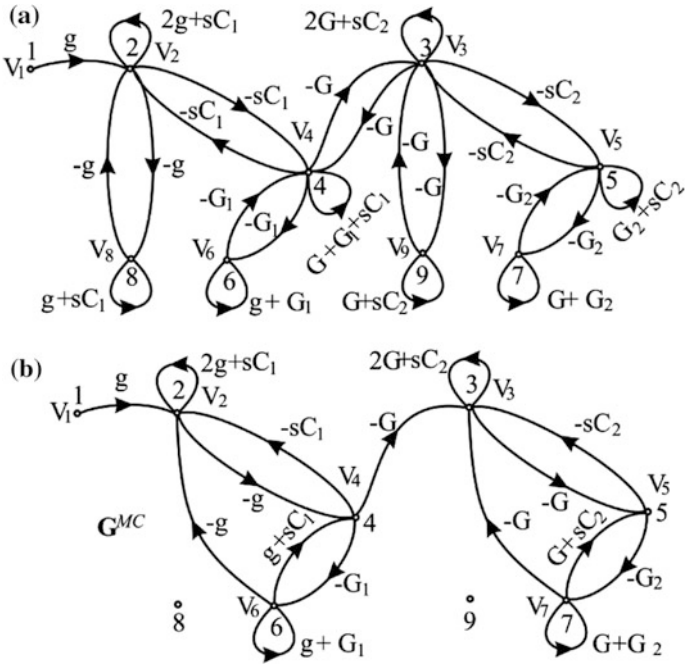


Fig. 24 Initial and modified Coates flow graphs

Determinant D together with the possible combinations of loops R_i, for $i = 1, \ldots, 9$ and their products (1F's) obtained using sub-graph $\mathbf{G}_0^{MC}$ are presented in [32]. The generated expressions can be easily transformed to the nested form (computer printout) and they are presented in Sect. 3. All partial transfer functions determined are: T21 = D21/D; T31 = D31/D; T41 = D41/D; T51 = D51/D; T61 = D61/D; T71 = D71/D; T52 = D52/D; T53 = D53/D; T54 = D54/D; T55 = D55/D; T56 = D56/D; T57 = D57/D.

Example 2.3.3 Let us find the multiparameter sensitivity of the voltage transfer function $T(s) = U_o(s)/U_i(s) = U_3/U_1$ for the second-order high-pass filter shown in Fig. 25a. The equivalent nullor model and its modified Coates flow graph are presented in Fig. 25b and c, respectively.

The reduction of the nullor model complexity is related with removing of two nodes ($R = 2$). The symbolic result for the algebraic value of the multiparameter symbolic sensitivity with respect to all parameters is

$$\begin{aligned} \mathrm{MS} \;=\; & (\mathrm{G2} * (\mathrm{G1} * \mathrm{G4} * (-\mathrm{sC2})) + \mathrm{G3} * (-(\mathrm{sC2} * \mathrm{G1} * (-\mathrm{sC2}))) + \\ & + \mathrm{G4} * (-(\mathrm{sC2} * \mathrm{G1} * (\mathrm{G2} + \mathrm{sC1}))) + \mathrm{sC1} * \mathrm{G1} * \mathrm{G4} * (-\mathrm{sC2}) \\ & + \mathrm{sC2} * \mathrm{G1} * \mathrm{G4} * (\mathrm{G2} + \mathrm{sC1}))/(\mathrm{sC2} * \mathrm{G1} * ((\mathrm{G2} + \mathrm{sC1}) * \mathrm{G4} - \mathrm{sC2} * \mathrm{G3})) - 1 \end{aligned} \tag{19}$$

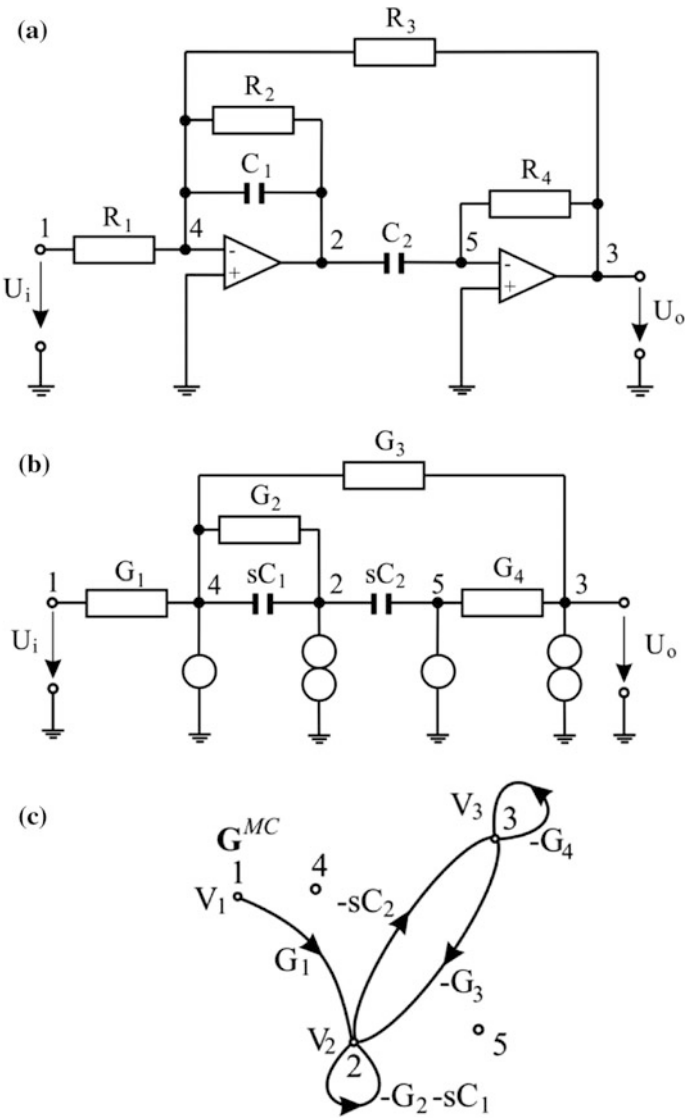


Fig. 25 **a** Second-order high-pass filter; **b** its equivalent nullor model; **c** modified Coates flow graph

The magnitude of the multiparameter sensitivities MS_k of the transfer function with respect to all parameters for $f = 1000$ Hz is obtained by the expression

$$MS_k = \sum_{i=1}^{6} \sqrt{\left[\mathrm{Re}(S_i)_k\right]^2 + \left[\mathrm{Im}(S_i)_k\right]^2}, \tag{20}$$

where S_i is the sensitivity with respect to parameter i.

3 SANMCFG Method Versus TI

In symbolic sensitivity analysis very important role plays the number of additionally generated expressions and in consequence additional number of arithmetical operations. Simplifications of the modified Coates flow graph introduced in this chapter lead to the significant reduction of the final symbolic expressions without violation of accuracy because of that this contribution is very important. This simplification method can be considered as SBG–type (Simplification Before Generation) and has significant impact on symbolic sensitivity analysis. Such simplification method is not known in literature devoted to symbolic sensitivity analysis [2, 11, 13]. In this section we compare the number of arithmetical operations and the circuit insight of the method presented with the two-port transimpedance method, which has been already related to other symbolic sensitivity analysis methods [2].

3.1 Comparison of Arithmetical Operations

In this section we will compare the number of arithmetical operations of the nulor model and modified Coates flow graph method (SANMCFG) with the number of arithmetical operations of the two-port transimpedance method while calculating the multiparameter sensitivity. We will take the following assumptions: each long arithmetical operation such as multiplication and division denoted as M/D (or Mults) corresponds to 6 flops and each short arithmetical operation such as addition and subtraction denoted as A/S (or Adds) corresponds to 2 flops. Let the sum of all flops will be the arithmetical effectiveness measure. Basing on this measure we will compare our method denoted as SANMCFG with the transimpedance method denoted as TI. The comparison tests were performed for:

- fourth-order LP filter circuit presented in this chapter as Example 2.3.2 and shown in Fig. 23a;
- second-order HP filter, presented in Fig. 25.

The manner, in which the number of flops was calculated, is shown in the listing below. This listing concerns the fourth-order LP filter (computer printout):

MS = ((**S1** + **S2** + **S3** + **S4** + **S5** + **S6**)/(**D**))/(**D51**); % Mults:2, Adds:5, Flops:22,

where:

D51 = (G^2)*(g^2)*(Y66)*(Y77); %Mults: 5, Flops: 30

D = (((((((((Y22)*(Y33)*G1*(Y46)*G2*(Y57))-((Y22)*G*sC2*G1*(Y46)*(Y77)))-((Y22)*G2*(G^2)*G1*(Y46)))- (g*sC1*(Y33)*G2*(Y57)*(Y66))) +(g*sC1*G*sC2*(Y66)*(Y77))) + (g*sC1*G2*(G^2)*(Y66)))-(G1*(g^2)*(Y33)*G2*(Y57))) + (G1*(g^2)*G*sC2*(Y77))) + G1*(g^2)*G2*(G^2);%Mults: 45, Adds: 8, Flops: 286

s = j*2*π*f; % *f* – frequency, Mults: 2, Flops: 12

sC1 = s*C1; sC2 = s*C2; % Mults: 2, Flops: 12

Y22 = 2 g + sC1; Y33 = 2G + sC2; Y46 = g+sC1; Y57 = G+sC2; Y77 = G +G2; Y66 = g+G1; % Adds: 6, Flops: 12

% Total SM Mults: 56, Adds: 19, Flops: 374

S1 = (g) * (D*D52 + (2*D21-D61)*D52 + (- D21 + D61)*D54 + D61*D56); % Mults:6, Adds:5, Flops: 46, % Total S1 Mults: 97, Adds: 18, Flops: 618

S2 = …; Flops: 494, **S3** = …; Flops: 252, **S4** = …; Flops: 228, **S5** = …; Flops: 352, **S6** = …; Flops: 264,

Table 1 Comparison of TI and SANMCFG arithmetical operation measures in case of fourth-order LP filter

Sens. function	Symbolic analysis	M/D		A/S		Flops	
$S_g^{T_{51}}$	SANMCFG(S1)	97		18		618	
	TI		88		54		636
$S_G^{T_{51}}$	SANMCFG(S2)	77		16		494	
	TI		91		51		648
$S_{G_1}^{T_{51}}$	SANMCFG(S3)	40		6		252	
	TI		38		19		266
$S_{G_2}^{T_{41}}$	SANMCFG(S4)	36		6		228	
	TI		26		15		186
$S_{C_1}^{T_{41}}$	SANMCFG(S5)	56		8		352	
	TI		61		36		438
$S_{C_2}^{T_{41}}$	SANMCFG(S6)	42		6		264	
	TI		58		34		416
SM	SANMCFG	56		19		374	
	TI		0		0		0
	Total:	**404**	**362**	**79**	**209**	**2582**	**2590**

MS = ((**S1** + **S2** + **S3** + **S4** + **S5** + **S6**)/(**D**))/(**D51**); % Mults:2, Adds:5, Flops:22

% Total **MS** Mults: 404, Adds: 79, Flops: 2582

Expressions for S*i* are given in [32].

The results of calculations are collected in Table 1 and compared with those obtained by using the transimpedance method.

Similar calculations were made for the second-order HP filter, for which we obtained the following number of total flops: for SANMCFG 190 and for TI 456.

We see, that in regard to arithmetical operations measure, the SANMCFG method is superior to TI method in case of smaller circuits and comparable to TI method in case of bigger circuits (see Table 1). For LP fourth-order filter the SANMCFG method needs 2582 flops while TI method needs 2590 flops. On the other hand, for HP second-order circuit the SANMCFG method needs 190 flops while TI method needs 456 flops.

Symbolic methods generate symbolic expressions in different forms, which need different number of arithmetical operations. This measure strongly depends on the form of representation of multiparameter sensitivity function. In the above comparisons, the performance measures were calculated as a sum of partial measures of partial relative sensitivities, because the multiparameter sensitivity represents such sum. For the fourth-order LP filter, the generated expressions can be easily transformed to the nested form, shown below (computer printout):

```
s = j*2*_*f; % f – frequency, % Mults: 2, Flops: 12
sC1 = s*C1; sC2 = s*C2; % Mults: 2, Flops: 12
Y22 = 2 g + sC1; Y33 = 2G + sC2; Y46 = g + sC1; Y57 = G + sC2; Y77 = G + G2;
Y66 = g + G1; % Adds: 6, Flops: 12
D21 = ((g*(Y33)*G1*(Y46)*G2*(Y57))-(g*G*sC2*G1*(Y46)*(Y77)))−
      (g*G2*(G^2)*G1*(Y46)); % Mults:15, Adds:2, Flops:94
D31 = …; % Flops:30, D41 = …; % Flops:94, D51 = …; Flops:30,
D52 = …; % Flops: 24, D53 = …; % Flops: 76, D54 = …; Flops: 24,
D55 = …; % Flops:76, D56 = …; % Flops: 50, D57 = …; Flops: 154
D61 = …; % Flops: 94, D71 = …; %, Flops: 30
D = …; % Mults: 45, Adds: 8, Flops: 286
MS = ((g*(D * D52 + (2 * D21−D61)*D52 + (−D21 + D61)*D54 + D61 * D56)+
G * ((D31−D41−D71)*D53 + (−D31 + D71)*D55 + D71*D57)+
G1 * ((−D41 + D61)*D56) + G2 * ((−D51 + D71)*D57) + sC1 *
((D21 + D41)*D52 + D61*D54) + sC2 * ((D31 + D51)*D53 +
D71*D55))/(D))/(D51); % Mults: 22, Adds: 21, Flops: 174
% Total Flops: 1272 (Expressions for Di are given in [32]).
```

It should be noticed that if the multiparameter sensitivity is recorded in nested form, shown above, it needs 1272 flops, only! In this representation, the SANMCFG method becomes superior to the TI standard method (without simplifications). The sequence of expressions shown above can be directly calculated in Matlab environment.

3.2 Comparison of Circuit Insights

Let us look at the Example 2.3.3 (HP second—order filter) more precisely. The SANMCFG method generates the following expression of the sensitivity function $S_{G_2}^{T_{31}}$:

$$S_{G_2}^{T_{31}} = (\mathrm{G2}/(\mathrm{sC2} * \mathrm{G1} * (((\mathrm{G2} + \mathrm{sC1}) * \mathrm{G4}) - \mathrm{sC2} * \mathrm{G3}))) * (-(-(\mathrm{G1} * \mathrm{G4}) * -(\mathrm{sC2}))) \tag{21}$$

After small rearrangement we get more familiar forms

$$S_{G_2}^{T_{31}} = \frac{-G_2G_4}{(G_2 + sC_1)G_4 - sC_2G_3} = -\frac{G_2G_4}{G_2G_4 + s(G_4C_1 - G_3C_2)} \tag{22}$$

If we accept the appropriate time constants equal: $R_3C_1 = R_4C_2$, then this sensitivity will not be depended on frequency and will be equal to -1.

On the other hand, TI method generates the following SoE (computer printout).

$$\begin{aligned}
\mathrm{Z21} &= \mathrm{G1*s*C2} \\
\mathrm{Zoi} &= \mathrm{Z21} \\
\mathrm{Z11} &= -(\mathrm{G3*s*C2 - G4*(G2 + s*C1)}) \\
\mathrm{Zii} &= \mathrm{Z11} \\
\mathrm{Z24} &= \mathrm{G1*s*C2} \\
\mathrm{Zok} &= -\mathrm{Z24} \\
\mathrm{Z31} &= -\mathrm{G1*G4} \\
\mathrm{Zki} &= \mathrm{Z31} \\
\mathrm{D00} &= \mathrm{G1*Z11} \\
\mathrm{STvG2} &= -\mathrm{G2*Zki*Zok/(Zoi*D00)}
\end{aligned} \tag{23}$$

Basing on this SoE, it is not possibly to predict the result obtained above, easily.

Let us consider the sensitivity measure $\left|\sum_j S_{G_j}^{T_{31}}\right| = |MS|$, $j = 1,2,\ldots,6$,

where MS is determined by (19).

After canceling common factors sC2*G1 in nominator and denominator in (19) and after small rearrangement we get more familiar form:

$$\begin{aligned}
|MS| &= \left|\frac{-G_2G_4 + sC_2G_3 - G_4(G_2 + sC_1) - sC_1G_4 + G_4(G_2 + sC_1)}{(G_2 + sC_1)G_4 - sC_2G_3} - 1\right| = \\
&= \left|\frac{-G_2G_4 + sC_2G_3 - G_4(G_2 + sC_1) - sC_1G_4 + sC_2G_3}{(G_2 + sC_1)G_4 - sC_2G_3}\right|
\end{aligned} \tag{24}$$

It is not difficult to recognize that nominator is two times greater than denominator. In this way we obtain very important property of this circuit—its multiparameter sensitivity measure is independent on frequency and is equal to 2: MS = 2. On the other hand, basing on series of SoE generated by TI method, it is almost impossible to anticipate such important property of this circuit.

Resuming, it can be stated, that:

- in respect to arithmetical operation measure, the presented method is comparable to the TI method and even superior after transformation the generated expressions into nested form;
- Moreover, the SANMCFG method gives much better circuit insight than TI method.

4 Conclusion

The method of nullor model and modified Coates flow graph for symbolic sensitivity determination automatically can generate symbolic admittance reduced matrix, determinants, partial transfer functions, symbolic first-, second-order and multiparameter sensitivities.

It is based on the equivalent nullor model of active devices and modified Coates flow graph. The method suggested in this chapter performs symbolic first-, second-order and multiparameter sensitivities analysis with respect to various circuit parameters to tune circuit parameters during sizing. "HoneySen" software implements the sequence of actions according to the presented method. To verify its applicability several examples are examined, some of them are: with a fourth order low pass filter and with a second-order high-pass filter.

A method of symbolic sensitivity determination is used for special cases of symbolic sensitivity analysis using nullors. It is based on some transformations of the modified Coates flow graph of the nullor model of the passive part in order to reflect the nullator-norator pairs' influence on the network transfer functions.

Advantages of the suggested method are that it is not necessary to multiply analyze the corresponding graph and the modified node admittance matrix inversion is not required. The carried out comparison tests showed the presented method to be comparable to the transimpedance method (and to other this kind of methods) in respect to arithmetical operation measure. After transformation the generated expressions into nested form, the proposed method becomes even more effective for middle-size circuits. Moreover, our investigations showed the presented method to be superior to the transimpedance method under the account for the circuit insight.

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Synthesis of Electronic Circuits Structures on the Basis of *Active Switches*

Marian Pierzchala and Mourad Fakhfakh

Abstract A novel idea for synthesis of electronic circuits' structures is presented. It is based on the use of '*active switches*' which can be considered as circuit implementation of the pathological elements since they connect and/or disconnect different elements in the circuits and thus impose on their terminals specific voltages and currents in a similar way as nullors and mirrors. Furthermore, the proposed technique consists of using a combinatorial approach; this allows not only demystifying the process of finding new circuits structures, but also opens large research areas for proposing new ones, as it will be shown in the chapter.

Keywords Synthesis of circuits structures · Pathological elements
Active switches · Signal-flow graph · Combinatorial approaches

1 Introduction

During the past six decades, researchers were looking for new analog circuit structures overcoming the limitations of conventional elements and allowing the design of complex circuits in different manners, thus performing different performances in terms of accuracy, sensitivity, speed, power consumption, circuit complexity, etc. [1, 2]. Such circuits are usually designed by skilled analog designers using largely intuitive design approaches. However, intuitive design methods have the following disadvantages.

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1. Known circuit topologies are favored, although there may exist alternative topologies that are more suitable. Innovations in circuit topology largely depend on deep insights of the designers.
2. It takes a long time for a designer to become experienced, thus such approaches are specific to skilled.
3. The intuitive approach is not very suitable for implementation in a CAD system.

These observations argue the need for the proposal of design methodologies that explore the design space in a more systematic way [3]. A natural way to explore a specific design space systematically is using graph theory. Of course, rules for selecting the useful solutions are needed here.

Systematic generation of all elementary transconductance-based circuits by using linear graphs has already been considered by a plethora of published works; see for instance [3–5]. In [5], a restriction has been implemented that consists of generating only circuits with at least one non-zero transmission parameter.

The combinatorial approach we propose in this work is similar to the one in [5] but instead of linear graphs we use a primitive signal-flow graph [6]. Further, one-port elements (resistors, capacitors) are used instead of transconductors. As a criterion of usefulness the same rule as in [5] will be used, i.e. the generated circuits should have at least one non-zero transmission parameter.

Our design technique allows generating, not only the already known circuits, but also proposing new ones. Moreover, it allows explaining how such building blocks can be built from scratch. It is to be stressed that the use of the known pathological elements is a particular case of the proposed approach, as it will be detailed below.

In addition, our approach consists of using '*active switches*' [7, 8] to generate different possible combinations of connecting one (or more) one-port(s) between the input and the output of a two-port circuit. Thus, *Kirchhoff* voltage laws (KVL) and *Kirchhoff* current (KCL) laws are fulfilled in a particular way, leading to the construction of different loop and cutset matrices, and as a consequence, it allows generating 'new' circuits. Primitive signal-flow graph is also used to screen the generated circuits.

The rest of the chapter is structured in three main sections. In the first one, i.e. Sect. 2, we present the use of primitive flow-graphs as a base of a combinatorial approach for searching new analog two-ports. In Sect. 3, we give details of switching one, two and three one-port elements via the use of the '*active switches*', for generating the active blocks. Then, in Sect. 4, we deal with some practical implementations of the proposed method.

2 Primitive Signal-Flow Graphs as a Base of a Combinatorial Approach for Constructing Analog Building Blocks

Consider the simpler case of a network consisting of immittance (impedance or admittance) elements and independent sources only. We assume that the independent voltage sources contain no loops, and the independent current sources contain no cutsets [9]. Then, it is always possible to select a tree T such that all voltage sources are tree branches and all current sources are links (cotree branches). Therefore a unique primitive signal-flow graph can be constructed [9] in which the three basic laws: *Kirchhoff* Voltage Law (KVL), *Kirchhoff* Current Law (KCL) and *Ohm* Law (OhmL) are clearly displayed. Figure 1 shows the general layout of a primitive signal-flow graph.

In Fig. 1 we adopt the following labels:
E–independent voltage sources,
I–independent current sources,
$\mathbf{Z_Z}$–impedance branches in the tree,
$\mathbf{Y_Y}$–admittance branches in the cotree (links)
$\mathbf{B_{YE}}$–loop submatrix between elements in E and Y_Y,
$\mathbf{B_{YZ}}$–loop submatrix between elements in Y_Y and Z_Z,
$\mathbf{Q_{ZI}}$–cutset submatrix between elements in I and Z_Z,
$\mathbf{Q_{ZY}}$–cutset submatrix between elements Z_Z and Y_Y.
For the passive networks (R, L, C) with independent sources we can write [9]

$$\boldsymbol{Q_{ZY}} = -\boldsymbol{B_{YZ}^t} \tag{1}$$

but for the active networks, we have:

$$\boldsymbol{Q_{ZY}} \neq -\boldsymbol{B_{YZ}^t} \tag{2}$$

Inequality (2) shows that it is possible to generate many active circuits in a systematic way. We should only propose a method which enables constructing the structures which fulfil the above inequalities. In this paper, we propose such a method that is based on using the *active switches* [7, 8], which enables connecting a number of passive elements in two different configurations. In the first configuration we will calculate the KVL to obtain the submatrix $\boldsymbol{B_{YZ}}$ and in the second configuration we

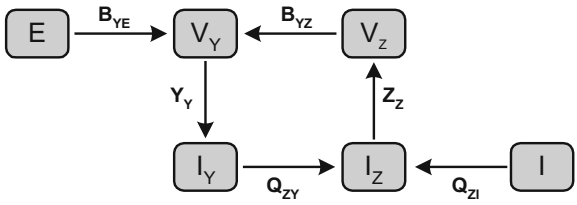


Fig. 1 General layout of a primitive signal-flow graph

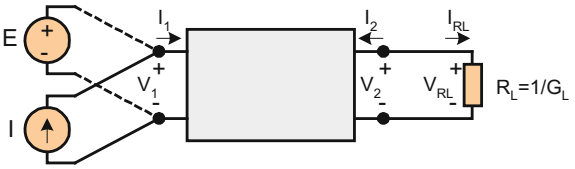


Fig. 2 The transmission parameters

$K_u=V_{RL}/E;\ K_i=I_{RL}/I;\ R_T=V_{RL}/I;\ G_T=I_{RL}/E$

will calculate KCL to obtain submatrix $\boldsymbol{Q_{ZY}}$. Due to the fact that these two configurations are different, inequality (2) is fulfilled. In the next step, we have to check up if such circuit has a practical meaning. As a criterion of 'the usefulness', we will only consider generated circuits having at least one non-zero transmission parameter, where transmission parameters are defined as shown in Fig. 2.

The transmission parameters can be calculated using any method. We use signal-flow graphs (SFG) and the *Mason*'s formula [6, 9] due to their 'visual' properties.

3 Searching for New Circuits Structures by a Combinatorial Approach

3.1 Circuits Structures with One Resistor

First, we consider one port resistor which can be characterized by three quantities, see Fig. 3:

- The nominal value of the resistance R,
- The voltage across its terminals $V_{k,l}$,
- The current flowing through that element I_{kl},

It is possible to imagine that using the *active switches* [7, 8] we can construct a two-port circuit, as shown in Fig. 4, in which the resistor will be connected optionally to the input or to the output of the circuit depending on the considered basic law, i.e. *Kirchhoff* voltage law or *Kirchhoff* current law, so inequality (2) is fulfilled.

In the considered situation we have the next possibilities:

- For the calculation of the loop submatrix $\mathbf{B_{YZ}}$, resistor R is connected to the input of the two-port circuit, and for the calculation of cutset submatrix $\mathbf{Q_{ZY}}$, resistor R is connected to the output (Actually, we have four such possibilities, as shown in Fig. 5).

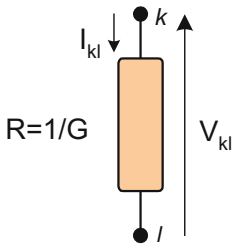


Fig. 3 The resistor

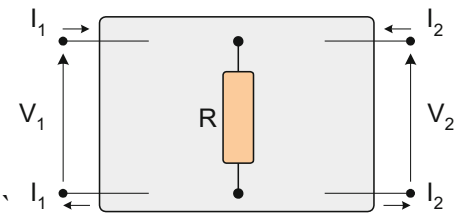


Fig. 4 A two port circuit

- For the calculation of the loop submatrix $\mathbf{B_{YZ}}$, resistor R is connected to the circuit's output, and for the calculation of the cutset submatrix $\mathbf{Q_{ZY}}$, the resistor is connected to the input (Similarly, we have four such possibilities but we show only one, see Fig. 6).

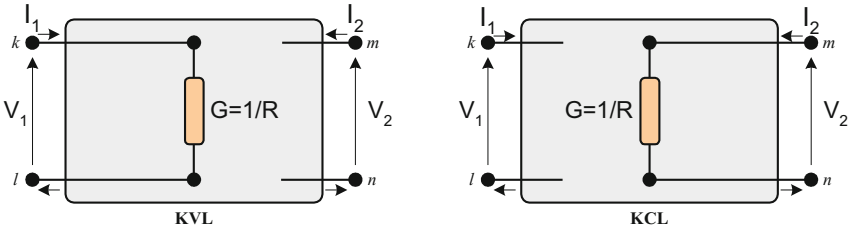
If we would like to check up on the usefulness of such circuits, we should calculate their parameters. This can be done by any chosen method. Here, we use signal flow-graphs (SFG) [6, 9] due to their *visual* properties, as mentioned above.

We check now the properties of two-ports circuits with the first combination of the resistors shown in the Fig. 5. We will calculate the transmission parameters using an independent voltage source on the input and a short circuit ($R_L = 0$) on the output (see Fig. 2). The corresponding signal flow-graphs are shown in Fig. 7.

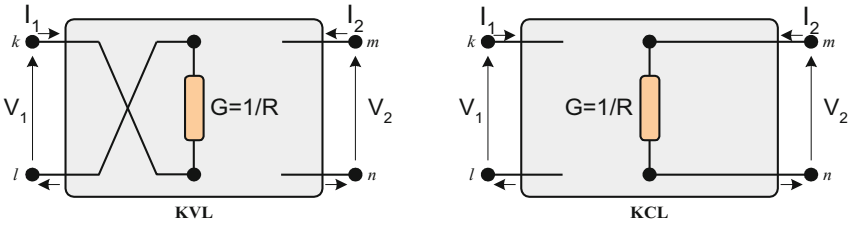
From these SFGs we can see that the corresponding resistor connections can be considered as a V to I converter: $I_{RL} = \pm G\ E$.

Consider now the circuit with the second combination of the resistor connection shown in Fig. 6. We will calculate the transmission parameter using an independent current source on the input and an open-circuit ($G_L = 0$) at the output (see Fig. 2). The signal-flow graph of this circuit is depicted in Fig. 8.

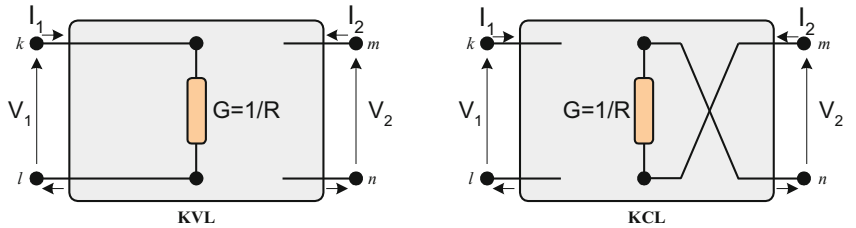
Similarly, as for the SFGs of Fig. 7, we can see that this resistor connection realizes the I to V conversion: $V_{GL} = R\ I$. Of course, we can put into use the crossover connections, thus enlarging the number of possible solutions.



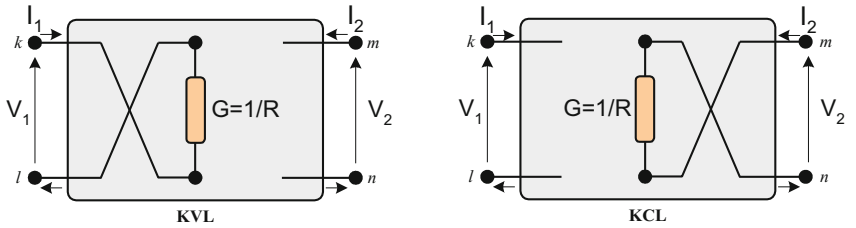
(a) The direct connection of the resistor R to the input and to the output.



(b) The crossover connection of the resistor R to the input and direct to the output



(c) The direct connection of the resistor R to the input and crossover the output.



(d) The crossover connection of the resistor R to the input and to the output.

Fig. 5 The first combination of the resistor connections. **a** The direct connection of the resistor R to the input and to the output. **b** The crossover connection of the resistor R to the input and direct to the output. **c** The direct connection of the resistor R to the input and crossover the output. **d** The crossover connection of the resistor R to the input and to the output

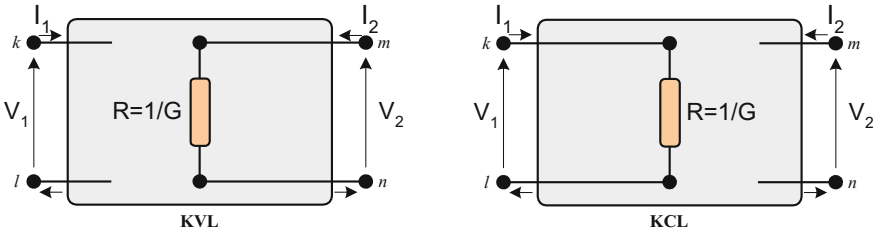


Fig. 6 The second combination of the resistor connections (we show only one among the four possibilities)

3.2 Circuits Structures with Two Resistors

If we consider the possible connections of two resistors with different nominal values (R_1 and R_2) with the help of the active switches [7, 8], than we can construct the two port circuits shown in Fig. 9 in which the resistors will be connected optionally in series or in parallel to the input or to the output of the circuit depending on the considered basic law, i.e. KVL or KCL. Accordingly, we have the following possibilities (among many others):

Now, we can check up the usefulness of the above circuits.

The circuit shown in Fig. 9a does not have any interesting properties because it presents two separate circuits, see SFG depicted in Fig. 10 (this SFG presents a circuit with the independent voltage source on the input and a short-circuit ($R_L = 0$) at the output).

However, the remaining configurations are very interesting. For example, the circuit shown in Fig. 9b can be considered as a two-port with transmissions both from the input to the output and from the output to the input. If we connect the independent current source to the input (output) and the open-circuit to the output (input) then this two-port can be consider as the current controlled voltage source (CCVS) with the coefficient of the transmission equal to R_2, from the output to the input and the CCVS with the transmission coefficient equal to R_1 from the input to the output, see SFG in Figs. 11a and b.

There exists in these combination admittedly parasitic interaction of the output current (I_{GL}) on the voltage (V_1) of the independent current source I, but it can be omitted, because $G_L = 0$. It can be also omitted, if the value of resistor $R_1(R_2)$ is very small (with a boundary value approaching to zero).

If both resistors take the boundary values, i.e. $R_1 \to 0$, $R_2 \to \infty$, the combination from Fig. 9b may be consider as four terminal nullor [10]. This is evident from Fig. 9b because for the process of the calculations of the KVL we have at the input a short-circuit and at the output an open-circuit. And vice versa, for the process of the calculations of the KCL we have at the input an open-circuit, and at the output a short-circuit.

There is also another application of this configuration. If we use the crossover connection between resistor R_1 and the input in the circuit for the calculation of the

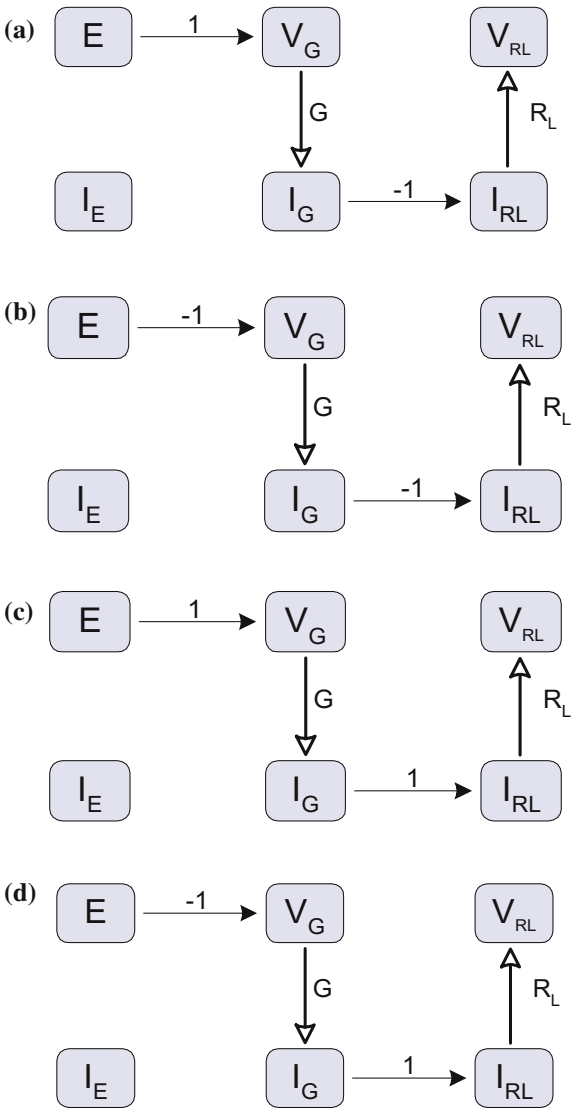


Fig. 7 SFGs of the circuits with the first combination of the resistor connections

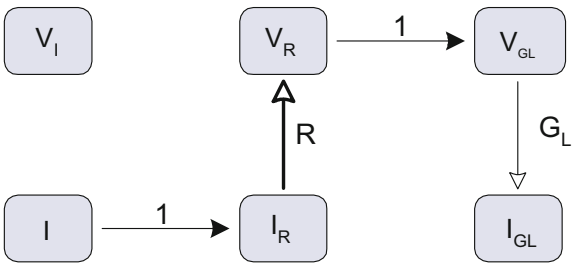


Fig. 8 SFG of the circuit with the second combination of the resistor connections

KVL, then this circuit (Fig. 12) will work as a *gyrator* [11] in the impedance form with different transmission coefficients R_1, R_2 (see Fig. 13).

In turn, the configuration from Fig. 9c can work as a voltage controlled voltage source (VCVS), (see the corresponding SFG in Fig. 14) with the transmission coefficient $\mu = -G_1R_2$.

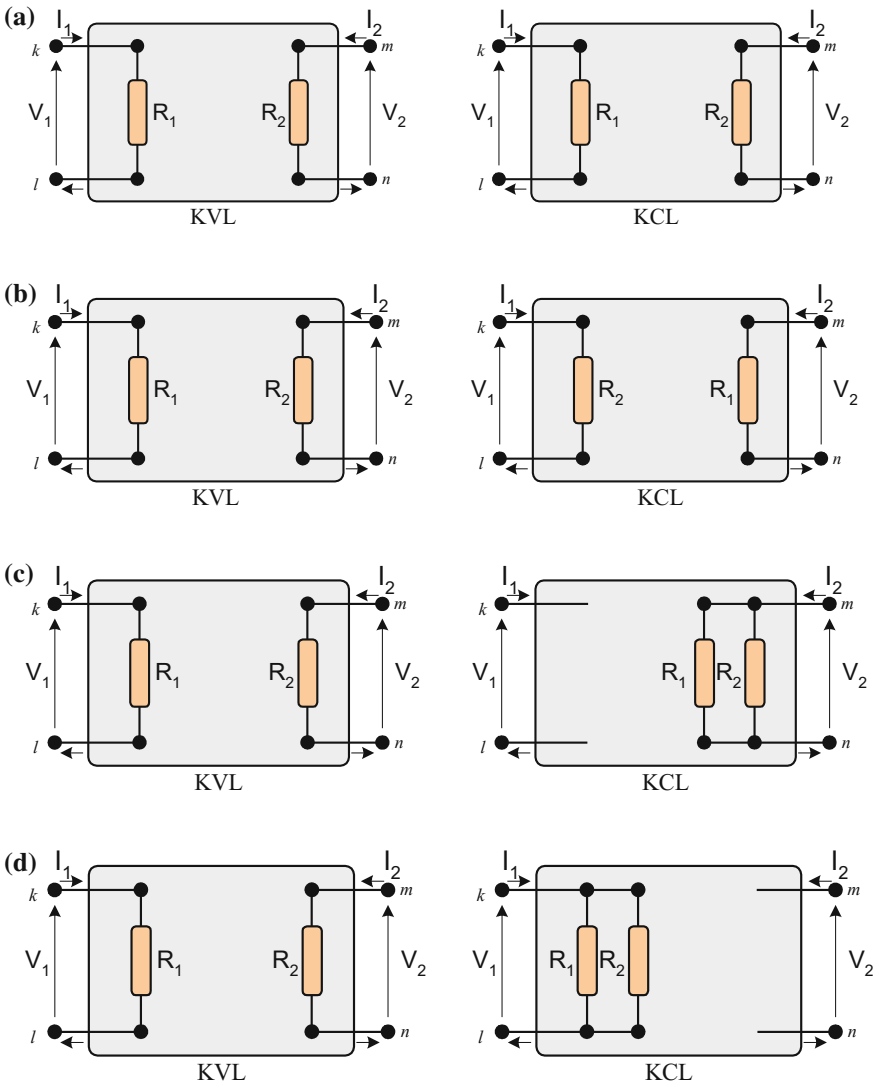


Fig. 9 The case of two resistors: few connection possibilities

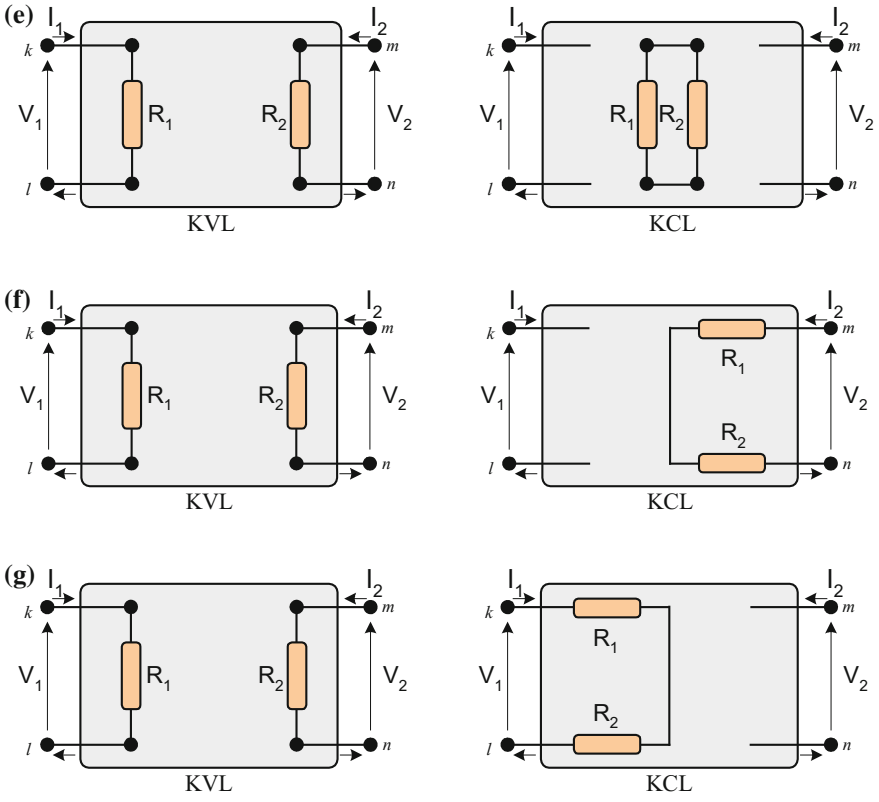


Fig. 9 (continued)

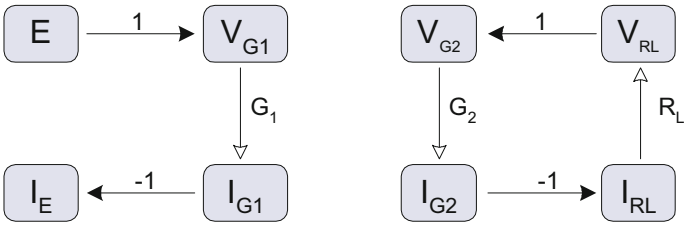


Fig. 10 SFG of the circuit of Fig. 9a

However, this circuit is not an ideal VCVS because it has an output resistance that is equal to R_2.

The circuit given in Fig. 9d can work as a VCVS that transmits the signal from the output to the input with the transmission coefficient $\mu = -R_1 G_2$ and the inner resistance $R_{in} = R_1$, see SFG given in Fig. 15.

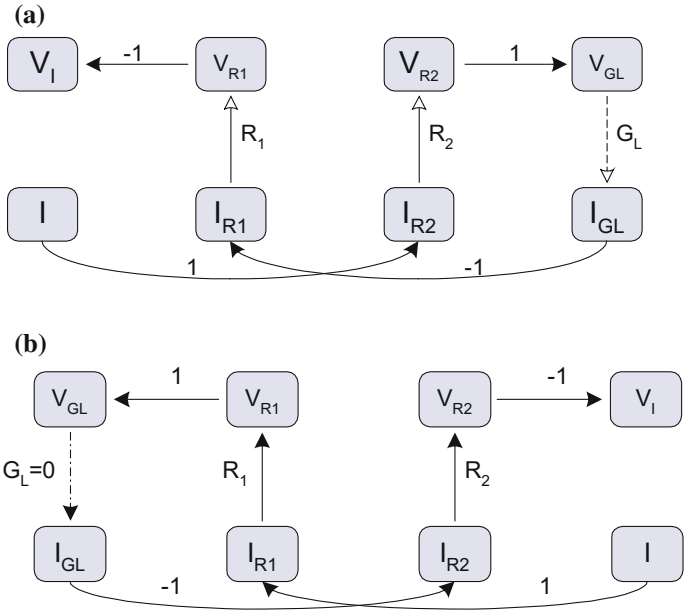


Fig. 11 **a** SFG of the circuit shown in Fig. 9b with the independent current source on the input and the open-circuit on the output. **b** SFG of the circuit shown in Fig. 9b with the independent current source on the output and the open-circuit on the input

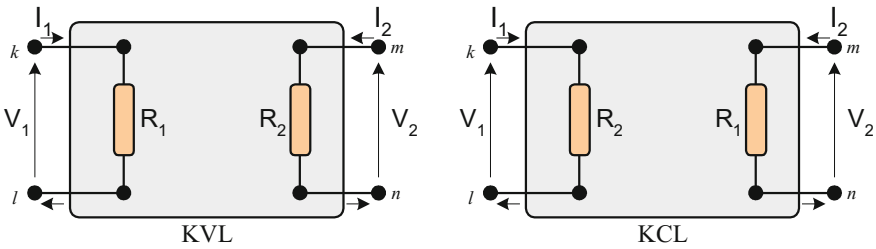


Fig. 12 The combination of the two resistors which works as gyrator

The next configuration (shown in Fig. 9e) can work as a voltage controlled voltage source (VCVS) with the transmission coefficient $\mu = -G_1R_2$ and both the input and the output resistances values are equal to infinity (see Fig. 16).

This configuration is very interesting. If we choose the same value for both resistors (i.e. $R_1 = R_2$), then this circuit will work as an inverting voltage follower with input and output resistances equal to infinity. Moreover, if we use the cross-over connection between resistors R_2 and R_1 (in the circuit for KCL calculation) and take equal values of resistors ($R_1 = R_2 = R$), then this circuit will work as a voltage mirror.

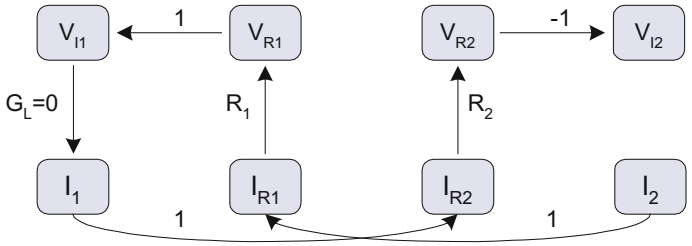


Fig. 13 The SFG of the circuit from Fig. 12 ($V_1 = -V_{I1} = -R_1\ I_2$; $V_2 = -V_{I2} = R_2 I_1$)

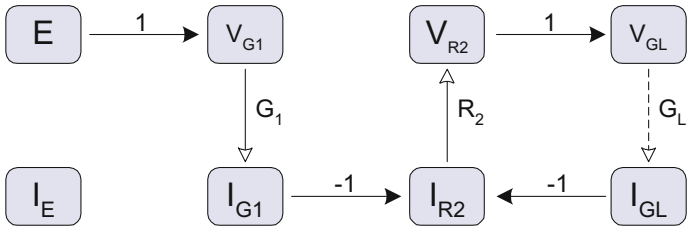


Fig. 14 SFG of the circuit from the Fig. 9c

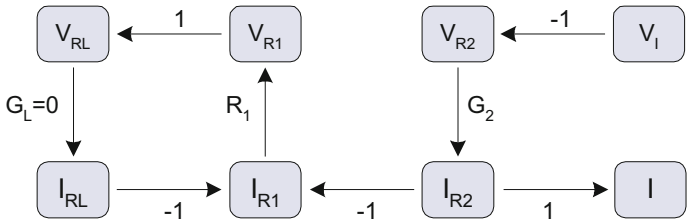


Fig. 15 SFG of the circuit shown in Fig. 9d

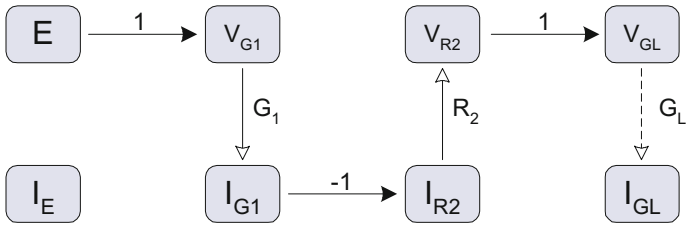


Fig. 16 SFG of the circuit from the Fig. 9e

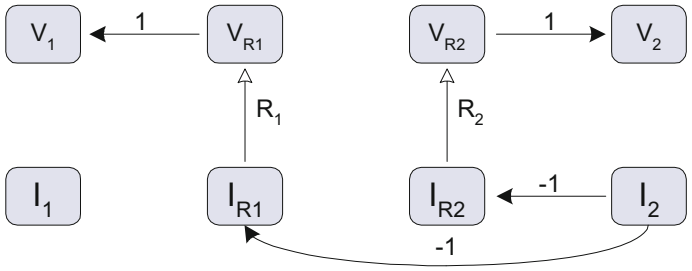


Fig. 17 SFG of the circuit of the Fig. 9f

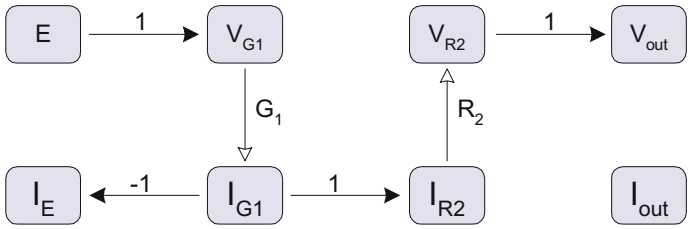


Fig. 18 SFG of the circuit from the Fig. 9g

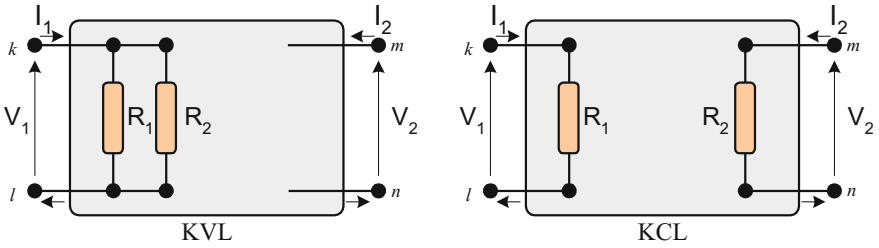


Fig. 19 Combination with two parallel resistors in the input (KVL) and two separate resistors (KCL)

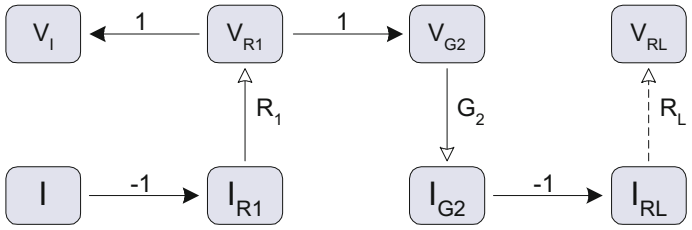


Fig. 20 SFG of the circuit shown in Fig. 19

In turn, the configuration of Fig. 9f can work as a current controlled voltage source (CCVS) transmitting the signal from the output to the input with the transmission coefficient $R_{tran} = -R_1$ and the output resistance $R_{out} = R_2$ (see corresponding SFG in Fig. 17).

The configuration shown in Fig. 9g can work as a VCVS (see SFG in Fig. 18) with the transmission coefficient $\mu = G_1R_2$, and the input resistance equal to R_1.

Of course, we can continue this analysis, but not all combinations are interesting. So we will show only some of them. For example the combination given in Fig. 19 will work as a CCCS with the transmission coefficient $\beta = R_1G_2$ (see Fig. 20) and the input resistance $R_{in} = R_1$.

A small modification of the above combination is shown in Fig. 21. It will permit constructing non-inverting current followers (for $R_1 = R_2$) with the input and output resistances equal to infinity, or the current mirror circuits (see SFG in Fig. 22).

Another interesting circuit can be constructed by the combination shown in Fig. 23.

This circuit has the SFG representation shown in Fig. 24.

The network function of this circuit can be calculated by direct application of *Mason* rule [6] to the graph of Fig. 24:

$$T(s) = \frac{V_{RL}}{E} = \frac{-G_1R_L}{1 + G_1R_2} = -\frac{1}{R_1 + R_2}R_L = -g_mR_L \tag{3}$$

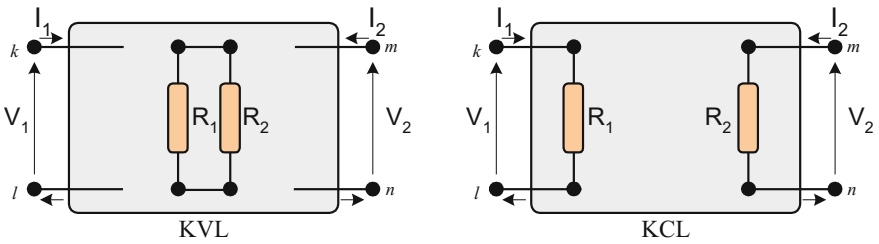


Fig. 21 Combination with two parallel resistors (KVL) and two separate resistors (KCL)

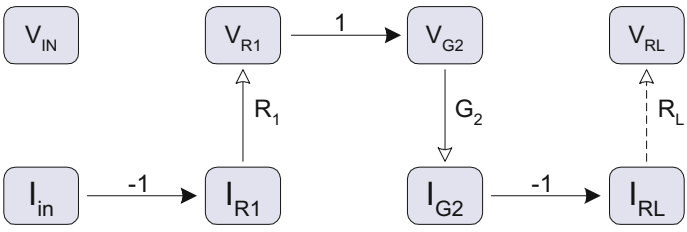


Fig. 22 SFG of the circuit shown in Fig. 21

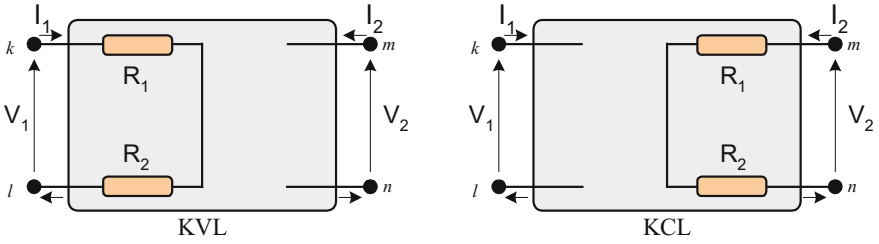


Fig. 23 Combination with two serial resistors in the input (for KVL) and the output (for KCL)

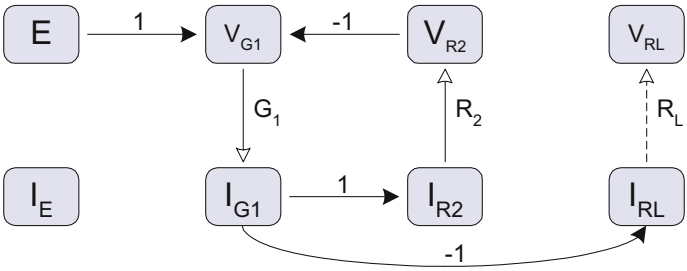


Fig. 24 SFG of the circuit of Fig. 19

where $g_m \frac{1}{R_1 R_2}$

This configuration works very stable, since the gain depends only on the values of the resistors; precisely the controlled amplifier (the gain value can be coarsely fixed by R_1, then finalized by the resistor R_2, smaller than R_1).

3.3 *Circuits Structures with Three and Four Resistors*

Circuits with only two resistors are not enough flexible. For example, the circuit shown in Fig. 9c has an output resistance equal to R_2, and, simultaneously, this value is a part of the transmission coefficient $\mu = G_1 R_2$. If we introduce additional elements in the inner structure of the circuit, we will have the possibility to remove this inconvenience. Moreover, it will be possible to build new structures. Of course, it is not possible to present all combinations of three and four resistors in the volume of one chapter; thus, we will present only a few solutions. For example, if we consider the combination of three resistors depicted in Fig. 25, we can see that this circuit is equivalent to the voltage controlled voltage source (VCVS) with the transmission coefficient is equal to $\mu = -G_1 R_2$ and the output resistance is equal to R_3, whereas the input resistance is equal to infinity, see the corresponding graph given in Fig. 26.

If we would like to have a particular circuit working as a voltage controlled voltage source with definite values of input and output resistances, we should

consider the combination of four resistors shown in Fig. 27 which SFG is given in Fig. 28.

If we compare the SFG of the above circuit with the SFG of a VCVS with the input resistance equal to R_{in}, the output resistance equal to R_{out}, and the transmission coefficient equal to μ (see the equivalent circuit and the corresponding SFG given in Figs. 29 and 30, respectively), we can see that this circuit can work as a VCVS with $R_{in} = R_4$, $R_{out} = R_3$ and the transmission coefficient $\mu = G_1R_2$.

Another combination of four resistors is presented in Fig. 31. It is easy to check that this circuit works as a current controlled current source (CCCS) with the input resistance equal to R_4, the output resistance equal to R_3 and the transmission

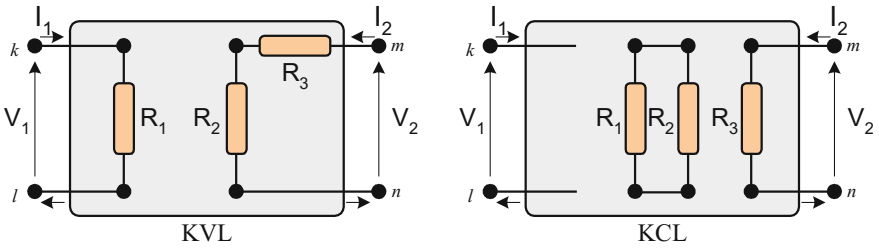


Fig. 25 A circuits with three resistors

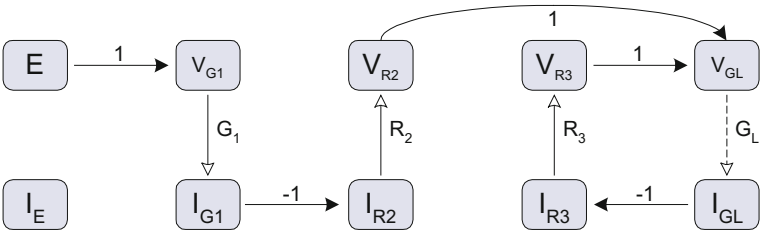


Fig. 26 SFG of the circuit of Fig. 25

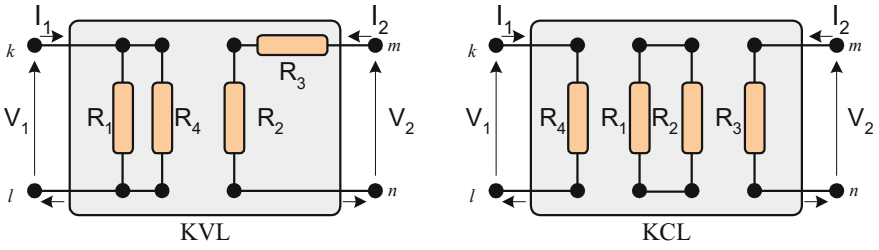


Fig. 27 A circuit with four resistors (a 1st possible combination)

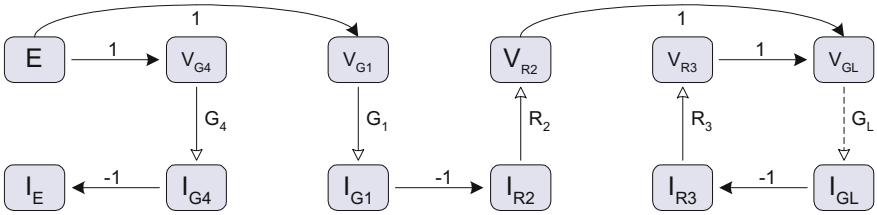


Fig. 28 SFG of the four resistor based VCVS shown in Fig. 27

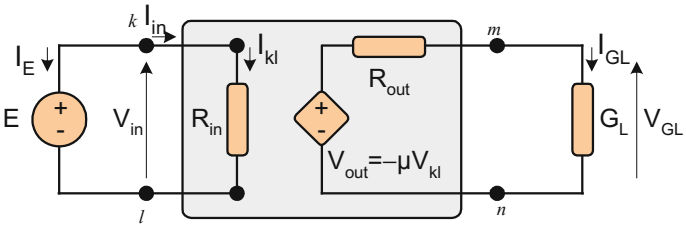


Fig. 29 An equivalent circuit of a VCVS

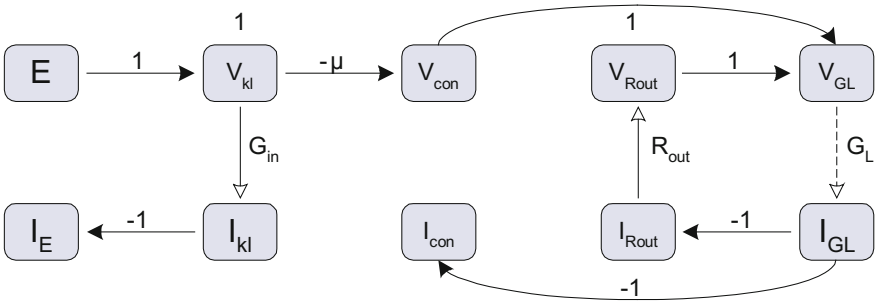


Fig. 30 SFG of the VCVS of Fig. 29

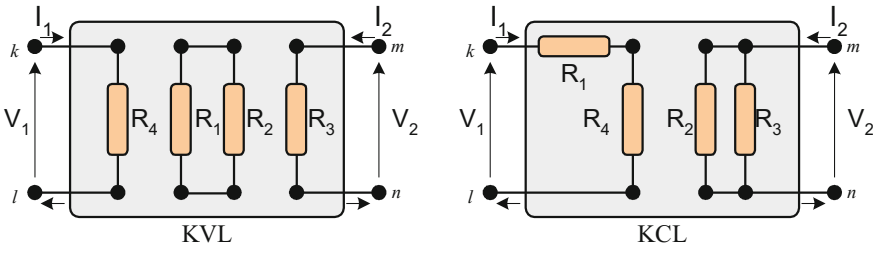


Fig. 31 A circuit with four resistors (a 2nd possible combination)

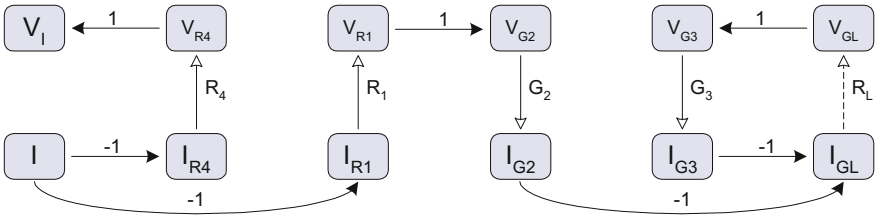


Fig. 32 SFG of the CCVS shown in Fig. 31

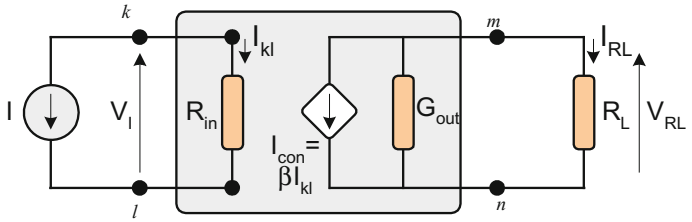


Fig. 33 An equivalent circuit of a CCCS

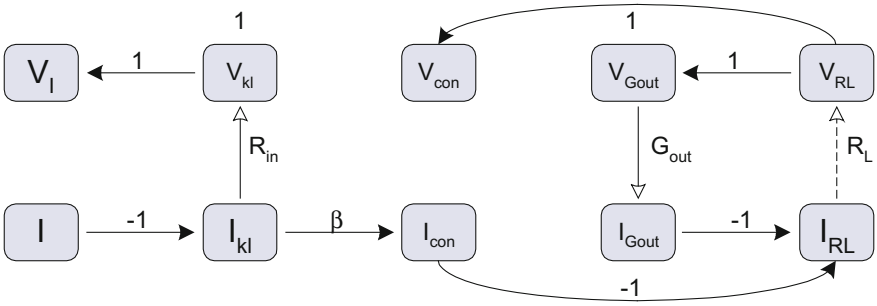


Fig. 34 SFG of the equivalent circuit of the CCCS depicted in Fig. 33

coefficient β equal to R_1G_2 (see the corresponding SFG in Fig. 32, and the CCCS's equivalent circuit and SFG in Figs. 33 and 34).

3.4 Circuits with Resistors and Passive Elements

The palette of these circuits structures can be made larger, particularly if we introduce not only resistors but the other passive elements (capacitors and inductors), also. In this chapter we will show only a few structures because the number of possible combinations is very large. We also consider only the combinations with

resistors and capacitors because in the integrated circuits the inductors are not very 'popular'.

If, in the first combination of the element connections (see Fig. 5), we introduce a capacitor instead of a resistor, then we obtain structures of a differentiator circuit. It is easy to see that the voltages on the resistor R_L are equal (see Fig. 7) $V_{RL} = (+/-)sCR_L$.

In turn, the structures on the basis of Fig. 8, with the capacitor instead of resistor, will work as an integrator with the time-constant equal to $1/(sCR_L)$. However, in both solutions the time-constant of the structures depends on the output resistor R_L. This inconvenience may be overcome when using the combinations with two elements. For example, if, in the Fig. 9e, we introduce a capacitor C in the place of the resistor R_1 (see SFG in Fig. 16), we obtain a classical differentiator with the time-constant equal to $(-sCR_2)$. In turn, if we introduce in Fig. 9e a capacitor C in the place of resistor R_2, we obtain a classical integrator (see SFG in Fig. 16) with the time-constant equal to $(-1/\mathrm{sCR}_1)$.

Another interesting circuit may be obtained on the basis of the structure shown in Fig. 19 if we introduce in the place of resistor R_1 a capacitor C. In this case we obtain a high pass filter with the network function equal to (see SFG in Fig. 24):

$$T(s) = \frac{V_{ZL}}{E} = \frac{sCR_L}{1 + sCR_2} = \frac{sR_L/R_2}{s + 1/(CR_2)} \tag{4}$$

The palette of the combinations is very reach. We present only few examples to show the viability and the potentiality of the proposed method.

4 Practical Implementations

In order to be able to fulfill KVL and KCL for the circuits proposed above, a special kind of switches has to be used. These switches have been proposed by the authors in [7, 8], and are denominated KVL-S and KCL-S. The former works as a closed switch (a shortcut) to fulfill the KVL, and as an open switch when KCL is considered. i.e. each KVL switch (KVL-S) will be switched on for the calculation of the *Kirchhoff* voltage law and switched off for the calculation of the *Kirchhoff* current law. And vice versa, each KCL switch (KCL-S) will be switched off for the calculation of the *Kirchhoff* voltage law and switch on for the calculation of the *Kirchhoff* current law.

Figure 35 shows the two possible forms for connecting a grounded or a floating resistor (capacitor).

There are many electronic elements that can ensure the concept of '*active switches*'. The most known ones are the operational amplifiers (Op-Amp) and the operational floating amplifier (OFA) [12, 13]. Op-Amps and OFAs working in the negative feedback topology, with the gain A very large (ideally infinite), can be considered as '*active switches*', as shown in Figs. 36 and 37.

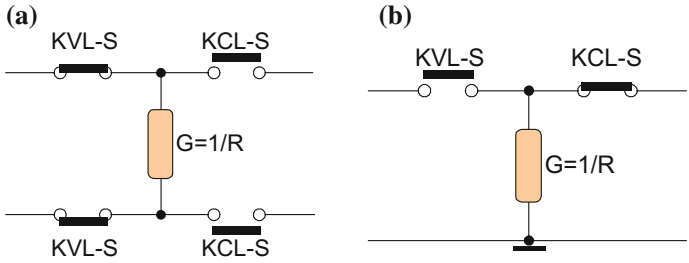


Fig. 35 Depiction of the use of the 'active switches: **a** the floating conductance is connected to fulfill the KVL, **b** the grounded conductance is connected to fulfill the KCL

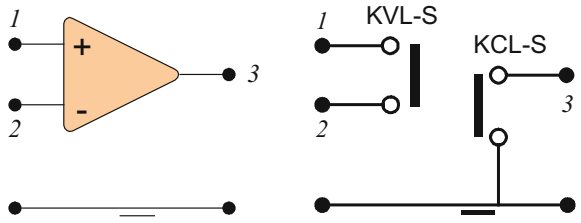


Fig. 36 The operational amplifier and its equivalent circuit with active switches

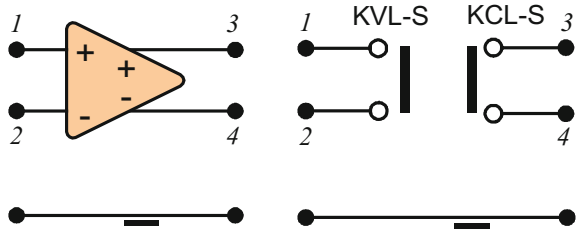


Fig. 37 The operational floating amplifier and its equivalent circuit with active switches

By means of this element we can realize, for example, the configuration shown in Fig. 9g (Fig. 38).

For calculating KVL and KCL for the above circuit, KVL-S and KCL-S switches have to be switched on/off accordingly, as shown in Fig. 39.

Now, we will show, on the basis of Fig. 39, that the circuit of Fig. 38 realizes the configuration given in Fig. 9g.

In the first step, we redraw these Figures, as it is shown (see Fig. 40).

In the second step we depict how the branches are connected and what are the reference directions for branch currents and voltages. For this purpose we draw two directed graphs associated with the circuit, the first for the directions of voltages (G_{dv}) and the second for the directions of currents (G_{di}), see Fig. 41.

In the third step we choose the trees of these graphs (heavy lines in Fig. 41) and determine the loop matrix $\boldsymbol{B_T}$ associated with the given tree and cutset matrix $\boldsymbol{Q_L}$ associated with the given cotree (see Table 1).

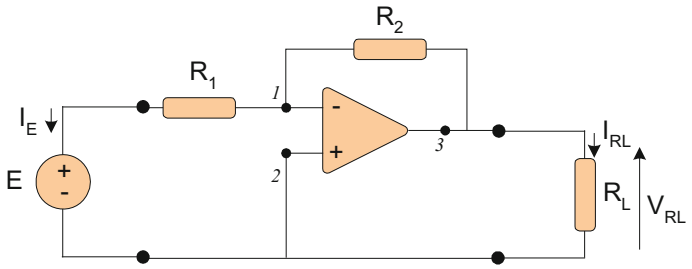


Fig. 38 Realization of the configuration of Fig. 9g

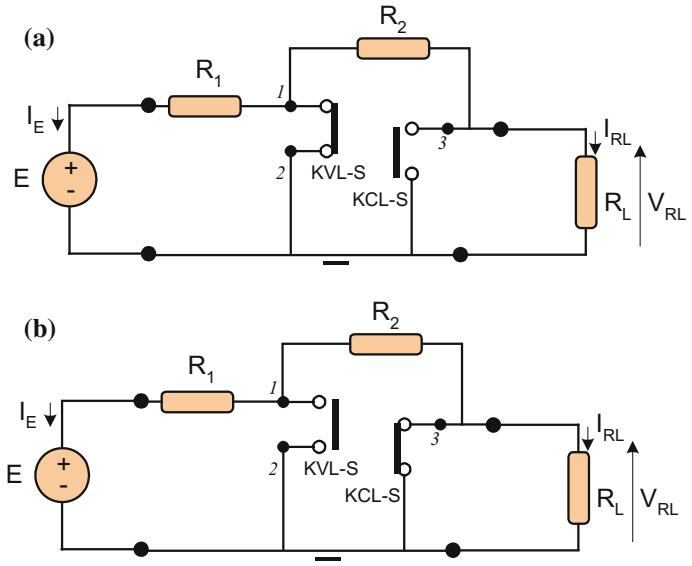


Fig. 39 The circuit of Fig. 33 with active switches. **a** KVL, **b** KCL

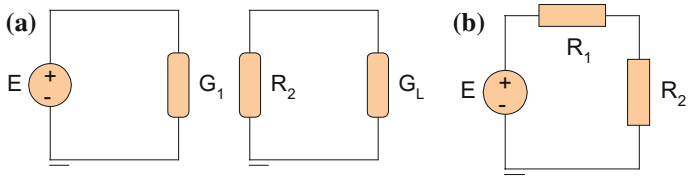


Fig. 40 The circuit of Fig. 39: **a** Circuit for calculation of KVL, **b** Circuit for calculation of KCL

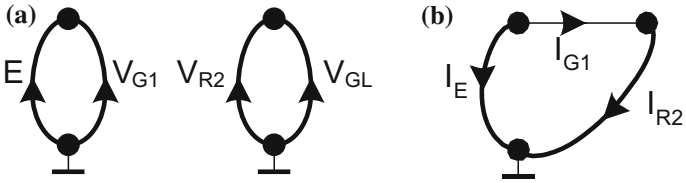


Fig. 41 The directed graphs of the circuits from Fig. 40: **a** G_{dv}, **b** G_{di}

Table 1 The $\boldsymbol{B_T}$ and $\boldsymbol{Q_L}$ matrices of the circuit from Fig. 39

B_T	**E**	$\mathbf{V_{R2}}$
$\mathbf{V_{G1}}$	1	0
$\mathbf{V_{GL}}$	0	1

Q_L	$\mathbf{I_{G1}}$
$\mathbf{I_E}$	-1
$\mathbf{I_{R2}}$	1

On the basis of the above matrices and Ohm law we can directly draw a primitive signal-flow graph (see Fig. 18).

The corresponding transfer function of this circuit can be calculated with *Mason*'s formula help:

$$T(s) = \frac{V_{RL}}{E} = -G_1 R_2 \tag{5}$$

Using the operational floating amplifier, we can realize any of the above shown combinations, for example the configuration given in Fig. 5a can be built as depicted in Fig. 42.

The equivalent circuits for the calculations of KVL and KCL are shown in Figs. 43a and b. Using the above procedure we can show that this circuit realizes the SFG shown in Fig. 7a and that this combination realizes a V to I converter presented in [13]:

$$I_2 = GV_1 \tag{6}$$

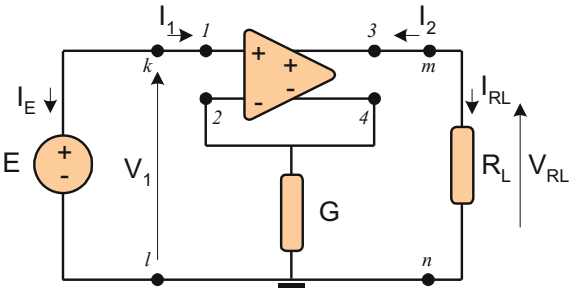


Fig. 42 A V to I converter presented in [13]

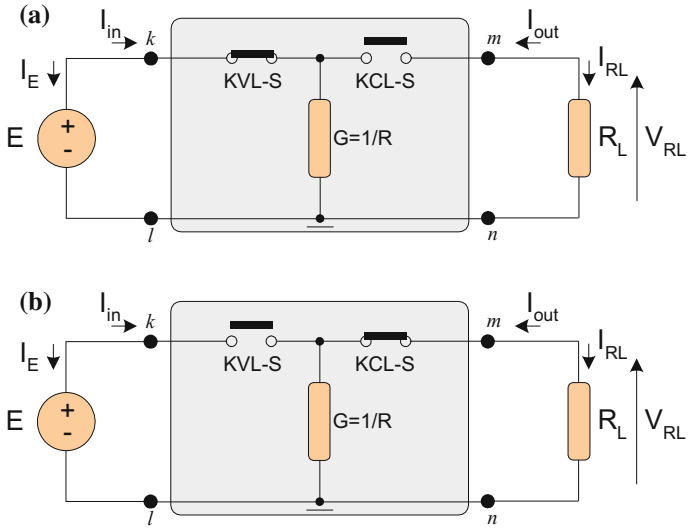


Fig. 43 The switched circuit corresponding to the circuit given in Fig. 5a: **a** the KVL configuration, **b** the KCL configuration

5 Conclusion

In this chapter, we propose a novel method for designing structures of analog building blocks and finding new ones. The approach is based on a combinatorial approach. One only has to check "all" possible combinations of connecting resistors to the input, to the output and between each other. The *active switches* are used to ensure KVL and KCL. The number of possible combination is very large. Already known active building blocks can thus be built. Furthermore, new structures can be investigated. The palette of these combinations can be made larger, particularly if we use not only resistors but also the other passive elements (capacitors and inductors). Thus, we believe that this work opens a large spectrum of future researches in this field.

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Part II
Pathological Elements in the Design of Analog Circuits

Applications of the Voltage Mirror-Current Mirror in Realizing Active Building Blocks

Ahmed M. Soliman

Abstract In this chapter four alternative realizations of the nullator using a single VM or two VMs are summarized. Similarly four alternative realizations of the norator using a single CM or two CMs are also demonstrated. It is also shown that the VM-CM pair can be used to realize a Nullor, A Voltage Op Amp, A Current Op amp, Voltage follower (VF), Voltage Inverter (VI), Current follower (CF), current Inverter (CI), Current Conveyors CCII+, CCII-, ICCII+ and an ICCII- without the use of any external resistors. The use of the VM-CM pair with additional resistors to realize the family of controlled sources, transconductance amplifiers and other active building blocks using NAM expansion is included. Finally it is shown the Nullator-CM pair as well as its adjoint which is the VM-Norator pair can also be used as Universal building blocks.

1 Introduction

The first two pathological elements were introduced in the literature by Carlin in 1964 [1] and are two terminal elements known as a nullator and a norator. A nullator has its voltage and current equal to zero. A norator has its voltage and current being arbitrary. A Nullor is a two port circuit element with its two ports being a nullator and a norator as shown in Fig. 1a. The Nullor is self adjoint [2, 3] and is floating [4] as is evident from its Nodal Admittance Matrix (NAM) given by [5–7]:

$$\begin{array}{c} \\ \mathrm{c} \\ \mathrm{d} \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{a} & \mathrm{b} \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{bmatrix} \end{array} \tag{1}$$

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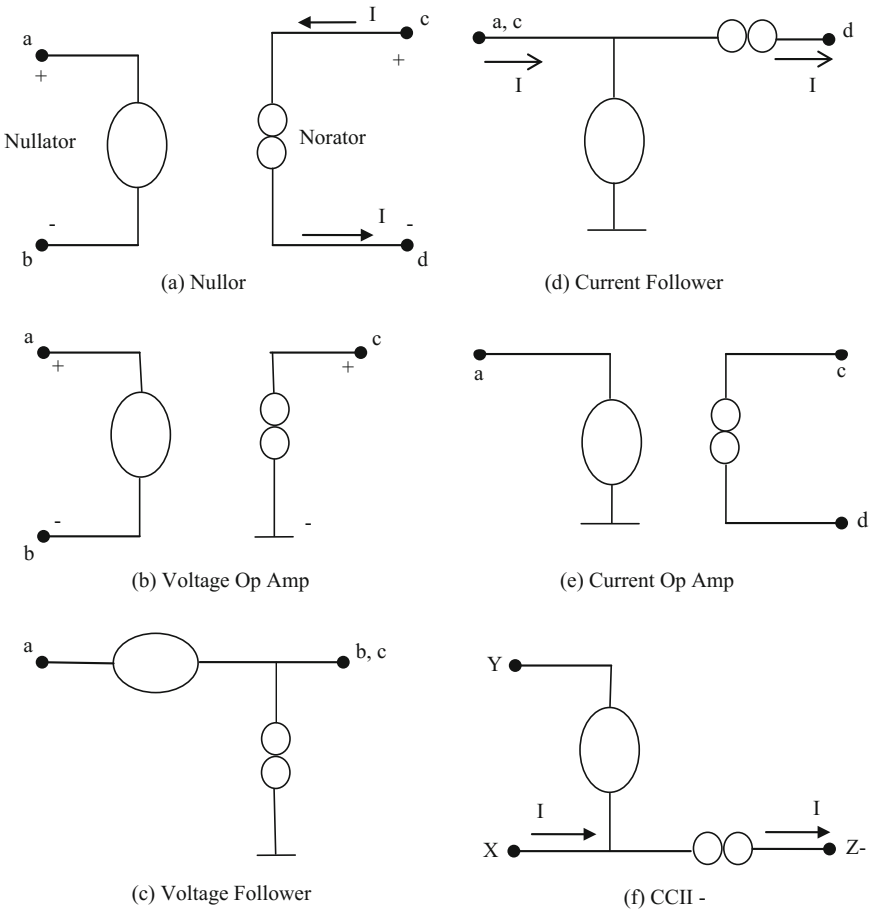


Fig. 1 Nullators and Norators realizing active blocks

The nullator and norator can also realize the Operational Amplifier (Op Amp) [8] as shown in Fig. 1b, the Voltage Follower (VF) as shown in Fig. 1c, Current Follower (CF) as shown in Fig. 1d, Current Op Amp as shown in Fig. 1e, the Current Conveyor (CCII-) [9], as shown in Fig. 1f.

The NAM stamp for the Voltage Op Amp is given by:

$$\begin{array}{cc} & \begin{array}{cc} a & b \end{array} \\ c & \begin{bmatrix} \infty_i & -\infty_i \end{bmatrix} \end{array} \tag{2}$$

The Current Op Amp is the adjoint to the VOA and is floating. Its NAM stamp is given by:

$$\begin{array}{c} \\ \mathrm{c} \\ \mathrm{d} \end{array} \begin{array}{c} \mathrm{a} \\ \left[\begin{array}{c} \infty_i \\ -\infty_i \end{array}\right] \end{array} \tag{3}$$

The CCII- is self adjoint and is floating; its NAM stamp is given by:

$$\begin{array}{c} \\ \mathrm{X} \\ \mathrm{Z}- \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{X} & \mathrm{Y} \end{array} \\ \left[\begin{array}{cc} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{array}\right] \end{array} \tag{4}$$

It is worth noting that with the Y terminal grounded, the CCII- realizes the CF as shown in Fig. 1d.

The nullator and norator cannot realize a CCII+ unless two external resistors are added to them [10], they cannot also realize the Inverting Current Conveyors (ICCII + and ICCII-) [10] without adding external resistors to them.

2 The Voltage Mirror and Current Mirror

The two additional pathological elements defined as the Voltage Mirror (VM) and the Current Mirror (CM) were introduced in the literature by Awad and Soliman in 1999 [10]. The VM and CM were used in the realization of different active building blocks in [10–18].

The VM is a two port circuit elements shown symbolically in Fig. 2a and is defined by:

$$V_1 = -V_2 \tag{5a}$$

$$I_1 = I_2 = 0 \tag{5b}$$

The CM is a two port circuit elements shown symbolically in Fig. 2b and is defined by:

$$V_1 \text{ and } V_2 \text{ are arbitrary} \tag{6a}$$

$$I_1 = I_2 \text{ and are also arbitrary} \tag{6b}$$

Although the pathological CM has the same symbol as the regular CM it is a bi-directional element and has a theoretical existence.

Although the VM and the CM cannot be realized using Nullor elements alone, they can be realized however if two additional resistors are allowed with the Nullor elements as will be summarized in the next section.

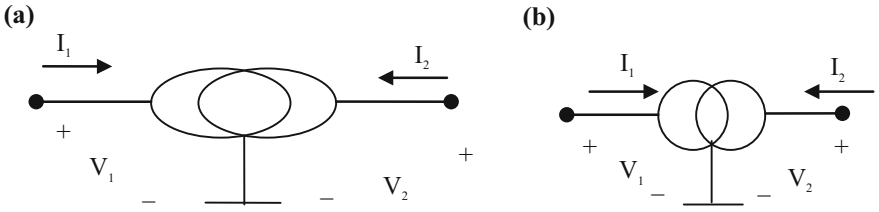


Fig. 2 The mirror elements **a** Voltage mirror **b** Current mirror

3 Realization of VM and CM Using Nullor Elements and Resistors

Two alternative realizations of the voltage mirror using two nullators, a norator and two equal resistors are shown in Fig. 3a and b, respectively. The realization shown in Fig. 3a uses grounded resistors whereas the realization shown in Fig. 3b uses floating resistors. It is seen that the currents I_1 and I_2 are equal to zero and the ground current equals to zero.

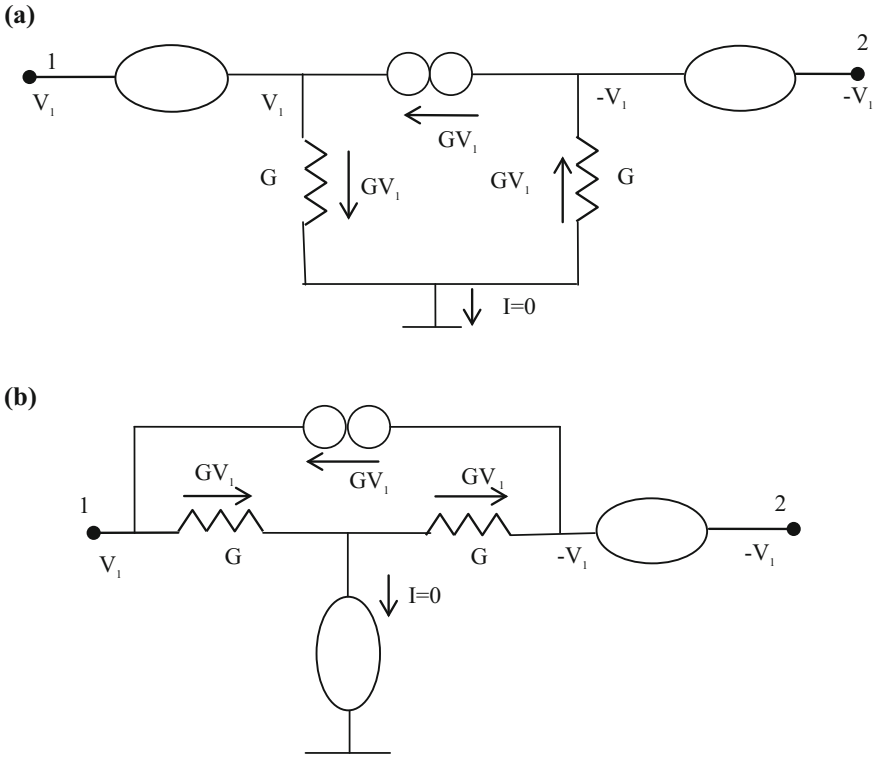


Fig. 3 Two alternative realizations of the VM using Nullor elements [10]

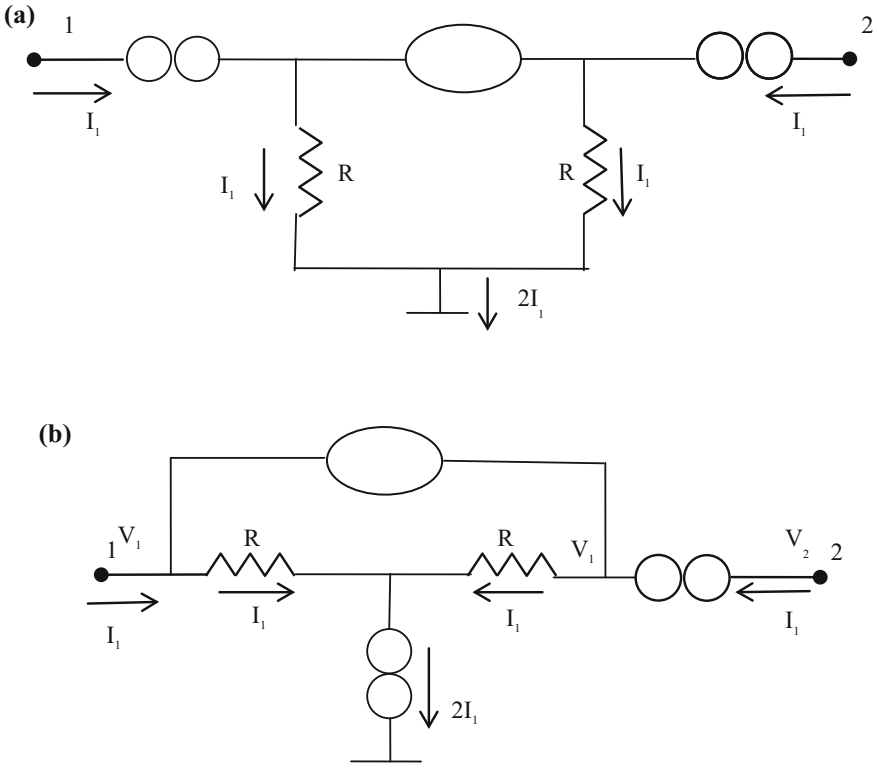


Fig. 4 Two alternative realizations of the CM using Nullor elements [10]

Two alternative realizations of the current mirror using a nullator, two norators and two equal resistors are shown in Fig. 4a and b respectively. The realization shown in Fig. 4a uses grounded resistors [10] whereas the realization shown in Fig. 4b uses floating resistors [19, 20]. It is seen that the circuit shown in Fig. 4a is the adjoint of that shown in Fig. 3a and the circuit shown in Fig. 4b is the adjoint of that shown in Fig. 3b.

4 The VM and CM Realizing Nullators and Norators

Two alternative realizations for the nullator using a single VM are shown in Fig. 5a and b [15]. For the circuit of Fig. 5a the voltage at the common node of the VM which is $(V_1 + V_2)/2$ is forced to be equal to V_2 due to direct connection, Thus, $V_2 = V_1$.

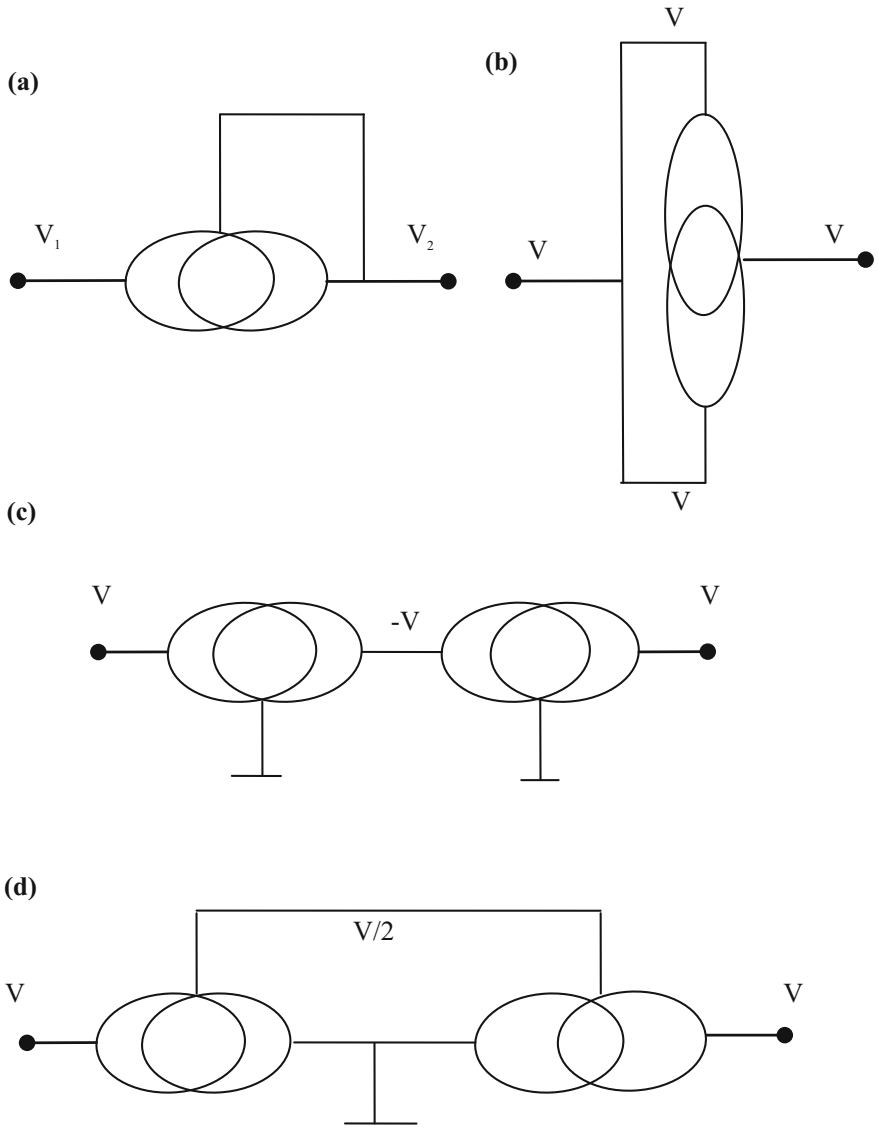


Fig. 5 Four alternative Nullator realizations using VM

Two alternative realizations for the nullator using two VMs are shown in Fig. 5c and d [15]. The circuit of Fig. 5d is a special case from the difference cell given in Fig. 11 of [15].

Two alternative realizations for the norator using a single CM are shown in Fig. 6a and b [15]. Also two alternative realizations for the norator using two CMs are shown in Fig. 6c and d [15]. The current arrows clearly demonstrates the circuits realize a norator.

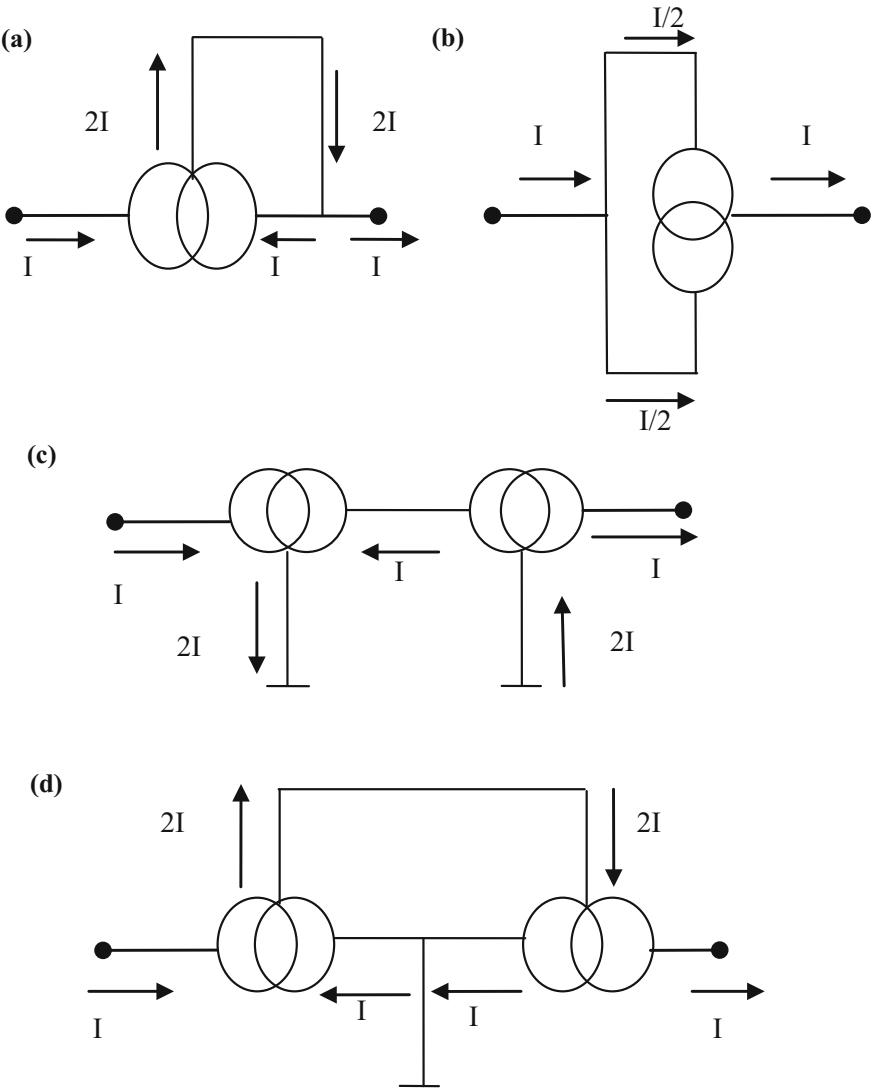


Fig. 6 Four alternative Norator realizations using CM

5 The VM-CM Pair Realizing Active Building Blocks

The VM-CM pair which is a universal element is shown in Fig. 7a where:

$$Ia = Ib = 0 \tag{7a}$$

$$Vaf = -Vbf \tag{7b}$$

$$Ic = Id \text{ and are arbitrary} \tag{8a}$$

$$Vcg \text{ and } Vdg \text{ are also arbitrary} \tag{8b}$$

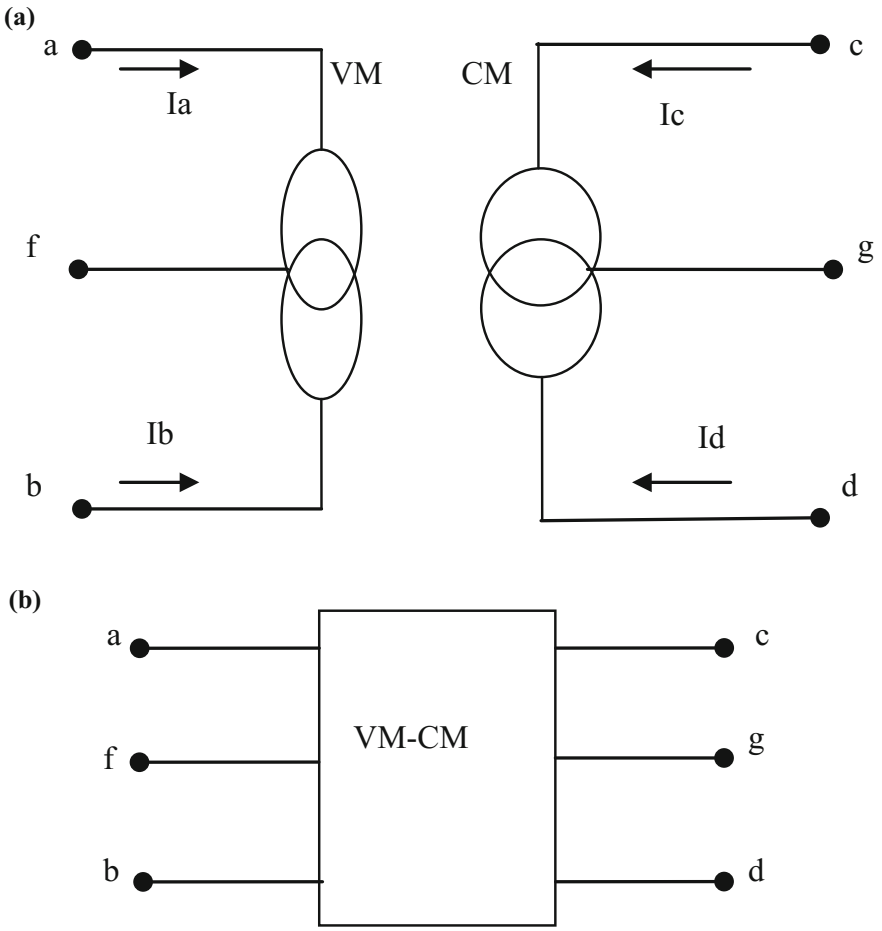


Fig. 7 The VM-CM pair as a universal element [13]

The suggested symbol for the VM-CM pair is shown in Fig. 7b. The NAM stamp for this universal element is given by Eq. (9), from which it is seen that it is self adjoint and floating.

$$\begin{array}{c} \\ \mathrm{c} \\ \mathrm{d} \\ \mathrm{g} \end{array} \begin{array}{c} \begin{array}{ccc} \mathrm{a} & \mathrm{b} & \mathrm{f} \end{array} \\ \begin{bmatrix} \infty_i & \infty_i & -2\infty_i \\ \infty_i & \infty_i & -2\infty_i \\ -2\infty_i & -2\infty_i & 4\infty_i \end{bmatrix} \end{array} \tag{9}$$

In the next section the application of the VM-CM pair in the realization of the Op Amp family is summarized and the NAM stamp for each building block is given.

5.1 Realization of the Op Amp Family

Figure 8a represents the realization of the nullor using a VM-CM pair by connecting the common terminal of the VM f to b and the common terminal of the CM g to d. This is equivalent to adding the two columns b and f in the NAM given by Eq. (9) and adding the two rows d and g and the NAM becomes as given by Eq. (10) which represents the NAM of the Nullor.

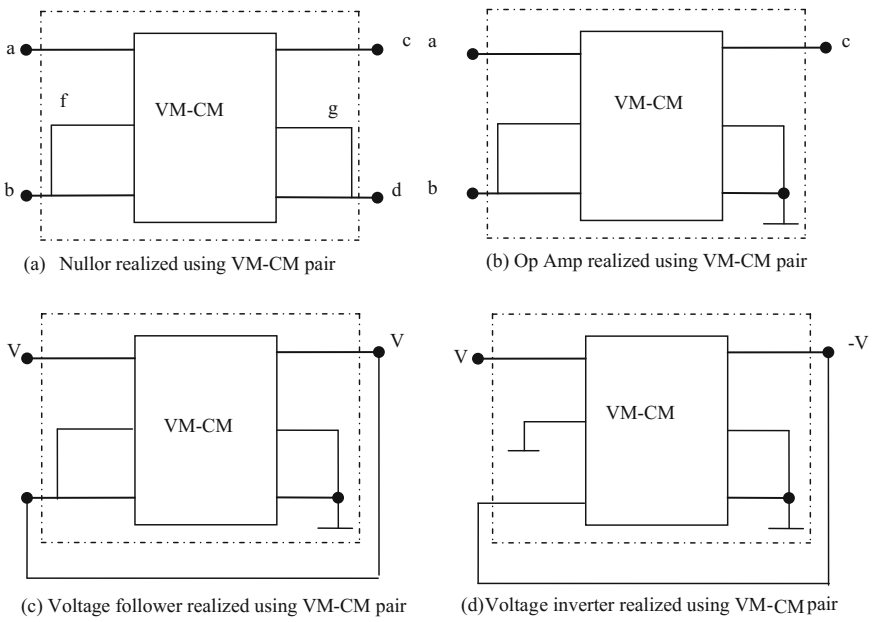


Fig. 8 Realization of the op Amp family using VM-CM pair

$$\begin{array}{c} \\ \mathrm{c} \\ \mathrm{d,\ g} \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{a} & \mathrm{b,\ f} \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{bmatrix} \end{array} \tag{10}$$

The realization given in Fig. 8a can also be considered as a combination of Figs. 5a and 6a in realizing a nullator and a norator from a VM and a CM respectively. The realization of the Op Amp is given in Fig. 8b as well as the voltage follower and voltage inverter are given in Fig. 8c and d respectively.

5.2 *Realization of the Current Conveyor Family*

As previously stated the current conveyor family cannot be realized using nullors only except the CCII- which is realized using a nullator and a norator with a common terminal as shown in Fig. 1f.

The CCII+ is realized using the VM-CM pair as shown in Fig. 9a, its NAM stamp is given by:

$$\begin{array}{c} \\ \mathrm{x} \\ \mathrm{Z+} \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{X} & \mathrm{Y} \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ \infty_i & -\infty_i \end{bmatrix} \end{array} \tag{11}$$

From Eq. (11) it is seen that the CCII+ is not floating.

The CCII- is realized using the VM-CM pair as shown in Fig. 9b, its NAM stamp is given by Eq. (4).

The ICCII+ is realized using the VM-CM pair as shown in Fig. 9c, its NAM stamp is given by Eq. (12). From Eq. (12) it is seen that the ICCII+ is self adjoint and is not floating.

$$\begin{array}{c} \\ \mathrm{x} \\ \mathrm{Z+} \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{X} & \mathrm{Y} \end{array} \\ \begin{bmatrix} \infty_i & \infty_i \\ \infty_i & \infty_i \end{bmatrix} \end{array} \tag{12}$$

The ICCII- is realized using the VM-CM pair as shown in Fig. 9d, its NAM stamp is given by Eq. (13); from which it is seen that the ICCII- is floating and is the adjoint of the CCII+.

$$\begin{array}{c} \\ \mathrm{x} \\ \mathrm{Z-} \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{X} & \mathrm{Y} \end{array} \\ \begin{bmatrix} \infty_i & \infty_i \\ -\infty_i & -\infty_i \end{bmatrix} \end{array} \tag{13}$$

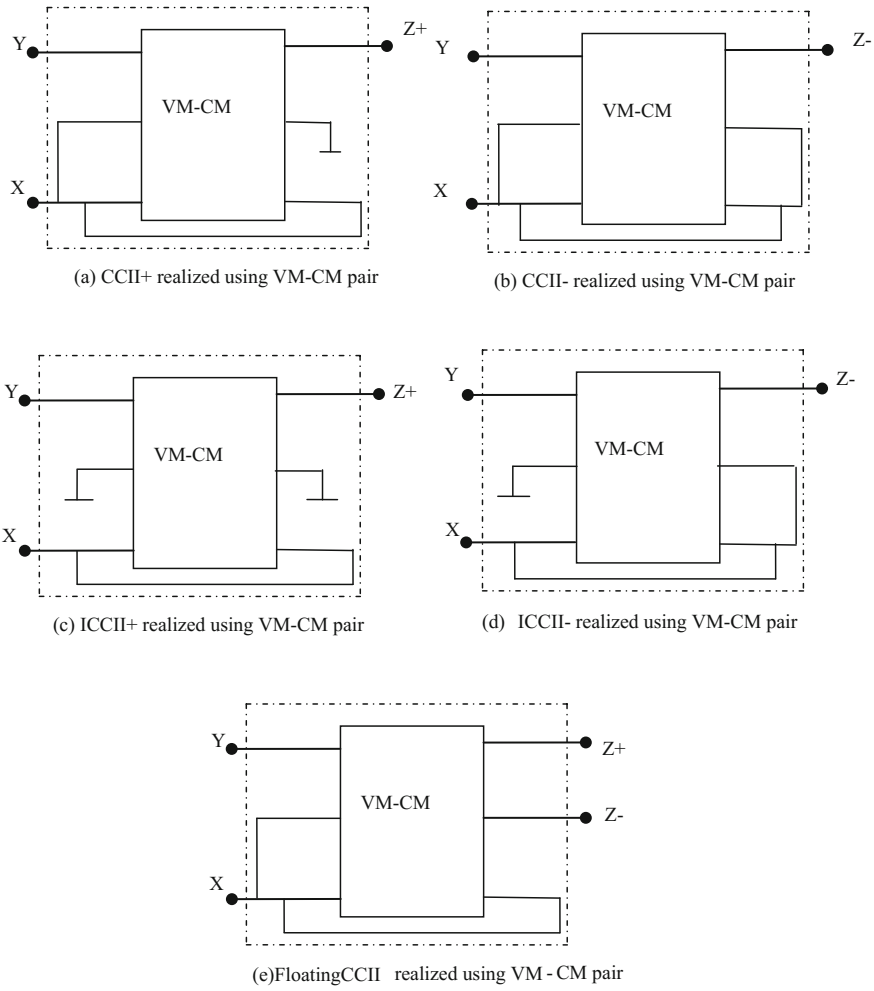


Fig. 9 Realization of the CCII family using VM-CM pair

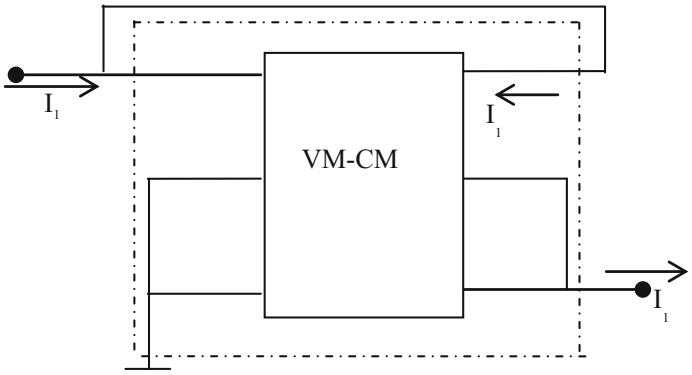
The floating CCII introduced by Soliman and Saad in [21] is realized using the VM-CM pair as shown in Fig. 9e, its NAM stamp is given by Eq. (14) from which it is seen that it is floating.

$$\begin{array}{c} \\ \mathrm{X} \\ \mathrm{Z}+ \\ \mathrm{Z}- \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{X} & \mathrm{Y} \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ \infty_i & -\infty_i \\ -2\infty_i & 2\infty_i \end{bmatrix} \end{array} \tag{14}$$

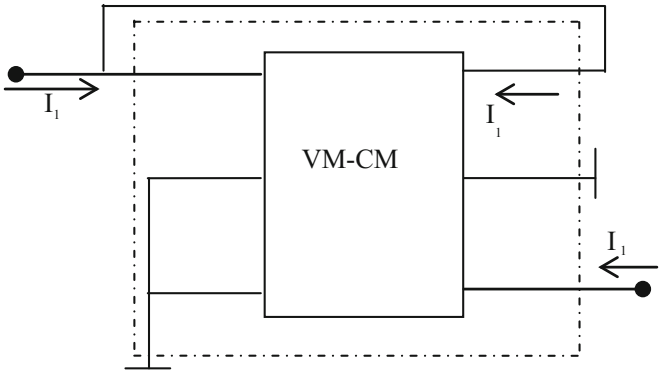
5.3 Realization of Current Follower and Current Inverter

The Current Follower (CF) which is the adjoint of the Voltage Follower (VF) is realized using the VM-CM pair as shown in Fig. 10a.

The Current inverter (CI) which is the adjoint of the Voltage Inverter (VI) is realized using the VM-CM pair as shown in Fig. 10b [22]. It is worth noting that the CI cannot be realized using nullators and norators without adding resistors.



(a) CF realized using VM-CM pair.



(b) CI realized using VM-CM pair

Fig. 10 Realization of CF and CI using VM-CM pair

6 Realization of Controlled Sources

6.1 Realization of VCVS Using VM-CM Pair

The well-known realization of the VCVS using Op Amp is shown in Fig. 11a with a voltage gain = $1 + G_1/G_2$. Its Nullor realization is shown in Fig. 11b. It is seen that one of the two resistors is floating.

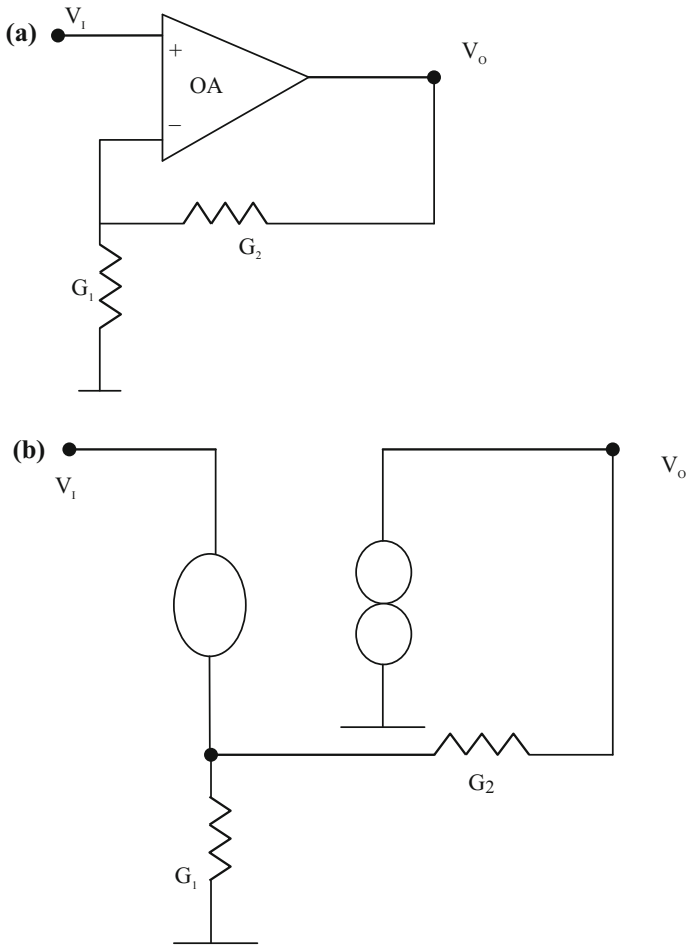


Fig. 11 Non-inverting VCVS realization using Op Amp

For VCVS if the requirement of low output impedance is relaxed on the account of the VCVS being loaded at port 2 by a high impedance such as port 1 of another VCVS, then the Y matrix can be simplified as follows [5, 23]:

$$Y = \begin{bmatrix} 0 & 0 \\ -N & D \end{bmatrix} \tag{15}$$

For a positive gain VCVS of gain $Av = G_1/G_2$, take $N = G_1$ and $D = G_2$ therefore:

$$Y = \begin{bmatrix} 0 & 0 \\ -G_1 & G_2 \end{bmatrix} \tag{16}$$

Adding a CM between nodes 2 and 3 to move $-G_1$ to the 3, 1 position, it follows that:

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & G_2 & 0 \\ G_1 & 0 & 0 \end{bmatrix} \tag{17}$$

Adding a nullator between nodes 1 and 3 to move the G_1 to the diagonal 3, 3 position it follows that:

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & G_2 & 0 \\ 0 & 0 & G_1 \end{bmatrix} \tag{18}$$

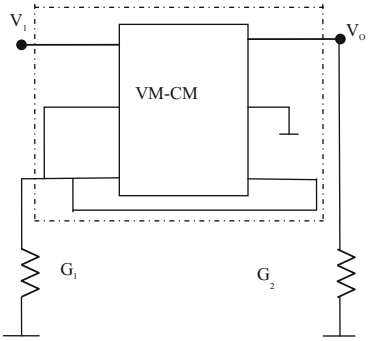
The VCVS is shown in Fig. 12a which is practically realizable by a single CCII+.

An alternative expansion for Y in Eq. (16) is possible using a VM between nodes 1 and 3 and a norator between nodes 2 and 3 as follows:

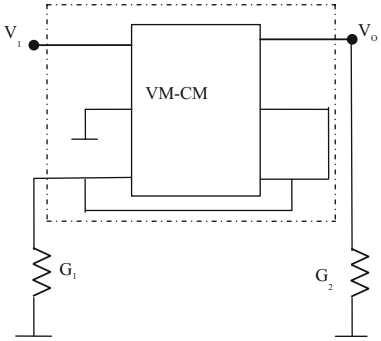
$$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & G_2 & 0 \\ 0 & 0 & G_1 \end{bmatrix} \tag{19}$$

The VCVS realization is using a VM-Norator pair (ICCII-) is shown in Fig. 12b.

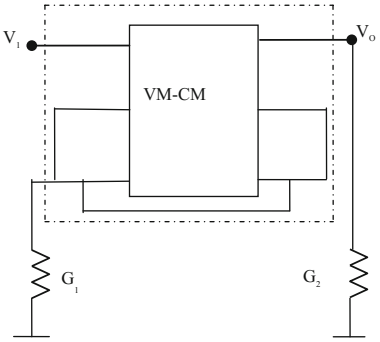
For a negative gain VCVS and from Eq. (15) and taking $N = -G_1$ and $D = G_2$ therefore:



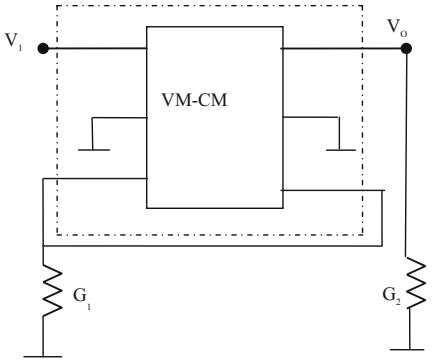
(a) Non-inverting VCVS realized using VM-CM pair



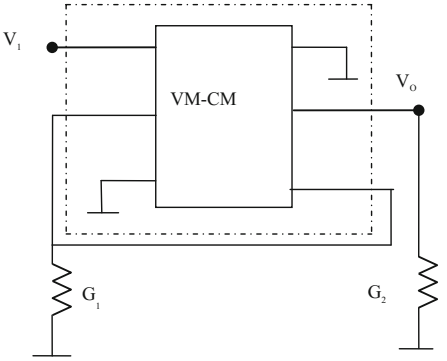
(b) Alternative non-inverting VCVS realized using VM-CM pair



(c) Inverting VCVS realized using VM-CM pair



(d) Alternative inverting VCVS realized using VM-CM pair



(e) Additional inverting VCVS realized using VM-CM pair

Fig. 12 Five alternative realizations of the VCVS using VM-CM pair

$$Y = \begin{bmatrix} 0 & 0 \\ G_1 & G_2 \end{bmatrix} \tag{20}$$

Adding a nullator between nodes 1 and 3 and a norator between nodes 2 and 3 to move the G_1 to the diagonal 3, 3 position it follows that:

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & G_2 & 0 \\ 0 & 0 & G_1 \end{bmatrix} \tag{21}$$

The grounded resistor inverting VCVS realization using CCII- [23] is shown in Fig. 12c.

An alternative realization of the grounded resistor inverting VCVS is shown in Fig. 12d which in fact is using ICCII+. Another alternative realization of the grounded resistor inverting VCVS is shown in Fig. 12e which is not using any of the CCII family.

6.2 Realization of CCCS Using VM-CM Pair

The Nullor realization of the CCCS is shown in Fig. 13 which is the adjoint of Fig. 11b with a current gain = $1 + G_1/G_2$. It is seen that one of the resistor R_2 is floating.

Following similar NAM expansion steps, four realizations for the CCCS are given in Fig. 14.

6.3 Realization of TA Using VM-CM Pair

Several pathological realizations of the VCCS also known as Transconductance Amplifiers (TA) are given in the literature [23–25].

The TA- is defined by the following admittance matrix Y:

$$Y = \begin{bmatrix} 0 & 0 \\ G & 0 \end{bmatrix} \tag{22}$$

The TA+ is defined by the following admittance matrix Y:

$$Y = \begin{bmatrix} 0 & 0 \\ -G & 0 \end{bmatrix} \tag{23}$$

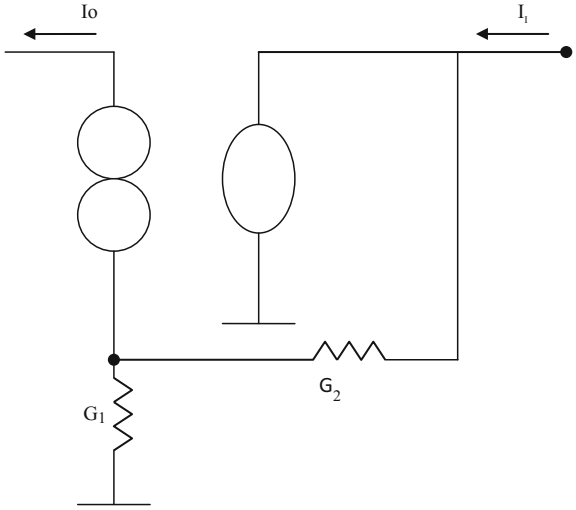
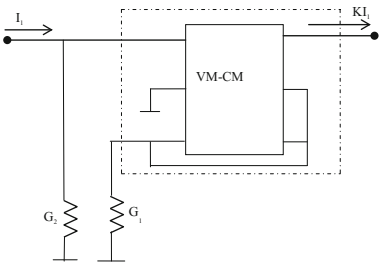
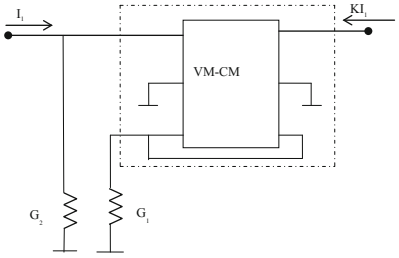


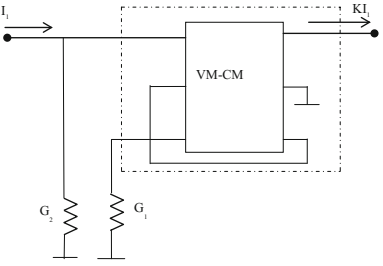
Fig. 13 Realization of CCCS using Nullor



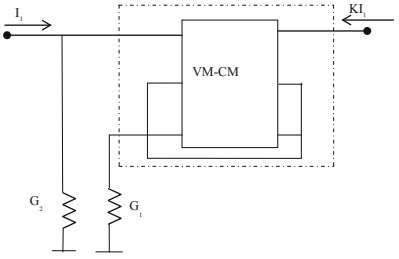
(a) Realization of CCCS of a positive gain using VM-CM pair



(c) Realization of CCCS of Negative gain using VM-CM pair



(b) Alternative realization of CCCS of a positive gain using VM-CM pair



(d) Alternative realization of CCCS of Negative gain using VM-CM pair

Fig. 14 Four alternative realizations of the CCCS using VM-CM pair

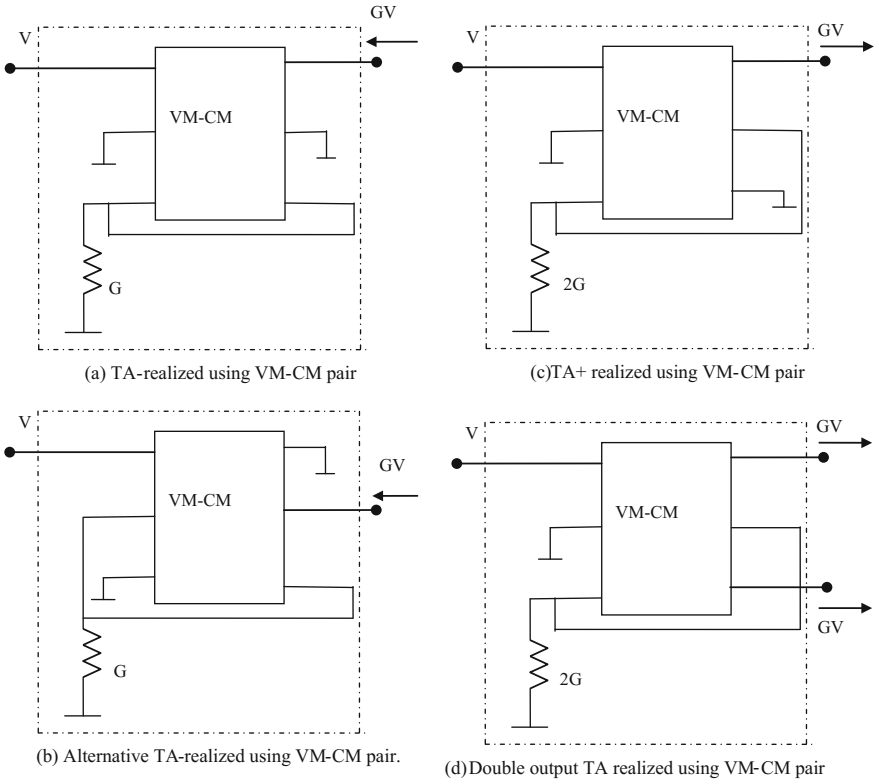


Fig. 15 Four alternative realizations of the TA using VM-CM pair

The realizations of the TA using the VM-CM pair can be generated using NAM expansion and are summarized in Fig. 15. The realization of Fig. 15b is using the common terminal of the VM and the CM. The realizations of Fig. 15c, d are using the common terminal of the CM.

In the next section two alternative universal building blocks are mentioned very briefly to limit the Chapter length.

7 The OMA and the VM-Norator Pair

The VM-Norator pair also known as the OMA [26] is shown symbolically in Fig. 16a and is realized using the VM-CM pair as in Fig. 16b.The OMA is represented by the following equations:

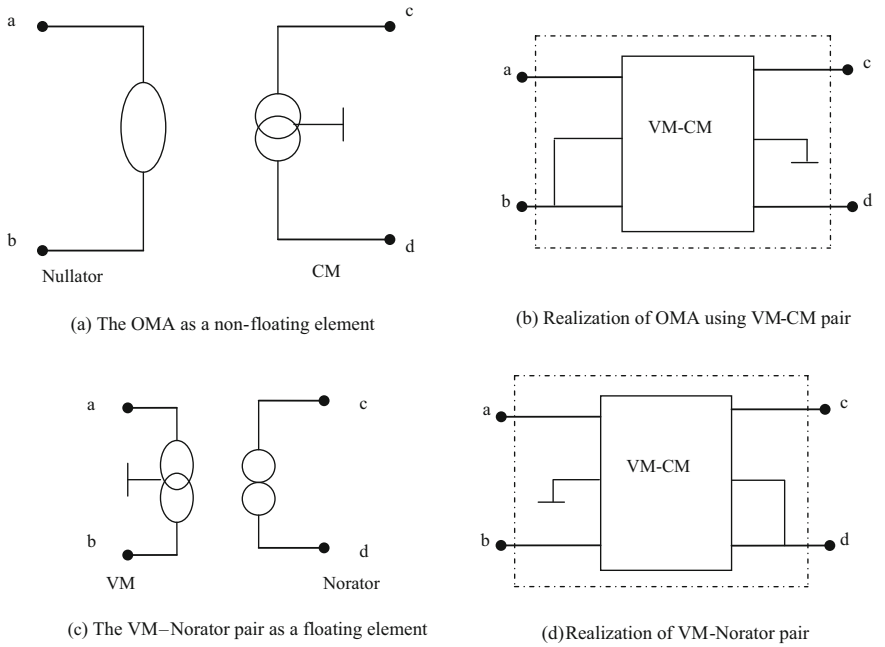


Fig. 16 The OMA and the VM-Norator pair as adjoints

$$\mathrm{Va} = \mathrm{Vb}, \mathrm{Ic} = \mathrm{Id} \tag{24}$$

Its NAM stamp is given by Eq. (24) from which it is seen that it is a non-floating building block.

The Nullator-CM pair is also a universal building block and is shown symbolically in Fig. 16c and is realized using the VM-CM pair in Fig. 16d, Its NAM stamp is given by Eq. (23) from which it is seen that it is a floating building block and is the adjoint of the OMA [4].

$$\begin{array}{c} \\ \mathrm{c} \\ \mathrm{d} \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{a} & \mathrm{b} \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ \infty_i & -\infty_i \end{bmatrix} \end{array} \tag{25}$$

$$\begin{array}{c} \\ \mathrm{c} \\ \mathrm{d} \end{array} \begin{array}{c} \begin{array}{cc} \mathrm{a} & \mathrm{b} \end{array} \\ \begin{bmatrix} \infty_i & \infty_i \\ -\infty_i & -\infty_i \end{bmatrix} \end{array} \tag{26}$$

8 Conclusions

The importance of the VM-CM pair as a universal element is demonstrated in this chapter. The realization of a nullator using a single VM or two VMs is summarized. Also the realization of a norator using a single CM or two CMs is also included.

The use of the VM-CM pair with additional resistors to realize the family of the controlled sources, transconductance amplifiers and other active building blocks with NAM expansion demonstration has been included.

Finally it is shown the Nullator-CM pair as well as its adjoint which is the VM-Norator pair can also be used as Universal building blocks [27].

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Circuit Biasing Using Fixator-Norator Pairs—A Tutorial

Reza Hashemian

Abstract A procedure based on local biasing is presented in this chapter. This procedure initiates from port nullification and extends to nonlinear device nullification. It is shown that when a device internally powered but is nullified through its ports it is locally biased. A device can be locally biasing with full supplies, or with reduced number of supplies, and the differences are discussed. The main advantage of local biasing of a device is separating it from the rest of the circuit and bias it individually based on its requirements. Disadvantages of local biasing, however, is its practicality, requiring numerous supply sources and in disarrays. The solution presented here is biasing through the use of fixator norator pairs (FNPs). By using FNP we are able to fix each transistor to its designated operating point, just like local biasing, while the power supplies remain in their normal location in the circuit (global biasing). Properties on fixators and norators are discussed and component modeling using FNPs are introduced. These models are of two types, linear and nonlinear. The effort in this chapter has been on making it a tutorial on the subject, and this has been done through several examples. The examples start from simple circuits and move into more elaborate integrated circuits.

Keywords Amplifiers · Analog circuit design · Biasing design
Fixator-norator pairs · Local biasing · Nullification

1 Introduction

Biasing of large and complex analog circuits has always been a great challenge for the designers. The challenge is normally in two areas. First, to get the number of iterations minimized and make the convergence possible and rather quick; second, to move to the right regions of operations for the active components so that the output signals could get far from being distorted or clipped. Both problems become

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complex as the number of active devices increase, the design requirements become tighter, and more efficient designs are in demand. One difficulty appears to be the lack of separation between the linear and nonlinear components in the circuit during the process. Traditional biasing techniques deal with the circuit as a whole, with no break or circuit partitioning; hence, the complexity quickly increases as the circuit grows [1, 2].

Recently a new biasing technique has been introduced that somewhat breaks the tradition [3–5]. It starts with biasing nonlinear components (say transistors) individually, and makes each transistor to become DC-isolated and to operate at its own selective operating point (OP). Here each transistor is biased locally without interfering with other components in the circuit. A major advantage in using this technique is to deal with nonlinearity locally and to avoid any nonlinear operation in the original circuit, as a whole. One may even claim zero nonlinearity being involved in this situation. This is because biasing individual transistors to operate at their desired OPs is just a matter of local sourcing.

In the method presented by Verhoeven et al. [3] the design of amplifiers is carried out linearly and in AC domain. Here the circuit biasing—performed at the end of the design—is reduced to just the transistors' biasing, which is again a local sourcing of the transistors, so that they can get to the OPs intended for each, without being interfered by other DC sources. This technique makes each transistor DC-isolate and it uses controlled sources for local adjustments. Although the controlled sources are later removed but initially they cause timely iterations until they are eliminated. In [4] this author presents a somewhat similar biasing method, called "local biasing". Despite the technique used in [3], here no controlled source is used for the biasing purposes. In addition, it is shown [3, 4] that in each locally biased port only one DC source delivers power to the device and the other source is sitting idle. As demonstrated, this property helps to cut down the number of biasing sources in the circuit by half, and the other half can be replaced with coupling capacitors. This is of course for the case that the biasing voltage sources are sitting idle. Similarly, in the case of the current sources delivering zero power inductors can replace them.

With all advantages and significant simplifications local biasing offers [4, 5], one major difficulty still remains to be addressed. The question is how to deal with those "scattered supplies" used in the circuit due to the local biasing? As expected, each bipolar transistor needs four (voltage and current) sources to get locally biased. There are known circuit techniques [3, 6] that are used to deal with the problem. The method proposed by Verhoeven et al. [3] uses shifts and other source transfer techniques to reduce the sources and push them to specific locations [6]. Techniques such as voltage dividing, source shifting, and current sourcing and mirroring help to reduce the number of DC supplies and push them to the right locations in the circuit. As expected, the method is more gradual and long and tedious procedures used often reduce the attraction and practicality of these methods. In addition, by implementing these procedures, there is no guaranty to ensure an optimal or a desirable solution.

In our methodology we are offering a new source transformation technique that despite the conventional one it does the entire process in a single step. We may begin the design of an analog circuit by choosing a desirable circuit topology. In case the design uses discrete components the nonlinear components (transistors) represent the drivers that must be biased to selected OPs. Now, because the regions of operations are specified for the drivers we can simply replace the transistors by their small signal linear models, bypassing the entire nonlinearity, and go directly for the design of the (linearized) AC circuit. Note that because no DC analysis is attempted yet then no DC supplies are specified. Indeed, in our methodology the circuit biasing is pushed to the end and it begins when the AC design is successfully completed, and the regions of operations (or simply OPs) for the drivers are specified, for maximum output swings and minimum distortions.

On the other hand, if the target circuit is an integrated circuit then we are facing with two types of nonlinear components: the drivers and the supporting components, such as current sources, current mirrors and active loads. Similar to the previous case here we also start the design for AC signals. We replace the drivers with their small signal linear models at the desired OPs, and the other nonlinear supporting components are also replaced with their linearized equivalent impedances for small signals (such as a dynamic load resistance ro), as specified by the design criteria.

Up to this point, the process of analog circuit design has followed a conventional routine. We still need to know how to design the biasing of the circuit to fulfill the following two conditions: (i) have the DC (voltage) supplies with specified values located at their selective locations in the circuit, and (ii) have the drivers, as well as the supporting components, biased at their selective OPs. In most cases the location of supplies, such as V_{CC} and V_{DD}, and their values are predetermined for the design. In such cases the question is, how to fulfill both set of requirements: (i) have the DC power supplies with specified values and specified locations in the circuit, and (ii) achieve the AC design requirements without any nonlinear iterations and with minimum design efforts? As discussed before, one way to do this is to design for the AC case first with the load and node impedances required for the design and do the biasing later. Traditional biasing methods start with fixed supplies at fixed locations in the circuit; whereas our method is to start biasing the individual transistors and move the biasing sources to the desired locations later. With the first method nonlinearity is unavoidable and because of the fixed AC models of the transistors fulfilling all design specifications is hard and time consuming. However, the difficulty with the individually biasing the transistors is to end up with too many (voltage and current) sources in the circuit, and unless we move all the sources to one or two designated locations, for the DC supplies, the job is incomplete. Again, what makes the proposed technique more attractive is the fact that, in one step this move takes place and those one or two supplies get replaced for all the sources used for the individual transistors biasing. This certainly eliminates all those conventional source reduction and transformation as well.

The tool we are going to use to achieve our goal is fixator-norator pair.[1] It is shown that while the use of fixators help to keep the critical biasing specs unchanged the matching norators actually find the values and the locations of the DC supplies. As it is shown, the use of fixator-norator pairs (or actually nullor pairs) is temporary here. The pair actually works as a catalyst, and get removed from the circuit after the DC supplies are allocated. This suggests that, there is no need to replace the norators with actual devices (such as Op-Amps or OTAs and so on). In fact, because of the temporary nature of the nullor pairs ideal controlled sources of type VCVS, VCCS, CCVS, and CCCS with high gains, approaching infinity, will perfectly do the job.

The use of nullor pair in analog designs has been very extensive [7–9]. Tlelo-Cuautle also introduces biasing techniques for amplifiers at nullor levels [10, 11]. These techniques use nullor pairs and their governing rules to simplify the biasing. The pairs are then replaced with transistors or Op-Amps for the final design. Haigh, Clarke and Radmore introduce a new framework for linear active circuits that use a special type of limit-variable in the circuit admittance matrix. This variable being initially finite can approach infinity resembling high gain Op-Amps or transistors as nullors [12–14]. Claudio Beccari [15] also uses the nullor concept eloquently to find and allocate the transmission zeros in a circuit.

The method proposed in this article is using nullor pairs (in form of fixator-norator pairs FNPs) quite differently. The pairs are used as tools to reallocate the DC supplies and conduct the DC power to the transistors, and then disappear. It is only during the circuit analysis and simulation that, in a fixator-norator pair, the fixator is used to sense certain specified current or voltage (OP) in the circuit. This sensing then tries to control a voltage across or a current through the associated norator. As a result, the voltage or current found for each norator is, in fact, an indication that indeed a DC (voltage or current) supply exists at the location that has caused the biasing. We repeat this for all critical ports (with biasing specified) until all supplies are allocated.

The rest of the materials in this article are arranged as follows. Section 2 is on fixator-norator pairs. The behavior and properties of fixators and norators are discussed in this section. Local biasing is reviewed in Sect. 3. Models of locally biased MOS and bipolar transistors are given in this section. The use of fixator-norator pairs in global biasing of analog circuits is investigated in Sect. 4. Rules governing the fixators and norators are also discussed here. Section 5 is on implementation aspects of fixator-norator pairs for biasing. An algorithm developed in this section provides a systematic procedure into the design of biasing for analog circuits. Two examples are worked out in Sect. 6 that use the FNP methodology introduced here as the basis for the biasing design of analog VLSI circuits. Finally, Sect. 7 concludes our discussions on analog circuit design with emphasis on biasing.

[1]This is similar to nullor pair except a fixator-norator pair can accept sources.

2 Nullification

To begin with, we need to define some terms that are used in the chapter [4]. We should also notify that all our discussions here apply to DC supplies and biasing, unless stated otherwise. We start from a port, which is a two terminal in a circuit used for signal or power exchanges. Later we move into devices, particularly nonlinear devices such as diodes BJT and MOS transistors for biasing purposes.

2.1 Port Nullification

In a circuit *N*, a port j(v_j, i_j) is *null* if the voltage v_j across the port and the current i_j through the port are both zero. In an unpowered circuit all ports are null. The question is, how do we *nullify* a port when the circuit has one or more DC supplies? Let us first define *Nullification*. In a circuit N with one or more DC supplies, a port j (v_j, i_j) is *nullified* if a voltage source v_j and a current source i_j are added to the port in order to make it null. Specifically, consider a circuit N, shown in Fig. 1a, which is partitioned into two sub-circuits N_1 and N_2, connected together through a port j (v_j, i_j). To nullify the port, all we need to do is to add two pairs of v_j and i_j sources to both sides of the port, as shown in Fig. 1b. This generates a null port k(v_k, i_k), but apparently nothing changes inside N_1 or N_2. Now we can separate the two newly formed sub-circuits N'_1 and N'_2 from port k(v_k, i_k) and leave the ports open, short circuited, or even connect either sub-circuits to another two-terminal circuit with no power supply in it; and in all doing this no change takes place inside N_1 or N_2. For example, sub-circuit N'_1 in Fig. 1b can be reduced to N_1 when all DC supplies are removed, as indicated in Fig. 1c.

Another important point to notice is that, in a port nullification only one source supplies (or consumes) power, and the other source stands idle. For example, in the port nullification given in Fig. 1b and c only the current sources are supplying power and the voltage sources stay idle. It will be revered if we move the current sources to the other side of the voltage sources.

Example 1 Consider the MOS diode circuit of Fig. 2a. The MOS transistor is characterized by: $\mu_n C'_{ox} = 200\ \mu A/V^2$, W/L = 10/2, and $V_{tn} = 1$ V. The circuit is partitioned into two parts, N_1 and N_2, connected together through a port j(v_j, i_j). If we analyse the circuit for DC operation we find that v_j, = 3 V and i_j = 1 mA. Next we apply a procedure similar to that in Fig. 1c, which is removing all supplies from N_1 and augmenting N_2 with a voltage source v_j and a current source i_j as shown in Fig. 2b. This causes the port k(v_k, i_k) to get nullified. So, if we remove v_j and i_j sources from N_1 and include them in N_2 we get two sub-circuits N'_1 and N'_2 separated by the null port k(v_k, i_k), as shown in Fig. 2b. Note that N'_1 is only a resistance network with no source, apparently nullified, and it can be reduced to a single resistor. This is the same as the Thevenin equivalent resistor $R_{th} = 2.86$ KΩ. In other words, the combination of R_{th} and the two sources, v_j, = 3 V and i_j = 1

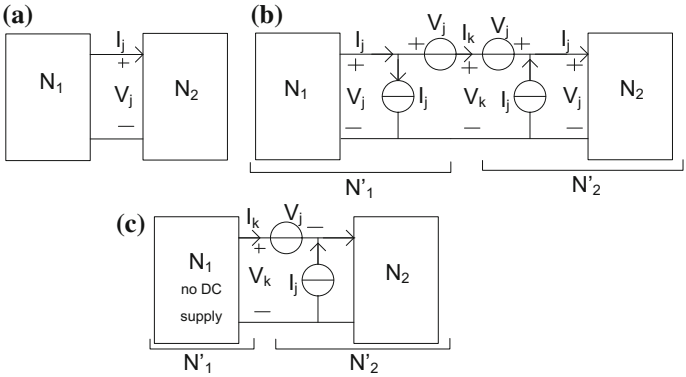

Fig. 1 Circuit nullification process; **a** Partitioned circuit, N_1: the power supplier, and N_2: devices to be nullified; **b** Power removed from N_1 and N_2, nullified; **c** Both N'_1 and N'_2 nullified

mA, form the hybrid equivalent circuit (H-model) of N_1, as shown in Fig. 3 [16], and reported in [17, 18]. Notice that for the MOS diode, on the right, a gate-source voltage of $V_{GS} = 3$ V will produce a current of

$$I_D = \frac{1}{2}\mu_n C'_{ox} W/L(V_{GS} - V_{tn})^2 = \frac{1}{2}.200.10/2(3-1)^2 = 2\,mA.$$

Hence, including the two sources, v_j, = 3 V and $i_j = 1$ mA into the sub-circuit N_2 will nullify its port, as expected.

2.2 *Multi-port Networks*

Port nullification can be generalized to include multi-port networks. Examples are BJT or MOS transistors. In general, consider a circuit N, partitioned into two sub-circuits N_1 and N_2 that are connected together through n ports, $j(v_j, i_j)$, all j = 1, 2, … n, as shown in Fig. 4a. Next, we nullify the ports by adding voltage sources v_j and current sources i_j to each port, as demonstrated in Fig. 4b. This simply creates n new and nullified ports $j_0(v_{0j}, i_{0j})$, all j = 1, 2, … n. This is for the sub-network N_2. To nullify the ports from the other side, it is sufficient to remove all DC supplies from N_1. Note also that if we remove N_2 in Fig. 4b we basically leave N_1 in its H-model [18].

The following algorithm provides a simple procedure to nullify circuit ports.

Algorithm 1

Consider a circuit N that is partitioned into two sub-circuits N_1 and N_2, through n ports. Let us assume N_1 contains the power supplies and the DC Power Conducting (DCPC) components of N, and N_2 consists primarily of the nonlinear devices. To nullify the ports we need to go through the following steps:

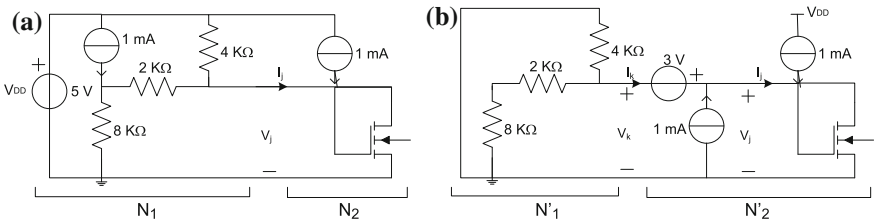

Fig. 2 Circuits for Example 1. **a** Partitioned circuit, N_1: the linear and power supplier, and N_2: the device to be nullified; **b** N'_1 and N'_2 nullified (Power removed from N'_1)

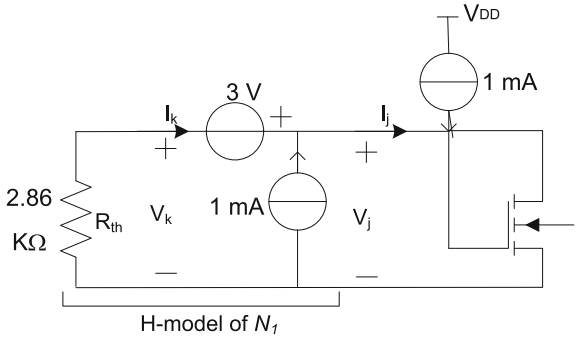

Fig. 3 Circuits for Example 1. Partitioned circuit, N_1: H-model equivalent circuit, and N_2: the device to be nullified

1. For each port j(v_j, i_j), all j = 1, 2, … n, add a voltage source v_j and a current source i_j to the port in N_2, as shown in Fig. 4b.
2. Remove all supplies from N_1.

Example 2 Consider a two stage BJT amplifier with feedback, shown in Fig. 5a. The transistors are biased through a power supply V_{CC}, and a current source I_S. Next, we partition the amplifier into two sections (sub-circuits) N_1 and N_2, where N_2 consists of the two transistors, and N_1 keeps the rest of the circuit that includes the power supplies and the DCPC components. By doing this we have simply separated the nonlinear components from the linear portion of the amplifier. Next, we can identify four ports connecting the two sub-circuits together. These ports are the base-emitter and the collector-emitter ports of the two transistors. Now, to nullify the ports we add the following sources to the ports: V_{B1}, I_1, I_S, V_{E2}, V_{C2}, and I_2 as demonstrated in Fig. 5b. To comply with Algorithm 1, we also need to remove the supply sources (V_{CC} and I_S) from N_1. The idea is that, if these voltage and current sources can take care of the biasing of the transistors then there is no need to have any extra supply in the circuit. The main point here is that, now are able to assign our desired set of biasing conditions through these six sources instead of relying on the circuit supplies (V_{CC} and I_S) and the associated DCPC components.

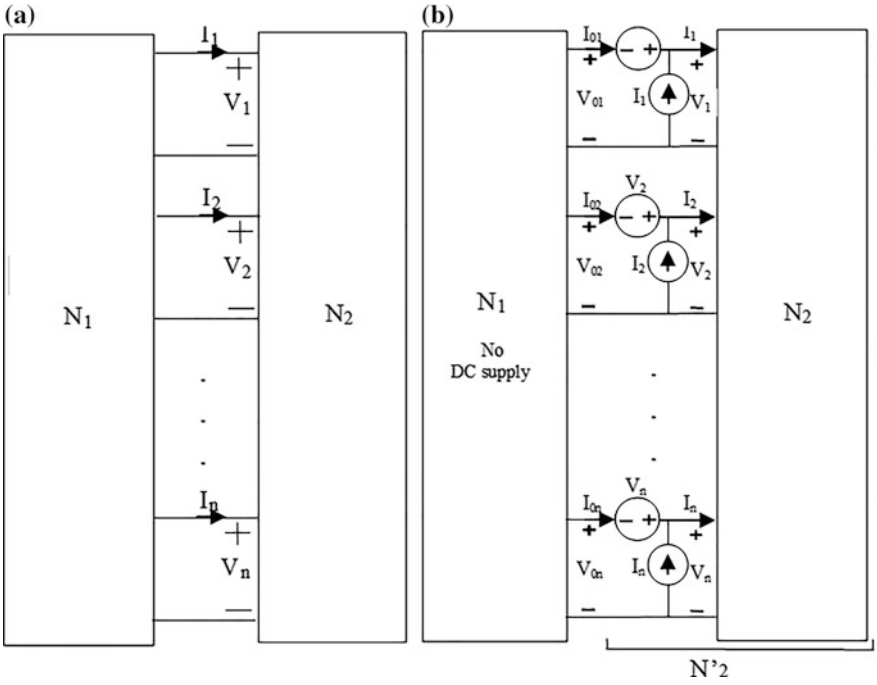

Fig. 4 Multi-port nullification; **a** Partitioned circuit, N_1: the linear and power supplier, and N_2: devices to be nullified; **b** N'_1 and N'_2 nullified (Power removed from N'_1)

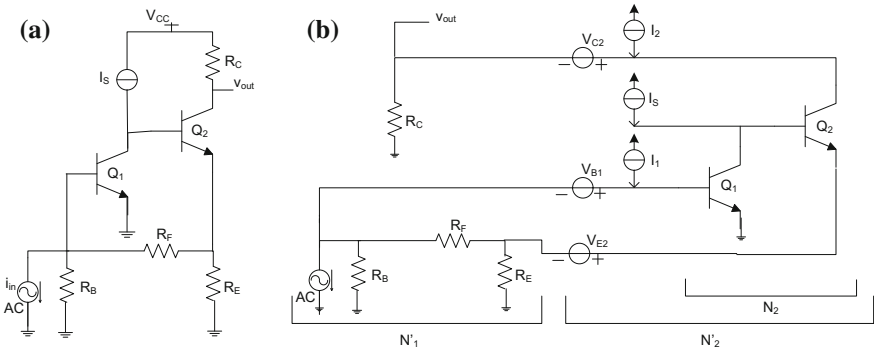

Fig. 5 Circuits for Example 2. **a** A two stage BJT amplifier with feedback; **b** Partitioned circuit into N'_1: the power supplies removed, and N'_2: nullified devices

In order to simulate the circuit we need to find the right values for the sources V_{B1}, I_1, I_S, V_{E2}, V_{C2}, and I_2 by assume our desirable (biasing) values to the transistors. Here are the biasing values: $V_{BE1} = 0.6$ V, $V_{CE1} = 2$ V, $V_{BE2} = 0.7$ V, $V_{CE2} = 4$ V, $I_{B1} = 10$ μA, $I_{C1} = 1$ mA, $I_{B2} = 100$ μA, and $I_{C2} = 10$ mA.

These are the biasing design specs, and based on these values we need to calculate the sources specified in Fig. 5b. From the circuits in Fig. 5 we get:

$$V_{B1} = V_{BE1} = 0.6\,\text{V}$$
$$I_1 = I_{B1} = 10\ \mu\text{A}$$
$$I_S = I_{C1} + I_{B2} = 1.1\,\text{mA}$$
$$V_{E2} = V_{CE1} - V_{BE2} = 1.3\,\text{V}$$
$$V_{C2} = V_{CE2} + I_{E2} = 5.3\,\text{V}$$
$$I_2 = I_{C2} = 10\,\text{mA}$$

Now the circuit in Fig. 5b is prepared for biasing. The following list is part of the WinSpice code used for the simulation, and Fig. 6 shows the transient response of the amplifier with local biasing in place.

```
.control
destroy all
tran 1u 400u 200u
plot v(9)
.endc
•  Circuit code
i1          0       2       DC      0       sin(0 27.5u 10k 0 0 0)
vb1         6       2       DC      6.463970e-01
vc1         3       7       DC      2
vb2         8       7       DC      7.059513e-01
vc2         4       9       DC      4
ib1         0       6       DC      10u
ic1         0       3       DC      1m
ib2         5       8       DC      100u
ic2         5       4       DC      10m
Q1          3       6       0       BJT1
Q2          4       8       5       BJT1
r1          2       0       100k
r2          2       5       40k
r3          5       0       200
r4          0       9       550
.MODEL BJT1 NPN
+ (is=14f  bf=100 . . . )
.end
```

Several points can be observed here:

1. From the WinSpice listing we notice that, although we have eight port variables V_{B1}, I_{B1}, V_{C1}, I_{C1}, V_{B2}, I_{B2}, V_{C2}, and I_{C2} but practically we are limited to four, which are I_{B1}, V_{C1}, I_{B2}, and V_{C2}, and the rest are computed by the devices models. We will pick up on this, and the reason for that in a later section.
2. Notice that the output plot does not show any DC component attached to it. This indicates that there is no need to insulate DC from AC signals through coupling capacitors, or by any other means. This is also true for the input signal that again doesn't need any coupling capacitor to operate. This is a major property of nullification (and later local biasing) that the DC signal is well contained within the devices itself, because they are externally nullified, and DC *blocked*.

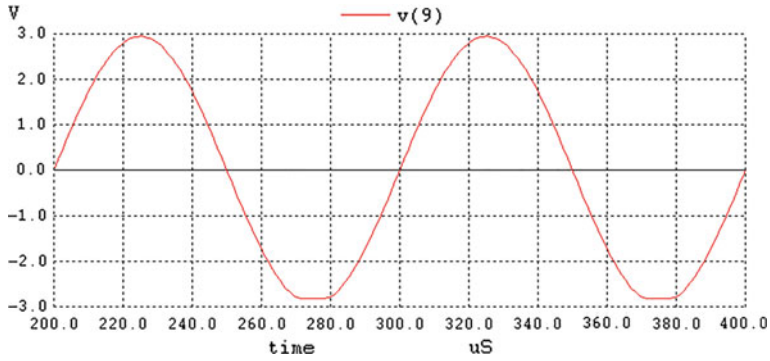

Fig. 6 Transient response of the amplifier with the devices being nullified

v–i characteristic curve: Our next investigation is to see how port nullification is mapped into the port's characteristic curve. In a circuit, the v–i characteristic curve of a port shows the relationship between its voltage and current variables as they change. Given the v–i characteristic of a port j(v_j, i_j), the port nullification moves the coordinates to the port's operating point Q(v_j, i_j), as a new origin. For example, Fig. 7a shows an nMOS transistor unbiased; hence, the Q-point of the output port is at the origin. This is because $V_{DS} = 0$ and $I_D = 0$, as plotted in Fig. 7b. Now, if we bias the transistor by a current source I_j the operating point moves to Q(V_j, I_j) on the characteristic curve, exhibiting a voltage of $V_{DS} = V_j$. Now by adding a voltage source V_j to the port we actually nullify the port as shown in Fig. 7c. This means the new port coordinate axis (v_k and i_k) have moved to the Q-point In this case a null port k(v_k, i_k) is created and the origin of the coordinate axis is simply the port Q-point. This is shown in Fig. 7d. In conclusion, by adding a power source, in this case I_j, to the port we bias the port to a Q(V_j, J_j) point, and then by adding a voltage source V_j to the port we nullify the port and move the origin of the new axis to the Q point. This simply means that by port nullification we have been able to move into the linear region of the device characteristic curve (as indicated in Fig. 7d) without any need to externally bias the device. This leads us to Property 1.

Property 1 Augment a port j(v_j, i_j) with a current source I_j and a voltage source V_j so that it operates at a Q(V_j, I_j) point on the port characteristic curve (Fig. 7c). The port is then nullified and the v–i coordinate axis move to Q, as the new origin, shown in Fig. 7d.

A circuit or device is *nullified* if all its ports are nullified. By a *device* we typically mean a nonlinear component such as a diode, a BJT or an MOS transistor.

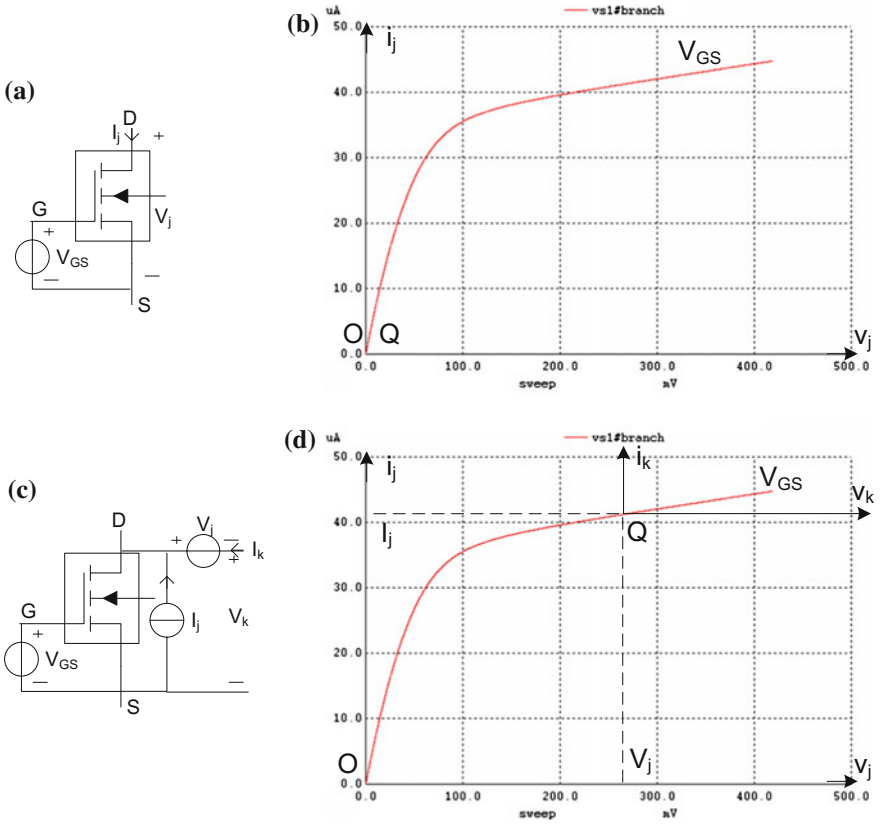

Fig. 7 nMOS output characteristic curves; **a** unbiased device with the Q-point at the origin; **b** locally biased device with a new Q point, still at the origin

3 Local Biasing

A port is locally biased if it is nullified. A circuit or a device is locally biased if it is nullified, i.e., all its ports are nullified. Note that local biasing of a circuit or a device is not unique. A port can be locally biased for any operating point (OP). This is also true for a device with multiple ports.

3.1 Local Biasing of Devices

To locally bias a device in a circuit all ports in the device must be nullified and remain nullified during the circuit operation. By giving the ports specifications in a device we can always nullify each port by adding a pair of voltage and current

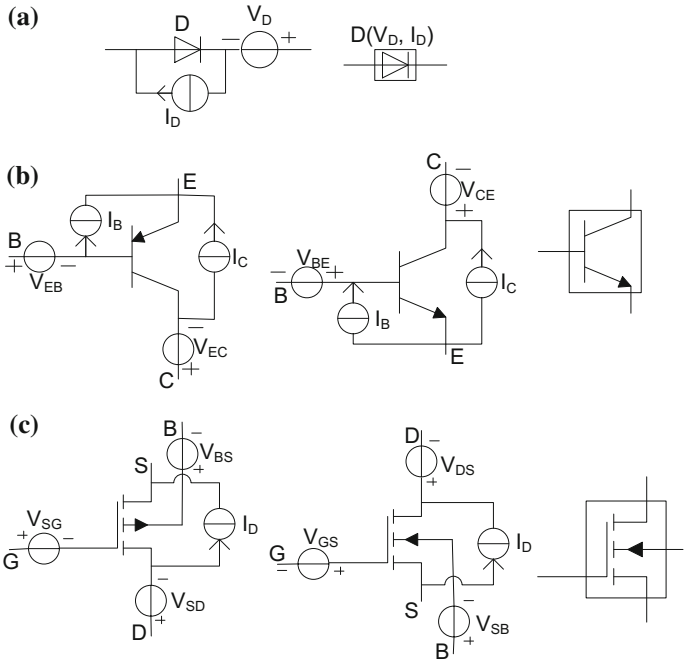

Fig. 8 Schematic representation of locally biased devices: diodes, BJT transistors, and MOS transistors, along with their symbolic representations

sources to each port, as described earlier. The schematic representation of locally biased diodes, BJT transistors, and MOS transistors, along with their symbolic representations, are given in Fig. 8. Note that in Fig. 8c the current sources are absent in gate and substrate ports for the MOS transistor. This is because these ports do not carry any DC current.

3.2 Properties of Local Biasing

There are certain properties of local biasing that are important in circuit operations, and particularly in distinction between DC and AC behavior of circuits. The followings describe some of these properties.

Theorem 1 Connecting locally biased devices together, directly or through a resistor network, does not make any changes in the devices operations, and it still makes the combined circuit locally biased.

Proof The proof is simple. Since the ports voltages and currents in any locally biased are zero connecting ports together makes no changes in them. In fact, there is no way for the devices to exchange (DC) power between them through the nullified ports.

As an example consider the circuit in Fig. 9. If the transistors are locally biased then the entire circuit is locally biased. That is, the DC current going through its nodes, 1, 2, 3, and 4, are all zero, and the DC voltage across any two nodes is also zero. In fact a generalized version of this property is given in Fig. 4.

Based on Theorem 1 we can state the following: virtually, if the transistors used in a design are each locally biased to the right operating point (see Fig. 7c and d) then the transistors can be used as ordinary circuit components, like resistors, without biasing, and still operate in the linear region for AC. Hence, a major application of Theorem 1 is in circuit design for performance (AC design). Once we configure the circuit, such as the one in Fig. 9, and locally bias the transistors, then we can change the resistors and even change the biasing of the devices (as long as they remain locally biased) in order to meet the AC design criteria. In other words, the biasing of a circuit is done as long as its transistors remain locally biased and any component variation aiming at the AC design does not change the biasing behavior. In mathematical terms we may state that, local biasing and designing for AC operation are orthogonal.

Property 2 If all devices within a circuit are locally biased then there is no need to have any DC supply in the rest of the circuit. In addition, any port of a circuit with no DC supply is nullified.

Property 3 The biasing strategy, whether it is *local* or *global,* does not affect the AC analysis of a circuit.

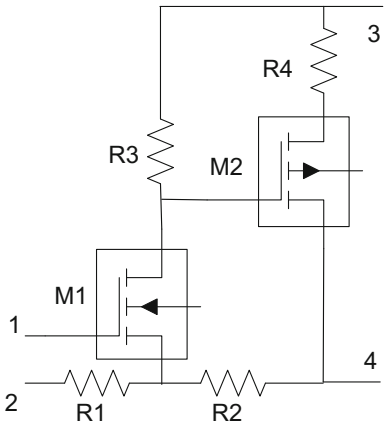

Fig. 9 Symbolic representation of a locally biased circuit

Property 3 is true because the DC supplies are all removed during the AC analysis; hence, there is no difference between the circuits being locally or globally biased. During the AC analysis we only need to have the operating points of the devices specified to get their small signal models.

Property 4 In a circuit that its transistors are locally biased, the DC power is contained within the locally biased components. Hence, by tapping to any node, which is not inside a locally biased transistor, we can directly input or output an AC signal without using a coupling capacitor.

Property 5 The power consumption within a circuit that its devices are locally biased is minimized.

Property 5 is true because in a circuit that its transistors are locally biased the DC power in contained within the locally biased components, and no were else, i.e., the rest of the circuit spend zero DC power.

4 Local Biasing Devices With Reduced Number of Supplies

With all the advantages and properties described for local biasing there are two major problems with it. First of all, there are too many local sources present in the circuit, i.e., a pair of voltage and current supplies for each port. Besides, these supply sources are spread within the circuit, and mostly not grounded. On the other hand, as we did find out, from two sources for each port only one carries power and the other one is just holding to the port voltage or current to nullify it. The second problem is that, a port, like a two-terminal component, needs only one of its variables (voltage or current) to be specified and the other one is obtained through the circuit analysis. Therefore, assigning both variables to a port may simply cause deviation from the port nullification, and hence the local biasing invalidates. So, the solution is to assign only one variable to each port and let the circuit provide the other port variable.

This makes us to propose a new local biasing scheme that addresses both problems, and provides a solution. In this scheme, one source is specified for each port and the other source is replaced with a reactive element. The reactive component is a capacitor in case a voltage source needs to be replaced, and it is an inductor in case a current source is aimed to be replaces. This is called *Local Biasing with Reduced number of Supplies* (LBRS) versus the previous scheme called *Local Biasing with full Supplies* (LBFS). Figure 10 shows LBRS applied to diodes, BJTs, and MOS transistors. Notice that Fig. 10 is identical to Fig. 8, except in Fig. 10 each port has one powered (voltage or current) source and the other

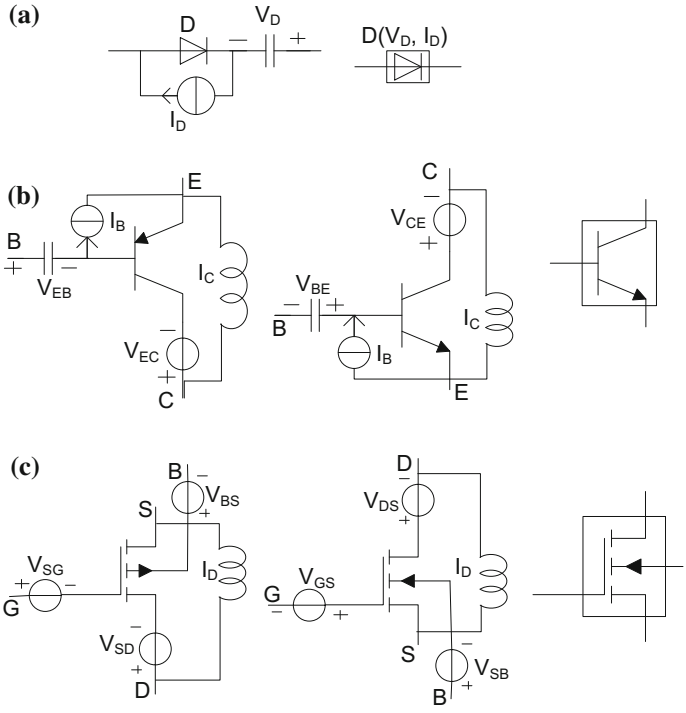

Fig. 10 Schematic representation of locally biased devices with reduced number of supplies: **a** diodes, **b** BJT transistors, and **c** MOS transistors, along with their symbolic representations

source is replaced with a reactive element, which is a capacitor replacing the port voltage source, and an inductor replacing the port current source. Initially, we may think of replacing voltage and current sources with capacitors and inductors may still complicate the locally biased circuits because of too many reactive elements. Although this may be true, but we should realize that with the capacitors and inductors added to the circuit for LBRS the circuit becomes totally DC free, when outside of the locally biased transistors. This, according to Property 4, allows us to directly tap into any node in the circuit to input a signal or receive an output signal without using any coupling capacitor that is commonly used in typical cases.

Example 3 Let us revisit the BJT amplifier discussed in Example 2, Fig. 5a. The transistors are locally biased using the LBRS technique in this example, as shown in Fig. 11. The reduced WinSpice code is also given below.

```
.control
destroy all
*tran 1u 400u 200u
print v(2) v(5) v(9) v(7)
print v(6) v(3) v(8)-v(5) v(4)-v(5)
*plot v(9)
.endc
•    Circuit code
i1   0    2    DC    0    sin(0 20u 10k 0 0 0)
c1   6    2    1u
vc1  3    7    DC    2
c2   8    7    1u
vc2  4    9    DC    4
ib1  0    6    DC    10u
l1   7    0    10m
ib2  5    8    DC    100u
l2   5    9    10m
Q1   3    6    0     BJT1
Q2   4    8    5     BJT1
r1   2    0    100k
r2   2    5    40k
r3   5    0    200
r4   9    0    550
.MODEL BJT1 NPN
+ (is=14f  bf=100 . . . )
.end
```

After simulating the circuit we get the simulation results for biasing as follows.

$$\begin{aligned}
&\text{DC Operating Point} \quad \ldots 100\% \\
&V_{BE1} = 6.463970e-01 \text{ V} \\
&V_{CE1} = 2.000000e+00 \text{ V} \\
&V_{BE2} = 7.059513e-01 \text{ V} \\
&V_{CE2} = 4.000000e+00 \text{ V}
\end{aligned}$$

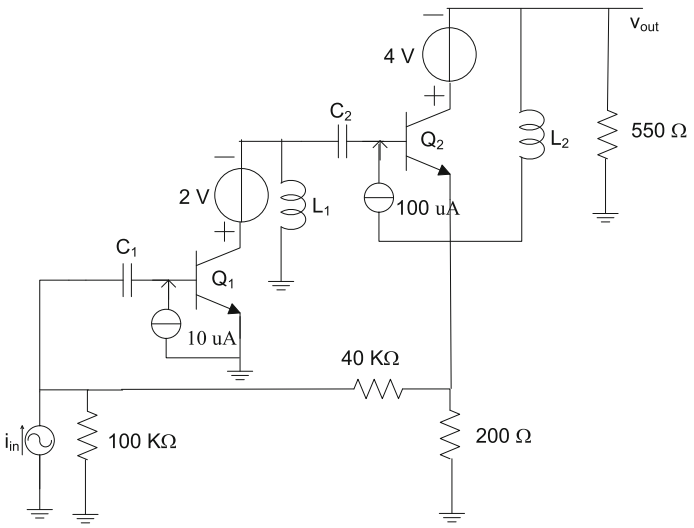

Fig. 11 Circuit for Example 3. Locally biased devices with reduced number of supplies, using capacitors and inductors instead

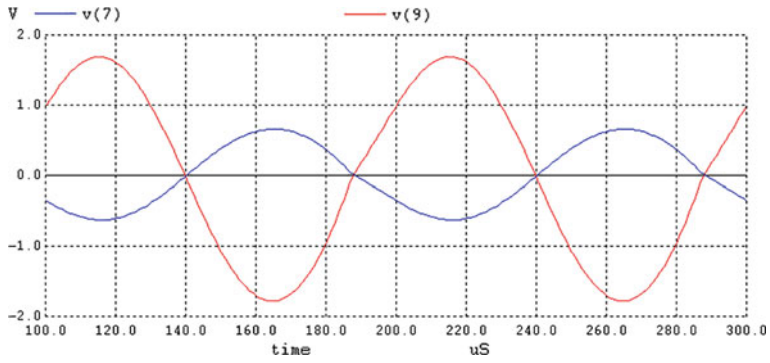

Fig. 12 Transient response of the locally biased amplifier

Notice that although we have provided only the biasing currents, the biasing voltages $V_{CE1} = 2$ V and, $V_{CE2} = 4$ V, are computed through the simulation.

Next, we simulate the amplifier for the transient analysis, and the output results from stages 1 and 2 are plotted in Fig. 12. Note that although the amplifier does not uses any coupling capacitors except for those in the local biasing, the input signal and the output responses are purely AC.

Finally, we can compute the DC power consumption P_{LBRS} of the amplifier by adding the powers spent in the local biasing of the two transistors as:

$$P_{LBRS} \cong V_{CE1}I_{C1} + V_{CE2}I_{C2} = 2*1 + 4*10 = 42\,\text{mW}$$

Compare this with the DC power P_{NB} spent in normal biasing situation, which is:

$$P_{NB} \cong V_{CC}(I_R + I_{C1} + I_{B2} + I_{C2}) = 9*(0.03 + 1 + 0.1 + 10) = 100\,\text{mW}$$

Therefore, the power saving is more than double. This concludes the example.

4.1 DC Nullator Representation of Devices

As we discussions before, if a device is "perfectly" locally biased then the device ports are nullified. However, these ports may not stay null if some DC sources are added to the circuit containing the devices, such as external power supplies. So, we can call these ports *slashed-nullators,* and symbolize them as shown in Fig. 13c. A slashed-nullator becomes a nullator only when a perfect locally biased is guaranteed. Figure 13 displays a combination of Figs. 8 and 10 equivalent locally biased devices in two types, full supplies and reduced supplies. In addition the devices can also be symbolized by one or more slashed-nullators, as shown in

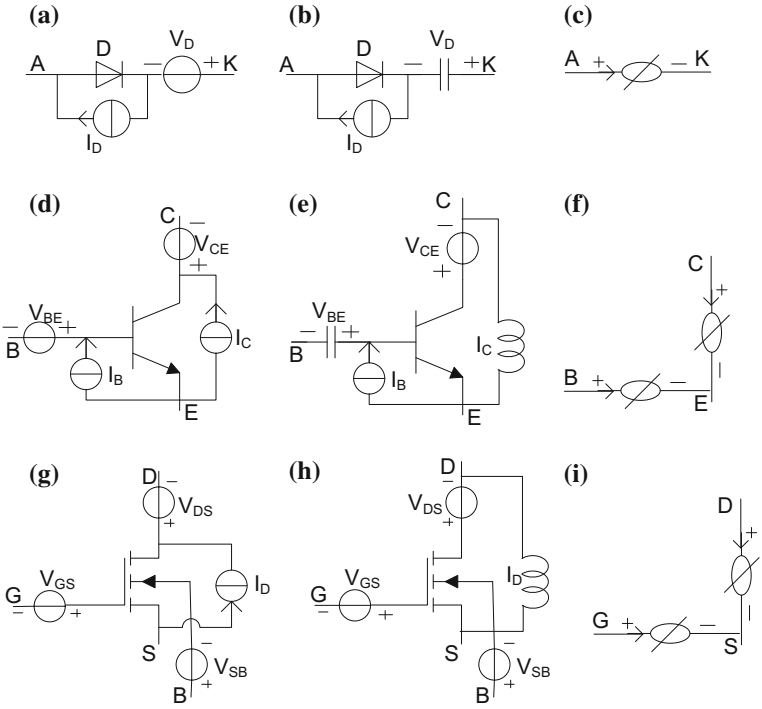

Fig. 13 Locally biased, and locally biased with reduced number of supplies for diodes, BJT and MOS transistors; their representations by slashed-nullators

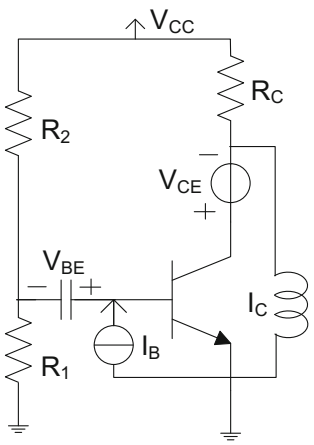

Fig. 14 A locally biased common emitter amplifier, with reduced number of supplies

Fig. 13c, f, and i. As an example for a slashed-nullator, consider Fig. 14, which shows a CE amplifier with the BJT being locally biased. The transistor can be represented by two slashed-nullators displayed in Fig. 13f. These slashed-nullators can become nullators only if the external supply V_{CC} is removed from the circuit, in which case the BJT is perfectly biased, locally. In what follows, we assume perfect local biasing unless stated otherwise.

5 Fixator-Norator Pairs in Biasing Designs

We discussed local biasing and its properties in Sects. 3 and 4. The main property of local biasing is its ability to totally remove global biasing in circuits by biasing individual devices, instead. The advantage was a "divide and concur" strategy that makes biasing device-independent and simple. The down side of this strategy, however, is having too many DC (voltage and current) supplies in the circuit, plus the fact that these supplies are distributed within the circuit and without being necessarily grounded. In Sect. 4 we proposed a technique that uses reactive elements, such as capacitors and inductors, to cut the number of supplies into half, but still not only the number of supplies are large for large circuits, many supplies remain ungrounded. As it turns out, one solution to both problems is to use Fixator Norator Pairs (FNP) as we will discuss it here.

5.1 Fixator

A fixator is very similar to a nullator, except a fixator represents a fixed current source as well as a fixed voltage source. In fact, a nullator can be considered a special case of a fixator, where both its current and voltage sources are zero. Figure 15 shows two versions of a fixator depending on whether (1) the voltage source V_j consumes (or provides) power in the fixator and the current source I_j stays idle, or (2) the other way around. In Fig. 15a the voltage source consumes power, and Fig. 15b is its symbolic representation. In Fig. 15c the power consuming source is left out, and $F_x(0, I_j)$ is a *current fixator*. Figure 15d, e, and f are similar to a, b, and c, except here the current source consumes power, and $F_x(V_j, 0)$ represents a *voltage fixator*.

In a circuit, a fixator must always be paired with a norator, where, the fixator sets both port variables according to a design spec, and the paring norator provides the require conditions for the fixator to operate.

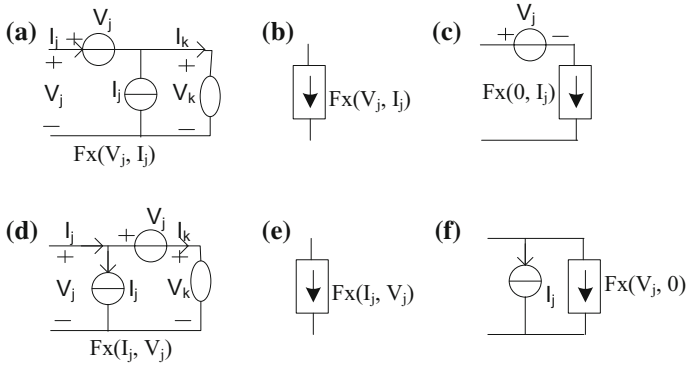

Fig. 15 Fixators; **a** and **b** voltage powered fixator and its symbol; **c** current fixator; **d** and **e** current powered fixator and its symbol; **f** voltage fixator

5.2 Rules Governing Fixators and Norators

A fixator represents a current source and a voltage source combined; hence, its rules must comply with both. For instance, a current source in series with a fixator may violate KCL, and a voltage source in parallel with a fixator may violate KVL. In general, a cutset of fixators with or without current sources may violate KCL and a loop of fixators with or without voltage sources may violate KVL.

A cutset of norators with or without current sources and fixators are not all independent, and a loop of norators with or without voltage sources and fixators are not all independent either.

Here are some other properties of the pair:

- A fixator Fx(V, I) consumes power, and the power consumed is P = V*I.
- A resistance R in series with a Fx(V, I) is absorbed by the fixator and the fixator becomes $Fx(V_1, I)$; where $V_1 = V + R*I$. A resistance R in parallel with a Fx (V, I) is absorbed by the fixator and the fixator becomes $Fx(V, I_1)$; where $I_1 = I + V/R$.
- A current source I_S in parallel with a fixator Fx(V, I) is absorbed by the fixator and the fixator becomes $Fx(V, I_1)$; where $I_1 = I + I_S$.
- A voltage source V_S in series with a fixator Fx(V, I) is absorbed by the fixator and the fixator becomes $Fx(V_1, I)$; where $V_1 = V + V_S$.
- A current source in series with a norator absorbs the norator with no change; and a voltage source in parallel with a norator absorbs the norator with no change. In addition, a current source in parallel with a norator is absorbed by the norator; and a voltage source in series with a norator is absorbed by the norator.
- A resistance in series or in parallel with a norator is absorbed by the norator.
- A norator in series with a fixator Fx(V, I) becomes a current source I; and a norator in parallel with a fixator Fx(V, I) becomes a voltage source V.

5.3 Fixators and Local Biasing

A major property of a fixator is that, when it is assigned to a circuit port it keeps its biasing (voltage and current) fixed. In a first glance we may think that local biasing does the same. It uses supplies internally to bias a transistor to a certain operating point and nullifying its ports. The difference, however, is that, local biasing does not guaranty to keep the biasing of a port fixed, it does it only when the ports remain null. What might happen is that, if after local biasing (and nullifying) a port we bring a new DC source to the circuit the biasing condition of the port may change and the port in no longer null. This is not the case in fixator. Fixators guarantee the biasing stay fixed. Fixators do not add any extra source to the circuit, but they make the existing sources in the circuit to provide the right conditions for the specified biasing. In other words, fixators only set the biasing requirements, and it is up to the remaining circuit to fulfill these requirements. Another major difference between local biasing and using fixators is that, with local biasing we can run the AC operation in a circuit, but not with the fixators attached. The fixators must be removed after their design job in done.

Just like local biasing models, diodes and transistors can also have fixator models, as shown in Fig. 16. The left column in the figure shows the devices that are normally biased, and the next two columns show the biasing being fixed (i changed to I and v changed to V). This indicates that there are two types of fixator models for each device. In the first type, shown in the middle column, the entire device is replaced with its model consisting of one or more fixators. In the second type, shown in the last column, the device remains intact but fixators are added to set specific variables in the device fixed. One may ask, why two types of models, and what are their differences? To explain this, we need to go back to the same discussion we did for local biasing. Here again, there are two fixed variables assigned to each port in the first type (the middle column), whereas only one is needed, and the other variable must be found through the circuit analysis. Therefore, providing fixed values for both port variables may cause deviation from the actual port characteristic, and subsequently from the device characteristic, as well. The advantage of using the first type, however, is its linearity and hence simplicity to analyze the circuit.

In the second type (the right column), the device remains in the circuit and typically one variable per port is only fixed. The other variable is found through the circuit analysis. This is definitely the most accurate model but the disadvantage is that the circuit remains nonlinear as its original. In our analysis, in this chapter, we more prefer to use the second type of models unless stated otherwise.

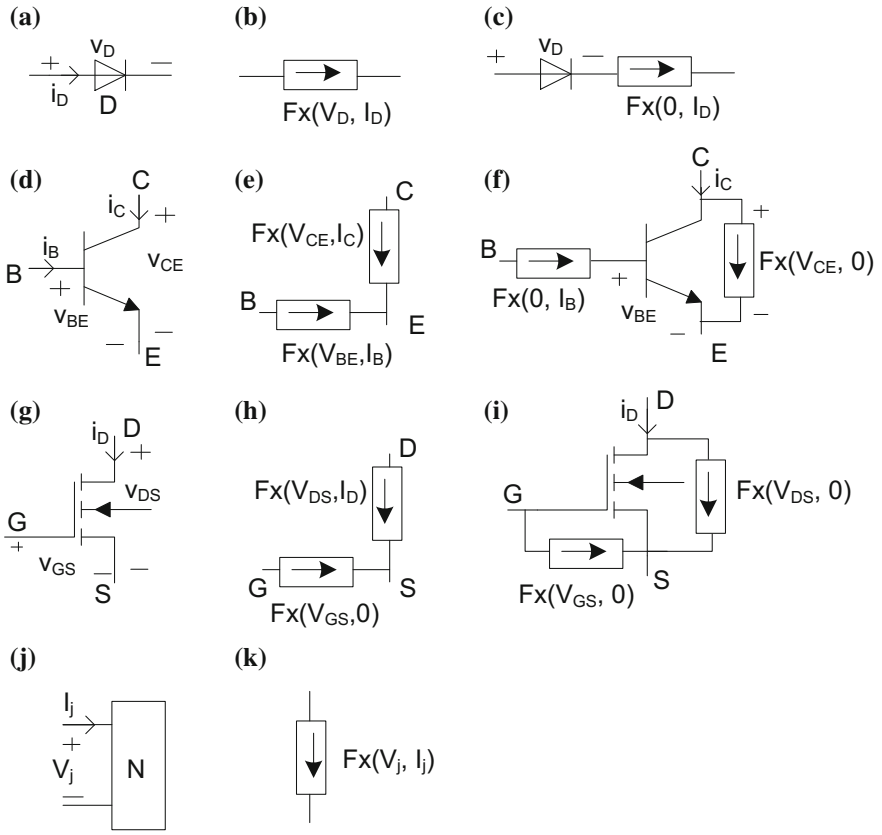

Fig. 16 Fixator modeling of the devices, diodes, BJT and MOS transistors, and a circuit port; **a**, **d**, and **g** normally (globally) biased devices; **b**, **e**, **h**, and **k** linear fixator models; **c**, **f**, and **i** the actual fixator models with the device included

5.4 Fixators Norator Pairs (FNP)

Fixators cannot stay alone in a circuit. This is because they have two variables (voltage and current) specified, and this violates Kirchhoff Laws. Norators, with no specified port variables, on the other hand can pair with fixators in a circuit. However, a fixator can pair with a norator only if they are mutually sensitive to each other. Actually a norator must be highly (theoretically infinitely) dependent on the pairing fixator, and a fixator must also be sensitive to the changes taking place in its pairing norator. The next question is, how the pairing takes place in a circuit that has multiple number of fixators and norators? The correct answer is that, it happens "collectively". Contrary to dependent sources that the controlling and controlled components always appear in pairs, in FNPs no paring is necessary, as long as the number of fixators and norators are equal. A full discussion on this is given in [19].

There is one exception, however, which is, when we use a typical circuit simulator like SPICE we need to replace each FNP with a controlled source. Therefore, because of the nature of controlled sources we are forced to pair the fixators and norators when dealing with conventional simulators.

We are now ready to put all this into an algorithm.

Algorithm 2

1. Given a circuit configuration (topology) with a certain number of biasing requirements, we start locally biasing the circuit. This biasing makes each device being biased separately, and based on its own biasing criteria. We then remove all other DC supplies from the circuit.
2. After the local biasing is completed and tested we introduce fixators to keep the biasing fixed. To do this, we need to replace the locally biased transistors (Fig. 8 or 10) with the fixator models that are given in Fig. 16. As mentioned earlier, there are two types of fixator models for each device, linear and non-linear. Here we need to choose the one that is more appropriate for our design case.
3. Next we need to allocate one norator for each fixator in the circuit. Each norator will be then replaced with either a DC (voltage or current) source or just as DC Power Conduction components (DCPCs), which is typically a resistor, or a transistor in ICs.
4. We then need to add DC supplies to the circuit, or alternatively one or more of the norators can be assigned to provide power to the circuit.
5. All circuit components and devices are in place for simulation now except for the fixators and norators that are only pathological components and they must be replaced with controlled sources. The closest components to replace a pair (FNP) is a controlled source with a very high gain. Among these sources a VCVS or a VCCS is a candidate for a FNP with current fixator, and a CCVS or a CCCS is a candidates for a FNP with voltage fixators. Current and voltage fixators are displayed in Fig. 15.
6. We now simulate the circuit. Following the circuit simulation we get four choices for each norator to decide. In general a norator k, represented by V_k and I_k as its voltage and current, can be replaced with a voltage source V_k, a current source I_k, a (DCPC) resistor $R_k = V_k/I_k$, or a combination of them.
7. Finally, we replace the norators with their replacement components found, and then remove the fixators from the circuit. The biasing design is now completed.

Example 4 Let us revisit the BJT amplifier discussed in Example 2 one more time. Referring to Fig. 5a we would like to bias the transistors, Q_1 and Q_2, for $I_{B1} = 10$ μA, $V_{CE1} = 2$ V, $I_{B2} = 100$ μA, and $V_{CE2} = 4$ V. Next, to keep the biasing values fixed during the process we use fixators. And from two types of device modeling by fixators, discussed before, we select the second type shown in Fig. 16f. Now we need to select four paring norators. We choose the components R_E, R_F, I_S, and R_C to replace them with the norators we need, namely N_1, N_2, N_3, and N_4, respectively, as shown in Fig. 17.

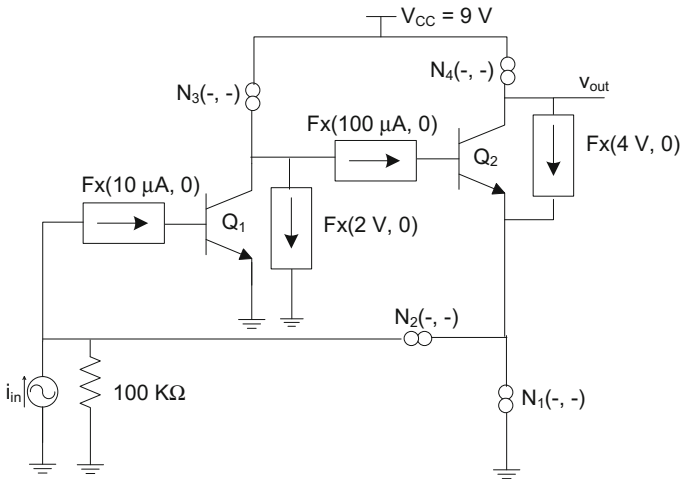

Fig. 17 Two stage BJT amplifier circuit with feedback using FNP for the biasing design

Now to simulate the circuit we need to pair each fixator with a norator in the circuit and then assign a controlled source to each FNP. Although this step can almost be arbitrary, but with a little effort we can find pairs of fixators and norators that are quite sensitive to each other. The following list shows the four FNPs that are paired and replaced with the controlled sources specified.

- N_1(-, -) and Fx(10 μA, 0) as a VCVS with the gain of 10^3.
- N_2(-, -) and Fx(2 V, 0) as a CCVS with the gain of 10^7.
- N_3(-, -) and Fx(100 μA, 0) as a VCCS with the gain of 10^3.
- N_4(-, -) and Fx(4 V, 0) as a CCVS with the gain of 10^7.

And the SPICE coding for the FNPs are given below:

```
e1  2  0  2  11  1.0e03
h2  5  2  V2 1.0e07
g3  1  3  3  12  1.0e03
h4  1  4  V4 1.0e07
```

Here is how we can describe each fixator: (1) the fixator Fx(10 μA, 0) is represented by a 10 μA current source from node 2−11, and (2) the fixator Fx(2 V, 0) is represented by a 2 V voltage source V2. Similar situation holds for the other two fixators Fx(100 μA, 0) and Fx(4 V, 0).

Next, we simulate the circuit so constructed and find the component values replacing the norators. The followings are the results after the circuit is simulated.

$$
\begin{aligned}
&\text{DC Operating Point } \ldots 100\% \\
&V_{BE1} = 6.463985e-01\ \text{V} \\
&V_{CE1} = 2.000009\ \text{V} \\
&V_{BE2} = 7.059356e-01\ \text{V} \\
&V_{CE2} = 3.999971\ \text{V} \qquad . \\
&N_1 = 1.284133e+02\ \Omega \\
&N_2 = 3.999971\ \Omega \\
&N_3 = 1.100027e-03\ \text{A} \\
&N_4 = 3.708204e+02\ \Omega
\end{aligned}
$$

Note that N_1, N_2, and N_4 are (DCPC) resistors, but N_3 is a current supplier. Note also that the values obtained are quite close to the original values given in Examples 2 and 3.

Finally, to finish off the biasing situation and prepare the amplifier for transient analysis, we need to do the followings: (1) replace the norators with the components found, (2) remove the fixator from the circuit and apply the input signal i_{in}, and (3) run the circuit for the transient analysis. The response is shown to be very close to what we see in Fig. 6. This concludes our example.

Example 5 Here, we are interested to design the biasing of a two stage MOS amplifier with feedback, shown in Fig. 18. The schematic provides the topology of the amplifier with the component values specified. Table 1 shows the transistors sizes along with their Operating Points (OPs), where the substrate effect is ignored for simplicity. As one of the criterions, to have the output waveform distortion free we have selected to have $V_{SD2} = 4$ V. This provide us with a maximum of 6 V output voltage swing.

Next, we locally bias the transistors. Figure 19 shows the schematic diagram of the amplifier when the transistors are locally biased, using the reduced supply scheme, i.e., instead of adding current supplies, I_{D1} and I_{D2}, for the drain currents we have used two inductors L_1 and L_2, in order to keep the ports nullified. In fact this scheme proves to be more effective than the one with complete sources (Fig. 8). This is because, it not only guaranties the nullity of the ports (a requirement for local biasing) but it also help us to find the actual current values needed for I_{D1} and I_{D2}. These values are found to be $I_{D1} = 7.151974e\text{-}05$ A and $I_{D2} = 7.997803e\text{-}04$ A, which are very close to the assigned values in Table 1. In case the differences between the spec values and the calculations exceed the tolerance we can either settle with the calculated values or make changes to get closer, for example, change V_{GS}.

After the transistors are locally biased we simulate the circuit for AC and transient analysis. It is at this stage that we can choose values for the circuit resistors and adjust them to meet the performance design criteria. These performance design criteria may include the gain, and input and output impedances. Because we are only doing biasing design here we assume the performance design is already carried

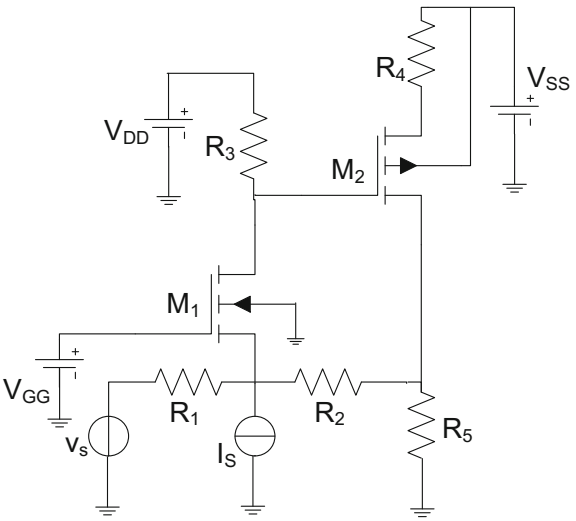

Fig. 18 Initial configuration of a CMOS amplifier with feedback

Table 1 Biasing design with specified values

Devices	W/L μm	V_{GS} V	V_{DS} V	I_D μA
M_1	20/1	1.0	1.9	70
M_2	50/1	−1.8	−4.0	800

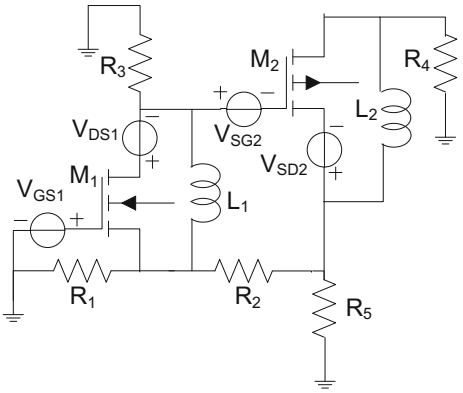

Fig. 19 Locally biased (reduced supplies) for the CMOS amplifier

Table 2 Component values for Example 5

R_1 KΩ	R_2 KΩ	R_3 KΩ	R_4 KΩ	R_5 KΩ
46.5	15	85	5.4	0.85

out and the circuit resistors are found, and Table 2 provides these resistor values for the amplifier. So, the only components left to be determined are the four power supplies, V_{GG}, V_{DD}, V_{SS}, and I_S.

Given the selected OPs, our next move is to replace the transistors with their fixator models. This stage of the design is needed to move from the local biasing to global (normal) biasing, and determine the values for the power supplies. We use the linear fixator model in this example, displayed in Fig. 16h. The MOS transistors are now totally replaced with their fixator models. Next, the fixators need to be paired with four norators, and these norators occupy the supplies, V_{GG}, V_{DD}, V_{SS}, and I_S, locations, as seen in Fig. 20. Our circuit is now ready for simulation. Notice that the entire circuit is linear.

Another important point to mention here is that, we are trying to keep the resistors unchanged in order not to disturb the performance design, and that is why we are focusing more on assigning the computed power supplies. However, this may not always work. The reason is that in most design cases the power supplies are standardized and need to stay at values such as 5, 3.3, 1.8, 1.0 V, whereas in finding the values through computation may send us way off. We can think of two solutions for this. Either use voltage dividers/references to adjust the values, or adjust the power conducting resistors in the circuit. Although the second solution is less complicated and more power friendly but the resistors obtained for DC biasing may be way different from those found in the performance design. In lumped analog circuits, these differences are typically solves by using bypass capacitors. For example, in a CS (common source) amplifier design with a source resistance, portion of the resistor is normally bypassed to boost the gain. In case of the integrated circuit the difference between (DC) static and (AC) dynamic resistors are typically solved by using dynamic loadings using active components.

We are now ready to solve the linear circuit with FNPs. Again, we use high gain dependent sources, very similar to what we used in Example 4. Note that the use of high-gain dependent sources are just temporary and do not appear in the actually

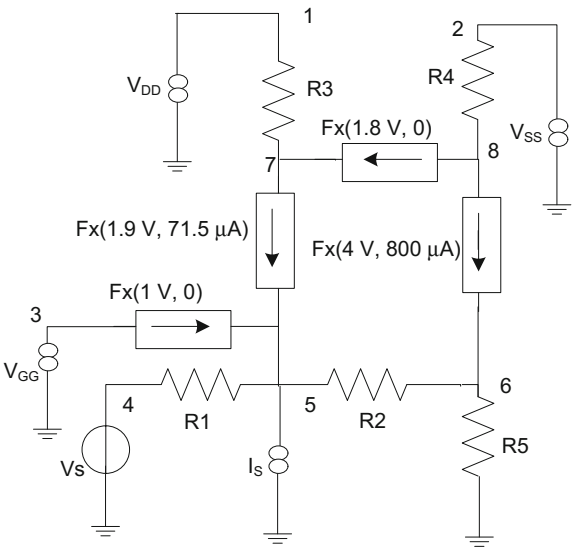

Fig. 20 The linear DC modeling of the CMOS amplifie using the fixator-norator modeling concept

designed circuit. The following is a partial SPICE code for this simulation. Notice that the fixator model used in this simulation code is the nonlinear mode type, shown in Fig. 16i. The difference is that, instead of using $I_{D1} = 7.151974e\text{-}05$ A and $I_{D2} = 7.997803e\text{-}04$ A found earlier in local biasing case, we are using the actual transistors M_1 and M_2 to carry the currents. The results show the same values.

```
 M1   4    2    5     5    N_1u   L=1u   W=20u
M2    7    4    6     6    P_1u   L=1u   W=50u
r1    5    0    46.47k
r2    7    5    15k
r3    4    1    85.3k
r4    6    3    5.376k
r5    7    0    854
*
vg1   2    5    DC    1.0
vd1   4    5    DC    1.9
vg2   6    4    DC    1.8
vd2   6    7    DC    4
hg    2    0    vd1   1.0e8
fs    5    0    vg1   1.0e5
hd    1    0    vg2   1.0e8
hs    3    0    vd2   1.0e8
```

After the norators' voltages and currents are found it is then up to us to play with these values, which previously we categorized them into four types: voltage sources, current sources, resistors (voltage/current), or a combination of the three. Our selection in this example is clear as calculated by Spice and shown below:

$$V_{GG} = 2.000169\,\text{V}$$
$$V_{DD} = 8.994837\,\text{V}$$
$$V_{SS} = 9.000755\,\text{V}$$
$$I_S = 30.01714\,\mu\text{A}$$

To make it simpler and more practical, in reference to Fig. 18, we can combine V_{DD} and V_{SS} and assume $V_{DD} = 9$ V. Also we take $V_{GG} = 2$ V, and $I_S = 30$ μA. This concludes our example.

6 Fixator-Norator Pairs in VLSI Biasing Designs

In the following two examples the FNP methodology is applied to analog integrated circuits for biasing designs.

Example 6 This example presents a negative feedback amplifier; fully explained in reference [3]. Figure 21 shows a simplified schematic of the amplifier after it has gone through the performance design in the three areas: noise reduction, clipping/distortion reduction, and high loop-gain-poles-product.[2] To do the biasing design

[2]For details please refer to Chap. 10 in [3].

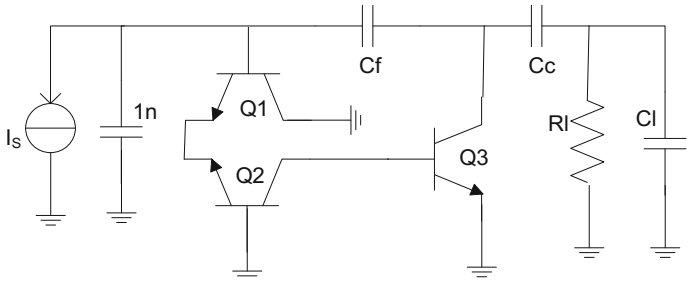

Fig. 21 A three stage amplifier topology after going through the performance AC design [3]

we need to first specify the values for the DC supplies and their locations in the circuit. Next, we need to select the operating points (OPs) for the transistors so that they can fulfill the design specs. For the actual power supplies, we choose two DC sources of 4 and −4 V, as selected in [3]. For evaluating the component values we need such as the power supplies and the DCPCs we go through FNP design procedure. According to the criteria given for the performance design the FNP procedure must address the following specs.

- The emitters of Q_1 and Q_2 must be driven by a high impedance current source, I_E.
- The base of Q_2 must be driven by a low impedance voltage source, V_{B2}.
- The collector of Q_1 can be driven directly by V_{CC}.
- The collector of both Q_2 and Q_3 must be driven by high impedance current sources I_{S2} and I_{S3}, to maximize the gain.
- The base current of Q_1 can be provided through a feedback resistor R_f.[3]

To proceed with the design we choose the collector-emitter voltages of the transistors Q_2 and Q_3 (v_{CE2} and v_{CE3}) to be the "critical" design criteria. Note that the voltage V_{CE1} of Q_1 is not critical because it is directly connected to V_{CC}. Next, we assume all the three collector currents i_{C1}, i_{C2}, and i_{C3} to be also "critical". Table 3, columns 1 and 2, provides all these five critical values for the transistors OPs, and it also gives all five fixators that keep the critical values unchanged during

Table 3 Bias design specs and fixator-norators

Critical specs	Fixator representations	Norator representations
$I_{C1} = 0.1$ mA	Fx(0, 0.1 mA)	RF
$V_{CE2} = 0.67$ V	Fx(0.67 V, 0)	VB2
$I_{C2} = 0.5$ mA	Fx(0, 0.5 mA)	IE
$V_{CE3} = 2.2$ V	Fx(2.2 V, 0)	IS3
$I_{C3} = 3.6$ mA	Fx(0, 3.6 mA)	IS2

[3]The resistance R_f is in the bias loop and part of a required AC filter.

the design process. Column 3, on the other hand, shows five pairing norators that are going to be replaced with appropriate circuit components, as specified in the table. Figure 22 is extracted from Fig. 21 after the FNPs, specified in Table 3, are added to the circuit.

Again, to simulate the circuit we need to replace the FNPs with high gain controlled sources. The following is a partial SPICE code showing five controlled sources used for the five FNPs.

```
ic1     2       a       DC      1.0e-04
e1      4       51      2       a       1.0e8
vce2    c       7       DC      0.67
hb2     Vb2     0       vce2    1.0e8
ic2     3       c       DC      0.5m
ge      7       11      3       c       1.0e8
vce3    e       0       DC      2.2
fc3     21      4       vce3    1.0e8
ic3     4       e       DC      3.6m
gc2     12      3       4       e       1.0e8
```

In Table 4, column 1 shows the type of controlled source used for each FNP, column 2 is the list of the controlling fixators, and column 3 shows the results obtained from the simulation, which are the ultimate components values for the design.

Finally, we remove the controlled sources (FNPs) from the circuit and replace each norator with its appropriate component listed in Table 4. The final amplifier so designed is depicted in Fig. 23. As expected, the resulted DC sourcing matches with those in [3], but here obtained much quicker.

Example 7 This example presents a two-stage CMOS Op-Amp [2]. The design uses low voltage 50 nm CMOS technology. Figure 24 provides a partial structure

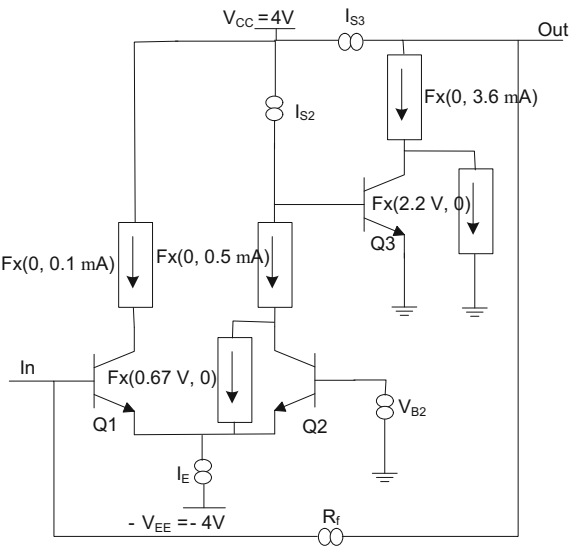

Fig. 22 The three stage amplifier with fixator-norator pairs indicating the biasing design specs

Table 4 Component values for the specified biasing

VCVC	FX(0, 0.1 mA)	RF = 1.53 MEGΩ
CCVS	FX(0.67 V, 0)	VB2 = 0.677 V
VCCS	FX(0, 0.5 mA)	IE = 0.607 mA
CCCS	FX(2.2 V, 0)	IS3 = 3.601 mA
VCCS	FX(0, 3.6 mA)	IS2 = 0.523 mA

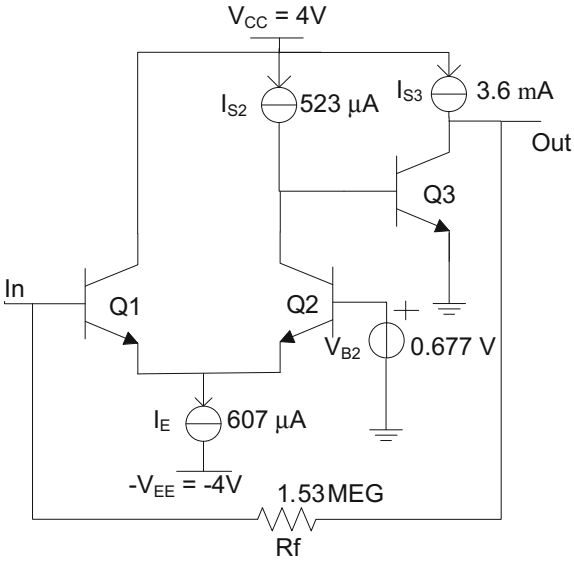

Fig. 23 The three stage amplifier with complete biasing

for the amplifier including the assigned FNPs. Below is the list of some design specs that are specified for this amplifier.

Output voltage swing	100–900 mV
Gain Stage current	10 µA
Differential Stage current	20 µA
Voltage Gain	60 dB
Drivers' W/L in 50 nm scale	M1: 50/2, M2: 50/2, M5: 100/2

For the biasing design purpose we particularly focus on the first two design criteria, i.e., to maximum the output swing, and get the current flow for the gain stage as specified. For the output voltage swing, we like to fix $V_{SD5} = 0.47$ V, and for the gain stage current flow we fix the current at $I_{D5} = 10$ µA. These assumptions translate into producing two fixators for the parameters. For the first one we assign Fx(0.47 V, 0) to the transistor M_2 to keep V_{SD5} constant at 0.47 V, and for the second criterion we assign Fx(0, 10 µA) to the drain of M_2 to keep I_{D5} constant at 10 µA, as shown in Fig. 24. Now, with the two design specs fixed we need to assign two norators to pair with the fixators. We have selected the two active loads/current mirrors, R_S and R_D to replace them with two norators. The two FNPs

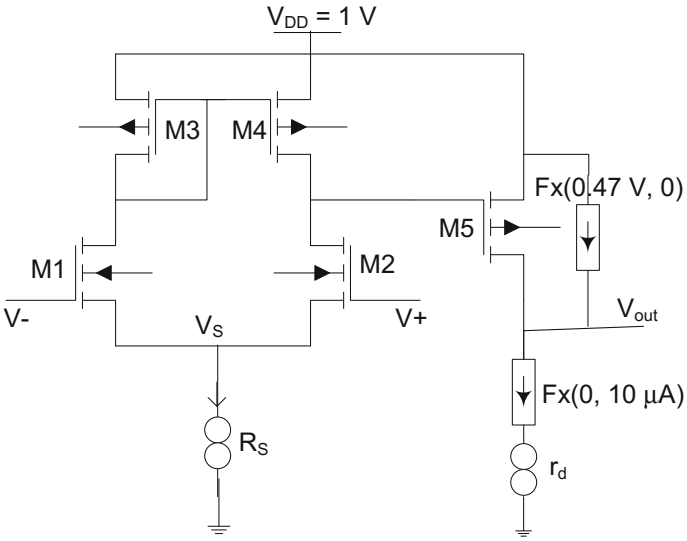

Fig. 24 Partial structure of a two-stage CMOS Op-Amp with fixator-norator pairs

Table 5 Parameter needed for DCPC designs

Amplifier stage	Component voltage V_j	Component current I_j	Dynamic resistance r_o	Static resistance R_o
Differential	122.8951 mV	18.99460 μA	41 KΩ	6.47 KΩ
Gain	530 mV	10.09308 μA	420 KΩ	53 KΩ

chosen for the biasing design are then (Fx(0, 10 μA), R_D) and (Fx(0.47 V, 0), R_S). For the first FNP there is no need to go through simulation. We can simply replace the norator R_D with the static load $R_D = (1-0.47)/10 = 53$ KΩ.

For the second FNP we do the followings. Here we aim at V_S, the source voltage for the differential stage. So with the fixator Fx(0.47 V, 0) we simply get $V_S = 0.123$ V for the pairing norator. And by having $I_S = 20$ μA we get the static load for the current mirror as $R_S = 6.47$ KΩ. This concludes our biasing design.

For the performance design, we need a dynamic load for the gain stage not less than $r_d = 420$ KΩ in order to get an overall gain of 60 dB for the amplifier. A similar procedure finds the dynamic resistance of the differential stage which is $r_s = 41$ KΩ, as listed in Table 5. Table 5 also provides other design criteria as well, including the static loads. Next, with the values found the circuit is simulated using WinSPICE and the DC simulation results are given as listed.

TEMP = 27 deg C
DC analysis… 100%%
vs = 1.228951e-01
v(5) = 4.695930e-01

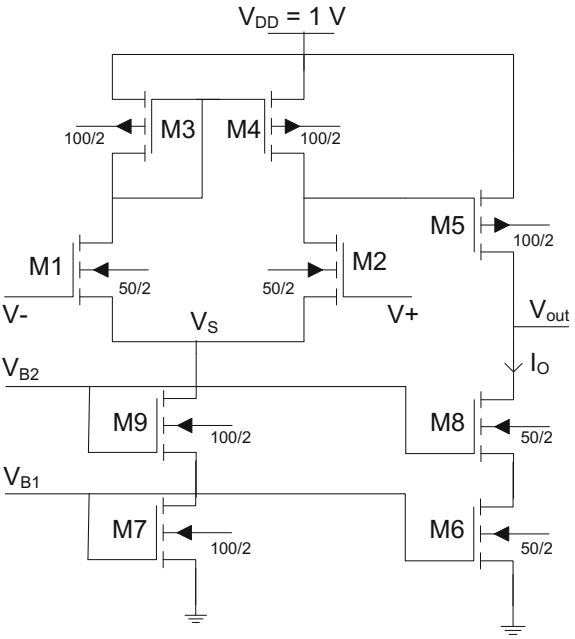

Fig. 25 Completed structure of a two-stage CMOS Op-Amp

vs1#branch = 1.899460e-05
vs2#branch = 1.009308e-05
WinSpice 3 ->

To complete the biasing design, the last step in here is to design the current mirrors/loads for both stages. Table 5 provides the parameter values needed for the designs of two DCPCs. The component needed for the differential pair is going to be a low voltage and low resistance component. A simple experiment reveals that one or more MOS transistors in the triode region will fulfill this requirement. For the Gain stage, the dynamic resistance must be high for the high gain and a cascode MOS current source structure is what is needed. This finalizes the design of the Op-Amp with the transistor sizing also given in Fig. 25.

7 Conclusion

The chapter is presented as a tutorial for biasing analog circuits using fixator-norator pairs. It starts introducing port nullification, which is an essential step in local biasing of the devices. This nullification is extended to nonlinear device nullification, which then leads us to actual local biasing of the devices. This step is important because it DC insulates the devices and bias them based on their design specs. It is shown how a device can be internally powered with no need to external power supplies. There

are, however, some draw backs in local biasing strategy. The problem is with its practicality, requiring numerous supply sources and in disarrays. The solution presented in this chapter is performing biasing through the use of FNPs. By using FNP we are able to fix each transistor to its designated operating point, just like any local biasing, while the power supplies remain in their original location in the circuit, called global biasing. Properties on fixators and norators are discussed and FNP-based modeling are introduced for nonlinear devices, diodes, BJTs, and MOS transistors. These models are of two types, linear and nonlinear. The linear models are trying to fix all the device parameters for certain specified operating points, whereas, the nonlinear models adopt themselves to the type of the devices. Apparently linear models are not well suited for the cases that the devices characteristics are varying from time to time. However, this is the price we need to pay for the linearity and simplicity we get. There are numerous examples that start from simple circuits and move into more elaborate integrated circuits.

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Fixator-Norator Pair Based Design of Analog Circuits

R. Rohith Krishnan and S. Krishnakumar

Abstract An approach towards the design and analysis of analog circuits is presented in this chapter. Fixator-Norator Pair (FNP), which is a combination of nullor plus sources, is the key element in this technique. A brief explanation about the possible realizations of FNPs is introduced in this chapter, which is followed by the use of FNPs in source allocation, source transformation, and biasing design. Second section deals with the design of analog integrated circuits based on FNPs. The design is primarily adhered with the design of active loads and/or current mirrors for satisfying the requirements of a given amplifier circuit. Feedback is an integral part of many analog circuits, so that the design automation of feedback networks is advantageous; which is also covered in this chapter. Finally, the complete AC performance design case is considered and it is a two-step process. FNP along with the linear equivalent model of the target circuit together does the first step, which is the design for input and output resistance and gain. The second step performs the design for bandwidth, i.e., mainly the cut-off frequencies. This is based on Bode plot analysis, which requires a reference circuit having the same frequency response as that of the desired one. All the proposed techniques are proved with the help of example circuits so that the reader can better understand the proposed method.

1 Introduction

Design of analog circuits is an artwork, where a skilled designer renders the design task into a careful selection of topology and circuit components. Normally, as the circuit length grows, the difficulty in design process also increases [1]. A designer may come across situations, not limited to source allocation, transformation, biasing

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design and frequency response design where his/her empirical skill is checked. The task becomes even complex when large number of nonlinear devices comes into play. We need a linear-like approach to treat such nonlinear circuits so that the difficulty associated with design process can be reduced [2]. This chapter proposes a tool called Fixator Norator Pair (FNP), which is a combination of nullor and source (s). The FNPs are temporary circuit components, and a fixator and norator should always be used in pairs. The pairs can be removed and replaced with actual circuit components if the final design is met [1–3]. A fixator keeps a critical design spec at the desired level and at the same time, its pairing norator helps to renders the spec into a suitable supporting component such as DC sources or passive devices. In an analog circuit design, to fix 'n' number of unknowns we need a maximum of 'n' FNPs. Sometimes, a careful analysis of the circuit under consideration directly provides solutions for some of the design specs, which means less number of unknowns to be find out and less number of FNPs required. In all the cases, the 'unknown' should have an effect on the design spec to be fixed, otherwise the feedback effect between fixator and norator fails. The basic idea is that, to define the value of an unknown for keeping a design spec fixed at a desired level, one can use FNP. Here, fixator fixes the design spec and norator defines the unknown. Once the unknown is defined, FNPs can be removed and instead real components can be placed [1–3].

Analog circuit design, diagnosis, and analysis are active areas of research [4, 5]. Among them, nullors, voltage mirror, and current mirrors share a dominant part [6, 7]. Nullors find applications in modeling of active elements and design of current mode filters [8]. Parametric fault detection, computer aided design and synthesis of active circuits are some other applications of nullors [9]. The pathological elements voltage mirrors and current mirrors are also employed in analog design. Symbolic analysis of analog circuits is another area which is gaining greater attention [10–12]. The combination of nullor and sources is called an FNP [1–3], which is an emerging tool in the design of analog circuits. Some of the advantages of FNP over its predecessors are ease of usability, simplicity in operation and its flexibility. Verhoeven et al. [13], proposed a method for the design of amplifiers based on controlled sources. Here, transistors are DC isolated and biased separately using controlled sources. Such a local biasing scheme allows the designer to do the designing of rest of the circuit in a linear way. At the end, local biasing sources are replaced with normal DC sources and current mirrors. Reza Hashemian [14] presented a somewhat similar methodology, but no controlled sources are used. In this method, the total number of local biasing sources is cut down to half, and the other half is replaced with storage elements. Local biasing results in large number of DC sources. One can use source transformation techniques to cut-down their number but the process is tedious and time-consuming. Later, Hashemian [1] introduced a more advanced tool, the FNP. It avoids most of the difficulties associated with local biasing. The pair found applications in source allocation, source transformation, biasing design, design of analog ICs, design of feedback networks and in frequency response designs. They are described in detail in the following sections.

2 The Tool

Fixator Norator Pair is the key tool in the proposed method, so a brief description about the tool is essential. This section gives an idea about the tool and its possible realizations.

Fixators: They are theoretical two terminal devices having a fixed current through and a fixed voltage across them. We can represent a fixator by $Fx(V_x, I_x)$, where V_x is the voltage across the fixator and I_x is the current through the fixator.

Norators: They are another theoretical two terminal devices in which both the current through and voltage across them can take any values.

Nullator: Equal to a fixator, but both the current through and voltage across the device are zero. That is a norator means a fixator Fx(0,0).

Nullor: A two-port device with a nullator at its input port and norator at the output port. Thus a fixator is the combination of nullor and sources

There are many different ways to realize the nullors; among them the use of ideal controlled sources and op-amps are popular [1, 3]. So realization of FNPs based on these two elements is discussed in this chapter.

Fixators are of two types; voltage fixator and current fixator. In a voltage fixator, the voltage source supplies/consumes power and the current source is inactive. On the other hand, in a current fixator, the current source supplies/consumes power and voltage source is inactive. Figure 1 represents the symbolic representation of various types of fixators and Fig. 2 gives the realization of fixators using controlled sources with very high gain (10^9) and op-amps.

In a voltage fixator the current through the voltage source, which controls the pairing norator, is monitored. Hence current controlled voltage source (CCVS) or current controlled current source (CCCS) of very high gain can be employed to work as voltage fixator. Similarly, in the case of current fixator, voltage across the current source regulates the norator. Hence such fixators can be realized using voltage controlled voltage source (VCVS) or voltage controlled current source (VCCS) of very high gain.

Op-amps are perfect nullors. Their input ports behave as nullators because both the voltage across and current through these ports are ideally zero. The output port

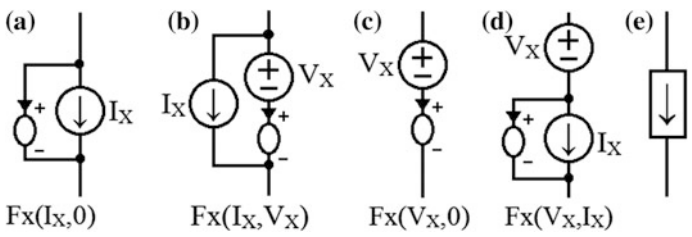

Fig. 1 Fixators; **a** and **b** current fixators; **c** and **d** voltage fixators; **e** symbol of a fixator

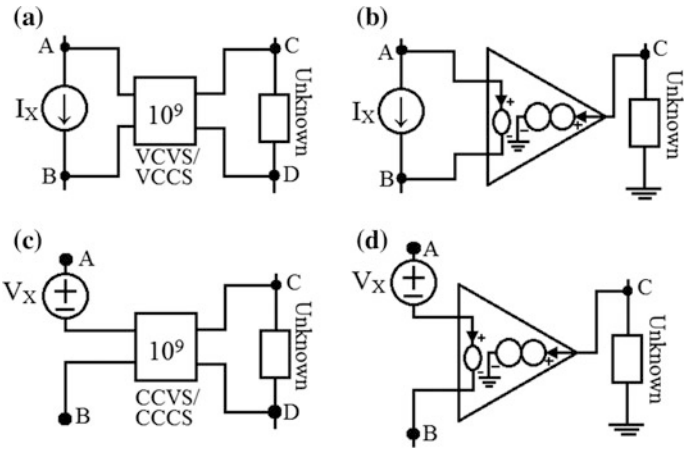

Fig. 2 Realization of fixators using controlled sources and op-amp; **a** and **b** current fixators; **c** and **d** voltage fixators

of op-amp is a norator, as the voltage and current sink/source at this port is unspecific. But it maintains a feedback effect between the ports. Thus op-amps are an ideal candidate to work as FNPs. Figure 2 shows the possible realizations of FNPs using ideal controlled sources as well as using op-amps. Op-amp fixators have the advantage that they are real components. Hence they can be realized in electronics labs, and designs can be made using the actual components we are expecting to use in our final circuit. But fixators using controlled sources are easier to insert and use in simulators. They allow more flexibility in usage than op-amps. In Fig. 2, points A and B denote the critical port, whose port value is to be fixed. Points C and D represent the port where the design supporting component is to be placed. This component may be sources or passive components such as resistors, capacitors or inductors. In some cases, a combination of two or more of these components is required to attain the given design spec. For problems such as biasing design and source allocation, current through and voltage across the norator provides required solutions. But in case of frequency response related designs, Bode plot and/or impedance function of norator is beneficial.

3 Source Allocation and Source Transformation

In this section, application of FNP in source allocation and transformation is discussed. Many times a designer may come across issues regarding source allocation and transformation in his/her designs. With the traditional approaches, the designer has to rely upon some source shifting and transformation techniques, including voltage dividing, shifting, and current mirroring. But such methods are long and

time-consuming. With the proposed approach, the designing becomes much simple. To demonstrate the technique, two examples are illustrated here, first one is a diode circuit and the second one is a common emitter amplifier circuit.

Example 1 Consider a simple diode circuit as shown in Fig. 3. The diode is biased with three sources but value of one of them, V_1 is unspecified. Our requirement is to design the value of V_1 so that the diode current will be fixed at 1 mA. In the figure, $R_1 = R_2 = 4.7\ k\Omega$, $R_3 = 3.3\ k\Omega$, $R_4 = 1\ k\Omega$, $R_5 = 860\ \Omega$, $V_2 = 1$ V, and $I_1 = 320\ \mu A$. The design steps are stated below.

1. Take the circuit under test, add a current fixator of 1 mA series to the diode. This will fix the diode current at 1 mA.
2. Replace V_1 with the pairing norator.
3. Simulate the circuit, analyze the voltage across norator. The norator voltage is equal to the required value of V_1.
4. Remove FNP from the circuit and place V_1 into its original position. V_1 have a value which is obtained in step 3.
5. Now, if we analyze this updated circuit, we can see that the diode current is 1 mA.

Here, we can see that the method does not affect the actual structure of the circuit, and the design method obeys all the network laws. Next question is how to implement the pair into the circuit. Figure 4a and b show the two possible

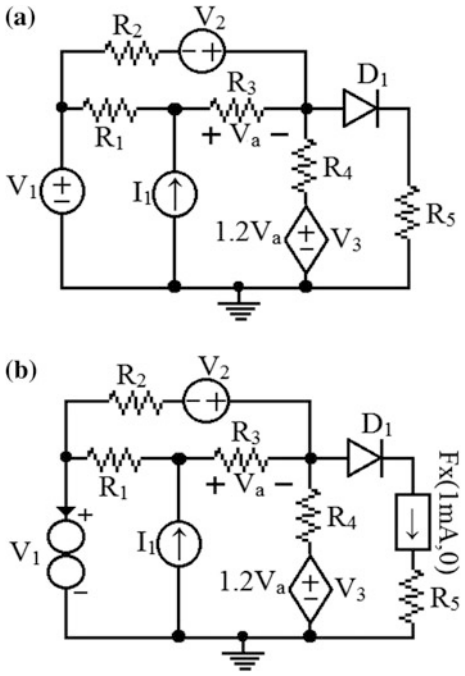

Fig. 3 **a** A diode circuit; **b** design of V_1 to get a diode current of 1 mA

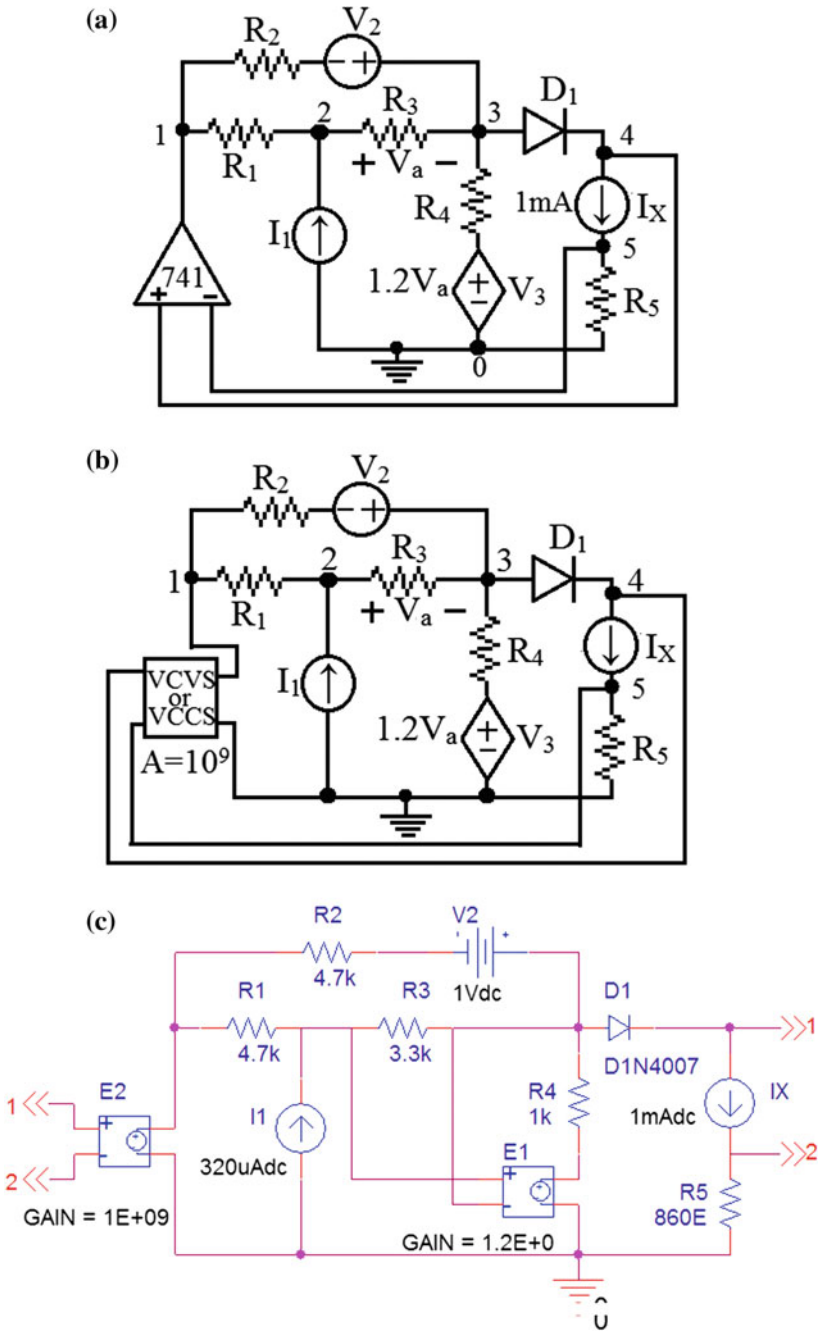

Fig. 4 Implementing FNP into diode circuit; **a** using op-amp; **b** using controlled source; **c** arrangement for simulation

implementations of the FNP method using op-amp and controlled source respectively. Figure 4c shows the circuit arrangement for simulation. Here, FNP is implemented by using the voltage controlled source E_2 together with current source I_X. The input port of E_2 works as the nullator and its output port behaves as a norator. The voltage across the output port of E_2 represents V_1, which is to be determined. Simulations show that $V_1 = 3$ V. We get same results with both the op-amp and controlled source realizations. If we re-simulate the circuit with designed value of V_1, we can see that the diode current is 1 mA.

In the remaining sections, we use the symbolic representation of FNPs for convenience in illustrations. The FNPs are implemented using controlled sources for simulations. The method employed in these sections is same as the one used in Example 1. Remember that, if we need to find the value of a voltage source or a current source which is represented by a norator, then we need to find norator voltage or norator current. But if our aim is to get the value of a resistor which is represented by a norator, we need to get both the norator voltage and current. Then, by simply dividing these parameters, we get the required value of resistance. In Sect. 7, we deal with reactive elements. In order to determine the value of a reactive element say capacitor which is represented by a norator, we need Bode plot of norator. Hence, both the AC voltage and current through the norator are critical. In all cases, the output ports of controlled sources with very high gain are used as norators. The controlling input ports together with sources are used as fixators. For determining reactive elements, a reference circuit itself is used as a 'source'.

A second case with the diode circuit is to reduce the total number of sources in the circuit to one voltage source, without changing the biasing of diode D_1, i.e., diode current should remain 1 mA. Here we assume that the requirement is to keep the actual circuit structure unchanged, with only the DC sources are replaced with a single equivalent source. The design process is explained below.

1. Remove all DC sources in the circuit except for their internal resistance.
2. Apply Fx (1 mA, 0) in series with diode D_1. Its pairing norator should be placed at a point in the circuit, where we want the equivalent source. Here we replace the source V_1 with norator.
3. Simulate the circuit. The norator voltage defines the equivalent source.

The design arrangement is depicted in Fig. 5a. Here also, the FNP can be represented with the help of VCVS (E), similar to what we done in Fig. 4c. The output port of E corresponds to the norator V_E. Hence the voltage across the norator is the equivalent voltage source V_E. The simulation shows that the value of voltage source $V_E = 4.35$ V.

Example 2 An npn-pnp feedback amplifier as shown in Fig. 6(a) is considered in this example. Our aim in this problem is to define the values of all DC sources so as to maintain a given DC bias condition for the transistors Q_1 and Q_2, which results in faithful amplification of an input signal. The desired operating points for Q_1 and Q_2 are, $V_{BE1} = 0.572$ V, $V_{CE1} = 3.4$ V, $I_{C1} = 61$ μA, $V_{BE2} = -0.66$ V, $V_{CE2} = -3.4$ V and $I_{C2} = 82$ μA. Here, $R_1 = 15$ kΩ, $R_2 = 3$ kΩ, $R_3 = 50$ kΩ,

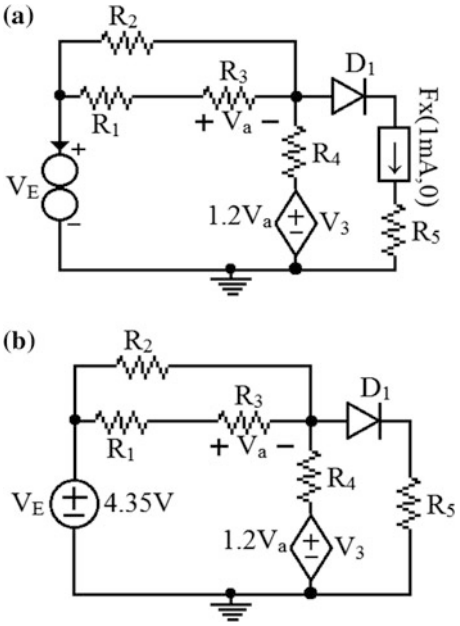

Fig. 5 **a** Design of equivalent source for the diode circuit; **b** final circuit diagram

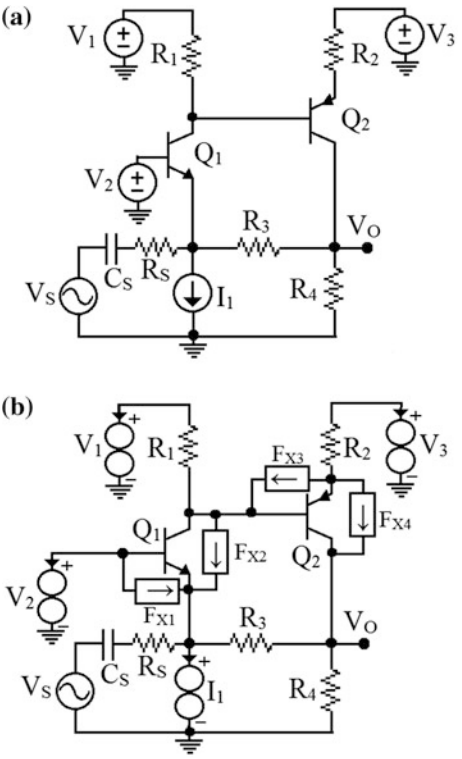

Fig. 6 **a** BJT feedback amplifier; **b** design of DC sources for a given operating point

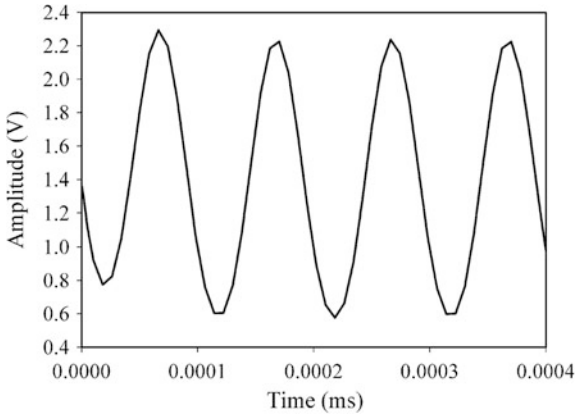

Fig. 7 The response of the BJT feedback amplifier for an input 10 sin (20000πt) mV

$R_4 = 20\ k\Omega$, $R_S = 100\ \Omega$ and $C_1 = 0.1\ \mu F$. For the transistors, $B_{f1} = 255.9$ and $B_{f2} = 231.7$. So, we have to freeze the operating points of both the transistors at the desired level and at the same time values of all DC sources should be defined. The circuit arrangement for design of DC sources using FNPs is shown in Fig. 6b. As we have to define four unknowns, viz. V_1, V_2, V_3 and I_1, we need four FNPs. The fixator F_{X1} (0.57 V, 0) fixes V_{BE} at 0.57 V and at the same time, its pairing norator defines the value of source V_1. Similarly, F_{X2} (3.4 V, 61 μA) fixes the V_{CE} and I_C of Q_1 at the design and its pairing norator defines the value of V_2. In the same way, F_{X3} (0.66 V, 0) and F_{X4} (3.4 V, 82 μA) fixes operating points of Q_2 and their norators define values of V_3 and I_1 respectively.

In order to simulate the FNP added circuit, we must remember to use output port of controlled sources as norators. As discussed, voltage controlled sources can be used for current fixators and current controlled sources can be used for voltage fxators. In both the cases, the input port of the controlled sources behaves as nullators, provided their gain should be 10^9. Here, norators corresponds to the DC biasing soures, whose value is to be defined. Upon simulating the FNP circuit as in Fig. 6b, norators define the values of all DC sources. They are, $V_1 = 5$ V, $V_2 = 1.25$ V, $V_3 = 5$ V and $I_1 = 75\ \mu A$. Now, we can remove all FNPs and instead of norators, place actual DC sources. The response of the amplifier for an input 10 sin(20000πt) mV is shown in Fig. 7. The waveform is undistorted and the amplifier has a voltage gain of around 40 dB. Hence it proves our design.

4 Biasing Design of Analog Circuits

Design of analog circuits needs attention, as it deals with DC biasing design as well as AC performance design. In this section biasing design of analog circuits employing FNPs is discussed and AC design is left for the following section. Biasing design aims at stabilizing the DC operating points of the analog circuit at a safe zone. For the case of an amplifier, generally, the transistors should be biased at

the active region. The region of operation is thus determined by the biasing of transistors and this is why the biasing design deserves much care.

Consider an amplifier circuit; there are active devices, passive devices and DC sources. Active devices are the signal conditioning elements, but the passive devices and DC sources are supporting elements. Hence there are two types of devices; drivers and supporting elements. The FNP approach is to 'DC isolate' the drivers from the rest of the circuit by freezing its critical biasing specs. With this approach, the fixator fixes a particular biasing spec at the design and at the same time, its pairing norator defines the corresponding bias supporting component. In other words, fixator fixes a port parameter and pairing norator renders it into a meaningful bias supporting component. Remember that for fixing one critical spec, we need one fixator and its pairing norator should replace one of the bias supporting components. Also, for getting fruitful results, the parameter to be fixed should have an effect on the selected bias supporting component. Sometimes, a careful analysis of the circuit gives us some solutions, which may help us to reduce the total number of FNPs. Algorithm 1 portrays the basic steps in biasing design.

Algorithm 1

1. Take the analog circuit under consideration; specify the DC operating points to be fixed.
2. Insert FNPs to the circuit. Each fixator fixes a particular design spec and its pairing norator should replace one of the bias supporting component such as a DC source or a power conducting component such as a resistor.
3. Use controlled sources with very high gain to represent FNPs. Remember to pair fixators and norators in a meaningful way, such that the fixator is sensitive to the changes in the norator.
4. Simulate the circuit. The norator voltage and current directly give us the required solutions.
5. The final step is to remove all FNPs and instead of norators, place actual supporting elements which are designed in step 4.

The design procedure is demonstrated with the help of two examples as given bellow. First one is a two-stage MOS amplifier and the second is a three-stage BJT amplifier.

Example 3 Here, a two-stage MOS amplifier as shown in Fig. 8a is considered. In this case, our aim is to maintain a maximum output voltage swing of 3 V peak and at the same time gate-source voltage of M_1 should maintained at 1.1 V. All the other biasing specs are not taken as critical, but transistors should operate at active region. As we have two critical biasing specs, we need two FNPs to define two unknowns. Let us assume that R_1 and R_4 are the unknowns and all other resistors are already defined as $R_2 = 77\ k\Omega$, $R_3 = 10\ k\Omega$, $R_5 = 3.3\ k\Omega$ and $R_L = 10\ k\Omega$. Also, the capacitors $C_S = 1\ \mu F$, $C_1 = 10\ \mu F$ and $C_2 = 5.3\ \mu F$. For the MOS devices, W/L = 10/1. The FNP arrangement for redesign is shown in Fig. 8b. The fixator F_{X1} (1.1 V, 0) fixes the gate to source voltage of M_1 at 1.1 V, at the same time; its pairing norator defines the value of R_1. Similarly, a second fixator F_{X2}

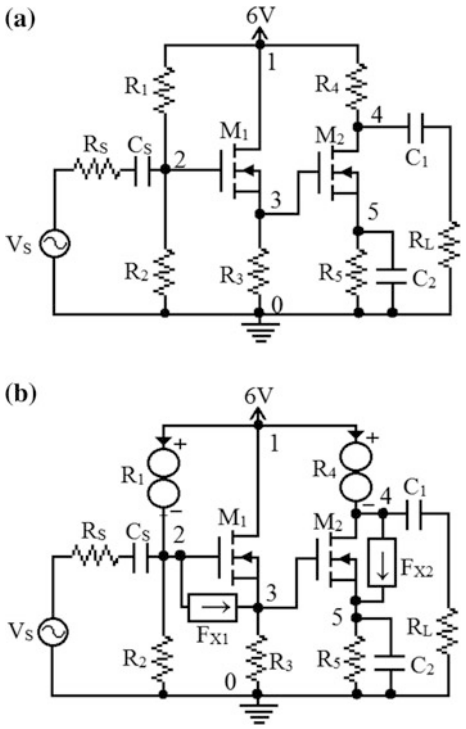

Fig. 8 **a** Two-stage MOS amplifier; **b** its biasing design using FNPs

(3 V, 0) sets the peak output voltage swing at 3 V, and its pairing norator defines the value of R_4. Here also, controlled sources with a gain of 10^9 are used to represent the FNPs.

Simulating the circuit as shown in Fig. 8b implies that the value of R_1 is 35.2 kΩ and that of R_2 is 1.94 kΩ. Now, it is necessary to check the final response of the amplifier. The result of bias point analysis of the final circuit is shown in Table 1. This validates our design.

Example 4 In this example, a part of the MC 1553 BJT amplifier circuit as shown in Fig. 9 is considered. Here, some of the power conducting components are already defined; but few are left out to the designer to design them in such a way that the critical biasing conditions for this circuit are met. In Fig. 9, resistors $R_S = 10\ \Omega$, $R_2 = 2.7$ kΩ, $R_3 = 9$ kΩ, $R_6 = 640\ \Omega$ and $R_7 = R_8 = 600\ \Omega$ and capacitor $C_S = 0.1$ μF. The transistor parameter $B_{f1} = B_{f2} = B_{f3} = 255.9$. For this circuit, the biasing specs, which are considered to be critical are, $V_{CE1} = 0.366$ V, $I_{B2} = 8.6$ μA, $V_{CE3} = 4.8$ V and $I_{C3} = 4.46$ mA.

The critical specs can be considered as three port parameters and three unknowns to be defined are resistors R_1, R_4 and R_5. Hence we need three FNPs. Figure 10

Table 1 The result of bias point analysis of the modified MOS amplifier

Node	1	2	3	4	5
Voltage (V)	6.00	4.12	3.02	4.89	1.89

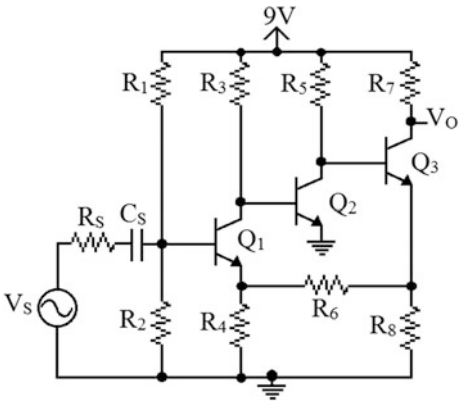

Fig. 9 Three stage BJT amplifier circuit

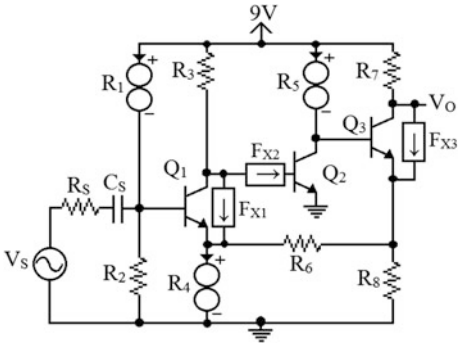

Fig. 10 Redesign of three stage BJT amplifier using FNPs

shows the circuit arrangement for biasing design. Here, F_{X1} fixes the value of V_{CE1}, F_{X2} fixes I_{B2} and F_{X3} fixes V_{CE} and I_C of Q_3. After simulating this circuit, we can calculate the values of R_1, R_4 and R_5 as 23 kΩ, 100.3 Ω and 4.98 kΩ respectively. Now, we can remove all FNPs from the circuit and instead of norators, place actual resistances of designed values. Bias point analysis of the final circuit implies that the DC biasing of the amplifier is very much close to the required values.

5 Design of Analog Integrated Circuits

An analog circuit mainly involves two types of components, drivers (active devices) and supporting components (passive devices). But in the case of analog integrated circuits (AIC), the role of supporting components is done by active loads (ALs) and current mirrors (CMs). The difference between the static and dynamic resistance of ALs (or CMs) is very high. Therefore it is possible to obtain a larger AC resistance using ALs or CMs with small DC voltage drops across them. This is advantageous

for amplifiers because for obtaining a larger AC gain, and need for a high valued resistor is avoided. This is why ALs and CMs are suited for integrated circuits.

Design of an analog circuit includes AC performance design and DC biasing design. The AC design aims at setting the input and output resistance, gain and bandwidth, whereas biasing design aims in non-distorted output signal; that is running the drivers at proper operating regions. The steps in design of AIC are discussed in Algorithm 2.

Algorithm 2

1. Select a working circuit topology. Define the AC specifications and critical DC biasing specs required for the circuit.
2. Create a linear equivalent model of the circuit, where all active devices have been replaced with their linear models at the desired operating points.
3. Apply FNPs into the linear circuit such that one fixator fixes one AC parameter and its pairing norator defines value of one supporting component. Here supporting component means dynamic resistance of ALs or CMs.
4. After simulating the circuit equipped with FNPs, we get values for all dynamic resistances. This is all about the AC design and next we go to biasing design.
5. Take the original circuit and add FNPs into it in such a way that fixators fix the critical DC biasing specs and at the same time, its pairing norators define the value of corresponding supporting components. Here supporting components refers to static resistance of ALs or CMs. Simulation of this arrangement provides values for all static resistances.
6. Concluding the results of AC and DC designs, we can select most suitable ALs and CMs, which can do the role of bias supporting components. Note that, a designer can select suitable ALs and CMs from a predefined library or a newer one can be designed.

In this section, two examples are worked out. They are a BJT differential amplifier and a three-stage MOS op-amp. Also, the design of ALs and CMs using FNPs is discussed and is portrayed in Algorithm 3.

Example 5 A BJT differential amplifier with a circuit topology as in Fig. 11 is considered in this example. The amplifier is required to have a voltage gain (A_V) of 84 dB, input resistance (R_{in}) 18 kΩ and output resistance (R_{out}) 46 kΩ. The DC biasing should be maintained such that it will allow maximum voltage swing at the output. The desired operating points for the three transistors are given in Table 2.

Next, the linear equivalent circuit of the differential amplifier is to be developed with active devices are replaced with their linear model at the desired operating point. The equivalent circuit is shown in Fig. 12a. Here, $r_{AL1\text{-}3}$ and r_{CM} represents the dynamic resistance of ALs and CMs. Our requirement is to define the values of all dynamic resistances so that the AC performance criteria are met. The design arrangement for dynamic resistance is shown in Fig. 12b.

In Fig. 12b, $r_{\pi 1} = r_{\pi 2} = 10.8$ kΩ, $r_{\pi 3} = 2.79$ kΩ, $r_{o1} = 228.16$ kΩ, $r_{o2} = 225.74$ kΩ, and $r_{o3} = 75$ kΩ. Fixator F_{X1} (100 μV, 5.55 nA) fixes input resistance of the differential amplifier at 18 kΩ and its pairing norator defines the value of

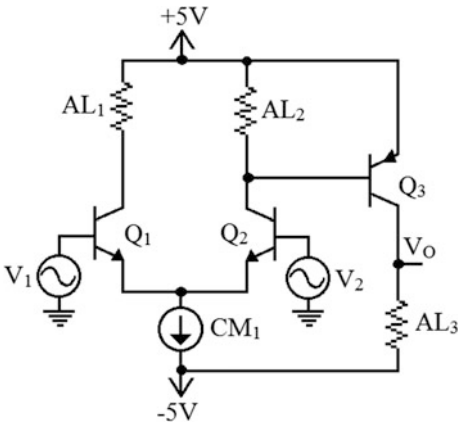

Fig. 11 BJT differential amplifier circuit

Table 2 Desired operating points for BJT differential amplifier

BJT	V_{CE} (V)	I_C (μA)
Q_1	4.1	324.33
Q_2	5.0	327.80
Q_3	−5.0	662.00

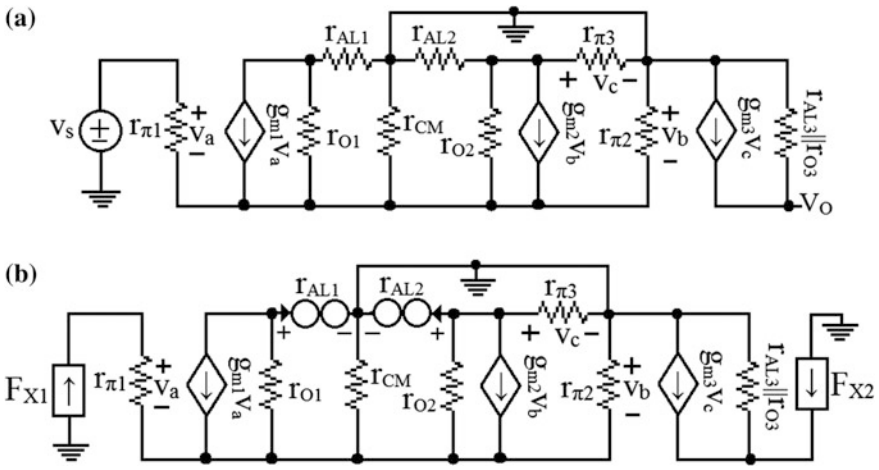

Fig. 12 **a** Linear model of BJT differential amplifier; **b** its AC design using FNPs

r_{AL1}, which is the dynamic resistance of AL_1. Similarly, output fixator F_{X2} (1.58 V, 0) fixes the gain of the amplifier at 84 dB and its pairing norator defines dynamic resistance of AL_2. As per the design requirement, our third AC parameter is output resistance r_{out} of amplifier. From the linear equivalent circuit, it is clear that r_{out} is the equivalent of parallel resistors r_{o3} and r_{AL3}. Hence dynamic resistance r_{AL3} can

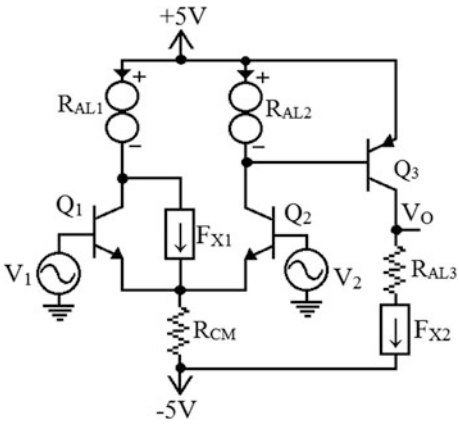

Fig. 13 DC design of BJT differential amplifier using FNPs

be directly calculated as 120 kΩ. Since we need to define only three unknowns, we can assume a suitable value for $r_{CM;}$ here it is taken as 120 kΩ. Simulating the circuit as shown in Fig. 12b, we get $r_{AL1} = 141$ kΩ and $r_{AL2} = 143.5$ kΩ. This is all about the AC design of BJT differential amplifier.

Next step is the design for static resistance of ALs and CMs, which is done through DC biasing design. Figure 13 shows the FNP arrangement for the DC design. Initially, the total number of unknowns is four. But through careful analysis, we directly get values of two unknowns. First, we know the expected current through and voltage across the CM. So we can directly calculate its static resistance R_{CM} and is seen to be 6.68 kΩ. A similar approach provides static resistance of AL_3 also. It is found to be 7.55 kΩ. Hence, the total number of unknowns is now reduced to two and we, therefore, need only two FNPs as indicated in Fig. 13. The fixator F_{X1} (4.1 V, 0) fixes the V_{CE} of Q_1 at 4.1 V and at the same time the pairing norator renders it into a proper static resistance of A_{L2}. Similarly, F_{X2} (662 μA, 0) fixes the collector current of Q_3 at 662 μA and its pairing norator defines static resistance of AL_1. Simulating the circuit arrangement as in Fig. 13 provides R_{AL1} and R_{AL2} as 4.57 kΩ and 2.05 kΩ respectively.

Now we have the values for all static and dynamic resistances of the BJT differential amplifier. Next step is to render the results of AC and DC design into a suitable selection of ALs and CMs. As discussed, a designer can either design a new AL and/or CM, or select from a predefined library. The FNP approach for the design of a simple CM as shown in Fig. 14a is portrayed in Algorithm 3.

Algorithm 3

1. State the desired value of DC mirror current I_M, which is the collector current of the transistor used in the mirror.
2. Select transistors having early voltage VA such that VA/I_M equals the required value of dynamic resistance r_M.
3. Bias the mirror transistor at a voltage V_M, which is the proposed DC drop across the mirror.

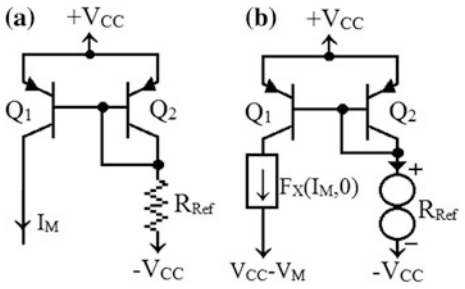

Fig. 14 **a** A simple CM circuit; **b** design of CM using FNP

4. Insert a current fixator F_X (I_M, 0) for fixing the collector current of mirror transistor at I_M, its pairing norator defines the value of reference resistor.

In the above algorithm, early voltage VA [15] is a parameter that relates the collector or drain current of a transistor with the collector to emitter or the drain to source voltage in the active or saturation region of operation. For BJTs, the large signal collector to emitter resistance is the ratio of VA to collector saturation current. In the case of MOSs, the large signal drain to source resistance is the ratio of VA to drain saturation current.

The design arrangement is shown in Fig. 14b. This concludes that a CM or AL is characterized mainly by three sets of parameters, r_M, I_M and V_M. For a regular designer, a library of ALs or CMs makes the overall design process simpler and quicker. Going back to Example 5, Fig. 15 shows the final circuit. The simulation result of final circuit is also given below, which proves our design.

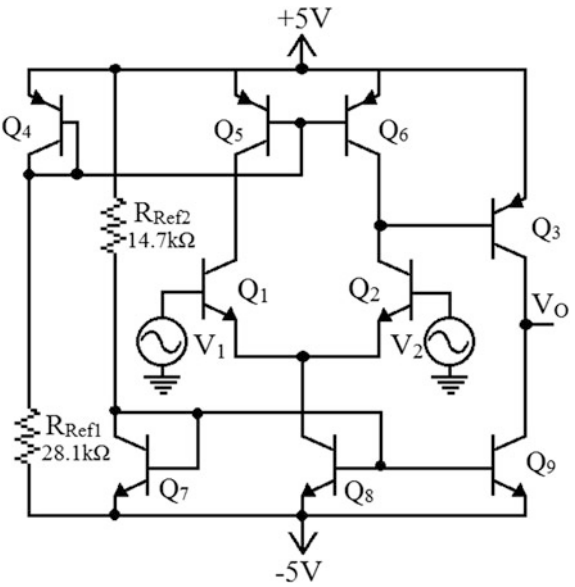

Fig. 15 Final circuit diagram of BJT differential amplifier

```
**** SMALL-SIGNAL CHARACTERISTICS
V(VO)/V_V1 = −1.565E + 04
INPUT RESISTANCE AT V_V1 = 1.858E + 04
OUTPUT RESISTANCE AT V(VO) = 4.615E + 04
```

Example 6 A three-stage MOS op-amp is considered in this example, which requires a voltage gain of 82 dB and output resistance of 27 kΩ. A circuit topology as shown in Fig. 16 is selected for this design with operating points as shown in Table 3. Following the Algorithm 3, designing starts with the construction of the linear equivalent model of the three stage amplifier. The rest of the designing process is same as that of BJT differential amplifier. Here we need to set only two parameters; hence we can relate them to only two unknowns using FNPs. Let them be r_{AL4} and r_{AL5}. Value of r_{AL5} can be directly defined as 54 kΩ and the total number of unknowns is now reduced to one. Keep in mind that before going for simulating the FNP arrangement, we must assign suitable values to other unknowns, i.e., the dynamic resistance of remaining ALs and CMs. The FNP arrangement for design of r_{AL3} is shown in Fig. 17. Fixator F_X(1.26 V, 0) fixes the voltage gain of the amplifier at 82 dB and at the same time, its pairing norator defines the value of r_{AL4}. Simulating the circuit as in Fig. 17 shows that value of r_{AL4} is 124 kΩ.

Next, the DC biasing design is to be performed so as to keep the biasing of the MOS transistors at the desired level and to define the static resistance of various ALs and CMs in the circuit. Figure 18 shows the design for DC biasing. It is due to

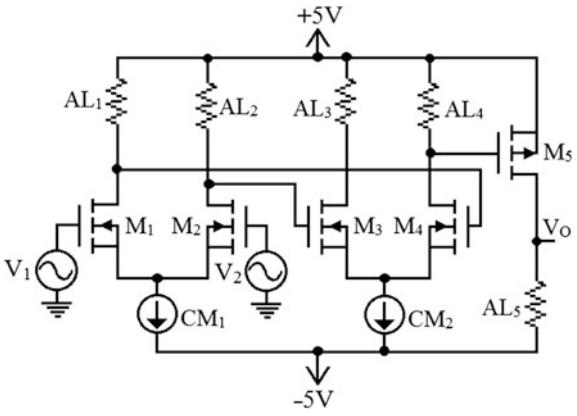

Fig. 16 The topology of three stage MOS op-amp

Table 3 Desired biasing specs for the three-stage MOS op-amp

MOS	V_{DS} (V)	V_{GS} (V)	I_D (μA)
M_1	3.212	3.589	200.00
M_2	3.212	3.589	200.00
M_3	4.368	3.556	193.67
M_4	4.368	3.556	193.67
M_5	−5.00	−4.560	467.20

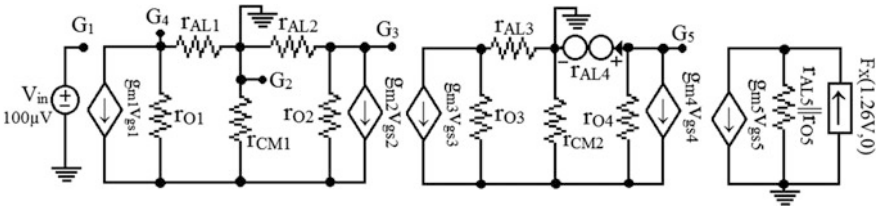

Fig. 17 Design of r_{AL4} using FNP for a required gain

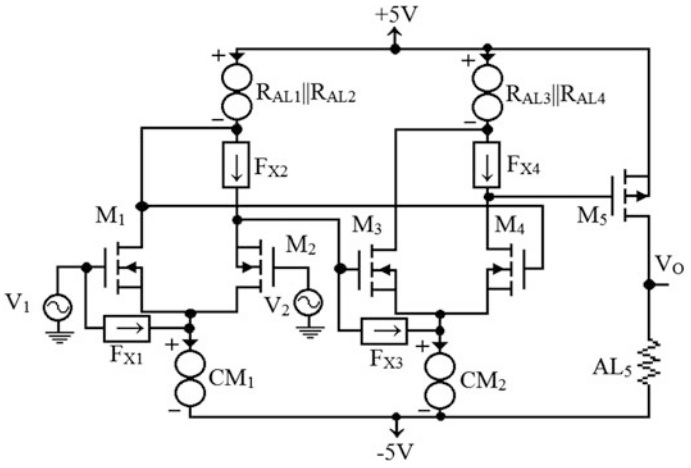

Fig. 18 DC design of the three stage MOS op-amp using FNPs

the symmetrical property of differential pair, we are using a single FNP to find the equivalent parallel resistance of R_{AL1} and R_{AL2} and similarly for R_{AL3} and R_{AL4}. Value of R_{AL5} can be directly obtained as 10.7 kΩ. In the figure, F_{X1} (3.59 V, 0) fixes V_{GS} of M_1 at the design and its pairing norator finds the value of $R_{AL1}||R_{AL2}$. A second fixaor F_{X2}(3.2 V, 200 μA) not only fixes V_{DS} and I_D of M_2 but also find the value of R_{CM1}. In a similar manner, F_{X3}(3.56 V, 0) and F_{X4}(4.37 V, 194 μA) defines values of $R_{AL3}||R_{AL4}$ and R_{CM2} respectively. Simulation shows that, $R_{AL1} = R_{AL2} = 27$ kΩ, $R_{AL3} = R_{AL4} = 23.6$ kΩ, $R_{CM1} = 3.5$ kΩ and $R_{CM2} = 2.75$ kΩ. Finally, we can select appropriate ALs and CMs to replace the FNPs. The final circuit of three-stage amplifier is shown in Fig. 19 and the analysis of the final circuit shows that the results are close to our design.

**** SMALL-SIGNAL CHARACTERIS
V(VO)/V_V1 = −1.304E + 04
INPUT RESISTANCE AT V_V1 = 1.000E + 20
OUTPUT RESISTANCE AT V(VO) = 2.675E + 04

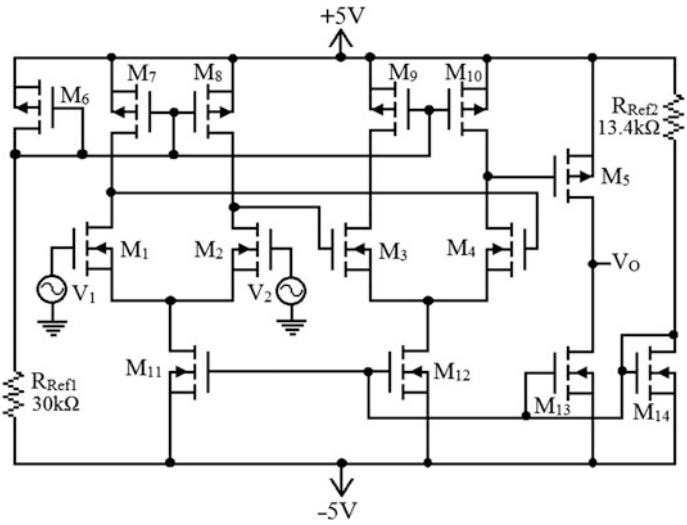

Fig. 19 Final circuit diagram of three-stage amplifier

6 Design of Feedback Networks

Feedback networks are an integral part of analog circuits. It defines the gain, input resistance, output resistance and even the stability of the circuit. Since we are dealing with AC parameters, it is appropriate to use the linear equivalent model of the desired circuit for designing. Such a linear circuit is suitable to apply FNPs for further analysis and design. In this section, design of feedback networks for controlling input resistance, output resistance and gain are considered. Fixators are applied to linear equivalent model of the target circuit and their pairing norators define the feedback components. Care should be taken to DC isolate the added feedback circuit so as to prevent any variation in the original biasing of the circuit. The symbolical representation of the methodology is portrayed in Fig. 20 and the basic steps in the procedure are given in Algorithm 4.

Algorithm 4

1. Define the required AC parameters of the target circuit, say amplifier.
2. Construct linear equivalent model of the circuit at the desired operating points.
3. Identify the location in the linear circuit $X_1 - X_2$ for applying fixators. Pairing norator should be placed at a proper location in the circuit, $Y_1 - Y_2$.
4. Simulate the circuit hence created. By analyzing the norator current and voltage, we can easily identify the component(s) in the feedback network.
5. Finally, remove all FNPs but replace norators with the designed feedback component(s). Also, add proper DC isolation capacitors in the feedback path to prevent biasing errors.

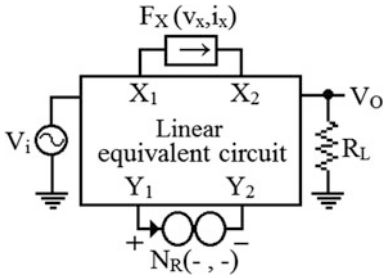

Fig. 20 Design of feedback network using FNP

Note that, selection of points $X_1 - X_2$ and $Y_1 - Y_2$ needs careful attention. For fixing parameters of a port $X_1 - X_2$, a fixator should be applied at this port and its pairing norator gets its place between points Y_1 and Y_2. Thus the points Y_1 and Y_2 have some significance. The points should be selected such that if a proper feedback network is applied between these points, then the parameters at $X_1 - X_2$ should be fixed. That is both the points $X_1 - X_2$ and $Y_1 - Y_2$ are sensitive to each other and changes in $Y_1 - Y_2$ should reflect at port $X_1 - X_2$.

Example 7 Here, a CMOS differential amplifier with buffer stage as shown in Fig. 21 is considered for design. The component values, $R_1 = R_2 = 28$ kΩ, $R_3 = 5.5$ kΩ, $R_4 = 121$ kΩ and for MOS M_1 and M_2, W/L = 10/1 and for M_3, W/L = 20/1. In this case, the input resistance and gain are the two critical design specs. Originally, the amplifier possesses an extremely high input resistance and a gain of 130 V/V. Our aim is to reduce the gain to 100 V/V and at the same time, input resistance should be fixed at 100 kΩ. Following the Algorithm 4, design process starts with the construction of linear equivalent model of the CMOS differential pair and is followed by insertion of proper FNPs. The FNP circuit for the design is shown in Fig. 22.

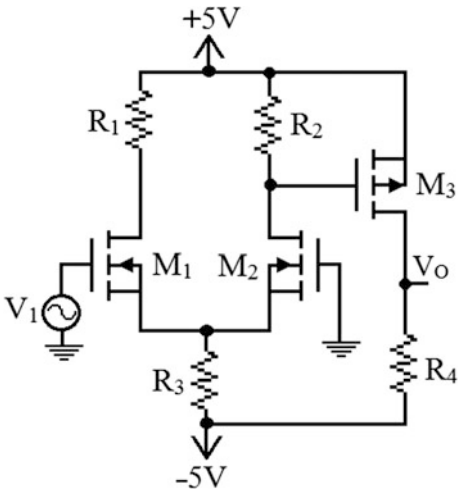

Fig. 21 CMOS differential amplifier with buffer stage

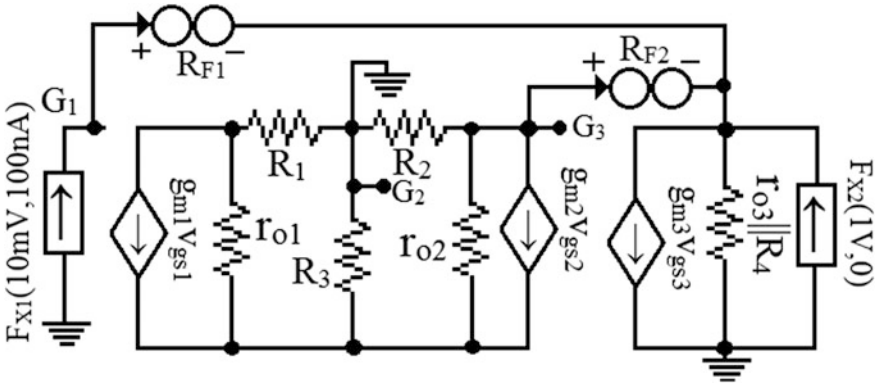

Fig. 22 AC design of CMOS differential amplifier using FNPs

Here, F_{X1} (10 mV, 100 nA) fixes the input resistance of the differential amplifier at 100 kΩ and its pairing norator defines the value of R_{F1}. Similarly, fixator F_{X2} (1 V, 0) fixes the gain of the differential amplifier at 100 V/V and R_{F2} is defined by its pairing norator. Simulation shows that the value of $R_{F1} = 10.1$ MΩ and $R_{F2} = 3.23$ MΩ. The feedback components should be DC isolated from rest of the circuit using proper coupling capacitors. The analysis of the modified circuit is shown below and this proves our design. Final circuit diagram of the amplifier with feedback is shown in Fig. 23. As discussed above the resistors R_{F1} and R_{F2} should be DC isolated using proper coupling capacitors, which are AC short at the region of operation of the differential amplifier.

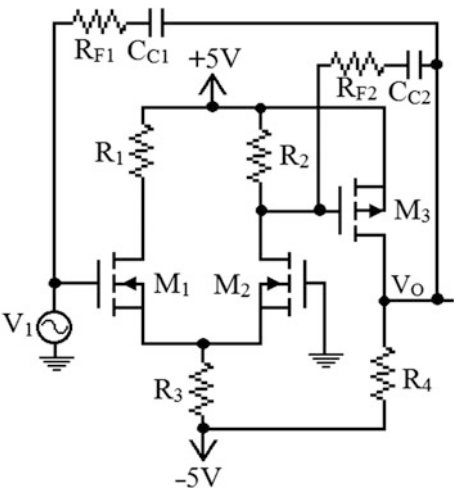

Fig. 23 Modified circuit of MOS differential amplifier

**** SMALL-SIGNAL CHARACTERISTICS
V (VO)/V_V1 = −9.999E + 01
INPUT RESISTANCE AT V_V1 = 1.000E + 05
OUTPUT RESISTANCE AT V (VO) = 7.830E + 04

The proposed method can be used for the design of input resistance, output resistance and gain. However, the design of cut-off frequencies and bandwidth are not included in the study. A modified form of this technique is useful for the complete design of analog circuits, which is explained in the next section.

7 Complete Design of Analog Circuits

In this section, we are dealing with performance design of analog circuit, which includes design for input and output resistance, gain and cut-off frequencies. The methodology consists of two parts; the first part is the design for input and output resistance and gain and the second part is the design for cut-off frequencies. First part of the design is already explained in Sect. 6, hence our primary focus in this section is on second part. The design for cut-off frequency using FNPs employs a Bode plot approach along with a reference circuit. The reference circuit should have the same frequency response as expected from the circuit to be designed. Here, a two terminal sub-circuit is designed with the help of FNPs and inserted into the circuit under design. The procedures in part 2 of the design are given in Algorithm 5 and its block diagram representation is shown in Fig. 24.

Algorithm 5

1. Take the circuit under consideration with all feedback elements designed in part 1 of the design are inserted.
2. Select a reactive element in the circuit which has an effect on the cut-off frequency to be set. Otherwise identify a port in the linear circuit, where a two

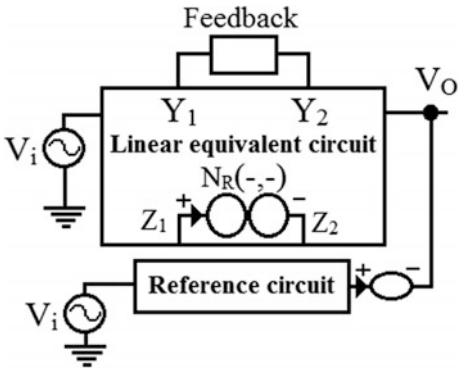

Fig. 24 Design of two terminal sub-circuit using FNP

terminal sub-circuit can be added. The addition of sub-circuit will modify the desired cut-off frequency.
3. Take a suitable reference circuit which having the same frequency response as that of the expected one. Connect the outputs of reference circuit and circuit under consideration through a nullor.
4. Place the norator at the location selected in step 2. Simulate the circuit and plot the impedance function of norator. By analyzing the plot, we can identify the component(s) in the sub-circuit.

Note that, in an analog circuit, there are mainly three types of capacitors. They are coupling, bypass, and internal transistor capacitors. First two types of capacitors are in series to signal flow and can affect lower cut-off frequency of the analog circuit. The internal transistor capacitors are in parallel to signal flow and it determines the higher cut-off frequency. This should be considered while dealing with cut-off frequencies of analog circuits.

In the Fig. 24, points $Y_1 - Y_2$ corresponds to points where feedback network is inserted as a result of part 1 of the design. Points $Z_1 - Z_2$ denotes the location for sub-circuit. As discussed, the reference circuit has the same frequency response as that of from the final circuit. Its frequency response is copied to the actual circuit by the insertion of proper sub-circuit.

Example 8 Consider the two-stage common emitter-common base (CE-CB) amplifier as shown in Fig. 25. Design requirements are, the circuit should have a voltage gain of 350 V/V, an input resistance of 1.25 kΩ and the higher cut-off frequency F_H of the amplifier should be 1 MHz. The first two parameters, i.e., gain and input resistance of the amplifier are set during part 1 of the design. The second part of the design sets the third parameter, i.e., the cut-off frequency F_H.

In the figure, $R_S = 200\ \Omega$, $R_1 = 22\ k\Omega$, $R_2 = 47\ k\Omega$, $R_3 = 15\ k\Omega$, $R_4 = 9\ k\Omega$, $R_5 = 9\ k\Omega$, $R_6 = 47\ k\Omega$, $R_7 = 22\ k\Omega$, $R_8 = 15\ k\Omega$, $R_9 = 10\ k\Omega$, $C_S = C_4 = 1\ \mu F$, $C_1 = C_2 = C_3 = 10\ \mu F$ and the transistor parameters $\beta_{f1} = \beta_{f2} = 100$. The

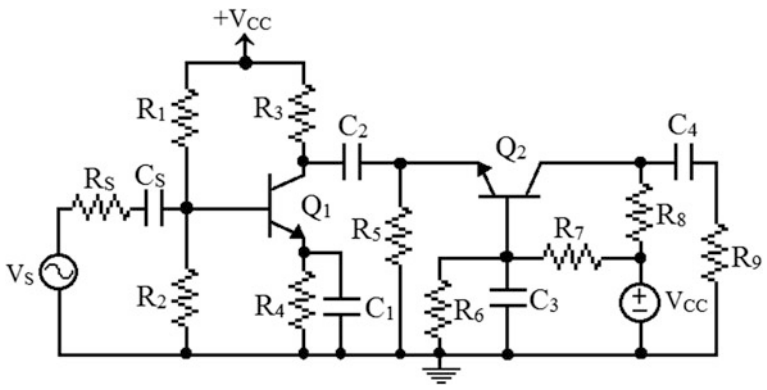

Fig. 25 Two-stage CE-CB amplifier circuit

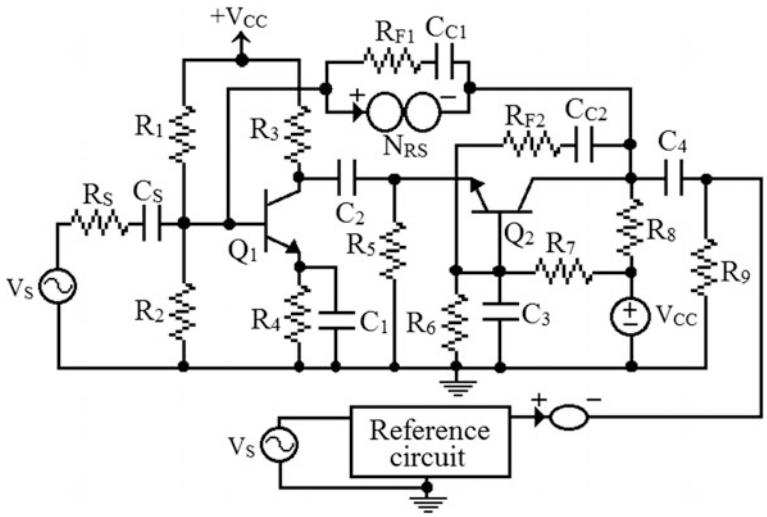

Fig. 26 Design of sub-circuit for the CE-CB amplifier

procedure for the first part of the design is already discussed in the previous section; hence it is not repeating here. In this case, the solution to first part of the design is to insert two feedback resistors R_{F1} and R_{F2}; first one between base of Q_1 and collector of Q_2, and the second one is between the base and collector of Q_2. Design result shows that value of $R_{F1} = 2.43$ MΩ and $R_{F2} = 349$ kΩ. Therefore, we can modify the original circuit by inserting the two resistors. The added resistors should be DC isolated using proper coupling capacitors. This modified circuit can be used for second part of the design along with a reference circuit, having the same frequency response as that of expecting.

As stated in Algorithm 5, in the second part of the design, the outputs of reference circuit and the modified amplifier are connected together through a nullor. The sub-circuit is planned to connect across resistor R_{F1}; hence the norator should be connected parallel to R_{F1}. The circuit arrangement for the design of sub-circuit is shown in Fig. 26 and Bode plot for norator is shown in Fig. 27.

By analyzing the bode plot, it is clear that the impedance function shows a magnitude of 118 dB at 100 kHz and it is further found that the sub-circuit is simply a capacitor. Using the equation $C = 1/(Z(\omega) \times \omega)$, its value is found to be 2 pF. The final circuit diagram of the two-stage BJT amplifier is shown in Fig. 28. The simulation result of the modified circuit is in agreed with our design requirements. Finally, it is necessary to check the stability of the modified circuit. As per the feedback stability theory, a system is considered as stable if the gain reaches 0 dB before the phase shift reaches ±360°. Magnitude-phase Bode plots of the final circuit is shown in Fig. 29. This implies that the system is stable and thus it concludes our design.

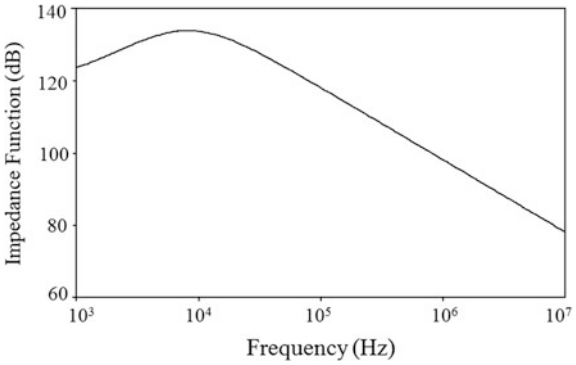

Fig. 27 Bode plot for norator

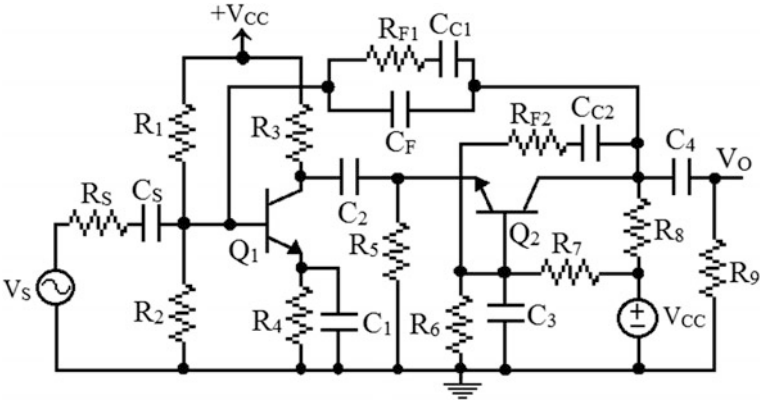

Fig. 28 Final circuit diagram of the two-stage amplifier

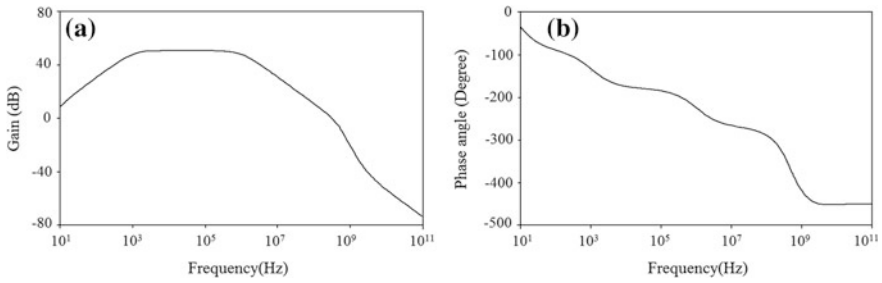

Fig. 29 Bode plots of modified two-stage amplifier; **a** magnitude; **b** phase angle

```
**** SMALL-SIGNAL CHARACTERISTICS
V(VO)/V_VS = −3.500E + 02
INPUT RESISTANCE AT V_VS = 1.250E + 03
OUTPUT RESISTANCE AT V(VO) = 5.715E + 03
```

8 Summary

The use of FNPs in analog design provides some shortcuts to a target solution. The FNPs are not limited for a set of designs, but a skillful designer can expand its applicability to any extend. The basic idea is, to design the value of an unknown so as to fix a critical design parameter at a desired level. Remember that the application of FNP should be within the rules and laws of circuits. Also, the fixator and norator should be paired in a meaningful manner, failing which results the lack of feedback effect between the pairs and thus the designing fails.

The concept of FNPs and their possible realizations, source allocation/transformation, biasing design, AC performance design and frequency response design are discussed in detail. In addition, using the proposed method, design of AICs, design of ALs/CMs and complete design of analog circuits for a given set of AC performance and DC biasing parameters are performed in a much simpler way. The scope of the work is very large, but some typical examples have been anchored with sufficient explanations. For obtaining fruitful results, it is better for the designer to have a basic knowledge on the target circuit so that a skillful analysis sometimes reduces the total number of unknowns to be found out. Less number of unknowns implies less number of FNPs and eventually reduction in the designing time and task. The applications of FNPs are not limited; they are the corner stone on which an efficient designer can develop much more sophisticated design tools.

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Application of Fixator-Norator Pairs in Analog Circuit Design

Reza Hashemian

Abstract Recently Fixator-Norator Pairs (FNP) have been shown to be very powerful tools in designing analog circuits for multiple specs. These specs are separated into different areas of the design, and for each area a specific design methodology is introduced in this chapter. The areas mainly consist of designing for circuit biasing, gains, input and output impedances, active loads and current mirrors in ICs, and frequency responses and bandwidth for amplifiers. Very similar to a nullor, it is shown that the role of the fixator in an FNP is to provide a fixed and stable response to a circuit variable as specified by the design criteria. The norator, on the other hand, acts as a place holder for one or more circuit components that are needed to provide the requirements in the circuit to respond to spec, being held constant by the fixator. In designing for frequency and bandwidth, specifically, the mission is harder because of the complexity of the situation. It is shown that a model circuit helps in this case to provide the frequency response needed for the design. Since a model circuit is only for simulation purposes, it can be constructed from ideal components such as controlled sources, and it can be even built quite modular. As shown, the FNP methodology works for both linear and nonlinear circuits. However, for nonlinear circuits we need to keep the biasing situation unchanged during the AC design process. The circuit biasing may change when feedbacks are added to the original amplifier circuit, if not protected. In case needed, coupling capacitors are added to protect the circuit biasing. There are sections in the chapter, where each covers a separate feature and application of FNP in analog circuit design. Examples have also been worked out in rather details to show the role and significance of FNP in each application.

Keywords Amplifiers · Analog circuit design · Bandwidth · Biasing Circuit simulation · Fixator-norator pairs · Gain

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1 Introduction

This chapter covers some major applications of Fixator-Norator Pairs (FNP) in analog circuit design [1, 2]. It starts with introducing fixators and norators. A fixator is considered a pathological element like a nullator, where its variables are fixed rather than being zero. The behavior of FNPs in linear circuits are discussed in Sect. 2. Rules concerning fixators and norators are also discussed in this section. Section 3 is on biasing design focusing on individual devices. It shows how the nonlinear devices, mainly diodes, BJT, and MOS transistors, are linearly and nonlinearly modeled by fixators.

The application of FNP in designing for gains, input impedances and output impedances are covered in Sect. 4. One of the issues we are commonly facing is when both biasing (DC) and performance (AC) designs are in conflict with the values of some circuit components, usually resistors. The problem is, how to assign two different values to a single component in two different cases. In integrated circuits the problem is resolved by using current mirrors and active loads. Fixators and norators are used for the design of active loads and current mirrors in Sect. 5. These components are classified into three types, which are types L, R, and H for MOS transistors as well as the same types for BJTs in this section. Designing for analog VLSI circuits are discussed in Sect. 6. Again, FNPs are very instrumental in this application. The difference between designing for lumped circuits and integrated circuits are made clear here. In lumped circuits mixing biasing design and performance design is possible by using coupling and bypass capacitors to separate power and signal paths. Whereas, this is not permissible in IC designs. The way we handle the separation of the two here is through the use of active loads and current mirrors.

Section 7 is devoted to the use of nullors in amplifier design for bandwidth. Because of the complexity and frequency dependency of the results such designs must be always guided by a model circuit. This model circuit is assumed to be given or synthetically constructed to produce the desirable output characteristic and bandwidth needed. The role played by a nullor here is two folded; one to make the circuit response follow the response from the model circuit, and two, to make required modifications to adequately respond to the desirable output characteristic. Since the model circuits are only for simulation purposes, they can be constructed from ideal components such as ideal controlled sources, and they can be even constructed quite modular.

There are numerous examples worked out and simulated to support the theory. Finally, the chapter finishes with conclusion and references.

2 Fixator-Norator Pairs

Fixator-norator pairs are pathological components that help to design analog circuits for a set of given specs. It is important to note, however, that FNPs are temporary and do not remain in the circuit after the circuit is designed. Before we go through the design methodologies we need to introduce FNP and its properties.

2.1 Fixator and Norator

A fixator represents a constant and fixed (in AC the amplitude and phase are fixed) current source as well as a fixed voltage source. A fixator is a generalized nullator that instead of zero it can accept any value for its voltage or current. There are different forms of fixators depending on the application. Figure 1 shows two forms of a fixator depending on whether (1) the voltage source V_j consumes power in the fixator and the current source I_j stays idle, or (2) the other way around. In Fig. 1a the voltage source consumes power in the fixator, and Fig. 1b is its symbolic representation. In Fig. 1c the power sink is left out, and $F_x(0, I_j)$ is a *current fixator*. Figure 1d, e, and f are similar to (a), (b), and (c), except here the current source consumes power in the fixator, and $F_x(V_j, 0)$ represents a *voltage fixator*.

Now we need to show that a fixator cannot stay alone in a circuit. In general, any circuit component is identified by its two variables, current and voltage. Typically the component specifies one of its variables or a relationship between them, and the other variable is found through KVL and KCL in a circuit analysis. However, this is not the case in a fixator. Here both variables are specified, and the only way to be able to include it to a circuit is to find a component that neither of its variables is specified. And this component is a norator. This is why a fixator, like a nullator, must always be accompanied by a norator. We may think of this pair like an ideal controlled source, but there are major differences between the two. The gain or the degree of dependency in an FNP is unlimited whereas it is limited in a controlled source. The second and the major difference between the two is that, in a multi-controlled sources situation each pair of controlling and controlled source must be specified in the circuit analysis, but this is not the case in multi-fixators multi-norators case. In the latter case any pairing works as long as the dependency (sensitivity) holds. We may look at this issue differently. As discussed in [3], in a connected circuit a typical two terminal component relies on the circuit by one of its variables, and the other variable (voltage or current) is found through the component characteristic. However, in case of a fixator both variables are specified by the component itself, and in case of a norator both rely on the circuit to be specified. So, any pair of a fixator and a norator, as long as they are mutually sensitive, satisfy the conditions for the circuit analysis, no matter how they pair. This is summarized as:

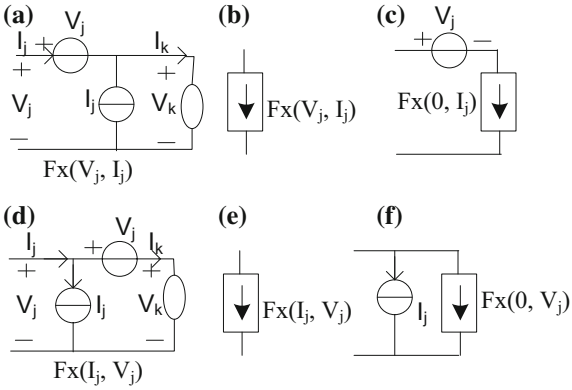

Fig. 1 Fixators; **a** and **b** voltage powered fixator and its symbol; **c** current fixator; **d** and **e** current powered fixator and its symbol; **f** voltage fixator

1. The number of fixators and norators must be equal.
2. Each norator must be sensitive to at least one fixator, and vice versa.

We will further discuss this in the following sub-section.

2.2 *Fixator-Norator Pairs in Linear Circuits*

Let us consider a single pair of FNP in a linear circuit N, as shown in Fig. 2. Because of the circuit linearity we can write

$$i_n = a_0 + a_1 I_f + a_2 V_f + a_3 I_f V_f \tag{1}$$

and

$$v_n = b_0 + b_1 I_f + b_2 V_f + b_3 I_f V_f \tag{2}$$

Ultimately, the impedance function of the norator becomes a bi-linear function of the fixator variables, I_f and V_f, as given in Eq. (3).

$$z_n = \frac{v_n}{i_n} = \frac{b_0 + b_1 I_f + b_2 V_f + a_3 I_f V_f}{a_0 + a_1 I_f + a_2 V_f + b_3 I_f V_f} \tag{3}$$

From Eqs. (1), (2), and (3) we can conclude that a norator can be replace by a current source (or sink) i_n, a voltage source (or sink) v_n, an impedance (resistance, in case of DC) z_n, or even a combination of all these. For example, suppose in a circuit design case, we get $i_n = 50$ μA, and $v_n = 2$ V for a norator. This can result in an equivalent resistor $R_n = v_n/i_n = 40$ KΩ replacing the norator. Alternatively we can replace the norator with a parallel combination of a current source $i_k = 40$ μA and a resistor $r_k = v_n/i_n = 200$ KΩ. This is in fact one of the major issues in biasing design versus performance design in analog ICs. For instance, in designing for an analog

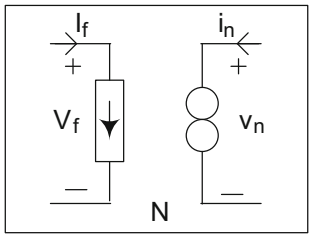

Fig. 2 A fixator-norator pair in a linear circuit N

VLSI circuit, the first choice of $R_n = 40$ KΩ may be considered as the static load, used for biasing a driver. Whereas, the second choice of the resistance, $r_k = 200$ KΩ, can well be taken as the dynamic load for the driver.

The following example demonstrates the relationship between a fixator and its pairing norator in a linear circuit. It also shows how we can find the coefficients a_i and b_i, for i = 0, 1, 2, and 3, given in Eqs. (1) and (2), through simulation.

Example 1 Consider a linearized common emitter amplifier shown in Fig. 3. As design criteria we like to keep $V_{CE} = 2.4$ V and allow 1 mA current to pass through R_5 in excess of the transistor collector current $I_C = \beta I_b$. In the final design, this 1 mA current is what the output load needs to draw from the amplifier. We assign these criteria to a fixator and pair it with a norator replacing R_2 as demonstrated in Fig. 3. We then simulate the circuit for four cases of fixator values: Fx(0, 0), Fx(2.4, 0), Fx(0, 0.001), and Fx(2.4, 0.001). So, there are now four equations and four unknown regarding Eq. (1), and also four equations and four unknown regarding Eq. (2). Solving these equations give us the coefficients a_i and b_i as: $a_0 = 8.00\text{E-}05$, $a_1 = -1.07\text{E-}02$, $a_2 = -1.10\text{E-}05$, and $a_3 = 4.17\text{E-}09$. Similarly $b_0 = 4.01$, $b_1 = 13.4$, $b_2 = 9.90\text{E-}02$, and $b_3 = 0$.

Now for our actual design criteria given in Fx(2.4, 0.001), we simply get $v_n = 4.256006$ V and $i_n = 42.9$ μA, which results in $R_2 = v_n/i_n = 99185.57$ Ω. What it means is that, if we remove the FNP (i.e., the CCVS $h_1 = 10^6$ in the Spice code) from the circuit and replace it with R2 = 99186 Ω we then should be getting the results we asked for, i.e., $V_{CE} = 2.4$ V with 1 mA delivered to the load (not shown here).

In order to test the circuit we first write the code for simulation. The WinSpice component listing is given below. Notice that the resistor R_2 is missing in the list, and instead we are considering a high gain CCVS as an FNP. The way it works is as follows: The V_{CE} is set for 2.4 V according to spec. However, this source must not draw any current because the 1 mA current is already delivered by the current source I_X. Subsequently a CCVS (*h1*) is assigned to provide the voltage necessary for the norator $R_{2(-,\,-)}$, and this controlled source is regulated by the current going through V_{CE}, which must be extremely small.

To test the design, we first remove the fixator and replace it with a 1 mA current source (representing the output load). Next, we replace the norator with a resistor $R_2 = 99186$ Ω. Now, if we simulate the circuit we get exactly $V_{CE} = 2.4$ V across the 1 mA current source.

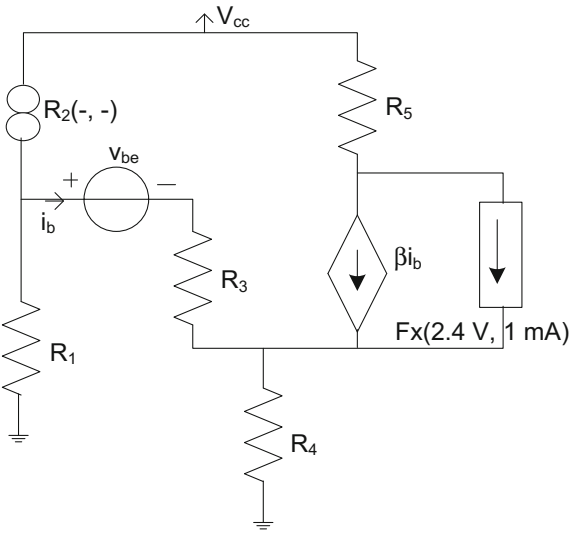

Fig. 3 Linearized CE amplifier for Example 1

The WinSpice component listing is given below.

```
.control
destroy all
op
print I(v2)
print v(1)-v(2)
print (v(1)-v(2))/I(v2)
.endc
.option ITL1=300
*
vcc     1       0       DC      5
vbe     2       3       DC      0.5
ix      5       4       DC      1m
vce     5       4       DC      2.4
v2      1       6       DC      0
R1      2       0       20k
R3      3       4       1.2k
R4      4       0       150
R5      1       5       1.5k
f1      5       4       vbe     100
h1      6       2       vce     1.0e8
*
.end
```

For further verification let us now assume $V_{CE} = 1.5$ V and allow 2 mA current to pass through R_5 in excess of the transistor collector current $I_C = \beta I_b$. Now, since we already have found the coefficients a_i and b_i in Eqs. (1) and (2) we do not need to use FNP anymore, and instead, we directly calculate the new $v_n = 4.18$ and $i_n = 42.2$ μA from Eqs. (1) and (2). This results in $R_2 = v_n/i_n = 99160$ Ω. Finally, if we now replace the older $R_2 = 99186$ Ω with this new one, $R_2 = 99160$ Ω, and

simulate, we get the desired criteria, i.e., $V_{CE} = 1.503759$ V and 2 mA excess of the collector current, as we expected. This concludes our example.

For multiple FNPs situation the case is extended and Eqs. (1) and (2) are represented by matrix equations. However, the impedance z_n is still bi-linearly dependent on as many fixators as the corresponding norator is sensitive to. As it has been shown [3] (in a typical circuit analysis using analytical methods) there is no need to pair the fixators and norators, and the nodal admittance matrix analysis will take care of all FNPs collectively.

Commercially available circuit simulator do not have the capability to incorporate FNPs directly into a nodal analysis. This is why we need to manually replace each FNP with a controlled source that has very high gain. The next question is, how to pair them and put them into controlled sources? To answer the question, we first need to find good matches (based on maximum sensitivity) between the fixators and the norators, and make them pairs. As experiments show, this is not a hard requirement, because pairing is not unique; any setting as long as rule 2 above applies is valid. Then, after paring, each FNP can be temporarily replaced with a dependent source with high gain. The type of controlled source being used depends on the fixator-norator relationship. For a *voltage* fixator the norator is replaced with a CCVS or CCCS, and for a *current* fixator the norator is replaced with a VCVS or VCCS. Now the circuit so prepared is ready for simulation. Among others, the simulation provides the currents i_n and the voltages v_n of the norators. Then, just like what we discussed earlier (Eqs. (1), (2), and (3)), each norator can be replaced with (a) a current source i_n, (b) a voltage source v_n, (c) an impedance z_n, $= v_n/i_n$, or (d) a combination of all this. Finally, all fixators are also removed from the circuit.

Now, before we move into applications we need to know the rules of engagement with FNPs in circuits. Here are some of these rules in relation to other circuit components.

2.3 Rules Governing Fixators and Norators

A fixator represents a current source and a voltage source combined; hence, its rules must comply with both. For instance, a current source in series with a fixator may violate KCL, and a voltage source in parallel with a fixator may violate KVL. In general, a cutset of fixators with or without current sources may violate KCL and a loop of fixators with or without voltage sources may violate KVL.

A cutset of norators with or without current sources and fixators are not all independent, and a loop of norators with or without voltage sources and fixators are not all independent either.

Here are some other properties of the pair:

- A fixator Fx(V, I) consumes power, and the power consumed is P = V*I.
- A resistor R in series with a fixator Fx(V, I) is absorbed by the fixator and the fixator becomes Fx(V_1, I); where $V_1 = V + R*I$. A resistor R in parallel with a fixator Fx(V, I) is absorbed by the fixator and the fixator becomes Fx(V, I_1); where $I_1 = I + V/R$.
- A current source I_S in parallel with a fixator Fx(V, I) is absorbed by the fixator and the fixator becomes Fx(V, I_1); where $I_1 = I + I_S$.
- A voltage source V_S in series with a fixator Fx(V, I) is absorbed by the fixator and the fixator becomes Fx(V_1, I); where $V_1 = V + V_S$.
- A current source in series with a norator absorbs the norator with no change; and a voltage source in parallel with a norator absorbs the norator with no change. In addition, a current source in parallel with a norator is absorbed by the norator; and a voltage source in series with a norator is absorbed by the norator.
- A resistor in series or in parallel with a norator is absorbed by the norator.
- A norator in series with a fixator Fx(V, I) is equivalent to a current source I; and a norator in parallel with a fixator Fx(V, I) is equivalent to a voltage source V.

3 Use of FNP in Biasing Design

A major property of a fixator is to keep the DC values (voltage and current) fixed when assigned to a circuit port. We can use this property to bias the transistors in a circuit according to a specified operating (Q) point. Figure 4 shows the biasing models of diodes, BJT and MOS transistors using fixators. There are two types of models for each. Figures 4a, c, and e show the *linearized models*, whereas Figs. 4b, d, and f show the *actual modes of fixators*. There are distinct differences between the two. In the linearized model we are assuming both voltage and current for each port as being known and according to the transistor characteristics. In this situation we are locked with the type of the transistor that is specified for the design, and in case this transistor is replaced with another one, with different characteristics, then the fixator model is no longer accurate. On the contrary, the actual model of the transistor specifies only one variable (voltage or current) for each port and the other variable is found through the transistor operation and according to its characteristics. Hence, any change in the circuit components (including different transistors) will keep the biasing intact. However, the price we need to pay for using the actual model is its nonlinearity, which means we need to go through iterations when we simulate the circuit.

Example 2 Consider a three stage BJT amplifier with feedback, shown in Fig. 5a. The amplifier is broadband known as MC1553 [4]. All components of the amplifier are assumed given, as listed in the following SPICE program, except for R_1 and R_7, which are kept unknown for biasing design purposes. There are two design specs to

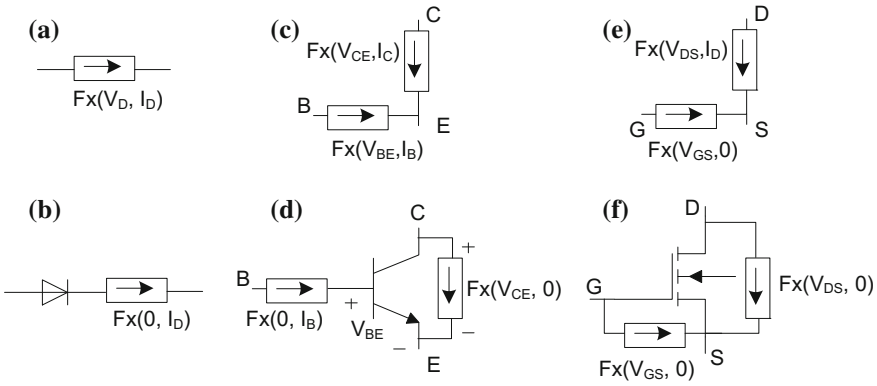

Fig. 4 Two types of biasing models; **a** and **b** diodes; **c** and **d** BJT transistors; **e** and **f** MOS transistors

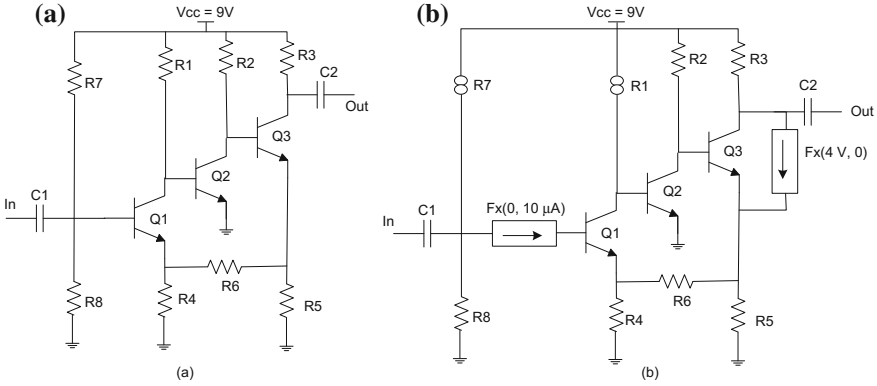

Fig. 5 Three stage BJT amplifier with feedback, known as MC1553; **a** the original amplifier; **b** biasing design using FNPs

consider here. First, for a proper operation of the amplifier with $V_{CC} = 9$ V we need to get a maximum output voltage swing close to 8 V; hence, we assign $V_{CE3} = 4$ V. This is for the collector-emitter voltage of Q_3. Second, we select to limit $I_{B1} = 10$ μA, which is the base current of Q_1. This current is almost half of the current going through R_8, and it is sufficient to provide a stable biasing condition for the first and the critical stage of the amplifier. Figure 5b shows the design set up using two FNPs. Notice that the norators are replacing the unknown resistors R_1 and R_7, as planned.

```
*** mc1553.cir *** from the data sheet
*** three stage npn amplifier with feedback (Sedra and Smith, 7th Edition, p. 851) ***
*
.control
destroy all
op
print (v(10)-v(2))/I(v1)
print (v(10)-v(3))/I(v2)
.endc
.option ITL1=300
*
vcc     10      0       DC      9
vin     1       0       DC 0    sin(0 60m 10k 0 0 0)
q1      3       8       4       BJT1
q2      5       3       0       BJT1
q3      6       5       7       BJT1
R2      10      5       5k
R3      10      6       500
R4      4       0       150
R5      7       0       80
R6      4       7       1k
R8      2       0       50k
c1      1       2       1u
*
ib1     2       8       DC      10u
vce3    6       7       DC      4
v1      10      a       DC      0
v2      10      b       DC      0
e1      a       2       2       8       1.0e3
h3      b       3       vce3    1.0e6
*
***** Spice models and macro models *****
...
...
.end
```

We next simulate the circuit and get the values for the unknown resistors. The WinSpice results are given below, and as indicated we get $R_1 = 2.985838e + 05$ or rather 300 KΩ, and $R_7 = 9.316896e + 03$ or 9.3 KΩ.

```
Circuit: *** mc1553.cir *** from the data sheet
TEMP=27 deg C
DC Operating Point ... 100%
(v(10)-v(2))/v1#branch = 2.985838e+05
(v(10)-v(3))/v2#branch = 9.316896e+03
```

Our next step is to test the circuit so designed. To do this, we remove the fixators, which means short circuit Fx(0, 10 μA) and open circuit Fx(4 V, 0), and replace the norators with R_1 and R_7 that were found. We then run the circuit for the transient analysis. The simulation result is shown in Fig. 6 with almost no distortion.

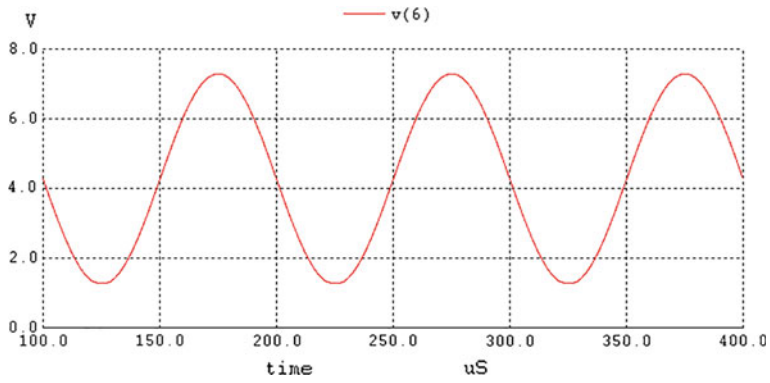

Fig. 6 Transient response of the amplifier in Example 2, designed for biasing

4 Designing for Gain, and Input and Output Impedances

Another application of FNP is in designing for AC performance of amplifiers. This includes the gain, input, and output impedances. The following example demonstrates one such application.

Example 3 Consider a single stage CMOS 50 nm process amplifier shown in Fig. 7a. The desired design criteria for this amplifier are: voltage gain $A_v = 25$ or higher; input and output impedances, R_{in} and R_{out}, in the range of 0.5 MΩ; maximum undistorted output voltage swing of V_{out}. Note that from the four specs, the first three (A_v, R_{in} and R_{out}) are related to the performance design, and the last one is bias-related spec. For the performance design we get:

$$R_{out} = r_{01} \| r_{02} \tag{4}$$

$$A_v = -g_{m1} R_{out} \tag{5}$$

$$R_{in} = R_1 \| (R_2 + R_3) \tag{6}$$

Where, r_{o1} and r_{o2} are the output impedances of the MOS transistors. Hence, for $R_{out} = 0.5$ MΩ we need to have each transistor to have an output impedance in the range of 1 MΩ. Similarly, from Eq. (5), and by assuming $A_v = 25$, we must have the trans-admittance for the driver $g_{m1} = 50$ μA/V or higher. The same is true for the biasing resistors, i.e. R_1, R_2 and R_3 must be in the range of 1 MΩ in order to satisfy $R_{in} = 0.5$ MΩ.

To fulfill the last criteria, i.e., to maximum the output voltage swing, we need to have the biasing to produce $V_{DS1} = V_{out} = V_{DD}/2 = 0.5$ V. This is done by using a FNP, where the fixator keeps $V_{DS1} = 0.5$ V and the norator replaces R_2 shown in Fig. 7b. For simulation purposes, we assume $R_1 = R_3 = 1$ MΩ, and the FNP is replaced with a high gain CCVS. The simulation produces $v_{R2} = 0.396$ V and

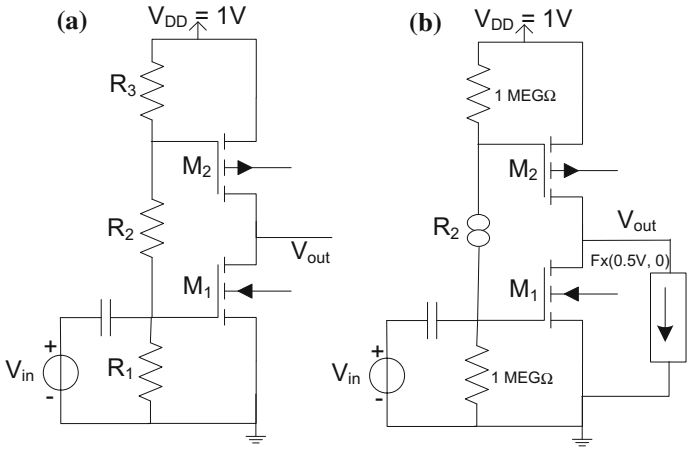

Fig. 7 A single stage CMOS amplifier, **a** amplifier structure, **b** biasing design procedure using an FNP

$i_{R2} = 0.3$ μA for the norator, which means we can replace the norator with a resistor $R_2 = 0.396/0.3 = 1.3$ MΩ.

We now need to select the right sized transistors. Following the performance design with the trans-admittance g_{m1} in the range of 50 μA/V, and the output impedances r_{oi} (i = 1 and 2), as specified, the closest choices for the transistors' sizes are: W/L = 50/2 for the nMOS driver and W/L = 100/2 for the pMOS active load. Finally, after complete design of the amplifier, the circuit is simulated and the results achieved are: $A_v = 27$, $R_{in} = 697$ KΩ, $R_{out} = 360$ KΩ, and $V_{out} = 0.5$ V that are reasonably within the range of the design specs. This concludes our example.

It is important to note that, although a circuit design can start with a number of specific requirements that we try to fulfill them all but there might be cases that some of the requirements conflict each other. This is needed to be paid special attention to. For instance, in Example 3 we found $R_2 = 1.3$ MΩ from the biasing criteria. Another way to find R_2 is through the input impedance. For example, instead of $R_{in} = 697$ KΩ let us assume $R_{in} = 600$ KΩ, which is closer to our desired value of 500 KΩ. Now from Eq. (6) we get $R_2 = 500$ KΩ. By far this is smaller than 1.3 MΩ, the one previously found. One solution to these types of problems is to assume two values for such a resistor, one static for DC biasing and another one dynamic resistance for AC operations. For example, in this case, we assume $R_2 = 500$ KΩ for the DC (biasing), and another one $r_2 = 1.3$ MΩ for the AC (performance) design. We will further discuss this issue in a later section.

Example 4 We are going to revisit the same three stage amplifier MC1553 discussed in Example 2 (Fig. 5a). The amplifier is already designed for biasing and the transistors used are of type 2N3904. The objective now is to redesign the amplifier for (AC) performance according to certain given criteria. Figure 8 shows a

linearized equivalent circuit of the amplifier. For this design we consider three criteria as follows: (a) the input resistance needs to be high and around $R_{in} = v_i/i_i = 10\ M\Omega$; (b) the gain obtained from the two first stages is aimed at $A_2 = v_2/v_i = 8$; and (c) the overall amplifier voltage gain is aimed at $A_{out} = v_{out}/v_i = 60$. Because of the three design criteria specified we need to apply three FNPs. One set of components to replace with three required norators can be R_1, R_3, and R_{C2}. Other choices of components are also possible, as well. Figure 9 shows the small signal equivalent circuit of the amplifier after three FNPs are added to the circuit. Table 1 shows the component values of the amplifier except for the three unspecified resistors R_1, R_3, and R_{C2} that are replaced with the norators.

After simulating the circuit the unspecified resistors are computer as shown below:

$R_1 = 96\ \Omega$

$R_3 = 85\ \Omega$

$R_{C2} = 4.617\ K\Omega$

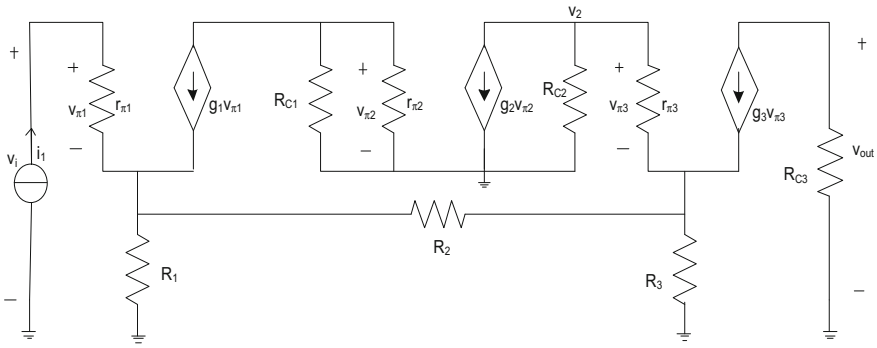

Fig. 8 Small signal equivalent circuit of the three stage amplifier MC1553, in Fig. 5a

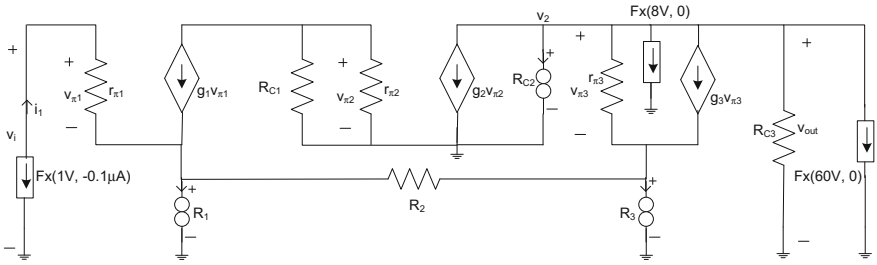

Fig. 9 Three FNPs used for the design of MC1553 amplifier; $v_i/i_i = 10\ M\Omega$; $v_2/v_i = 8$; $v_{out}/v_i = 60$

Table 1 Component values for the amplifier

R_{C1} KΩ	R_{C3} Ω	R_2 Ω	$r_{\pi 1}$ KΩ	$r_{\pi 2}$ KΩ	$r_{\pi 3}$ Ω	g_1 mS	g_2 mS	g_3 mS
9.0	600	640	4.18	2.7	750	36	70	293

Next, we need to verify the results again. To do this we first remove the fixators and then replace the norators with the three resistors found. The circuit is now ready for performance simulation. The current source i_1 is the only signal source in the circuit and we can assign $i_1 = 10^{-8}$A. The simulation results are then obtained as: $v_1 = 0.1$ V, $v_2 = 0.8$ V, and $v_{out} = 6$ V. If we now translate these into the design criteria we get $R_{in} = 10$ MΩ, $A_2 = 8$ V/V, and $A_{out} = 60$ V/V, as expected. This concludes our example.

Before we leave this example, however, it is important to realize that the linearized AC solution is valid only if the transistors operate at the (active) regions, as modeled. To check this we need to replace the models with actual transistors and re-run the simulation with the biasing supplies included. In this particular case we had the biasing completed successfully in Example 2, and all transistors were in the active regions. However, in general, any performance design of an amplifier must include both DC and AC criteria fulfilled, i.e., we need to perform both to be sure of accuracy.

Algorithm 1 provides a step-by-step procedure that leads to designing an amplifier for a set of specified criteria.

Algorithm 1:

1. Given a set of design specs for an amplifier, a designer needs to go through certain initial assumptions that form the overall circuit configuration (topology) before starting a formal design procedure. For example, the designer may need to specify the number of amplifier stages, and characterize each stage in terms of types (CE, CS, …). The next assumption the designer can make is to assume the region of operation of each transistor for biasing purposes, and so on.
2. Following the selection of the transistors and their operating regions we are dealing with two types of circuits. One for the biasing design, which is the circuit with all the original components present, including the transistors. Another circuit is for the performance design. In the later case the transistors are replaced with their small signal linear models. The DC sources are removed, the coupling capacitors are short circuited, and the inductors are removed. In case a region of operation is selected to be outside of the active region for a BJT, or outside of the saturation region of a MOS transistor, then the designer can still replace the component with the appropriate linear model, as long as the region remains unchanged during the AC operation. This step produces a complete linearized circuit for AC design.

3. Next, the designer needs to split the design criteria into two categories: biasing (DC) and performance (gain, I/O impedances, and so on). For n number of (DC or AC) design criteria the designer needs to allocate n components in the circuit to pair with the n design criteria. The n design criteria are set by using appropriate fixators, and the n paring components are replaced with norators.
4. The next step is to pair fixators and norators and replace each pair with a controlled source with high enough gain. The type of the controlled source used is discussed in Sect. 2.2.
5. The circuit so created is simulated next, and the result of the simulation provides the voltage and current for each norator.
6. These norators are then replaces with a voltage source, a current source, a resistor, or a combination of them, as appropriate. Finally, the fixators are removed from the circuit and the circuit so constructed can be tested for verification.

Example 5 Consider a CMOS differential pair with buffer shown in Fig. 10. The initial design criteria for this amplifier are given in Table 2.

The transistors for this example are considered long-channel with L = 2 μm channel lengths, and their major SPICE model parameters are given in Table 3.

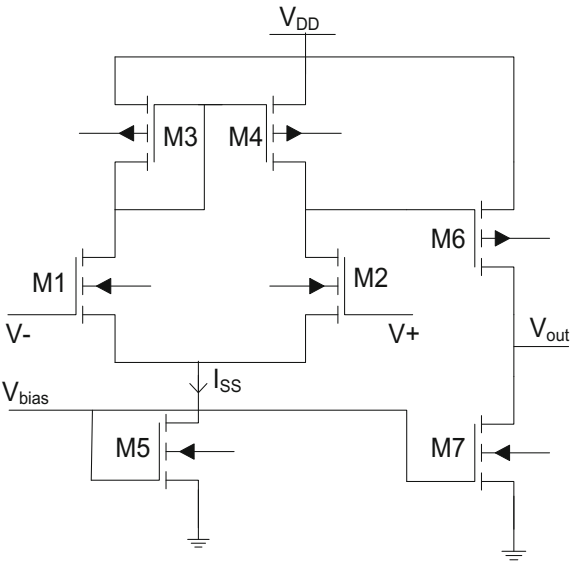

Fig. 10 A CMOS differential pair with buffer for Example 5

Table 2 Initial design criteria for the amplifier

V_{DD} V	I_{SS} μA	V_{Out} V	A_v dB	CMRR dB
5.0	150	2.5	74	86

Table 3 MOS transistor parameters

	K'_P $\mu A/V^2$	V_{Th} V	Lambda V^{-1}	Gamma $V^{1/2}$
nMOS	25	0.75	0.0133	0.76
pMOS	9.3	−0.83	0.0133	0.76

We first need to take some initial steps to simplify the design. (1) The transistor M_5 must carry $I_{SS} = 150$ μA; so we need to decide on its channel width W_5, and its bias voltage $V_{bias} = V_{GS5}$. For this we assume $W_5 = 20$ μm, and then calculate the biasing voltage which is $V_{bias} = 1.1$ V. (2) Next, we need to balance the operation of M_6 and M_7 to achieve $V_{Out} = 2.5$ V. This is to maximum the output swing, as another criterion. With the assumption of $W_7 = 20$ μm and $W_6 = 3*W_7$ we get the gate voltage values $V_{SG6} = V_{SG3} = 1.16$ V. Up to here the design criteria have helped us to find the operating (biasing) voltages for the transistors, except for M_1 and M_2 and their paring transistors M_3 and M_4. By the assumption that I_{SS} is equally split between M_1 and M_2, and since we already have the width W_5, we can simply find $W_1 = W_2 = W_5/2 = 10$ μm. Finally, we get $W_3 = W_4 = 3*W_1 = 30$ μm. This concludes our biasing design.

For the performance design, however, we have two criteria to fulfill that are (1) the differential gain 74 dB or $A_d = 5$ K V/V, and (2) the targeted CMRR = 86 dB. To further simplify the design, we notice that the later criterion can be treated as $CMRR = A_d/A_c$, which results in $A_c = 0.25$ V/V. The next step is to create a linearized AC equivalent circuit for the amplifier, which its schematic is given in Fig. 11. Here the transistors are replaced with their linear small signal models. Notice that the transistors' body effect are also included in the schematic.

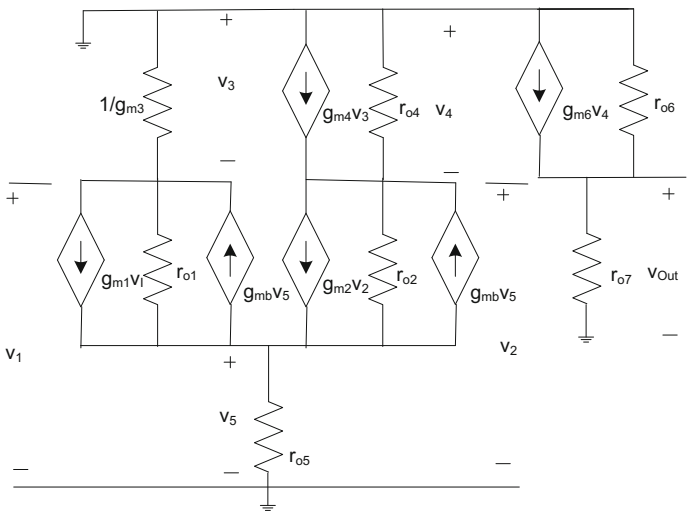

Fig. 11 Linearized CMOS differential pair

Now we have two steps to go, one to fulfill the differential gain $A_v = 5$ K, and the second one to handle the common-mode gain $A_c = 0.25$ V/V. This means we need to use FNP methodology in two separate incidences. For the first step we know that $A_v = g*R_o$, where g is the overall trans-conductance of the differential pair, and $R_o = r_6 \,||\, r_7$ is the generic output load. So, to produce the differential gain $A_v = v_{out}/v_d = 5$ K we first apply $v_d = 100$ μV to the input port, and then assign a fixator Fx(0.5, 0) at the output port. Then to pair with this fixator we remove both r_6 and r_7 from the circuit (Fig. 11) and replace them with a norator. The WinSpice code listing of the design is shown below.

```
.control
destroy all
op
print v(6)/I(va)
.endc
.option ITL1=300
v1          1     0     DC      100u
v2          2     0     DC      0
r1          3     5     1.0Meg
r2          4     5     1.0Meg
r3          3     0     7k
r4          4     0     1.0Meg
r5          5     0     0.5Meg
g1          3     5     1       5       137u
g2          4     5     2       5       137u
gb1 3       5     0     5       14u
gb2 4       5     0     5       14u
g4          4     0     3       0       145u
g6          6     0     4       0       290u
*
vo          0     6     DC      0.5
va          6     a     DC      0
h1          a     0     vo      1.0e6
.end
```

The code is simulated and the result of the simulation is shown below.

```
Circuit: *** L-MOS-DA.cir
TEMP=27 deg C
DC Operating Point ... 100%
v(6)/va#branch = 2.007606e+05
```

Note that the simulation is producing $R_o = 2.007606e + 05\ \Omega$, or equivalently, $r_6 = r_7 = 0.4\ M\Omega$, which are not far from the actual transistors' output impedances of 0.5 MΩ.

Finally, we need to get the common-mode gain of $A_c = 0.25$. Initially, it seems unnecessary to further proceed with the design; because there is no parameter left to be calculated. One way to deal with this issue is to make some modifications in the circuit topology, if needed. Thus, we first check for the common-mode gain as the design is setup, and in case the gain exceeds well above the target value (reducing the CMRR) then we need to replace M_5 with a cascade current mirror [5]. However,

Table 4 The transistor widths for the differential amplifier

M_1 μm	M_2 μm	M_3 μm	M_4 μm	M_5 μm	M_6 μm	M_7 μm
10	10	30	30	20	60	20

the calculated common-mode gain for this design stays at $A_c = 0.31$, which is within the acceptable tolerance. Therefore, there is no need to make changes in the overall circuit topology.

Nevertheless, in case one desires to attempt for correcting $A_c = 0.31$, the way to do this is to apply, for example, $v_1 = v_2 = 1$ V to the input port and then assign a fixator Fx(0.25, 0) to the output port for getting $A_c = 0.25$. Then to pair a norator with this fixator we may remove r_5 from the circuit (Fig. 11) and replace it with a norator. The result of the simulation provides the voltage and currents of the norator, which in turn produces a newly computed r_5.

This concludes the design of the differential amplifier, with the transistors widths given in Table 4.

5 Designing Active Load and Current Mirrors Using FNP

As we discussed in Sect. 2, a norator can be replaced with a current source, a voltage source, an impedance, or a combination of those. For example, let us assume we get $I_j = 42$ μA and $V_j = 308$ mV for a norator in a circuit simulation that contains FNPs. Let us further assume that this norator is replacing a current mirror or an active load located in an analog IC. For DC operation, this norator conducts power to properly bias the driver(s) in the circuit and can be represented by a resistor $R_j = 308/42 = 7.33$ KΩ. At the same time this norator is replacing a dynamic load in an AC analysis of the circuit, and it can perhaps be represented by a parallel combination of a current source $I_j' = 36$ μA and a resistor $r_j = 308/6 = 51.3$ KΩ, as illustrated in Fig. 12a. The i-v characteristics of the norator for both cases are given in Fig. 12b. This simply means that a component substituted for the norator can be a BJT or MOS transistor, as an active load or current mirror, with the dynamic resistance $r_j = 51.3$ KΩ, where the transistor is biased at the operating point $I_D = I_j = 42$ μA and $V_{DS} = V_j = 308$ mV. This is depicted in Fig. 12c, with the static load R_j and the dynamic load r_j displayed.

This example leads us to the solution of a loading problem in analog IC where the static (DC) load for biasing is different from the dynamic one. In general there are different types of dynamic loads commonly used in IC designs. Figure 13 shows three basic types of dynamic loads used in MOS ICs, and Fig. 14 are those typically but used in BJT ICs. As noticed in Figs. 12 and 13, active loads or current mirrors[1]

[1]Active loads and current mirrors are similar in construction, and are used interchangeably. Here we only refer to them as active loads.

are constructed from one or more MOS or BJT ICs. Depending on their structure and the region of operation active loads are of three types.

Type L: Type L is a low impedance active load, shown in Figs. 13a and 14a. In its basic structure a type L load is a diode-connected BJT or MOS transistor used mainly for voltage drops. The dynamic resistance of a Type L is $r_j = 1/g_m$, for MOS and $r_e = r_\pi/(1 + \beta)$ in case of a BJT.

Type R: Type R is a resistive active load. A type R active load represents a biased BJT or MOS transistor operating in the triode (for MOS) or in the saturation (for BJT) region with static resistance of $R_j = V_j/I_j$, as shown in Figs. 13b and 14b. The dynamic resistance r_j of this type of load is practically equal to the static resistance R_j. A typical lumped resistance can also be considered as a Type R load.

Type H: Type H is a high impedance active load. A type H active load is a biased BJT or MOS transistor operating in the saturation (for MOS) or in the active (for BJT) region with high dynamic resistance of $r_j = r_o$. Note that Figs. 13c or 14c represents only a simple and basic structure of a high impedance active load. Other active loads such as cascodes or folded cascodes structures are also commonly used [5]. For example, Fig. 15 shows two samples of a cascode current mirror and a cascode active load.

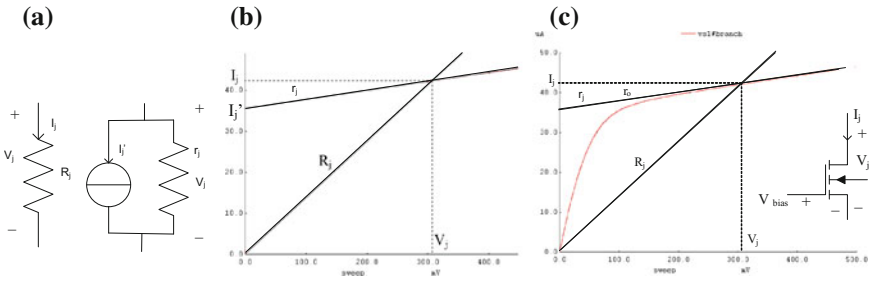

Fig. 12 **a** Passive (DC) and active (AC) load representation; **b** graphical representation; **c** circuit construction with MOS

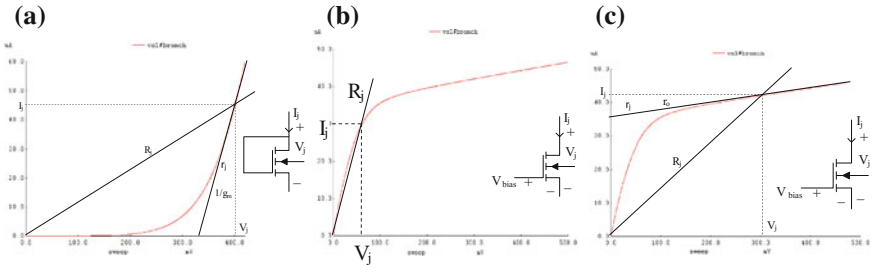

Fig. 13 Active load designs; **a** Type L active load; **b** Type R active load; **c** Type H active load; **d** Main design parameters in an active load; **e** cascode current mirror/active load

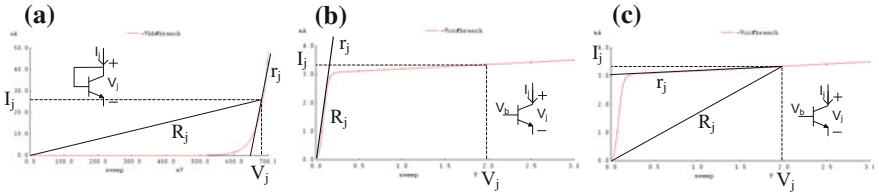

Fig. 14 Active load designs; **a** Type L active load; **b** Type R active load; **c** Type H active load; **d** Main design parameters in an active load; **e** cascode current mirror/active load

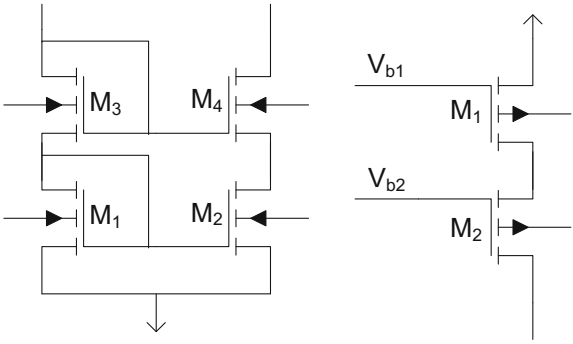

Fig. 15 Active load designs; **a** Type L active load; **b** Type R active load; **c** Type H active load; **d** Main design parameters in an active load; **e** cascode current mirror/ active load

5.1 Active Load Design

Designing for active loads can be a challenging issue. As mentioned earlier, one needs to consider both DC (biasing) and AC (performance) criteria for the design. For a frequent designer it might pay off to form a library of active loads before designing for analog ICs. A typical library contains three lists of parameters for each type of active load (L, R or H), and for each type of transistors, MOS or BJT. Each active load in a type is identified by its circuit structure (typically one or more MOSs or BJTs in series), and its three design parameters, V_j, I_j, and r_j are specified. This library can be created first, so that for a given set of parameters (V_j, I_j, and r_j) the designer can simply look up and select one that fits with the design specs. In fact, depending on the type of technology, component size, and the level of complexity (single, multiple, cascode and so on) the construction of such a library can be expanded to include other design criteria such as the frequency spectrum, noise characterization, and power consumption.

The next question pertaining to this issue is how to extract the set of specified parameters (V_j, I_j, and r_j) for an active load, in a given IC design environment? In other words, how the circuit performance criteria (gains, bandwidth, impedances, and so on) can be translated into the right selections of the dynamic loads r_i? Similarly, how the selective operating points for the drivers can result in right selections of V_j, and I_j for the active loads? Let us just consider one criterion. For

the dynamic resistances (r_j), we can typically extract them from the I/O impedances or the gain that we need. For designing a circuit for its performance, each transistor is replaced with its small signal model, and each active load is replaced with its dynamic resistance r_j. Now, since the entire AC circuit is linear, finding all r_j values that we need for active loads is rather simple and a matter of linear circuit analysis. In case FNPs are candidate to help, each fixator secures a design spec while its pairing norator takes the location of a dynamic load in the circuit. After the performance design is done we can start the biasing design. Circuit biasing must be performed in order to find the other two parameters, V_j and I_j for the active loads. Here again FNPs come into play. Then for each fixator holding a biasing criterion (V_b and I_b) a norator provides a pair of V_j and I_j, that represents a voltage supply, a current supply, or a power conducting component (PCC). Hence, with V_j and I_j being found through the biasing and r_j coming from the performance design, one can completely characterize an active load, or look it up in the active load library just described.

6 Designing Analog VLSI Circuits

Design of high performance analog circuits can be a complex and often a multi stage process. One approach, to simplify the design and cut loops and feedbacks between the stages, is to use as much orthogonally between the stages as possible [6]. In the proposed method this orthogonality is practiced between the circuit performances and the biasing; or simply between AC and DC designs. The first task clearly is to design for the circuit performances; mainly gain, input and output impedances, noise, signal power, and bandwidth. The process starts with a selected circuit topology, and then selecting regions of operations for the nonlinear components so that the design requirements can be achieved. The next step in the design process is two folded: (i) bias the circuit with DC supplies (voltages and currents) so that the selected operating points for the (driving) transistors are well established, and (ii) complete the DC design of the active loads that have been already selected for the performance design. The following examples show this design procedure using FNPs.

Example 6 Consider a CMOS differential amplifier partially shown in Fig. 16a. All known component values including the transistors' sizes are listed in the following WinSpice code. We start designing the amplifier for a differential gain of $A_v = v_{out}/v_{in} = 200$ V/V. To do this we first use a fixator Fx(0.2 V, 0) at the output port to keep the output $v_{out} = 0.2$ V for an input signal of $v_{in} = v_+ - v_- = 1$ mV already assigned. The pairing norator, on the other hand, is chosen to replace the resistor R_b, as shown in Fig. 16a. Now the circuit is ready for simulation, and for that the FNP is replaced with a VCVS as indicated in the SPICE listing. For transistor sizing we are assuming a constant channel length of $L = 1$ μm. The width of the

transistors are all related. For V_{GS} close to 1 V and the reference current about $I_R = 27$ mA the transistor widths W come about the values listed in the Spice code.

```
*** CMOS Diff-Amp ***.
.control
destroy all
op
let r1 = v(7)-v(6)
print r1
print I(vr)
print r1/I(vr)
.endc
.option ITL1=300
vdd     10      0       DC      2.5
vss     0       20      DC      2.5
v1      2       1       DC      1.0e-3
M1      3       1       5       10      P_1u    L=1u    W=60u
M2      4       2       5       10      P_1u    L=1u    W=60u
M3      5       7       10      10      P_1u    L=1u    W=120u
M4      3       6       20      20      N_1u    L=1u    W=20u
M5      4       6       20      20      N_1u    L=1u    W=20u
M6      7       7       10      10      P_1u    L=1u    W=60u
M7      6       6       20      20      N_1u    L=1u    W=20u
vo      3       8       DC      2.0e-01
ro      8       4       10MEG
vr      7       a       DC      0
e1      6       a       8       4       1.0e6
*
.include cmosedu_models.txt
*
.end
```

The results from the simulation are listed below, where V_b, $= 3.11166$ *V*, $I_b = 2.736193e\text{-}05$ *A* are given for the norator that can be replaced with a resistor $R_b = 1.137223e + 05\ \Omega$, or simply $R_b = 114$ KΩ. The final differential amplifier is shown in Fig. 16b.

```
WinSpice 1 -> source "MOS-OpAmp1.cir"
Circuit: *** CMOS OP-Amp ***.
TEMP=27 deg C
DC Operating Point ... 100%

r1 = 3.111660e+00
vr#branch = 2.736193e-05
r1/vr#branch = 1.137223e+05
```

Example 7 The objective here is to design a three stages CMOS 50 nm process OP-Amp with the performance criteria given as follows: (i) the overall open-loop voltage gain is set to 77 dB (6,500 V/V), (ii) the input impedance is supposed to be high, and (iii) the output impedance of $R_{out} = 10$ KΩ [5]. An initial configuration

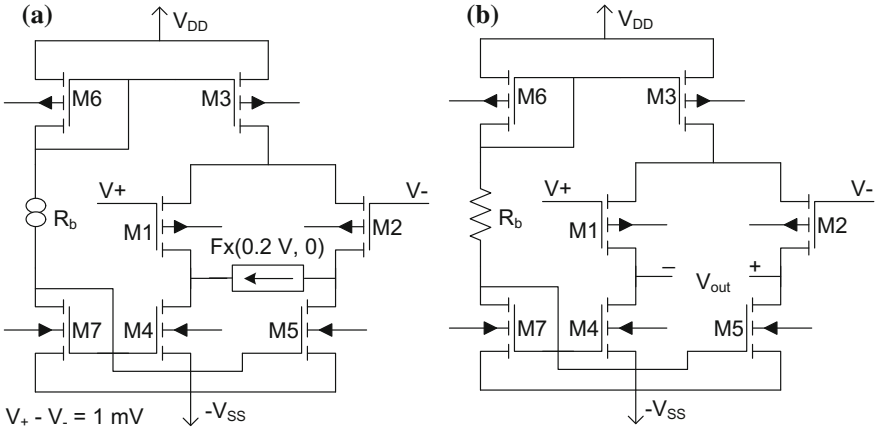

Fig. 16 CMOS differential amplifier; **a** the amplifier with an FNP added; **b** the amplifier after the design is completed

of the amplifier is shown in Fig. 17 with the active loads (AL) and the current mirrors (CM) unspecified. In scale of 50 nm process the nMOS drivers (M_1, M_2, M_3 and M_4) are sized at W/L = 50/2, and the pMOS driver, M_5, is sized at W/L = 1000/2, for greater current delivery. Table 5 provides a biasing specification for the amplifier.

Practically there are only five biasing criteria in Table 5, namely V_{out}, V_{DS1}, V_{DS3}, I_1 and I_3, that need to be fulfilled vs the seven active loads and current mirrors that are going to be designed, instead. One way to solve this unmatched situation is

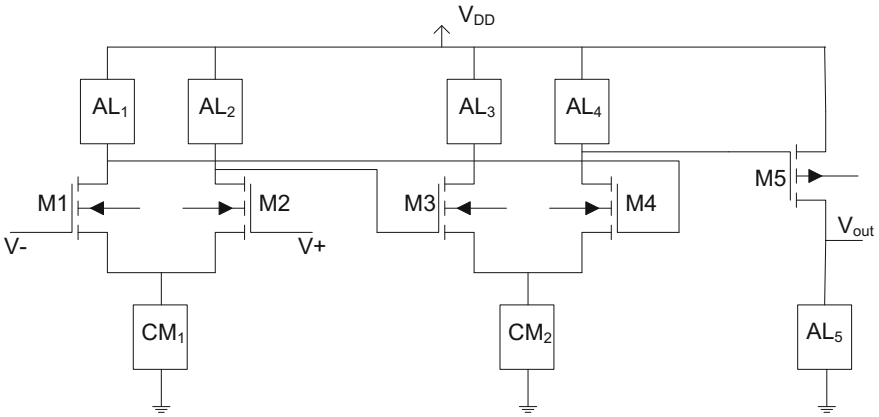

Fig. 17 Symbolic structure of a three stages CMOS OP-Amp with the active loads and current mirrors unspecified

Table 5 Biasing criteria for the Op-Amp

V_+ V	V_- V	V_{out} V	I_1 μA	I_3 μA	V_{DS1} V	V_{DS3} V	V_{DD} V
0.5	0.5	0.5	3.4	3.8	0.5	0.34	1.0

to use the symmetry that exist in the differential pairs, and hence, reduce the size of the biasing circuit to the one shown in Fig. 18. Notice that the current mirrors CM_a and CM_b carry half the currents going through the original mirrors CM_1 and CM_2, respectively.

To start the design, we notice that the current mirrors CM_a and CM_b can be initially replaced with two current sources $I_1/2$ and $I_3/2$. This is quite consistence with the design procedure that is aimed for high impedance current mirrors. Later, when the voltages across the current sources are found these current sources can be replaced with appropriate (nMOS) current mirrors. Now the biasing design is quite simplified, and the design can be proceed with only three FNPs, as depicted in Fig. 19.

Next, the DC circuit so created is simulated. The simulation results given for the active loads and the current mirrors are listed in Table 6. Table 6 also provides the static and dynamic resistances of the components, as indicated in Fig. 13. As described in Algorithm 1, the dynamic resistances are obtained through the linear analysis of the original amplifier of Fig. 17 (not shown here). This is when the drivers are replaced with their linear models and the active loads and current mirrors are replaced with their dynamic resistances so that the circuit can perform according to the AC performance criteria (gain and output impedance) specified.

Before getting into the final stage of the design, note that the biasing design can go with different sets of specs. For instance, the design criteria V_{DS1}, given in Table 5, can be replaced with the buffer current I_5 in Fig. 18, i.e., instead of having

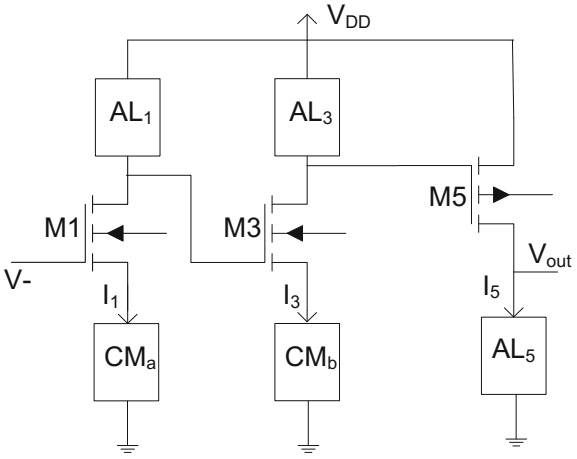

Fig. 18 The reduced DC biasing structure for the CMOS OP-Amp

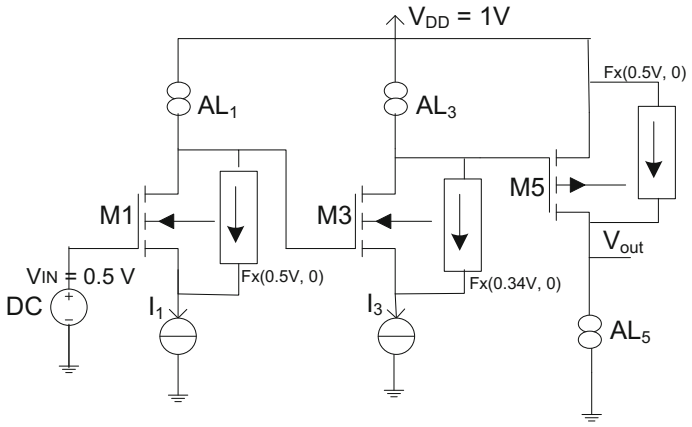

Fig. 19 Use of FNPs for the biasing design of the CMOS OP-Amp

Table 6 Active loads charactrization table

Active loads	DC voltage mV	DC current μA	DC Res. KΩ	AC Res. KΩ	Load type
AL_1	330	3.4	97	7.9	L
AL_2	330	3.4	97	764	H
AL_3	340	3.8	90	7.3	L
AL_4	340	3.8	90	1350	H
AL_5	500	172	2.9	10	H
CM_1	170	6.8	25	84	H
CM_2	290	7.5	39	98	H

$V_{DS1} = 0.5$ V, as a biasing criterion it can be replaced with $I_5 = 100$ mA as an alternative criterion. To verify the design a simulation is conducted with this new setting and the results closely confirm with the previous results (not given here for space limitation).

Finally, with all the parameters found through the simulation, the active loads can be designed (or looked up in the table) for the Op-Amp. In conclusion, Fig. 20 shows the CMOS Op-Amp that is designed after the active loads and current mirrors are included in the design. Table 7 also provides the transistors sizes for the active loads and the current mirrors. For the transistor sizing the channel length is selected as $L = 100$ nm. The transistor widths are all related, and for the design specs given the *Ws* are found, as listed in Table 7, in 50 nm.

The next step is to verify the results by applying the transient analysis to the amplifier. Figure 21 is the open loop transient response of the amplifier. Notice that with $V_{out,p\text{-}p} = 0.9$ V the distortion is almost negligible. Also, note that the DC off-set voltage for the output remains at 0.5 V, as specified by the design.

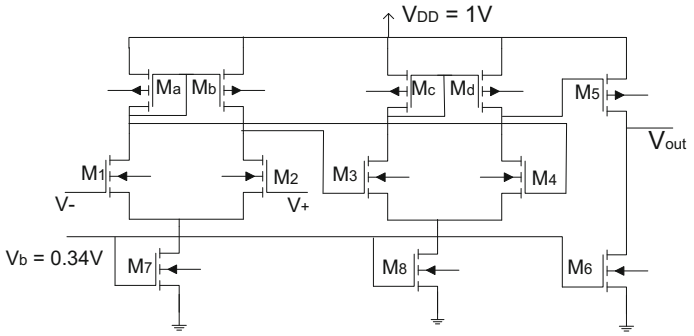

Fig. 20 CMOS Op-Amp designed with the active loads and current mirrors included

Table 7 Transistor sizes W/L for the dynamic loads and the current mirrors

AL_1	AL_2	AL_3	AL_4	AL_5	CM_1	CM_2
100/2	100/2	100/2	100/2	450/2	100/2	100/2

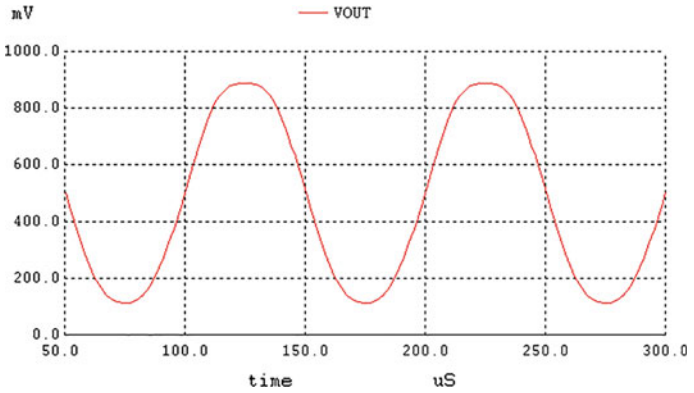

Fig. 21 The open loop transient response of the CMOS OP-Amp

To verify other performance design criteria, the amplifier is simulated using the SPICE transfer function (.TR) and the simulation results are listed below.

```
TEMP=27 deg C
Transfer function analysis ...
transfer_function = 6.955680e+03
output_impedance_at_v(9,0) = 1.077840e+04
vin#input_impedance = 2.401113e+08
WinSpice 1 ->
```

Note that the outcomes of the simulation quite confirm the design criteria, with about 6% of error margin. That is, the gain $A_v = 6956$, the input impedance $R_{in} = 240$ MΩ, and the output impedance $R_{out} = 10.778$ KΩ. This concludes our design example.

7 Nullors in Amplifier Design for Bandwidth

Designing for frequency responses has always been the center piece of designing analog circuits for performances. Analog filters, for instance, are all about frequency profiles and bandwidth. Or in applications such as analog hearing aids, the major part of the design is profiling, frequency curve fitting, and bandwidth adjusting. But the job is not so easy. Part of the problem is because we need to handle complex values rather than real data. Frequency responses mean dealing with the magnitudes as well as the phase angles of the response, and coordination between the two for cases such as stability and convergence needs quite an effort. This usually creates problems and complicates the design procedure substantially. One way to avoid this complexity is to go after the circuit poles and zeros, but even that has its own limitations when it comes to extraction of poles and zeros [7]. New advances in symbolic analysis of circuits are available but these methodologies are relatively new and untested for designs that are rather complex [8–10].

Our objective here is to address the frequency responses of amplifiers when designing for performances. There are typically two approach in solving this problem. One method goes through the poles and zeros methodologies such as root locus techniques, and symbolic verification of poles and zeros, and the second method goes after transfer function characterization. It utilizes the conventional Bode plot representation, common to all commercially available circuit simulators such as SPICE [11]. Here we choose to go after the second approach, and try to design for a desirable frequency response of a circuit transfer function. This of course can cover a wide variety of cases and circuit types. However, here we only consider the design of amplifiers for specified bandwidths. The tools we use are nullors or FNPs in general.

7.1 Design Procedure for Bandwidth Matching

The purpose here is to design for a given frequency bandwidth specified for a particular application, such as audio or video amplifiers, hearing aids and so on. The goal is to modify the bandwidth of an amplifier to match with the frequency bandwidth of a model circuit in one or a few steps so that we could achieve a desirable frequency response.

The following methodology provides a technique that is quick and, if the bandwidth requested is realizable it modifies the circuit to closely match with it.

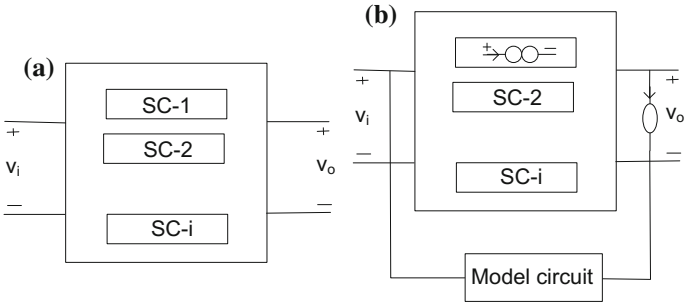

Fig. 22 **a** Circuit *N* with possible two-terminal feedback; **b** Combined circuit with model circuit and a nullor added

Methodology—We start with the following question. Given an analog circuit (amplifier) *N*, how can we get a desired frequency response from *N* by adding one or more sub-circuits to it? For simplicity, we assume the missing sub-circuits (SC) are passive two-terminals, and usually connected to *N* as feedbacks, as shown in Fig. 22a. In brief, we like to design one or more two-terminal circuits and add them to *N*, so that the transfer function of *N* in Eq. (7) becomes close enough to a specified function within a given bandwidth.

$$T(s) = V_0(s)/V_i(s) \tag{7}$$

In our solution, we need to have a model circuit that can produce the characterized frequency response. In case such a specific model circuit is not available we can always create one by synthesizing methods. Our second task is to have the output of *N* to exactly follow the desired frequency response generated by the model circuit. However, this enforcement requires two things: (1) not to disturb the output port situation for both *N* and the model circuit, and (2) make changes in the circuit *N* so that the circuit responds favorably to the conditions imposed to its output port.

For the first requirement a nullator is placed between the two output ports, and the pairing norator takes care of the second requirement, as depicted in Fig. 22b. The combined circuit is now ready for simulation. After the simulation if we assume $V_n(s)$ and $I_n(s)$ are the voltage and current functions associated with the norator then there would be no change in the circuit response if we replace the norator with a two-terminal circuit that its impedance function is represented by

$$Z_{sc}(s) = V_n(s)/I_n(s) \tag{8}$$

In other words, we will get exactly the frequency response we need (represented through the model circuit) if we could find a two-terminal circuit with the impedance function given by Eq. (8) and replace it for the norator.

So, the problem can be restated as follows: *find a two-terminal (feedback) circuit so that its impedance function $Z'_{SC}(s)$ is close enough to that of the norator $Z_{SC}(s)$ for the specified bandwidth*. This may sound like we are back into square one, designing another circuit like *N*, with specified frequency response. Although this may be correct but designing for the feedback circuit is completely different from designing the original circuit *N*. This is a two-terminal circuit, linear, passive and much smaller than N; whereas, *N* can be linear or nonlinear of any size and any complexity. Nevertheless, we need to be aware of a major difficulty here. Although both $V(s)$ and $I(s)$ in Eq. (8) are frequency dependent, but because they represent a non-real component (norator), the chances are that they may not be so related to produce $Z_{SC}(s)$ of Eq. (8), a realizable impedance function. In general, if $Z_{SC}(s)$ is realizable then there must be a two-terminal circuit with the impedance $Z'_{SC}(s)$ so that $Z_{SC}(s)$ and $Z'_{SC}(s)$ share a portion of the Bode plot that covers the specified bandwidth. For more complex cases the process may take multiple steps, resulting in multiple feedbacks to resolve the issue, as we can see it later.

Design challenges

In general finding the right feedback is a very critical step and often hard to fulfill in a single step. As it turns out, the designer's skill will definitely play an important role in designing such feedbacks. There are certain difficulties that we need to address before proceeding further.

1. The goal must be achievable. That is, we should ask for a frequency response that is deliverable by the circuit we have already configured. Obviously, taking any circuit cannot bring us the desired frequency bandwidth that we are looking for, and not all is possible by just adding feedbacks.
2. Which locations in the circuit are good candidates to attach the feedbacks? The location of each feedback must definitely be skillfully selected, and a bad choice might elongate the design process, add more numbers of feedbacks than are required, and even end up unsuccessfully. A decision to select a right location for a feedback depends on its mutual sensitivity with respect to the output response. In other words, the changes in the norator variables ($V_n(s)$ and $I_n(s)$) must substantially affect the output response of the circuit.
3. How many feedbacks are needed to get close enough to the desired frequency response?
4. Finally, how each feedback is designed based on a given $Z_{SC}(s)$? We must remember that $Z_{SC}(s)$ is a complex function, and when turned into real components both magnitude and phase must match. Another problem is the polarity. There are cases when real components are fund to construct the two-terminal curcuit but the component values are negative.

Nevertheless, we should not always expect 100% match between the model response and that of the modified circuit after the process is completed. Just getting "close" to the desired frequency response "within the requested bandwidth" must be enough.

Model circuit
The next question is how to get the model circuit M chosen? Sometimes the model circuit is given, whether it is a prototype, a working unit with older technology, or a black box with no information about its internal structure. In this case we need to reconstruct or modify our target circuit N, so that both N and M have close frequency responses within a certain bandwidth. In the second category the model circuit is not physically available, but the desired response can be translated into a transfer function $T(s) = N(s)/D(s)$ with specified poles and zeros. We may then artificially synthesize and construct the model. A model circuit is typically constructed from multiple circuit modules using ideal dependent sources. A cascade decomposition method, for example, can simply realize a transfer function $T(s)$. Or, tools such as MATLAB can be used to generate the Bode plots from a given transfer function $T(s)$.

7.2 Implementation Procedures

It is important to discuss some implementation issues when the design involves nonlinear devices such as transistors. As we know, nonlinear circuits need biasing and this biasing must not change during the performance design. Hence, adding any two-terminal feedback to the circuit must not disturb the circuit biasing. This simply means that the nonlinear circuit N must be protected by (coupling/bypass) capacitors when any feedback is added to the circuit.

Here is an algorithm that explains the design procedure in a step-wise routine.
Algorithm 2

1. Consider an analog circuit (linear or nonlinear) N that must be redesigned for a selected frequency bandwidth according to a specified criteria and application. Next, try to find a model circuit M that produces the desirable frequency response. If circuit M is not physically available, try to artificially synthesize M, possibly through a cascade decomposition methodology, or else.
2. Find a location in the circuit N so that adding a two-terminal feedback to N can significantly affect the output response.
3. Connect the two circuits, N and M, in parallel-parallel. Keep the two output currents zero by adding a nullator between the outputs, as shown in Fig. 22b. Further, add a matching norator in the designated location, to be replaced with a feedback circuit, later in the process.
   Note 1: parallel-parallel connection of N and M (Fig. 22b) is only valid for voltage to voltage transfer functions. For the case of currents the connections must be in series, as appropriate.[2]

[2] $T(s)$ can be of any of the four types of transfer functions: voltage to voltage, voltage to current, current to current, and current to voltage, and only the first type is selected for study here.

4. Simulate the combined circuit. The output frequency response of the circuit *N* is now exactly the same as that of the model circuit *M*. This simulation will also produce the impedance function $Z_{sc}(s) = V_n(s)/I_n(s)$, for the norator.
5. Next, find a two-terminal circuit so that its impedance characteristic closely matches with $Z_{SC}(s)$, for the bandwidth specified. Next, replace the norator with the two-terminal circuit just found. If $Z_p(s)$ is not realizable make proper approximation/adjustments to fit, or declare un-realizability.
   Note 2: The methodology works for nonlinear circuit as well, provided that the two-terminal circuit does not disturb the circuit biasing, as explained earlier. That is, circuit *N* must be protected by coupling/bypass capacitors, if needed.
6. Finally, if the response obtained is not satisfactory go to step 2 and continue until the bandwidth obtained for N is within the specs.

We are now ready for implementation. The following examples demonstrate the bandwidth adjustment in different amplifiers.

7.3 Design Examples

Example 8 Let us assume a two stage nMOS amplifier shown in Fig. 23a. The magnitude Bode plot for the voltage gain transfer function is plotted in Fig. 24a, plot k. The amplifier shows a bandwidth of B = 75 MHz, which is considered too wide for our designated application. To modify this bandwidth we first need to get a model circuit with the desirable bandwidth. A model circuit for our application is synthesized next. This model circuit is simply an RC circuit with the output voltage magnified by a VCVS to provide a gain of A_0 = 51 dB (350 V/V), which is equal to that of the amplifier. The model circuit is shown in Fig. 23b, which has the desired bandwidth of B = 1 MHz. The model circuit is then simulated and its output Bode plot is shown in Fig. 24a, plot j.

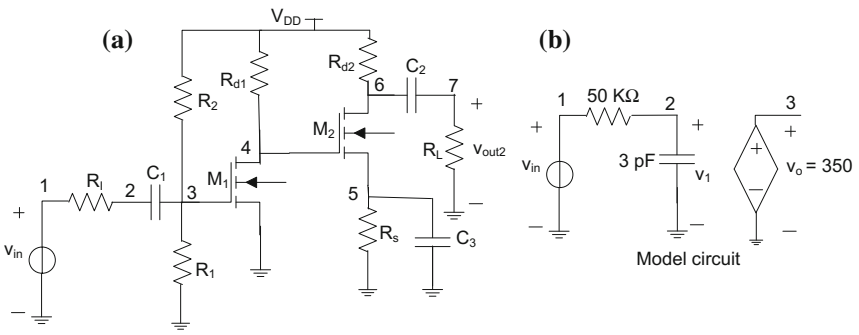

Fig. 23 Circuits for Example 1. **a** An MOS amplifier: M_1 and M_2: W/L = 50/1 μm, R_I = 2 KΩ, R_1 = 110 KΩ, R_2 = 860 KΩ, R_4 = 5 KΩ, R_5 = 0.5 KΩ, R_6 = 100 KΩ C_1 = 20 nF, C_2 = 100 nF, and C_3 = 2.5 μF. **b** The model circuit

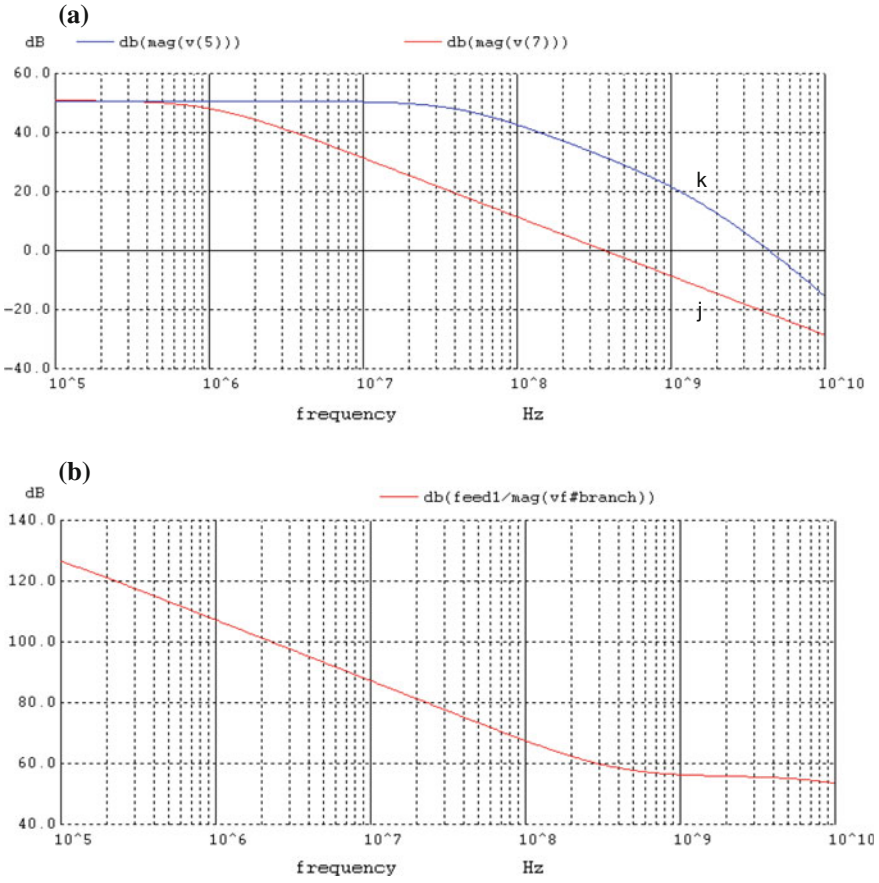

Fig. 24 Bode plots for the MOS amplifier (plot *k*), and the model circuit (plot *j*)

Our next step is to find and add a feedback circuit to the amplifier circuit so that its frequency response get close enough to the frequency response of the model circuit, as our target profile. The location is selected to connect the outputs of the two stages together, as shown in Fig. 25. The pairing nullator, on the other hand, is used to isolate the output ports of the amplifier and the model from affecting each other, while connected in parallel. The nullator is mainly used to stop the current flow between the two circuits. Now the circuit is ready for simulation, but before the simulation takes place we need to replace the nullor with a high gain controlled source. We select a CCCS for this purpose, as shown (f_1) in the SPICE code listed below.

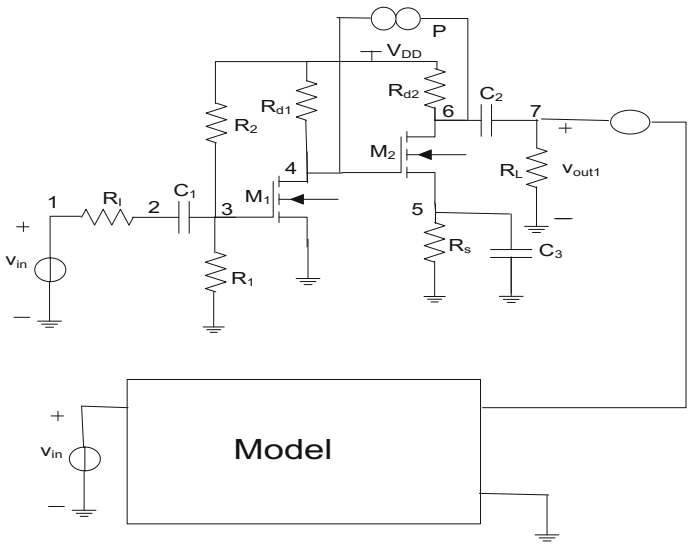

Fig. 25 Combined circuit, the MOS amplifier, the model circuit and the nullor

```
.subckt Mamp2 1 3 4 6 7
* Main MOS amplifier
VDD   10          0                DC              10
M1    4           3                0               0          N_1u L=1 W=50
M2    6           4                5               0          N_1u L=1 W=50
RI                1                2               2k
R1                3                0               110k
R2                10               3               860k
R3                10               4               20k
R4                10               6               5K
R5                5                0               500
R6                7                0               100k
C1                2                3               20n
C2                6                7               100nu
C3                5                0               2.5u
.ends
* ********* The MOS amplifier
X1 1 2 3 4 5  Mamp2
* ********* RC Model circuit
R1                1                6               50k
C1                6                0               3p
e1      7                 0                6               0          350
* ********* The MOS amplifier connected to the model circuit
X2 1 8 9 11 12  Mamp2
v1                12               7               DC 0
vf                11               a               DC 0
f1      a                 9                v1              1.0e6
```

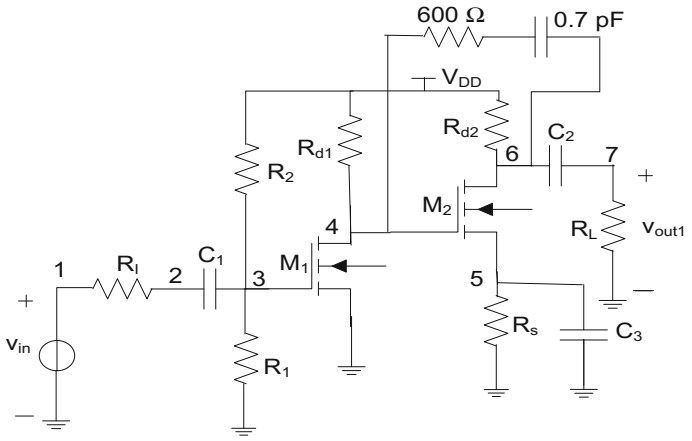

Fig. 26 The MOS amplifier after being modified with feedback

Next we need to see how best can we replace the norator with a two-terminal feedback? To do so we need to characterize the norator from its magnitude and phase Bode plots, associated with the pseudo-impedance $Z_p(s) = V_p(s)/I_p(s)$, where $V_p(s)$ and $I_p(s)$ are the voltage and currents of the norator. Our next move is to try to find a two-terminal circuit that best matches with these frequency responses. Figure 24b shows the magnitude Bode plot of the pseudo-impedance $Z_p(s)$ of the norator (for simplicity we ignore the phase plot). A close look at this plot reveals that it represents very closely the impedance characteristic of a series RC circuit. With a magnitude slope of −20 dB/dec at lower frequencies and a break point for a zero at 380 MHz. we simply get R = 600 Ω and C = 0.7 pF. Figure 27b compares the frequency characteristics of the norator (plot i) with the one from the RC feedback (plot j, a shift of 2 dB is applied for clarity). We notice the closeness of the two responses. The RC circuit so found is then replaced for the norator in Fig. 26. Subsequently, we remove the nullor, and also the model circuit. The amplifier is now ready for simulation. The frequency response of the amplifier with feedback (Bode plot) is given in Fig. 27a, plot i. This result is compared with the responses from the original amplifier without feedback, and the model circuit as well. We notice that the frequency characteristic of the amplifier with feedback (plot i) is almost identical to that of the model circuit (plot j), and it is distinctly far from that of the original amplifier (plot k). This concludes our example.

7.4 Designing for Bandwidth with Multiple Feedbacks

Given the realizability of the case, it is possible to continue modifying the bandwidth of an amplifier through multiple feedbacks until we get close enough to the

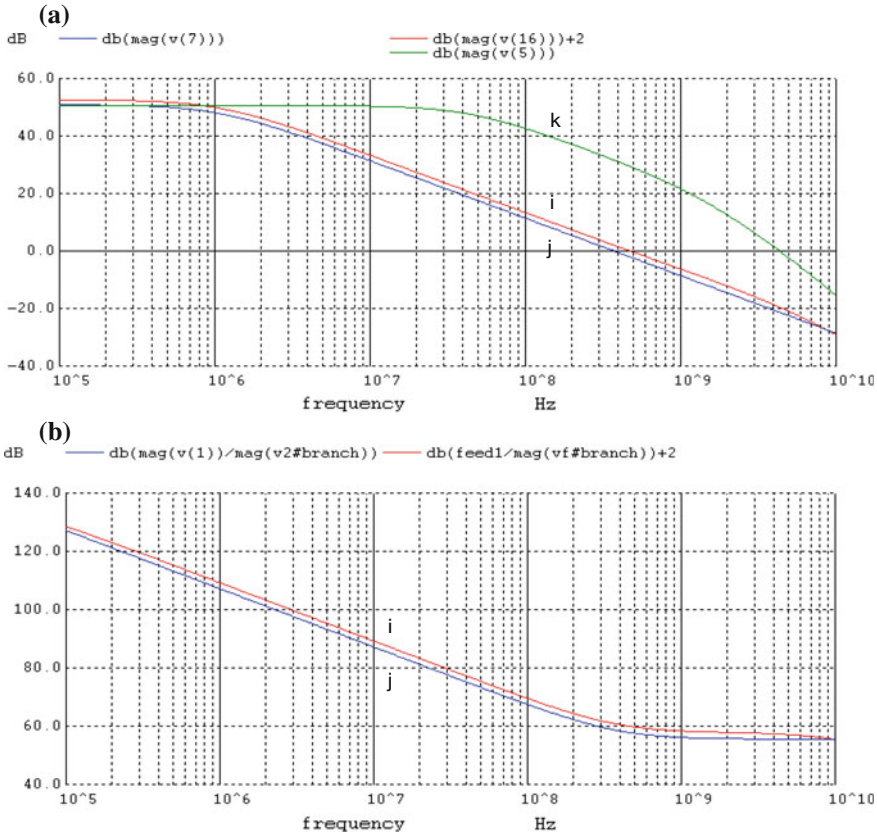

Fig. 27 Bode plots for MOS amplifier after being modified by the feedback

model circuit bandwidth. One way to do this is to go through a step by step procedure and in each step repeat the combined circuit similar to Fig. 25 with including the newest amplifier circuit that was designed in the previous step. We will see this in the following example.

In the following example we are trying to make a reverse process, i.e., expanding the bandwidth of an amplifier rather than shrinking it. The other difference that exists between this example compared to the previous one is that here we go through multiple feedbacks to achieve the maximum bandwidth expansion required. Because of the two stages amplifier, employing multiple feedbacks are convenient, and because a model circuit is always present we can continuously check to see how close we are to meet the desirable solution.

Example 9 Consider a two stage BJT amplifier shown in Fig. 28a. The gain frequency response of the amplifier in shown in Fig. 28b, plot x. The amplifier is characterized as: gain $A_0 = 72$ dB (4,000 V/V), and bandwidth B = 450 kHz. This bandwidth is considered too low for our application, and we need to increase. To

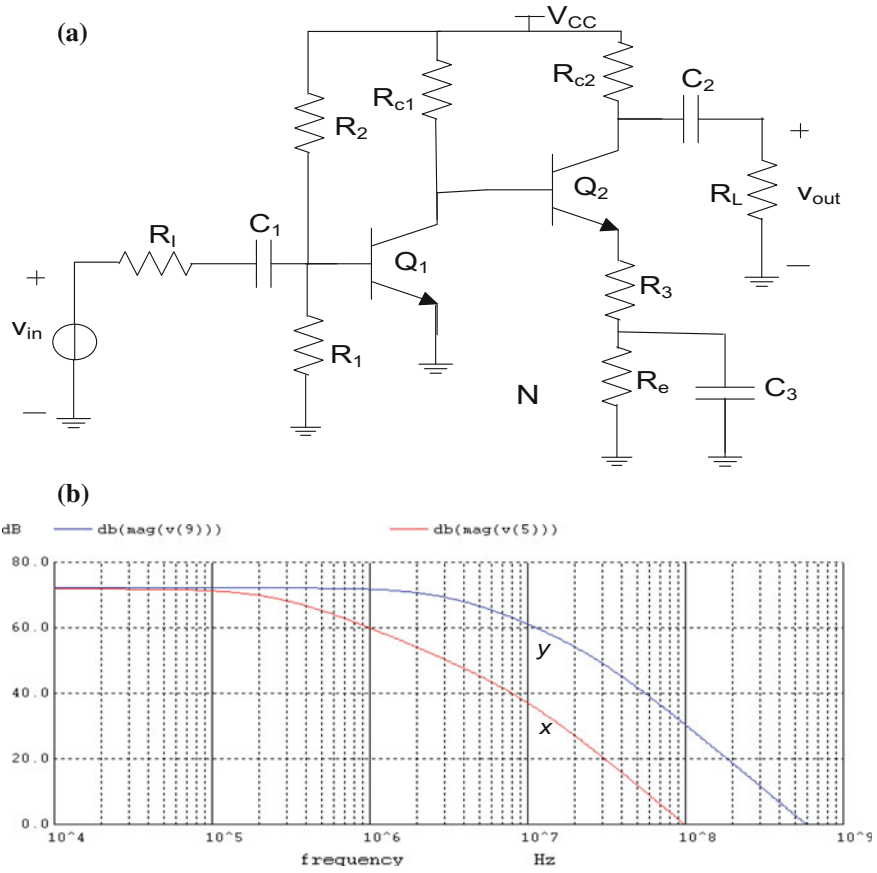

Fig. 28 The BJT amplifier, it Bode plots response, plot x, and the ideal response, plot y

expand the bandwidth we first need to get a model circuit with the desired bandwidth. We have simply constructed the model circuit with modular RC circuits and ideal dependent sources (not shown). The model circuit represents the desired bandwidth of B = 5.5 MHz and the frequency response of the circuit is shown in Fig. 28b, plot y.

Our next move is to add a feedback circuit to the amplifier in order to modify its response. Figure 29 shows a combined circuit set up. The amplifier is parallel-parallel connected to the model circuit. A nullator stops the flow of currents across the two circuit outputs while the pairing norator, as a place holder, occupies a feedback position providing required conditions for the amplifier to respond to the model bandwidth.

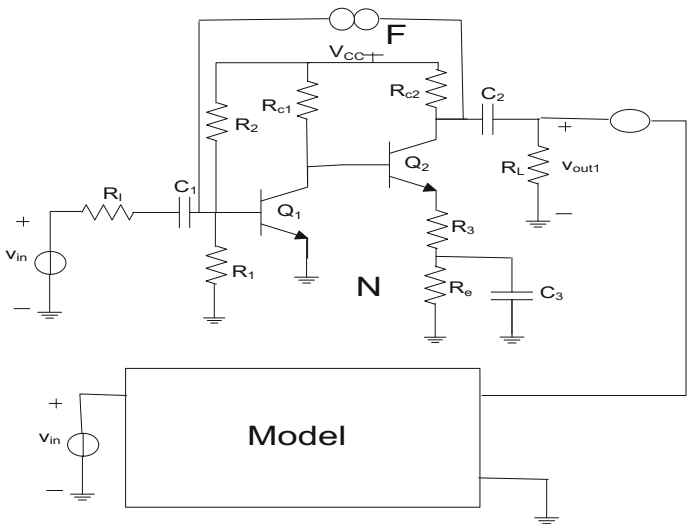

Fig. 29 Combined circuit, the BJT amplifier, the model circuit and the nullor

Next, we need to characterize the norator in order to safely replace it with a two-terminal feedback circuit. Figure 30a, plot y, represents the magnitude Bode plot for the pseudo-impedance $Z_p(s) = V_p(s)/I_p(s)$ of the norator. Now we should be thinking of replacing the norator with a feedback circuit that best represents it. Looking at the plot y we realize that the upper part of the plot closely represents the frequency response of a capacitor. To find this capacitor, we assume a feedback capacitor $C_{f1} = 70$ fF with the impedance characteristic plotted in Fig. 30a, plot z. This plot is almost identical to that of the norator (plot y), or at least at the lower frequencies. Subsequently we simulate the amplifier after the norator is replace with the capacitor $C_{f1} = 70$ fF, and after removing the model circuit all together. The simulation result is plotted in Fig. 30b, plot z. Note that both frequency responses from the original amplifier (plot x) and the one from the model circuit (plot y) are also plotted in Fig. 30b for comparison. We now clearly notice that the bandwidth of the amplifier in extended, and has jumped from 450 to 2.5 MHz, which is much improved, and not far away from the desired bandwidth of 5.5 MHz.

In case further improvement is needed, one option to go for forward is to try for a second feedback. To do this we repeat the steps we took for the first feedback except that this time we have come closer to the model response. So we repeat connecting the amplifier (this time with the feedback C_{f1} included) with model circuit, as shown in Fig. 29. Our selection for the feedback location this time is across the second stage amplifier, while the first one was across the two stages. We then simulate the combined circuit as constructed. We again get the impedance characteristic curve for the norator, say $Z_{SC}(s) = V_n(s)/I_n(s)$. Although this characteristic curve is not shown here, but it shows that it is very close to a series RC circuit. The values found are $R_{f2} = 40$ kΩ and $C_{f2} = 1.8$ pF. Finally, we replace the

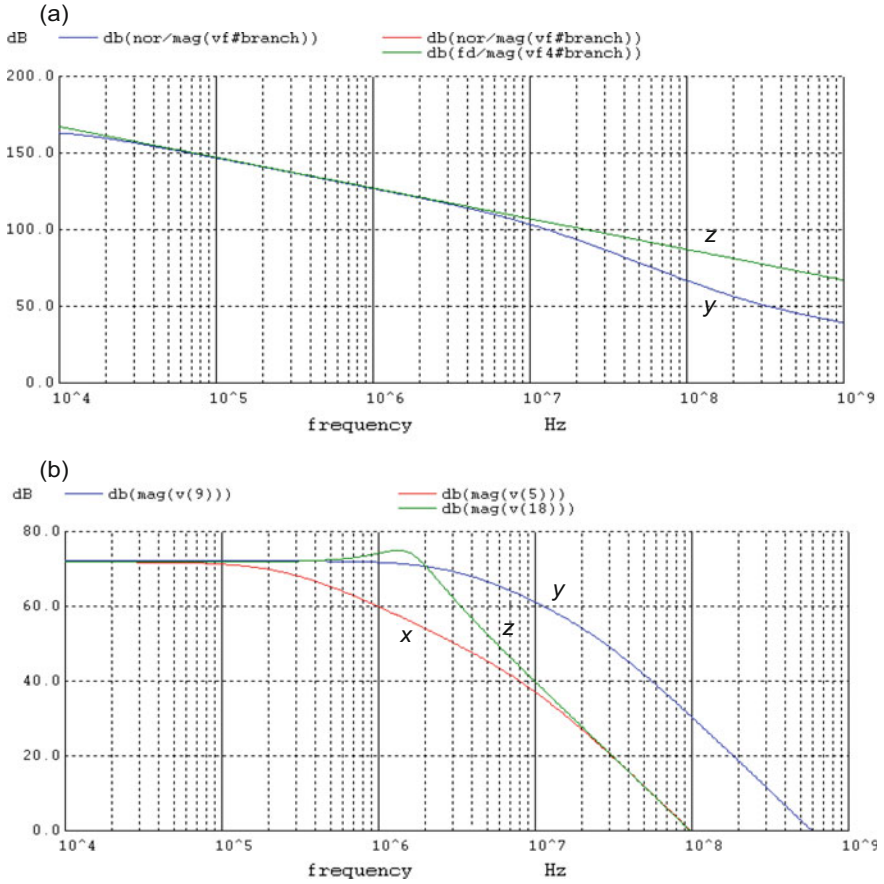

Fig. 30 Bode plots BIT amplifier: plot x for the original amplifier, plot y for the model circuit (norator), and plot z for the modified amplifier

norator with the RC circuit, and after removing the model circuit we simulate the amplifier circuit; this time with two feedbacks. The result of the simulation is plotted in Fig. 31, plot z, along with the other plots, x and y, for the original amplifier and the model circuit. Now the bandwidth is improved substantially and it has reached to B = 4.4 MHz, which is 20% less than the ideal case (the model response). There is still possibility to go for the third modification, but we prefer to stop here. In comparing with plot z in Fig. 30b we also notice a substantial improvement in the general form of the characteristic curve obtained. In Fig. 30b the plots z and x almost come together and sharply cutting the bandwidth, whereas in Fig. 31b plot z has moved further away from plot x of the original amplifier. Finally, the modified amplifier circuit with both feedbacks is shown in Fig. 32. Note that neither feedbacks disturb the biasing of the amplifier, because they have capacitors that stop DC from entering the feedbacks. This concludes our example.

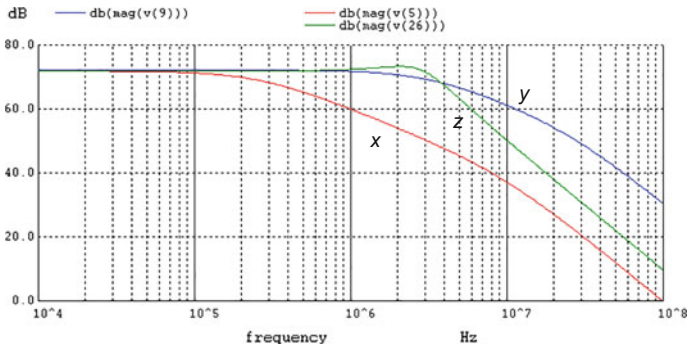

Fig. 31 Improved frequency response (plot z) after adding two feedbacks

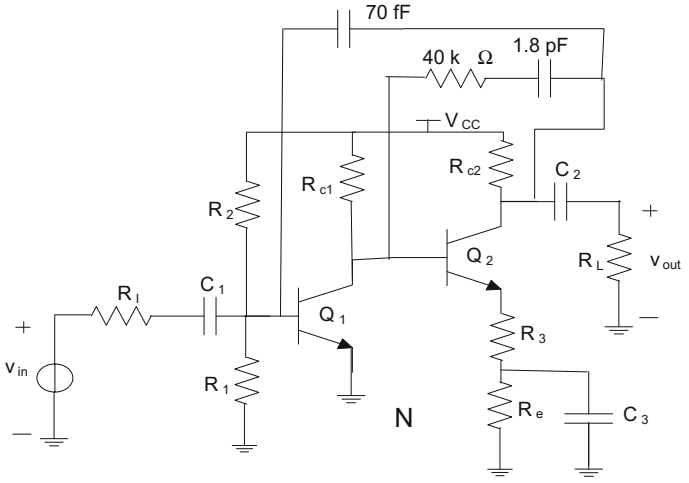

Fig. 32 Bode plots for Example 1: **a** Output x characteristics; **b** frequency responses of the norator and the two-terminal feedback *P*

8 Conclusion

The chapter starts with introducing Fixator-Norator Pairs (FNPs). They have been shown to be very powerful tools for designing analog circuits. The application of FNPs are shown to be wide spread in almost all aspects of analog circuit designs, including biasing, gain, input and output impedances, and frequency responses. FNPs are also used in designing active loads and current mirrors in IC circuits. In all these application the role of a fixator is to provide a fixed and stable response to a circuit variable as specified by the design criteria, and the pairing norator acts as a place holder for a two terminal sub-circuit that is needed to sufficiently modify the circuit in order to respond to the fixator.

Because of the complexity that exist in designing for a specific bandwidth and frequency profile, the design methodology is changing here. It is shown that a model circuit is extremely helpful in this case. This model circuit provides the frequency response needed and FNP is used to force the original circuit to follow the model circuit on its bandwidth. Since a model circuit is only for simulation purposes, it can be constructed from ideal components such as controlled sources, and it can be built modular.

As discussed, the FNP methodology works for both linear and nonlinear circuits. However, for nonlinear circuits we need to keep the biasing condition unchanged during the AC design process. The circuit biasing may change when feedbacks are added to the original amplifier circuit, unless it is protected. In this chapter we use coupling capacitors to protect the circuit biasing if needed.

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Nullor-Based Negative-Feedback Memristive Amplifiers: Symbolic-Oriented Modelling and Design

Arturo Sarmiento-Reyes and José Balaam Alarcón-Angulo

Abstract The memristor as an actual device was introduced in April 2008 at the HP labs, while its original foundations are dated from 1971 when Prof. L. O. Chua devised the memristor as the fourth basic circuit element. Nowadays, the memristor has captured most of the attention not only from circuit theoreticians, but also from circuit designers because the widely open possibilities of the device in applications where it co-exists with traditional electronics. A particular case of such an application arises when the memristor is combined with the nullor in order to achieve a memristive input-output transfer function. In this chapter, we firstly introduce a fully symbolic model of the memristor that is used for the symbolic analysis of the amplifier configurations. It is important to point out the symbolic nature of our memristor model in contrast with other models that are of numerical nature or implemented in a macro-equivalent. Secondly, the four single-loop negative-feedback nullor-based amplifier configurations are introduced, and their corresponding analytic transfer functions are generated and characterised. Similarly, the noise and harmonic distortion analyses are carried out on the four configurations yielding fully symbolic expressions for both, the output equivalent noise and the harmonic components. In a next step, the nullor is synthesised by using a memistor, which is a combination of two memristors connected back-to-back. Finally, a transmemristance amplifier is used as a case study of design when the nullor is substituted by a memistor. Along the manuscript, the resulting expressions from the mathematical analyses are verified with HSPICE simulations that incorporate the memristor model from a description in the VERILOG-A language.

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1 Introduction

This chapter deals with a singular element (the nullor) when combined with the memristor to form special classes of memristive circuits, namely the memristive amplifiers.

1.1 The Nullor

The nullor was firstly employed by Carlin and Youla in 1961 [1], where the term "pathologic" was coined for both the nullator and the norator. However, the nullor was formally introduced in 1964 by Carlin [2] as a two-port defined by a nullator at port 1 and a norator at port 2—as shown in Fig. 1a. In his work, Prof. Carlin wisely pointed out that the nullor exhibits a more natural (and understandable) behaviour when it appears interconnected with other circuit elements. However, it was Prof. Bernard D.H. Tellegen who stated the concept of the four ideal amplifiers in 1954 [3].

An important niche of the nullor has been as a key-element to achieve circuit transformations in active and passive network theory and synthesis [4–7]. In the search for an actual implementation of a nullor in the form of an integrated circuit, we can mention the works reported in [8–10]. This line of research led indeed to the design of op-amps and OTAs.

The nullor is a two-port. On one side, the nullator at the input port handles:

$$\begin{aligned} v_i &= 0 \\ i_i &= 0 \end{aligned} \tag{1}$$

On the other side, the norator at the output port handles:

$$\begin{aligned} v_i &= \times \\ i_i &= \times \end{aligned} \tag{2}$$

where "×" indicates that both voltage and current have arbitrary values determined by the environment, i.e. the circuitry that is connected at the output of the nullor.

It clearly results that after combining the expressions from Eqs. (1) and (2), the chain matrix of the nullor can be expressed as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{3}$$

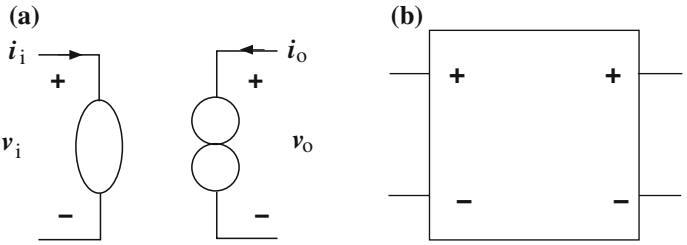

Fig. 1 Symbols of the nullor

with:

$$A = \frac{1}{\mu} = \frac{v_i}{v_o}\Big|_{i_o=0} = 0 \qquad B = \frac{1}{\gamma} = \frac{v_i}{i_o}\Big|_{u_o=0} = 0$$
$$C = \frac{1}{\zeta} = \frac{i_i}{v_o}\Big|_{i_o=0} = 0 \qquad D = \frac{1}{\beta_F} = \frac{i_i}{i_o}\Big|_{u_o=0} = 0$$

Therefore, the nullor models the four ideal infinite-gain amplifiers:

$$\begin{array}{ll} \mu = \infty & \gamma = \infty \\ \zeta = \infty & \beta_F = \infty \end{array} \tag{4}$$

The infinite gains in Eq. (4) led to use the nullor as the active part in negative feedback finite-gain amplifiers, with the aim of producing high performance transfer functions of these types of amplifiers. A design methodology oriented to structure the synthesis of negative feedback amplifiers is reported in [11–15]. Herein, the synthesis of the nullor by using transistors as active devices was driven by tackling noise, clipping and distortion as key-specifications of the procedure. Further treatment of this methodology has been reported in [16–19]. In the rest of the manuscript, the symbol of the nullor to be used corresponds to the one shown in Fig. 1b.

1.2 The Memristor

The memristor was introduced by Prof. L.O. Chua in his seminal paper from 1971 [20] as the fourth basic electric element that closes the loop around the basic electric variables of Circuit Theory, namely the electric charge q, voltage v, current i, and flux linkage ϕ as sketched in Fig. 2. Besides, the relationships of the cross corners of the figure are the charge-conservation and flux-conservation laws, which are given respectively as:

$$\frac{dq(t)}{dt} = i(t) \qquad \text{or} \qquad q(t) = \int_{-\infty}^{t} i(\tau)d\tau \tag{5}$$

and

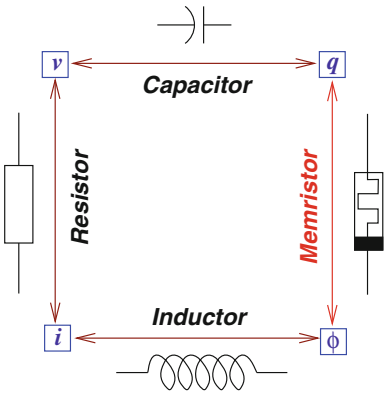

Fig. 2 Basic circuit elements

$$\frac{d\phi(t)}{dt} = v(t) \qquad \text{or} \qquad \phi(t) = \int_{-\infty}^{t} v(\tau)d\tau \tag{6}$$

Since the electric charge and the flux are the variables involved in the memristor branch relationship, a memristor can be either flux-controlled or charge-controlled:

$$\begin{array}{ll} q(t) = g_M(\phi) & \phi(t) = f_M(q) \\ \text{flux-controlled} & \text{charge-controlled} \end{array} \tag{7}$$

From Eqs. (5), (6), and (7), it can be easily found:

$$\begin{array}{ll} i(t) = \frac{d\ g_M(\phi)}{d\phi} v(t) & v(t) = \frac{df_M(q)}{dq} i(t) \\ \text{flux-controlled} & \text{charge-controlled} \end{array} \tag{8}$$

These expressions can be recast in a pair of ohmic relationships:

$$\begin{array}{ll} i(t) = W(\phi)v(t) & v(t) = M(q)i(t) \\ \text{flux-controlled} & \text{charge-controlled} \end{array} \tag{9}$$

where $W(\phi)$ and $M(q)$ are denoted as the memductance and the memristance respectively. A publication posterior to the seminal paper appeared in 1976 [21] revealed an extension to memristive systems.

The theoretical concepts developed by Prof. Chua stayed in latency for nearly 30 years-time, until a nanometric memristor was actually fabricated at the HP Labs [22, 23]. This event as well as the publication of the seminal paper represent the most important milestones in memristor development.

Nowadays, the memristor has captured most of the attention not only from circuit theoreticians, but also from circuit designers because of the widely open possibilities of the device in applications where it co-exists with traditional electronics.

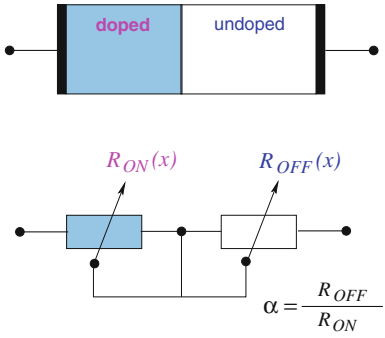

Fig. 3 Series equivalent

2 Development of the Memristor Model

In order to carry out any further analysis of the nullor-based memristive amplifiers, it becomes necessary to firstly determine a model for the memristor. The speed of the drift from the doped region toward the undoped region is described by [24]:

$$\frac{dx(t)}{dt} = \frac{\mu R_{on}}{\Delta^2} i(t) f_w(x) \tag{10}$$

where Δ stands for the full length of the semiconductor material and $x(t)$ is the **normalised** state-variable ($x = w/\Delta$), normalised by the total length. Besides, μ is the mobility of the charges, R_{on} is the ON-state resistance and $f_w(x)$ is a window function that bounds the state-variable x. The current is the stimuli function given as: $i(t) = A_p \sin(\omega t)$ where A_p is the amplitude, and ω is the angular frequency.

An electrical equivalent of the mechanism can be devised as a series connexion of the coupled resistors R_{on} and R_{off}, as shown in Fig. 3. A fully symbolic solution to the ordinary differential equation in (10) has been found by using the perturbation-based homotopy method from [25–27]. In order to solve the nonlinear drift equation, the bounding of the state-variable is defined by the Joglekar function [28]:

$$f_w(x) = 1 - (2x - 1)^{2k} \tag{11}$$

Equation (10) is solved by using a homotopy method of order-3 with $k = 1$, which yields a harmonic solution for $x(t)$:

$$x(t) = \begin{array}{l} X_0 - \frac{80}{3}\mathcal{P}_3 + 12\mathcal{P}_2 - 4\mathcal{P}_1 \\ + \left(40\mathcal{P}_3 - 16\mathcal{P}_2 + 4\mathcal{P}_1\right)\cos(\omega t) \\ + \left(4\mathcal{P}_2 - 16\mathcal{P}_3\right)\cos(2\omega t) \\ + \frac{8}{3}\mathcal{P}_3 \cos(3\omega t) \end{array} \tag{12}$$

It can be easily demonstrated that $x(0) = X_0$ is the initial condition of the state variable. Besides, the variables $\mathcal{P}_i$ are polynomials defined as:

$$\begin{aligned}\mathcal{P}_1 &= \gamma X_0(X_0 - 1)R_{on} \\ \mathcal{P}_2 &= \gamma^2 X_0(X_0 - 1)(2X_0 - 1)R_{on}^2 \\ \mathcal{P}_3 &= \gamma^3 X_0(X_0 - 1)(6X_0^2 - 6X_0 + 1)R_{on}^3\end{aligned} \tag{13}$$

with:

$$\gamma = \frac{\mu A p}{\Delta^2 \omega}$$

The resulting solution from Eq. (12) is substituted in the coupled resistor series equivalent given as:

$$M(t) = R_{on}x(t) + R_{off}\left[1 - x(t)\right] \tag{14}$$

which yields the memristor model:

$$M(t) = R_{on}(\alpha - 1)\begin{bmatrix}(\frac{80}{3}\mathcal{P}_3 - 12\mathcal{P}_2 + 4\mathcal{P}_1)+ \\ (-40\mathcal{P}_3 + 16\mathcal{P}_2 - 4\mathcal{P}_1)\cos(\omega t)+ \\ (16\mathcal{P}_3 - 4\mathcal{P}_2)\cos(2\omega t)+ \\ (-\frac{8}{3}\mathcal{P}_3)\cos(3\omega t)\end{bmatrix} + R_{init} \tag{15}$$

In addition:

$$R_{init} = \left[X_0 + \alpha(1 - X_0)\right]R_{on} \tag{16}$$

The expression in Eq. (15) constitutes indeed a fully symbolic model of the memristor as function of physical parameters. The model have been recast in a Verilog-A module, that can be used for electric simulation of memristive circuits. Appendix A shows the code of the model.

Model characterisation

Further numeric evaluations are achieved in a very straightforward form in order to verify the fingerprints of the memristor model [29]. Nominal values corresponding to the well-known HP-memristor are listed in Table 1.

The $i(t) - v(t)$ characteristics for several values of the angular frequency are shown in the t-parametric plots of Fig. 4. These characteristics proof that the developed model possesses the first fingerprint of a memristor, which is a self-crossing pinched-hysteresis loop (PHL). In addition, it can be noticed that the area of these characteristics decreases as the frequency increases which is another important fingerprint. Besides, since the curves lie on the first and third quadrants of the $i(t) - v(t)$ plane, the passivity of the memristor is guaranteed, which is another important signature of the device.

Table 1 HP-memristor parameters

Parameter	Value
μ	10^{-10} cm^2 s^{-1} V^{-1}
R_{on}	100 Ω
Δ	10 nm
Ap	40 μA
α	160

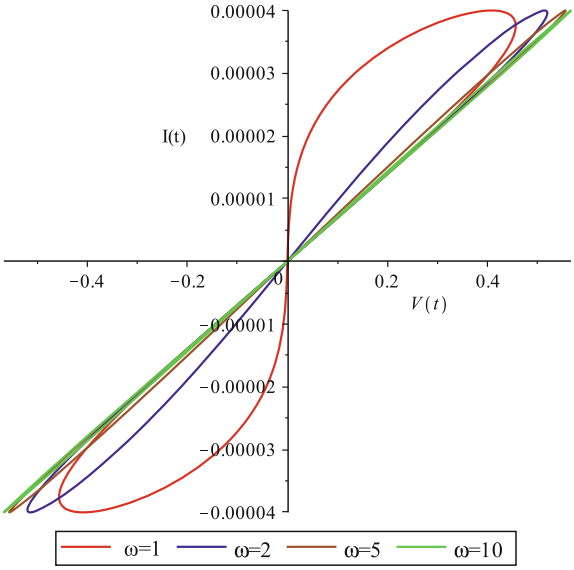

Fig. 4 Pinched hysteresis loop for several values of ω

Besides, the memristance-current plots for the same set of ω values are shown in Fig. 5. Here again, it can be noticed that the memristance has an excursion that spans from a maximum to a minimum value. The difference between both values decreases with the frequency.

On one side, the maximum value of the memristance is the same for any frequency, and it is defined as:

$$M_{max} = M(t)|_{t=0} = \left[X_0 + \alpha(1 - X_0)\right] R_{on} \tag{17}$$

i.e. $M_{max} = R_{init}$ and it depends only on the initial condition, the on-state resistance and the ratio with the off-state.

On the other side, the minimum value is given as:

$$M_{min} = M(t)|_{t=\frac{\pi}{\omega}} = R_{init} + R_{on}\,(\alpha - 1)\left(8\mathcal{P}_1 - 32\mathcal{P}_2 + \frac{256}{3}\mathcal{P}_3\right) \tag{18}$$

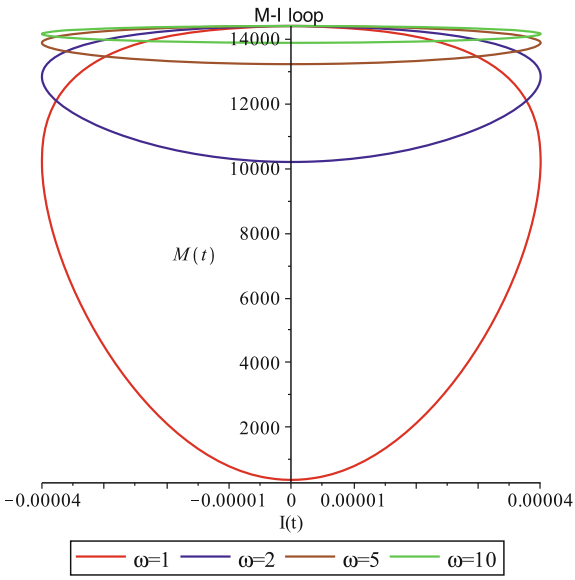

Fig. 5 $M - I$ characteristics for several values of ω

Table 2 M_{max} and M_{min} for some discrete values of ω

ω	M_{max}	M_{min}
1	14.41 kΩ	374 Ω
2	14.41 kΩ	10.205 kΩ
5	14.41 kΩ	13.23 kΩ
10	14.41 kΩ	13.889 kΩ
100	14.41 kΩ	14.363 kΩ

Table 2 shows the values of the maximum and minimum memristance for several discrete values of the angular frequency ω for the parameter values given in Table 1. Figure 6 show the behaviour of both limit memristances in a continuous plot versus the frequency. This plot illustrates the assymptotic behaviour of the minimum memristance that tends to M_{max}. Hence, the memristor behaves as a linear resistor as $\omega \to \infty$, which is another important fingerprint.

Last, but not least, Fig. 7 shows the waveforms for the current and the voltage of the memristor for $\omega = 1$. It can be noticed, that they fulfil the nullor behaviour of the the memristor crossing the origin, i.e. $v = 0$ and $i = 0$ simultaneously.

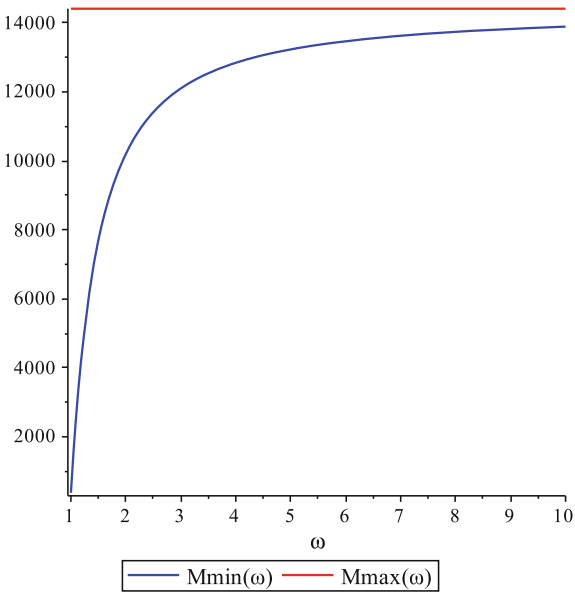

Fig. 6 M_{max} and M_{min} versus the frequency

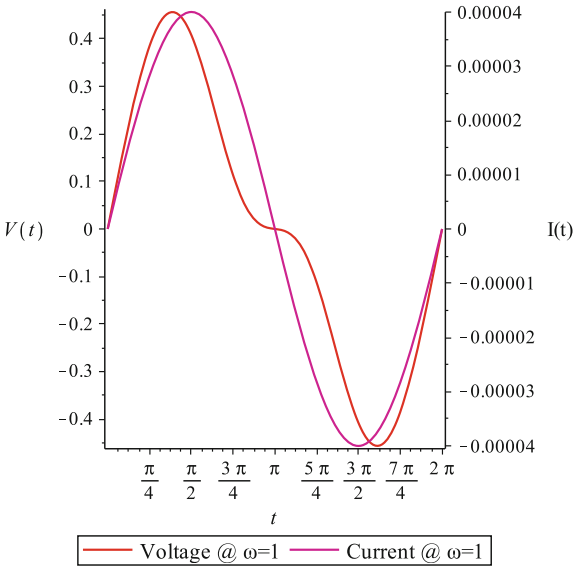

Fig. 7 Voltage and current of the memristor for $\omega = 1$

3 Memristive Amplifiers

A particular case of memristive circuit application arises when the memristor is combined with the nullor in order to achieve a memristive output-input transfer function. The memristive versions of the single-loop nullor-based negative-feedback ampli-

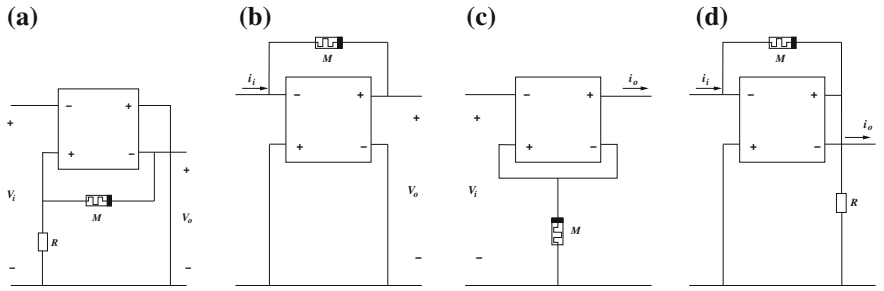

Fig. 8 Basic memristive nullor-based amplifiers: **a** Voltage amplifier **b** Transmemristance amplifier **c** Transmemductance amplifier **d** Current amplifier

fiers are shown in Fig. 8. Under the assumption of instantaneous linearity [30], the gain of the amplifiers depicted in Fig. 8 can be expressed as:

$$\begin{aligned} \frac{V_o}{V_i}(t) &= 1 + \frac{M(t)}{R} \\ \frac{V_o}{I_i}(t) &= -M(t) \\ \frac{I_o}{V_i}(t) &= -W(t) \\ \frac{I_o}{I_i}(t) &= 1 + \frac{M(t)}{R} \end{aligned} \tag{19}$$

3.1 Memristive Voltage Amplifier

The gain of this amplifier configuration is given as

$$\frac{V_o}{V_i}(t) = 1 + \frac{M(t)}{R} \tag{20}$$

The voltage amplifier is simulated using the memristor model given in Eq. (15) with the nominal values from Table 1, and chosing a value of 300 Ω for R. The resulting $V_o - V_i$ transfer loops are shown in Fig. 9a from the evaluation of the symbolic model, (b) from the symbolic circuit simulation framework AnalogInsydes [31] and (c) from HSPICE. The obtained overall transfer characteristics have the form of a pinched-hysteresis loop, i.e. the amplifier mimics in fact the memristor behaviour.

A usual form of reporting the behaviour of the overall gain of the amplifier is by plotting the gain as a function of time for a given frequency [32]. For this amplifier, the time-varying voltage gain of the amplifier is shown in Fig. 10 for $\omega = 1$. This curve can be better understood by looking at the values of M_{max} and M_{max} in Table 2, which yield maximum and minimum gains, respectively:

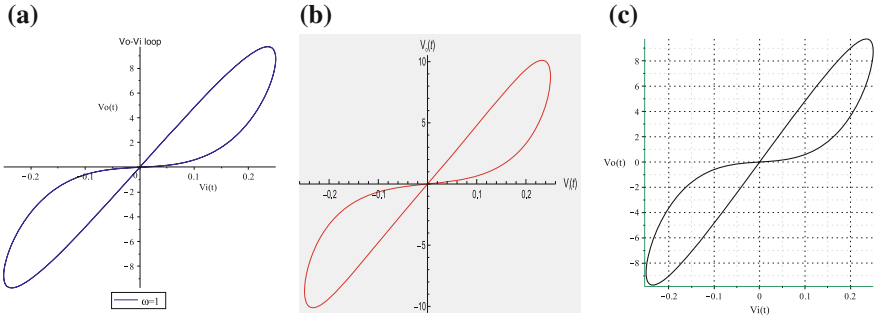

Fig. 9 Pinched hysteresis transfer loop for the voltage amplifier for $\omega = 1$

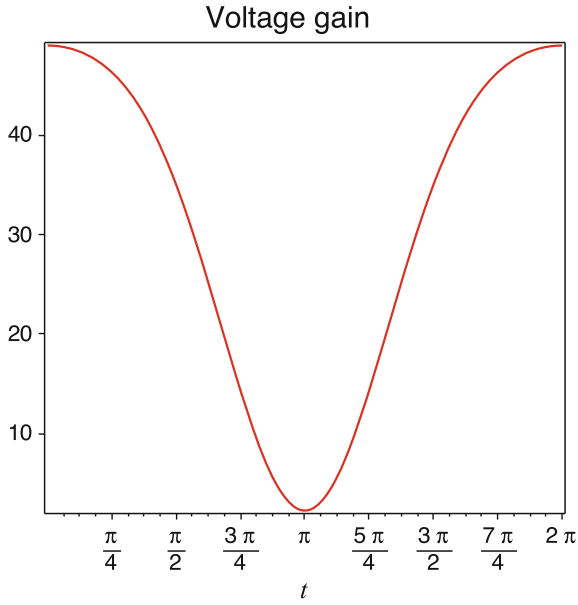

Fig. 10 Voltage gain for $\omega = 1$

$$\begin{aligned} \max\left(\frac{V_o}{V_i}\right) &= \left(1+\frac{M(t)}{R}\right)\Big|_{M(t)=M_{max}} = 1+\frac{14410}{300} = 49.033 \\ \min\left(\frac{V_o}{V_i}\right) &= \left(1+\frac{M(t)}{R}\right)\Big|_{M(t)=Mmin} = 1+\frac{374}{300} = 2.246 \end{aligned} \tag{21}$$

On the one side, the maximum gain occurs at $t = 0, 2\pi$, i.e. at the begin and end of the PHL, which can be seen as the cross at the origin with maximum slope. On the other side, the minimum gain occurs at the half of the period, i.e. the cross at the origin with minimum slope.

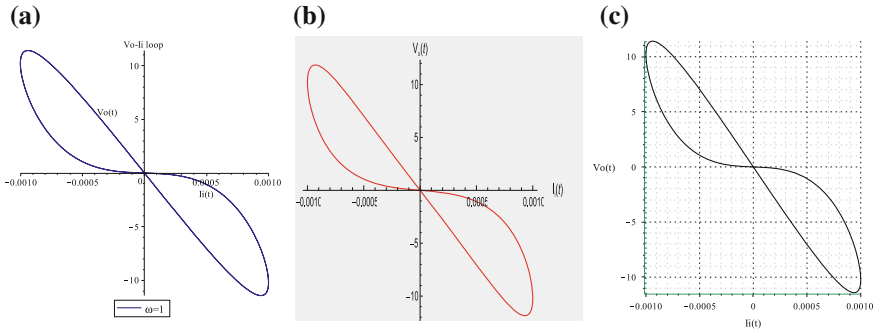

Fig. 11 Pinched hysteresis transfer loop for the transmemristance amplifier for $\omega = 1$

3.2 Transmemristance Amplifier

A similar treatment is done with this amplifier. The gain of this configuration is given as

$$\frac{V_o}{I_i}(t) = -M(t) \tag{22}$$

i.e. the gain is purely defined by the memristance. The $V_o - I_i$ transfer characteristic of the amplifier is obtained and shown in in Fig. 11.

The maximum and minimum gains at $\omega = 1$ are in fact determined by the limit values of the memristance at $\omega = 1$:

$$\begin{aligned} \max\left(\frac{V_o}{I_i}\right) &= -M_{max} = -14410\Omega \\ \min\left(\frac{V_o}{I_i}\right) &= -M_{min} = -374\Omega \end{aligned} \tag{23}$$

Notice that the maximum and minimum correspond to the absolute values of the gain, because the negative sign complies with the fact that the PHL transfer loop is on the second and fourth quadrant. Figure 12 shows the time-varying gain.

3.3 Transmemductance Amplifier

The gain of this amplifier configuration is given as

$$\frac{I_o}{V_i} = -\frac{1}{M(t)} \tag{24}$$

The $I_o - V_i$ transfer characteristic of the amplifier is obtained and shown in in Fig. 13.

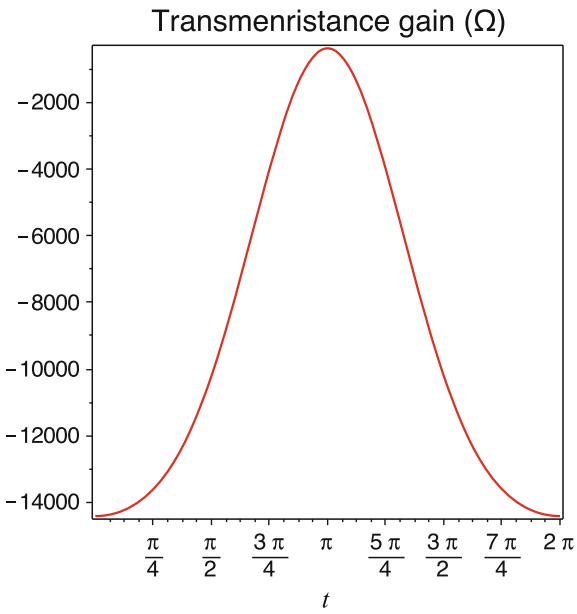

Fig. 12 Transmemristance gain for $\omega = 1$

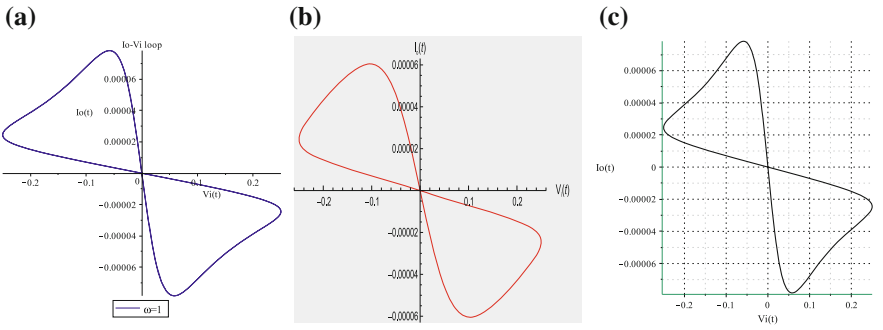

Fig. 13 Pinched hysteresis transfer loop for the transmemductance amplifier for $\omega = 1$

The maximum and minimum inverting gains at $\omega = 1$ are in fact determined by the limit values of the inverse of the memristance at $\omega = 1$:

$$\begin{aligned} \max\left(\frac{I_o}{V_i}\right) &= -\frac{1}{M_{min}} = -\frac{1}{374} = -2.67m\mho \\ \min\left(\frac{I_o}{V_i}\right) &= -\frac{1}{M_{max}} = -\frac{1}{14410} = -69.39\mu\mho \end{aligned} \tag{25}$$

The PHL of the transfer (Fig. 13) has a steep slope in the zero crossing when $t = \pi$. The plot of the gain as a function of time given in Fig. 14 shows how the gain drops very fast in the vicinity of this time value. In general, the sharpness of the gain and the PHL indicates a highly nonlinear behaviour of this amplifier.

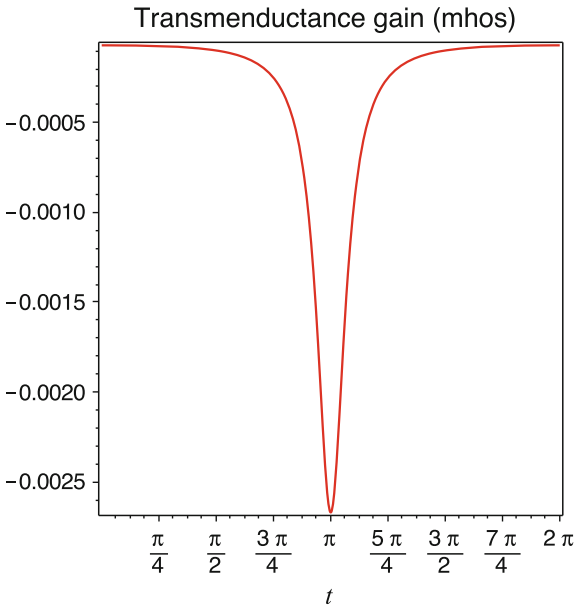

Fig. 14 Transmemductance gain for $\omega = 1$

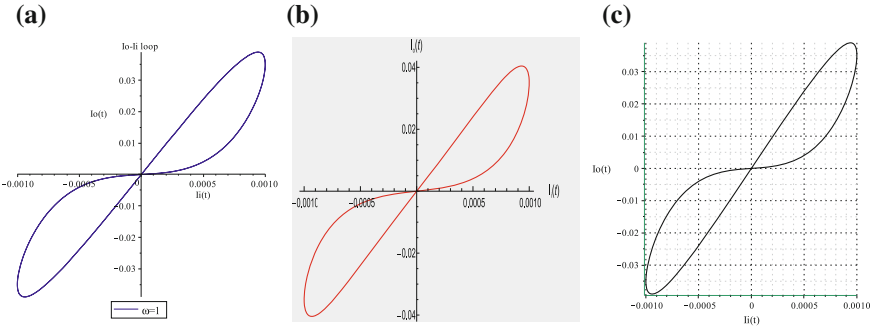

Fig. 15 Pinched hysteresis transfer loop for the transmemconductance amplifier for $\omega = 1$

3.4 Memristive Current Amplifier

The gain of this amplifier configuration is given as

$$\frac{I_o}{I_i} = 1 + \frac{M(t)}{R} \tag{26}$$

The $I_o - I_i$ transfer characteristic of the amplifier is shown in in Fig. 15.

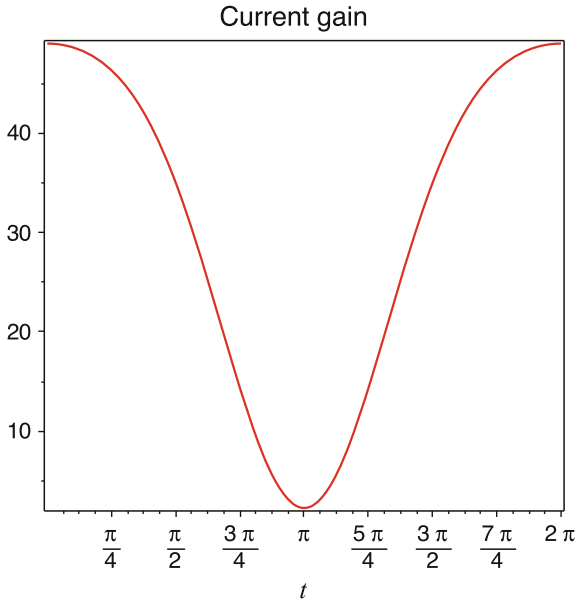

Fig. 16 Current gain for $\omega = 1$

The time-dependent gain is shown in Fig. 16. The maximum and minimum current gains are 49.03 and 2.24, respectively.

4 Noise Analysis

In the basic schemes of the nullor-based memristive amplifiers, the noise comes from the resistors and the memristor. This noise is of thermal nature, i.e. due to the thermal fluctuation of charge carriers. For the resistor, the noise can be represented as a series noise voltage source in series with the noise-less resistor—as shown in Fig. 17a. The power density can be expressed as:

$$\bar{v}_n^2 = 4kTR \qquad (V^2/Hz) \tag{27}$$

where T is the absolute temperature of the resistor, $k = 1.38^{-23}$ J/K is the Boltzmann constant and R is the value of the resistor. Norton equivalent allows us to express the noise current as:

$$\bar{i}_n^2 = \frac{4kT}{R} \qquad (A^2/Hz) \tag{28}$$

In order to determine how the noise of the memristor can be represented, it is useful to point out that the memristor model from Eq. (15) implies an ohmic relationship:

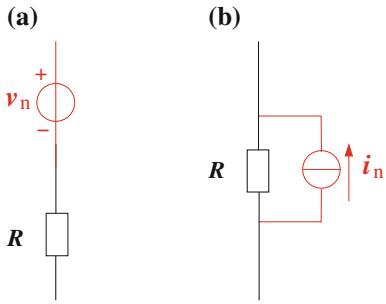

Fig. 17 Noise model of a resistor

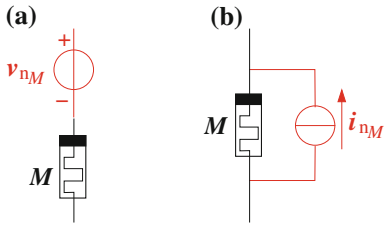

Fig. 18 Noise model of a memristor

$$v(t) = M(t)i(t) \tag{29}$$

In [30], under the assumption of instantaneous linearity, the noise of the memristor is regarded in a way similar to the noise in a linear resistor. Herein, the power density can be expressed as:

$$\bar{v}^2_{n_M} = 4kTM \tag{30}$$

The noise current is given as:

$$\bar{i}^2_{n_M} = \frac{4kT}{M} \tag{31}$$

The noise equivalents for the expressions above are given in Fig. 18.

4.1 Noise in the Memristive Amplifiers

Figure 19 shows the diagram of the memristive amplifiers with the sources of noise that contribute to the overall noise. As mentioned, the noise contributions arise from the source resistor R_s and the feedback network. For the case of the voltage and current amplifiers R and M are the noise contributors, while for the transmemristance and transmemductance amplifiers, M is the only contributor. Besides, even though the nullor is noiseless, two noise contributions are set apart for the nullor when it is synthesised by an active device in a forthcoming step, namely a noise voltage v_{n_n} and a noise current i_{n_n}.

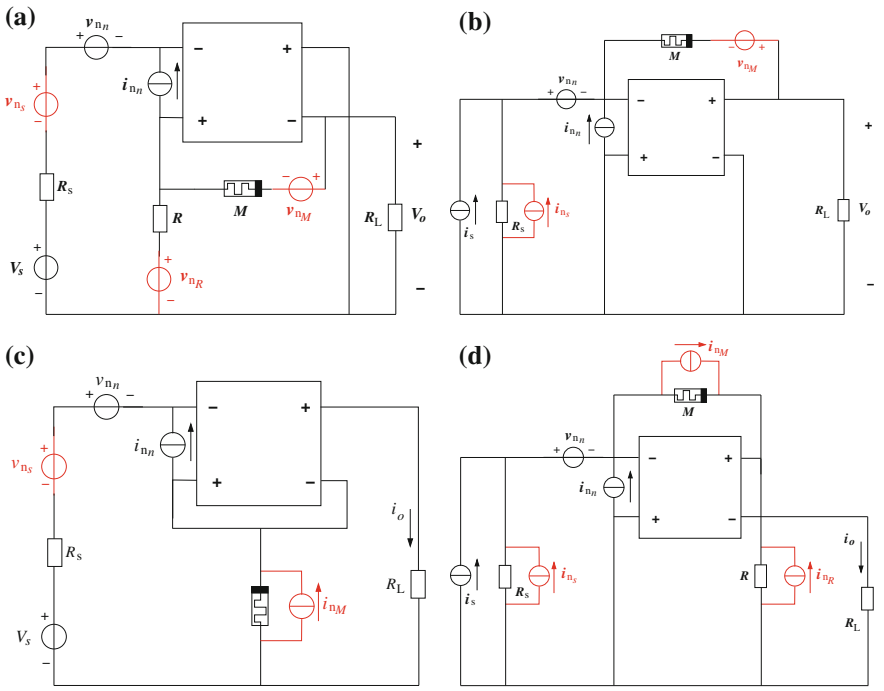

Fig. 19 Memristive amplifiers with noise sources: **a** Voltage amplifier **b** Transmemristance amplifier **c** Transmemductance amplifier **d** Current amplifier

The next step in the analysis consists in determining the so-called equivalent noise source at the input of the amplifier, which in fact models all noise contributions from the amplifier components. The noise sources present in the amplifier schemes from Fig. 19 must be reflected to the input by following several network transformations based on circuit theory [17]. The result is a fully symbolic expression for the total noise present at the input of the amplifier.

The total noise source at the input of the voltage amplifier is given as:

$$v_{n,eq,in} = v_{n_s} + v_{n_n} + (R_s + \frac{RM}{R+M})i_{n_n} + \frac{\frac{RM}{R+M}}{R}v_{n_R} + \frac{\frac{RM}{R+M}}{M}v_{n_M} \tag{32}$$

The total noise source at the input of the transmemristance amplifier is given as:

$$i_{n,eq,in} = i_{n_s} + i_{n_n} + (\frac{1}{R_s} + \frac{1}{M})v_{n_n} + \frac{1}{M}v_{n_M} \tag{33}$$

The total noise source at the input of the transmemductance amplifier is given as:

$$v_{n,eq,in} = v_{n_s} + v_{n_n} + (R_s + M)i_{n_n} + Mi_{n_M} \tag{34}$$

Table 3 Noise analysis of the memristive amplifiers

t	Voltage amplifier $R_S = 100\Omega, R = 300\Omega$		Transmemristance amplifier		Transmemductance amplifier		Current Amplifier $R_S = 10M\Omega, R = 300\Omega$	
	Evaluated	Simulated	Evaluated	Simulated	Evaluated	Simulated	Evaluated	Simulated
0	3.785344512 nV	2.5466 nV	1.112702349 pA	1.0697 pA	16.73449724 nV	15.4605 nV	1.242362347 pA	1.0588 pA
π	3.631962760 nV	2.0946 nV	6.690900784 pA	6.6352 pA	3.777004760 nV	2.7937 nV	7.037613172 pA	4.9428 pA

The total noise source at the input of the current amplifier is given as:

$$i_{n,eq,in} = i_{n_s} + i_{n_n} + (\frac{1}{R_s} + \frac{1}{M+R})v_{n_n} + \frac{R}{M+R}i_{n_R} + \frac{M}{M+R}i_{n_M} \tag{35}$$

In fact, Eqs. (32–35) represent the equivalent noise at the input of every amplifier. Evaluations of these equations and simulation with HSPICE are summarised in Table 3.

The deviations between evaluated and simulated results arise from the fact that the nullor has been approximated by high-gain controlled sources because of the lack of the nullor as a legal component in the simulator.

5 Harmonic Analysis

In this section, the memristor model described by Eq. (15) is used to obtain the symbolic expressions for the harmonic components of the output signal for the memristive configurations of the voltage and transmemristance amplifiers.

5.1 Harmonic Analysis for the Memristive Voltage Amplifier

The total harmonic distortion (THD) is a measure of the distortion in a system when its input is a sinusoidal signal. THD is expressed as:

$$THD = \frac{\sqrt{A_2^2 + A_3^2 + \cdots + A_n^2}}{A_1} \tag{36}$$

where A_i is the amplitude of the i-th harmonic, n is the maximum harmonic component considered in the analysis, and A_1 is the amplitude of the fundamental frequency. In fact, Eq. (36) is a comparison of the output amplitudes of all harmonic components with respect to the amplitude of the fundamental.

The output voltage of the nullor-based memristive voltage amplifier is given by:

$$v_{out} = \left(1 + \frac{M(t)}{R}\right) v_{in} \tag{37}$$

where $v_{in} = A\sin(\omega t)$ is the input voltage. The HPM memristor model from Eq. (15), expressed in harmonic form, is given as:

$$M(t) = C_0 + C_1\cos(\omega t) + C_2\cos(2\omega t) + C_3\cos(3\omega t) \tag{38}$$

After combining Eqs. (37) and (38), a symbolic expression for the output voltage can be obtained:

$$v_{out} = A\left[\left(1 + \frac{C_0}{R} - \frac{C_2}{2R}\right)\sin(\omega t) + \left(\frac{C_1}{2R} - \frac{C_3}{2R}\right)\sin(2\omega t) + \frac{C_2}{2R}\sin(3\omega t) + \frac{C_3}{2R}\sin(4\omega t)\right] \tag{39}$$

The amplitudes A_1, A_2, A_3 and A_4 can be easily identified as:

$$\begin{aligned} A_1 &= \left(1 + \tfrac{C_0}{R} - \tfrac{C_2}{2R}\right)A \\ A_2 &= \left(\tfrac{C_1}{2R} - \tfrac{C_3}{2R}\right)A \\ A_3 &= \tfrac{C_2}{2R}A \\ A_4 &= \tfrac{C_3}{2R}A \end{aligned} \tag{40}$$

The resulting symbolic expressions of the harmonic components are given as:

$$\begin{aligned} F_v &= A_{in}\left(1 + \tfrac{R_{init}}{R}\right) + A_{in}\tfrac{(\alpha-1)}{R}(\tfrac{56}{3}\mathcal{P}_3 - 10\mathcal{P}_2 + 4\mathcal{P}_1) \\ H_{2_v} &= A_{in}\tfrac{(\alpha-1)}{R}(-\tfrac{56}{3}\mathcal{P}_3 + 8\mathcal{P}_2 - 2\mathcal{P}_1) \\ H_{3_v} &= A_{in}\tfrac{(\alpha-1)}{R}(8\mathcal{P}_3 - 2\mathcal{P}_2) \\ H_{4_v} &= A_{in}\tfrac{(\alpha-1)}{R}(\tfrac{4}{3}\mathcal{P}_3) \end{aligned} \tag{41}$$

where F_v, H_{2_v}, H_{3_v}. and H_{4_v} stand for the fundamental, second, third and fourth harmonic components of the output voltage, respectively. Equation (41) constitutes indeed the symbolic harmonic model for the the memristive voltage amplifier. It should be pointed out that up to the fourth harmonic can be obtained in fully symbolic form due to the third-order of the memristor model from Eq. (15). The expressions above are normalised with respect to the fundamental, and they appear in Table 4 as the fully-symbolic expressions of the normalised harmonic components.

The voltage amplifier and the input and output signals obtained from the symbolic simulation are shown in Fig. 20, for $\omega = 1$. We have chosen this value for ω since the memristor exhibits its higher nonlinearity at this frequency. Therefore, the transfer function is given as:

$$\begin{aligned} \frac{V_o}{V_i} = 1 + \frac{M}{R}|_{\omega=1} &= 30.32984533 + 23.01811200\cos(t) \\ &-4.689100800\cos(2t) + 0.3744768000\cos(3t) \end{aligned} \tag{42}$$

This expression has been obtained by using the memristor model given in Eq. (15) with the nominal values from Table 1, and $R = 300\Omega$. Numerical evaluations and simulation results are shown in columns 3 and 4 of Table 4, respectively. Simulation

Table 4 Normalised symbolic harmonic analysis for the memristive voltage amplifier

Memristive voltage amp.	**Normalised symbolic**	Evaluated	HSPICE simulations
F	1	1	1
H2	$-2\frac{(\alpha-1)\left(\mathcal{P}_1-4\,\mathcal{P}_2+\frac{28}{3}\,\mathcal{P}_3\right)}{(\alpha-1)\left(4\mathcal{P}_1-10\mathcal{P}_2+\frac{56}{3}\mathcal{P}_3\right)+R+Rinit}$	346.504 m	345.7994 m
H3	$-2\frac{(\alpha-1)\left(\mathcal{P}_2-4\,\mathcal{P}_3\right)}{(\alpha-1)\left(4\mathcal{P}_1-10\mathcal{P}_2+\frac{56}{3}\mathcal{P}_3\right)+R+Rinit}$	71.7549 m	72.2021 m
H4	$-\frac{4}{3}\frac{(\alpha-1)\mathcal{P}_3}{(\alpha-1)\left(4\mathcal{P}_1-10\mathcal{P}_2+\frac{56}{3}\mathcal{P}_3\right)+R+Rinit}$	5.7304 m	5.5046 m
H5	–	–	189.0610 μ
THD%		35.39	35.33

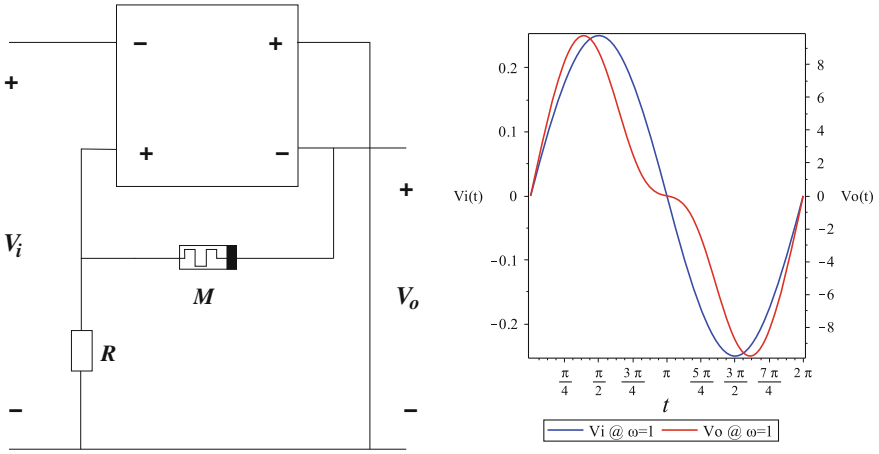

Fig. 20 Voltage amplifier with input and output voltages for $\omega = 1$

have been obtained by using HSPICE with the memristor model recast as a Verilog-A module.

A similar procedure is carried out in order to derive the expressions for symbolic harmonics for the rest of amplifiers.

5.2 Harmonic Analysis for the Transmemristance Amplifier

The transmemristance amplifier and the input and output signals obtained are shown in Fig. 21 for $\omega = 1$. The transfer function at this frequency is given as:

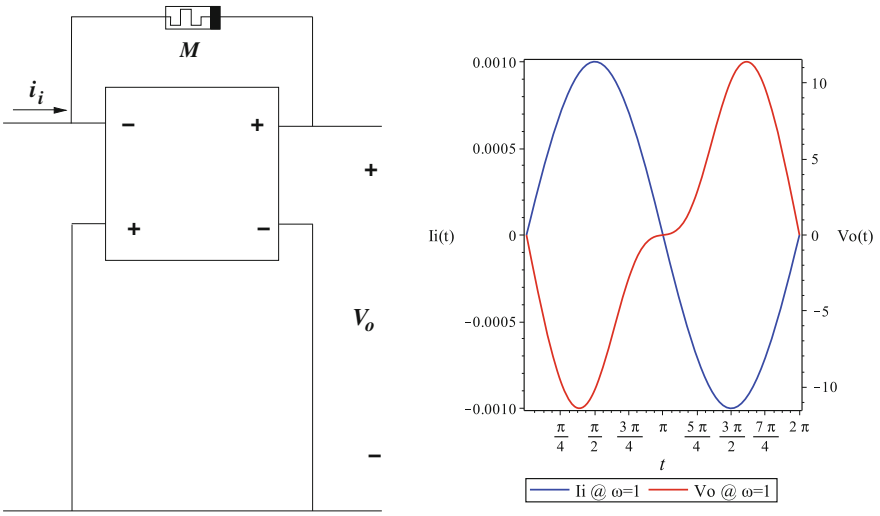

Fig. 21 Transmemristance amplifier with input current and output voltage for $\omega = 1$

Table 5 Normalised symbolic harmonic analysis for the transmemristance amplifier

Transmemristance amplifier	**Normalised symbolic**	Evaluated	HSPICE simulations
F	1	1	1
H2	$-2\frac{(\alpha-1)\left(\mathcal{P}_1-4\mathcal{P}_2+\frac{28}{3}\mathcal{P}_3\right)}{(\alpha-1)\left(4\mathcal{P}_1-10\mathcal{P}_2+\frac{56}{3}\mathcal{P}_3\right)+Rinit}$	357.44 m	355.7455 m
H3	$-2\frac{(\alpha-1)\left(\mathcal{P}_2-4\mathcal{P}_3\right)}{(\alpha-1)\left(4\mathcal{P}_1-10\mathcal{P}_2+\frac{56}{3}\mathcal{P}_3\right)+Rinit}$	74.0203 m	73.9590 m
H4	$-\frac{4}{3}\frac{(\alpha-1)\mathcal{P}_3}{(\alpha-1)\left(4\mathcal{P}_1-10\mathcal{P}_2+\frac{56}{3}\mathcal{P}_3\right)+Rinit}$	5.9113 m	5.8484 m
H5	–	–	174.7701 μ
THD%		36.507	36.34

$$\frac{V_o}{I_i} = -M|_{\omega=1} = -8798.953600 - 6905.433600\cos(t) + 1406.730240\cos(2t) - 112.3430400\cos(3t) \tag{43}$$

The symbolic harmonic model yields the expressions of the harmonic components as:

$$\begin{aligned} F_m &= A_{in}R_{init} + A_{in}(\alpha-1)(\tfrac{56}{3}\mathcal{P}_3 - 10\mathcal{P}_2 + 4\mathcal{P}_1) \\ H_{2_m} &= A_{in}(\alpha-1)(-\tfrac{56}{3}\mathcal{P}_3 + 8\mathcal{P}_2 - 2\mathcal{P}_1) \\ H_{3_m} &= A_{in}(\alpha-1)(8\mathcal{P}_3 - 2\mathcal{P}_2) \\ H_{4_v} &= A_{in}(\alpha-1)(\tfrac{4}{3}\mathcal{P}_3) \end{aligned} \tag{44}$$

From Eq. (44), the normalised harmonic components can be obtained also in fully-symbolic form, as shown in Table 5. Columns 3 and 4 of this table show the evaluated and simulated results respectively.

5.3 *Harmonic Analysis for the Transmemductance Amplifier*

The transmemductance amplifier and the input and output signals are shown in Fig. 22 for $\omega = 1$. The transfer function is given as:

$$\frac{I_o}{V_i} = -\frac{1}{M}|_{\omega=1} = -[8798.953600 + 6905.433600\ \cos(t) - 1406.730240\ \cos(2\,t) + 112.3430400\ \cos(3\,t)]^{-1} \tag{45}$$

From the waveform of the output current, it follows that this amplifier exhibits the most nonlinear behaviour, which is a direct result of obtaining the transmemductance transfer function by inverting the memristance expression as denoted in Eq. (45). In fact it conveys to a sec-like function, which is well known for having discontinuities. Simulations results permits to verify this, as shown in Table 6.

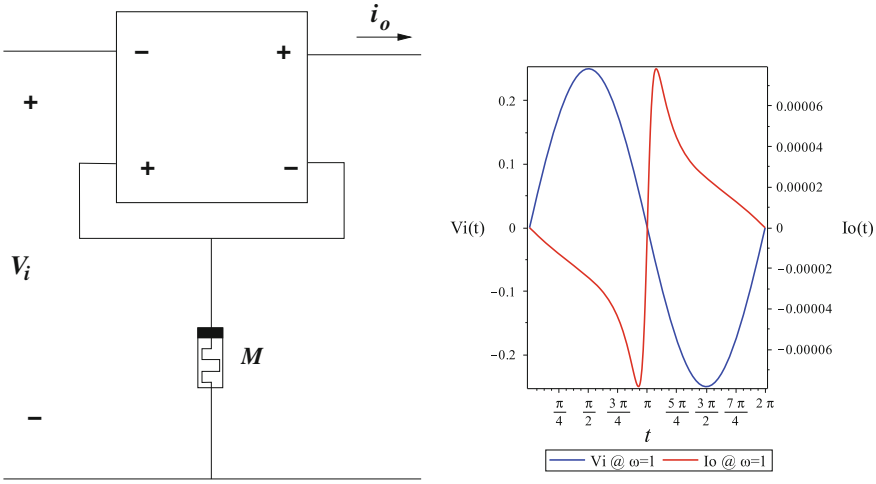

Fig. 22 Transmemductance amplifier with input voltage and output current for $\omega = 1$

Table 6 Harmonic analysis for the transmemductance amplifier: simulation results

Transmemductance amplifier	HSPICE simulations
F	1
H2	650.9889 m
H3	574.5942 m
H4	−462.3486 m
H5	211.1704 m
THD%	105.654

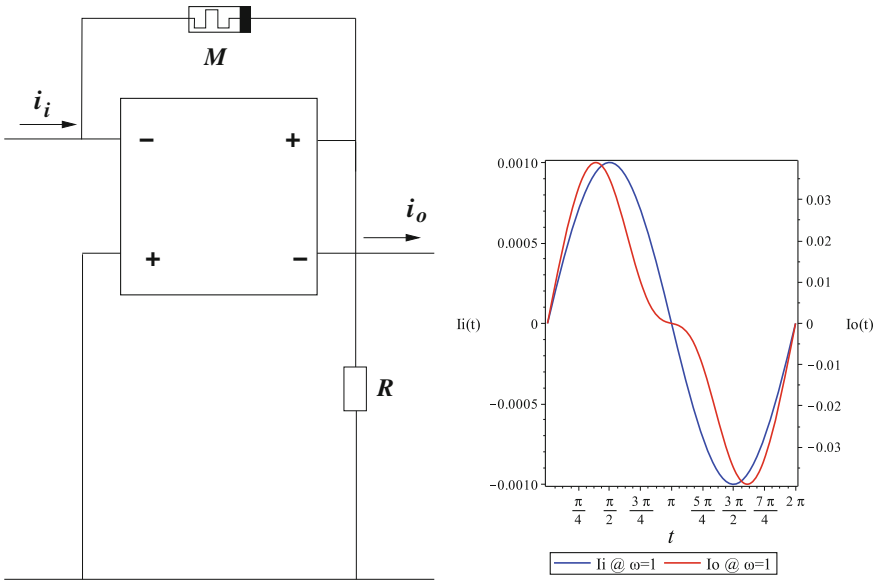

Fig. 23 Current amplifier with input and output currents for $\omega = 1$

5.4 *Harmonic Analysis for the Current Amplifier*

For this amplifier, its diagram as well as the input and output currents are shown in Fig. 23 for $\omega = 1$.
The memristive transfer function is:

$$\frac{I_o}{I_i} = 1 + \frac{M}{R}|_{\omega=1} = 30.32984533 + 23.01811200\cos(t) - 4.689100800\cos(2t) + 0.3744768000\cos(3t) \quad (46)$$

which results identical to the transfer function of the memristive voltage amplifier. As a clear result, the harmonic analysis yields the same symbolic and numerical results.

6 Implementing the Nullor with a Memistor

The synthesis of the nullor with active devices has been already matter of study by several researchers and scholars [11, 12, 17–19, 33, 34]. The synthesis methodology is carried out by attending a series of design guidelines with the aim of fulfilling the user specifications. In particular, the research just mentioned has been focused on tackling noise, distortion and bandwidth.

Hereafter, the nullor is implemented by a memistor. The memistor is a concept introduced by Widrow in the form of three-terminal memory resistor [35]. Not only does the name "memistor" imply a natural a confussion with the name of the "memristor", but it also brings into light the link between both concepts, as reported in [36–38].

The nullor is implemented by a memistor consisting in two memristors connected back-to-back (anti-series connection) in order to establish a two-port network. The nullor implementation results from setting an end terminal of the anti-series connection as the common terminal of the two-port, as depicted in Fig. 24. The memristor model given by Eq. (15) is used to describe the memristors that appear in the scheme.

Noise in the memistor

As established before, the memristor contributes with noise in the same form a resistor does, and as a result of this, all possible sources of noise were treated in Sect. 4. In addition, the noise contributions for the nullor were temporarily set aside because of the ideal properties of the nullor. However, Eqs. (32–35) already considered the forthcoming noise contributions of the nullor when it is synthesised with devices.

In our nullor implementation with a memistor, i.e. a pair of memristors M_D and M_S, it clearly results that they contribute with noise currents as depicted in Fig. 25.

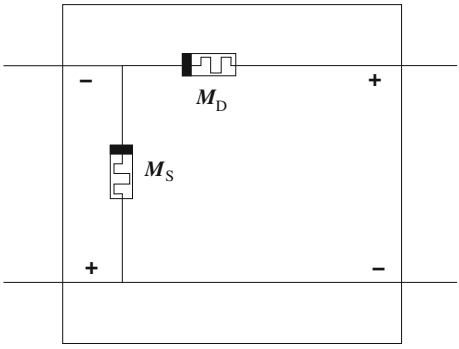

Fig. 24 Nullor implementation with memistor

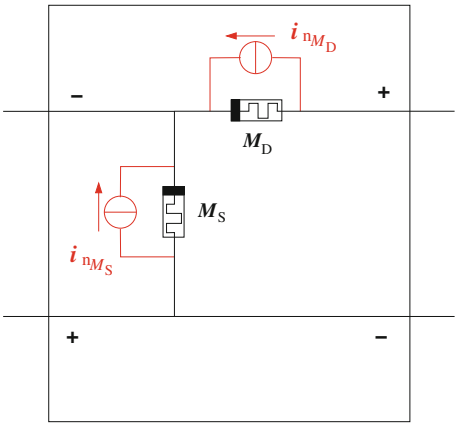

Fig. 25 Memistor with noise contributions

Table 7 Noise equivalent at the input of the memristor from evaluation of Eq. (48)

t	i_{n_n}	v_{n_n}
0	4.288033476 pA	15.44764060 nV
π	26.60082721 pA	24.90148125 nV

According to Eq. (31), the noise currents for the memristors are given by:

$$\begin{aligned} \bar{i}^2_{n_{M_S}} &= \frac{4kT}{M_S} \\ \bar{i}^2_{n_{M_D}} &= \frac{4kT}{M_D} \end{aligned} \tag{47}$$

After manipulating the $i_{n_{M_S}}$ and $i_{n_{M_D}}$, the amount of equivalent noise present at the input of the memistor two-port can be expressed as:

$$\begin{aligned} i_{n_n} &= i_{n_{M_S}} + \left(1 + \frac{M_S + M_D}{M_S}\right) i_{n_{M_D}} \\ v_{n_n} &= M_D i_{n_{M_D}} \end{aligned} \tag{48}$$

Both expressions are incorporated to Eqs. (32–35) in order to calculate the total noise present at the input of the amplifiers.

The equivalent noise contributions at the input of the memistor from Eq. (48) are evaluated at $t = 0, \pi$ and the values are summarised in Table 7.

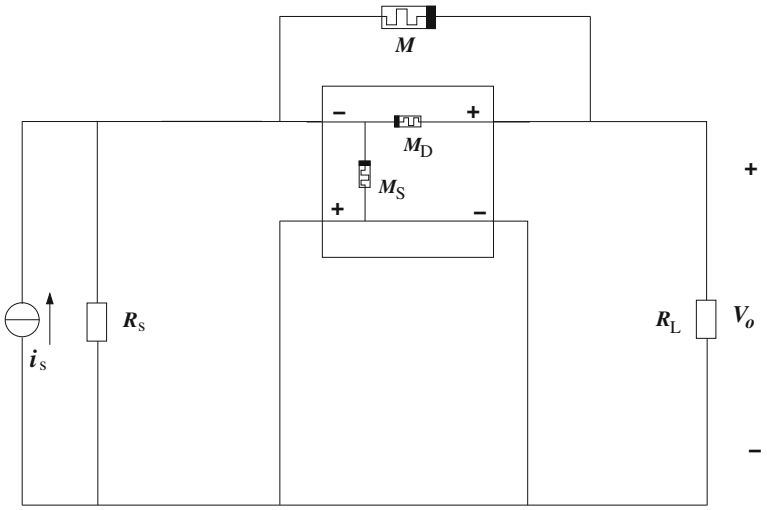

Fig. 26 Case study: Transmemristance amplifier with memistor

Table 8 Total noise present at the input of the transmemristance amplifier using memistor

t	Transmemristance amp.	
	Evaluated	Simulated
0	1.112702349 pA	1.3118 pA
π	6.690900783 pA	8.1268 pA

6.1 A Case Study: The Transmemristance Amplifier

As an example of the use of the memistor for determining a transmemristive transfer in a nullor-based amplifier, the transmemristance amplifier is designed by resorting to the memistor configuration. This is schematically shown in Fig. 26.

Noise simulations

Fig. 27 depicts the transmemristance amplifier with all components having attached the noise contributions. In fact the contributions of the nullor, namely v_{n_n} and i_{n_n}, are result of Eq. (48). The memristor of the feedback network (M), and the memristors of the memistor (M_S and M_D) are modelled by Eq. (15). It is possible to determine that the total noise at the input of the amplifier can be expressed as:

$$i_{n,eq,in} = i_{n_s} + i_{n_{M_S}} \tag{49}$$

Evaluations of Eq. (49) and results from HSPICE simulations are recast in Table 8 for $t = 0, \pi$.

Harmonic analysis

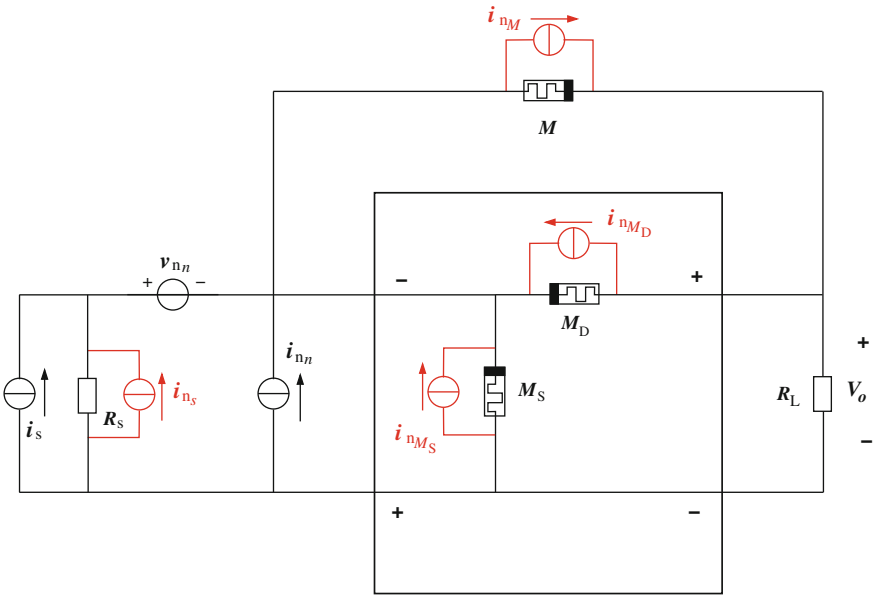

Fig. 27 Case study: noise contributions in the transmemristance amplifier

Table 9 Normalised symbolic harmonic analysis for the transmemristance amplifier

Transmemristance amplifier	Nullor		Memistor
	Evaluated	Simulated	Simulated
F	1	1	1
H2	357.44 m	355.7455 m	356.1120 m
H3	74.0203 m	73.9590 m	73.8547 m
H4	5.9113 m	5.8484 m	5.7772 m
H5	–	174.7701 µ	170.0354 µ
THD%	36.507	36.34	36.3736

Table 9 shows the simulation results of the amplifier for the harmonic analysis. The columns corresponding to the memristive amplifier when using an ideal nullor are repeated from Table 5 for sake of comparison.

Finally, Fig. 28 shows plots from simulation of the input current and output voltage of the transmemristance amplifier.

7 Conclusions

In this chapter, a strategy for the design of nullor-based memristive amplifiers with memistor realization of the nullor has been presented. A direct result of this strategy is that the final implementation of the amplifier results in a full memristive circuit. Moreover, a fully symbolic memristor model is introduced and the most important fingerprints are highlighted. This model is used along the analysis and design steps. The model has been recast as a behavioural model in Verilog-A. In the first stage, the memristive amplifiers are composed by the nullor and a memristive feedback network. Herein, noise and harmonic analyses are carried out with symbolic and numerical simulations. In the second stage, the nullor is implemented by a memistor, i.e. an anti-series connection of 2 memristors. Special attention has been devoted to the noise contribution the memistor. Finally, a transmemristance amplifier has been used as case study for the memistor implementation of the nullor, and noise and harmonic analyses were also done.

8 Appendix

The memristor model given in Eq. (15) has been coded in Verilog-A. The `.va` file is given hereafter:

```
`include "const.va"
```

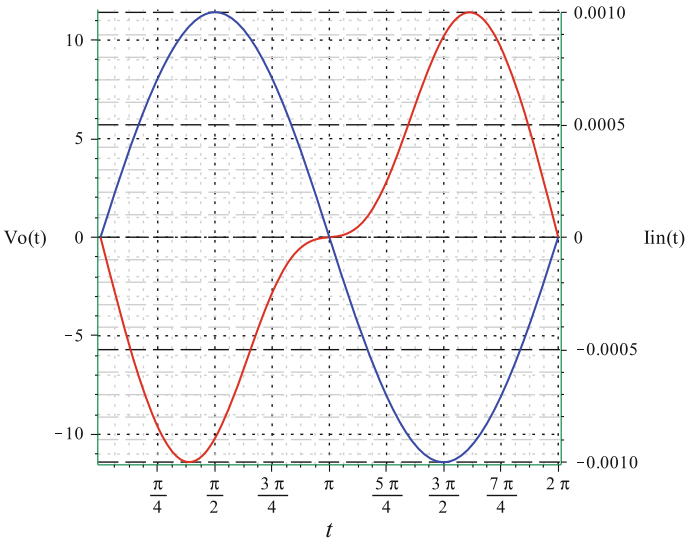

Fig. 28 V_o and I_i of the transmemristance amplifier with memistor: simulated results

```
`include "std.va"
`include "disciplines.vams"
module Memristor(in,out);
    inout in,out;
    electrical in,out;
    parameter  real Delta = 10.0e-9;
    parameter  real Pi = 3.1416;
    parameter  real Ron = 100;
    parameter  real  mu = 1.0e-14;
    parameter  real  alpha = 160;
    parameter  real  Ap = 40.0e-6;
    parameter  real  omega = 1;
    parameter  real  Xo = 0.1;
    real mem, Rinit, p1, p2, p3, p4;
analog begin
Rinit=(Xo+(alpha*(1-Xo)))*Ron;
p1 = ((mu*Ap)/(Delta*Delta*omega))*Xo*(Xo-1)*Ron*Ron;
p2 = pow(((mu*Ap)/(Delta*Delta*omega)),2)*Xo*(Xo-1)*(2*Xo-1)*pow(Ron,3);
p3 = pow(((mu*Ap)/(Delta*Delta*omega)),3)*Xo*(Xo-1)*((6*Xo*Xo)-6*Xo+1)*pow(Ron,4);
mem=(alpha-1)*(
                    (16*p2-40*p3-4*p1)*cos(omega*($abstime))+
                    (16*p3-4*p2)*cos(2*omega*($abstime))-
                    ((8*p3)/3)*cos(3*omega*($abstime))+
                    ((80*p3)/3-12*p2+4*p1)
                )+Rinit;
I(in,out)<+(V(in,out))/mem;
end
endmodule
```

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