Chapter 1
An Introduction on Phase-Change Memories

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1.1 Introduction

The phase-change memory (PCM), also called ovonic unified memory (OUM) or phase-change RAM (PCRAM), is an emerging nonvolatile semiconductor technology based on thermally induced phase transitions of a thin-film chalcogenide material [1]. PCM relies on a resistance change to store data permanently. However, the historical origin of the PCM concept that dates back in the 1970s and the research efforts specifically devoted to this technology by semiconductor industries set them apart from the larger class of emerging memory technologies based on resistance variation and usually referred to as resistive RAM (ReRAM).

The PCM device is essentially a resistor of a thin-film chalcogenide material, usually a Ge–Sb–Te alloy [2] with a low-field resistance that changes by orders of magnitudes, depending on the phase state of the material in the active region (i.e., crystalline or amorphous). In memory operation, cell readout is performed at low bias by sensing the resistance value. Programming requires instead a relatively large current, in order to heat up the chalcogenide material and lead to a thermally induced local phase change. Phase transitions can thus be easily obtained by applying voltage pulses with different amplitudes and with durations in the range of tenths of nanoseconds [3].

Such technology is one of the most promising candidates for next-generation nonvolatile memories (NVM) [4–6] having the potentiality to improve the performance compared to flash – random access time and read throughput (versus NOR flash), write throughput (versus NAND flash), direct write, bit granularity, and endurance – as well as to be scalable beyond flash technology [7].

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1.2 PCM Historical Development

PCM technology relies on the unique electrical properties shown by amorphous chalcogenide alloys. They are compounds with at least one element of the VI group of the chemical table of elements (chalcogens), usually combined with elements of the IV (carbon group elements like silicon and germanium) and V groups (pnictogens). Research on the electronic properties of amorphous chalcogenides dates back to the original work of Ovshinsky in the ’50s. From 1958 to 1961, he investigated the chemical and the electrical properties of chalcogenide alloys, demonstrating their electrical behavior as amorphous semiconductors and discovering the existence of reversible switching effects [9].

The unique electrooptical properties of amorphous chalcogenides found a first commercial application in the ’70s of the last century for the xerography technology [10, 11], a dry photocopying technique. In this equipment, amorphous selenium was employed for covering the drum used for transferring the ink, exploiting its photoconductive properties that allowed to hold an electrostatic charge in darkness and to conduct it away under light. In those years, the idea of exploiting the huge reversible resistance variation observed in some chalcogenide alloys was proposed for fabricating a solid-state NVM device [10, 12, 13]. It is worth mentioning that the possible exploitation of amorphous chalcogenide for both electrically alterable read-mostly memories and optical storage application based on laser light was largely discussed in [14] by R. G. Neale and J. A. Aseltine. Compared to the first PCM prototype chip described in [12], a second, more efficient, 256-bit array (Fig. 1.1) was proposed where the selecting device, a diode, is placed under the chalcogenide storage element to save additional space and reduce costs. Unfortunately, the chalcogenide alloys used in that first attempt of PCM device was characterized by a slow transition speed and high programming currents, thus making PCM technology not suitable for commercialization.

A significant development in the comprehension of chalcogenide glass physics and for its exploitation in commercial application was achieved starting from the

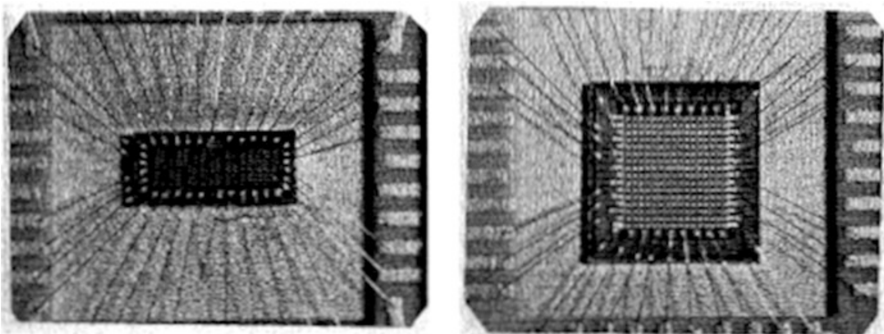

Fig. 1.1 Vertically stacked 256-bit array (left) shown for size comparison with the original 256-bit integrated array (right) [14]

1990s. The Ovshinsky-founded company, Energy Conversion Devices, Inc., developed an amorphous semiconductor alloy made by germanium, antimony, and tellurium, or Ge–Sb–Te (GST), and exploited it in the phase-change technology used in rewritable optical disks [15, 16]. In phase-change optical storage applications, the information storage relies on a laser-induced reversible phase transition [17–19]. A focused laser pulse heats up the GST, which induces the change between the amorphous and the crystalline phases. Since the two phases feature a different reflectance, the optical readout is performed with a low-power probing optical pulse. The GST alloy compositions developed for optical disk at the end of the 1990s are able to switch between the amorphous and the crystalline phase in tens of nanosecond, several orders of magnitude less than the chalcogenide alloys originally employed in the prototype 256-bit PCM device [3, 20, 21]. This achievement renewed the interest of the semiconductor industries on solid-state PCM devices, and several research programs were started around the end of the millennium [2, 3].

In this case, the idea is to induce electrically the phase change in a GST cell and to associate the stored information to the corresponding high and low resistance values. Since both states are stable, no energy is required to keep data stored, resulting in an inherently NVM technology. In order to exploit the PCM concept in solid-state memory devices, the storage element based on the chalcogenide alloy must be coupled with a selecting device that allows to select the individual memory cells for reading and writing. To this purpose, metal–oxide–semiconductor field-effect transistors (MOSFETs) [4], bipolar junction transistors (BJTs) [2], and diodes [22] have been proposed.

The technology development road map of PCM is reported in Fig. 1.2. A test chip fabricated at the 180 nm technology node was used to develop the first demonstrator vehicles and to prove the technology viability [2]. The BJT-selected cell was chosen for the high-performance and high-density application, since the cell size can be $8F^2$ (where F is the minimum cell half-pitch) down to $4F^2$. The MOSFET-selected cell is instead suitable for system-on-chip or embedded application [23], because in spite of the larger cell size (~$20F^2$), the memory integration adds only very few masks to the logic process with a clear cost advantage.

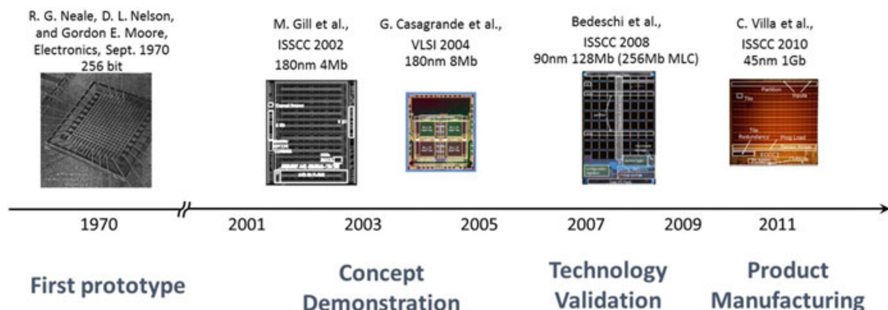

Fig. 1.2 Timeline for the development of PCM technology from the first prototype to the commercial volume production

Successively a 90 nm technology node was developed and a 128 Mb PCM product was commercialized [24]. At this stage of development, PCM was able to deliver legacy performances for NOR replacement as well as new features related to the finer bit granularity and alterability and to the extended endurance capability. Similar preproduction full-spec devices used for the technology development were claimed in [22] with a 512 Mb array at 90 nm technology node. Finally, a 1 Gb PCM product fabricated at the 45 nm technology node with a cell size of $5.5F^2$ was developed, and it has been produced for wireless application [8]. The 45 nm PCM product clearly demonstrates the maturity of the technology [8]. The energy delivered to program a bit is in the order of 10pJ, with a state-of-the-art access time of 85 ns, read throughput of 266 MB/s, and write throughput of 9 MB/s [25]. These peculiar features combined with data retention, single-bit alterability, execution in place, and good cycling performance enable traditional NVM utilizations and novel applications. A similar PCM product has been reported in [26] with a full product based on a 58 nm node technology and with a low-power double-data-rate nonvolatile memory (LPDDR2-NVM) interface. Moreover, PCM is considered one of the best candidates to push to the market the so-called storage-class memory (SCM) [27], a nonvolatile solid-state memory technology that is capable of filling the gap between CPU and disks.

1.3 PCM Working Principle and Device Physics

Some alloys based on the VI group elements (usually referred as chalcogenides) have the interesting characteristic to be stable at room temperature both in the amorphous and in the crystalline phase. In particular, the most promising are the GeSbTe alloys which follow a pseudo-binary composition (between GeTe and Sb_2Te_3), hereafter referred to as GST. The most interesting feature of these alloys is their capability to reversibly switch between a high-resistance amorphous phase and a low-resistance crystalline one in few hundreds of nanoseconds.

The PCM cell is essentially a resistor of a thin-film chalcogenide material with a low-field resistance that changes by orders of magnitudes, depending on the phase state of the GST in the active region. The switch between the two states occurs by means of local temperature increase. Above the critical temperature, the crystal nucleation and growth occur and the material becomes crystalline (set operation). To bring the chalcogenide alloy back to the amorphous state (reset operation), the temperature must be increased above the melting point of hundreds of °C and then very quickly quenched down in order to preserve the disorder and not let the material to crystallize. From an electrical point of view, it is possible to use the Joule effect to reach locally both critical temperatures using the current flow through the material by setting proper voltage pulses (Fig. 1.3).

Depending on the GST phase, the memory device features the electrical characteristics depicted in Fig. 1.3b. The crystalline GST (xGST) behaves as a resistor with a slope mainly determined by the heater resistance itself. The amorphous

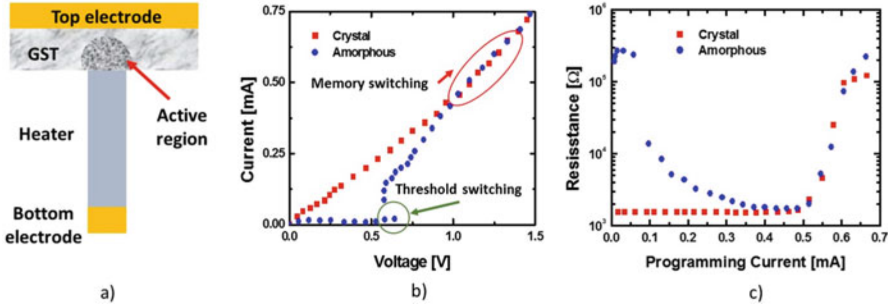

Fig. 1.3 Prototype 180 nm PCM cell (**a**) current voltage characteristics of the cell with the GST in the crystalline and amorphous phase (**b**) and corresponding programming curves (**c**)

phase (aGST) shows an S-shaped negative differential conductance (SNDC), collapsing from a high resistive off-state into a high conductive on-state through the so-called threshold switching effect [28]. Figure 1.3c shows the cell resistance measured after a current pulse of varying amplitude and a duration of 100 ns. Both types of state transitions are shown in the figure: for the reset-to-set transition, the cell was always prepared in the reset state (R $\approx$ 1.5 MΩ) prior to the application of the program pulse. In this case, the programmed resistance steeply decreases for programming currents greater than 100 µA, due to the crystallization of amorphous GST in the active region. The figure also shows the opposite (set-to-reset) transition, where the cell is prepared in the low-resistance state ($R \approx 3\text{k}\Omega$). Here, the cell resistance remains unchanged for moderately small programming currents and then markedly increases for current values greater than 450 µA. This marks the GST melting within the active region. In fact, rapid cooling of the melted chalcogenide along the falling edge of the program pulse results in a final amorphous phase, increasing cell resistance. Note that the falling edge is a critical parameter in the set-to-reset transition: if the falling edge is not fast enough, the melted GST may recrystallize leading to a final state with lower resistance.

From Fig. 1.3b, it is worth noting that there exist two electrically driven switching effects in chalcogenide glasses, as already pointed out in the pioneering work of Ovshinsky [9, 29]. The first one is related to the reversible switching mechanism between an electrical low conductive state and a high conductive one, without any change in the microscopic structure of the material. Since this mechanism requires a threshold voltage and is usually associated with SNDCs, it has been named threshold switching. A second mechanism was also discovered in some chalcogenide compounds, this one related to a thermally activated phase transition of the chalcogenide alloy that can be switched between a high conductive polycrystalline state and a low conductive amorphous one, through proper electrical pulses that cause a Joule heating of the material. Since both the crystalline and the amorphous states are stable, the two phases could be used to store binary information in a nonvolatile memory device, the bit "1" corresponding to the conductive state and the bit "0" to the insulating one. This electrically induced structural

change has been thus named memory switching. It is worth noting that the threshold switching effect is required to get the memory switching mechanism but not vice versa. In fact, an amorphous chalcogenide has to be driven in a highly conductive electrical state through threshold switching to get the transition temperatures without enormous electrical fields [9, 30].

1.4 PCM Device Performance and Applications

PCM represents one of the most promising candidates for next-generation NVM devices [31–33], having the potentiality to improve the performance compared to flash with an exceptional scalability [34]. To exploit the PCM technology for high-performance applications, fast write and read times are mandatory while still preserving good data retention capabilities (Table 1.1).

Compared to other memory technologies, PCM can fill the performance/cost gap between DRAM and NAND, and they can provide a full replacement for NOR flash with a better scalability. In looking at application requirements in comparison with the current memory hierarchy, a very interesting opportunity can be identified for a memory technology with properties in between DRAM and NAND, both in terms of latency and cost. Such a memory system, conventionally defined as storage-class memory (SCM), represents the ideal realm for PCM technologies due to their low-power capabilities. However, stringent requirements in terms of speed and cost must also be met. As reported in Table 1, PCM can deliver much better performance than flash in terms of latency and speed with the attribute of good bit granularity and nonvolatile nature of the storage mechanism.

This perspective PCM technology can be effectively exploited in:

(i) Wireless systems, where LPDDR2-NVM PCM devices have latency in the same order of magnitude as DRAM, could reduce cost and power consumption in the system and can offer reduced application start time and reduced boot time through execute-in-place (XiP) operation.

Table 1.1 Comparison of key attributes among PCM, floating-gate NVM (NOR and NAND flash), and DRAM

Attributes	PCM	NOR	NAND	DRAM
Nonvolatile	Yes	Yes	Yes	No
Clear scaling to	1× nm	45 nm	1× nm	1× nm
Granularity	Small/byte	Large	Large	Small/byte
Erase	No	Yes	Yes	No
Software	Easy	Moderate	Hard	Easy
Power	~Flash	~Flash	~Flash	High
Write bandwidth	1–15+ MB/s	0.5–2 MB/s	10+ MB/s	100+ MB/s
Read latency	50–100 ns	70–100 ns	15−50us	20–80 ns
Endurance	10^6+	10^5	10^4–10^5	Unlimited

(ii) Solid-state storage subsystem to store frequently accessed pages and to store those elements which are more easily managed when manipulated in place. A key advantage is the bit alterable nature of PCM that solves the issue of increased write cycles when the device is full. Higher endurance on PCM addresses the needs of these systems when heavy use is expected.

(iii) PCIe-attached storage arrays, where the fast random read/write operations allow performances much higher than in state-of-the-art flash-based SSD [35].

(iv) Computing platform, exploiting the non-volatility to reduce the power consumption. DRAM, being a volatile memory, consumes watts/GB to simply maintain the contents of the memory. PCM banks can be simply turned off when they are not in use providing reduced power in idle states and decoupling the relationship between density and power consumption.

In order to be able to enter into a well-established memory market, there are key factors that must be fulfilled: (i) match the cost of the existing technology in terms of cell size and process complexity, (ii) find application opportunities optimizing the overall “memory system,” and (iii) provide a good perspective in terms of scalability. PCM has been able so far to progress in line with all these requirements.

One of the key challenges that must be faced for industrializing PCM devices is the large programming current needed to melt the cell active region. Such current value may become a limitation in all the applications with a limited budget for power consumption, and it imposes stringent requirements on the current delivered by the memory cell selector integrated in series with the PCM. If the current density delivered by the selecting device is lower than the one required by PCM cell, the selector area must be increased; thus, the size of the cell selecting device becomes the limiting factor for the device density and annihilates the small size advantage of PCM technology. Therefore, reducing the programming current is necessary for achieving both high density and low power consumption of PCM.

Memory cells organized in an array must have a means to select the individual memory cells for reading and writing (RAM operation). The memory cell selection device ensures there is no parasitic current path, the selected cell is writable, and there is adequate read signal-to-noise margin. Ideally, the memory cell selection device has high on-state conductivity and infinite off-state resistance and occupies a small layout area. BJTs and diodes have similar device structures, differing only in the doping of the junctions and the number of contacts [36]. Diodes can have the minimum $4F^2$ layout area. By sharing the base contact with several cells, the footprint of a BJT selector ranges from $8F^2$ [2] to about $5.5F^2$ [8]. The device width of the MOSFET selector is determined by the programming current required. PCM requires a substantial reset programming current that calls for good-quality diode/BJT or wide device width for a MOSFET selector. PN junction diodes with various materials have been studied, including poly-Si, epitaxially grown silicon, doped semiconducting metal oxide, and Ge nanowire: in all these attempts, it has been difficult to find a cell selection diode that simultaneously satisfies the on/off ratio requirement and the on-current required to program the PCM.

1.5 Conclusions

PCM technology represents a serious contender in the emerging NVM arena, being the only technology that has been capable to demonstrate the maturity for large-volume manufacturing at the state-of-the-art technology node. Good electrical performances, superior reliability, and bit granularity can provide a competitive advantage over the mainstream flash technology and make them a good candidate for storage-class memory applications. In order to reduce the cell size and therefore the cost of this technology, two approaches have been deeply investigated in the last decade. First, several alternative cell architectures have been proposed to minimize the programming current. Second, various selecting devices have been experimented to find the optimal solution for different applications and requirements. Finally, MLC and neuromorphic applications represent today the leading edge for the research activities on PCM technology, and they may allow a giant leap for their exploitation in the next years.

With respect to traditional electron device based on the electrical transport properties of silicon, PCM devices exploit several effects that are not usually accounted for in semiconductor devices, at least in solid-state memories. In fact the electrical properties are strongly coupled with the thermal ones, thus requiring to consider the electrothermal physics for all the operating condition of PCM devices. Moreover, for the first time in semiconductor history, the phase-change properties and related physics represent a key topic for device understanding and optimization, thus asking to researchers and engineers operating in this field for new expertise and skills. The aim of this book is to provide a comprehensive treatment of the PCM device physics, including the most recent advances in the modeling of such phenomena and in the comprehension of new chalcogenide material properties, as well as a deep insight in the engineering challenges from the single device to large-sized PCM products.

The electrical properties of amorphous and crystalline chalcogenide alloys have been long debated in the scientific community due to the peculiar features that are unique for these alloys. Chapter 2 reports a complete review of the conduction mechanisms responsible for the subthreshold behavior in chalcogenide alloy as well as the key ingredients to explain the threshold switching phenomenon. Thermal properties and phase-change dynamics are the topic for Chap. 3, with a focus on the phenomena involved in the transition from the amorphous to the crystalline phase. Crystallization dynamics represents the slowest mechanism in PCM operation, and a deep analysis of the crystal nucleation and growth mechanisms is mandatory for the optimization of the device performance. Electrical, thermal, and phase-change physics are then combined in a self-consistent environment described in Chap. 4 and that allow the reader to understand the cross-links between the various mechanisms involved in PCM operations. Apart from the exceptional performance in terms of read and write speed, a key attribute for nonvolatile memories is their reliability to keep the data stored unaltered for a very long time. The physical mechanisms that are responsible for a premature data loss and for a poor device

functionality are deeply discussed in Chap. 5. As mentioned in the historical overview, the optimization of the chalcogenide alloy composition has been the key ingredient for the commercial success of rewritable optical storage and for boosting the renewed interest in solid-state device applications. This has been the first step for a continuous improvement of the device performance based on the development of better and better chalcogenide alloys that are suited for different applications. The scope of Chaps. 6 and 7 is to provide a deep insight in material engineering for optimizing the PCM device performance. Chapter 8 is dedicated to the PCM scaling capabilities. Starting from the fundamental physical limitations for the phase-change mechanism, the ultimate limits for the PCM cell functionality are explored and discussed. To complete our journey in PCM technology, the last three chapters of the book deliver to the reader an unprecedented overview of the PCM cell design strategies, the array architectures, and the specific management techniques adopted for mitigating issues and for exploiting the unique opportunities offered by PCM, with a final outlook in the future of phase-change memory technology and their applications.

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