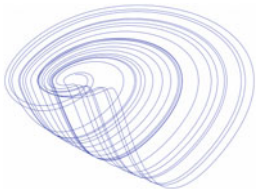
Chapter 5
Chaos



Simulated chaotic attractor from the Muthuswamy-Chua system [19, 22]

Abstract So far we have studied the fundamentals of (nonlinear) circuit theory. We have encountered a variety of multi-terminal elements and circuit analysis techniques. In this final chapter, we will discuss the fascinating mathematical concept of chaos. Notice we use the word mathematical: chaos has been largely studied by mathematicians and scientists. Yet we conclude this book on circuit theory with an advanced mathematical topic because chaos will prove invaluable in **integrating** a majority of the concepts discussed in this book. Chaos is also fundamentally restricted to nonlinear circuits, linear networks do not exhibit chaos. So it is appropriate to conclude this book with a chapter on an exclusive property of nonlinear circuits. For those mathematically familiar with chaos, this chapter takes an "experimentalist" approach when discussing a variety of chaotic circuits.

5.1 An Introduction to Chaos

Chaotic circuits provide excellent examples for utilizing nonlinear elements in **topologically simple circuits**,[1] to study an interesting phenomenon.

Since a thorough treatment of chaos requires a book on its own, in this chapter we will instead mainly focus on a fundamental idea discussed throughout the book:

[1] That is, most of the normal form equations can be derived by inspection.

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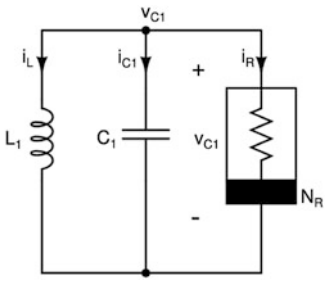


Fig. 5.1 Circuit model of the Van der Pol oscillator

the concept of device modeling. Hence a recurring theme throughout this chapter would be to first discuss a circuit that has been **systematically designed to exhibit chaotic behavior**, and then discuss a circuit that **exhibits chaos because of physical nonlinearities**. We will also focus on the PWL approximation technique, because as we learned throughout the book, we can synthesize any PWL characteristic using opamps, etc. We will design chaotic circuits using nonlinear resistors, capacitors, and inductors. We will also discuss memristor and transistor based chaotic circuits.

We will be performing simulations of the (chaotic) circuits in QUCS and normal form equations in SageMath. We will show implementation results only for the Muthuswamy-Chua chaotic circuit,[2] in order to encourage the reader to investigate the physical implementation of other chaotic circuits, and hence "learn by experimenting." Also, many end-of-chapter exercises are essentially capstone design problems. In other words the ideas discussed in this chapter should lead to interesting research problems for the motivated reader, perhaps even resulting in "good" publications.

We will start by revisiting the Van der Pol oscillator from Sect. 4.6.3. Reconsider the schematic of the Van der Pol oscillator in Fig. 5.1. Note that we are using the dual [3] of the series $LC\mathscr{N}_R$ circuit from Sect. 4.6.3. We now have a voltage-controlled $\mathscr{N}_R$:

$$i_R(v_{C1}) = a v_{C1} + b v_{C1}^3 \tag{5.1}$$

One could implement the cubic nonlinearity in Eq. (5.1) using the twin-tunnel-diode circuit in Fig. 4.53 or by using analog multipliers as shown in Fig. 5.2 From Fig. 5.2 (see Exercise 5.1), we get:

$$i_R(v_{C1}) = \left[-v_{C1} + \left(1 + \frac{R_5}{R_4}\right) \frac{(v_{C1})^3}{100} \right] \frac{1}{R_3} \tag{5.2}$$

However, as stated earlier, we will use a PWL approximation for the cubic nonlinearity. Consider the QUCS schematic in Fig. 5.3. U1 and U2 are QUCS

[2] We picked this circuit to implement because it requires a memristor emulator that has the most number of components of all the chaotic circuits discussed in this chapter.

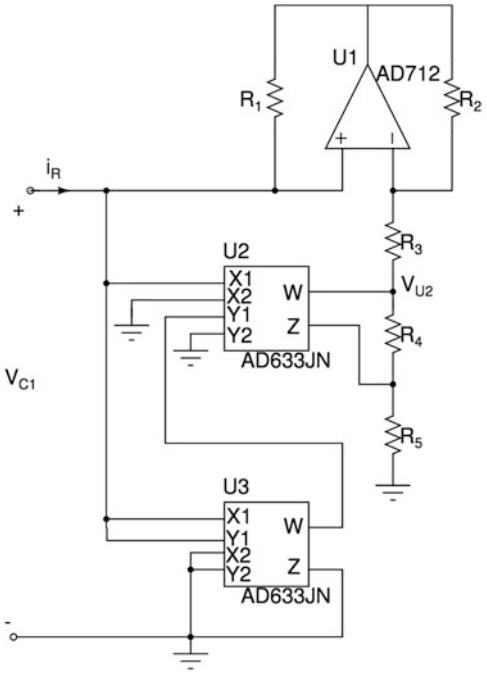


Fig. 5.2 A circuit implementation of $\mathcal{N}_R$ from Fig. 5.1. All power supplies are ± 15 V. Opamp U1 acts as a current inverter when $R_1 = R_2$, U2 and U3 are analog multipliers

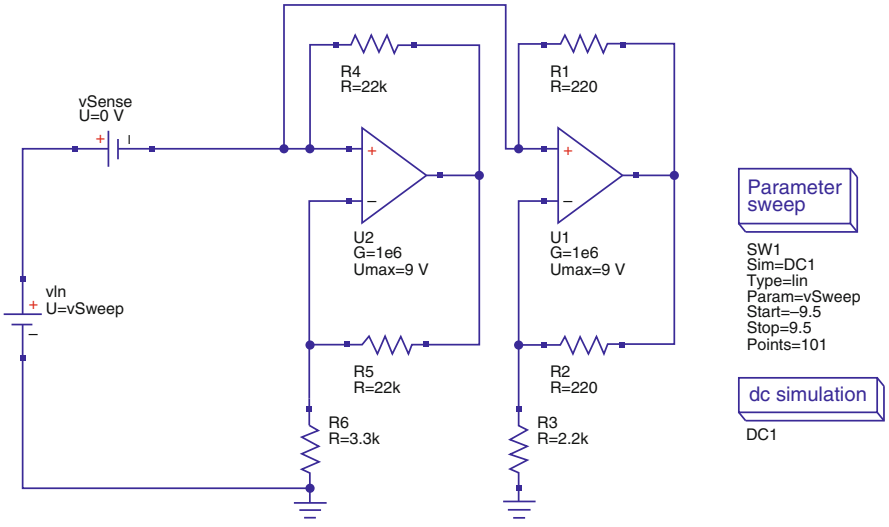


Fig. 5.3 PWL approximation of the cubic nonlinearity. This circuit is called the "Chua diode" [6]

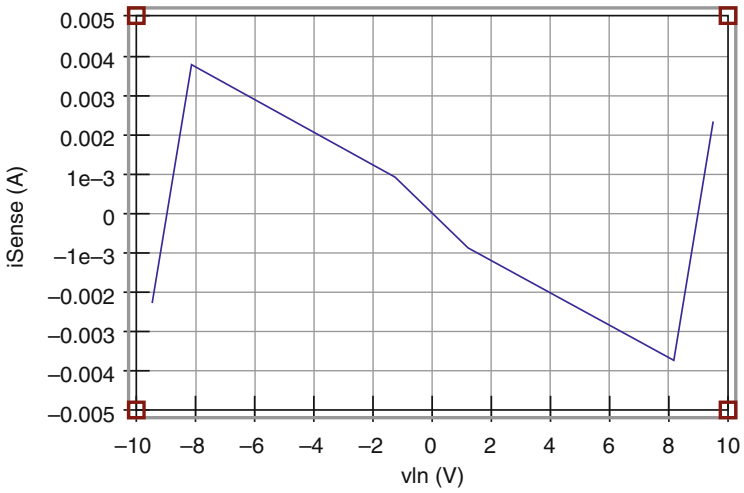


Fig. 5.4 Chua diode DP characteristic. iSense is the current flowing (according to the passive sign convention) through the vSense voltage source in Fig. 5.3

nonlinear model[3] of opamps. We have specified an open-loop gain of $1e6$ and $E = \pm 9\,\text{V}$. We will perform a parameter sweep simulation and plot the DP characteristic. The result is shown in Fig. 5.4. Notice that opamp circuit is a parallel combination of two nonlinear resistors. Each opamp is the voltage-controlled dual of the opamp negative impedance converter from Fig. 2.41. Because of the parallel combination of the resistors, we have two additional breakpoints[4] in the negative resistance region.

Next, we will simply add a resistor and capacitor (to make the system three dimensional,[5] in other words, the order of complexity is now three) as shown in Fig. 5.5, to obtain **Chua's circuit** [6]. The purpose of adding just two components will be clear from simulating Chua's circuit. The complete QUCS schematic for simulation is shown in Fig. 5.6. Simulating the circuit in Fig. 5.6, we get the results in Fig. 5.7.

[3]These can be found under **Nonlinear Components** in the components tab of QUCS. Note that simulating chaotic circuits with a physical opamp (like μA741 models) from the Opamp QUCS Library may not cause the simulation to converge for some circuits.

[4]The reason for breakpoints is to obtain chaos in a three-dimensional extension of the Van der Pol oscillator. The justification is beyond the scope of this book, for details refer to [5].

[5]The minimal dimension of a continuous time chaotic system is usually said to be three because of the Poincaré-Bendixson theorem. But there are unusual systems of lower order that violate this theorem and exhibit chaos, see [27]. Moreover, even one-dimensional discrete-time systems (maps) can exhibit chaotic behavior. Such maps will not be discussed in this book, although they appear in very simple electric circuits, see [26].

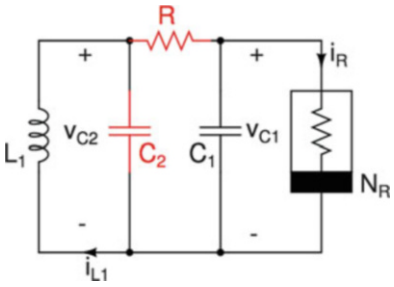


Fig. 5.5 Circuit model for Chua's circuit. The only elements added to the Van der Pol oscillator in Fig. 5.1 are highlighted in red

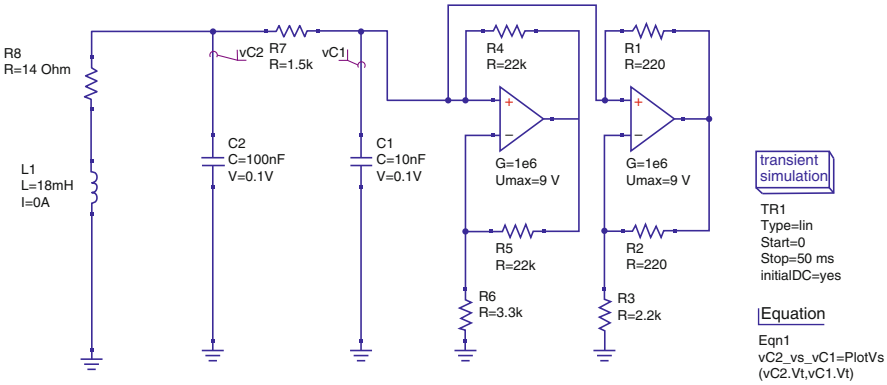


Fig. 5.6 Chua's circuit in QUCS setup for transient analysis

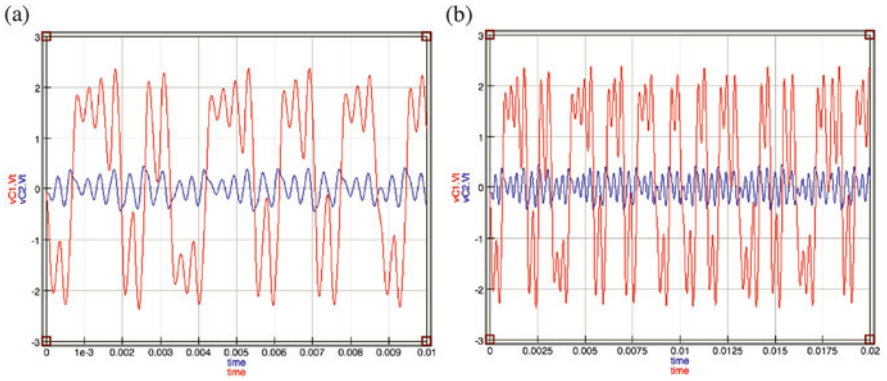


Fig. 5.7 Time domain plots of the voltages across the two capacitors. (**a**) $t = 0$ to $t = 10$ ms. (**b**) $t = 0$ to $t = 20$ ms

An important point is the issue of convergence in circuit simulation of nonlinear (chaotic) circuits. Although this topic is beyond the scope of this text (see [23]), one needs to pay attention to the log messages from the simulator to investigate the source of the issue, and if the convergence error can be safely ignored. If the simulation does not converge at all or seems to converge to incorrect results, the warnings should be closely studied.

In this case, the log messages show:

Listing 5.1 QUCS log from simulating Chua's circuit

```
Output:
-------

Starting new simulation on Thu 11. Jan 2018 at 11:33:19:169

creating netlist... done.
Starting /usr/local/bin/qucsator

project location:
modules to load: 0
factorycreate.size() is 0
factorycreate has registered:
parsing netlist...
checking netlist...
checker notice, variable `vC1.Vt' in equation `vC2_vs_vC1'
    not yet defined
checker notice, variable `vC2.Vt' in equation `vC2_vs_vC1'
    not yet defined
netlist content
      2 C instances
      1 L instances
      8 R instances
      2 OpAmp instances
      1 TR instances
creating netlist...
checker notice, variable `vC1.Vt' in equation `vC2_vs_vC1'
    not yet defined
checker notice, variable `vC2.Vt' in equation `vC2_vs_vC1'
    not yet defined
NOTIFY: TR1: average time-step 2.16797e-06, 4326 rejections
NOTIFY: TR1: average NR-iterations 3.10133, 947 non-
    convergences

Simulation ended on Thu 11. Jan 2018 at 11:33:20:959
Ready.
```

We can see that there are non-convergence warnings, in this case, they can be safely ignored.

Comparing Fig. 5.7a, b, we may be tempted to conclude the transient response is periodic. But closely examining the two time domain waveforms, we can see that

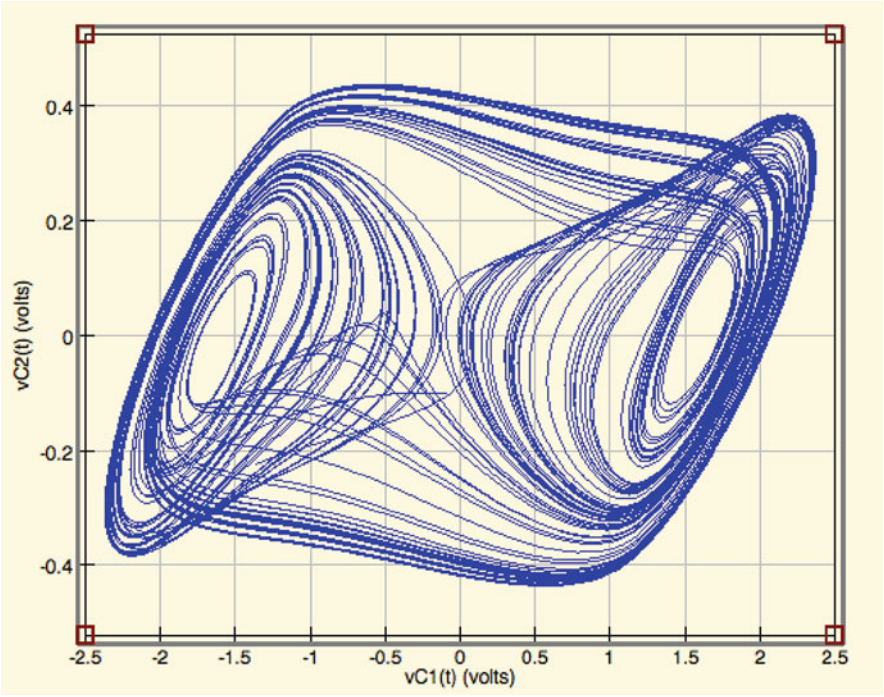


Fig. 5.8 A phase portrait (plot) of $(v_{C1}(t), v_{C2}(t))$ from Fig. 5.7, plotted from $t = 0$ to $t = 50$ ms

may not be true. For instance, they clearly show the number of "oscillating maxima and minima" in each ms interval is different.

A more insightful picture is the phase portrait (plot) discussed in Sect. 4.6.3. The $v_{C1} - v_{C2}$ phase plot is shown Fig. 5.8. We now see that there is a "structure," called a **chaotic attractor**, in phase space. It turns out the chaotic attractor **is the steady-state** response for this circuit.

The structure is so named because it tends to "attract" points in a "basin of attraction" into the attractor (see Exercise 5.2). The term "chaotic" or "chaos" was coined by James Yorke and T.Y. Li [18]. Nevertheless, there is no agreed upon definition of chaos, although researchers generally concur that a chaotic system should satisfy the following properties:

1. Boundedness[6]
2. Aperiodicity
3. Sensitive dependence on initial conditions

[6]We add this property because without it, linear one-dimensional unstable systems could be considered "chaotic" since they satisfy properties 2 and 3.

We will not discuss property 1 in this chapter. Property 2 we have already encountered in Fig. 5.7. Before we investigate property 3, a mindful reader should have noticed that we seemingly have trajectories that are "crossing" each other in Fig. 5.8, whereas in Sect. 4.6.3 we commented that this is not possible because our system is deterministic. The reason why the trajectories seem to cross is because we are looking at a projection on the 2D plane! To further investigate the third seminal property of chaos and the actual structure of the chaotic attractor, it would be helpful to invoke the idea of dimensionless scaling from Sect. 4.6.3. First, we can easily write down the normal form equations for Chua's circuit in Fig. 5.5 (assume parasitic series resistance R_8 of L is 0, see Exercise 5.3):

$$\begin{aligned}\frac{dv_{C1}}{dt} &= \frac{1}{C_1}\left[\frac{v_{C2}-v_{C1}}{R} - g(v_{C1})\right] \\ \frac{dv_{C2}}{dt} &= \frac{1}{C_2}\left[\frac{v_{C1}-v_{C2}}{R} + i_L\right] \\ \frac{di_L}{dt} &= \frac{-v_{C2}}{L}\end{aligned} \tag{5.3}$$

The general nonlinear characteristic $g(v_R)$ of the Chua diode, shown in Fig. 5.9, is given by:

$$g(v_R) = G_b v_R + \frac{1}{2}(G_a - G_b)(|v_R + B_p| - |v_R - B_p|) \tag{5.4}$$

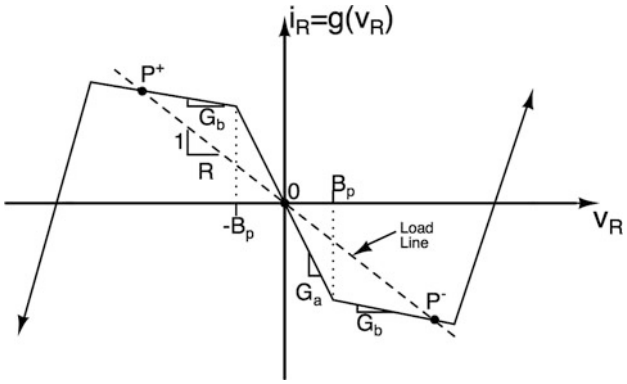


Fig. 5.9 The five segment PWL characteristic from Fig. 5.4, with $v_{C1} = v_R$. Note that $\mathcal{N}_R$ is not passive since we have segments in the second and fourth quadrant, which correspond to the active regions of $\mathcal{N}_R$. The linear resistor R from Fig. 5.5 has been plotted as a load line at steady state. For particular values of R, notice we get three equilibrium points, $P^+, 0, P^-$. This justifies our choice of connecting two voltage-controlled nonlinear resistors in parallel in Fig. 5.3. Note that $\mathcal{N}_R$ eventually becomes strictly passive. Those segments are due to opamp saturation and should not be included when deriving Eq. (5.4)

We will now scale the equations from Chua's circuit into dimensionless, as shown in Example 5.1.1.

Example 5.1.1 Derive the dimensionless form for Eq. (5.3).

Solution Following the procedure in Sect. 4.6.3, let $\tau \triangleq \frac{t}{RC_2}$. Replacing t in Eq. (5.3), we get:

$$\begin{aligned}\frac{dv_{C1}}{d\tau} &= \frac{C_2}{C_1}\left[(v_{C2} - v_{C1}) - Rg(v_{C1})\right] \\ \frac{dv_{C2}}{d\tau} &= \left[(v_{C1} - v_{C2}) + Ri_L\right] \\ \frac{di_L}{d\tau} &= RC_2\left(\frac{-v_{C2}}{i_L}\right)\end{aligned} \tag{5.5}$$

We will take the dimensionless time form in Eq. (5.5) and make the state variables dimensionless as well. Hence we will finally get a dimensionless state equation. To do this, consider the first equation, replacing $g(v_{C1})$ from Eq. (5.4):

$$\frac{dv_{C1}}{d\tau} = \frac{C_2}{C_1}\left[(v_{C2} - v_{C1}) - \{RG_b v_{C1} + \frac{R}{2}(G_a - G_b)(|v_{C1} + B_p| - |v_{C1} - B_p|)\}\right] \tag{5.6}$$

Factoring out B_p ($B_p > 0$), we get:

$$\frac{dv_{C1}/B_p}{d\tau} = \frac{C_2}{C_1}\left[\left(\frac{v_{C2}}{B_p} - \frac{v_{C1}}{B_p}\right) - Rg\left(\frac{v_{C1}}{B_p}\right)\right] \tag{5.7}$$

Let: $x \triangleq \frac{v_{C1}}{B_p}$, $y \triangleq \frac{v_{C2}}{B_p}$, $a \triangleq G_a R$, $b \triangleq G_b R$, $\alpha \triangleq \frac{C_2}{C_1}$. Equation (5.7) simplifies to:

$$\frac{dx}{d\tau} = \alpha(y - x - f(x)) \tag{5.8}$$

where $f(x) = bx + \frac{1}{2}(a - b)(|x + 1| - |x - 1|)$.

(continued)

Example 5.1.1 (continued)
Notice all the parameters defined above are dimensionless. Multiplying and dividing $\frac{dv_{C2}}{d\tau}$ in Eq. (5.5) by B_p:

$$\frac{dv_{C2}/B_p}{d\tau} = \left[\left(\frac{v_{C1}}{B_p} - \frac{v_{C2}}{B_p}\right) + \frac{Ri_L}{B_p}\right] \tag{5.9}$$

Let: $z \triangleq \frac{i_L R}{B_p}$. We thus have:

$$\frac{dy}{d\tau} = x - y + z \tag{5.10}$$

Finally, if we define $\beta \triangleq \frac{R^2 C_2}{L}$, $\frac{di_L}{d\tau}$ in Eq. (5.5) becomes:

$$\frac{dz}{d\tau} = -\beta y \tag{5.11}$$

Hence, the dimensionless form of Chua's circuit equations are:

$$\begin{aligned}\frac{dx}{d\tau} &= \alpha(y - x - f(x))\\ \frac{dy}{d\tau} &= x - y + z\\ \frac{dz}{d\tau} &= -\beta y\end{aligned} \tag{5.12}$$

Some observations from the dimensionless form:

1. Example 5.1.1 illustrates a semi-systematic procedure for obtaining dimensionless normal form: we always start by scaling the time variable. The justification is that there are three choices for scaling to dimensionless time: $\tau = \frac{t}{R_n C_n}$, $\tau = \frac{t}{L_n/R_n}$ or $\tau = \frac{t}{\sqrt{L_n C_n}}$. After scaling time, the actual scaling of the state variables, parameters, and nonlinearities depend on the particular system. Hence, the procedure is "semi-systematic."
2. Equation (5.12) has four parameters that can be tuned: α, β, a, b. In contrast, Eq. (5.3) has seven parameters: $R, C_1, C_2, L, G_a, G_b, B_p$. Hence it is always convenient to scale circuit equations to dimensionless form.

SageMath simulation results for Eq. (5.12) with two different initial conditions ([0.1, 0, 0.1], [0.1, 0, 0.01]) are shown in Fig. 5.10. SageMath code is shown in Listing 5.2.

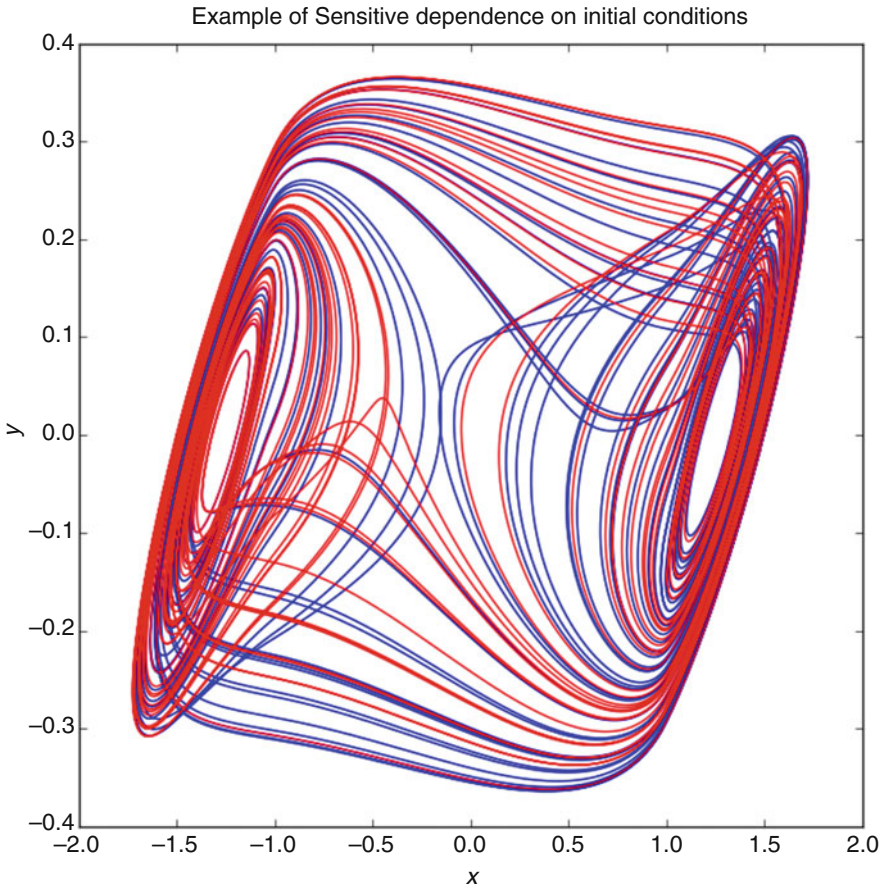


Fig. 5.10 The result of simulating with two different initial conditions are shown in different colors. Notice that the trajectories do not superimpose

Listing 5.2 SageMath code

```
# Simulate the autonomous Chua oscillator (dimensionless form
    )
from scipy.integrate import odeint
from matplotlib import pyplot as plt
plt.rcParams['figure.figsize'] = (8.0,8.0)
plt.rc('text', usetex=True)
plt.rc('font', family='serif')
from mpl_toolkits.mplot3d import Axes3D
# Circuit parameters
C1=10e-9
C2=100e-9
L=18e-3
R=1514
```

```
Bp=1
Ga=(0.864e-3+0.864e-3)/(-1.14-1.14)
Gb=(2.94e-3-0.864e-3)/(-8.36+1.14)
#dimensionless parameters
a=Ga*R
b=Gb*R
alpha=C2/C1
beta=((R**2)*C2)/L
# system
def f(x,a,b):
    return b*x+0.5*(a-b)*(abs(x+1)-abs(x-1))
def chuaDimensionless(previousState,t):
    # Let previousState = [x(t-dt),y(t-dt),z(t-dt)].
    # Hence, we are going to return the normal form equations
        to be integrated
    # by odeint:
    # x(t) = f_1(x(t-dt),y(t-dt),z(t-dt))
    # y(t) = f_2(x(t-dt),y(t-dt),z(t-dt))
    # z(t) = f_3(x(t-dt),y(t-dt),z(t-dt))
    x,y,z=previousState
    return (alpha*(y-x-f(x,a,b)),x-y+z,-beta*y)
# setup and run simulation
times=srange(0,500,0.01)
ics=[0.1,0,0.1]
chuaDimensionlessSolIC1=odeint(chuaDimensionless,ics,times,
    rtol=1e-14,atol=1e-13)
chuaDimensionlessSolIC2=odeint(chuaDimensionless,[0.1,0,0.01
    ],times,rtol=1e-14,atol=1e-13)
# make sure we obtain STEADY STATE values of (x,y,z)
x1=chuaDimensionlessSolIC1[30000:45000,0]
y1=chuaDimensionlessSolIC1[30000:45000,1]
z1=chuaDimensionlessSolIC1[30000:45000,2]
x2=chuaDimensionlessSolIC2[30000:45000,0]
y2=chuaDimensionlessSolIC2[30000:45000,1]
z2=chuaDimensionlessSolIC2[30000:45000,2]
# 2D plot
plt.plot(x1,y1,'b',x2,y2,'r')
plt.xlabel('$x$',fontsize=16)
plt.ylabel('$y$',fontsize=16)
plt.title('Example of sensitive dependence on initial
    conditions')
plt.show()
# 3D plot
fig = plt.figure()
ax = fig.add_subplot(111, projection='3d')
ax.view_init(20,70)
plt.xlabel('$x$',fontsize=16)
plt.ylabel('$y$',fontsize=16)
plt.ylabel('$z$',fontsize=16)
plt.plot(x,y,z)
plt.show()
```

Figure 5.11 shows a 3D plot. Notice how the chaotic attractor trajectories clearly will not self-intersect in three dimensions, consistent with our explanation in

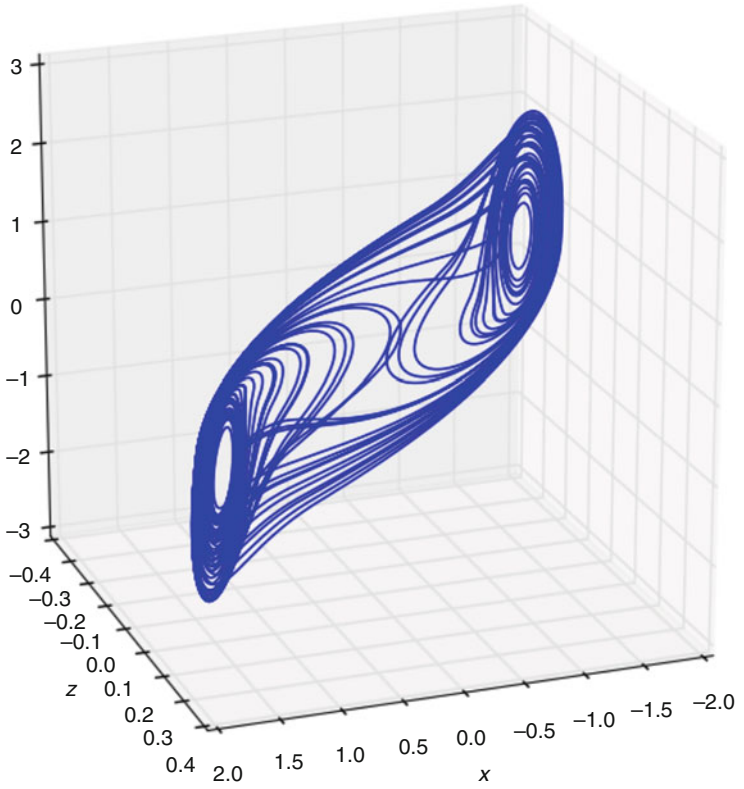


Fig. 5.11 Chaotic attractor in 3D

Sect. 4.6.3. In fact, the chaotic attractor has a **fractional Kaplan-Yorke dimension** between 2 and 3. For details on computing measures for chaotic systems such as the (Kaplan-Yorke) dimension, Lyapunov exponents, etc., see [27]. Browsing through the simulation code shows a very important point: **we have to be careful before declaring a system to be chaotic from simulation results alone**. It could be the steady state solution is (very) long-term periodic, or we may be looking at a transient response. Although a variety of mathematical techniques exist that can be used to rigorously prove chaos, they are beyond the scope of this book. For a very good overview of the different techniques available, with a circuit theoretic emphasis, see related chapters in [1]. However, we can easily avoid the trap of **misidentifying a transient response as the steady state solution by simply plotting the phase portrait with different time ranges**. In this case, we chose to plot the range [30,000 : 45,000].

Another point to note are the parameters we chose. Since the parasitic series resistance of L was chosen to be zero, we added 14 Ω to R because at **DC, we get a load line using $R = 1514\,\Omega$, consistent with the circuit in Fig. 5.6**.

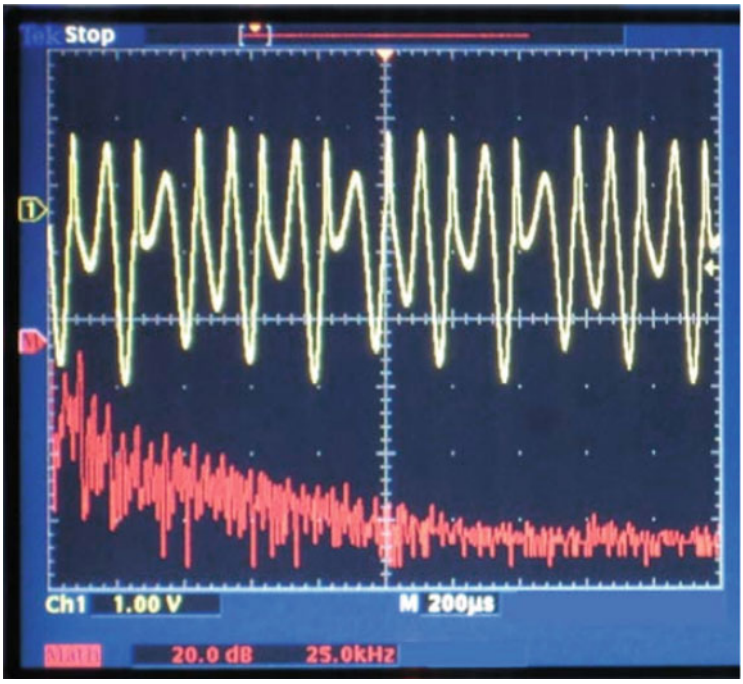


Fig. 5.12 Plot (in red) of the Fourier transform of the voltage across a capacitor from the Muthuswamy-Chua circuit (to be discussed in Sect. 5.4.1). Notice how the signal has content across a wide range of frequencies

A very important property of chaos that is beyond the scope of this book is the frequency content of chaotic signals. It turns out that chaotic signals possess a **wideband** frequency content. An example is shown in Fig. 5.12. As a result chaos can be easily confused with noise. Hence, before the advent of computer simulations, chaos was observed but not identified in a variety of circuits and systems. We will now look at a very brief history of chaos and see circuits where chaos was observed but not identified.

5.2 A History of Chaos in Circuit Theory

In 1922, Armstrong invented the (super)regenerative circuit as a detector with high sensitivity and selectivity as compared to other types of receivers [16]. In the early days of radio engineering, this type of detection was frequently used. Nowadays, regenerative devices are still used as predetection systems when very high frequencies (e.g., microwave communication) are involved. The regenerative detector

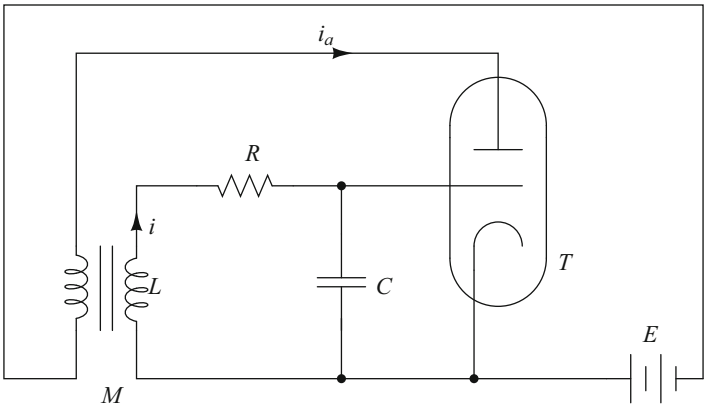


Fig. 5.13 The grid oscillator, T is a three-terminal nonlinear vacuum tube. An incoming signal is modeled as a sinusoidal forcing of the form $A\cos(\omega t)$. For circuit equations and detailed analysis, see [16]

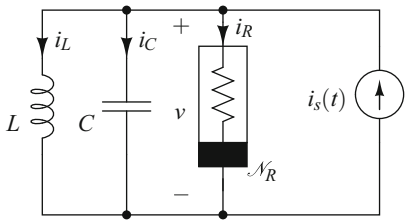


Fig. 5.14 Sinusoidally forced Van der Pol oscillator that displays chaotic behavior, $i_s(t) = A\cos(\omega t)$, see [27]

is favorably used in applications where simplicity and compactness outweigh the need for low noise reception. These circuits use a three terminal vacuum tube, as a receiver as well as in the transmitter, with inductive coupling. Figure 5.13 shows the grid oscillator, a good model for studying chaos in Armstrong's circuit. It turns out that in a simplified model of the circuit above, one can show that the current i behaves chaotically during a small period in time after which the circuit becomes an oscillator. Armstrong was not aware of the circuits' chaotic behavior, but reported "strange irregular startups of the oscillator." It also turns out that during the period in which irregularities appear, the amplification of the circuit is maximal. Hence Armstrong's circuit is an example application of chaos to signal amplification.

Van der Pol in fact also observed similar phenomena, i.e. "irregular noise," when he forced his oscillator with a sinusoidal signal (Fig. 5.14). Unfortunately, he also dismissed chaos as "noise" and did not study the phenomenon further. Note that the

nonautonomous Van der Pol equations for the circuit in Fig. 5.14:

$$\begin{aligned} \frac{di_L}{dt} &= \frac{v}{L} \\ \frac{dv}{dt} &= \frac{-i_L - i_R + A\cos(\omega t)}{C} \end{aligned} \tag{5.13}$$

can be put it into autonomous normal form by a simple change of variables. If $z \triangleq \omega t$, we get:

$$\begin{aligned} \frac{i_L}{dt} &= \frac{v}{L} \\ \frac{dv}{dt} &= \frac{-i_L - i_R + A\cos(z)}{C} \\ \frac{dz}{dt} &= \omega \end{aligned} \tag{5.14}$$

A variety of "near-misses" also occurred with respect to chaos when investigating nonlinear circuits. Ueda studied combinations such as the Duffing[7]-Van der Pol oscillator by means of analog and digital computers as early as 1961 while he was a graduate student but did not publish results [27]. Many investigations into chaotic circuits in the 1970s were focused on the nonautonomous type, where an external (usually sinusoidal) forcing function was used.

In 1983, while on a visit to Dr. Matsumoto's lab in Waseda University, Dr. Leon O. Chua witnessed his colleague unable to reproduce chaos in a physical circuit implementation of the Lorenz chaotic system. Chua realized that the issue at hand was the use of analog multipliers, which were not reliable in the early 1980s [5]. As a result of the failure, Dr. Chua **systematically designed** an **autonomous** circuit that could potentially reproduce chaotic behavior physically. The core concept was to make use of the $\mathscr{N}_R$ shown in Fig. 5.9 such that at equilibrium, the circuit possessed three **unstable** equilibrium points, as Example 5.2.1 shows.

Example 5.2.1 Using the dimensionless formulation of Chua's circuit from Eq. (5.12) in Example 5.1.1, determine the equilibrium points for the parameter values from Fig. 5.6 and classify them as unstable or stable.

Solution The equilibrium points are simply found by setting the derivatives equal to zero and solving the resulting system of nonlinear equations. Thus, if

(continued)

[7] We will study the Duffing oscillator in Sect. 5.5.

Example 5.2.1 (continued)
the equilibrium points are (x^*, y^*, z^*), we have:

$$\begin{aligned} \alpha(y^* - x^* - f(x^*)) &= 0 \\ x^* - y^* + z^* &= 0 \\ \beta y^* &= 0 \end{aligned} \tag{5.15}$$

Simplifying:

$$\begin{aligned} x^* &= -f(x^*) \\ x^* &= -z^* \\ y^* &= 0 \end{aligned} \tag{5.16}$$

Solving the above equations, we get the equilibrium points $(0, 0, 0)$, $(+1.261, 0, -1.261)$, $(-1.261, 0, 1.261)$. When $|x(t)| < 1$, the nonlinear function is: $f(x) = ax$. Thus the Jacobian matrix J_0 is:

$$\mathbf{J}_0 = \begin{bmatrix} -\alpha - \alpha \cdot a & \alpha & 0 \\ 1 & -1 & 1 \\ 0 & -\beta & 0 \end{bmatrix} \tag{5.17}$$

When $|x(t)| > 1$, the nonlinear function is: $f(x) = bx \pm (a - b)$. the Jacobian matrices $J_{\pm 1}$ are both:

$$\mathbf{J}_{\pm 1} = \begin{bmatrix} -\alpha - \alpha \cdot b & \alpha & 0 \\ 1 & -1 & 1 \\ 0 & -\beta & 0 \end{bmatrix} \tag{5.18}$$

Notice $\mathbf{J}_0$ and $\mathbf{J}_{\pm 1}$ do not depend on the values of the equilibrium points, but only the parameters. For $\mathbf{J}_0$, the eigenvalues are $\lambda_1 \approx 2.659$, $\lambda_{2,3} \approx -1.092 \pm 2.423j$. For $\mathbf{J}_{\pm 1}$, the eigenvalues are $\lambda_1 \approx -6.937$, $\lambda_{2,3} \approx 0.143 \pm 3.217j$.

Notice how the Jacobian shows all three equilibrium points are unstable. But, since $\mathcal{N}_R$ in Fig. 5.9 is eventually passive, the circuit variables cannot arbitrarily increase. Hence, the circuit eventually settles into a strange attractor.[8]

[8]There is another very important criterion for a chaotic attractor in Chua's circuit—the homoclinic orbit. For details, see [1].

Although Chua's circuit has more components than required for a chaotic electronic circuit, its significance is the fact that since it was systematically designed, a rigorous proof of chaos was quickly possible within only 2 years after its invention [1]. Moreover, systematically understanding how chaos is produced in Chua's circuit will help in approaching the study of chaos in other "simpler" electronic circuits. This is because of the fact that Chua used PWL analysis in designing the Chua diode. So, when possible, we encourage the reader to use a PWL approximation of a nonlinear function in order to not only implement the function physically, but also to aid in the mathematical analysis of the underlying differential equations.

For instance, in the next section, we will list two circuits which have very simple topologies, but they produce "rich" chaotic behavior. Also, the underlying nonlinear device model that gives rise to chaotic behavior is still a subject of active research.

5.3 Chaos from Physical Nonlinearities: *pn*-Junctions and PWL Inductors

5.3.1 RLD Chaotic Circuit

Consider the QUCS schematic of the RLD circuit in Fig. 5.15. A chaotic time-domain waveform is shown in Fig. 5.16. Investigations into the physical source of chaos in the diode for the circuit from Fig. 5.15 focus on the nonlinear junction capacitance. In fact, [20] has an elegant PWL model for the nonlinear junction capacitance. Hence a circuit that uses a nonlinear capacitor to produce chaotic

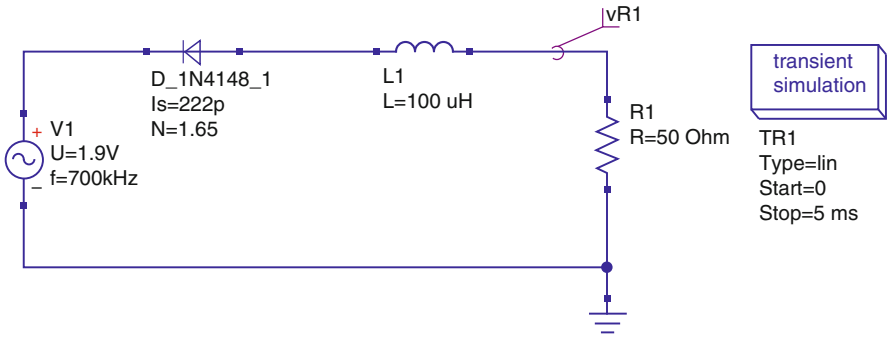


Fig. 5.15 Chaotic circuit from a forced diode resonator

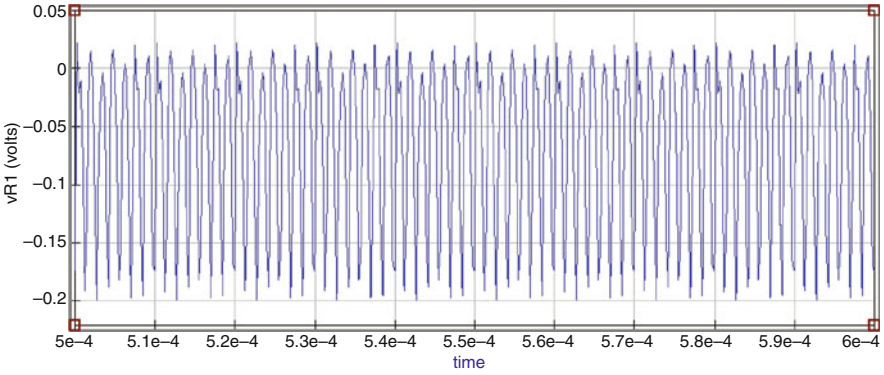


Fig. 5.16 The voltage across the 50 Ω resistor from Fig. 5.16 as a function of time

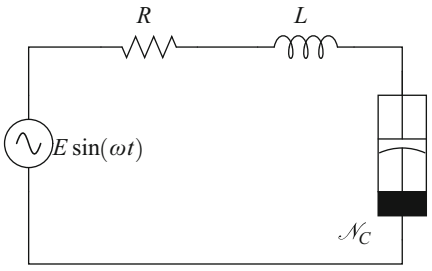


Fig. 5.17 PWL capacitor used to model the diode in the RLD chaotic circuit

behavior is shown in Fig. 5.17. The circuit equations for the PWL model are:

$$\begin{aligned} \frac{dq}{dt} &= i \\ \frac{di}{dt} &= -\frac{1}{L}\left(iR + f(q) - E\sin(\omega t)\right) \end{aligned} \tag{5.19}$$

where:

$$f(q) = a|q| + bq + E_0 \tag{5.20}$$

$a = \frac{C_2 - C_1}{2C_1C_2}, b = \frac{C_1 + C_2}{2C_1C_2}$. Chaos has been observed by fixing $R = 60\,\Omega, L = 100\,\mu\text{H}, C_1 = 0.1\,\mu\text{F}, C_2 = 400\,\text{pF}, \omega/2\pi = 700\,\text{kHz}, E_0 = 0.1\,\text{V}$ and varying E from 0 to 2.0 V. We leave the exploration to the reader.

But, there are a variety of nonlinearities present in the junction diode, besides capacitance. For example, the conductivity modulation effect present in diodes is due to memristance [7]. Hence an interesting avenue for further research would be

to examine if the memristor's nonlinearity plays any role in chaos in the RLD circuit (under appropriate range of parameters).

5.3.2 PWL Inductor Circuit

If we make only the inductor nonlinear in an RLC circuit by introducing hysteresis (example: iron core inductors), chaos can occur [8]. The PWL schematic for the circuit is shown in Fig. 5.18. $\mathscr{N}_L$ is defined by the following PWL function:

$$i(\phi) = \begin{cases} \frac{\phi-\phi_1}{L_1} & \text{for } \phi > \phi_0 \\ \frac{\phi}{L_0} & \text{for } |\phi| < \phi_0 \\ \frac{\phi+\phi_1}{L_1} & \text{for } \phi < -\phi_0 \end{cases} \tag{5.21}$$

where

$$\phi_1 = \phi_0 \left(1 - \frac{L_1}{L_0}\right) \tag{5.22}$$

Practically, $0 < L_1 < L_0$. The circuit equations are:

$$\begin{aligned} \frac{d\phi}{dt} &= \frac{R_1 R_2}{R_1 + R_2} i(\phi) - \frac{R_2}{R_1 + R_2}(v - E\cos(\omega t)) \\ \frac{dv}{dt} &= \frac{1}{C}\left[\frac{R_2}{R_1 + R_2} i(\phi) - \frac{1}{R_1 + R_2}(v - E\cos(\omega t))\right] \end{aligned} \tag{5.23}$$

Circuit parameters used for simulation are: $\omega/2\pi = 50\,\text{Hz}$, $R_1 = 50\,\Omega$, $R_2 = 10\,k\Omega$, $C = 1.69\,\mu\text{F}$, $L_0 = 33.33\,\text{H}$, $L_1 = 1.28\,\text{H}$, $\phi_0 = 0.92\,\text{Vs}$. Varying E should produce chaotic behavior, we also leave this exploration to the reader. What is interesting however is the physical mechanism of chaos in this circuit is still unknown.

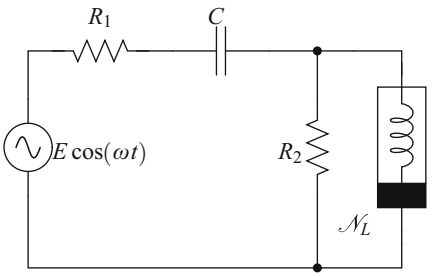


Fig. 5.18 A nonlinear resonant circuit

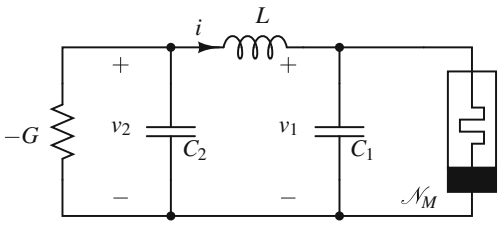


Fig. 5.19 Canonical Chua's oscillator with a flux-controlled memristor

5.4 Memristor Based Chaotic Circuits

We will now discuss chaotic circuits using the fourth fundamental circuit element, the memristor. Consider the canonical Chua's circuit[9] in Fig. 5.19, with $\mathscr{N}_R$ replaced by $\mathscr{N}_M$ [13]. However, one has to use caution when deriving the circuit equations. This is because simply writing the equations in terms of current and voltage would give:

$$\begin{aligned}
\frac{di}{dt} &= \frac{1}{L}(v_2 - v_1) \\
\frac{dv_2}{dt} &= \frac{1}{C_2}(Gv_2 - i) \\
\frac{dv_1}{dt} &= \frac{1}{C_1}(i - W(\phi_1)v_1) \\
\frac{d\phi_1}{dt} &\triangleq v_1
\end{aligned} \tag{5.24}$$

Exercise 5.5 asks you to rewrite the system equations in terms of charge and flux, so the number of ODEs is reduced by one.

A variety of chaotic attractors have been derived for the circuit in Fig. 5.19. What is interesting however is that we **only need one** capacitor, **one** inductor, and **one** memristor to obtain a chaotic circuit, as the next section illustrates.

5.4.1 Muthuswamy-Chua Circuit

Let us play the same "trick" that we used in Chua's circuit, of replacing $\mathscr{N}_R$ with $\mathscr{N}_M$, but in the topologically simpler (series) Van der Pol oscillator. We consider the series implementation in this section because Muthuswamy and Chua **systematically** obtained chaos [22] in the circuit shown in Fig. 5.20, called the Muthuswamy-Chua circuit [19]. Assuming a current-controlled $\mathscr{N}_M$ with only one

[9] This circuit is slightly different from the circuit we discussed in Sect. 5.1.

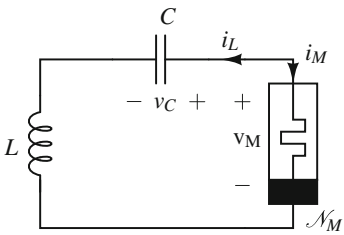


Fig. 5.20 The Muthuswamy-Chua circuit [22]

internal state z,[10] the system equations for the circuit can be trivially derived:

$$\begin{aligned}\frac{dv_C}{dt} &= \frac{i_L}{C}\\ \frac{di_L}{dt} &= -\frac{1}{L}\left(v_C + R(z, i_L)i_L\right)\\ \frac{dz}{dt} &\triangleq f(z, i)\end{aligned} \tag{5.25}$$

The significance of the Muthuswamy-Chua circuit is that it is the **simplest known chaotic circuit** that uses only the **fundamental circuit elements**. Also, only the memristor is nonlinear.[11] Consider the following specific system equations derived from Eq. (5.25). We have assumed $x = v_C$, $y = i_L$.

$$\begin{aligned}\frac{dx}{dt} &= \frac{y}{C}\\ \frac{dy}{dt} &= -\frac{1}{L}\left(x + \beta(z^2 - 1)y\right)\\ \frac{dz}{dt} &= -y - \alpha z + yz\end{aligned} \tag{5.26}$$

Inspired by Rössler's intuitive arguments in deriving his namesake chaotic equation, the memristance and state functions in Eq. (5.26) were systematically derived by Dr. Muthuswamy for producing chaotic behavior. Assuming $\beta > 0$, $R(z) = \beta(z^2 - 1)$ is negative for $|z| < 1$. Hence when we "power on" the circuit in Fig. 5.20, since initial memristor state variable will naturally be assumed to be close to zero, we have a

[10] The system of equations is autonomous and the minimum number of state variables to obtain chaos in a continuous time autonomous system is three. Hence we need only one internal state for the memristor to have a three-dimensional autonomous ODE model of the Muthuswamy-Chua circuit.

[11] Of course, we know by definition a linear memristor is simply a resistor.

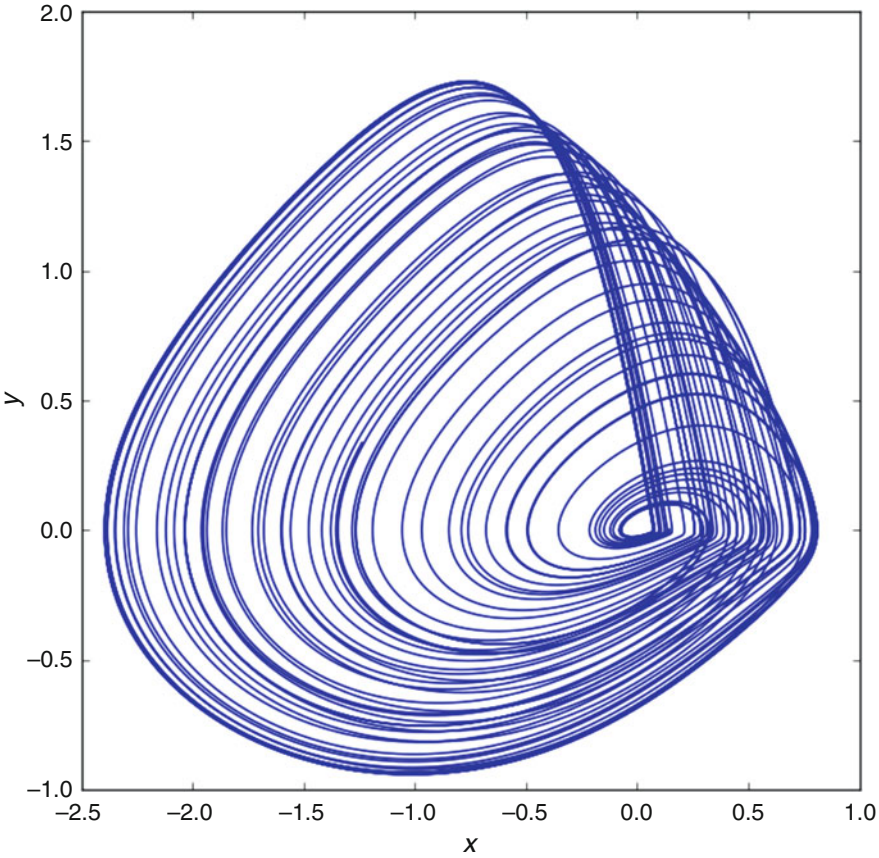


Fig. 5.21 $x - y$ phase plot resulting from simulating Eq. (5.26) with parameters $C = 1, L = 3.3, \beta = 1.7, \alpha = 0.2$. We chose an appropriate interval to avoid transient and plot the "steady-state" chaotic attractor

negative memristance. Hence the circuit is **unstable** and the voltage, current values start increasing. In the RHS of the $\dot{z}$ Eq. (5.26), we can see the product yz also starts increasing. But, if $|z| > 1$, the memristance is positive and hence the circuit becomes **stable**. Furthermore, the $-y - \alpha z$ will also eventually cause trajectories in z to head back to the origin, until the circuit becomes unstable again. This alternating unstable and stable behavior leads to limit cycles (similar to our discussion in Sect. 4.6.3) for some parameter values, and chaos for other (systematically chosen) parameter values. In fact, it has been rigorously proved [12] that the chaotic attractor shown in Fig. 5.21 is topologically the same as the Rössler attractor.

We will now discuss the implementation of the Muthuswamy-Chua circuit in detail since we have to emulate the memristor. Consider the schematic Fig. 5.22.

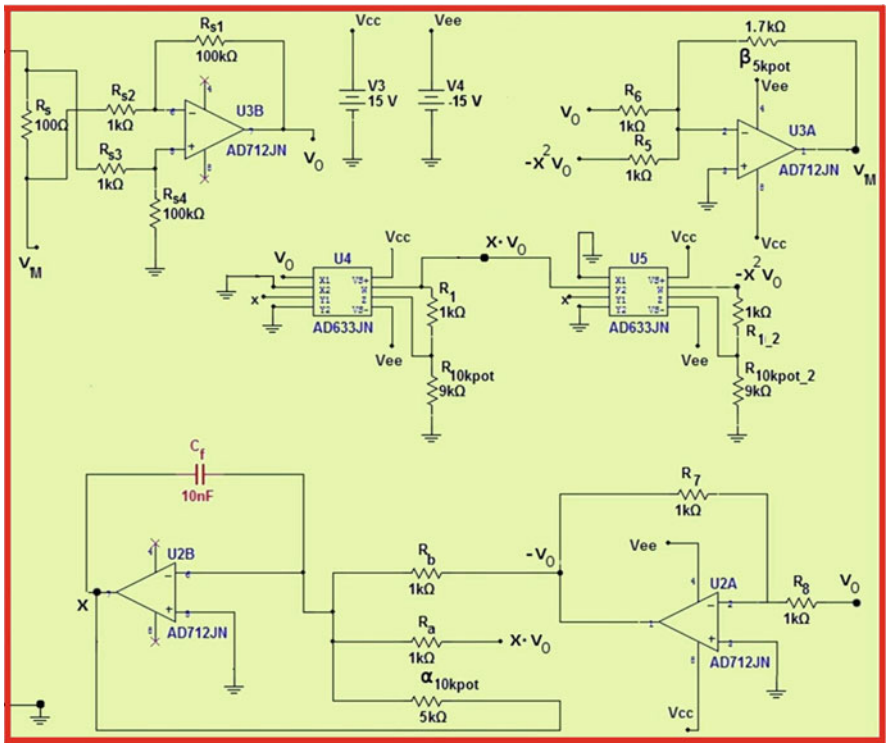


Fig. 5.22 Circuit for emulating $\mathcal{N}_M$ from Fig. 5.20

The first step is to sense the current using a "sense" resistor R_s. This resistor must be "small enough" so it does not affect the dynamics of the circuit. In our case we have $R_s = 100\,\Omega$ connected to the difference amplifier U3B. Hence the output of U3B is:

$$v_0 = \frac{R_{s1}}{R_{s2}} R_s i_M = -R_{\text{scale}} i_L \tag{5.27}$$

Thus we have scaled and mapped the current into a voltage v_0, so that we can easily use components such as analog multipliers, which are voltage based.

The next step is to realize the memristor function $R(x) = \beta(x^2 - 1)$,[12] using opamp U3A, multipliers U4, U5. Using the datasheets of the multipliers and the

[12]We will use x instead of z for the memristor state in the implementation discussion, to be consistent with the original publication [22].

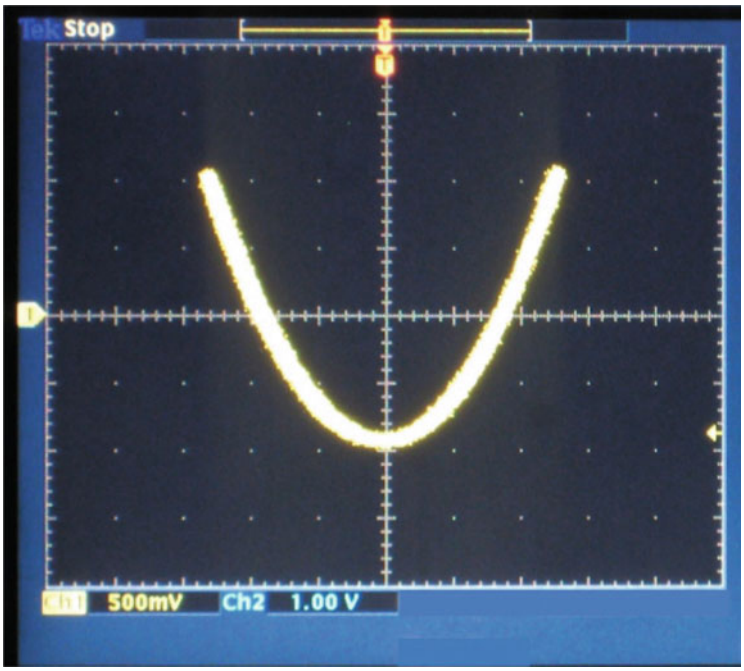


Fig. 5.23 Experimental plot of $R(x) = 1.5(x^2 - 1)$. Horizontal axis scale is 0.5 V/division; vertical axis scale is 1.00 V/division. The experimental curve crosses the horizontal axis at -1 V and approximately 0.9 V

connections shown in the schematic, we can infer that:

$$v_{\mathrm{M}} = -\frac{\beta_{5\mathrm{kpot}}}{R_6} v_0 - \frac{\beta_{5\mathrm{kpot}}}{R_5}(-x^2 v_0) \tag{5.28}$$

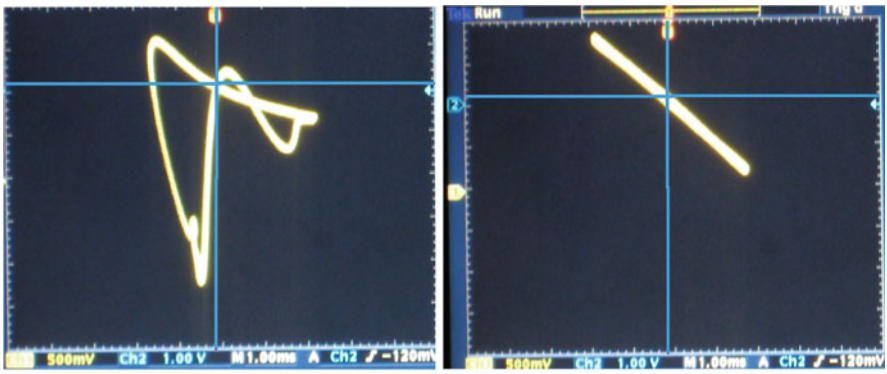
We will choose $R_5 = R_6 = R = 1k$ and $\beta \triangleq \frac{\beta_{5\mathrm{kpot}}}{R}$. Replacing v_0 in Eq. (5.28) from Eq. (5.27) and simplifying, we get:

$$v_{\mathrm{M}} = \beta R_{\mathrm{scale}}(x^2 - 1) i_L \tag{5.29}$$

A plot of $R(x)$ obtained from the circuit is shown in Fig. 5.23. The reader should have noticed that R is not PWL. A good avenue for further research would be to consider PWL versions of R.

The final step is to realize the memristor internal state equation. This is done by means of opamps U2B, U2A. The output x of opamp U2B is given by:

$$\frac{dx}{dt} = \frac{1}{C_f}\left[\frac{v_0}{R_b} - \frac{x}{\alpha_{10\mathrm{kpot}}} - \frac{x v_0}{R_a}\right] \tag{5.30}$$



(a) (b)

Fig. 5.24 Memristor pinched hysteresis loop (Lissajous figures). Axes scales are 0.5 V/division for horizontal axis (i_M), 1.00 V/division for vertical axis (v_M). (**a**) 3 kHz. (**b**) 35 kHz

Substituting for v_0 from Eq. (5.27), we get:

$$\frac{dx}{dt} = \frac{1}{C_f}\left[-\frac{R_{\text{scale}} i_L}{R_b} - \frac{x}{\alpha_{10\text{kpot}}} + \frac{R_{\text{scale}} i_L x}{R_a}\right] \tag{5.31}$$

Let us check memristor pinched-hysteresis $v - i$ characteristics, based on our discussions in Sect. 4.4.2. Results are shown in Fig. 5.24a, b. The DC characteristic has already been verified in Fig. 4.41. Notice that as $\omega \rightarrow \infty$, the hysteresis loop degenerates to that of a linear resistor, as required. Let us now consider the memristor emulator connected to a physical C_n and L_n. Circuit equations are:

$$\begin{aligned}
\frac{dv_C}{dt} &= \frac{i_L}{C_n} \\
\frac{di_L}{dt} &= -\frac{1}{L_n}\left[v_C + \beta R_{\text{scale}}(x^2 - 1) i_L + R_s i_L\right] \\
\frac{dx}{dt} &= \frac{1}{C_f}\left[-\frac{R_{\text{scale}} i_L}{R_b} - \frac{x}{\alpha_{10\text{kpot}}} + \frac{R_{\text{scale}} i_L x}{R_a}\right]
\end{aligned} \tag{5.32}$$

Notice that we have included the effect of the sense resistor R_s in the $\dot{i}_L$ equation above.

We finally need to convert the circuit equations into the system Eq. (5.26). To do this, we will first perform the time scaling as $\tau \stackrel{\triangle}{=} T_s t = 10^5 t$. In this case, we **do not perform a dimensionless scaling** using $\tau = \frac{t}{\sqrt{LC}}$. The reason is that choosing

this time scale would eventually make $L = C$ in Eq. (5.26). We will also scale $y(\tau)$ to hundreds of microamps, for physical implementation. Thus, we have:

$$\begin{aligned} x(\tau) &\triangleq v_C(t) \\ y(\tau) &\triangleq R_{\text{scale}} i_L(t) \\ z(\tau) &\triangleq x(t) \end{aligned} \tag{5.33}$$

To be clear, the **dimension of** x, y, z **are all volts**. Substituting the definitions above into Eq. (5.32) and simplifying using the component values from the emulator we get:

$$\begin{aligned} \frac{dx}{d\tau} &= \frac{y}{C} \\ \frac{dy}{d\tau} &= -\frac{1}{L}\left(x + \beta(z^2 - 1)y + 0.01y\right) \\ \frac{dz}{d\tau} &= -y - \alpha z + yz \end{aligned} \tag{5.34}$$

where:

$$\begin{aligned} C &= R_{\text{scale}} C_n T_s \\ L &= \frac{L_n T_s}{R_{\text{scale}}} \\ \beta &= \frac{\beta_{5\text{kpot}}}{R} \\ \alpha &= \frac{1}{T_s C_f \alpha_{10\text{kpot}}} \end{aligned} \tag{5.35}$$

Choosing $C_n = 1\,\text{nF}$, $L_n = 330\,\text{mH}$ and $\beta_{5\text{kpot}} = 1.7k, \alpha_{10\text{kpot}} = 5k$, we get: $C = 1, L = 3.3, \beta = 1.7, \alpha = 0.2$. The attractor obtained from the physical circuit is shown in Fig. 5.25. Based on our experience with the memristor emulator, a natural follow-up question is: are there chaotic circuits where physical memristor nonlinearities cause chaos? As of the writing of this book (January 2018), no one has **explicitly** found such a circuit. But, there are a variety of candidates. One promising candidate is Theodorchik's oscillator [2] shown in Fig. 5.26. Anischenko et. al. [2] do not explicitly state the $R(T)$ modeled by a thermistor, is a memristor. They rather assume the memristance to be a linear function of temperature. They modify the

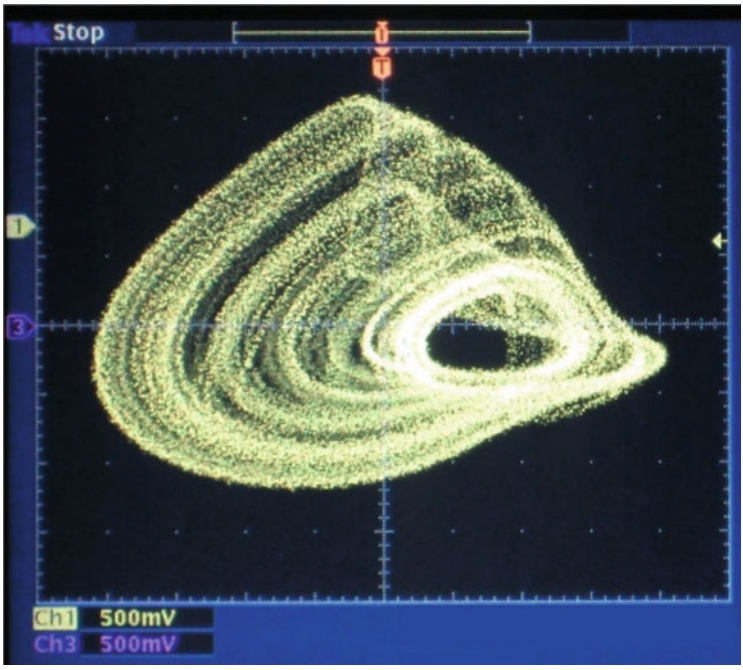


Fig. 5.25 Experimental chaotic attractor, axes scales are 0.5 V/division. We used a current probe to measure the current i_L through the inductor. In the experimental plot, $(0, 0)$ has been shifted to the right for clarity on the oscilloscope. Compare to Fig. 5.21

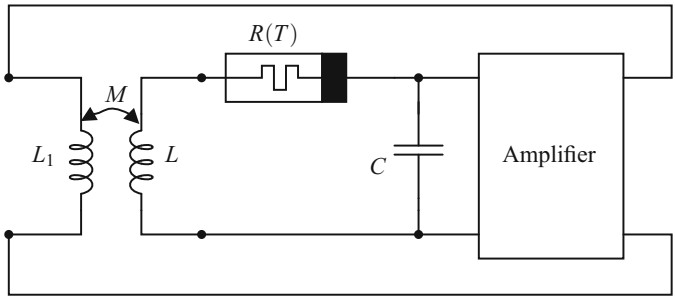


Fig. 5.26 Theodorchik's oscillator with "inertial nonlinearity"

oscillator in Fig. 5.26 by adding more amplifier stages, assume the amplifier to be nonlinear and obtain chaos. It would be interesting for the reader to investigate this problem further (see Exercise 5.7).

5.5 Implementing the Duffing Oscillator Using a Higher-Order Element

Having obtained chaotic circuits by using all four fundamental circuit elements, we will next propose a chaotic circuit using a higher-order circuit element. We alluded to this in earlier chapters, recall the Duffing oscillator equation from Chap. 1:

$$\ddot{v} + c\dot{v} + v(b + a \cdot v^2) = i(t) \tag{5.36}$$

We discussed that we will use a $(0, -2)$ element to implement $\ddot{v}$ and proposed a schematic in Sect. 4.6.2, reproduced in Fig. 5.27. Consider now the circuit in Fig. 5.28. From the U2 voltage follower, we get: $v_1 = v_2$.

The voltage drop across R is $i_2 R$, since the current into the noninverting input of U3 is zero. Also, since the noninverting input of U3 is at virtual ground, we have the **noninverting input voltage of** U1 to be equal to $i_2 R$. Hence:

$$\begin{aligned} i_3 &= -C_3 \frac{di_2 R}{dt} \\ &= RC_2C_3 \frac{d^2 v_2}{dt^2} \\ &= RC_2C_3 \frac{d^2 v_1}{dt^2} \end{aligned} \tag{5.37}$$

Since the current into the noninverting input of U2 is also zero, the CFOA ensures $i_1 = i_3$. So we finally have:

$$i_1 = RC_2C_3 \frac{d^2 v_1}{dt^2} \tag{5.38}$$

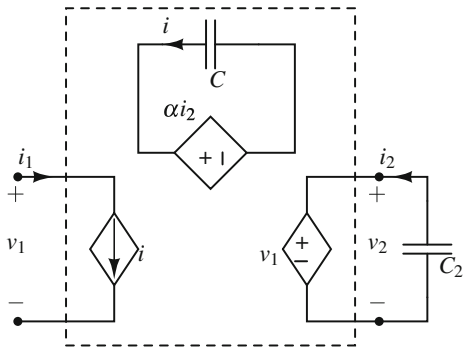


Fig. 5.27 A mutator for synthesizing $(0, -2)$ from a $(0, -1)$ element (capacitor C_2 at port 2)

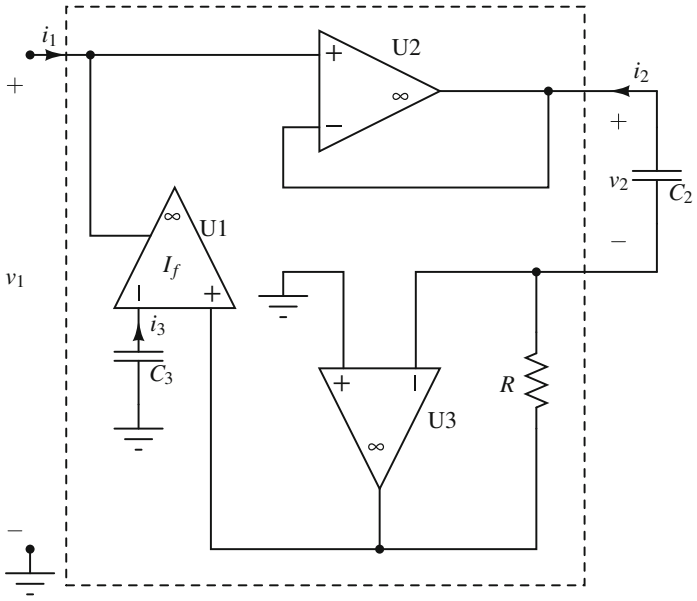


Fig. 5.28 One implementation of Fig. 4.51

Notice the equation above is dimensionally consistent. Exercise 5.4 asks you to complete the implementation of the Duffing oscillator using the higher-order element we implemented above.

5.6 Transistor Based Chaotic Circuits

Consider[13] the Colpitts Chaotic Oscillator[14] QUCS schematic shown in Fig. 5.29. Simulation results are shown in Fig. 5.30. The PWL equivalent circuit is shown in Fig. 5.31. The circuit equations based on the PWL model are:

$$\begin{aligned}
\frac{dV_{CE}}{dt} &= \frac{1}{C_1}\left(I_L - I_C\right) \\
\frac{dV_{BE}}{dt} &= -\frac{1}{C_2}\left(\frac{V_{EE} + V_{BE}}{R_{EE}} + I_L + I_B\right) \\
\frac{dI_L}{dt} &= \frac{1}{L}\left(V_{CC} - V_{CE} + V_{BE} - I_L R_L\right)
\end{aligned} \tag{5.39}$$

[13] This is another example of a circuit where a physical nonlinearity is the cause of chaos.

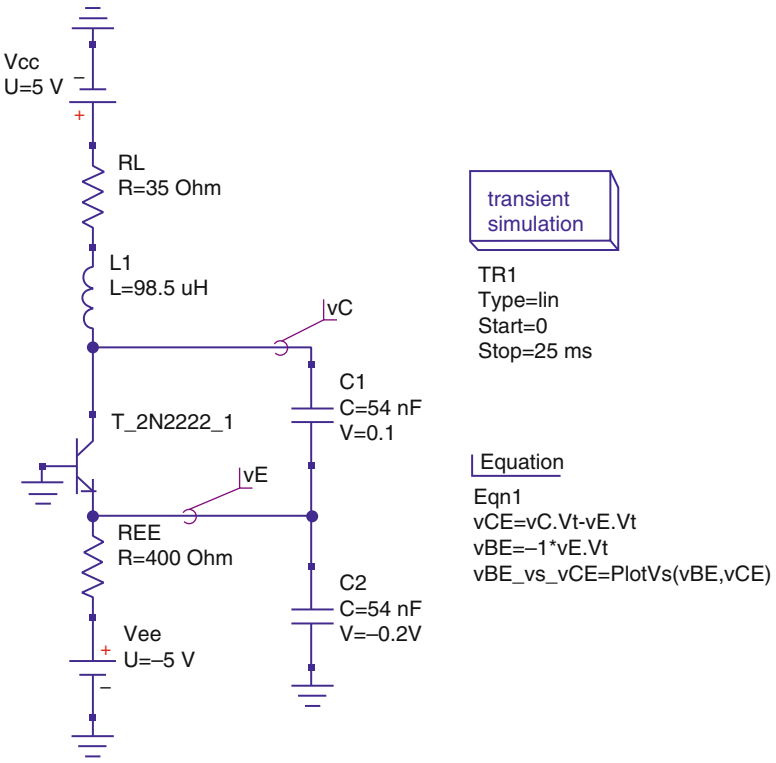


Fig. 5.29 A chaotic Colpitts oscillator

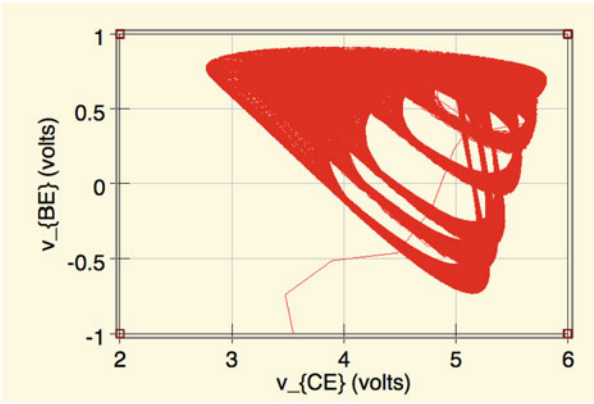


Fig. 5.30 QUCS simulated chaotic attractor. y-axis is v_{BE}, x-axis is v_{CE}. Notice the initial transient settling into the chaotic attractor

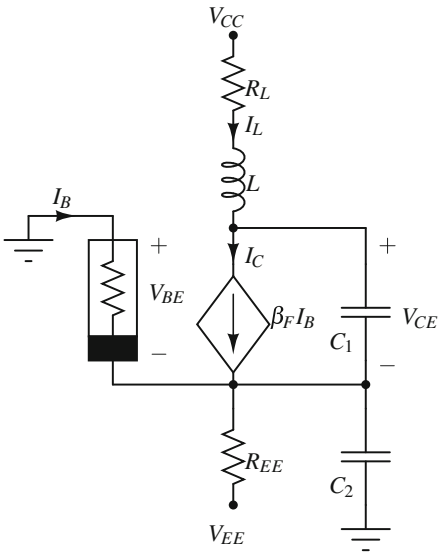


Fig. 5.31 PWL model of the Colpitts chaotic oscillator

Experimentally, it has been observed that the transistor is operating in either forward active or cutoff. Consequently, the following PWL linear function for I_B is used (compare to Fig. 2.18):

$$I_B = \begin{cases} 0 & \text{if } V_{BE} \leq V_{TH} \\ \frac{V_{BE} - V_{TH}}{R_{ON}} & \text{if } V_{BE} > V_{TH} \end{cases} \tag{5.40}$$

$$I_C = \beta_F I_B \tag{5.41}$$

where $V_{TH} \approx 0.75$ V is the threshold voltage, R_{ON} is the small-signal on-resistance of the base-emitter junction, and β_F is the forward current gain of the device.

We would like to conclude this chapter by illustrating the elegance of dimensionless scaling. We will only highlight the main concepts, leaving the actual dimensionless scaling of the equations to the reader.

There are a variety of concepts that need to be taken into account for dimensionless scaling of Eq. (5.39). The first is the time scale. There is every possible combination of time scaling: $\tau \stackrel{\triangle}{=} \frac{t}{R_L C1}$, $\tau \stackrel{\triangle}{=} \frac{t}{L/R_L}$, etc. in the circuit. So let us take a step back and **understand** the problem.[14] It seems like the primary mechanism of chaos should involve the inductor and **both** capacitor(s), as they are the dynamic elements in our PWL model. Hence a logical choice for time scale should involve some combination of L, C_1, C_2. Again from experience, the reader will realize by

[14]The reader has hopefully been applying the steps to problem solving elucidated in Example 1.10.2 throughout the book.

looking at the form of the RHS in Eq. (5.39) that:

$$\tau \stackrel{\triangle}{=} \sqrt{\frac{LC_1C_2}{C_1+C_2}} \tag{5.42}$$

is a "good" choice. Next, let us examine the I_B nonlinearity. Notice it can be rewritten as:

$$I_B = \begin{cases} 0 & \text{if } V_{BE}/V_{TH} \leq 1 \\ \frac{V_{TH}(V_{BE}/V_{TH}-1)}{R_{ON}} & \text{if } V_{BE}/V_{TH} > 1 \end{cases} \tag{5.43}$$

The justification for doing so is to define (for the second state equation in Eq. (5.39)) $y \stackrel{\triangle}{=} \frac{V_{BE}}{V_{TH}}$. But notice we can carry the simplification above for the PWL one step further:

$$\frac{I_B R_{ON}}{V_{TH}} = \begin{cases} 0 & \text{if } V_{BE}/V_{TH} \leq 1 \\ V_{BE}/V_{TH} - 1 & \text{if } V_{BE}/V_{TH} > 1 \end{cases} \tag{5.44}$$

The LHS of the equation above gives us a hint that:

$$z \stackrel{\triangle}{=} \frac{I_L R_{ON}}{V_{TH}} \tag{5.45}$$

Moreover, the nonlinear function simply becomes:

$$f(y) = \begin{cases} 0 & \text{if } y \leq 1 \\ y-1 & \text{if } y > 1 \end{cases} \tag{5.46}$$

We have now the dimensionless definitions for time, all state variables **and** the nonlinearity!

5.7 Conclusion to This Book

In this book we have covered lumped circuit theory. A reader who is probably familiar with classic linear circuit theory should hopefully now appreciate the advantage of following a "top-down" general approach to circuit theory: it enables them to properly analyze a very broad class of circuits. For example, consider our discussion of on opamps in Sect. 2.5. The reason we were able to properly analyze negative **and** positive feedback circuits is because we clearly (and correctly) separate static behavior from dynamic circuit behavior. Thus, the concept of instability in positive feedback circuits (opamp or otherwise) **requires** us to introduce (parasitic)

dynamic $v - i$ components such as capacitors and inductors (perhaps even the memristor for a hitherto undiscovered circuit). In this chapter, we saw how all the concepts integrated together in the form of chaotic circuits using fundamental circuit elements, opamps and transistors.

So, having been armed with the proper approach to circuit theory, where does a reader go from here? An answer to this question is for the reader to follow up on particular concepts of interest. Some (by no means, exhaustive) examples:

1. Recall the Simultaneity Postulate from Sect. 1.3. This postulate dictates when the techniques in this book are valid. Hence, a natural follow-up for the interested reader would be on distributed circuits,[15] where the simultaneity postulate is inapplicable.
2. Another approach would be to pick up books that exhaustively cover the ideas introduced here. For example, the graph theoretic approach to circuits is extensively covered in [4]. Another excellent very recent volume on the topic is [24].
3. Chaotic systems are the subject of many excellent books. An excellent starting point is [27]. Sprott has a chapter devoted exclusively to chaotic electrical circuits.

Exercises

5.1 Show that Fig. 5.2 (assuming $R_1 = R_2$) gives Eq. (5.2).

5.2 NOTE: This is an open-ended problem
Systematically change the values of the initial conditions; inductor, capacitor(s) values and the DP characteristic of $\mathcal{N}_R$, to obtain different behaviors in Chua's circuit. What happens in Fig. 5.6 if the parasitic series resistance for the inductor is removed? Does the simulation converge?

The reader should notice that it is much easier to simulate the dimensionless form in a mathematical package such as SageMath, rather than obtaining results from the circuit simulator. Why do you think this is the case? **Think** about **all** reasons. Also think about advantages of simulating the circuit equations.

5.3 Derive the circuit Eq. (5.3) for Fig. 5.5. Use Sect. 1.9.1.2 to derive the $\mathcal{N}_R$ characteristics in Eq. (5.4) from Fig. 5.9.

[15] We (Dr. Muthuswamy and Dr. Banerjee) are planning to write such a follow-up volume to this book, tentatively titled: "Advanced Nonlinear Circuits and Networks." In the follow-up book, we plan to first discuss rigorously how circuit theory is an approximation of electromagnetic field theory. This would then set us up nicely to discuss distributed circuits.

5.4 NOTE: This is an open-ended problem
Synthesize the Duffing oscillator from Sect. 5.5. We recommend approximating the cubic using a simple PWL nonlinearity (realized using one opamp).

5.5 Write system equations for the Chua oscillator from Fig. 5.19 in terms of charge and flux, using the ideas from Sect. 4.4.1.

5.6 NOTE: This is an open-ended problem
Design and implement a memristor simulation library for QUCS.

5.7 NOTE: This is an open-ended problem
Investigate chaotic circuit implementations where the source of chaos is a **physical (not emulated)** memristor's nonlinearity. As a starting point, we know of three devices that can be modeled by memristors: *pn*-junction diodes, thermistors, and discharge tubes. Hence a good approach would be to investigate existing chaotic circuits based on these devices and check if the underlying memristor nonlinearity is the cause of chaos.

Lab 5: Capstone Chaos Project(s)

In this final "lab," we will give some further suggestions for capstone projects. Note again that most of the exercises above are capstone projects.

1. At the turn of the twenty-first century, an active area of research in chaotic circuits (systems) is the notion of classifying chaotic attractors into "self-excited" and "hidden." We have discussed "self-excited" chaotic attractors: those that arise due to unstable equilibrium points. Kuznetsov et. al. coined the notion of "hidden" attractors, so named because they are present in a neighborhood of stable equilibrium points. An excellent starting point is the survey paper by Leonov and Kuznetsov [17]. Physically implementing chaotic circuits that exhibit hidden attractors are tricky because they exist close to stable equilibrium points, for a good example, see [28].
2. Mathematically investigating chaotic circuits is difficult because one has to be well-versed in the theory of dynamical systems. But, excellent works abound online. A good tractable starting point for the curious undergraduate would be the papers on **interval arithmetic** by Galias [11].
3. There has been no experimental confirmation of chaos from a physical (Josephson junction, *pn*-junctions, thermistor, discharge tube) memristor.
4. An energy approach to the study of chaotic systems.
5. Chaotic circuits with time delay, see [27], although a realistic circuit representation of chaotic time delay systems should probably use distributed components such as waveguides.
6. We also encourage the reader to look through some of the references in this chapter for exciting ideas related to chaotic circuits.
7. Further references for projects are [9, 10, 15, 21, 25].

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