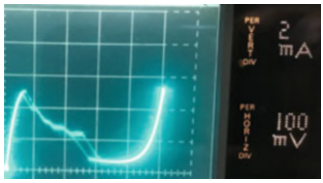
Chapter 3
Resistive Nonlinear Networks



Typical $v - i$ plot ($(0, 0)$ is in the lower-left corner) of a negative resistance device, the 1N3716 tunnel-diode. Notice the effects of parasitics are visible in the form of hysteresis in the negative resistance region.

Abstract Having described two-terminal and multi-terminal circuit elements in the "first part" of this book, we have hence discussed the laws of elements. We will now study, in this chapter and the next, KCL/KVL based circuit theoretic techniques that allow us to analyze circuits of varying degrees of "complexity" (a term we make precise in Chap. 4). We will study these techniques by following the classical approach: discussing static (resistive) networks in this chapter and then dynamic (inductive, capacitive, and memristive) networks in Chap. 4. Such a division is not accidental: in terms of circuit variables, dynamic networks usually involve differential equations, unlike static networks. Hence in this chapter we will study simpler resistive networks. We will first discuss the fundamental concept of operating points. Next, we will expand upon graph theoretic concepts and then discuss two of the most important techniques: nodal and tableau analysis. We will conclude the chapter by discussing some general properties of linear resistive networks (superposition, Thévenin-Norton theorems) and nonlinear resistive networks (strict passivity, strict monotonicity).

B. Muthuswamy, S. Banerjee, *Introduction to Nonlinear Circuits and Networks*,
https://doi.org/10.1007/978-3-319-67325-7_3

3.1 The Operating Point Concept

Given any circuit, one is interested in determining a solution [3]. For some circuits, there exists a unique solution. This is the case of a circuit containing two-terminal linear passive resistors and an independent current source connected to any two nodes of the circuit serving as input.[1] For other circuits, there may exist a unique solution, multiple solutions, or even no solution at all. This happens with circuits containing nonlinear resistors.

The solutions to a circuit with DC input are called **operating points** or **Quiescent (Q)-point**. The term **DC analysis** refers to the determination of operating points. It will be shown later that DC analysis of general dynamic circuits (with inductors, capacitors, and memristors) is equivalent to finding solutions of a resistive circuit which can be simply derived from the given circuit. The subject is of major importance in circuit theory and electronics. In this section, we will consider DC analysis for simple circuits using a variety of techniques.

The basic concepts of DC analysis can be illustrated with the simple circuit configuration shown in Fig. 3.1, i.e., the back-to-back connection of two one-ports at nodes 1 and 2. What is interesting to note is that this simple configuration, because it includes two unspecified one-ports, covers circuits with great generality. We assume that each one-port is specified by the following DP characteristics in terms of its port voltage and port current, v_a, i_a and v_b, i_b, respectively:

$$f_a(v_a, i_a) = 0 \quad \text{and} \quad f_b(v_b, i_b) = 0 \tag{3.1}$$

These are the generalizations of the branch characteristics since each one-port is formed by an interconnection of resistors. We are not concerned with what is inside of the one-ports N_a and N_b. Therefore we only need to use KCL and KVL to describe the port interconnection at the two nodes 1 and 2. KCL states:

$$i_a = -i_b \tag{3.2}$$

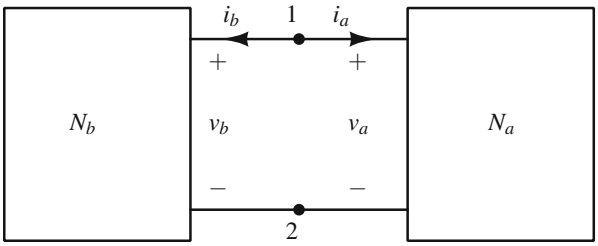


Fig. 3.1 Two resistive one-ports connected in parallel

[1] We will discuss existence and uniqueness theorem for general resistive nonlinear networks later in this chapter.

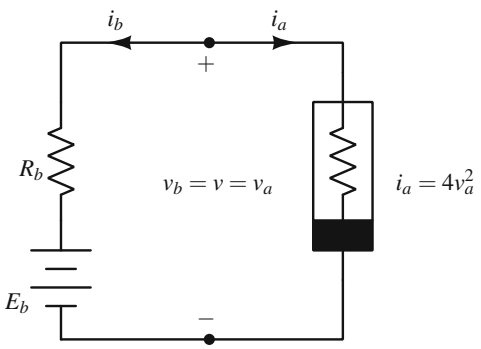


Fig. 3.2 Circuit of Fig. 3.1 with given characteristics of N_a and N_b

KVL states:

$$v_a = v_b \tag{3.3}$$

Therefore we can eliminate one set of voltage and current by combining Eqs. (3.1)–(3.3). Let us denote: $i_a = -i_b \triangleq i$ and $v_a = v_b \triangleq v$. The two resulting equations in terms of v and i are:

$$f_a(v, i) = 0 \quad \text{and} \quad f_b(v, -i) = 0 \tag{3.4}$$

The solutions of the two equations are the operating points that we are looking for. We will give a number of examples to illustrate the analytic, graphical, and PWL methods.

Example 3.1.1 (Analytical Method) Determine the operating points in Fig. 3.2.

Solution We will consider the nonlinear resistor as N_a, hence the specification $f(v_a, i_a)$ is:

$$i_a - 4v_a^2 = 0 \tag{3.5}$$

Let N_b be the series connection of the DC voltage source and linear resistor, which can be used to model a real battery connected in series with a resistive load. The specification $f(v_b, i_b)$ is:

$$v_b - E_b - R_b i_b = 0 \tag{3.6}$$

(continued)

Example 3.1.1 (continued)
As before, we let $i_a = -i_b \triangleq i$ and $v_a = v_b \triangleq v$. Hence $f(v_a, i_a)$ and $f(v_b, i_b)$ become:

$$i = 4v^2 \tag{3.7}$$

$$v = E_b - R_b i \tag{3.8}$$

These two equations lead to a quadratic equation in terms of v:

$$4R_b v^2 + v - E_b = 0 \tag{3.9}$$

The equation above can be solved for specific values of E_b and R_b. For instance, with $E_b = 2$ V and $R_b = 0.25\ \Omega$, the two solutions (and hence operating points) are: $v = 1$ V, -2 V and $i = 4$ A, 16 A, respectively.

In practice one rarely encounters problems in nonlinear circuits which can be solved analytically. Hence we will next see probably one of the most powerful graphical analysis techniques, the load line method.

Example 3.1.2 (Graphical (Load Line) Method) Determine the operating points in Fig. 3.2 graphically.

Solution The circuit in Fig. 3.2 represents a typical **biasing circuit** in DC design, i.e., a simple nonlinear circuit which consists of a battery, a resistor and an electronic device modeled by a nonlinear resistor with a specified $v-i$ characteristic.

The way to find the solution is to transcribe the characteristic of the battery and the resistor in the $v_b - i_b$ plane to the $v_a - i_a$ plane, where the characteristic of the device is plotted. We could of course transcribe the characteristic of the device from the $v_a - i_a$ plane onto the battery-resistor characteristic in the $v_b - i_b$ plane. But it is always easier to transcribe a linear equation.

Since $v_b = v_a$ and $i_b = -i_a$, the transcribed curve is the mirror image with respect to the v axis of the curve in the $v_b - i_b$ plane. This is superimposed with the characteristic of the nonlinear one-port N_a, as shown in Fig. 3.3, for $E_b = 2$ V, $R_b = 0.25\ \Omega$ from Example 3.1.1. There are two intersections of the two curves, and these give the operating points, equal to the values we obtained in Example 3.1.1.

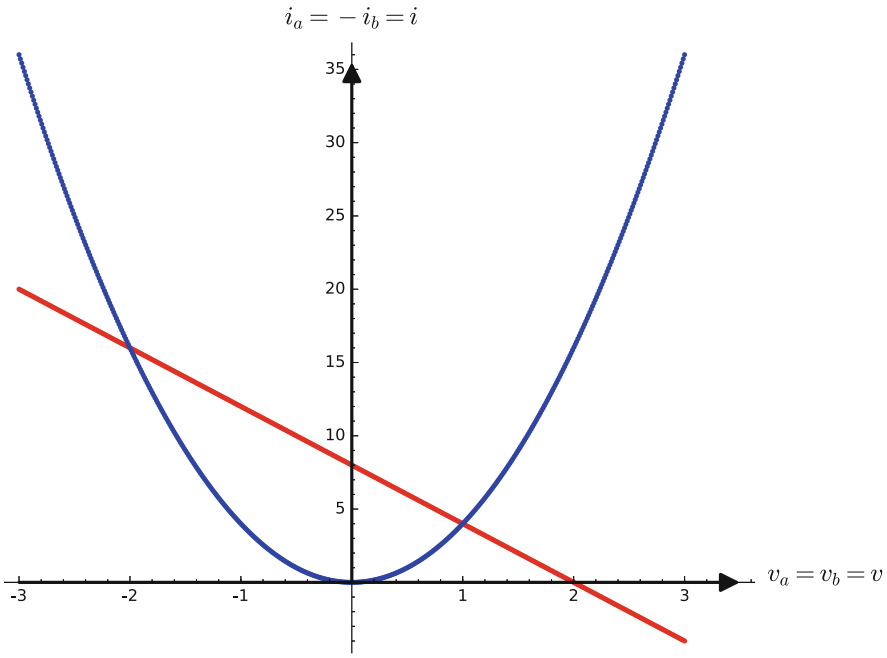


Fig. 3.3 The two one-port characteristics are superimposed on the $v - i$ plane

The transcribed battery-resistor characteristic in Fig. 3.3 is called the **load line**. It is a straight line which has E_b as its v-axis intercept and has E_b/R_b as its i-axis intercept. The load line method for determining the operating point(s) is used in practice because the $v - i$ characteristic of the one-port N_a is often given as a measured curve.

The third example shows how to use a PWL numerical method.

Example 3.1.3 (PWL Method) Consider the tunnel-diode circuit shown in Fig. 3.4 where the nonlinear characteristic N_a has been changed to that of a tunnel-diode with PWL characteristics. This device exhibits negative resistance characteristics. Determine the operating points of the circuit.

Solution Using the ideas from Sect. 1.9.1.2, we assume that the PWL characteristics for the tunnel-diode can be written as:

$$i = a_0 + a_1 v + b_1|v - E_1| + b_2|v - E_2| \tag{3.10}$$

(continued)

Example 3.1.3 (continued)
The parameters are: $a_0 = -\frac{1}{2}, a_1 = 2, b_1 = -\frac{5}{2}, b_2 = \frac{3}{2}, E_1 = 1, E_2 = 2$. Let the battery-resistor characteristic be given by $E_b = 6$ V, $R_b = 2\ \Omega$. The superimposed curves in the $v - i$ plane via the load line method are shown in Fig. 3.4b. Thus we know that the three operating points are at the three intersections Q_1, Q_2, Q_3. However, for the present, we wish to determine them analytically by using Eq. (3.10).

As we have shown in the Sect. 1.9.1.2 on PWL characteristics, the v axis can be divided into three regions:

$$\text{Region 1:} \quad v \leq E_1 = 1 \tag{3.11}$$

$$\text{Region 2:} \quad 1 < v \leq E_2 = 2 \tag{3.12}$$

$$\text{Region 3:} \quad v > 2 \tag{3.13}$$

In the three regions, Eq. (3.10) can be replaced by equations without absolute value signs as follows:

$$\text{Region 1:} \quad i = a_0 + a_1 v - b_1(v - E_1) - b_2(v - E_2) \tag{3.14}$$

$$\text{Region 2:} \quad i = a_0 + a_1 v + b_1(v - E_1) - b_2(v - E_2) \tag{3.15}$$

$$\text{Region 3:} \quad i = a_0 + a_1 v + b_1(v - E_1) + b_2(v - E_2) \tag{3.16}$$

For the battery-resistor combination, the equation is:

$$\begin{aligned} v &= E_b - R_b i \\ &= 6 - 2i \end{aligned} \tag{3.17}$$

First, solving Eqs. (3.14) and (3.17) for the solution in region 1, we obtain $V_{Q1} = \frac{6}{7}$. Similarly, solving Eqs. (3.15) and (3.17) for the solution in region 2, we obtain $V_{Q2} = \frac{4}{3}$. Finally, solving Eqs. (3.16) and (3.17), we get $V_{Q3} = \frac{8}{3}$ for region 3.

It is crucial to remember that we must check these calculated solutions to see whether they fall in the assumed regions. If they indeed do, they are valid solutions, otherwise they are called virtual solutions. They do not corresponding to reality, they are artifacts of the method. In the present case, we see that all three voltages are valid solutions because they do indeed fall in the respective regions: $V_{Q1} = \frac{6}{7} \leq 1$, $V_{Q2} = \frac{4}{3}$ falls in region 2 ($1 < v \leq 2$) and $V_{Q3} = \frac{8}{3}$ falls in region 3 ($v > 2$). Since all voltage solutions are confirmed to be valid, we can find the corresponding currents from Eq. (3.17). Thus, the operating points are : $\left(\frac{6}{7}, \frac{18}{7}\right), \left(\frac{4}{3}, \frac{7}{3}\right), \left(\frac{8}{3}, \frac{5}{3}\right)$.

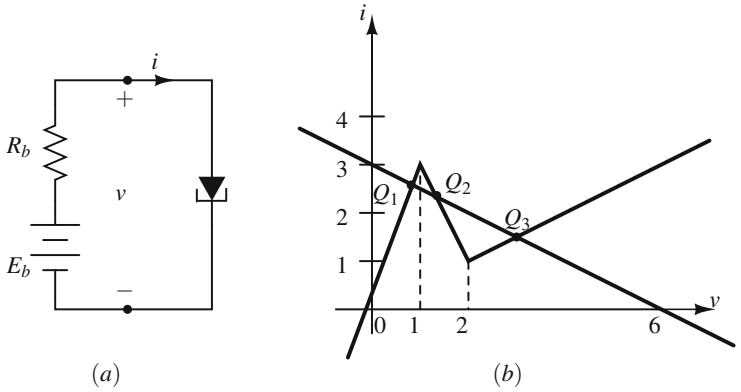


Fig. 3.4 Operating points of a tunnel-diode circuit determined by the PWL method (**a**) Circuit (**b**) load line

3.1.1 Small Signal Analysis

There is a good reason to call the solutions to DC analysis "operating points." When a circuit is used, some input signal (example, a sinusoidal waveform) is applied to it so that we get a useful output. An operating point specifies a region in the $v - i$ plane in the neighborhood of which the actual voltage and current in the circuit vary as a function of time. If the applied signal has a sufficiently small voltage or current (in magnitude), the circuit can be analyzed to a good approximation by using **small-signal analysis**.

Consider the tunnel-diode circuit shown in Fig. 3.5 where, in addition to the circuit elements treated earlier, there is a sinusoidal voltage source:

$$v_s(t) = V_m \cos \omega t \tag{3.18}$$

First we assume that the biasing circuit, i.e., the circuit without the signal source $v_s(t)$ has been designed properly so that there is only one operating point Q as shown. To be specific, assume that it lies where the slope is negative. As $v_s(t)$ varies with time, we may imagine that the load line is being moved parallel to the biasing load line as shown in the figure. Thus the solution of the circuit driven by the input signal $v_s(t)$ can be determined graphically point by point as the intersection point of the characteristic of the tunnel diode and the moving load line. This gives us a mental picture of the influence of the signal source $v_s(t)$ as t changes.

Let the $v - i$ characteristic of the tunnel diode be specified by:

$$i = \hat{i}(v) \tag{3.19}$$

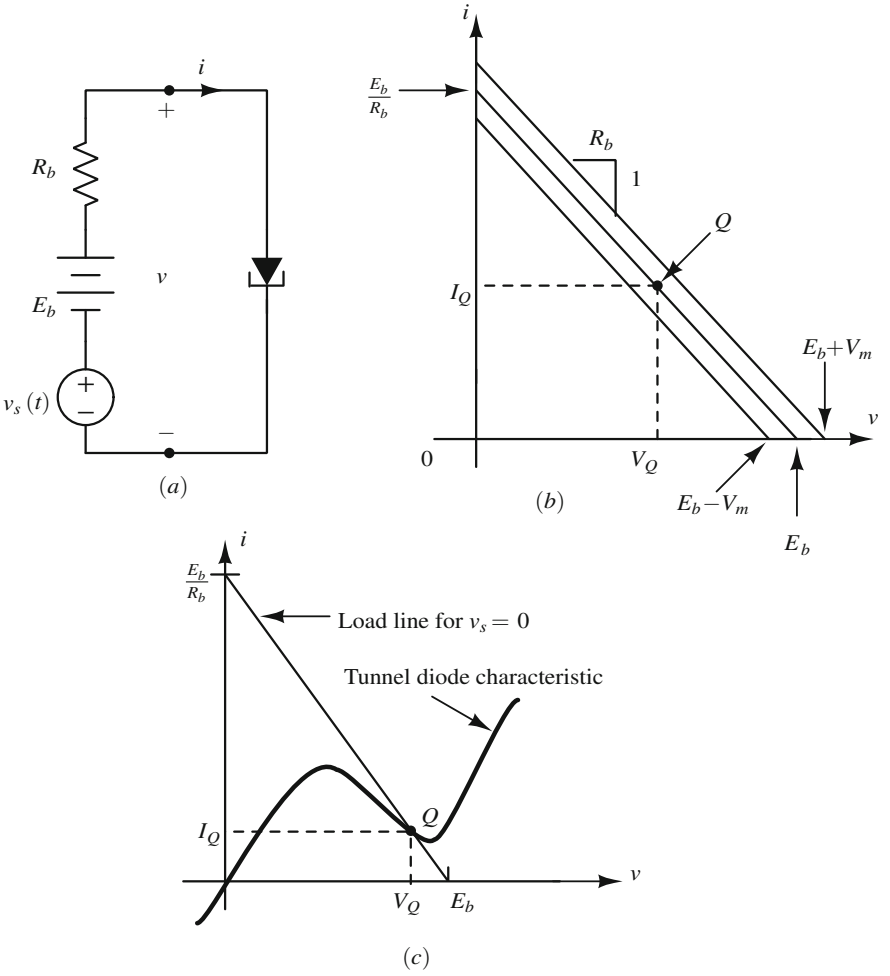


Fig. 3.5 (**a**) Tunnel-diode circuit with signal source $v_s(t)$. (**b**) Moving load line, and (**c**) linear approximation to the diode characteristic at the operating point Q

KCL states that all branch currents in the circuit are the same. KVL for the single loop in the circuit yields the following equation:

$$v(t) = v_s(t) + E_b - R_b i(t) \tag{3.20}$$

Combining Eqs. (3.19) and (3.20) we obtain a single equation with $v(\cdot)$ as the unknown to be solved for:

$$v(t) = v_s(t) + E_b - R_b \hat{i}[v(t)] \tag{3.21}$$

This cannot be solved readily since we only know the curve given by the tunnel-diode data sheet. Of course for each value of t, we can find $v(t)$, thus $v(\cdot)$ can be determined point by point.

As seen in Fig. 3.5b, the actual signal voltage $v(t)$ and signal current $i(t)$ lie on the characteristic in the neighborhood[2] of Q. Therefore, let us denote:

$$v(t) \triangleq V_Q + \tilde{v}(t) \tag{3.22}$$

$$i(t) \triangleq I_Q + \tilde{i}(t) \tag{3.23}$$

where (V_Q, I_Q) is the operating point. This, in essence, shifts the coordinates from the origin to the operating point. The two equations (3.19) and (3.20) are satisfied with the signal $v_s(t) = 0$, i.e.,

$$I_Q = \hat{i}(V_Q) \tag{3.24}$$

$$V_Q = E_b - R_b I_Q \tag{3.25}$$

Note that $\tilde{v}(t)$ and $\tilde{i}(t)$ book keep the displacement of the instantaneous operating point away from (V_Q, I_Q) when the signal is applied. The pertinent concept above can be illustrated with the two circuits shown in Fig. 3.6. Figure 3.6a gives the DC equivalent circuit which is specified by Eqs. (3.24) and (3.25). We can eliminate E_b in Eq. (3.20) by using Eq. (3.25):

$$v(t) = v_s(t) + V_Q + R_b(I_Q - i(t)) \tag{3.26}$$

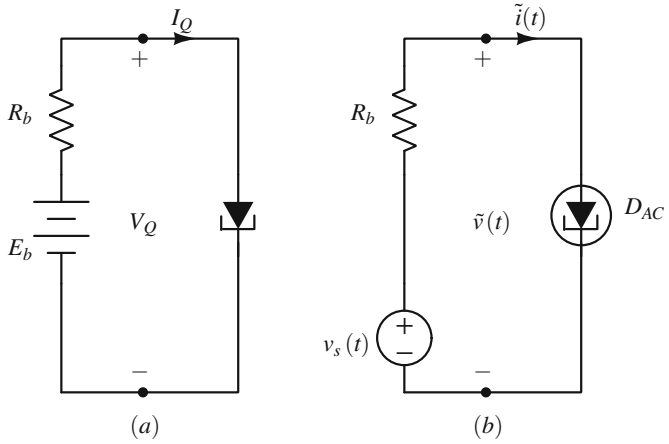


Fig. 3.6 The circuit shown in Fig. 3.5a can be viewed in terms of (**a**) its DC equivalent circuit and (**b**) its AC equivalent circuit, where the diode characteristic has its origin at (V_Q, I_Q). D_{AC} denotes the diode with the origin shifted

[2]Figure 3.5b has been exaggerated for clarity.

Using the definitions of V_Q and I_Q from Eqs. (3.22) and (3.23), respectively, we can eliminate $v(t)$ and $i(t)$ in the equation above to obtain:

$$\tilde{v}(t) = v_s(t) - R_b\tilde{i}(t) \tag{3.27}$$

This equation can be represented by the circuit shown in Fig. 3.6b, where D_{AC} represents the AC behavior of the diode measured with respect to the operating point Q. To determine $(\tilde{v}(t), \tilde{i}(t))$, we substitute Eqs. (3.22) and (3.23) into (3.19) to obtain:

$$I_Q + \tilde{i}(t) = \hat{i}[V_Q + \tilde{v}(t)] \tag{3.28}$$

Up to now our analysis is general. At this juncture, let us assume that the amplitude of the sinusoidal voltage $v_s(t)$ is small, i.e., $V_M << E$. Thus the voltage $\tilde{v}(t)$ is "small" in comparison with V_Q. What follows below is **small-signal analysis**.

Taking the first two terms of the Taylor series expansion of $\hat{i}[V_Q + \tilde{v}(t)]$ about the points (V_Q, I_Q), we get:

$$\begin{aligned} i(t) &= I_Q + \tilde{i}(t) \\ &= \hat{i}[V_Q + \tilde{v}(t)] \\ &\approx \hat{i}[V_Q] + \left(\left.\frac{d\hat{i}}{dv}\right|_{V_Q}\right)\tilde{v}(t) \quad \forall t \end{aligned} \tag{3.29}$$

Geometrically (see Fig. 3.5c), the approximation carried out in Eq. (3.29) amounts to replacing the nonlinear diode characteristic by its linear approximation about the operating point Q. In other words:

$$\tilde{i}(t) \approx \left(\left.\frac{d\hat{i}}{dv}\right|_{V_Q}\right)\tilde{v}(t) \tag{3.30}$$

The term $\left.\frac{d\hat{i}}{dv}\right|_{V_Q}$ is the slope of the diode characteristic at the operating point Q; note that in the present case it is negative. Let us denote:

$$G \triangleq \left.\frac{d\hat{i}}{dv}\right|_{V_Q} \tag{3.31}$$

where G is negative. The quantity $\left.\frac{d\hat{i}}{dv}\right|_{V_Q}$ is called the **small-signal conductance** of the diode at the operating point Q. In other words, we simply have:

$$\tilde{i}(t) = G\tilde{v}(t) \tag{3.32}$$

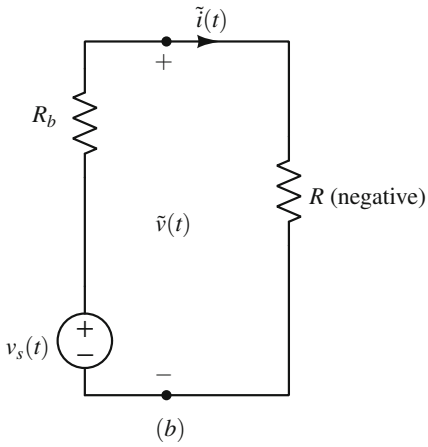


Fig. 3.7 Small-signal equivalent circuit for the tunnel-diode

Hence D_{AC} from Fig. 3.6 is interpreted as a **negative** small-signal resistance $R = \frac{1}{G}$ as shown in Fig. 3.7. The small-signal equivalent circuit is a linear circuit because the two resistors are linear. Note that the resistance R is negative, thus we have a linear **active** resistor in the circuit. The solution can be obtained immediately from the small-signal equivalent circuit:

$$\tilde{i}(t) = \frac{V_m}{R_b + R} \cos \omega t \tag{3.33}$$

$$\tilde{v}(t) = \frac{R V_m}{R_b + R} \cos \omega t \tag{3.34}$$

Since R is negative, the factor $|R/(R_b + R)|$ can be made very large. From the equations above, we can define the **small-signal power gain** as:

$$\mathscr{P} \triangleq \left| \frac{\tilde{v}\tilde{i}}{v_s \tilde{i}} \right| = \left| \frac{R}{R_b + R} \right| \tag{3.35}$$

We will now derive the small-signal (linearized) hybrid two-port representation of the npn bipolar transistor (recall Sect. 2.2.2). In other words, we are extending small-signal analysis above from a two-terminal element (diode) to a three-terminal element (transistor). The procedure is the same, the only difference being we will obtain a matrix for our small-signal hybrid parameter(s).

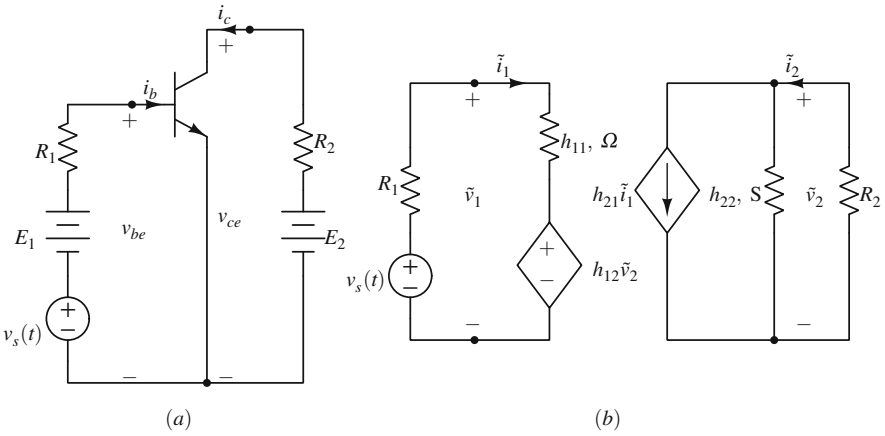


Fig. 3.8 (**a**) BJT Common-Emitter (CE) amplifier. (**b**) Small-signal model

Example 3.1.4 Derive the small-signal model for the CE amplifier shown in Fig. 3.8a.

Solution We will assume the input is a small-signal source, $v_s(t) = V_m \cos \omega t$. We will then see that the output voltage v_{ce} contains an amplified waveform at the same angular frequency ω.

The hybrid representation of the CE amplifier is repeated below:

$$v_{be} = \hat{v}_{be}(i_b, v_{ce}) \tag{3.36}$$

$$i_c = \hat{i}_c(i_b, v_{ce}) \tag{3.37}$$

Obviously, without the small-signal source v_s, the operating point (V_{beQ}, I_{bQ}), (V_{ceQ}, I_{cQ}) satisfies not only the above two equations but also Eqs. (3.40) and (3.41). They are written as follows:

$$V_{beQ} = \hat{v}_{be}\left(I_{bQ}, V_{ceQ}\right) \tag{3.38}$$

$$I_{cQ} = \hat{i}_c\left(I_{bQ}, V_{ceQ}\right) \tag{3.39}$$

$$V_{beQ} = E_1 - R_1 I_{bQ} \tag{3.40}$$

$$V_{ceQ} = E_2 - R_2 I_{cQ} \tag{3.41}$$

(continued)

Example 3.1.4 (continued)
When the signal source $v_s(t)$ is present in the circuit, we may express the four signal variables $v_{be}(t)$, $i_b(t).v_{ce}(t)$, $i_c(t)$ for all t as:

$$v_{be}(t) = V_{beQ} + \tilde{v}_1(t) \tag{3.42}$$

$$i_b(t) = I_{bQ} + \tilde{i}_1(t) \tag{3.43}$$

$$v_{ce}(t) = v_{ceQ} + \tilde{v}_2(t) \tag{3.44}$$

$$i_c(t) = I_{cQ} + \tilde{i}_2(t) \tag{3.45}$$

where $\tilde{v}_{1,2}(t), \tilde{i}_{1,2}(t)$ represent the "small" displacements of voltages and currents from the fixed operating point Q. At this juncture it remains only to determine these small-signal voltages and currents.

First substituting Eqs. (3.42) through (3.45) into Eqs. (3.36) and (3.37), we obtain:

$$\begin{aligned} v_{be}(t) &= V_{beQ} + \tilde{v}_1(t) \\ &= \hat{v}_{be}[I_{bQ} + \tilde{i}_1(t), V_{ceQ} + \tilde{v}_2(t)] \end{aligned} \tag{3.46}$$

$$\begin{aligned} i_c(t) &= I_{cQ} + \tilde{i}_2(t) \\ &= \hat{i}_c[I_{bQ} + \tilde{i}_1(t), V_{ceQ} + \tilde{v}_2(t)] \end{aligned} \tag{3.47}$$

No approximation has been introduced up to this step. Next we assume that the signal $v_s(t)$ is "small" and take the first two terms of the Taylor series expansions of $\hat{v}_{be}(\cdot, \cdot)$ and $\hat{i}_c(\cdot, \cdot)$ about the operating point Q. We obtain the following approximation:

$$v_{be}(t) \approx \hat{v}_{be}(I_{bQ}, V_{ceQ}) + \left.\frac{\partial \hat{v}_{be}}{\partial i_b}\right|_Q \tilde{i}_1(t) + \left.\frac{\partial \hat{v}_{be}}{\partial v_{ce}}\right|_Q \tilde{v}_2(t) \tag{3.48}$$

$$i_c(t) \approx \hat{i}_c(I_{bQ}, V_{ceQ}) + \left.\frac{\partial \hat{i}_c}{\partial i_b}\right|_Q \tilde{i}_1(t) + \left.\frac{\partial \hat{i}_c}{\partial v_{ce}}\right|_Q \tilde{v}_2(t) \tag{3.49}$$

(continued)

Example 3.1.4 (continued)
Comparing Eqs. (3.46) and (3.47) with Eqs. (3.48) and (3.49), and using Eqs. (3.36) and (3.37), we obtain the following approximations:

$$\tilde{v}_1(t) \approx \left.\frac{\partial \hat{v}_{be}}{\partial i_b}\right|_Q \tilde{i}_1(t) + \left.\frac{\partial \hat{v}_{be}}{\partial v_{ce}}\right|_Q \tilde{v}_2(t) \tag{3.50}$$

$$\tilde{i}_2(t) \approx \left.\frac{\partial \hat{i}_c}{\partial i_b}\right|_Q \tilde{i}_1(t) + \left.\frac{\partial \hat{i}_c}{\partial v_{ce}}\right|_Q \tilde{v}_2(t) \tag{3.51}$$

The two equations can be viewed as hybrid equations relating the small signals $\tilde{i}_1$ and $\tilde{v}_2$ to $\tilde{v}_1$ and $\tilde{i}_2$. Hence we have:

$$\begin{bmatrix} \tilde{v}_1 \\ \tilde{i}_2 \end{bmatrix} = \mathbf{H} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_2 \end{bmatrix} \tag{3.52}$$

where:

$$\mathbf{H} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \triangleq \begin{bmatrix} \frac{\partial \hat{v}_{be}}{\partial i_b} & \frac{\partial \hat{v}_{be}}{\partial v_{ce}} \\ \frac{\partial \hat{i}_c}{\partial i_b} & \frac{\partial \hat{i}_c}{\partial v_{ce}} \end{bmatrix}_Q \tag{3.53}$$

Figure 3.8b shows the small-signal model for the CE amplifier. Exercise 3.1 asks the reader to derive the small-signal voltage gain.

If we can build an amplifier with a single transistor, as Exercise 3.1 shows, why then do we have more than one transistor in the schematic for μA741 in Fig. 2.25? One answer to this question is the concept of **gain-bandwidth product**. A detailed discussion is beyond the scope of this book, but conceptually, we need to ensure that the gain of the amplifier is **ideally** maintained across a range of frequencies (the **bandwidth** of the amplifier). In other words, the gain-bandwidth product is a constant. In a nutshell, we need the transistors shown in Fig. 2.25 to ensure a constant gain-bandwidth product. Nevertheless, the fact is: we are able to achieve a constant gain across a large bandwidth with so **few** transistors.

In Sect. 4.2.2.3, we will extend small signal analysis to nonlinear dynamic networks.

3.2 Matrix Formulation of Kirchhoff's Laws

So far, we have been using KCL and KVL to describe simple circuits. For more complicated circuits, other formal circuit techniques of circuit analysis exist. These methods will help us systematically derive the circuit equations. Before discussing these methods, we need to expand upon the graph theoretic concepts and matrix formulation of Kirchhoff's laws, that were introduced in Chap. 1. This will help us in the discussion of nodal and tableau analysis techniques later in this chapter.

3.2.1 Cut Sets, Hinged Graphs, and Linear Independence

Definition 3.1 Given a network graph $\mathscr{G}$, a **cut set** is a set of branches $\mathscr{C}$ of $\mathscr{G}$ having the property that if we "cut" (as if with scissors) each branch in the set once, $\mathscr{G}$ gets separated into two disconnected **subgraphs** $\mathscr{G}_1$ and $\mathscr{G}_2$, and if we leave any one branch of the set uncut, $\mathscr{G}$ remains connected in one piece by that branch.

For instance, consider the digraph shown in Fig. 3.9. The set of branches {3, 4, 8, 6} is a cut set, since cutting these branches once separates the graph into two subgraphs. Similarly, the set {3, 4, 8, 5, 7} is also a cut set.

Some remarks about cut sets:

1. Any cut set creates a partition of the set of nodes in the graph into two subsets
2. To any cut set corresponds a gaussian surface (recall Definition 1.9) which cuts precisely the same branches
3. Similarly, to any gaussian surface corresponds either one cut set or a union of cut sets. For example, $\mathscr{S}_1$ in Fig. 3.10.
4. To each cut set we can define arbitrarily a **reference direction**, as shown by the arrows attached to the cut sets in Fig. 3.10.

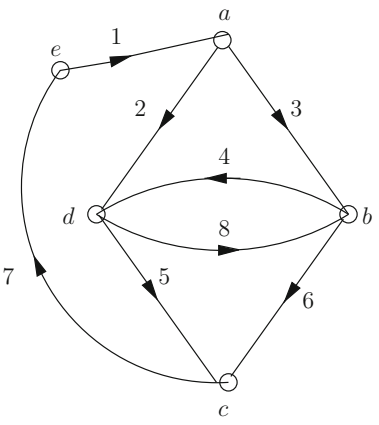


Fig. 3.9 A digraph associated with a bridge circuit

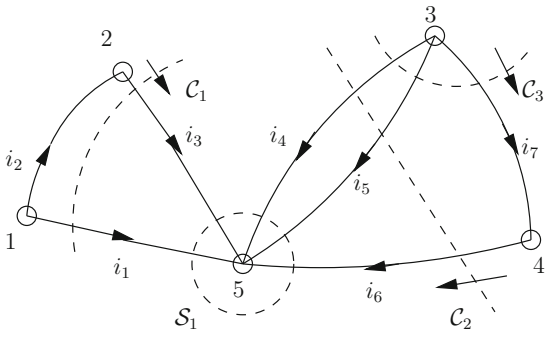


Fig. 3.10 Digraph illustrating cut sets

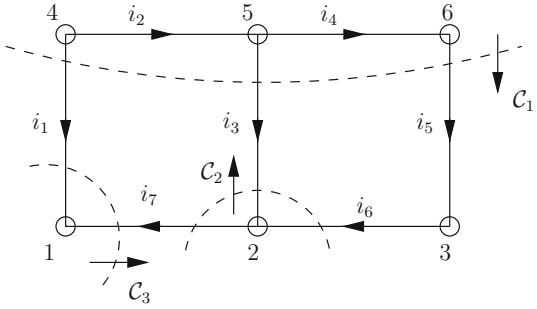


Fig. 3.11 Digraph for Example 3.2.1

Definition 3.2 KCL (Cut Set Law): For all lumped circuits, for all time t, the algebraic sum of the currents associated with any cut set is equal to zero.

Example 3.2.1 The digraph in Fig. 3.11 shows some example cut sets. Write the KCL equation associated with those cut sets.

Solution Cut set $\mathscr{C}_1$ consists of the set of branches $\{\beta_1, \beta_3, \beta_5\}$. Since all currents are in the direction of the cut set, the KCL associated with $\mathscr{C}_1$ is:

$$i_1 + i_3 + i_5 = 0 \tag{3.54}$$

For $\mathscr{C}_2$, we have:

$$i_7 - i_3 - i_6 = 0 \tag{3.55}$$

$-i_3, -i_6$ are because both those currents are going in, while the cut set direction is pointing out. Similarly, for $\mathscr{C}_3$, we have:

$$-i_1 - i_7 = 0 \tag{3.56}$$

Combined with the KCL definitions from Chap. 1, we have learned three forms of KCL, namely, in terms of (1) gaussian surfaces, (2) nodes, and (3) cut sets.

Theorem 3.1 (KCL Equivalence Theorem) *The three forms of KCL are equivalent: (1) KCL gaussian surface ⇔ (2) KCL node law ⇔ (3) KCL cut sets*

Proof We will only prove the implication as the other direction can be proved in a similar manner.

- (1) ⇒ (2) Simply use the gaussian surface that surrounds only the node in question. For example, consider node 5 in Fig. 3.10. For the gaussian surface $\mathscr{S}_1$, KCL applied to $\mathscr{S}_1$ is identical to KCL applied to node 5:

$$i_1 - i_3 - i_4 - i_5 - i_6 = 0 \tag{3.57}$$

- (2) ⇒ (3) Any cut set partitions the set of nodes into two subsets. Writing the KCL equation for each node in such a subset and adding the results, we obtain the cut set equation, except for maybe a -1 factor. For example, consider the cut set $\mathscr{C}_2$ in Fig. 3.10. If we add the KCL equations applied to nodes 3 and 4, we obtain:

$$i_4 + i_5 + i_6 = 0 \tag{3.58}$$

  Note that i_7 cancels out in the addition, resulting in the KCL cut set equation for $\mathscr{C}_2$.
- (3) ⇒ (1) It is easy to demonstrate that the set of branches cut by a gaussian surface is either a cut set or a disjoint union of cut sets. So given any gaussian surface, let us write the KCL equation for each of these cut sets; then adding or subtracting these equations, we obtain the KCL equation for the gaussian surface. For example, consider gaussian surface $\mathscr{S}_1$ in Fig. 3.10. It is the union of the cut set $\{\beta_1, \beta_3\}$ and cut set $\{\beta_4, \beta_5, \beta_6\}$ whose equations are, respectively,

$$-i_1 - i_3 = 0 \tag{3.59}$$

$$-i_4 - i_5 - i_6 = 0 \tag{3.60}$$

  Adding the two equations above, we get:

$$-i_1 - i_3 - i_4 - i_5 - i_6 = 0 \tag{3.61}$$

  which is the KCL equation for the gaussian surface $\mathscr{S}_1$. □

Up to now, we have assumed the circuit is connected. But, recall from our discussion of transformers in Sects. 2.2.1.3 and 2.2.3.1 that a circuit with a physical transformer is not connected. It turns out that we can easily take care of this situation. We first generalize the element graph representation from one-port to a two-port, by using two branches and four nodes for its element graph as shown in Fig. 3.12.

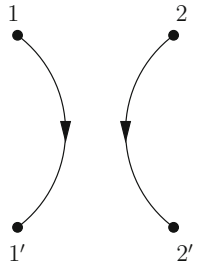


Fig. 3.12 The element graph of a two-port

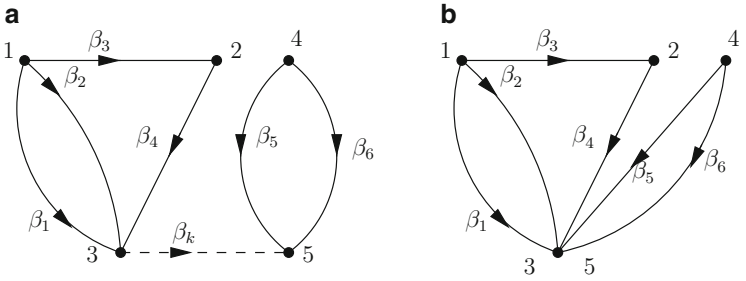


Fig. 3.13 (**a**) Connecting nodes 3 and 5 by a branch k. (**b**) Soldering together nodes 3 and 5 to obtain a hinged graph

Next, we need to understand the element graph of a two-port consists of two branches which are not connected, because it signifies that port voltages or port currents at different ports are not related because of connections but rather are **coupled** because of physical phenomena within the element. For example, recall from Sect. 2.2.3.1 that physical transformer port voltages are coupled magnetically via the flux linkages among the various windings.

To avoid an unconnected digraph (circuit graph), we can tie together the two separate ports of a digraph at two arbitrary nodes by a branch. This is illustrated in Fig. 3.13a where nodes 3 and 5 are tied together by a branch k. This connection does not change any branch voltage or current in the original circuit. This is easily seen because, by using KCL with a gaussian surface which encloses one of the separate parts of the graph and which cuts branch k, the current i_k is zero. If $i_k = 0$, it amounts to an open circuit or no connection; thus we have not changed the behavior of the circuit. Next, since voltages are measured between nodes, we choose a ground node for the separate parts. If we choose nodes 3 and 5 as the ground nodes for the separate parts, we may "solder" together node 3 and node 5 as shown in Fig. 3.13b to make them the common ground node. The graph so obtained is called a **hinged graph**. With the introduction of the concept of a hinged graph, we have generalized our treatment so far to include two-ports and multi-ports, that is, we can always

assume without loss of generality that any lumped circuit and its associated digraph are connected.

We now have all the graph theoretic concepts that we need for this chapter. But, before discussing independent KCL and KVL equations, we need to discuss the concept of **linear independence**.

Consider a set of m linear algebraic equations in n unknowns. For $j = 1, 2, \cdots, m$

$$f_j(x_1, x_2, \ldots, x_n) \triangleq \alpha_{j1}x_1 + \alpha_{j2}x_2 + \cdots + \alpha_{jn}x_n = 0 \tag{3.62}$$

where the α_{jk}'s are real or complex numbers. It is important to decide whether or not each equation brings new information not contained in the others; equivalently, it is important to decide whether the equations are linearly independent. These m equations are said to be **linearly dependent** iff there are constants $k_1, k_2, \cdots, k_m$ and **not all zero** such that:

$$\sum_{j=1}^{m} k_j f_j(x_1, x_2, \ldots, x_n) = 0 \quad \forall\, x_1, x_2, \ldots, x_n \tag{3.63}$$

Clearly if these m equations are linearly dependent, then at least one equation may be written as a linear combination of the others; in other words, that equation repeats the information contained in the others.

It is crucial to note that the LHS of Eq. (3.63) must be zero **for all** values of $x_1, x_2, \ldots, x_n$.

Example 3.2.2 Are the equations below ($m = 3$ and $n = 4$) linearly dependent?

$$\begin{aligned} x_1 - x_2 + x_3 + 3x_4 &= 0 \\ 2x_1 + 3x_2 - x_3 - 4x_4 &= 0 \\ -4x_1 - 11x_2 + 5x_3 + 18x_4 &= 0 \end{aligned}$$

Solution Direct calculation shows that with $k_1 = 2, k_2 = -3$ and $k_3 = -1$ the condition for Eq. (3.63) holds; in other words, these three equations are linearly dependent.

A set of m linear algebraic equations is said to be **linearly independent** iff it is not linearly dependent. In practice, we use gaussian elimination to decide whether or not a given set of linear equations is linearly dependent.

3.2.2 Independent KCL Equations

For a given circuit, we can write KCL equations by the node law or the cut set law, or using gaussian surfaces. How many of the KCL equations are linearly independent and how to write a complete set that contains all the necessary information as far as KCL is concerned are the subjects of this subsection. We will give a systematic treatment by means of the digraph of the circuit under consideration: in particular, a list of nodes, a list of branches, and for each branch the specification of the node that the branch leaves and enters. This is done by the **incidence matrix** $\mathbf{A}_a$ of the digraph.

Let the digraph $\mathscr{G}$ have n nodes and b branches, then $\mathbf{A}_a$ has n rows—one row for each node—and b columns—one column for each branch. To see how the matrix is built up consider the four-node six-branch digraph shown in Fig. 3.14. Let us write the KCL equations for each node:

$$\begin{aligned} i_1 + i_2 \qquad\qquad - i_6 &= 0 \\ -i_1 \quad - i_3 + i_4 \qquad\quad &= 0 \\ - i_2 + i_3 \quad + i_5 \quad &= 0 \\ - i_4 - i_5 + i_6 &= 0 \end{aligned} \tag{3.64}$$

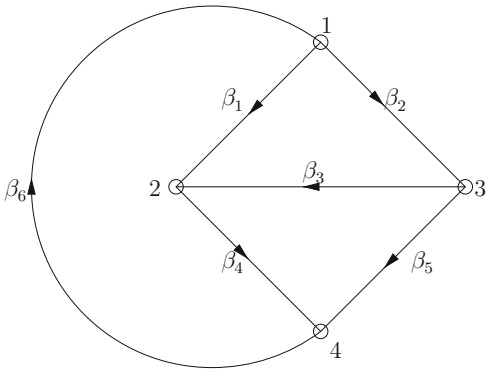


Fig. 3.14 A digraph with four nodes and six branches

In matrix form, it reads:

$$\begin{array}{c} \\ \text{Node 1}\rightarrow \\ \text{Node 2}\rightarrow \\ \text{Node 3}\rightarrow \\ \text{Node 4}\rightarrow \end{array} \overset{\begin{array}{cccccc} \text{Branch 1} & & & & & \text{Branch 6} \end{array}}{\begin{bmatrix} 1 & 1 & 0 & 0 & 0 & -1 \\ -1 & 0 & -1 & 1 & 0 & 0 \\ 0 & -1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & -1 & 1 \end{bmatrix}} \begin{pmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{3.65}$$

Since each row corresponds to a node and each column corresponds to a branch, we have the 4×6 incidence matrix $\mathbf{A}_a$. For example, for node 4 we have i_4, i_5 coming in and i_6 going out and hence the 4th row in the matrix has two -1 s and one $+1$. Similarly, branch β_1 that connects node 1 to 2 has one $+1$ and one -1 in column 1.

In general, for any n-node b-branch **connected** digraph $\mathscr{G}$ which does **not** contain **self-loops**,[3] the matrix $\mathbf{A}_a$ is specified as follows: For $i = 1, 2, \cdots, n$ and $k = 1, 2, \cdots b$:

$$a_{ik} = \begin{cases} +1 & \text{if branch } k \textbf{ leaves} \text{ node } i \\ -1 & \text{if branch } k \textbf{ enters} \text{ node } i \\ 0 & \text{if branch } k \text{ does not touch node } i \end{cases} \tag{3.66}$$

and the node n node equations of $\mathscr{G}$ read:

$$\mathbf{A}_a \mathbf{i} = \mathbf{0} \tag{3.67}$$

where $\mathbf{i} = (i_1, i_2, \cdots, i_b)^T$ is called the **branch current vector**.

Example 3.2.3 Is the incidence matrix in Eq. (3.65) full row rank?

Solution Equivalently, the question posed is asking whether the KCL equations corresponding to the incidence matrix are linearly dependent or independent. We could transform the incidence matrix to row-echelon form. Instead, simple observation shows that with $k_1 = k_2 = k_3 = k_4 = 1$, the condition for Eq. (3.63) holds; in other words, the incidence matrix is **not** full row rank.

Example 3.2.3 shows that each column of $\mathbf{A}_a$ has precisely a single $+1$ and a single -1; consequently, if we add together n equations in Eq. (3.67), all the

[3] A self-loop contains precisely one node and one branch, they are not loops according to Definition 1.6 (of a loop).

variables $i_1, i_2, \cdots, i_b$ cancel out; equivalently, the n KCL equations are linearly dependent.

But, suppose that for a **connected**[4] digraph $\mathscr{G}$ we choose a ground node and we throw away the corresponding KCL equation, then the remaining $n-1$ equations are linearly independent. This is the defining property of this subsection, hence we state it formally as a theorem and prove it:

Theorem 3.2 (Independence Property of KCL Equations) *For any connected digraph $\mathscr{G}$ with n nodes, the KCL equations for* ***any*** $n-1$ *of these nodes form a set of* $n-1$ ***linearly independent equations***.

Proof We prove it by contradiction. Suppose that the first k of these $n-1$ equations are linearly dependent. More precisely, there are k real constants $\gamma_1, \gamma_2, \cdots, \gamma_k$ not all zero such that:

$$\sum_{j=1}^{k} \gamma_j f_j(i_1, i_2, \ldots, i_n) = 0 \quad \forall\, i_1, i_2, \ldots, i_n \tag{3.68}$$

Consider the two sets of nodes in $\mathscr{G}$, namely, the set which corresponds to the k equations and that of the remaining nodes. Since the digraph is connected, there is at least one branch which connects a node in the first set to a node in the second set. Clearly the current in that branch appears only once in the first k node equations, hence that current cannot cancel out in the sum of Eq. (3.68). This contradiction shows that for any $k \leq n-1$, it is not the case that a subset of k of the KCL equations is linearly independent. That is, these $n-1$ equations are linearly independent. □

If in $\mathbf{A}_a$, the incidence matrix of the connected digraph $\mathscr{G}$, we delete the row corresponding to the ground node, we obtain the **reduced incidence matrix A** which is of dimension $(n-1) \times b$. The corresponding **linearly independent** KCL equations read:

$$\mathbf{Ai} = \mathbf{0} \tag{3.69}$$

As a consequence of the independence property proved in Theorem 3.2, we may equivalently state that the matrix **A** is full rank.

[4] If a digraph is not connected, there are two simple solutions to the problem: one approach would be to treat each graph separately. In this case, each part would have its own incidence matrix and ground node. The other approach would be to use a hinged graph, as described in Sect. 3.2.1. We will use both approaches in this book.

3.2.3 Independent KVL Equations

Similarly, to write a set of linearly independent KVL equations in a systematic way is of crucial importance. Let us write the KVL equations for the four-node six-branch digraph of Fig. 3.14. Using associated reference directions and choosing node 4 as the ground node, we obtain:

$$\begin{aligned} v_1 &= e_1 - e_2 \\ v_2 &= e_1 - e_3 \\ v_3 &= -e_2 + e_3 \\ v_4 &= e_2 \\ v_5 &= e_3 \\ v_6 &= -e_1 \end{aligned} \tag{3.70}$$

or in matrix form:

$$\mathbf{v} = \mathbf{M}\mathbf{e} \tag{3.71}$$

where $\mathbf{v} = (v_1, v_2, \ldots, v_b)^T$ is the **branch voltage vector**, $\mathbf{e} = (e_1, e_2, \ldots, e_{n-1})^T$ is the **node-to-ground voltage vector**, and $\mathbf{M}$ is a $b \times (n-1)$ matrix. Thinking in terms of KVL, we see that for $k = 1, 2, \ldots, b$ and $i = 1, 2, \ldots, n-1$:

$$m_{ki} = \begin{cases} +1 & \text{if branch } k \textbf{ leaves} \text{ node } i \\ -1 & \text{if branch } k \textbf{ enters} \text{ node } i \\ 0 & \text{if branch } k \text{ does not touch node } i \end{cases} \tag{3.72}$$

Comparing Eq. (3.72) with (3.66) we conclude that:

$$\mathbf{M} = \mathbf{A}^T \tag{3.73}$$

and more usefully, KVL is expressed by the equation:

$$\mathbf{v} = \mathbf{A}^T\mathbf{e} \tag{3.74}$$

With a connected digraph $\mathscr{G}$, $\mathbf{A}$ has $n-1$ linearly independent rows (full row rank) and consequently $\mathbf{A}^T$ has $n-1$ linearly independent columns (full column rank).

Thus, to summarize, in order to obtain linearly independent KCL and KVL equations from a digraph representation of a circuit:

1. We choose current reference directions

2. We choose a ground node and define the reduced incidence matrix $\mathbf{A}$
3. We write KCL as $\mathbf{Ai} = \mathbf{0}$
4. We then use associated reference directions (or passive sign convention, recall Definition 1.2) to find that KVL reads $\mathbf{v} = \mathbf{A}^T\mathbf{e}$.

Note that we are assuming we use the same ground node for writing KCL and KVL.

3.2.4 A Proof of Tellegen's Theorem

We can now state and prove Tellegen's theorem.

Theorem 3.3 (Tellegen's Theorem) *Consider an arbitrary circuit. Let the associated digraph $\mathscr{G}$ have b branches. Using passive sign convention, let $\mathbf{v} = (v_1, v_2, \ldots, v_b)^T$ be **any** set of branch voltages satisfying KVL for $\mathscr{G}$ and let $\mathbf{i} = (i_1, i_2, \ldots, i_b)^T$ be **any** set of branch currents satisfying KCL for $\mathscr{G}$. Then:*

$$\sum_{k=1}^{b} v_k i_k = 0 \tag{3.75}$$

Equivalently:

$$\mathbf{v}^T\mathbf{i} = 0 \tag{3.76}$$

Proof For a connected digraph $\mathscr{G}$, choose a ground node; hence, a reduced matrix $\mathbf{A}$ is defined unambiguously. Since $\mathbf{i}$ satisfies KCL, we have:

$$\mathbf{Ai} = \mathbf{0} \tag{3.77}$$

Since $\mathbf{v}$ satisfies KVL and since we use associated reference directions, for some node-to-ground voltages $\mathbf{e}$, we have:

$$\mathbf{v} = \mathbf{A}^T\mathbf{e} \tag{3.78}$$

Using the two equations above, we successively obtain:

$$\begin{aligned}\mathbf{v}^T\mathbf{i} &= (\mathbf{A}^T\mathbf{e})^T\mathbf{i}\\ &= \mathbf{e}^T(\mathbf{A}^T)^T\mathbf{i}\\ &= \mathbf{e}^T(\mathbf{Ai})\\ &= 0\end{aligned} \tag{3.79}$$

□

Note how the proof essentially uses our discussion from Sect. 1.6.1. Now the idea from Sect. 1.6.1 should be very clear: **v** and **i** in the theorem need not bear any relation to each other: **v** must only satisfy KVL and **i** must only satisfy KCL (using associated reference directions). We will use Tellegen's theorem to prove some very general results for nonlinear resistive networks in Sect. 3.7.

3.2.5 *The Relation Between Kirchhoff's Laws and Tellegen's Theorem*

In circuit theory, there are two fundamental postulates: KCL and KVL. We have proved that KCL and KVL imply Tellegen's theorem. It is interesting to note that any one of Kirchhoff's laws together with Tellegen's theorem implies the other. More precisely, we have the following theorem:

Theorem 3.4 (Tellegen's Theorem and Kirchhoff's Laws)

1. If, for all $\mathbf{v}$ *satisfying KVL,* $\mathbf{v}^T\mathbf{i} = 0$*, then* $\mathbf{i}$ *satisfies KCL.*
2. If, for all $\mathbf{i}$ *satisfying KCL,* $\mathbf{v}^T\mathbf{i} = 0$*, then* $\mathbf{v}$ *satisfies KVL.*

Proof For 1: Since $\mathbf{v}$ satisfies KVL, we know that $\mathbf{v} = \mathbf{A}^T\mathbf{e}$ for all $\mathbf{e}$. But, given that Tellegen's theorem is also satisfied, we have:

$$\mathbf{v}^T\mathbf{i} = \mathbf{e}^T(\mathbf{A}\mathbf{i}) = 0 \tag{3.80}$$

Since $\mathbf{e}$ is an arbitrary node-to-ground voltage, the last equality implies $\mathbf{A}\mathbf{i} = \mathbf{0}$, that is, $\mathbf{i}$ satisfies KCL.
For 2: Let $\mathscr{L}$ be an arbitrary loop in the graph $\mathscr{G}$. Consider the $\mathbf{i}$ obtained by assigning zero current to all branches of $\mathscr{G}$ except for those of loop $\mathscr{L}$; depending on whether the reference direction of branch j in loop $\mathscr{L}$ agrees with that of loop $\mathscr{L}$, we assign i_j to be 1 A or -1 A. The resulting $\mathbf{i}$ satisfies KCL at all nodes of $\mathscr{G}$. Tellegen's theorem applied only to the branches in loop $\mathscr{L}$ gives:

$$\sum \pm v_j = 0 \tag{3.81}$$

Thus the algebraic sum of branch voltages around loop $\mathscr{L}$ is zero, i.e., KVL holds for loop $\mathscr{L}$. Since $\mathscr{L}$ is arbitrary, we have shown that KVL holds for all loops of $\mathscr{G}$. □

3.3 An Introduction to General Resistive Circuit Analysis

We can now embark on a more general and definitive study of resistive circuits. Our aim for the rest of this chapter is to develop general methods of analysis, for both linear and nonlinear resistive circuits, and to derive general properties of such

circuits. A common theme would be to start with (an example of) the linear case because equations for linear circuits can almost be derived by "inspection."

The term **resistive circuit** applies to all circuits containing **two-terminal resistors, multi-terminal resistors, multi-port resistors** and **independent voltage** and **current sources**. Common circuit elements such as ideal transformers, rotators, gyrators, controlled sources, transistors and opamps modeled by resistive circuits etc. **are all included**. To avoid clutter, all of these garden variety circuit elements will be lumped under the umbrella "multi-terminal and multi-port resistors". However, independent sources will always be singled out separately, because, as will be clear shortly, they play a fundamentally different role.

The importance of resistive circuits cannot be understated. The analysis of many general nonresistive circuits reduces to the analysis of the associated resistive circuit. Secondly, many computer algorithms for simulating dynamic circuits require at each step the analysis of a resistive circuit.

Recall that a **physical** circuit is an interconnection of **real** electric devices. For purposes of analysis and design, each electric device is replaced by a **device model** made of ideal circuit elements[5] (e.g., ideal diodes, batteries, linear and nonlinear resistors, controlled sources, etc.). The interconnection of these models gives the electric circuit. Since, the detailed but important study of **device modeling** is beyond the scope of this book, our point of departure for analysis would be a circuit. Whether the circuit arises from models of physical devices, or from the figment of one's imagination is irrelevant. In fact, it is often through the **introduction of hypothetical**, and **sometimes pathological circuits**, that one gains an **in-depth understanding of this subject**.

A few words concerning some general technical terms to be used throughout this book. A resistive circuit is said to be linear iff, after settings all independent sources to zero, it contains only **linear** (recall Exercise 1.9 for the superposition definition of linearity) two-terminal, multi-terminal, and/or multi-port resistors. A resistive circuit is said to be nonlinear iff it contains at least one nonlinear resistor besides independent sources.

Finally, we need to caution the reader to "not lose sight of the forest for its trees." In other words, one should not be so consumed by the systematic techniques that we lose total insight into the circuit at hand. After all, only a computer circuit simulation program "blindly" applies the techniques, without any insight.

[5]Of course, **all circuit elements are ideal**. We will, nevertheless, occasionally throw in the word "ideal" to remind the reader that "nonphysical" answers (e.g., the Schmitt trigger VTC) are quite possible and even expected. When they do occur, the culprit is not the theory, but the model. Such situations can only be rectified by returning to the drawing board to come up with a more detailed circuit model. Again, in the case of the Schmitt trigger, we will account for physical parasitics to explain the observed behavior.

3.4 Nodal Analysis for Resistive Circuits

The simplest method for analyzing a resistive circuit is to solve for its **node-to-ground** voltages. Once these node voltages have been calculated, we can solve for the branch voltages trivially via KVL: $\mathbf{v} = \mathbf{A}^T\mathbf{e}$. They in turn can be used to calculate the branch currents, provided all the elements in the circuit other than current sources are voltage-controlled. In this section, we will consider only the subclass of resistive circuits which are amenable to this common analysis method, henceforth called **node analysis**. The goal would be to determine the corresponding **node equation** for the circuit in question.

For simple resistive circuits, the node equation can be formulated almost by inspection, as illustrated in the following example.

Example 3.4.1 Determine the node equation for the circuit in Fig. 3.15.

Solution The circuit shown in Fig. 3.15 contains only linear (two-terminal) resistors and independent current sources. Choosing (arbitrarily) node 4 as the ground node, each branch current can be expressed in terms of at most two node voltages, simply by using Ohm's law since we have linear resistors. Thus:

$$\begin{aligned} i_1 &= G_1 v_1 = G_1 e_1 & i_4 &= G_4 v_4 = G_4(e_1 - e_2) \\ i_2 &= G_2 v_2 = G_2(e_2 - e_1) & i_5 &= G_5 v_5 = G_5(e_3 - e_2) \\ i_3 &= G_3 v_3 = G_3(-e_2) & i_6 &= G_6 v_6 = G_6 e_3 \end{aligned} \tag{3.82}$$

It follows from Sect. 3.2.2 that we can write three linearly independent KCL equations in terms of e_1, e_2, and e_3, namely:

$$\begin{aligned} &\text{Node 1}: && G_1 e_1 - G_2(e_2 - e_1) + G_4(e_1 - e_2) = i_{s1}(t) \\ &\text{Node 2}: && G_2(e_2 - e_1) - G_3(-e_2) - G_4(e_1 - e_2) - G_5(e_3 - e_2) = -i_{s3}(t) \\ &\text{Node 3}: && G_5(e_3 - e_2) + G_6 e_3 = i_{s3}(t) - i_{s2}(t) \end{aligned} \tag{3.83}$$

Recasting in matrix form:

$$\begin{bmatrix} (G_1 + G_2 + G_4) & -(G_2 + G_4) & 0 \\ -(G_2 + G_4) & (G_2 + G_3 + G_4 + G_5) & -G_5 \\ 0 & -G_5 & (G_5 + G_6) \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = \begin{bmatrix} i_{s1}(t) \\ -i_{s2}(t) \\ i_{s3}(t) - i_{s2}(t) \end{bmatrix} \tag{3.84}$$

(continued)

Example 3.4.1 (continued)
In other words, we have:

$$\mathbf{Y}_n \mathbf{e} = \mathbf{i}_s(t) \tag{3.85}$$

henceforth called the **node equation**. $\mathbf{Y}_n$ is a square matrix called the **node-admittance matrix** and $\mathbf{i}_s(t)$ is called the equivalent source vector.

We will shortly show that a large class of linear resistive circuits is described by a form like Eq. (3.85). But first, an inspection of Fig. 3.15 and Eq. (3.84) reveals the following properties.

We will prove the properties in Table 3.1, once we obtain the node-admittance matrix in terms of the reduced incidence matrix **A**, which we will do so below.

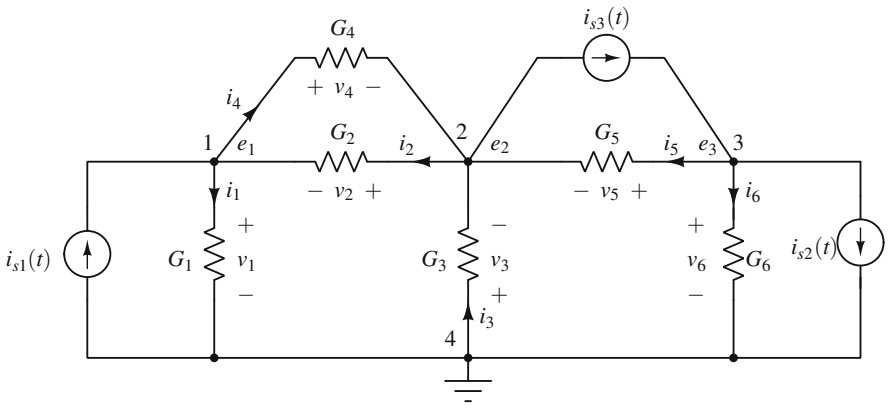


Fig. 3.15 Circuit for example 3.4.1. Here, G_j denotes the conductance in S for the jth resistor

Table 3.1 Properties of Eq. (3.85)

For any circuit made of linear two-terminal resistors and independent sources
1. The kth diagonal element of $\mathbf{Y}_n$ is equal to the sum of all conductances attached to node k
2. The jkth off-diagonal element of $\mathbf{Y}_n$ is equal to the **negative** of the sum of all conductances between node j and node k
3. The matrix $\mathbf{Y}_n$ is **symmetric**: $\mathbf{Y}_n = \mathbf{Y}_n^T$
4. The kth element of $i_s(t)$ is equal to the algebraic sum of currents of all independent current sources entering node k

3.4.1 Formulation in Terms of Reduced Incidence Matrix

Let $\mathcal{N}$ denote any connected linear resistive circuit containing only two-terminal, multi-terminal and/or multi-port linear voltage-controlled resistors, and independent current sources. For example, $\mathcal{N}$ may contain gyrators because they are defined by a voltage-controlled linear equation, Eq. (2.167). On the other hand, $\mathcal{N}$ may not contain ideal transformers because it is not voltage-controlled, that is, it is impossible to solve for i_1, i_2 from the defining Eq. (2.37) in terms of only v_1, v_2. Controlled sources other than VCCS are also disallowed for the same reason.[6] Note that although independent voltage sources are not allowed in our present formulation, they can be included later through equivalent circuit transformations.

If the terminals and/or ports of all circuit elements which are not independent current sources are labeled consecutively, and if $\mathbf{v} = (v_1, v_2, \ldots, v_b)^T$ and $\mathbf{i} = (i_1, i_2, \ldots, i_n)^T$ denote the respective branch voltage and branch current vectors, then $\mathcal{N}$ is precisely the class where $\mathbf{i}$ can be described as a linear function of $\mathbf{v}$; namely,

$$\begin{bmatrix} i_1 \\ i_2 \\ . \\ . \\ . \\ i_b \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1b} \\ y_{21} & y_{22} & \cdots & y_{2b} \\ . & . & \cdots & . \\ . & . & \cdots & . \\ . & . & \cdots & . \\ y_{b1} & y_{b2} & \cdots & y_{bb} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ . \\ . \\ . \\ v_b \end{bmatrix} \tag{3.86}$$

or simply,

$$\mathbf{i} = \mathbf{Y}_b \mathbf{v} \tag{3.87}$$

Equation (3.87) is the **branch equation**, where $\mathbf{Y}_b$ is called the **branch admittance matrix**. In general, $\mathbf{Y}_b$ is a $b \times b$ nonsymmetric and nondiagonal real matrix, where b is the number of branches, excluding the independent current sources, in the associated digraph.

We have deliberately left out the independent current sources because they can be easily accounted for separately. In particular, the contribution of current sources can be represented by a single vector:

$$\mathbf{i}_s(t) = \left[i_{s1}(t)\ i_{s2}(t)\ \cdots\ i_{s(n-1)}(t) \right]^T \tag{3.88}$$

where $\imath_{sk}(t)$ denotes the algebraic sum of currents of all independent current sources entering node k, $k = 1, 2, \ldots, n-1$ and n denotes the number of nodes in the

[6] We will however be able to use tableau analysis from Sect. 3.5 to analyze circuits with any resistive element.

connected circuit $\mathcal{N}$. To avoid violating KCL, it is necessary to assume that no cut sets are made exclusively of independent current sources.

Equivalently, the digraph associated with the reduced circuit obtained by open-circuiting all independent current sources is connected. Let $\mathbf{A}$ denote the reduced incidence matrix of this connected digraph. It follows that:

$$\mathbf{A}\mathbf{i} = \mathbf{i}_s(t) \tag{3.89}$$

constitutes a system of $n-1$ linearly independent KCL equations. It is important to note that the KCL Eq. (3.89) differs from the usual form ($\mathbf{A}\mathbf{i} = \mathbf{0}$) because here, the reduced incidence matrix $\mathbf{A}$ pertains to the reduced digraph obtained by open-circuiting all independent current sources from the digraph associated with the circuit.

Substituting the branch Eq. (3.87) in place of $\mathbf{i}$ in Eq. (3.89), we obtain:

$$\mathbf{A}\mathbf{Y}_b\mathbf{v} = \mathbf{i}_s(t) \tag{3.90}$$

Rewriting the branch voltage $\mathbf{v}$ in terms of the node voltage $\mathbf{e}$ via KVL (Eq. (3.74)), we get:

$$(\mathbf{A}\mathbf{Y}_b\mathbf{A}^T)\mathbf{e} = \mathbf{i}_s(t) \tag{3.91}$$

Comparing Eqs. (3.85) and (3.91), we have derived the **node-admittance matrix**:

$$\mathbf{Y}_n = \mathbf{A}\mathbf{Y}_b\mathbf{A}^T \tag{3.92}$$

We have hence derived the following general result, our first systematic circuit analysis technique:

Nodal Analysis for Linear Resistive Circuits

For any connected circuit containing two-terminal, multi-terminal, and/or multi-port linear voltage-controlled resistors and independent current sources which do not form cut sets, the node equation is given explicitly by:

$$\mathbf{Y}_n(t)\mathbf{e}(t) = \mathbf{i}_s(t) \tag{3.93}$$

$\mathbf{Y}_n(t) \triangleq \mathbf{A}\mathbf{Y}_b(t)\mathbf{A}^T$, $\mathbf{Y}_n(t)$ is the node-admittance matrix, $\mathbf{i}_s(t)$ denotes the equivalent source vector whose kth element $i_{sk}(t)$ is equal to the algebraic sum of the current of all independent current sources **entering** node k, and $\mathbf{A}$ denotes the reduced incidence matrix of the digraph associated with the **reduced** circuit obtained by deleting all **independent** current sources.

The astute reader would have noticed that we have defined Eq. (3.93) for time-varying elements as well. This is fine because if branch k is a time-varying resistor described by $i_k(t) = G_k(t)v_k(t)$, then $y_{kk} = G_k(t)$.

Note that the dimension of A and $Y_b(t)$ are $(n-1) \times b$ and $b \times b$, respectively, where n is the number of nodes in the circuit, and b is the number of branches in the digraph associated with the reduced circuit. Consequently, the dimensions of the node-admittance matrix $\mathbf{Y}_n(t)$ is $(n-1) \times (n-1)$.

In other words, the node Eq. (3.93) always contains $n-1$ linear equations in terms of $n-1$ node voltages $e_1, e_2, \ldots, e_{n-1}$.

To find the solution of the circuit, we simply solve Eq. (3.93) at each instant of time t by any convenient method, say gaussian elimination. If n is very large, say $n > 100$, and if the matrix $\mathbf{Y}_n(t)$ contains only a small percentage of nonzero entries as is typical in practice ($\mathbf{Y}_n(t)$ is said to be sparse), there exist specially efficient computer algorithms for solving the equation. If the circuit is time-invariant and contains only DC current sources, then $\mathbf{Y}_n(t)$ is a constant matrix and $\mathbf{i}_s(t)$ is a constant vector. In this case, Eq. (3.93) need to be solved only once.

Unlike several other methods of analysis (e.g., tableau analysis, modified nodal analysis) to be studied later, the number of equations to be solved in node analysis does not depend on the number of circuit elements. Hence for a 100-element circuit containing only 10 nodes, we only need to solve 9 equations.

Once $\mathbf{e}(t)$ has been found, the branch voltages can be calculated by substitution into the time-varying case for Eq. (3.74): $\mathbf{v}(t) = \mathbf{A}^T\mathbf{e}(t)$—and the branch currents can be calculated by substitution into the time-varying case for branch Eq. (3.87): $\mathbf{i}(t) = \mathbf{Y}_b(t)\mathbf{v}(t)$.

Example 3.4.2 Prove the properties in Table 3.1.

Solution Let us begin by expanding Eq. (3.92), for a circuit with three nodes and three resistors:

$$\begin{aligned}
\mathbf{Y_n} &= \mathbf{A}\mathbf{Y}_b\mathbf{A}^T \\
&= \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \end{bmatrix} \begin{bmatrix} G_1 & 0 & 0 \\ 0 & G_2 & 0 \\ 0 & 0 & G_3 \end{bmatrix} \begin{bmatrix} a_{11} & a_{21} \\ a_{12} & a_{22} \\ a_{13} & a_{23} \end{bmatrix} \\
&= \begin{bmatrix} (a_{11}a_{11}G_1 + a_{12}a_{12}G_2 + a_{13}a_{13}G_3) & (a_{11}a_{21}G_1 + a_{12}a_{22}G_2 + a_{13}a_{23}G_3) \\ (a_{21}a_{11}G_1 + a_{22}a_{12}G_2 + a_{23}a_{13}G_3) & (a_{21}a_{21}G_1 + a_{22}a_{22}G_2 + a_{23}a_{23}G_3) \end{bmatrix}
\end{aligned} \tag{3.94}$$

(continued)

Example 3.4.2 (continued)
If we denote the jkth element of $\mathbf{Y}_n$ by $(\mathbf{Y}_n)_{jk}$ and the kth diagonal of $\mathbf{Y}_b$ by G_k, then in general, we have:

$$(\mathbf{Y}_n)_{jk} = \sum_{l=1}^{b} a_{jk} a_{kl} G_l \tag{3.95}$$

provided that $\mathbf{Y}_b$ is a diagonal matrix, i.e., provided the circuit contains only two-terminal resistors and independent current sources.

If we let $j = k$ in Eq. (3.95), we find the kth diagonal element is given by:

$$\begin{aligned}(\mathbf{Y}_n)_{kk} &= \sum_{l=1}^{b} a_{kl}^2 G_l \\ &= \sum_{\beta_k} G_l \end{aligned} \tag{3.96}$$

where $\sum_{\beta_k}$ is defined as the sum over all branches connected to node k. This is true because of the observation that $a_{kl} = 1, -1$ or 0, and $a_{kl} \neq 0$ if and only if branch G_l is connected to node k. Hence we have proved property 1 of Table 3.1 holds for any circuit described by a diagonal branch admittance matrix $\mathbf{Y}_b$.

Observe next that if $a_{jl} \neq 0$, i.e., G_l is connected to node j, then

$$a_{kl} = -a_{jl} \tag{3.97}$$

if G_l is connected between nodes j and k, and

$$a_{kl} = 0 \tag{3.98}$$

if G_l is connected between node j and the ground node. It follows from Eqs. (3.95) and (3.98) that each off-diagonal element ($j \neq k$) of $\mathbf{Y_n}$ can be simplified as follows:

$$(\mathbf{Y}_n) = -\sum_{\beta_{jk}} G_l \tag{3.99}$$

(continued)

Example 3.4.2 (continued)

where $\sum_{\beta_{jk}}$ is defined to be the sum over all branches connected between nodes j and k. Hence we have proved property 2 of Table 3.1. Moreover, Eq. (3.99) implies that:

$$(\mathbf{Y}_n)_{jk} = (\mathbf{Y}_n)_{kj} \quad \text{or} \quad \mathbf{Y}_n = \mathbf{Y}_n^T \tag{3.100}$$

This proves property 3 of Table 3.1. Note that this symmetry property has nothing to do with whether the circuit is symmetrical or not. It is actually a consequence of an important circuit-theoretic property called **reciprocity** that will be discussed in Sect. 4.6.1.

The last property of Table 3.1 follows by definition and is therefore true regardless of whether $\mathbf{Y}_n$ is diagonal or not.

3.4.2 *Existence and Uniqueness of Solutions*

When we talked about various methods for solving the linear node Eq. (3.93) in the previous section, we implicitly assumed that Eq. (3.93) had a unique solution for any time t. To show that this assumption is not always satisfied even by simple circuits, consider the circuit shown in Fig. 3.16a.

Using the properties from Table 3.1, we obtain the following node equation by inspection (note the resistances are given in ohms):

$$\begin{bmatrix} 1 & -2 \\ -2 & 4 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} i_{s1}(t) \\ i_{s2}(t) \end{bmatrix} \tag{3.101}$$

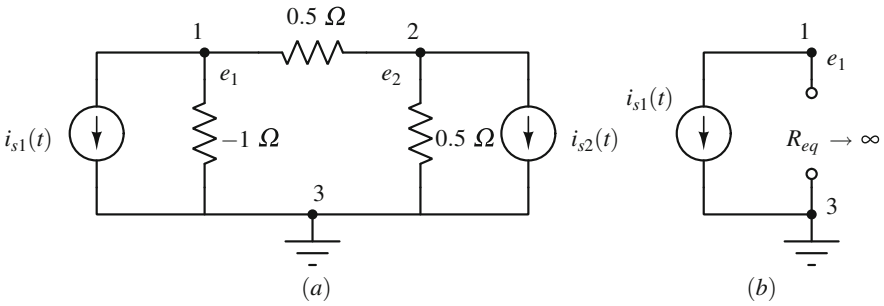


Fig. 3.16 A circuit containing a negative resistance

Since the determinant of $\mathbf{Y}_n$ is zero, Eq. (3.101) either has no solution or has infinitely many solutions. The latter occurs if and only if, $\forall\, t, i_{s1}(t) = -\frac{1}{2} i_{s1}(t)$.

To give a circuit interpretation of the above conclusion, let us assume for simplicity that $i_{s2}(t) = 0$ for all t so that the current source on the right-hand side can be deleted without affecting the circuit's solution. The resulting circuit can be further simplified to that shown in Fig. 3.16b, where the three resistors in Fig. 3.16a are replaced by an equivalent resistor R_{eq}. Since the current source $i_s(t)$ flows into an open circuit, it follows that the circuit does not have a solution if $i_{s1}(t) \neq 0$. On the other hand, if $i_{s1}(t) = 0$ for all t, then the circuit is satisfied by any node voltage e_1, and hence it admits an infinite number of solutions.

The following result gives a sufficient (but not necessary) condition for a circuit to have a unique solution.

Existence and Uniqueness Condition
Any resistive circuit containing only two-terminal linear positive conductances and independent current sources which do not form cut sets has a unique solution.

Proof Note that linear positive conductances or strictly passive resistors will be defined in Sect. 3.7. The above hypotheses guarantee that the node equation given by Eq. (3.93) is well-defined. Moreover, $\mathbf{Y}_b$ is a positive-definite diagonal matrix (since for all j, $G_j > 0$); i.e., $\mathbf{v}^T \mathbf{Y}_b \mathbf{v} > 0, \forall\, \mathbf{v} \neq \mathbf{0}$.

Now, for any node voltage vector $\mathbf{e} \neq \mathbf{0}$:

$$\begin{aligned} \mathbf{e}^T \mathbf{Y_n} \mathbf{e} &= \mathbf{e}^T (\mathbf{A} \mathbf{Y}_b \mathbf{A}^T) \mathbf{e} \\ &= (\mathbf{A}^T \mathbf{e})^T \mathbf{Y}_b (\mathbf{A}^T \mathbf{e}) \\ &= \mathbf{v}^T \mathbf{Y}_b \mathbf{v} \\ &> 0 \end{aligned} \tag{3.102}$$

Hence $\mathbf{Y}_n$ is a positive-definite matrix and thus is full rank. Therefore Eq. (3.93) has a unique solution given by $\mathbf{e} = \mathbf{Y}_n^{-1} \mathbf{i}_s(t)$. □

3.4.3 *Node Equation Formulation: Nonlinear Resistive Circuits*

When the circuit contains one more nonlinear resistors, the procedure for writing the node equation discussed in Sect. 3.4 in terms of the node voltage vector $\mathbf{e}$ still holds provided all nonlinear resistors are voltage-controlled. For example, consider the two linear resistors G_2 and G_5 in Fig. 3.15 replaced by a *pn*-junction diode

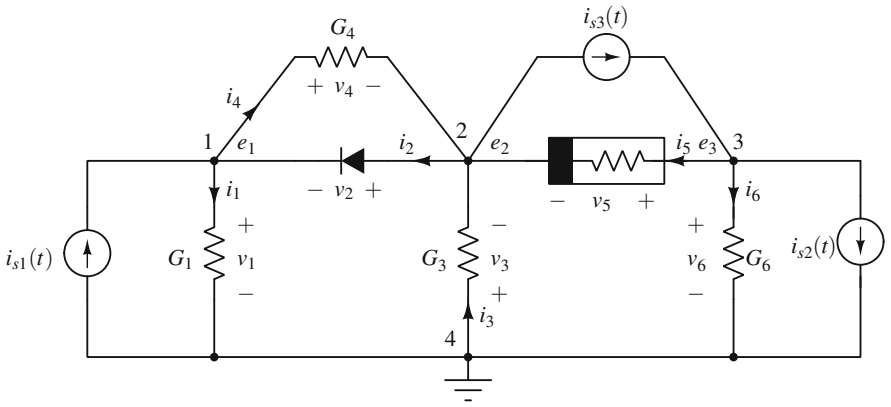


Fig. 3.17 A nonlinear circuit

described by $i_2 = I_s\left(e^{(v_2/V_T)} - 1\right)$ and an $\mathcal{N}_R$ described by $i_5 = v_5^3$ as shown in Fig. 3.17.

Our first step as usual is to express the branch currents of the resistors in terms of the node voltages e_1, e_2, and e_3:

$$\begin{aligned} i_1 &= G_1 v_1 = G_1 e_1 & i_4 &= G_4 v_4 = G_4(e_1 - e_2) \\ i_2 &= I_s\left(e^{(v_2/V_T)} - 1\right) = I_s\left(e^{\frac{e_2 - e_1}{V_T}} - 1\right) & i_5 &= v_5^3 = (e_3 - e_2)^3 \\ i_3 &= G_3 v_3 = G_3(-e_2) & i_6 &= G_6 v_6 = G_6 e_3 \end{aligned} \tag{3.103}$$

Note that this step is possible as long as the nonlinear resistors are voltage-controlled, i.e., the branch currents are functions of branch voltages.

Our next step is to apply KCL at each node (excluding the ground node):

$$\begin{aligned} &\text{Node 1}: \quad G_1 e_1 - I_s\left(e^{\frac{e_2 - e_1}{V_T}} - 1\right) + G_4(e_1 - e_2) = i_{s1}(t) \\ &\text{Node 2}: \quad I_s\left(e^{\frac{e_2 - e_1}{V_T}} - 1\right) - G_3(-e_2) - G_4(e_1 - e_2) - (e_3 - e_2)^3 = -i_{s3}(t) \\ &\text{Node 3}: \quad (e_3 - e_2)^3 + G_6 e_3 = i_{s3}(t) - i_{s2}(t) \end{aligned} \tag{3.104}$$

The equations above constitute the node equation of the circuit in Fig. 3.17. But since these equations are nonlinear, they cannot be described by a node-admittance matrix.

Consider now the general case where the circuit may contain two-terminal, multi-terminal, and/or multi-port nonlinear voltage-controlled resistors, in addition to independent current sources. In this case, the branch equations now assume the

following form:

$$\begin{aligned} i_1 &= g_1(v_1, v_2, \ldots, v_b) \\ i_2 &= g_2(v_1, v_2, \ldots, v_b) \\ &\vdots \\ i_b &= g_b(v_1, v_2, \ldots, v_b) \end{aligned} \tag{3.105}$$

In vector notation we have:

$$\mathbf{i} = \mathbf{g}(\mathbf{v}) \tag{3.106}$$

called the **nonlinear branch equation**. Since independent current sources do not form cut sets (by assumption), Eq. (3.89) remains valid. Substituting Eq. (3.106) for **i** in Eq. (3.89), we get:

$$\mathbf{Ag}(\mathbf{v}) = \mathbf{i_s}(t) \tag{3.107}$$

Substituting next Eq. (3.74) for **v**, we get the **nonlinear node equation**:

$$\mathbf{Ag}(\mathbf{A}^T\mathbf{e}) = \mathbf{i}_s(t) \tag{3.108}$$

For each solution of **e** in Eq. (3.108), we can calculate the corresponding branch voltage vector **v** by direct substitution into Eq. (3.74), namely, $\mathbf{v} = \mathbf{A}^T\mathbf{e}$. This in turn can be used to calculate the branch current vector **i** by direct substitution into Eq. (3.106). Hence the basic problem is to solve the nonlinear node Eq. (3.108). The rest is trivial. In general, nonlinear equations do not have closed form solutions. Consequently, they must be solved by numerical techniques, that are beyond the scope of this book. The most widely used method is the Newton-Raphson algorithm, the reader is referred to excellent sources such as [3] for details.

3.5 Tableau Analysis for Resistive Circuits

The only, albeit major, shortcoming of node analysis is that it disallows many standard circuit elements from the class of allowable circuits, e.g., the voltage source, ideal transformer, ideal op amp, CCCS, CCVS, VCVS, current-controlled nonlinear resistor, etc. In this section, we overcome this issue by presenting a completely general analysis method—one that works for all resistive circuits. Conceptually, this method is simpler than node analysis. It consists of writing out the complete list of linearly independent KCL equations, linearly independent KVL equations, and the branch equations. For obvious reasons, this list of equations is called **tableau equations** [2].

Since no variables are eliminated[7] in listing the tableau equations, all three vectors $\mathbf{e}$, $\mathbf{v}$, and $\mathbf{i}$ are present as variables. Since we must have as many tableau equations as there are variables, it is clear that the price we pay for the increased generality is that tableau analysis involves many more equations than node analysis does. In our era of computer-aided circuit analysis, however, this objection turns out to be a blessing in disguise because the matrix associated with tableau analysis is often extremely sparse, thereby allowing highly efficient numerical algorithms to be used.

The significance of tableau analysis actually transcends the above more mundane numerical considerations. As the reader will gather while reading this and other advanced textbooks on nonlinear circuits, tableau analysis is a powerful analytic tool which allows us to derive many profound results with almost no pain at all—at least compared to other approaches.

To write the tableau equation for any linear resistive circuit, we simply use the following algorithm[8]:

1. Draw the digraph of the circuit and hinge it if necessary so that the resulting digraph is connected. Pick an arbitrary ground node and formulate the reduced incidence matrix $\mathbf{A}$.
2. Write a complete set of linearly independent KCL equations:

$$\mathbf{A}\mathbf{i}(t) = \mathbf{0} \tag{3.109}$$

   Note that unlike Eq. (3.89), tableau analysis deals with the original digraph where each independent current source is represented by a branch.
3. Write a complete set of linearly independent KVL equations:

$$\mathbf{v}(t) - \mathbf{A}^T\mathbf{e}(t) = \mathbf{0} \tag{3.110}$$

4. Write the branch equations. Since the circuit is linear, these equations can always be recast into the form:

$$\mathbf{M}(t)\mathbf{v}(t) + \mathbf{N}(t)\mathbf{i}(t) = \mathbf{u}_s(t) \tag{3.111}$$

Together Eqs. (3.109)–(3.111) constitute the tableau equations. If the digraph has n nodes and b branches, Eqs. (3.109)–(3.111) will contain $n-1$, b and b equations, respectively. Since the vectors e, v, and i also contain $n-1$, b and b variables, respectively, the tableau equation for a linear resistive circuit always consists of $(n-1)+2b$ linear equations in $(n-1)+2b$ variables.

[7] Recall both $\mathbf{v}$ and $\mathbf{i}$ must be eliminated in node analysis, leaving $\mathbf{e}$ as the only variable.

[8] The reader may wish to scan Example 3.5.1 after each step in order to get familiarized first with the notations used in writing the tableau equation.

Example 3.5.1 Write the tableau equations for the linear circuit in Fig. 3.18.

Solution The circuit only contains three elements: a voltage source, an ideal transformer, and a time-varying resistor. The first two elements are not allowed in nodal analysis because they are not voltage-controlled. The third element, which would normally be acceptable, is also disallowed here because its conductance $G(t) = 1/(R_0 \sin t) \rightarrow \infty$ at $t = 0, 2\pi, 4, \pi, \cdots$ and is therefore not defined for all t.

Applying the preceding recipe, we hinge nodes 3 and 4 and draw the connected digraph shown in Fig. 3.18b. Choosing the hinged node as ground, the tableau equations are formulated below.

$$\text{KCL}: \quad \mathbf{AI} = \mathbf{0} \Leftrightarrow \begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.112}$$

$$\text{KVL}: \quad \mathbf{v} - \mathbf{A}^T \mathbf{e} = \mathbf{0} \Leftrightarrow \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.113}$$

$$\text{Branch Equations}: \quad \left.\begin{array}{c} n_2 v_1 - n_1 v_2 = 0 \\ n_1 i_1 + n_2 i_2 = 0 \\ v_3 - R(t) i_3 = 0 \\ v_4 = E \cos \omega t \end{array}\right\} \Leftrightarrow \begin{bmatrix} n_2 & -n_1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix}$$

$$+ \begin{bmatrix} 0 & 0 & 0 & 0 \\ n_1 & n_2 & 0 & 0 \\ 0 & 0 & -R(t) & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ E \cos \omega t \end{bmatrix} \tag{3.114}$$

$n = 3, b = 4$ for the digraph in Fig. 3.18b. Consequently, we expect the tableau equation to contain $(n-1) + 2b = 10$ equations involving 10 variables, namely $e_1, e_2, v_1, v_2, v_3, v_4, i_1, i_2, i_3, i_4$. An inspection of Eqs. (3.112), (3.113), and (3.114) shows that indeed we have 10 equations involving these 10 variables.

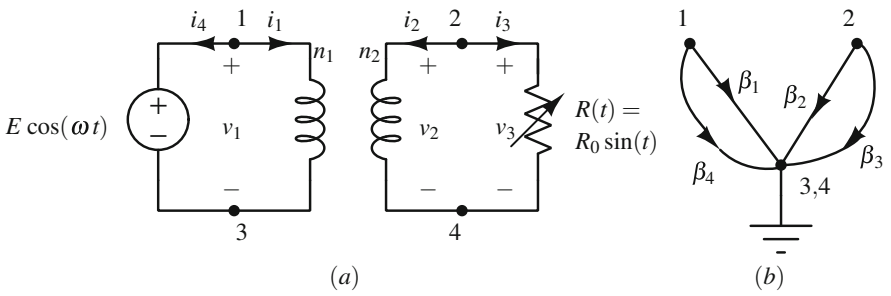


Fig. 3.18 All three elements in this circuit are disallowed in node analysis

Example 3.5.1 simply illustrated how to apply the tableau analysis algorithm. Had one encountered the circuit in Fig. 3.18a in practice, assuming enough experience in circuit analysis, one can quickly write the necessary equations "on the back of an envelope." The point we wish to emphasize again is that one should use insight, along with technique.

The vector $\mathbf{u}_s(t)$ on the right-hand side of Eq. (3.111) does not depend on any variable e_j, v_j or i_j and is therefore due to only independent voltage and current sources in the circuit. Consequently, element k of $\mathbf{u}_s(t)$ will be zero whenever branch k is not an independent source. Note that controlled source coefficients always appear in the matrices $\mathbf{M}(t)$ and/or $\mathbf{N}(t)$, never in $\mathbf{u}_s(t)$.

An inspection of Eq. (3.114) reveals that each row k of $\mathbf{M}(t)$ and $\mathbf{N}(t)$ contains coefficients or time functions which define uniquely the linear relation between v_k and i_k of branch k in the digraph, assuming branch k corresponds to a resistor. If branch k happens to be an independent source, then the kth diagonal element is equal to one in $\mathbf{M}(t)$ (for a voltage source) or $\mathbf{N}(t)$ (for a current source), while all other elements in row k are zeros. In this case, the kth element of $\mathbf{u}_s(t)$ will contain either a constant (for a DC source) or a time function which specifies uniquely this independent source. On the other hand, if branch k is not an independent source, then the k element of $\mathbf{u}_s(t)$ is always zero. It follows from the above interpretation that both $\mathbf{M}(t)$ and $\mathbf{N}(t)$ are $b \times b$ matrices and $\mathbf{u}_s(t)$ is a $b \times 1$ vector, where b is the number of branches in the digraph.

Finally note that we can state that a resistive circuit is linear iff its branch equations can be written in the form stipulated in Eq. (3.111), and it is time-invariant iff both $\mathbf{M}(t)$ and $\mathbf{N}(t)$ are constant real matrices.

In the general case, it is more illuminating to write Eqs. (3.109)–(3.111) as a single matrix equation, the **linear tableau equation**, shown in Eq. (3.115).

$$\underbrace{\begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{A} \\ -\mathbf{A}^T & \mathbf{I} & \mathbf{0} \\ \mathbf{0} & \mathbf{M}(t) & \mathbf{N}(t) \end{bmatrix}}_{\mathbf{T}(t)} \underbrace{\begin{bmatrix} \mathbf{e}(t) \\ \mathbf{v}(t) \\ \mathbf{i}(t) \end{bmatrix}}_{\mathbf{w}(t)} = \underbrace{\begin{bmatrix} \mathbf{0} \\ \mathbf{0} \\ \mathbf{u}_s(t) \end{bmatrix}}_{\mathbf{u}(t)} \tag{3.115}$$

It is natural to call $\mathbf{T}(t)$ the **tableau matrix** associated with the linear resistive circuit. If the circuit is time-invariant, $\mathbf{T}(t) = \mathbf{T}$, a constant real matrix.

Every linear resistive circuit is associated with a **unique** $[(n-1)+2b] \times [(n-1)+2b]$ square tableau matrix $\mathbf{T}(t)$, and a **unique** $[(n-1)+2b] \times 1$ vector $\mathbf{u}(t)$.[9] Note the significance of the tableau matrix is the fact that, if and only if, $\det[\mathbf{T}(t_0)] \neq 0$ at any time t_0, a **unique** solution to the linear circuit exists in the form of $\mathbf{w}(t_0) = \mathbf{T}^{-1}(t_0)\mathbf{u}(t_0)$.

3.5.1 *Tableau Equation Formulation: Nonlinear Resistive Circuits*

Exactly the same principle is used to formulate the tableau equation for **nonlinear** resistive circuits: Simply list the linearly independent KCL and KVL equations, and the branch equations, which are now nonlinear. Hence, the first three steps of the algorithm at the beginning of Sect. 3.5 remain unchanged. Only step 4 needs to be modified because Eq. (3.111) is valid only for linear resistive circuits. Example 3.19 illustrates and suggests the modified form of Eq. (3.111).

Example 3.5.2 Write the tableau equations for the nonlinear circuit in Fig. 3.19. The *npn* transistor is modeled by the following nonlinear Ebers-Moll equation (see Eqs. (2.40) and (2.41) from Chap. 2):

$$i_1 = -I_{ES}\left(e^{\frac{-v_1}{V_T}} - 1\right) + \alpha_R I_{CS}\left(e^{\frac{-v_2}{V_T}} - 1\right) \tag{3.116}$$

$$i_2 = \alpha_F I_{ES}\left(e^{\frac{-v_1}{V_T}} - 1\right) - I_{CS}\left(e^{\frac{-v_2}{V_T}} - 1\right) \tag{3.117}$$

(continued)

[9] The "uniqueness" is of course relative to a particular choice of element and node numbers.

Example 3.5.2 (continued)
Solution Since the digraph for this circuit is identical to that shown in Fig. 3.18b, the same KCL Eq. (3.112) and KVL Eq. (3.113) also apply for this circuit. However, instead of Eq. (3.114), we have the following branch equations:

$$\begin{aligned} h_1(v_1, v_2, i_1) &\triangleq i_1 + I_{ES}\left(e^{\frac{-v_1}{V_T}} - 1\right) - \alpha_R I_{CS}\left(e^{\frac{-v_2}{V_T}} - 1\right) = 0 \\ h_2(v_1, v_2, i_1) &\triangleq i_2 - \alpha_F I_{ES}\left(e^{\frac{-v_1}{V_T}} - 1\right) + I_{CS}\left(e^{\frac{-v_2}{V_T}} - 1\right) = 0 \\ h_3(v_3, i_3, t) &\triangleq v_3 - R(t) i_3 = 0 \\ h_4(v_4, t) &\triangleq v_4 - E\cos\omega t = 0 \end{aligned} \tag{3.118}$$

Note that $h_1(\cdot, \cdot, \cdot)$ and $h_2(\cdot, \cdot, \cdot)$ are nonlinear functions of (v_1, v_2, i_1) and (v_1, v_2, i_2), respectively; $h_3(\cdot, \cdot, \cdot)$ is a linear function of v_3 and i_3 but a nonlinear function of t; and $h_4(\cdot, \cdot)$ is a function of only v_4 and t. Even for this simple circuit, we see that there is really no simple form analogous to Eq. (3.114). To avoid keeping track of which variables are present in each function, we will simply denote Eq. (3.118) as follows:

$$\begin{aligned} h_1(v_1, v_2, i_1, i_2, t) &= 0 \\ h_2(v_1, v_2, i_1, i_2, t) &= 0 \\ h_3(v_1, v_2, i_1, i_2, t) &= 0 \\ h_4(v_1, v_2, i_1, i_2, t) &= 0 \end{aligned} \tag{3.119}$$

or in vector form, we simply write:

$$\mathbf{h}(\mathbf{v}, \mathbf{i}, t) = 0 \tag{3.120}$$

It is understood that some variables may not be present in each component equation.

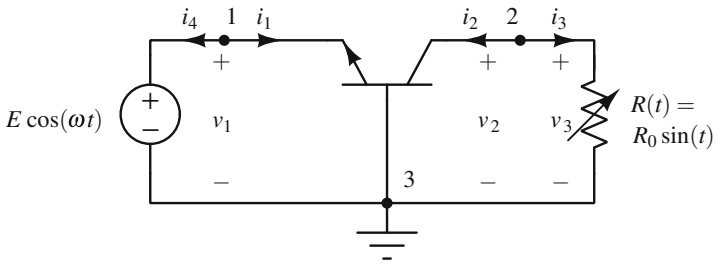


Fig. 3.19 A nonlinear resistive circuit

It follows from Example 3.5.2 that **every** nonlinear resistive circuit is described by a unique system of $(n-1)+2b$ nonlinear algebraic equations in $(n-1)+2b$ variables, called the **nonlinear tableau equation**:

$$\begin{aligned} \mathbf{A}\mathbf{i}(t) &= \mathbf{0} \\ \mathbf{v}(t) - \mathbf{A}^T \mathbf{e}(t) &= \mathbf{0} \\ \mathbf{h}(\mathbf{v}(t), \mathbf{i}(t), t) &= \mathbf{0} \end{aligned} \tag{3.121}$$

We usually resort to numerical methods to solve Eq. (3.121), which is beyond the scope of this book.

3.6 General Properties of Linear Resistive Circuits

In this section, we state and prove two general theorems for linear time-invariant resistive circuits,[10] namely the **superposition theorem** and the **Thévenin-Norton theorem**. Intelligent use of these theorems often results in a dramatic simplification of an otherwise much more difficult problem.

Both these theorems are valid if and only if the associated circuit is **uniquely solvable**, equivalently, if and only if the associated tableau matrix $\mathbf{T}$ is nonsingular. Although these theorems are stated only for time-invariant circuits for simplicity, both theorems are valid also for time-varying circuits by simply allowing all parameters and coefficients to vary with time.

[10] Recall that a **linear** resistive circuit may contain, in addition to two-terminal resistors and independent sources, any multi-terminal or multi-port linear resistors (for example, ideal transformers, gyrators, and all four types of linear-dependent sources).

3.6.1 Superposition Theorem

Theorem 3.5 (Superposition Theorem for Linear Time-Invariant Circuits) *Let $\mathcal{N}$ be any linear time-invariant uniquely solvable resistive circuit driven by α independent voltage sources $v_{s1}(t), v_{s2}(t), \ldots, v_{s\alpha}(t)$ and β independent current sources $i_{s1}(t), i_{s2}(t), \ldots, i_{s\beta}(t)$.*

Then any node voltage $e_j(t)$, any branch voltage $v_j(t)$, or any branch current $i_j(t)$ is given by an expression of the form

$$H_1 v_{s1}(t) + \cdots + H_\alpha v_{s\alpha}(t) + K_1 i_{s1}(t) + \cdots + K_\beta i_{s\beta}(t) \tag{3.122}$$

*where the coefficients H_k, $k = 1, 2, \ldots, \alpha$ and K_k, $k = 1, 2, \ldots, \beta$ are constants which depend only on the circuit parameters of $\mathcal{N}$ and the choice of the output variable (i.e., e_j, v_j or i_j) but **not** on the independent sources.*

Before we prove Theorem 3.5, it is instructive to give some circuit interpretations and an example. The circuit interpretations are:

1. Each term $y(v_{sk}) \triangleq H_k v_{sk}$ in Eq. (3.122) is equal to the response of y when all independent sources in $\mathcal{N}$ except $v_{sk}(t)$ are set to zero.
2. Each term $y(i_{sk}) \triangleq K_k i_{sk}$ in Eq. (3.122) is equal to the response of y when all independent sources in $\mathcal{N}$ except $i_{sk}(t)$ are set to zero.
3. Equation (3.122) shows that the response due to several independent voltage and current sources is equal to the **sum** of the responses due to **each** independent source **acting alone**, i.e., with all other **independent** voltage sources replaced by short circuits, and all other **independent** current sources replaced by open circuits.[11]
4. Equation (3.122) also shows that in applying the superposition theorem, **controlled sources are left intact**.
5. The response at **any time** $t = t_0$ depends **only** on the value of the independent sources at the **same time** $t = t_0$. In other words, linear **resistive** circuits have **no memory**.

[11] Compare this description to the definition of superposition from Exercise 1.9.

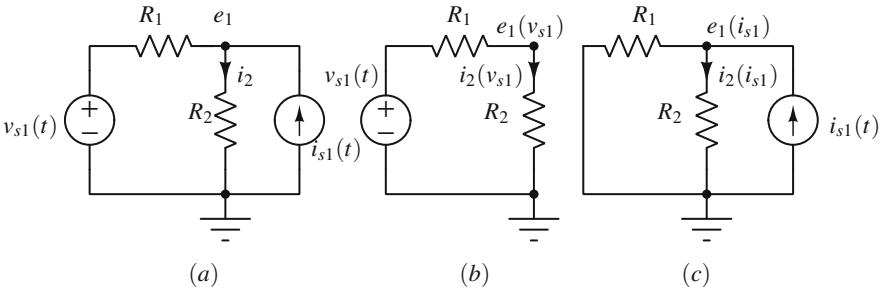


Fig. 3.20 (**a**) Circuit for superposition. (**b**) Voltage divider. (**c**) Current divider

Example 3.6.1 Use the superposition theorem to calculate the node voltage e_1 and resistor current i_2 in Fig. 3.20a.

Solution The contributions to e_1 and i_2 due to $v_{s1}(t)$ acting alone (with $i_{s1}(t) = 0$) can be found by inspection of the **voltage-divider** circuit in Fig. 3.20b, obtained by replacing the current source in Fig. 3.20a with an open circuit:

$$e_1(v_{s1}) = \frac{R_1}{R_1 + R_2} v_{s1}(t) \tag{3.123}$$

$$i_2(v_{s1}) = \frac{1}{R_1 + R_2} v_{s1}(t) \tag{3.124}$$

Here, the "input" v_{s1} is shown as the "argument" of $e_1(\bullet)$ and $i_2(\bullet)$ to remind the reader that the node voltage e_1 given by Eq. (3.123) and the branch current i_2 given by Eq. (3.124) are due to v_{s1} acting alone, and are therefore functions of v_{s1} only.

The contributions to e_1 and i_2 due to $i_{s2}(t)$ acting alone (with $v_{s1}(t) = 0$) can be found by inspection of the **current-divider** circuit shown in Fig. 3.20c, obtained by replacing the voltage source in Fig. 3.20a with a short circuit:

$$e_1(i_{s1}) = \frac{R_1 R_2}{R_1 + R_2} i_{s1}(t) \tag{3.125}$$

$$i_2(i_{s1}) = \frac{R_1}{R_1 + R_2} i_{s1}(t) \tag{3.126}$$

Adding the respective contributions, we obtain:

$$e_1 = e_1(v_{s1}) + e_2(i_{s1}) = H_1 v_{s1}(t) + K_1 i_{s1}(t) \tag{3.127}$$

(continued)

Example 3.6.1 (continued)
where $H_1 \triangleq \frac{R_2}{R_1+R_2}$, $K_1 \triangleq \frac{R_1R_2}{R_1+R_2}$. and:

$$i_2 = i_2(v_{s1}) + i_2(i_{s1}) = H_1 v_{s1}(t) + K_1 i_{s1}(t) \tag{3.128}$$

where $H_1 \triangleq \frac{1}{R_1+R_2}$, $K_1 \triangleq \frac{R_1}{R_1+R_2}$.

As expected, both e_1 and i_2 are of the form specified by Eq. (3.122) where H_1 and K_1 are constants depending **only** on the circuit parameters R_1, R_2 and the chosen output variable. They do not depend on $v_{s1}(t)$ or $i_{s1}(t)$. Of course, for different choices of output variables, we get different H_1's and K_1's, as seen in the expressions for e_1 and i_2.

Proof of the Superposition Theorem Since $\mathcal{N}$ is linear and time-invariant, it is described by the linear tableau equation:

$$\mathbf{T}\mathbf{w}(t) = \mathbf{u}(t) \tag{3.129}$$

where $\mathbf{T}$ is an $[(n-1)+2b] \times [(n-1)+2b]$ constant real tableau matrix. However, since $\mathcal{N}$ is uniquely solvable (by assumption), $\mathbf{T}^{-1}$ exists and the unique solution is given by:

$$\mathbf{w}(t) = \mathbf{T}^{-1}\mathbf{u}(t) \tag{3.130}$$

where:

$$\mathbf{u}(t) \triangleq \left[\underbrace{\mathbf{0}^T}_{n-1} \underbrace{\mathbf{0}^T}_{b} \underbrace{0 \cdots 0}_{\text{resistors}} \underbrace{v_{s1}(t) \cdots v_{s\alpha}(t)}_{\text{voltage sources}} \underbrace{i_{s1}(t) \cdots i_{s\beta}(t)}_{\text{current sources}} \right]^T \tag{3.131}$$

Here we have assumed without loss of generality that all independent sources are labeled last in the order depicted above.

Since each component of $\mathbf{w}(t)$ (i.e., e_j, v_j or i_j) is obtained by multiplying the corresponding row of $\mathbf{T}^{-1}$ with $\mathbf{u}(t)$, it follows that each response e_j, v_j or i_j is given by an expression in the form of Eq. (3.122). Moreover, since $\mathbf{T}^{-1}$ is a constant matrix which does not involve any independent source terms, so are the constant coefficients H_k and K_k. □

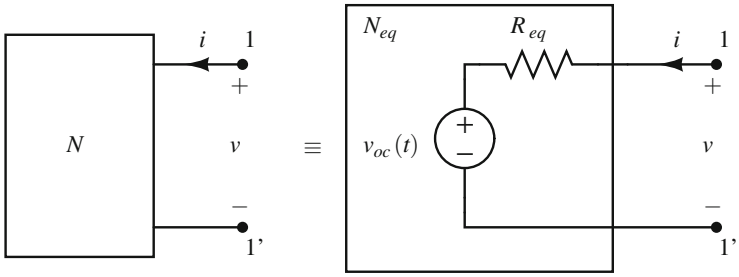
3.6.2 Thévenin-Norton Theorem

Definition 3.3 A one-port N is said to be **well-defined** iff it does not contain any circuit element which is **coupled**, electrically or nonelectrically, to some physical variable **outside** of N.

An example of an ill-defined N would be if it contains a photoresistor coupled to an external light source.

Theorem 3.6 *Any well-defined linear time-invariant resistive one-port N which satisfies the following **unique solvability** condition can be replaced by the following **equivalent one-ports** N_{eq} without affecting the solution of any **external** circuit (not necessarily linear or resistive) connected across N.*

1. *Thévenin equivalent one-port N_{eq}*
   ***unique solvability condition**: The circuit $\mathcal{N}$ obtained by connecting a current source i across N has a unique solution for all i.*



$R_{eq} \triangleq$ *Thévenin-equivalent resistance in ohms*

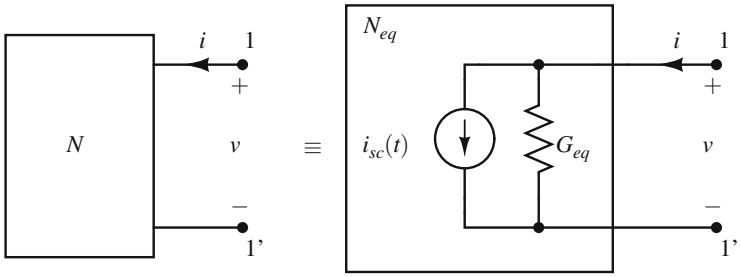
$\triangleq$ *DP or input resistance across N*

after all independent sources inside N are set to zero

$v_{oc}(t) \triangleq$ *open-circuit voltage*

$\triangleq$ *voltage v across terminals 1 and 1' when the port 1, 1' is left open-circuited*

2. *Norton equivalent one-port N_{eq}*
   ***unique solvability condition**: The circuit $\mathcal{N}$ obtained by connecting a voltage source v across N has a unique solution for all v.*



$G_{eq} \triangleq$ *Norton-equivalent conductance in siemens*

$\triangleq$ *DP or input conductance across N*

after all independent sources inside N are set to zero

$i_{sc}(t) \triangleq$ *short-circuit current*

$\triangleq$ *current i entering terminal 1 when terminals 1*

and 1' are connected by an external short circuit

As before, we will consider first some circuit interpretations and an example, before proving the theorem. The circuit interpretations are:

1. The main value of Thévenin's and Norton's theorem is that it allows us to replace any part of a circuit which forms a linear resistive one-port, by only two circuit elements, without affecting the solution of the remainder of the circuit. Conceptually this works because a linear circuit is described by a linear equation. Graphically, in the $i-v$ ($v-i$) plane, we need only two points to fully characterize the linear equation. Thévenin and Norton theorems say we choose the intercepts (i_{sc}, v_{oc}) $((v_{oc}, i_{sc}))$ as the two points (see 3. below).
2. Let $R_{eq} \neq 0$. If we short-circuit the Thévenin equivalent circuit N_{eq} and solve for the current i, we would obtain

$$i_{sc} = -\frac{v_{oc}}{R_{eq}} \tag{3.132}$$

If $i_{sc} \neq 0$, we can calculate the Thévenin equivalent resistance by

$$R_{eq} = -\frac{v_{oc}}{i_{sc}} \tag{3.133}$$

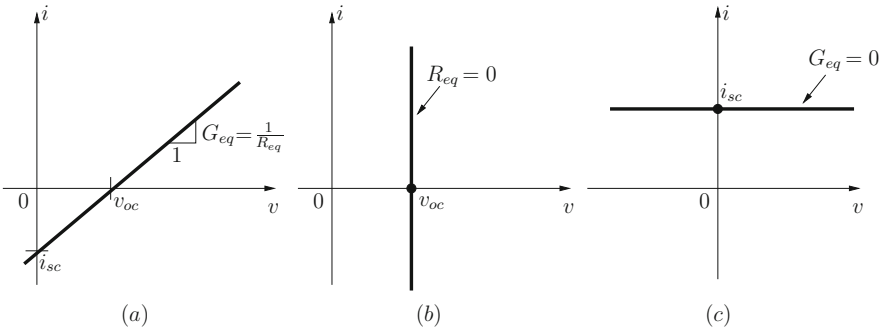


Fig. 3.21 (**a**) DP characteristic of N with $v_{oc} > 0$ and $G_{eq} > 0$. (**b**) DP characteristic with $v_{oc} > 0$ and $R_{eq} = 0$. (**c**) DP characteristic with $i_{sc} > 0$ and $G_{eq} = 0$

3. When $R_{eq} \neq 0$ and $G_{eq} \neq 0$, the one-port N is equivalent to both its Thévenin and its Norton equivalent one-ports: Its DP characteristic at any time t is defined by:

$$v = R_{eq} i + v_{oc}(t) \tag{3.134}$$

$$i = G_{eq} v + i_{sc}(t) \tag{3.135}$$

   This DP characteristic consists of a straight line with a slope R_{eq} and voltage intercept $v_{oc}(t)$ in the $i - v$ plane, or with a slope G_{eq} and current intercept $i_{sc}(t)$ in the $v - i$ plane (shown in Fig. 3.21a).
4. The limiting case of $R_{eq} = 0$ is shown in Fig. 3.21b. The Thévenin equivalent one-port in this case consists of just a battery of v_{oc} volts. The corresponding Norton equivalent one-port does not exist because $G_{eq} \to \infty$. Indeed, the unique solvability condition fails in this case—KVL is violated when a voltage source $v \neq v_{oc}$ is applied.

   The "dual" limiting case $G_{eq} = 0$ is shown in Fig. 3.21c.
5. A one-port which has neither a Thévenin nor Norton equivalent is shown in Fig. 3.22a.

   Its DP characteristic is defined by:

$$v = 0 \quad i = 0 \tag{3.136}$$

   and consists therefore of only one point, namely, the origin. Note that the "virtual short circuit" characterizing the input port of an **ideal** opamp operating in the linear region has precisely this property. Such a one-port is called a **nullator**.
6. It follows from the above observations that if N is not current-controlled, then it does **not** possess a Thévenin equivalent. Dually, if N is not voltage-controlled, then it does **not** possess a Norton equivalent. Hence, in applying Thévenin's or Norton's theorem, we can ignore checking for the "unique solvability condition"

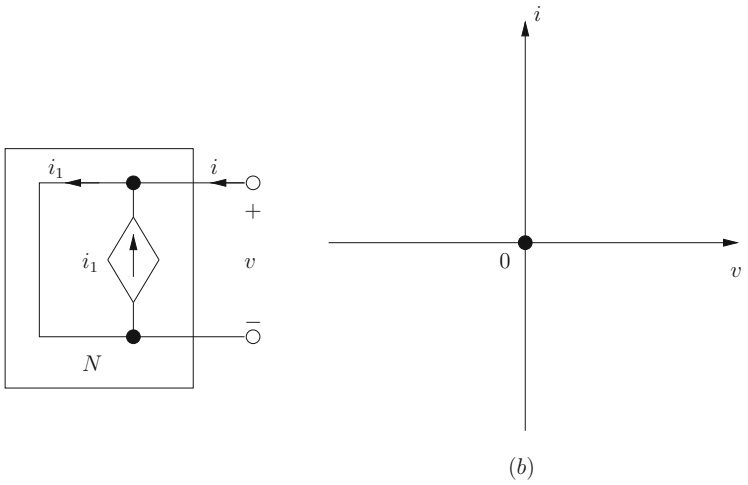


Fig. 3.22 A one-port characterized by only one point (**a**) Circuit (**b**) DP plot

since this generally entails the difficult task of checking if the associated tableau matrix **T** is invertible. Instead, we simply proceed to calculate R_{eq} or G_{eq}. Failure to obtain a unique finite value for R_{eq} (respectively G_{eq}) would then imply that N does not have a Thévenin (respectively Norton) equivalent.

Example 3.6.2 Find the Thévenin and Norton equivalent one-ports for the circuit shown in Fig. 3.23a.

Solution Let us calculate R_{eq} and G_{eq} first using the simplified circuit shown in Fig. 3.23b. For any applied voltage v, we find $i_1 = v/R$ so that $i = -4i_1 = -(4/R)v$. Hence,

$$R_{eq} = \frac{1}{G_{eq}} = -\frac{R}{4} \tag{3.137}$$

Since both R_{eq} and G_{eq} are finite numbers, we know that N has a Thévenin and a Norton equivalent one-port.

We proceed therefore to calculate v_{oc} using the circuit shown in Fig. 3.23c. Applying KCL we obtain $i_1 - 5i_1 + I_s = 0$ or $i_1 = I_s/4$. Hence,

$$v_{oc} = E + \frac{R}{4} I_s \tag{3.138}$$

(continued)

Example 3.6.2 (continued)
To calculate i_{sc}, we use Eqs. (3.132) and (3.138) to get:

$$i_{sc} = -\frac{v_{oc}}{R_{eq}} = \frac{4E}{R} + I_s \tag{3.139}$$

As an independent check, let us derive i_{sc} using the circuit in Fig. 3.23d. Since $i_1 = -\frac{E}{R}$ in this case, KCL implies:

$$i_{sc} = i_1 - 5i_1 + I_s = \frac{4E}{R} + I_s \tag{3.140}$$

which agrees with our first i_{sc} equation (as it should).

Proof of Norton's Theorem We will prove only Norton's theorem, as the dual proof then applies to Thévenin's theorem. Let N denote the one-port in question, and let the remaining part of the circuit $\mathcal{N}$ be denoted by N_L, as shown in Fig. 3.24a. By hypotheses, N contains only linear time-invariant resistors and independent sources, whereas N_L need not be linear or resistive.

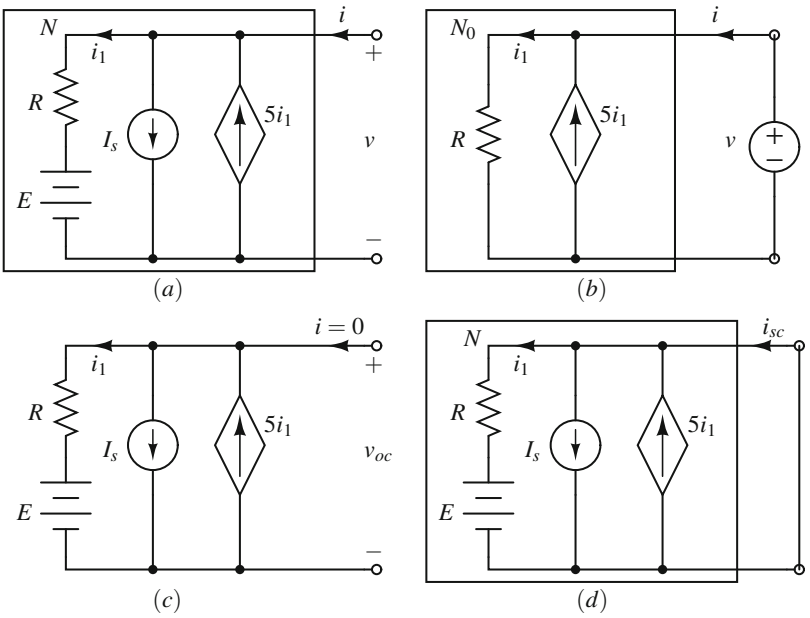


Fig. 3.23 (**a**) One-port N. (**b**) Simplified one-port N_0 obtained by setting all independent sources inside N to zero. (**c**) Circuit used for calculating v_{oc}. (**d**) Circuit used for calculating i_{sc}

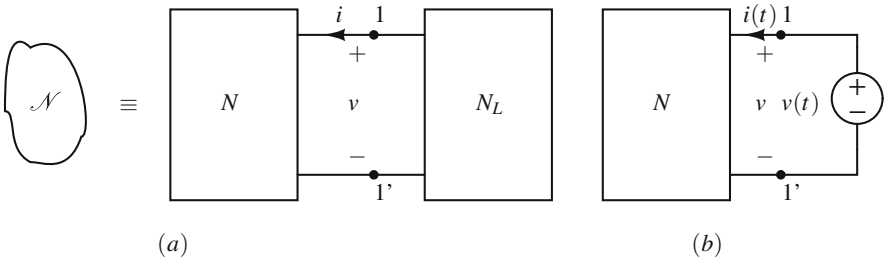


Fig. 3.24 (**a**) Partitioning arbitrary circuit $\mathcal{N}$ into a linear resistive one-port N and a not necessarily linear or resistive one-port N_L. (**b**) Driving N with a voltage source $v(t)$

Since N is purely resistive, it is completely specified by its DP characteristic at each instant of time. Hence, as far as N_L is concerned, its solution depends only on this DP characteristic: The elements inside N which give rise to this DP characteristic are completely irrelevant. For example, we don't care if N consists of a 2 Ω resistor or two 1 Ω resistors in series, as long as we have a 2 Ω **equivalent** DP resistance. It suffices therefore to prove that both N and its Norton equivalent one-port have identical DP characteristics.

Let us drive N with an independent voltage source $v(t)$ as shown in Fig. 3.24b. Let us label this voltage source, together with the independent voltage sources inside N by $v_{s0}(t), v_{s1}(t), \ldots, v_{s\alpha}(t)$, where $v_{s0}(t) \triangleq v(t)$. Similarly, let us label the independent current sources inside N by $i_{s1}(t), \ldots, i_{s\beta}(t)$.

It follows from the unique solvability condition that the linear time-invariant resistive circuit in Fig. 3.24b has a unique solution for all values of the independent sources, at all times. Hence we can apply the superposition theorem and conclude that the port current $i(t)$ in Fig. 3.24b must assume the form:

$$i(t) = H_o v(t) + \sum_{k=1}^{\alpha} H_k v_{sk}(t) + \sum_{k=1}^{\beta} K_k i_{sk}(t) \tag{3.141}$$

Now if $v(t) = 0 \ \forall t$, $i(t)$ is by definition $i_{sc}(t)$. Hence the last two sums in Eq. (3.141) add up to $i_{sc}(t)$.

If we set to zero all independent sources inside N, we are left with $i(t) = H_0 v(t)$, i.e., $H_0 = G_{eq}$. Hence Eq. (3.141) can be written in the form:

$$i(t) = G_{eq} v(t) + i_{sc}(t) \tag{3.142}$$

where G_{eq} and $i_{sc}(t)$ are as defined in the theorem. Equation (3.142) gives the DP characteristic of the given one-port N. Since this is the same equation which defines the Norton equivalent one-port N_{eq}, it follows that N can indeed be replaced by a Norton equivalent N_{eq} without affecting the solution inside N_L. □

3.7 Some General Properties of Nonlinear Resistive Circuits

The behavior of linear resistive circuits is intimately related to linear algebraic equations. As a consequence of linearity, we were able to derive several rather general properties in the preceding section. Precisely because their proofs depend on linearity in a crucial way, none of these properties holds even if the circuit contains only one nonlinear resistor.

The behavior of nonlinear resistive circuits is far more complicated. For example, multiple solutions are frequent. Even describing a two-terminal nonlinear resistor alone can be complicated. To specify it analytically we need to use a function which may require many parameters (for example, the *pn*-junction diode).

In spite of its greatly increased complexity, many useful properties can be proved for various subclasses of nonlinear resistive circuits. Our objective in this section is to state only those properties which we are in a position to prove, in a remarkably elegant manner. These general properties, derived from the fundamental concepts of passivity and monotonicity, form only a small albeit important subset of our "nonlinear tool kits." We hope this final section will whet the reader's appetite into a more advanced study of this subject.

3.7.1 Strict Passivity

Definition 3.4 A two-terminal resistor is said to be **strictly passive** iff $vi > 0$ for all points (v, i) on its characteristic, except the origin $(0, 0)$.

Geometrically, this means that the $v - i$ curve of a strictly passive resistor must lie only in the first and third quadrants and stay clear of the v and i axis, except the origin.

Most of the nonlinear resistors we have encountered so far as strictly passive. However, the ideal diode concave resistor, and convex resistor are passive but not strictly passive.

In this section we will state and prove three general theorems for circuits containing only strictly passive resistors and independent sources.

Theorem 3.7 (Strict Passivity Property) *A one-port made of strictly passive two-terminal resistors is itself strictly passive.*

Proof Consider the one-port N shown in Fig. 3.25, which is driven by a voltage source. Let N contain m strictly passive resistors. Applying Tellegen's theorem and noting that the current **entering** the positive terminal of the voltage source is equal

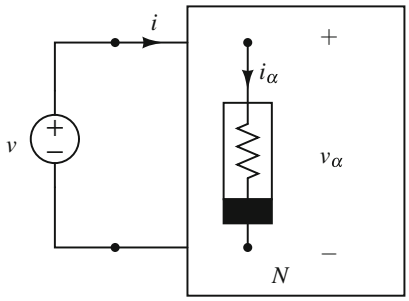


Fig. 3.25 One-port N

to $-i$ (passive sign convention), we obtain:

$$vi = \sum_{\alpha=1}^{m} v_\alpha i_\alpha \tag{3.143}$$

Since the m resistors are strictly passive for all α, $v_\alpha i_\alpha \geq 0$, hence $vi \geq 0$.

Suppose $v > 0$, then by KVL some of the v_α's must be nonzero. Thus by strict passivity, the corresponding i_α's are also nonzero and of the same sign. Hence whenever $v > 0$ at least one term, say $v_k i_k$, is positive. So we have $v > 0$ implies $i > 0$.

A similar argument shows that $v < 0$ implies $i < 0$. Hence $vi > 0$ for all points on the driving point characteristic except the origin (where $vi = 0$). Therefore N is strictly passive. □

Theorem 3.8 (Maximum Node-Voltage Property) *Let $\mathcal{N}$ be a connected circuit made of strictly passive two-terminal resistors and driven by a single DC voltage source of E volts, $E > 0$. Then, with the negative voltage-source terminal chosen as ground, no node-to-ground voltage can exceed E volts.*

Proof Since $\mathcal{N}$ is connected, all node-to-ground voltages $e_1, e_2, \cdots, e_{n-1}$ are well-defined.

Suppose there exists a node m with the highest potential $e_m > E$. Since $e_a, e_b, \ldots, e_k \leq e_m$, we have $v_a, v_b, \ldots, v_k \geq 0$. Since all resistors are strictly passive, this implies that $i_a, i_b, \ldots, i_k \geq 0$. But for KCL to be satisfied at node m, we must have $i_a = i_b = \cdots = i_k = 0$. By strict passivity, this implies that $v_a = v_b = \cdots = v_k = 0$. Thus, we have $e_a = e_b = \cdots = e_k = e_m > E$ (Fig. 3.26).

Hence we can move on to nodes $a, b, \ldots, k$ and repeat the above reasoning. We must eventually reach node 1 of the voltage source, where our reasoning would still

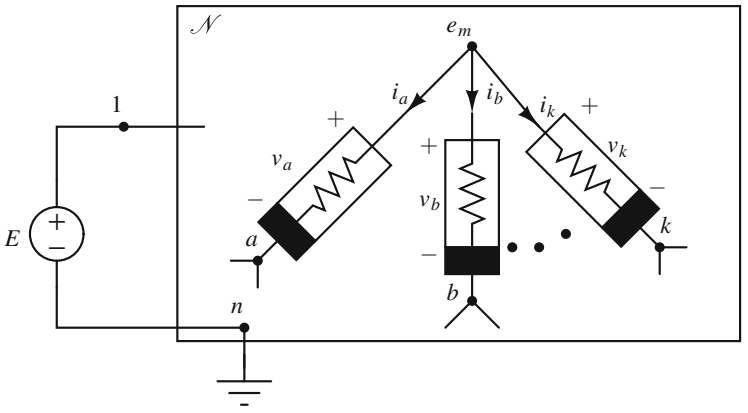


Fig. 3.26 KCL at node m implies $i_a + i_b + \cdots + i_k = 0$

imply that $e_1 = e_m > E$, which is false. Hence our assumption that $e_m > E$ is wrong and thus $e_m \leq E$. □

Theorem 3.9 (Transfer Characteristic Bounding Region) *The v_o vs. v_{in} transfer characteristic of any connected circuit made of strictly passive two-terminal resistors must lie within the wedge-shaped region*

$$|v_o| \leq |v_{in}| \tag{3.144}$$

as shown in Fig. 3.27b.

Proof Consider in Fig. 3.27b the right-half plane with $v_{in} > 0$. Suppose the output voltage v_o is measured between node k and node l so that:

$$v_o = e_k - e_l \tag{3.145}$$

where e_k and e_l are measured with respect to the ground node shown in Fig. 3.27a.

Since $\mathcal{N}$ contains only strictly passive two-terminal resistors, it follows from the maximum node-voltage property in Theorem 3.8 that:

$$0 \leq e_k \leq v_{in} \tag{3.146}$$

$$0 \leq e_l \leq v_{in} \tag{3.147}$$

Inequality (3.147) can be rewritten as:

$$-v_{in} \leq -e_l \leq 0 \tag{3.148}$$

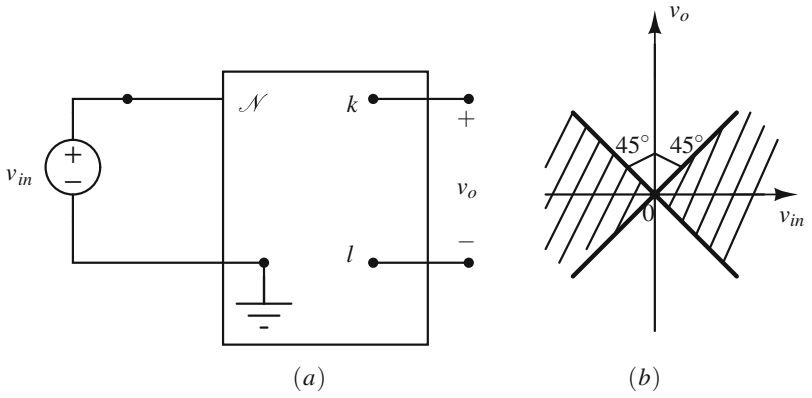


Fig. 3.27 Output voltage bounding region

Adding both inequalities (3.146) and (3.148), we get:

$$-v_{in} \leq e_k - e_l \leq v_{in} \tag{3.149}$$

Using our earlier definition: $v_o = e_k - e_l$ and simplifying we get:

$$|v_o| \leq v_{in} \tag{3.150}$$

Note that we had assumed $v_{in} > 0$ and used the right-half plane. A similar proof for the left-half plane ($v_{in} < 0$) would give: $|v_o| \leq -v_{in}$. We thus have: $|v_o| \leq |v_{in}|$. □

3.7.2 Strict Monotonicity

Strict passivity does not impose any constraint on the slope of the resistor characteristic. It only requires that the product vi be positive except at the origin. For example, the tunnel diode described earlier is strictly passive. Yet the slope of its characteristics can assume both positive and negative values, depending on the operating point. Such characteristics are said to be **nonmonotonic**.

It is clear that resistive circuits made of nonmonotonic resistors would in general also give rise to a nonmonotonic DP and transfer characteristics. Hence in order to derive properties involving constraints on the slope of the DP and transfer characteristics, it is necessary to impose stronger conditions on the resistor characteristics. The strictly monotone-increasing, or **strictly increasing** for brevity, is one such condition which we investigate in this final section.

Strictly increasing means roughly that the slope of the characteristic is positive everywhere. More precisely, a two-terminal resistor is said to be **strictly increasing**

iff, for all pairs of (distinct) points on its characteristic, say (v', i') and (v'', i'') $(v' > v'', i' > i'')$ we have:

$$(v' - v'')(i' - i'') > 0 \tag{3.151}$$

Note that a strictly increasing characteristic is not restricted to lie in the first and third quadrants only. Hence, a strictly increasing resistor need not be strictly passive, and a strictly passive resistor need not be strictly increasing.

Theorem 3.10 *Any circuit made of strictly increasing two-terminal resistors and independent sources has at most one solution.*

Proof Suppose there are two distinct operating points Q and Q', at some time t, corresponding to $(v_1, v_2, \ldots, v_b; i_1, i_2, \ldots, i_b)$ and $(v'_1, v'_2, \ldots, v'_b; i'_1, i'_2, \ldots, i'_b)$, respectively. Here we assume passive sign convention for all elements.

Since each of these two solutions satisfies Tellegen's theorem, so does their difference:

$$\sum_{k=1}^{b} (v_k - v'_k)(i_k - i'_k) = 0 \tag{3.152}$$

Observe that each term in Eq. (3.152) which corresponds to either a voltage source $(v_k = v'_k)$ or a current source $(i_k = i'_k)$ vanishes. However, since these are two distinct solutions and since all resistors are strictly increasing, there must exist at least one branch such that $(v_k - v'_k)(i_k - i'_k) > 0$ for this branch. This contradicts Eq. (3.152). Hence there cannot be two distinct operating points Q and Q'. □

Theorem 3.11 *A one-port made of strictly increasing two-terminal resistors is itself strictly increasing.*

Proof Suppose the one-port N in Fig. 3.25 contains only strictly increasing resistors. Then for any two distinct DP voltages v and v', let (v_k, i_k) and (v'_k, i'_k), $k = 1, 2, \ldots, b$ denote the corresponding unique branch voltage and current solutions, for all b resistors inside N. It follows from Tellegen's theorem that:

$$(v - v')(i - i') = \sum_{k=1}^{b} (v_k - v'_k)(i_k - i'_k) \tag{3.153}$$

where the input term appears on the left of the equation because the input current i in Fig. 3.25 is defined as leaving the positive terminal of the voltage source.

Since $v \neq v'$, KVL requires that at least one of the $(v_k - v'_k)$ differs from 0; hence, at least one term on the right-hand side of Eq. (3.153) is positive, while all the others are ≥ 0 (since all resistors are strictly increasing) where the equality sign holds whenever $v_k = v'_k$ or $i_k = i'_k$. Consequently,

$$(v - v')(i - i') > 0 \tag{3.154}$$

whenever $v \neq v'$, i.e., the DP characteristic of N is strictly increasing. □

3.8 Conclusion

This chapter has given an **overview** of techniques for analysis of nonlinear networks. But, unlike dynamic nonlinear networks (the subject of Chap. 4), the realm of resistive nonlinear networks does have a general theory. Once the reader has mastered the concepts summarized below from this chapter, they can pick up this general theory from excellent references such as [1].

1. For resistive circuits, nodal analysis is applicable if the circuit contains only voltage-controlled resistors and independent current sources (which do not form cut sets among themselves).
2. The node equation for a linear resistive circuit is given by:

$$\mathbf{Y}_n \mathbf{e}(t) = \mathbf{i}_s(t) \tag{3.155}$$

where $\mathbf{Y}_n \triangleq \mathbf{A}\mathbf{Y}_b\mathbf{A}^T$ is called the node-admittance matrix; $\mathbf{A}$ is the reduced incidence matrix of the reduced digraph obtained by open-circuiting all branches corresponding to independent current sources from the original digraph; $\mathbf{Y}_b$ is the branch-admittance matrix; $\mathbf{i}_s(t)$ is the source vector whose kth entry is equal to the algebraic sum of all independent current sources entering node k.

For a reduced digraph with n nodes and b branches, $\mathbf{Y}_b$ is a $b \times b$ matrix, $\mathbf{Y}_n$ is an $(n-1) \times (n-1)$ matrix, $\mathbf{A}$ is an $(n-1) \times b$ matrix; both $\mathbf{e}$ and $\mathbf{i}_s(t)$ are $n-1$ vectors.

3. A nonlinear resistive circuit driven only by independent current sources has a node equation given by:

$$\mathbf{A}\mathbf{g}(\mathbf{A}^T\mathbf{e}) = \mathbf{i}_s(t) \tag{3.156}$$

where $\mathbf{i} = \mathbf{g}(\mathbf{v})$ denotes the characteristics of all (voltage-controlled) resistors.

4. Both the linear and nonlinear node equations consist of $n-1$ equations in terms of the node voltage vector $\mathbf{e}$, where n is the number of nodes in the circuit. Hence the number of equations in nodal analysis does not depend on the number of branches in the circuit.

5. Every linear time-invariant resistive circuit has a tableau equation of the form:

$$\underbrace{\begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{A} \\ -\mathbf{A}^T & \mathbf{I} & \mathbf{0} \\ \mathbf{0} & \mathbf{M}(t) & \mathbf{N}(t) \end{bmatrix}}_{\mathbf{T}(t)} \underbrace{\begin{bmatrix} \mathbf{e}(t) \\ \mathbf{v}(t) \\ \mathbf{i}(t) \end{bmatrix}}_{\mathbf{w}(t)} = \underbrace{\begin{bmatrix} \mathbf{0} \\ \mathbf{0} \\ \mathbf{u}_s(t) \end{bmatrix}}_{\mathbf{u}(t)} \tag{3.157}$$

   The entries of **M** and **N** contain constant coefficients defining the resistors; the entries of $\mathbf{u}_s(t)$ contain constant or time functions defining the independent sources.
6. A linear time-invariant resistive circuit has a unique solution iff the tableau matrix **T** is nonsingular.
7. Every nonlinear resistive circuit has a tableau equation of the form:

$$\begin{aligned} \mathbf{A}\mathbf{i}(t) &= \mathbf{0} \\ \mathbf{v}(t) - \mathbf{A}^T\mathbf{e}(t) &= \mathbf{0} \\ \mathbf{h}(\mathbf{v}(t), \mathbf{i}(t), t) &= \mathbf{0} \end{aligned} \tag{3.158}$$

8. A resistive circuit is said to be uniquely solvable iff Kirchhoff's laws and the branch equations are simultaneously satisfied by a unique set of branch voltages and a unique set of branch currents for all t.
9. The superposition theorem is applicable to any linear uniquely solvable resistive circuit. It allows us to find the solution by calculating first the solutions due to each independent source acting alone, and then adding them.
10. A one-port N is said to be well-defined iff it does not contain any circuit element which is coupled, electrically or nonelectrically, to some physical variable outside of N.
11. The Thévenin (Norton) theorem allows us to replace any well-defined linear current-controlled (voltage-controlled) resistive one-port by an equivalent one-port consisting of an equivalent Thévenin resistance R_{eq} (equivalent Norton conductance G_{eq}) in series (parallel) with an open-circuit (short-circuit) voltage source $v_{oc}(t)$ (current source $i_{sc}(t)$).
12. In applying the superposition, Thévenin and Norton theorems, all dependent sources must be left intact.
13. A two-terminal resistor is strictly passive iff $vi > 0$, for all points in its characteristic except the origin.
14. We studied the strict passivity, maximum node-voltage and transfer characteristic bounding regions for strictly passive networks.
15. A two-terminal resistor is strictly increasing iff $(v'-v'')(i'-i'') > 0$ for all pairs of distinct points (v', i') and (v'', i'') on its characteristic ($v' > v'', i' > i''$).
16. We studied the uniqueness and strictly increasing closure properties for networks with strictly increasing resistors.

Lab 3: DC Simulation in QUCS

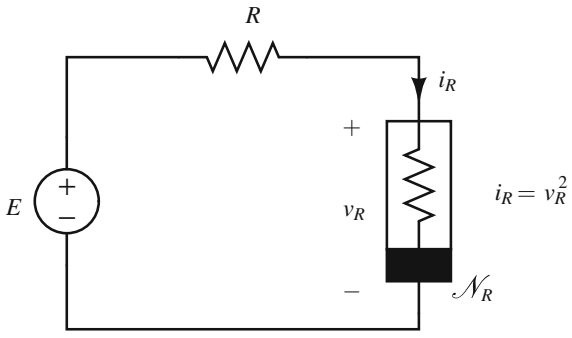
Objective: To understand DC simulation in QUCS
Theory:
Unlike the previous chapters, we first encourage you to do the lab component to this chapter. In other words, now that you have an understanding of the techniques for nonlinear resistive circuit analysis, be sure to simulate the circuits from this chapter (and the exercises) below in QUCS. In this lab, you will perform DC analysis (DC simulation in QUCS) for the nonlinear circuit shown in Fig. 3.28.

1. Suppose $E = 6$ V, $R = 2\ \Omega$. Solve analytically for the DC solution, specifically i_{QR} and v_{QR}. Although the circuit equations are trivial to set up, we recommend that you use tableau analysis so that you become familiar with the method.
2. Now, let $E = 2$ V, $R = 2\ \Omega$. Again analytically find the DC solution: i_{QR}, v_{QR}.

We will now simulate the circuit in QUCS.
Lab Exercise:

1. The circuit.[12] to be entered in QUCS is shown in Fig. 3.29. Use the Equation Defined Device (EDD) for specifying $\mathcal{N}_R$. This device can be found under nonlinear components.
2. Simulate the circuit for both $E = 6\,\text{V}$ and $E = 2\,\text{V}$. Discuss the results. Specifically, what do you notice about the solution when $E = 2\,\text{V}$. Explain the solution.

Fig. 3.28 Circuit for lab 3



[12] If you are unfamiliar with the QUCS component notation for the passive sign convention, please be sure to go through the introductory QUCS video online (refer to lab 1).

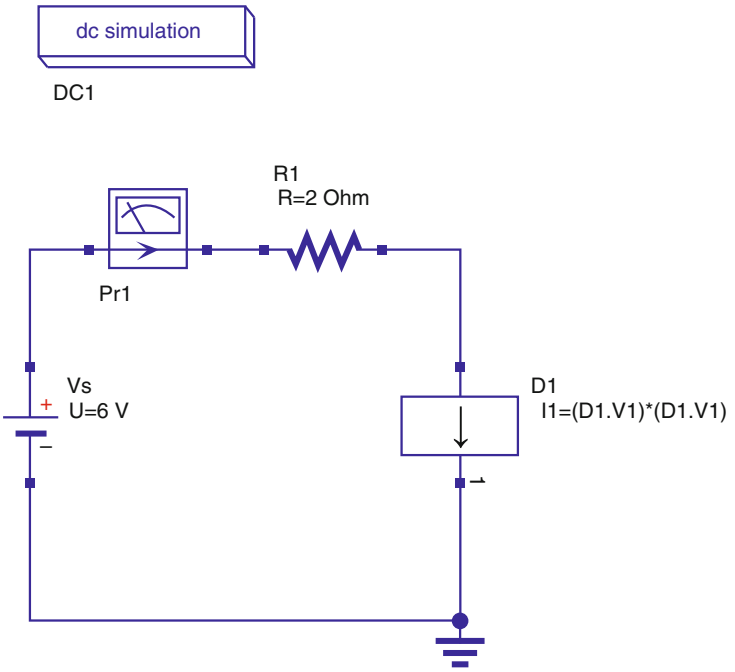


Fig. 3.29 QUCS schematic for circuit in Fig. 3.28

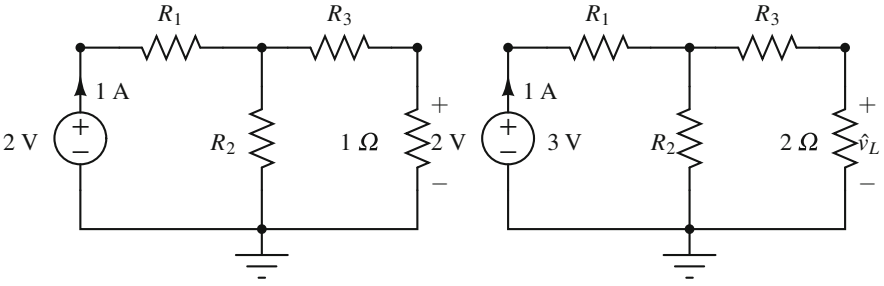


Fig. 3.30 Circuit for problem 3.2

Exercises

3.1 Show that the voltage gain of the CE amplifier in Fig. 3.8b is given by:

$$\frac{\tilde{v}_2}{v_s} = \frac{-h_{21}}{(h_{11} + R_1)(h_{22} + 1/R_2) - h_{12}h_{21}} \tag{3.159}$$

3.2 Figure 3.30 shows two distinct networks $\mathcal{N}$ and $\hat{\mathcal{N}}$. Determine the value of $\hat{v}_L$.

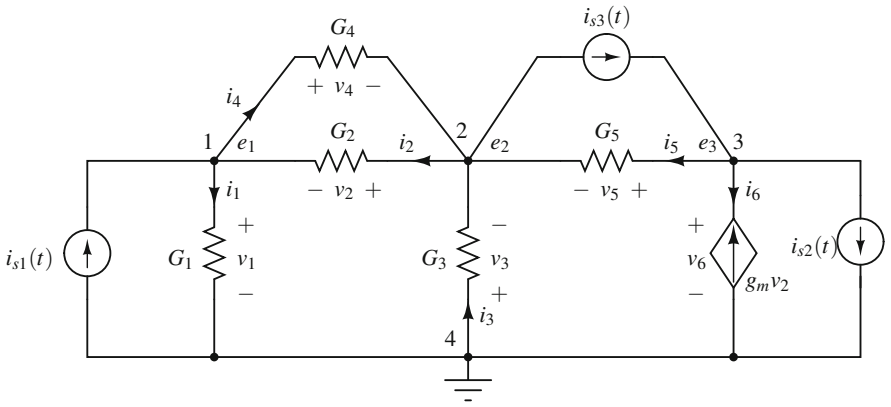


Fig. 3.31 Circuit for problem 3.3

3.3 Write the node equations for the circuit in Fig. 3.31, in terms of the reduced incidence matrix **A**.

3.4 Show that branch admittance matrix $\mathbf{Y}_b$ in Eq. (3.87) is a diagonal matrix, if $\mathcal{N}$ contains only two-terminal linear resistors and independent current sources.

3.5 To appreciate the benefits of superposition and its domain of applicability, consider a nonlinear resistor $v = \hat{v}(i) = i^3$ driven by two current sources $i_{s1}(t) = I_1 \cos \omega_1 t$ and $i_{s2}(t) = I_2 \cos \omega_2 t$ connected in parallel, where $I_1, \omega_1, I_2, \omega_2$ are constants. Calculate the voltage v when each source acts alone, and when they act together. In each case, reduce your answer to a sum of pure sine waves.

1. Does superposition hold for this circuit?
2. What are the frequency components of the output waveform for each case?

Exercise 4.13 explores further the frequency behavior of linear vs. nonlinear systems.

3.6 Find the Thévenin and Norton equivalent circuits for the one-ports shown in Fig. 3.32. If a particular circuit fails to have a Thévenin and/or Norton equivalent, explain.

3.7 In this exercise, we will derive the **maximum power transfer theorem for linear resistive circuits**.

Consider the circuit shown in Fig. 3.33. R_L models a loudspeaker in a concert hall. In order to maximize the output power delivered by the power amplifier (modeled by $v_s(t)$ in series with internal resistance R_1), a transformer with an appropriate turns ratio n is sandwiched between the amplifier and the loudspeaker.

1. Simplify the circuit by first finding the Thévenin equivalent at terminals $2, 2'$. Your v_{oc} and R_{eq} expressions should include a function of the transformer turns ratio n.

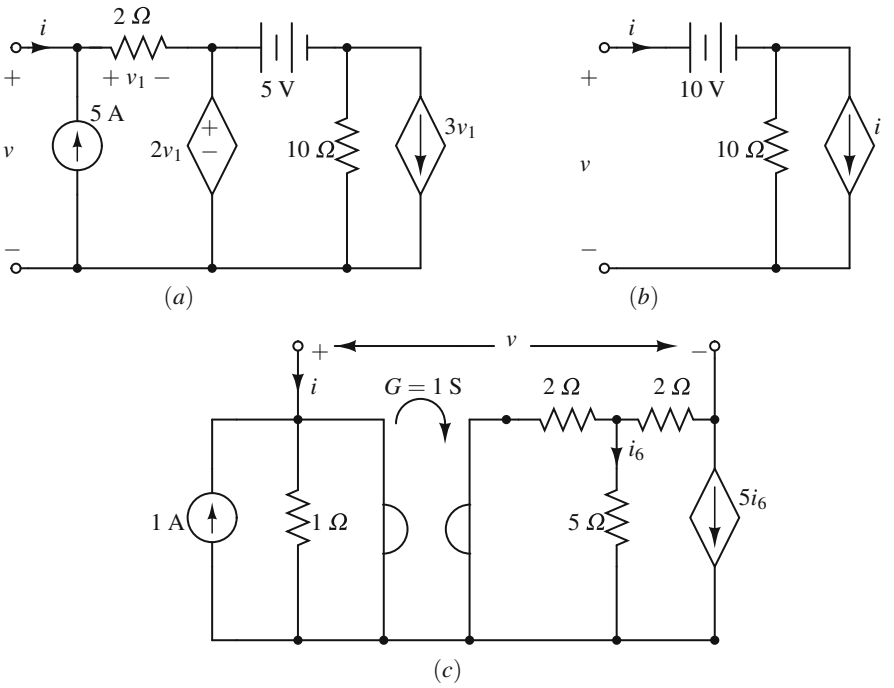


Fig. 3.32 (**a**-**c**) Circuits for problem 3.6

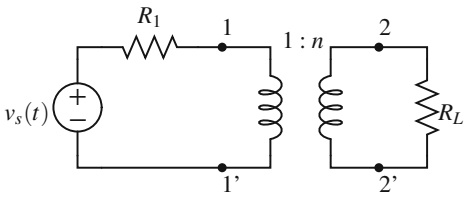


Fig. 3.33 Circuit for problem 3.7

2. From the answer in 1. above, determine the value of R_L (in terms of R_{eq}) that would maximize the power dissipated **in** R_L. To do this, you would have to find an expression for the power associated with R_L and use calculus.

The answer to 2. above is the maximum power transfer theorem for linear resistive circuits.

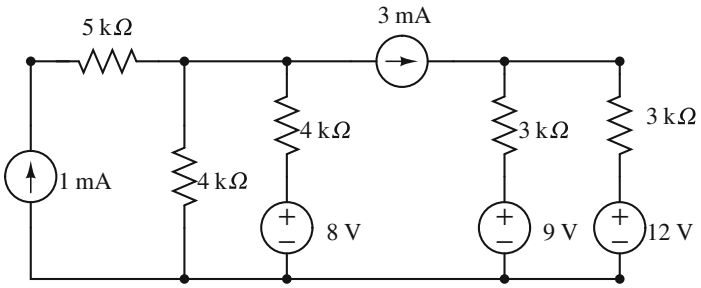


Fig. 3.34 Circuit for problem 3.8

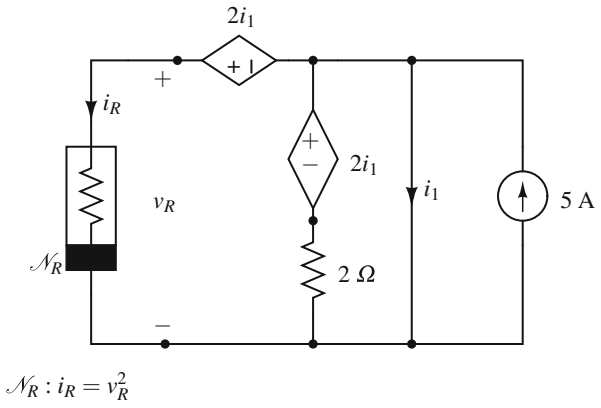


Fig. 3.35 Circuit for problem 3.9

3.8 Using repeated application of Thévenin and Norton theorems, simplify the circuit in Fig. 3.34 to a single loop and then determine the voltage across current source 3 mA current source. This repeated simplification of a circuit by switching between Thévenin and Norton equivalents is called **source transforms**.

3.9 Find all possible values for i_R and v_R for the circuit shown in Fig. 3.35.

References

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2. Chua, L.O.: University of California, Berkeley EE100 Fall 2008 Supplementary Lecture Notes on Tableau Analysis (2008). Available, online: http://inst.eecs.berkeley.edu/~ee100/fa08/lectures/EE100supplementary_notes_12.pdf. Last accessed November 25th 2017
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