Cameras with On-chip Memory CMOS Image Sensors

Rihito Kuroda and Shigetoshi Sugawa

Abstract In this article we give an overview of ultra high-speed (UHS) CMOS image sensors with on-chip analog memories placed on the periphery of pixel array and high speed cameras with the UHS CMOS image sensors for the visualization of UHS phenomena. The developed image sensors consist of $400^{H} \times 256^{V}$ pixels and 128 memories/pixel, and the readout speed of 1 T pixel/s is obtained, leading to 10 Mfps full resolution video capturing with consecutive 128 frames, and 20 Mfps half resolution video capturing with consecutive 256 frames. The first development chip was employed in the high-speed video camera and put in practical use in 2012. By the development of dedicated process technologies, photosensitivity improvement and power consumption reduction were simultaneously achieved, and the performance-improved chip has been utilized in the commercialized high-speed video camera since 2015 offering 10 Mfps with ISO 16000 photosensitivity. Due to the improved photosensitivity, clear images can be captured and analyzed even under low light condition, such as under a microscope, and capturing of UHS light emission phenomena.

1 Introduction

Ultra high-speed (UHS) image sensors with over 1 Mfps (frames per second) video capturing speed are utilized in various scientific and engineering fields for studying UHS phenomena, such as microbubbles, fluids, high speed impacts, breakdown, plasma and discharge, and others [1–10]. A high frame rate is needed especially when analyzing small moving objects under the microscope, because the field of

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view becomes small. In order to visualize these fast object, a frame rate of around 10 Mfps is required.

In order to capture the UHS phenomena precisely, a high frame rate is not the only performance that is required for imaging devices. A high resolution and a long record length are also required. There are fundamental trade-off relationships among these three performances; it is hard to improve all of the speed, the resolution and the record length simultaneously. Consequently, it is a realistic target to develop an image sensor that achieves a UHS frame rate of 10 Mfps while maintaining a sufficient resolution and record length.

Various types of UHS image sensors have been reported in recent years [10]; a back side illumination CCD (charge coupled device) image sensor with serial CCD memories near photodiode (PD) in each pixel [11], a CMOS (complementary metal oxide semiconductor) and CCD hybrid image sensor with two dimensional CCD memories near photodiode in each pixel [12, 13], a CMOS image sensor with multiple on chip analog memories per pixel separately placed from the pixel region developed by the authors' group [10, 14–17], and a multi-aperture CMOS image sensor with temporally compressive sampling [18].

The UHS CMOS image sensor developed by the authors' group has simultaneously achieved 10 Mfps (20 Mfps in development), 10 Kpixels, 128 frames, and the high-speed video camera employing the sensor chip has been utilized to capture what had not been seen before [5–10].

The following points are the main performance requirements that we targeted to achieve for the development of the UHS image sensor.

- Maximum frame rate: about 10 Mfps
- Number of pixels: 60–100 Kpixels, i.e., the signal readout rate given by the product of frame rate and number of pixels of 1 Tpixel/s
- Light sensitivity: High sensitivity due to a large number of incident photons and high photo-electron conversion efficiency
- Spectral response: High sensitivity for a wide wave band of visible to near infrared (NIR) light
- Record length: Over 100 frames with burst capturing
- Capturing mode: Both burst and continuous video capturing
- Electronic shutter: Global shutter of which shutter period is controllable independent of the frame rate
- Standby operation: Sufficiently long standby operation for UHS video capturing, i.e., over 1 min with the highest frame rate condition
- Trigger for burst capturing: Start, end and middle trigger modes with various trigger signals such as light, sound, voltage, current, image signal and so on
- Parasitic light sensitivity of the on-chip memory: No impact to the stored signal under a strong light illumination that is often employed during video capturing of UHS phenomena
- Usability/maintenance: Without complicated setup sequence and maintenance
- System size: Easy-to-handle small size and light weight without cooling system

For the UHS video camera, a CCD image sensor with on-chip CCD cells amounting to the recording frame number near the photodiode was developed and put into practical use, and the research and development have been made for further performance improvement. However, there are some difficulties to be overcome; the charge transfer characteristic degrades at a high speed, the stored signals tend to be affected due to strong light illumination, the standby operation period is limited due to the heat generation even though a cooling system is employed. Subsequently, the practical frame rate has been limited at around 1 Mfps.

On the other hand, for the CMOS image sensors due to their active pixel operation scheme, it is easier to reduce the power consumption than for CCD image sensors, as well as on-chip circuitry is flexibly implemented. Therefore, it is possible to develop a UHS CMOS image sensor with a higher performance than the CCD image sensors.

Figure 1 shows the schematic illustrations of the various high speed CMOS image sensor architectures in comparison to the general analog signal output CMOS image sensors [10]. The high-speed CMOS image sensors are classified into three groups; the parallel analog output type shown in Fig. 1b, the column parallel analog-to-digital converter (ADC) and digital signal output type shown in Fig. 1c, and the on-chip analog memory type shown in Fig. 1d. The first two types shown in Fig. 1b–c are for the continuous video capturing operation. The pixel readout rates of 1–10 Gpixel/s have been achieved.

Figure 2 summarizes the factors affecting the frame rate of CMOS image sensors [10]. These are;

(A) Photo-carrier collection time which is limited to diffusion/drift time of photo-carriers in the photodiode.
(B) Settling time of the pixel driving signals mainly limited by the RC time constant of metal wires.
(C) Readout time from the pixel to the column line mainly limited by the constant current source and RC time constant of metal wires.

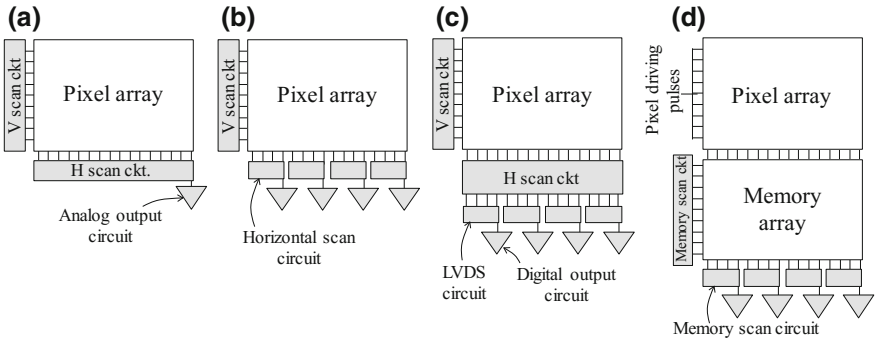

Fig. 1 Schematic illustrations of high speed CMOS image sensor architectures, **a** general analog signal output type, **b** parallel analog output type, **c** column parallel ADC and digital output type and **d** on-chip analog memory type

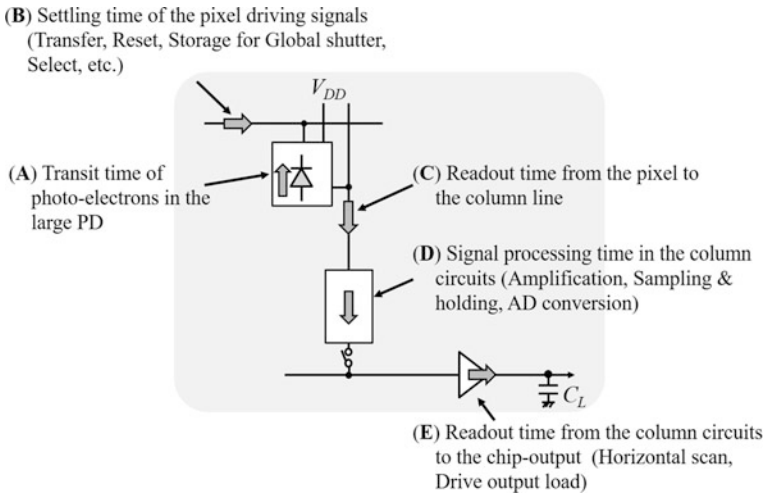

Fig. 2 Factors affecting the frame rate in a CMOS image sensor

(D) Signal processing time in the column circuits mainly due to amplification, sampling & holding and analog-to-digital conversion.
(E) Readout time from the column circuits to the horizontal line and the chip output limited by RC time constant of metal wire and output load.

If the factor (A) is the only constraint, a frame rate of over 100 Mfps is to be achieved regardless of pixel numbers. However, in reality, there are other constraints regarding the global pixel driving pulse time with a large current and electro-migration limit of applicable current. Thus, with the current large scale integrated circuit (LSI) manufacturing technology, 1–5 Tpixel/s is a practical limit, where the frame rate is dependent on the number of pixels.

For the continuous video capturing CMOS image sensor types shown in Figs. 1b–c, the major speed limiting factor is the (E) [19, 20]. Theoretically, a higher speed is possible by increasing the number of parallel signal outputs. However, increasing the parallel circuit number leads to an increase of power consumption and an increase of circuit complexity. Consequently, the upper limit of the pixel readout rate of the continuous video capturing CMOS image sensor type is about 10 Gpixel/s.

On the contrary, for the burst video capturing on-chip memory CMOS image sensors, output load is not necessary to be driven at a high speed, the factor (E) is eliminated, which leads to a potential to achieve higher performances than CCD image sensors. Figure 3 shows the structures of (a) the on-chip memory CCD, (b) the on-chip memory CMOS image sensor and (c) the CMOS image sensor with stacked-chip memory with pixel-wise connections as a structure in the future. For the stacked structure in Fig. 3c the factors (C) and (D) are relaxed due to the pixel-wise connection, which leads to a higher frame rate with a higher resolution.

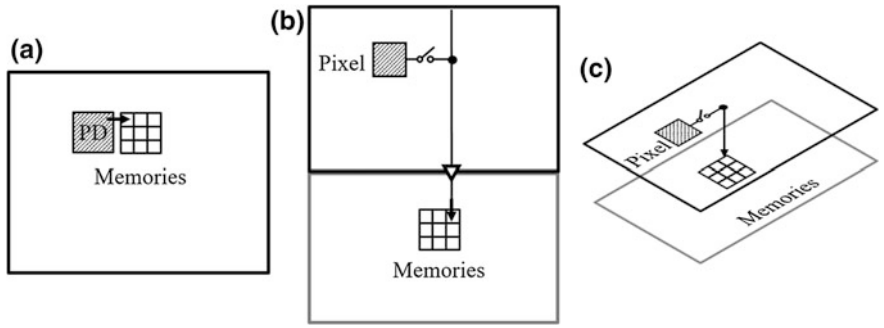

Fig. 3 UHS Image sensors with on-chip memories. **a** CCD image sensor with on-chip memories, **b** CMOS image sensor with on-chip memories, and **c** CMOS image sensor with stacked-chip memory

We have developed the on-chip memory CMOS image sensors that achieve the aforementioned requirements and put them into practical use. In this chapter, the detail of the design, key technologies and the performances of the developed on-chip memory CMOS image sensor achieving 10 Mfps and 1 T pixel/s shown in Figs. 1d and 3b, as well a the captured UHS phenomena are described.

2 Structure of the CMOS Image Sensor with On-chip Memory

Here follow the major considerations when developing the structure of the UHS CMOS image sensor with on-chip memory.

For pixel design;

- Large pixel size to receive sufficient amount of incident photons within a short integration period of less than 100 ns
- Short photo-carrier transit time due to drift and diffusion and electrical field formation inside the photodiode
- Wide spectral sensitivity response
- High resistance to smear and blooming under strong light illumination
- In-pixel circuitry (source follower, current source, amplifier, noise reduction circuit, etc.)
- Floating diffusion (FD) structure that determines the photo-electron to voltage conversion gain

For the total sensor chip;

- Die size and balance between pixel and memory numbers in order to achieve global shutter operation of reset, integration, transfer, signal readout within 100 ns simultaneously at all the pixels
- Drop of power supply voltage and rise of ground due to current during chip operation and immunities to electro-migration, stress-migration of the metal wires
- Parasitic resistance, capacitance and inductance of metal wires for driving pulses in horizontal direction
- Parasitic resistance, capacitance and inductance of pixel output wires in vertical direction and its structure

For memory design;

- Equalization of distance between pixel to memory and introduction of signal waveform shaping circuits
- Analog memory capacitor structure with a high areal efficiency and high-symmetry for minimizing the thermal noise and maximizing record length under a limited area
- Structure of analog memory with high light shield performance and low leakage current in order to avoid signal distortion during signal storing period

For signal output circuitry;

- Selection of analog or digital signal output
- Number of parallel circuits

For chip package and assembly;

- Structure to minimize impedance of metal wires especially the parasitic inductance component in the voltage supply wires
- Structure for high heat dissipation capability with high thermal conductivity in order to suppress the rise of temperature at maximum speed operation

In order to meet the requirements to the UHS video camera, the structure of the UHS CMOS image sensor was developed by taking into consideration the issues mentioned above, while all the elements are approaching near the physical limits. Under the constrain that a standard image sensor process is to be used, we decided that the CMOS image architecture with on-chip analog memory array placed on the periphery of the pixel array, where the number of memories for each pixel corresponding to the recording frames are connected to one or several pixels through a metal wire, is most adequate for this purpose. Figure 4 shows the schematic illustration of the developed UHS CMOS image sensor architecture. In this figure, an example is shown where the analog memories per pixel is connected in the pixel by pixel manner.

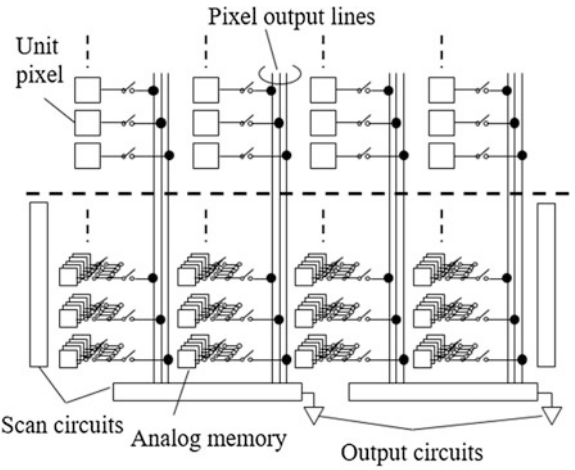

Fig. 4 Schematic illustration of the UHS CMOS image sensor architecture

It is one of the features of the developed UHS CMOS image sensor that the pixel array and memory array are separately placed on a chip, which leads to a prominent merit that the signals stored in memory are not distorted even when a strong light is used for illumination. On the other hand, in the case of UHS image sensors with on-chip CCD memory, the memories are placed close to the photodiode in pixel as shown in Fig. 3a. Due to this structure, signal distortion under a strong light illumination condition has been a challenge for the UHS CCD image sensors. In addition, for the UHS CMOS image sensor, parasitic capacitance of the wires of driving pulses for horizontal direction and vertical output wires is about one or two orders of magnitude lower than that of the CCD image sensors, as well as the supply voltage is less than about 1/3 of the CCD. By these features, a higher speed, a lower power consumption with a suppression of heat generation are achievable with the UHS CMOS image sensor.

For the optical UHS image sensors, a large pixel size is required as it is indicated by the following equation. Suppose A_{pixel} [cm^2], T_i [s], $F_{\#}$, L [lux] are pixel area, integration time, F number of lens, light illumination, and transmittance of lens T_{lens} is 100% and the wavelength λ is 555 nm, the number of incident photons per pixel in an integration time is given by the following equation [21],

$$N_{photon} = \frac{L}{683}\frac{\lambda}{hc}\frac{A_{pixel}T_{lens}T_i}{F_{\#}^2} = 4.05 \times 10^{11} \cdot \frac{LA_{pixel}T_i}{F_{\#}^2} \quad (1)$$

Here, if L = 1000 lx, $F_{\#}$ = 2, T_i = 100 ns (10 Mfps), N_{photon} = 1 for A_{pixel} = 10 μm^2 (3.16 × 3.16 μm^2) and N_{photon} = 100 for A_{pixel} = 1000 μm^2 (31.6 × 31.6 μm^2). Since the N_{photon} is proportional to A_{pixel}, a large pixel size is advantageous to receive a sufficient number of incident photons for imaging under a short integration time less than 100 ns. For the developed UHS CMOS image

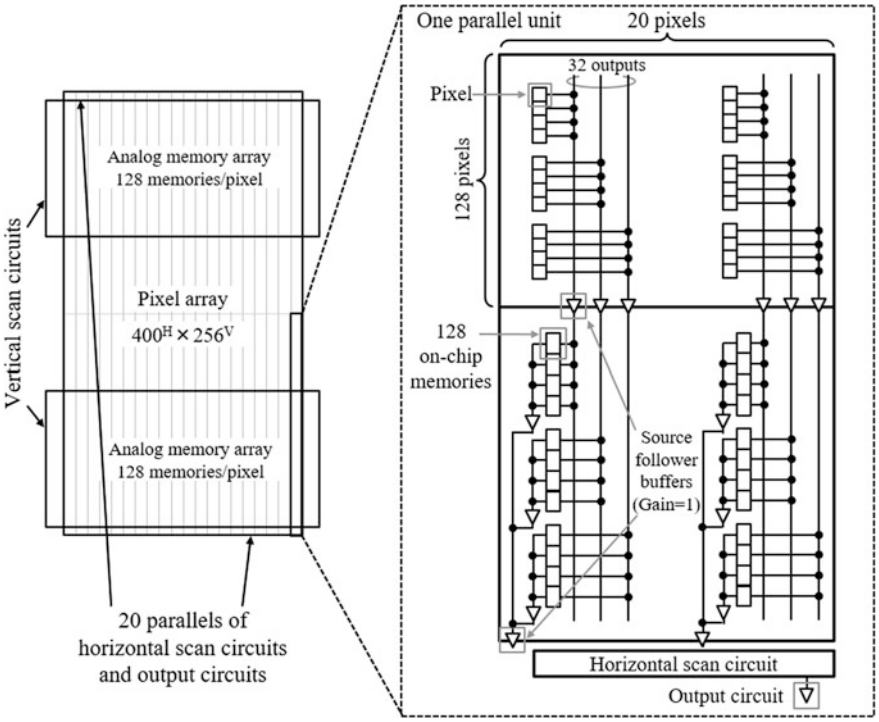

Fig. 5 Block diagram of the developed UHS CMOS image sensor chip

sensor, by considering the balance between die size, pixel number and memory number, the largest pixel pitch of 32 μm was selected.

Figure 5 shows the block diagram of the developed UHS CMOS image sensor chip [14–17]. The chip consists of a pixel array, two on-chip memory arrays, vertical scanning circuits, 20 × 2 parallel horizontal scanning circuits and 20 × 2 parallel output circuits. The number of pixels is $400^{H} \times 256^{V}$ and the pixel pitch is 32 μm. Figure 3b shows the block diagram of one parallel unit from pixel to output circuit. In order to achieve a burst video operation, each pixel has 128 on-chip memories corresponding to the number of recording frames during burst video operation. The pixel region and the on-chip memory region are spatially separated so as to allow us to independently design both the pixel and the on-chip memory layouts. With this architecture, number of pixels and memories are flexibly designed. This design also allows us to form a light shield layer on the on-chip memory region. As the memory array area is fully covered by a shield metal, signal degradation on on-chip memory due to high light illumination does not occur. This CMOS image sensor carries out both the burst video operation and the continuous video operation on the same chip. With the burst video operation, this CMOS image sensor operates at maximum speed of 10 Mfps with 128 frames in full resolution or at 20 Mfps with 256 frames in checkered-pattern half resolution.

In addition, in continuous video operation, 780 Mpixel/s, corresponding to 7.8 Kfps at full resolution is performed. During the burst video operation, the signals are readout to the on-chip memories without being output from the image sensor chip. On the other hand, during the continuous video operation, the signals are read out to the on-chip memories and are output from the image sensor chip at every frame. In order to achieve a high readout speed and a large number of pixels with a high fill factor, 32 output wires are placed in each column, thus, four pixels share one output wire. Figure 6 shows the equivalent circuit and the layout of the pixel. The pixel size is 32 $\mu m^{H} \times 32\ \mu m^{V}$. The pixel includes a pinned photodiode with a photoelectron collection time of less than 10 ns [15], a correlated double sampling (CDS) circuit to reduce the number of readout signal per frame, and current source transistors to eliminate IR-drop in output wires [22]. The on-chip memories consist of memory switches and highly area-efficient capacitors. The die size is 15 $mm^{H} \times 24\ mm^{V}$. The number of pins of package is 424.

The basic structure of this type of UHS CMOS image sensor that contains pixel region and frame memory region is similar to that of frame transfer CCD and CMOS image sensors [23, 24]. By an introduction of several key technologies such as the high-speed charge collection PD [15], multiple pixel column output lines, in-pixel CDS circuit and current sources, the first developed UHS CMOS image sensor model employing a 2-polycrystalline Si 4-metal layers (2P4M) 0.18 μm CMOS image sensor process technology has achieved signal reading out from the pixel region to the on-chip memory region within 10 ns at each frame [14]. The image signals are stored in on-chip memories and readout after the end of video capturing. Consequently, a burst video capturing over 20 Mfps has been achieved.

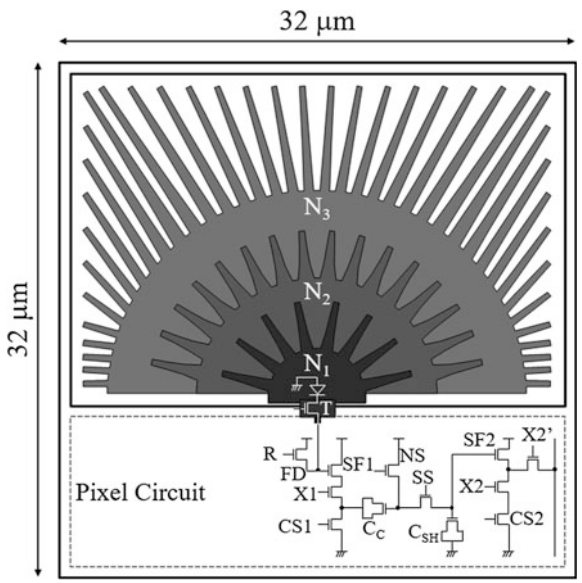

Fig. 6 Photodiode and pixel circuit

For the performance-improved chip, based on 1-polycrystalline Si 6-metal layers (1P6M) 0.18 μm CMOS image sensor process technology, several key technologies were introduced for the improvement of light sensitivity and power consumption [16, 17]. Figure 7 show the circuit schematic diagram of the analog memory. Figure 8a, b shows the cross sectional illustrations of the active and passive device components developed for the performance-improved UHS CMOS image sensor. A higher light sensitivity was achieved by the following three means; A. increasing number of photo-generated carriers to be collected under a same light illumination by increasing the fill factor and charge collection efficiency, B. increasing conversion gain by reducing the floating diffusion capacitance enabled by optimization of PD's buried n-layer, and C. increasing signal readout gain by optimizing the readout circuit. Also, the lower power consumption is to be achieved by the decrease of power supply voltage from 5.0 to 3.3 V and the reduction of source follower amplifiers' current.

Regarding point A, there are 32 pixel output lines per column, where each line is shared by 4 pixels in different rows in order to improve the signal readout speed from the pixel region to the analog memory region [14]. In the first development chip, one of the four metal layers was designated to form the 32 pixel output lines with a same pitch above the PD. For the performance-improved chip, two of the six metal layers were designated for the same usage. Consequently, the fill factor was

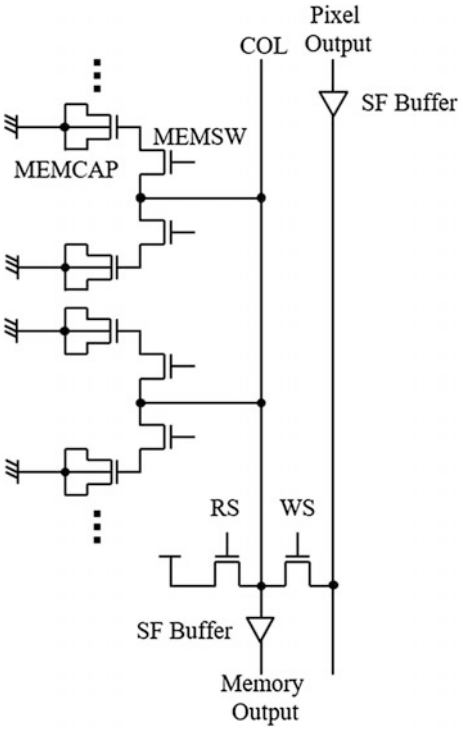

Fig. 7 Analog memory circuit schematic

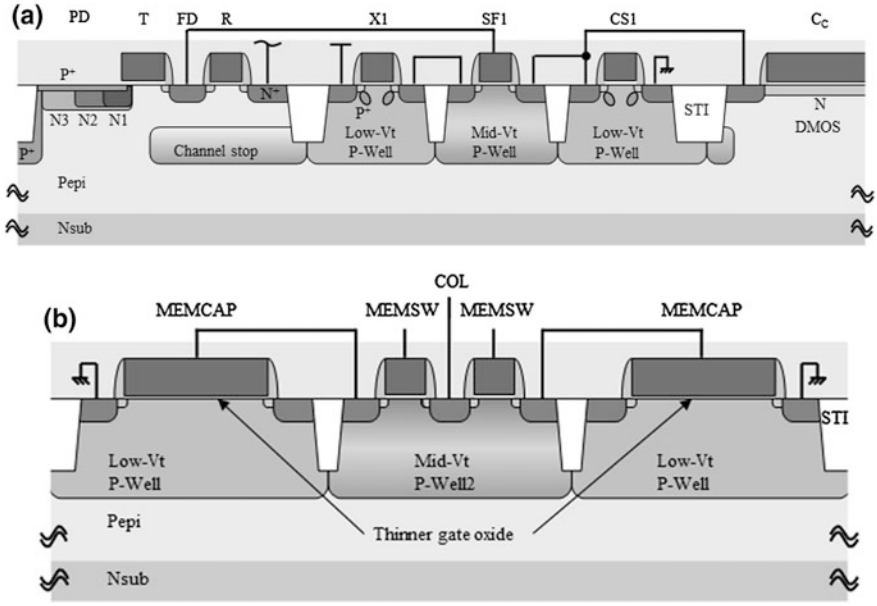

Fig. 8 Cross sectional illustrations of passive and active devices in **a** pixel and **b** analog memory developed for the performance-improved chip

improved from 37 to 55%. In addition, parasitic capacitance in output lines was also reduced due to the enlarged spacing between each line, which is also beneficial for a reduction of the current of the source follower amplifiers in pixels and in-between the pixel and memory regions under the same operation speed. In addition, by an introduction of the PD structure mentioned next, a high charge collection efficiency of 96% is to be achieved in a short charge transfer time.

Regarding point B, the PD structure achieving the full charge transfer from the large area PD within 10 ns shown in Fig. 6 was introduced [15]. In order to generate the electric field over 400 V/cm in the PD region toward the FD node to achieve high speed charge collection, two technologies were implemented; one is to form a gradient of buried pinned n-layer doping by employing the three levels of dopant concentrations and the other is to form a gradient of the width of the n-layer. The width of each sector-shaped portion of the n-layer becomes narrower from the proximal end to the distal end, making the whole shape similar to hedgehogs. By these technologies, the gradient of pinned potential of the n-layer, i.e., the electric field is efficiently and uniformly formed with a limited increase of process steps. Using process, device and optical TCAD simulations the PD design was carried out with a sufficient margin when taking into account the variation of ion implantation dosage and proximity of the lithography. By doing so, the full charge transfer within 10 ns to a single FD node with the charge collection efficiency of 96% was achieved for a large PD size of 30.00 $\mu m^H \times 21.34\ \mu m^V$ [15]. Here, with

simulation results under the condition that the incident light is uniformly irradiated to the PD area, the remaining 4% of the photo-generated charge is either recombined or drained out to n-type substrate and not accumulated in the buried n-layer [15]. The high conversion gain can be obtained by forming a small capacitance FD node on the edge of the PD. Also, the formation process of the PD junction was optimized to enhance the quantum efficiency especially for the UV-light wave band [25]. In addition, a Si wafer with 8 μm thickness and a low concentration p-type epitaxial layer on n-type substrate was employed for this sensor to compromise the near infrared light sensitivity, vertical overflow capability and crosstalk.

Regarding point C, gains of source follower buffers in the signal readout path and capacitive charge division readout from the analog memory to the signal line (COL) in Fig. 7 were improved by introducing the developed transistors and highly area efficient capacitors.

In order to implement the aforementioned features as well as to tune the voltage transfer range of the signal readout chain under the condition that the power supply voltage is reduced from 5.0 to 3.3 V while maintaining the full well capacity (FWC), the chip fabrication process technology was completely renewed from the first developed one regarding both front-end-of-line (FEOL) and back-end-of-line (BEOL) processes. The several designated passive and active device components shown in Fig. 8 were developed besides the basic high threshold voltage (Vth) and low Vth transistors and they were utilized in the developed image sensor listed as follows; the low Vth nMOS with channel stop p-type implantation and without halo implantation for reset gates in pixels, the medium Vth nMOS without halo implantation designated to the first source follower driver, the high capacitance depletion-type MOS (DMOS) capacitor for in-pixel CDS circuit with a large capacitance linearity range, the medium Vth nMOS without halo implantation for analog memory select switch with small junction and subthreshold leakage currents, and the highly area efficient MOS capacitor for analog memory with thinner gate oxide than that for 3.3 V transistors. Regarding the pixel circuit schematic, the position of X1 was changed from between the reset voltage node and the SF1 in the first developed chip [14] to between the SF1 and the CS1, and the X1 source is connected to the Cc. Subsequently, the voltage drop at X1 guarantees that the Cc operates in its linear capacitance region during the whole operation condition. The total conversion gain was improved due to the smaller FD capacitance without the bootstrap effect utilized in the first developed chip [14]. Here, an increase of the capacitance value of analog memory has several merits, such that the thermal noise is reduced, the signal readout gain from analog memory to signal line due to capacitive charge division readout is increased, and the effect of leakage current during signal holding period becomes smaller. Thus, an introduction of a capacitor with a higher area efficiency is critically important to benefit from the merits mentioned above under the same usage of chip area. In order to utilize the thinner

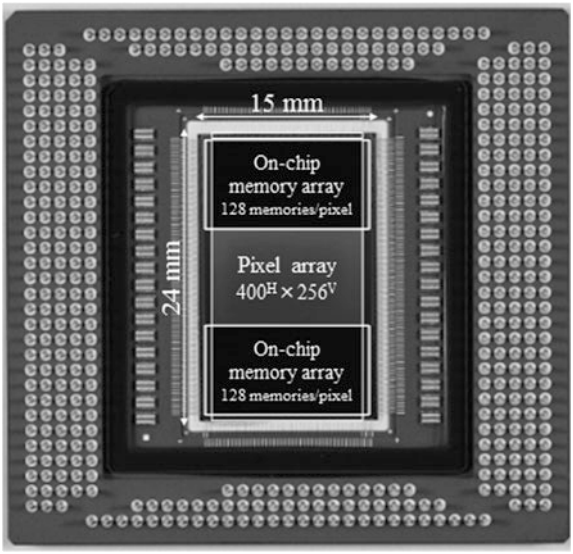

Fig. 9 Fabricated chip micrograph

gate oxide to the analog memory for this purpose, the voltage range applied to the analog memory was controlled to be below 1.8 V. In addition, a triple well process was employed for the source follower circuits in order to obtain the unity gain by removing the body bias effect.

Figure 9 shows the fabricated chip micrograph of the developed UHS CMOS image sensor with on-chip memory [16, 17]. Besides the numbers of pixels and on-chip memories, the positions of PADs and the chip package were identical as those of the first developed sensor chip. It is also beneficial for an easy substitution of the image sensor chips of the formerly developed UHS video cameras. The on-chip memory array regions are fully covered by the shield metal, so that the stored signal is not affected by incident light. The quartz glass was used as the package lid for the chip performance measurement described in the next section.

3 Performances of the Developed CMOS Image Sensor with On-chip Memory

Figure 10 shows the photoelectric conversion characteristic of the fabricated UHS CMOS image sensor chip. The input-referred FWC of 10,000 e^- was obtained. The major noise source of the developed sensor chip is the thermal noise at the on-chip memory, as it was the same case in the first developed chip [14]. By the increase of conversion gain, signal readout gain and the on-chip memory capacitance, the total input referred temporal noise of about 5 e^-_{rms} was obtained.

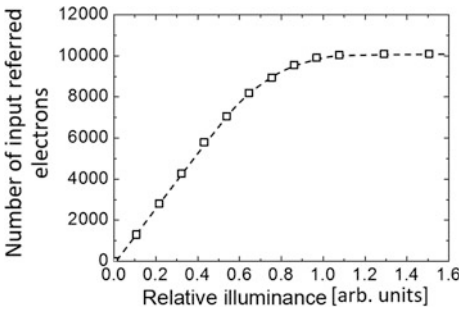

Fig. 10 Photoelectric conversion characteristic

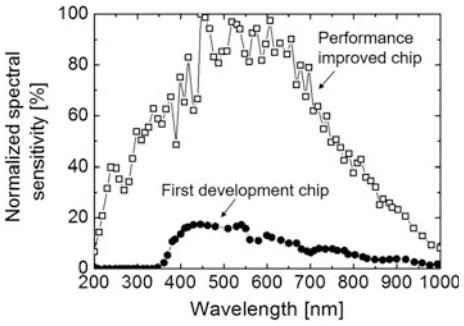

Fig. 11 Normalized output referred characteristic

Figure 11 shows the output referred spectral sensitivity characteristics of the performance-improved chip and first developed one. The improvement by factor eight of the light sensitivity was confirmed at the wavelength of around 550 nm. Here, about four-times improvement of light sensitivity is attributed to the increases of the fill factor, the charge collection efficiency and the conversion gain, and the rest is attributed to the improvement of signal readout gain, respectively. Also, the spectral sensitivity range was extended to the UV-light wave band for the performance-improved sensor chip due to the employed PD junction formation technology [25].

This is beneficial to capture ultra-high speed phenomena with UV-light, such as the dynamic behavior of plasma and flames. The spectral sensitivity of polarized light parallel and perpendicular to the pixel output lines above the PD was measured, and the results suggest that the polarization effect was negligibly small across the whole sensitive wave band.

The characteristic of image lag is shown in Fig. 12. In this experiment, under the frame period of 50 ns, the incident light from a 635 nm laser diode was cut off, just before the pulse rising timing of the transfer gate at the frame number 1, so that the incident light was kept off for the subsequent frames. The vertical axis is the ratio of output signal at each frame to that of the frame number 1, i.e., the image lag. Here, the output signal of the frame number 1 was about 3/4 of the saturation level. The output signal at frame numbers 2 and higher were the same as the dark level,

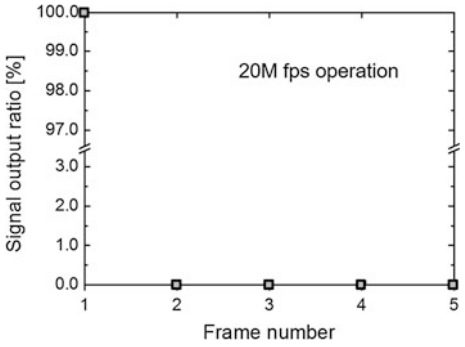

Fig. 12 Measured image lag at 20 Mfps

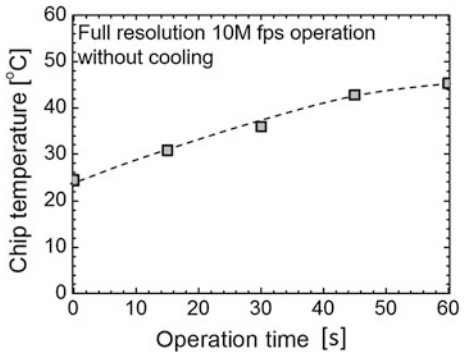

Fig. 13 Chip temperature as a function of operation time

indicating that the image lag was under the detection limit even at 20 Mfps operation [15].

In Fig. 13 the chip temperature is plotted as a function of the operation time. The temperature was measured by the on-chip thermometer during the 10 Mfps operation with burst full pixel mode under room temperature. No cooling system was used. The measured chip temperature was under 50 °C even after 60 s operation time. This result indicates that the developed image sensor chip is capable of operating at the maximum pixel readout speed while waiting for the arrival of trigger signal for the video capturing. This ability is critically important for capturing non-repeatable UHS phenomena.

Figure 14 presents the power consumption of the performance-improved image sensor chip at various frame rate with burst full and half pixel modes. Due to the reduction of the power supply voltage, the power consumption at 1 Tpixel/s operation was reduced by half, i.e., 10 W compared to 20 W of the first developed chip [14]. The performances of the developed UHS CMOS image sensor are summarized in Table 1.

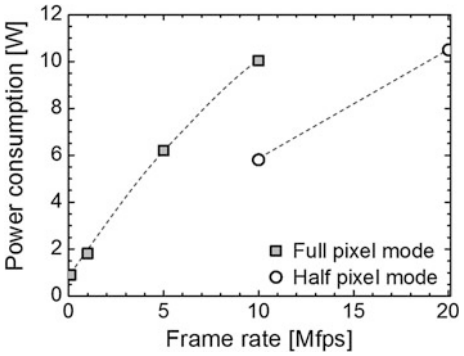

Fig. 14 Power consumption as a function of frame rate with burst full pixel and half pixel modes

Table 1 Summary of the developed image sensor performance

Process technology		1P6M 0.18 μm CMOS with pinned photodiode			
Die size		15 mm^H × 24 mm^V			
Pixel size, photodiode size		32 μm^H × 32 μm^V, 30.00 μm^H × 21.34 μm			
# of pixels	Total, effective	400^H × 256 ^{V}, 400^H × 250^V			
Aperture ratio		55%			
# of parallel outputs		40			
# of PADs		424			
# of frames in burst operation		Full	128	Half	256
Maximum frame rate	Burst		10 Mfps (1 Tpixel/s)		20 Mfps (1 Tpixel/s)
	Continuous		7.8 Kfps (780 Mpixel/s)		15 Kfps (780 Mpixel/s)
Conversion gain (input referred)		112 $\mu V/e^-$			
Full well capacity		10,000 e^-			
Power consumption		10 W at 1 Tpixel/s			
Image lag at 20 Mfps		Below the measurement limit			
Spectral sensitive range		200–1000 nm			
Full charge transfer time		≤ 10 ns			

4 Camera with On-chip Memory CMOS Image Sensor

The first developed UHS CMOS image sensor with on-chip memory was employed in the commercialized high speed video camera: HPV-X [26]. This high-speed video camera has been utilized to capture what had not been seen before [5–10]. By the development of dedicated process technologies, eight times photosensitivity improvement and 50% power consumption reduction were simultaneously achieved [16, 17], and the performance-improved chip has been utilized in the

commercialized high-speed video camera: HPV-X2 since 2015 that offers 10 Mfps with ISO 16000 photosensitivity. Due to the improved photosensitivity, clear images can be taken and analyzed even under low light conditions, such as under a microscope as well as in capturing of UHS light emission phenomena [27–31].

Figures 15, 16 and 17 are some examples of images taken by this high-speed camera. Figure 15 shows a series of images of a crack generation of glass. A glass plate of 1 mm thickness was shot with a plastic bullet of 6 mm diameter at a speed of 20 m/s. The video was taken at 5 and 20 Mfps. The trigger signal was generated by the intercept of a laser by the bullet. The light intensity of the flash lamp was 76,000 W and the light-emitting time was 2 ms. The experimental set-up is illustrated in Fig. 15a–c show the series of images: at first, the crack extended radially

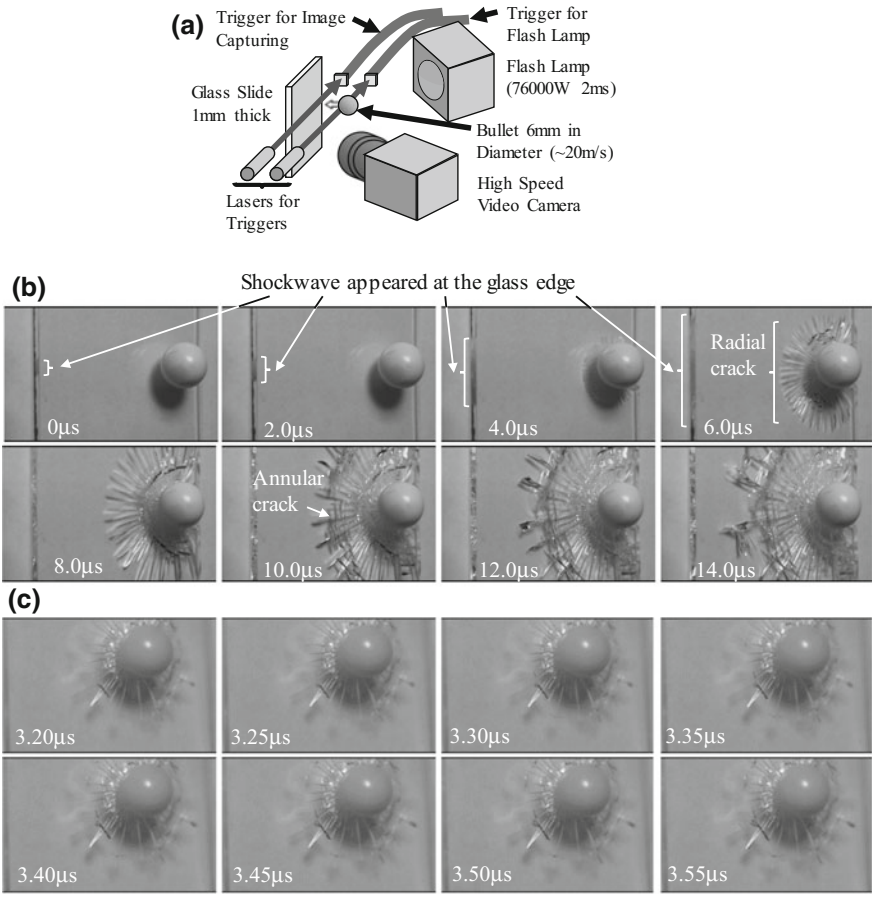

Fig. 15 **a** Schematic illustration of the video capturing of glass crack generated by bullet shooting and captured images by **b** 5 Mfps full resolution mode and **c** 20 Mfps half resolution mode, respectively. The corresponding movies are available online

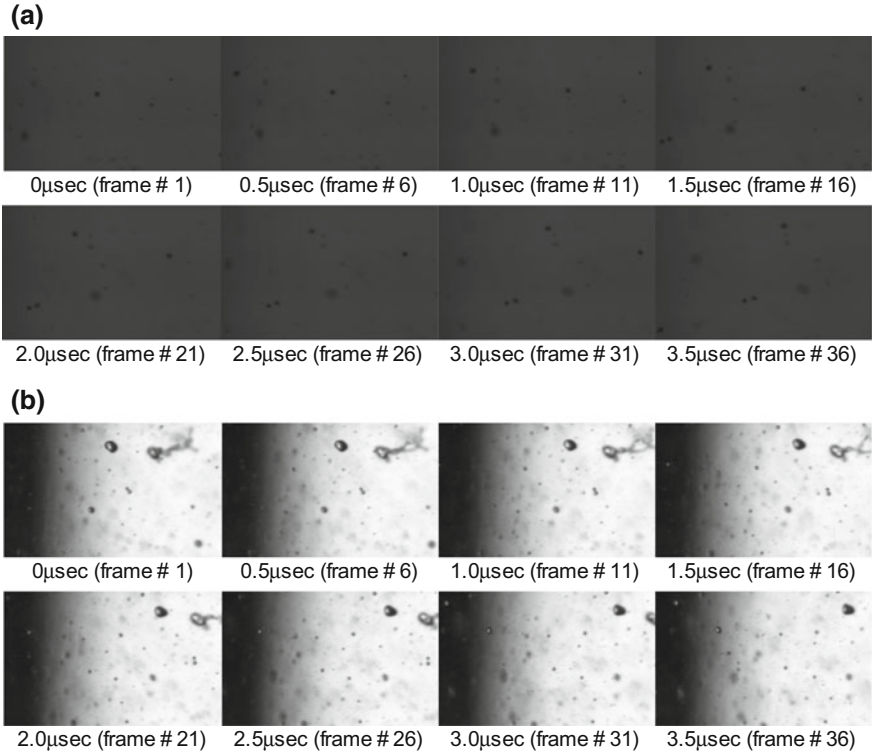

Fig. 16 Images of water mist injected from an air brush taken at 10 Mfps burst half pixel mode by **a** first developed chip and **b** performance-improved chip. The corresponding movie is available online

from the point of impact, shock waves were reflected at the edges of the glass, and after that the crack developed annularly from the position around the meeting points of reflected shockwaves. Crack branching at several spots was also seen. From these images, we estimated that the speed of the crack was about 1 km/s.

Figure 16 shows the images of water mist ejected from an air brush captured at 10 Mfps burst half pixel mode operation. Figure 17 shows a series of images of a breakdown of Al/SiO_2/n–Si capacitor with an oxide film of 100 nm thickness, induced by the gate voltage ramped up to and kept at 100 V. Images were captured at 1 Mfps burst half pixel mode operation. Figures 16a and 17a are the images taken by a camera with the first developed chip (HPV-X), while Figs. 16b and 17b are those taken by a camera with the performance-improved chip (HPV-X2). The effectiveness of sensitivity improvement is clearly recognized by the higher signal-to-noise ratio (SNR) images captured by the developed sensor. The higher sensitivity is greatly useful for capturing microscopic UHS phenomena, capturing images with a deeper depth of focus, and capturing light emitting objects.

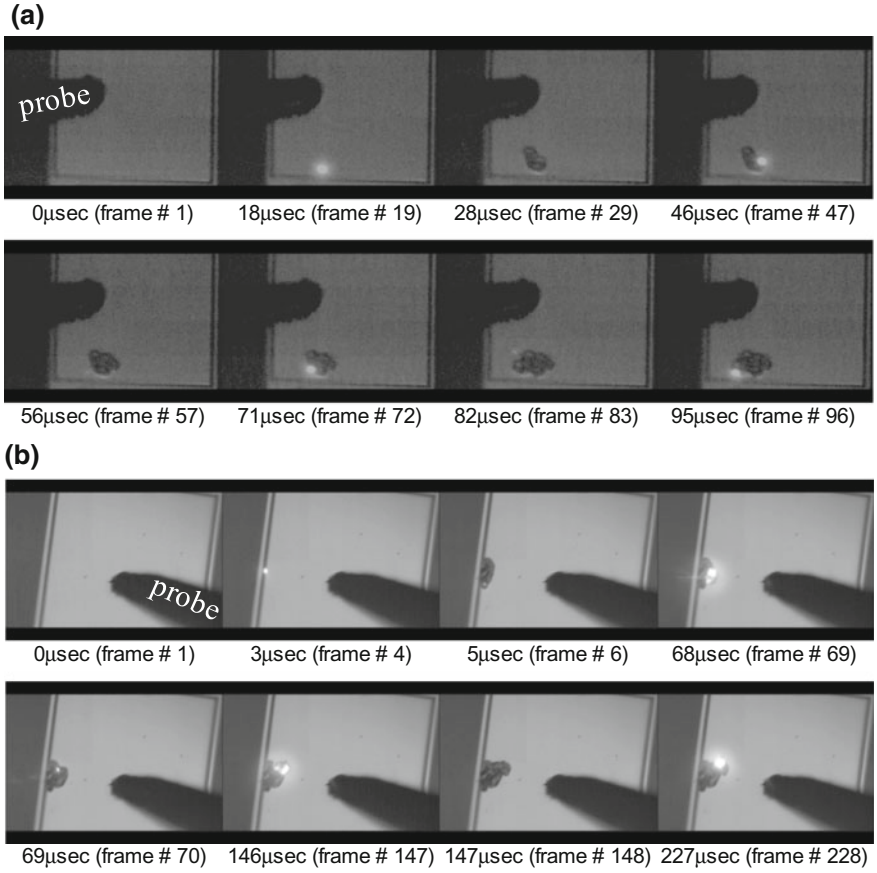

Fig. 17 Images of the electric field breakdown in Al/SiO_2 (100 nm)/n–Si MOS capacitor taken at 1 Mfps burst half pixel mode by **a** first developed chip and **b** performance-improved chip

5 Summary and Future Perspective

UHS CMOS image sensors with on-chip analog memories placed on the periphery of a pixel array for the visualization of UHS phenomena are overviewed. The developed UHS CMOS image sensors with $400^{H} \times 256^{V}$ pixels and 128 memories/pixel exhibit readout speed of 1 Tpixel/s, leading to 10 Mfps full resolution image capturing with consecutive 128 frames, and 20 Mfps half resolution image capturing with consecutive 256 frames. By the development of dedicated process technologies such as the large area high speed charge collection PD, the DMOS capacitor for in-pixel CDS circuit, the high capacitance MOS capacitor for on-chip analog memory and the designated threshold voltage MOS transistors for SF based signal readout chain with 3.3 V power supply voltage, eight-times higher photosensitivity and 50% reduction of power consumption were simultaneously

achieved. The developed UHS CMOS image sensor and high speed video camera are effective to capture and analyze various UHS phenomena.

From now onward, the main factors that obstruct higher speed and higher pixel- and memory-counts are as follows:

- Inductance of package-interconnect and pad-bonding-line
- Power consumption and heat generation
- Electro-migration in metal wires

And the challenges to be tackled in order to overcome these obstacles are:

- A large number of on-chip memories with high area efficiency capacitors
- Low-heat-generation and heat-sink
- Short interconnect by stacked-chip

Looking at the history, drastic improvements in the science and technology developments were driven to occur when extraordinarily advanced measurement and analysis technologies emerged.

UHS imaging technology is now expected to be utilized more than ever for the technological innovation of a wide range of science and engineering fields such as material science, electronic engineering, nanotechnology and life sciences.

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