# Chapter 13
# FDSOI Technology, Advantages for Analog/RF and Mixed-Signal Designs

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## 13.1 General Considerations Regarding FDSOI Technology

The race on the More Moore integration scale has brought several major limitations for efficient process integration starting from the 40 nm technology node, in CMOS planar solutions. It had appeared that the transistor channel was more and more difficult to control in terms of electrostatics, and a lot of process engineering methods (e.g., silicon strain) have been needed in order to provide transistors with good carrier speed and decent electrical characteristics. Starting from the 28 nm node, the obvious solution for transistors with increased electrical performances was the use of fully depleted channel devices. Two integration paths have been chosen in the semiconductor industry for these fully depleted devices: fully depleted silicon on insulator CMOS (FDSOI) and FinFET CMOS devices. The fundamental carrier semiconductor equations are similar; nevertheless, the process integration is very different. This paper will focus on planar FDSOI CMOS technology features as integrated by STMicroelectronics [1, 2] and its specific features for analog, RF, and mmW integrations.

Figure 13.1 gives a generic cross section of a FDSOI CMOS device. We call this technology Ultrathin Body and BOX (UTBB) FDSOI CMOS, as the active device is integrated atop an ultrathin layer of buried oxide (BOX). The transistor active conduction area (also called silicon film) is very thin as well. In the 28 nm UTBB FDSOI technology from ST, the BOX thickness is 25 nm and the film layer is 7 nm. This *planar* topology's direct implications are the following: thanks to the

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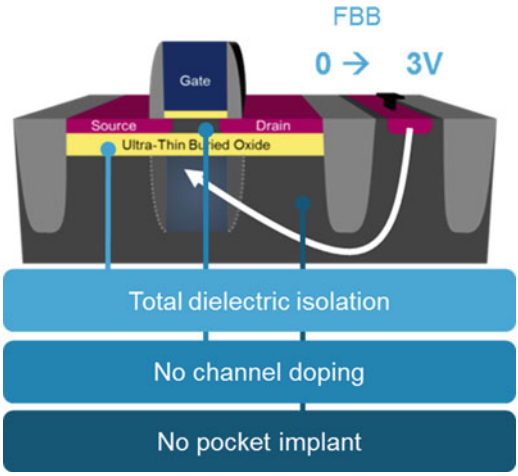



**Fig. 13.1** Generic cross section of an UTBB FDSOI transistor

SOI BOX layer, the transistor gets total dielectric isolation. No channel doping is needed as, thanks to the thin silicon film, the channel is fully depleted. Also enabled by this topology, no pocket implants are needed for the source and drain, which enhances naturally the analog/RF transistor's behavior. Another implication of the thin layer consisting the BOX is the fact that the front side transistor's electrostatics can be controlled through the area underneath the BOX, also called transistor body. By applying a voltage on the transistor body (hence underneath the BOX), one can change or modulate the threshold voltage of the main (front side) transistor. We can see this device as well as a planar dual-gate device: the front gate is the regular one (like in bulk technology), and the second one comes from the body tie, with the BOX as the backside gate oxide. As the thickness report of the front and back gate oxides is about 10, we can state the front side transistor's transconductance Gm is ten times bigger than the one of the backside gate.

In terms of manufacturing, the 28 nm FDSOI CMOS process from STMicroelectronics is sharing most of process steps with the equivalent 28 nm *bulk* technology from ST. It is a modified bulk 28 nm high-K metal gate LP process using the same back end of the line and same gate module. Several process steps, specifically channel implants, halo implants, and masking levels are removed compared to the traditional 28 nm bulk technology because of the undoped FDSOI channel. There is less than 20% change with respect to a classical CMOS bulk flow; the two extra specific steps are related to the hybridation and raised source/drain epitaxy. At this node, more than 10% of the process steps and seven masks are saved, resulting in an overall manufacturing process cost saving of 10% [3].

## 13.2 Electrical Features of Active Devices in 28 nm FDSOI CMOS Technology and Comparison with an Equivalent Bulk Technology

### *13.2.1 Different Types of Active Devices in FDSOI Technology and Body Biasing Effect on the Threshold Voltage*

In order to get a good understanding of the different types of FDSOI transistor's specific features, let's first start with a small reminder from planar *bulk* CMOS transistors.

Figure 13.2 gives a cross section of NMOS and respective PMOS transistors in a regular *bulk* CMOS technology. The potential threshold voltage ($V_T$) modulation can be obtained by the body bias tuning through the application of a voltage on the respective transistor's body ties. In such technologies, this is very limited by the threshold voltage of the parasitic source/drain diodes toward the respective transistor body. As this voltage is around 0.6 V, the effective safe body biasing voltage range spans only from 0 to 0.3 V (modulus). The body factor in bulk technologies is also quite limited ( 45 mV/V); hence, the total possible variation of the threshold voltage is limited in bulk technologies to only few tens of mV.

Figure 13.3 presents cross sections of the respective NMOS and PMOS transistors in the 28 nm UTBB FDSOI technology. The darker side of the respective NWells corresponds to the deep-NWell layer.

Regarding the regular VT (RVT) transistors (see the bottom part of the figure), one can observe the specific UTBB FDSOI topology, with the raised sources and drains and the thin BOX isolating the front side transistor for its body. If we get interest on the VT modulation through body bias biasing, one can see that now the only limiting parasitic diodes are those between deep NWell to P-substrate for NMOS and respectively embedded PWell to deep NWell for PMOS devices. These are Zener type of diodes, with an opening voltage around modulus of 3 V. We hence can do a very efficient body biasing on these RVT devices, called here reverse body biasing (RBB), the effective biasing voltage range being from roughly 0 to 3 V (modulus).

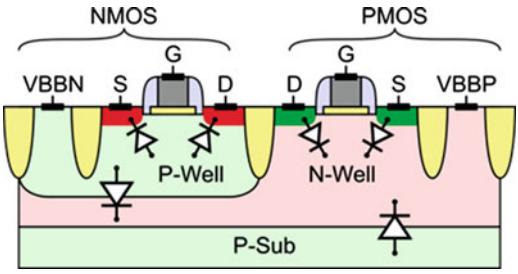



**Fig. 13.2** Cross section of CMOS transistors in a regular bulk technology

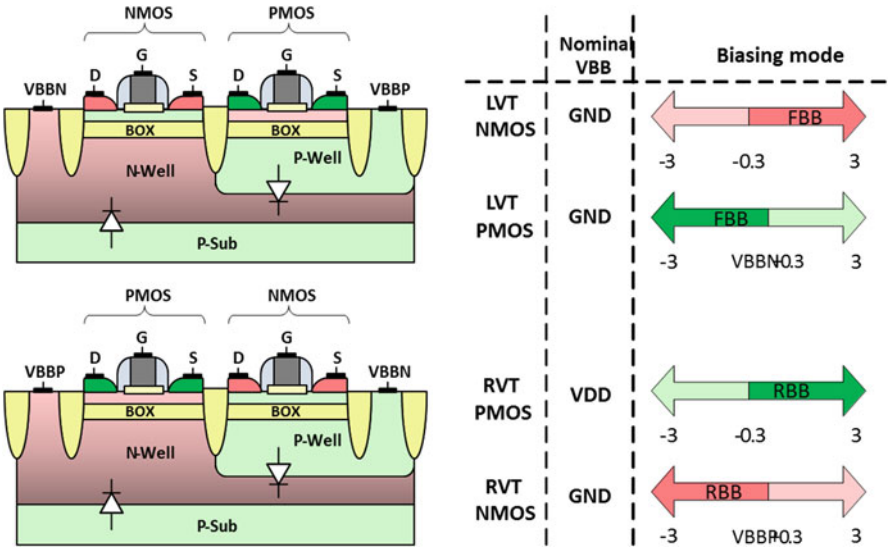



**Fig. 13.3** Cross section of 28 nm UTBB FDSOI CMOS transistors: *Top* – Low VT (LVT) transistors; *Bottom* – Regular VT (RVT) transistors

Let's now focus on the low VT (LVT) devices on the upper part of Fig. 13.3. These devices are also called "flipped-well" devices, as in order to obtain the lower VT characteristics, the process engineering has proposed a solution when the NMOS devices lay on an NWell body, and respectively the PMOS on a PWell body. In an equivalent way, we can apply forward body biasing (FBB) on these devices, with also an equivalent body voltage variation from roughly 0 to 3 V (modulus).

The body factor for both families of devices (RVT and LVT) is much larger in FDSOI than in an equivalent body node, here in 28 nm being 85 mV/V. This argument together with the very wide body biasing range result in an unprecedented wide variation of the threshold voltage (VT) of around 250 mV, as depicted in Fig. 13.4.

### *13.2.2 FDSOI Transistors' Analog Features*

When we were following the historical nm downscaling of the CMOS bulk road map, the analog designers had to get used with the fact that the analog behavior of the respective transistors was getting worse and worse with the downscaled technology node. This was inherent from the planar CMOS bulk transistor topology, in the race for faster and faster digital behavior and/or low power. Some foundries,

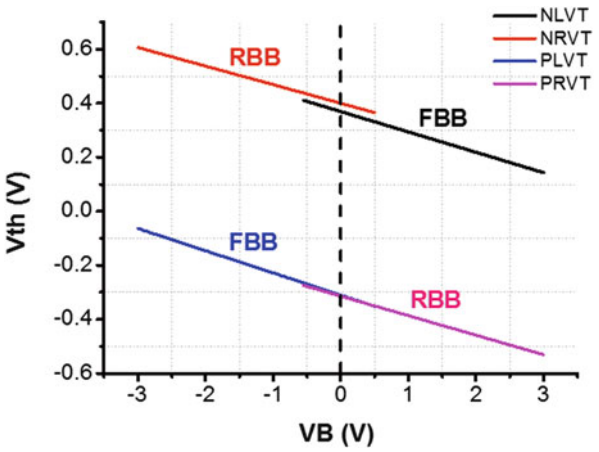



**Fig. 13.4** Threshold voltage (VT) variation with respect to body biasing voltage for RVT and LVT devices in 28 nm FDSOI technology

like ST, had solved that in the 65nm node by introducing a specific analog transistor called HPA (high-performance analog) which was overcoming this problem by eliminating the transistor pockets. In the 28 FDSOI planar technology, thanks to the thin film structure, we do not need transistor pockets, and hence we can recover nice native analog behavior.

FDSOI hence brings several advantages to analog designers in terms of efficient short channel devices, improved analog performances, and lower noise variability. For comparison, in the several following figures, we show comparison of the 28 nm FDSOI technology with its equivalent 28 nm LP *bulk* technology, both from STMicroelectronics.

Figure 13.5 shows major improvements of FDSOI vs. bulk solution regarding analog gain and VT matching parameter. For example, in 28 nm FDSOI, an LVT NMOS device of size 1 μm/100 nm can show an excellent analog performance of DC gain of 80 and a sigma (VT) of only 6 mV.

Figure 13.6 shows that FDSOI provides higher Gm for a given current, with respect to the equivalent 28 nm LP bulk node. This, combined with the lower parasitic capacitances coming inherently from the SOI insulation, permits to achieve higher operation bandwidths for a given current consumption or – if working at constant bandwidth – lower power consumption.

The variability in planar FDSOI technologies is improved with respect to an equivalent LP bulk node, thanks to the simpler manufacturing process steps. This helps a lot as well for the noise behavior, as it can be seen in Fig. 13.7. As an example, for an LVT NMOS of size 1 μm/120 nm biased at a 1 μA drain current, we get 1.5 dB lower 1/f noise in FDSOI than in bulk. This is a typical value of the main branch current for a LNA in low GHz frequencies.

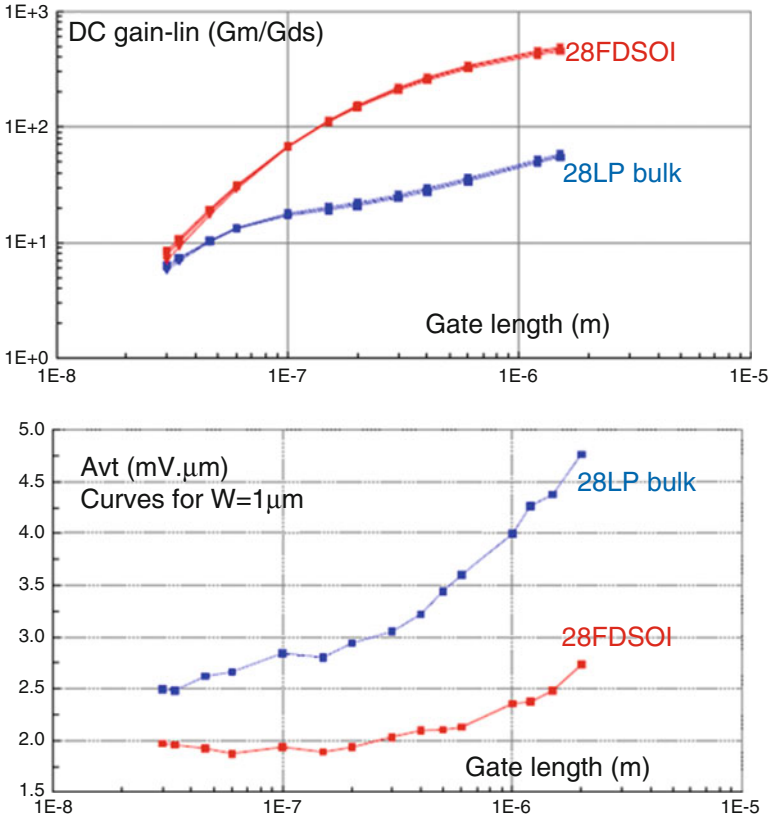



**Fig. 13.5** Analog gain (Gm/Gds) and matching (AVT) for NMOS LVT devices in 28 nm FDSOI technology (*red*) and comparison with 28 nm LP bulk (*blue*)

### *13.2.3 FDSOI Transistors RF and mmW Features*

Thanks to the deep submicron lithography, this technology node provides very fast transistors. The intrinsic devices (FEOL plus Metal1 contact) in the LVT flavor, for example, here NMOS, show $f_T$ and $f_{max}$ superior to 300 GHz (Fig. 13.8).

We can hence distinguish two types of dimensioning and biasing strategies, depending on the operation frequency.

If we talk about RF operation frequency below 10 GHz, we can then work with a transistor length of 100 nm. Performances such as a maximum available gain MAG = 12 dB and NFmin 0.5 dB can be obtained for a current density: 125 µA/µm (here $W = 1$ µm).

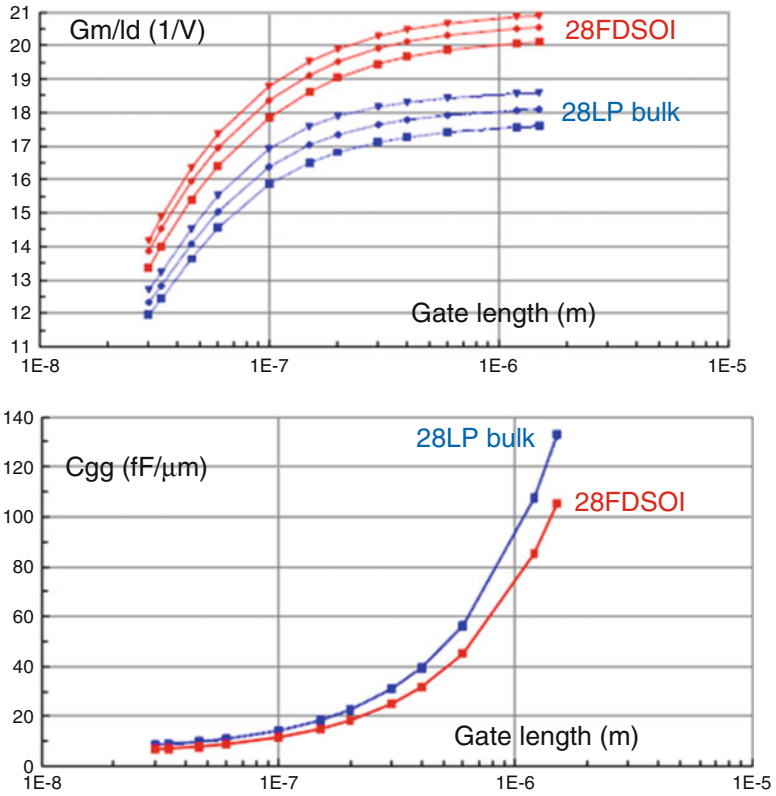



**Fig. 13.6** Improved analog performance (Gm/Id and total gate capacitance Cgg) for NMOS LVT devices in 28 nm FDSOI technology (*red*) and comparison with 28 nm LP bulk (*blue*)

Going higher in frequency will then request working with the minimum transistor length of 30 nm. Here, for example, for a 60 GHz operation frequency, a MAG = 12 dB and NFmin 1.3 dB can be obtained, when working at a current density of 200 µA/µm. This value is 33% lower than in 28LP bulk.

Deep submicron CMOS has the counterpart of very low and dense back end of line, with a large number of metal layers. This can be seen as a limiting point for mmW design; nevertheless, the eight metal layers of the discussed technology permit to obtain very decent values for the integrated passive devices. This is enabled by the operation in a low parasitics environment coming with the SOI technologies. Several examples can be cited here: an inductor of $L = 0.5$ nH with a $Q$ factor of 18 at 10 GHz, a varactor of $C = 50$fF with a $Q$ factor of 20 at 20 GHz and a 50 Ohm transmission line of 08 dB/mm losses at 60 GHz.

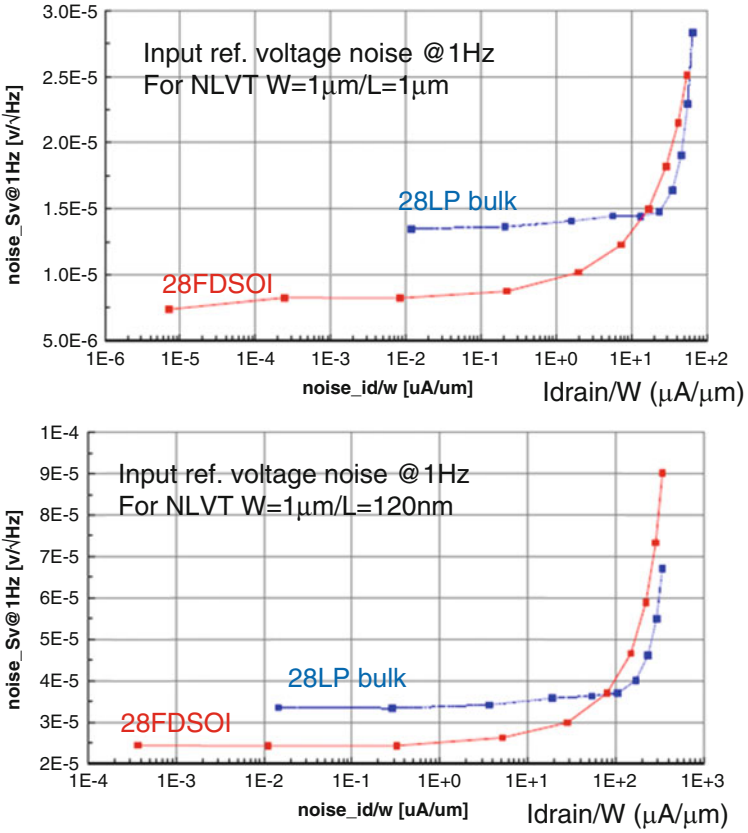



**Fig. 13.7** Noise behavior for NMOS LVT devices in 28 nm FDSOI technology (*red*) and comparison with 28 nm LP bulk (*blue*)

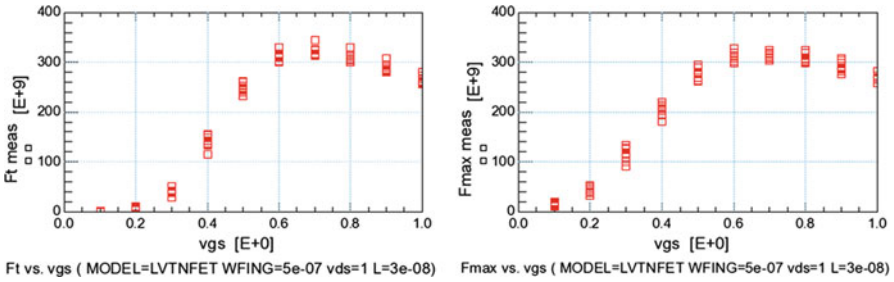



**Fig. 13.8** High-frequency behavior ($f_T$ and $f_{max}$) of LVT NMOS 0.5 µM/30 nm in 28 nm FDSOI CMOS

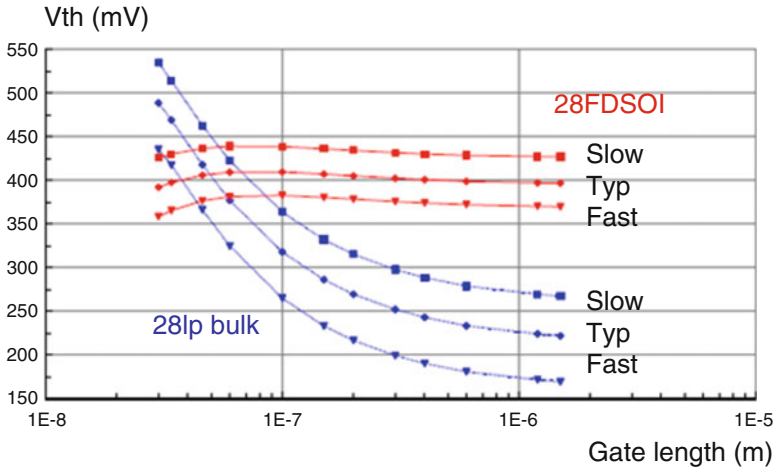



**Fig. 13.9** VT process corners for LVT NMOS devices, comparison between 28 nm FDSOI CMOS and 28 nm LP bulk

### *13.2.4 FDSOI Transistors' Mixed-Signal Features*

In terms of process variability, we experience in FDSOI tighter process corners and less random mismatch than competing processes at the same lithography node. The benefits become immediate in terms of simpler design process and shorter design cycle, hence improved yield or improved performance at given yield. Figure 13.9 illustrates this for the VT parameter.

Body biasing allows for VTH reduction by tuning, as depicted in Fig. 13.10 [4]. This result is an unprecedented quality of analog switches. One can observe the exceptional flat behavior of the CMOS switch resistance in the case of the FDSOI integration using body biasing, its absolute value being much lower than the one in bulk. We experience here compounding benefits: a smaller resistance yields a smaller switch with a more compact layout, hence with lower parasitics, which finally gives an even smaller switch. This feature is key for high-performance data converters and other switched-capacitor circuits.

Lower junction capacitances as those experienced in FDSOI make a substantial difference in high-speed circuits. They permit drastic reduction of self-loading in gain stages and a significant reduction of switches self-loading. This yields a twofold benefit: not only incremental improvements, but mostly they allow the designer to use circuit architectures that would be infeasible/inefficient in bulk technologies.

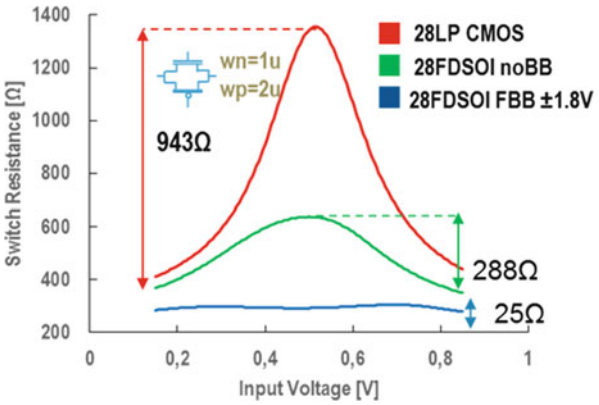



**Fig. 13.10** LVT CMOS switch resistance variation wrt input voltage, comparison between 28 nm FDSOI CMOS and 28 nm LP bulk

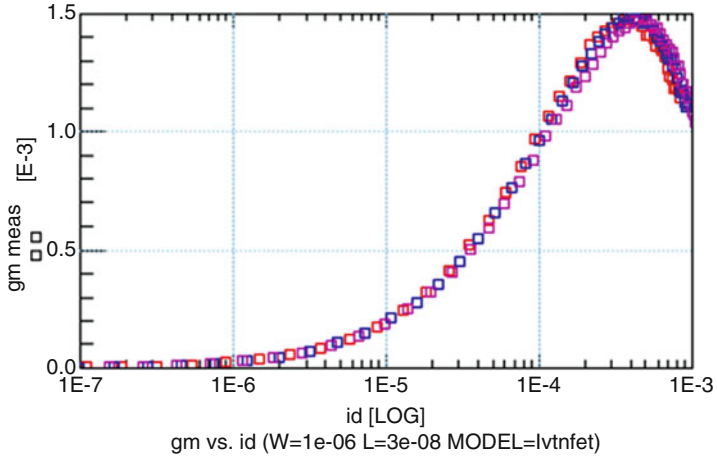



**Fig. 13.11** 28 nm FDSOI LVT CMOS 1 μm/30 nm transistor measured Gm for different drain currents, Vbody varies from 0 to 2 V, Vds = 1.1 V

### *13.2.5 FDSOI Transistors' Feature Variation with the Body Biasing Tuning*

The semiconductor physics in FDSOI predict that the main design transistor's parameters (such as Gm or $f_T$) do not depend on the body biasing variation, for an operation at constant current.

The following two figures illustrate this aspect by providing measurement curves for different devices (Figs. 13.11 and 13.12).

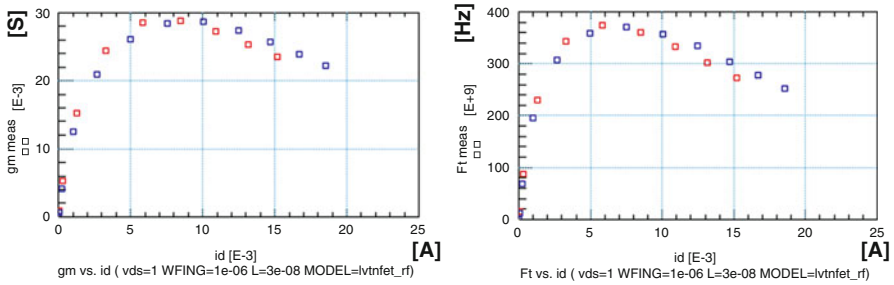



**Fig. 13.12** 28 nm FDSOI LVT CMOS 1 μm × 20 fingers/30 nm transistor* measured Gm and $f_T$ for different drain currents, Vbody varies from 0 to 2 V, Vds = 1.1 V. ()* intrinsic device (FEOL plus Metal 1)

## 13.3 Design Example of an Analog/RF Building Bloc with FDSOI Specific Features

This section presents a typical bloc used in most of wireless communication IC's, and it highlights the main benefits that such a design can take from a 28 nm FDSOI integration. We hence discuss in this section the integration of analog filters with several 100's MHz bandwidth. In the real life of a SoC, they suffer from process, voltage, temperature (PVT), and aging variations, which affect system operation and directly influence overall applicative behavior. All such blocs need to be tuned or trimmed inside the SoC, in order to strictly control independently several of its parameters: cutoff frequency, linearity, and noise, all these for an optimal power consumption.

Since more than 10 years now, in deep submicron CMOS processes, it is very practical and straightforward to implement inverter-based analog functions: They yield to simple and compact solutions, which nicely scale with technology nodes. The example here discusses about an analog low-pass Gm-C filter with cutoff frequencies in the range of hundreds of MHz. The typical implementation of such topology is realized with fixed capacitors, then the filter parameters are varied by tuning the different filter Gm's; see Fig. 13.13. Each filter transconductor Gm is composed of several invertors operated in the gain region (analog operation with biasing point on the middle of the out/in transfer function), as, for example, presented in [5].

In traditional bulk CMOS technologies, the only tuning way of such inverter-based topologies is to define as unique tuning knob the local Vdd of the analog operated inverters. A dedicated LDO with controlled output voltage is, for example, implemented between the global system Vdd and the bloc local Vdd, generating this tuning value. This is generating extra power consumption and reduced voltage headroom (hence linearity) for the bloc to be controlled. In general, with only one tuning knob for such blocs and several parameters to tune (cutoff frequency, linearity, etc.),

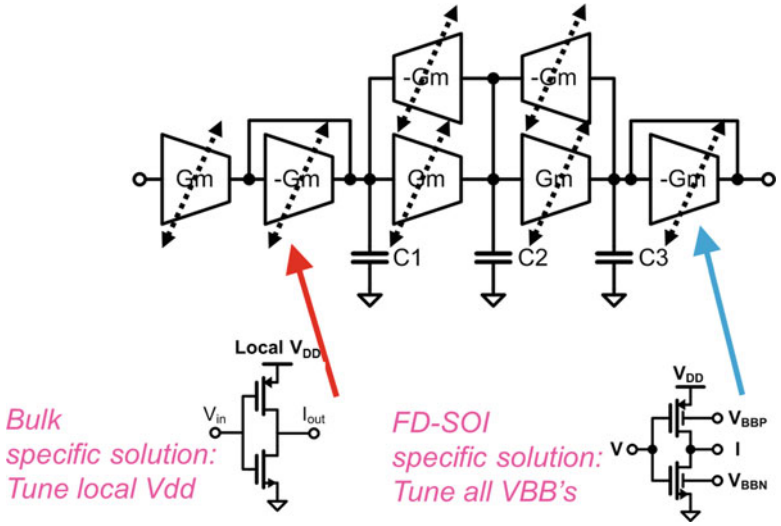



**Fig. 13.13** Typical tuning methods in bulk and FDSOI CMOS integration for analog Gm-C filters

the designers have to take a very large power consumption margin in order to be able to satisfy the system level specifications in all operation conditions.

In FDSOI CMOS technologies, as presented in the previous section, there are two available and independent new tuning knobs in the system: the local bodies of the NMOS and respective PMOS transistors. Thanks to the very wide tuning voltage range of these individual body biases knobs, there is an independent variation of the respective transistors' threshold voltages, hence generating at system level a variation of the system level parameters, and this over a very wide range. Moreover, this permits also an *independent* tuning of the different system level parameters (e.g., cutoff frequency and linearity).

Another consideration can be made here regarding the parasitic influence of a tuning control loop on the main signal path operation of a system. In classical bulk CMOS implementation, the loop control signal is somewhere either on the signal path or with direct parasitic influence on the signal path. In these FDSOI tuning systems, the tuning control signal are on the body ties, which are isolated by a buried oxide layer with respect to the signal path main operation, hence all parasitic signals on these signals have much less influence on the main signal path operation.

All these will be illustrated in a simple intuitive way in the following paragraphs.

In a bulk CMOS implementation, the inverter transconductance variation (hence the global filter transconductor variation) is obtained by the local Vdd variation, as depicted in Fig. 13.14. In this example, the capacitor values are fixed, meaning that the global transconductor variation is directly proportional to the one of the filter cutoff frequency. Unfortunately, this transconductance variation will also imply a variation of the linearity; hence, a larger design margin will have to be taken in order to cover these two variations.

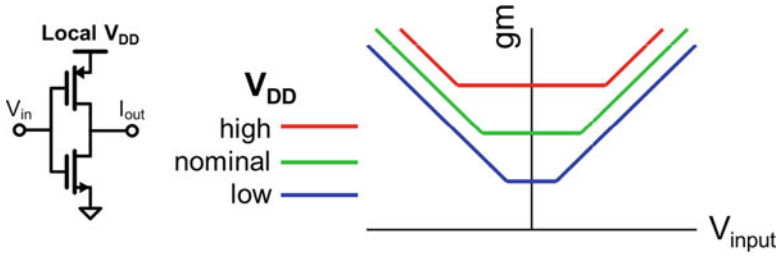



**Fig. 13.14** Bulk CMOS operation: inverter-based design tuning through local Vdd variation

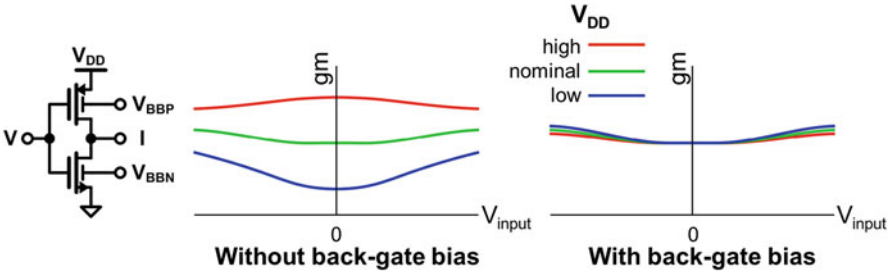


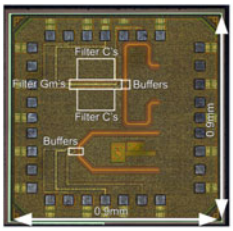

**Fig. 13.15** FDSOI CMOS operation: inverter-based design tuning through independent Vbody_N and respective Vbody_P variation

In Fig. 13.15, we show an FDSOI CMOS typical implementation for this filter tuning strategy. The inverters constituting the Gm-C filter have all a global Vdd, which is the global (system) Vdd, and in any ways it is not used for tuning means. Two independent tuning knobs are materialized here by the body ties of the NMOS, respective PMOS transistors. Without body biasing, any variation on the global Vdd will induce a variation in the transconductance and the linearity of the inverters, hence the filter. Thanks to these new independent tuning knobs, a combination of the two tuning voltages can always be found in order to get the desired values for both transconductance and linearity. The very wide tuning voltage range available on these body ties (see Sect. 13.2.1) permits to lower the design margins that are needed on such design, hence the typical power consumption.

This FDSOI tuning concept has been implemented in a third-order Gm-C low-pass filter, as presented in [6]. The measured performances as well as the comparison with the state of the art are given in Fig. 13.16.

This RF low-pass Gm-C filter using CMOS inverters has been successfully tuned by back gate instead of supply, moreover with no signal path interference. This supply regulator-free operation is energy efficient and also able of low voltage operation (down to VDD = 0.7 V).

There are two main categories of analog filters, each with advantages and drawbacks, these considered for an equivalent input referred noise level: the active-RC filters show generally excellent linearity, with the counterpart of large power




| | This work | | | | [2] | [5] | [6] | [7] |
|---|---|---|---|---|---|---|---|---|
| **Technology** | 28nm FD-SOI CMOS | | | | 65nm CMOS | 65nm CMOS | 0.13um CMOS | 0.18um CMOS |
| **Order** | 3 | | | | 3 | 5 | 2 | 3 |
| **Supply voltage [V]** | 0.7 | 0.8 | 0.9 | 1 | 1 | 1.2 | 1.2 | 1.8 |
| **Cut-off freq. [MHz]** | 454 | 454 | 457 | 459 | 4700 | 275 | 200 | 300 |
| **Input ref. noise [$nV_{rms}/\sqrt{Hz}$]** | 5.9 | 6.1 | 6.1 | 5.9 | 6.6 | 7.8 | 35.4 | 5 |
| **in-band IIP3 [dBVp]** | 1.2 | 4.0 | 4.0 | 2.4 | -3 | -12.5 | 4 | 6.9 |
| **Power diss. [mW]** | 4.0 | 4.6 | 5.2 | 5.6 | 19 | 36 | 21 | 72 |
| **SFDR/BW [dB/Hz]** | 109 | 110 | 110 | 109 | 105 | 98 | 100 | 113 |
| **NSNR [dB]** | **137** | **139** | **138** | **137** | 125 | 111 | 117 | 131 |

[2] Houfaf, *et al., ISSCC 2012*
[5] Saari, *et al., TCAS-I 2009*
[6] Mobarak, *et al., JSSC 2010*
[7] Kwon, *et al., TMTT 2009*

**Fig. 13.16** 28 nm FDSOI Gm-C low-pass filter, chip photomicrograph, measured performances, and comparison with the state of the art

consumption and limited operation in high frequency; the Gm-C filters show excellent frequency behavior and straightforward implementation from passive LC prototypes but have traditionally limited linearity performance. This FDSOI Gm-C implementation shows nevertheless competitive linearity. When compared to similar circuit in 65 nm bulk [7], at the same noise level, we get twice the linearity for a power level divided by four. When compared to best-in-class filters (active-RC) [8], at same noise level and cutoff frequency, we get competitive linearity for a power level divided by 14.

This 28 nm FDSOI CMOS solution implemented in ST's technology exhibits best in class compromise noise linearity power, thanks to the excellent analog/RF process intrinsic features.

## 13.4 Design Example of a Millimeter-Wave Building Bloc with FDSOI Specific Features

This section presents a millimeter-wave representative design in 28 nm FDSOI CMOS technology. We have chosen to present an integrated power amplifier for 60 GHz WiGig applications, as in such 60 GHz transceivers half of the power is burned by the power amplification section. For CMOS mmW-integrated power amplifiers (PA), there is also a trade-off to be solved between linearity and power-added efficiency at −8 dB back-off (this is the point with the maximum operation probability in such OFDM-based standard). The goal of this design example is to leverage this compromise and propose high linearity PAs with, at the same time, performant efficiency.

In order to satisfy with a same bloc the linearity and efficiency constraints, classical architectures rely on the Doherty PA topology. This structure relies on two different power amplification units that are operated one at a time, in order to privilege one or the other system constraints. The parallelization of these structures

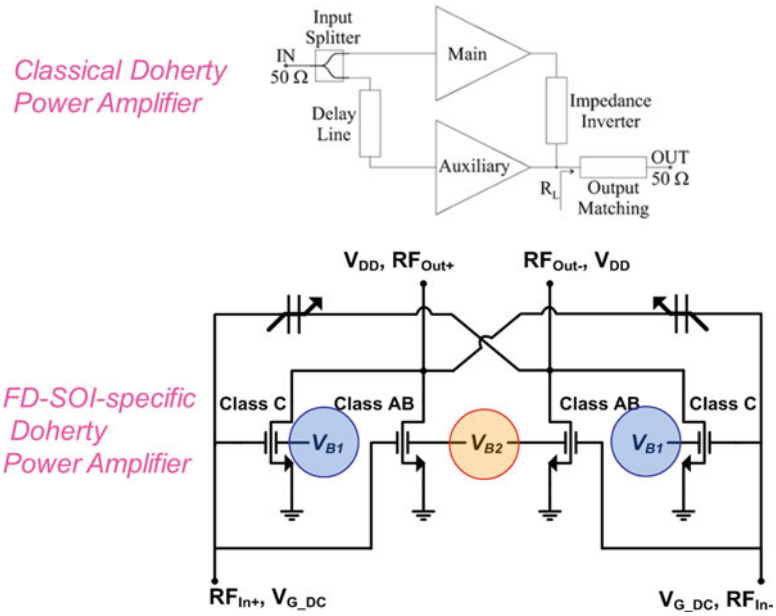



**Fig. 13.17** 28 nm Classical and FDSOI revisited Doherty power amplification topology

implies also passive power adaptation structures at the input and output, which inherently bring passive losses, hence natural lower efficiency. Such structures are typically implemented in classical CMOS integration.

In a specific FDSOI CMOS integration, we have decided to revisit this classical Doherty PA architecture, as depicted in Fig. 13.17 [9]. Two different class power amplifiers are as well connected in parallel, but here they are materialized by two differential pairs. The parallelization of such structures is straightforward, with no lossy passive elements; hence, the starting point for energy efficiency is already improved. Each PA cell (i.e., differential pair) is biased in a different class (here class AB and C), and each individual biasing point is changed by *gradually* varying the body voltage of each differential pair. We hence get the ability of gradually changing the overall class of the PA (mix of class AB and class C), thanks to the wide range of the forward body biasing voltage. Moreover, we get a new equivalent class of PA, which at any instant is composed of *x%* class AB operation and *y%* class C. At the two-class operation extremities, we get either Class-C at zero body bias or Class-A in maximum forward bias.

The compression of the Class-AB transistors is compensated by the gain expansion of the Class-C transistors, increasing the PA compression point without DC current penalty. The Class-AB devices are sized to carry the RMS power of the modulated signal and determine the average power consumption, while Class-C devices pass the peaks. Static body bias and dynamic modulated signals induce drain-gate nonlinear capacitance variations, tracked by MOS neutralization

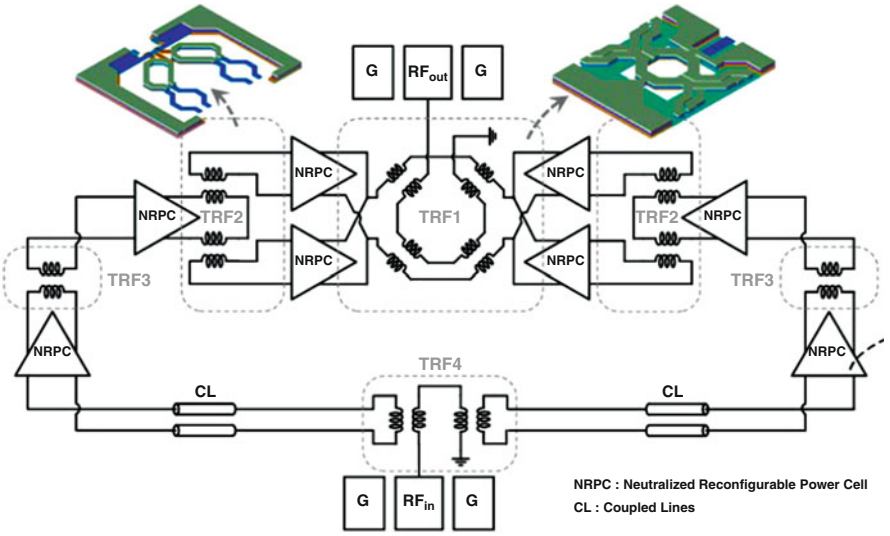


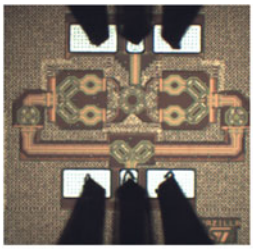

**Fig. 13.18** 28 nm FDSOI 10ML CMOS implementation of the WiGig 60 GHz Power Amplifier

capacitors across process, temperature, bias, and signal conditions. This robustness allows to safely use the full neutralized power cell flexibility to trade power gain and consumption for linearity, between "high gain mode" (all forward bias, Class-A) and "high linearity mode" (dual body bias, optimized Class-AB Class-C combination).

This new design topology, uniquely enabled by FDSOI wide range body biasing capabilities, permits to optimize in the same time power efficiency and linearity in such power amplification cells.

The total PA consists of three-stage transformer-based power amplification cells, each active cell as depicted before. This PA has been implemented in a 10 ML process option of the ST's 28 nm FDSOI CMOS technology; see Fig. 13.18. The VLSI-like dense and low BEOL still permits to obtain very competitive passives design, thanks to the SOI substrate feature.

At the output, a parallel-series eight-way power combiner TRF1 sums four differential reconfigurable power cells and performs differential to single-ended conversion. While the distributed active transformer (DAT) transforms 50Ω output to four 7Ω input ports with a coupling factor close to 0.87, the access lines are used to create eight ports presenting the optimal large signal load impedance for the power devices. This compact topology achieves an insertion loss of only 1 dB at 60 GHz. The 1:2 differential TRF2 and 1:4 TRF4 power splitters are based on a DAT structure and implement wideband matching networks. The two secondary windings are orthogonally placed to reduce parasitic magnetic coupling. The 1:2 transformer TRF3 performs impedance matching between the two driver stages.



| | This work | | | S. Kulkami *ISSCC 2014* | D. Zhao *JSSC 2013* | D. Zhao *JSSC 2012* | E. Kaymaksut *RFIC 2014* | A. Siligaris *JSSC 2010* |
|---|---|---|---|---|---|---|---|---|
| Technology | 28nm UTBB FD-SOI | | | 40nm | 40nm | 40nm | 40nm | 65nm PD-SOI |
| Operating mode | High gain | High linearity | | NA | Low/High power | NA | NA | NA |
| Supply voltage [V] | 1.0 | 1.0 | 0.8 | 0.9 | 1.0 | 1.0 | 0.9 | 1.8 |
| Freq. [GHz] | 61 | 60 | 60 | 63 | 61 | 60 | 77 | 60 |
| Gain [dB] | 35 | 15.4 | 15.1 | 22.4 | 16.8 / 17 | 26 | 9 | 16 |
| $P_{SAT}$ [dBm] | 18.9 | 18.8 | 16.9 | 16.4 | 12.1 / 17 | 15.6 | 16.2 | 14.5 |
| $P_{1dB}$ [dBm] | 15 | 18.2 | 16.2 | 13.9 | 9.1 / 13.8 | 15.6 | 15.2 | 12.7 |
| $PAE_{max}$ [%] | 17.7 | 21 | 21 | 23 | 22.2 / 30.3 | 25 | 12 | 25.7 |
| $PAE_{1dB}$ [%] | 9 | 21 | 21 | 18.9 | 14.1 / 21.6 | 25 | 11.1 | 22.6 |
| $PAE_{8dB\ backoff}$ [%] | 1.5 | 8 | 7.5 | 3 | - / 4.7 | 5.8 | 3.5 | 2.7 |
| $P_{DC}$ [mW] | 331 | 74 | 58 | 88 | 56 / 75# | 117 | 126 | 77.4 |
| $P_{DC\ 8dB\ backoff}$ [mW] | 332 | 124 | 84 | 94 | 56 / 78# | 120 | 140 | 79 |
| $100xP_{1dB}/P_{DC}$ | 9.6 | 89 | 72 | 28 | 14.5 / 32# | 31 | 26 | 24 |
| Active area [mm²] | 0.162 | | | 0.081 | 0.074 | 0.33 | 0.1 | 0.573* |
| ITRS FOM [W.GHz²] | 161,671 | 1,988 | 1,198 | 6,925 | 641 / 2,832 | 13,009 | 236 | 1,038 |

ITRS FOM = $P_{SAT}.PAE_{max}.Gain.Freq^2$ *: with pads #: estimated

**Fig. 13.19** 28 nm FDSOI 10 ML CMOS WiGig PA, chip photomicrograph, measured performance, and comparison with the state of the art

Figure 13.19 gives the measured performance of this mmW PA, for three extreme operation cases, knowing that an infinite number of operation conditions can be met when the two different body bias voltages are varied from 0 to 2 V (FBB conditions).

This power amplifier is fully WiGiG compliant, when taking into consideration linearity and frequency operation range (all four bands of the standard). It has introduced a new PA architecture which permits to continuously reconfigure power cells. This continuous operation class tuning is enabled by the very wide body bias voltage range.

Moreover, in the high gain mode, it exhibits the highest ITRS FOM, improving by an impressive factor of 10 the previous state of the art. In the high linearity mode, it breaks the linearity/consumption trade-off. It permits also a low-voltage high-efficiency operation (Vdd_min = 0.8 V).

## 13.5 Overview of FDSOI Specific Tuning and Trimming Techniques Using Body Biasing for Analog/RF Designs

Before concluding, this section gives an overview of the potential body biasing enabled tuning and trimming methods, identified as of today.

By taking advantage of the unique very wideband body biasing (BB) voltage range available in FDSOI technologies, the state of the art proposes several unique techniques bringing uncontested chip energy saving and revisiting system performances.

The first method consists in generating and making available on chip a body bias voltage variable over time and process, voltage, and temperature (PVT) variations. This permits to:

– Cancel system level PVT effects by continuously tuning transistors' respective VT. Several design examples can be found in references [6, 10, 11].
– Reconfigure circuit/bloc/system depending on application operation mode. Design examples can be found in [9] (at bloc level) and [11] (at system level).
– Propose new energy-efficient design techniques for tunable blocs via body tie, as in [12].

The second method consists in generating and making available on chip a fixed body bias voltage. In such cases, the design can efficiently:

– Enable operation at ULV (0.5 V) and at the same time increase circuit speed. Some design examples are [13, 14].
– Minimize switches on-resistance value and excursion for energy-efficient and high-speed switched-capacitors circuits (e.g., ADC), as in [4, 15].

For sure, each type of such on-chip body bias generators has to be carefully considered, in terms of power consumption, ripple, and noise on the generated control voltages. They may have a constant over time operation or duty cycled, depending on the system operation. And finally, they can address smaller or larger islands of transistors to be tuned or controlled.

## 13.6 Conclusion and Perspectives

This paper has presented a short overview of planar UTBB FDSOI technologies and their application for analog, RF, mmW, and mixed-signal designs.

As a summary, here are the major arguments of such technologies to focus on for analog/RF designs:

– Make massive usage of the body biasing techniques which enable transistors' VT as tuning knob and this over an unprecedented very wide tuning range
– Take profit of the very good analog performances. They permit designs with lower power consumption and which can safely operate at $L > L_{min}$ for design margin.

For RF to mmW design, atop the previously mentioned aspects, we should take into consideration the deep submicron technology features for the active devices (excellent $f_T, f_{max}$). The back end of line in an FDSOI environment permits to obtain performant passive devices, despite the very dense VLSI constraints.

For mixed-signal and high-speed designs, the major key parameters are the improved variability, the remarkable CMOS switches performance, and the reduced parasitic capacitances.

And finally, the UTBB FDSOI technologies open a new era in terms of innovative energy-efficient circuits and systems. They find excellent application for IoT implementations. Ultralow Power SoCs take benefit of efficient ultralow-voltage digital performances [16]; the full mixed-signal integration is then enabled by

efficient analog, RF [11], and mmW operation. Finally, the FDSOI implementation exhibit power and performance flexibility, thanks to the new tuning knobs brought in by very wide voltage range body biasing.

## References


1. Planes, N., Weber, O., Barral, V., Haendler, S., Noblet, D., Croain, D., Bocat, M., Sassoulas, P., Federspiel, X., Cros, A., Bajolet, A., Richard, E., Dumont, B., Perreau, P., Petit, D., Golanski, D., Fenouillet-Beranger, C., Guillot, N., Rafik, M., Huard, V., Puget, S., Montagner, X., Jaud, M.-A., Rozeau, O., Saxod, O., Wacquant, F., Monsieur, F., Barge, D., Pinzelli, L., Mellier, M., Boeuf, F., Arnaud, F., Haond, M.: 28 nm FD-SOI technology platform for high-speed low-voltage digital applications. In: Proceedings of Symposium VLSI Technology (VLSIT), pp. 133–134 (2012)
2. Arnaud, F., Planes, N., Weber, O., Barral, V., Haendler, S., Flatresse, P., Nyer, F.: Switching energy efficiency optimization for advanced CPU thanks to UTBB technology. In: IEEE International Electron Devices Meeting (IEDM) Dig., pp. 3.2.1–3.2.4 (2012)
3. Jacquet, D., Hasbani, F., Flatresse, P., Wilson, R., Arnaud, F., Cesana, G., Di Gilio, T., Lecocq, C., Roy, T., Chhabra, A., Grover, C., Minez, O., Uginet, J., Durieu, G., Adobati, C., Casalotto, D., Nyer, F., Menut, P., Cathelin, A., Vongsavady, I., Magarshack, P.: A 3 GHz Dual Core Processor ARM Cortex TM -A9 in 28 nm UTBB FD-SOI CMOS With Ultra-Wide Voltage Range and Energy Efficiency Optimization. IEEE J. Solid-State Circuits. **49**(4), (2014)
4. Kumar, A., Debnath, C., Narayan Singh, P., Bhatia, V., Chaudhary, S., Jain, V., Le Tual, S., Malik, R.: A 0.065mm2 19.8mW single channel calibration-free 12b 600MS/s ADC in 28nm UTBB FDSOI using FBB. In: ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, pp. 165–168 (2016)
5. Nauta, B.: A CMOS transconductance-C filter technique for very high frequencies. IEEE J. Solid-State Circuits. **27**(2), 142–153 (1992)
6. Lechevallier, J., Struiksma, R., Sherry, H., Cathelin, A., Klumperink, E., Nauta, B.: A forward-body-bias tuned 450 MHz Gm-C 3rd-order low-pass filter in 28nm UTBB FD-SOI with >1dBVp IIP3 over a 0.7-to-1V supply. In: 2015 IEEE International Solid-State Circuits Conference – (ISSCC) Digest of Technical Papers, pp. 1–3 (2015)
7. Houfaf, F. et al.: A 65nm CMOS 1-to-10GHz Tunable Continuous-Time Lowpass Filter for High-Data-Rate Communications. In: IEEE ISSCC Digest of Techical Papers, pp. 362–364 (2012)
8. Kwon, K., et al.: A 50–300-MHz highly linear and low-noise CMOS gm-C filter adopting multiple gated transistors for digital TV tuner ICs. IEEE Trans. Microwave Theory Techn. **57**(2), 306–313 (2009)
9. Larie, A., Kerhervé, E., Martineau, B., Vogt, L., Belot, L.: A 60GHz 28nm UTBB FD-SOI CMOS reconfigurable power amplifier with 21% PAE, 18.2dBm P1dB and 74mW PDC. In: 2015 IEEE International Solid-State Circuits Conference – (ISSCC) Digest of Technical Papers, pp. 1–3 (2015)
10. Danilovic, D., Milovanovic, V., Cathelin, A., Vladimirescu, A., Nikolic, B.: Low-power inductorless RF receiver front-end with IIP2 calibration through body bias control in 28 nm UTBB FDSOI. In: 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 87–90 (2016)
11. de Streel, G., Stas, F., Gurné, T., Durant, F., Frenkel, C., Cathelin, A., Bol, D.: Sleep Talker: A ULV 802.15.4a IR-UWB Transmitter SoC in 28-nm FDSOI Achieving 14 pJ/b at 27 Mb/s With Channel Selection Based on Adaptive FBB and Digitally Programmable Pulse Shaping. IEEE J. Solid-State Circuits. **PP**(99), 1–15 (2017)

12. Sourikopoulos, I., Frappé, A., Cathelin, A., Clavier, L., Kaiser, A.: A digital delay line with coarse/fine tuning through gate/body biasing in 28nm FDSOI. In: ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, pp. 145–148 (2016)
13. Fanori, L., Mahmoud, A., Mattsson, T., Caputa, P., Rämö, S., Andreani, P.: A 2.8-to-5.8 GHz harmonic VCO in a 28 nm UTBB FD-SOI CMOS process. In: 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 195–198 (2015)
14. Lahiri, A., Gupta, N.: A 0.0175 mm2 600 μW 32kHz input 307 MHz output PLL with 190 psrms jitter in 28 nm FD-SOI. In: ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, pp. 339–342 (2016)
15. Le Tual, S., Narayan Singh, P., Curis, C., Dautriche, P.: A 20 GHz-BW 6b 10GS/s 32 mW time-interleaved SAR ADC with Master T&H in 28 nm UTBB FDSOI technology. In: 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp. 382–383 (2014)
16. Zimmer, B., Lee, Y., Puggelli, A., Kwak, J., Jevtić, R., Keller, B., Bailey, S., Blagojević, M., Chiu, P.-F., Le, H.-P., Chen, P.-H., Sutardja, N., Avizienis, R., Waterman, A., Richards, B., Flatresse, P., Alon, E., Asanović, K., Nikolić, B.: A RISC-V vector processor with simultaneous-switching switched-capacitor DC–DC converters in 28 nm FDSOI. IEEE J. Solid-State Circuits. **51**(4), 930–942 (2016)