Chapter 12
Silicon Photonics Switch Matrices: Technologies and Architectures

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12.1 Introduction

Optical switching in *intra-data center networking* is gaining momentum, thanks to the unique advantages that it offers in terms of energy efficiency, low latency, cost reduction, wide bandwidth and transparency to bit rate and protocol with respect to electronic switching [1–3].

Key parameters for the introduction of optical switching in *data centers* are cost, integration level, port count, and footprint of the optical switching matrices. Recent achievements in silicon *photonics integrated technologies* for high-speed optical interconnects boost the advancement in the realization of new highly *integrated optical switching devices*.

The *integrated optical switch matrices* considered here are monolithically integrated photonic chips in which the signals to be processed propagate through optical waveguides.

Silicon integration will allow to exploit the highly developed silicon manufacturing infrastructure and the materials used for electronic integrated circuits. This ensures low cost and mass manufacturability, while the high refractive index contrast of silicon photonics allows to implement highly miniaturized optical circuits. Low power consumption is ensured by the energy-efficient physical mechanisms

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used to switch the light, by the small dimensions of the photonic integrated circuits, and by the tight integration of photonic and control electronic circuits made possible by the use of the same production technologies. There are also some limitations to cope with using silicon photonics such as the need to generate light by heterogeneously integrating blocks taken from InP-based technology, a more complex handling of signal polarization and coupling with single-mode fibers with respect to conventional optical technologies.

Optical switch matrices for data centers should allow to connect any idle input port to an arbitrary idle output port (non-blocking characteristic), in order to fully utilize the switch internal bandwidth. Moreover, they should have port count as large as possible (larger than 64×64) to allow building up of a larger multistage optical switching fabric ensuring networking of thousands of servers. They should have small size to be included in a module of few squared centimeters in order to utilize effectively the data center footprint and low loss, low differential loss among the different paths, and low crosstalk in order to realize scalable matrices. The characteristics of low polarization sensitivity are also crucial due the use of a single-mode fiber as interconnect infrastructure.

However, integrated optical switches, different from integrated electrical switch counterparts, are purely analog devices. While in digital electrical switches signal regeneration occurs in the internal CMOS gates, inside the optical switches, loss and crosstalk are experienced during processing through the many traversed switching cells. Loss and crosstalk increase with the switch matrix port count and complexity and eventually limit the scalability. Different prototypes of silicon-integrated optical switching matrices are presented, explained, and discussed in this chapter, with non-blocking characteristics, having potential high port count, low loss, and low crosstalk.

The chapter is organized as follows: the physical effects used to switch optical signals in silicon-integrated matrices are presented in Sect. 12.2, and the relevant switching cell types are discussed in Sect. 12.3. In Sect. 12.4, the optical switch matrix architectures for optical circuit switching are explained, and the relative integrated devices proposed and demonstrated so far are reported. Section 12.5 is dedicated to the presentation of optical switching matrices used in optical packet switching. Section 12.6 reports on a silicon photonics wavelength selective switch implementation, and in Sect. 12.7, a comparison table among the switching fabrics is presented. Finally, in Sect. 12.8, the perspectives and future research directions are briefly discussed.

12.2 Physical Effects and Mechanisms for Optical Switching in Silicon

In a first category of photonics integrated switch matrices, the mechanisms used for optical switching are associated to a change in the index of refraction of optical waveguides in interferometric- or resonant circuit-based switching cells. In such integrated switching cells, this index variation causes a change of the signal path from one input port to another output port.

In such silicon photonics switches, two physical effects are used: the plasma dispersion effect and the thermo-optic effect with quite different response times. With the plasma dispersion effect, the switch can be reconfigured in a nanosecond scale, while with the thermo-optic effect, the reconfiguration time is in the order of microseconds.

A completely different mechanism used for switching in silicon monolithic integrated optical devices is the physical movement of optical waveguides driven by electrostatic actuators. They have become attractive due to the widely developed micro-electromechanical system (MEMS) process technology in which micrometric-scale switching cells are created combining mechanical and electrical components. This technology leverages on silicon wafer-scale fabrication processing to achieve low cost and high repeatability, and it is already widely adopted in consumer electronics accelerometers and gyroscopes for mobile phones. These types of optical switches have reconfiguration times very much dependent on the mechanical design of the MEMS switching cell; typically, they are spanning from 1 to 100 μs.

12.2.1   Plasma Dispersion Effect

Plasma dispersion effect, also named free carrier dispersion effect, has been investigated and numerically analyzed for the first time in 30 years [4]. From that time, many progresses have been made, and today optical modulator in silicon photonics using this physical effect has become commercially available in optical interconnects [5]. The optical switches utilize the same effect of modulators consisting of the variation of the refractive index in an optical waveguide induced by the variation in the concentration of free carriers.

Unfortunately, it is not possible to change the waveguide refractive index without affecting the optical loss generated by the free carrier absorption since the two effects are coupled by the Kramers-Kronig dispersion equation:

$$\Delta n(\omega) = \left(\frac{c}{\pi}\right) P \int_{\infty}^{0} \frac{\Delta \alpha(\omega') d\omega'}{\omega'^2 - \omega^2} \tag{12.1}$$

in which P indicates the principal part of the integral due to the singularity at $\omega = \omega'$, Δn is the refractive index change, $\Delta \alpha$ is the absorption coefficient change, c is the light velocity, and ω is the angular frequency of the light.

The refractive index and absorption coefficient change with respect to the change in the carrier density have been quantified in [6]:

$$-\Delta n(\lambda) = p(\lambda) \Delta N_e^{q(\lambda)} + r(\lambda) \Delta N_h^{s(\lambda)} \tag{12.2}$$

$$\Delta \alpha(\lambda) = a(\lambda) \Delta N_e^{b(\lambda)} + c(\lambda) \Delta N_h^{d(\lambda)} \tag{12.3}$$

in which ΔN_e and ΔN_h are relevant with the concentration of electrons and holes, respectively.

The coefficients have been empirically found in [6] for crystalline silicon for wavelength from 1 up to 14 μm.

At the wavelengths of interest in optical fiber communication systems at 1.3 μm and 1.5 μm, the coefficients are:

for $\lambda = 1.3$ μm

$$
\begin{aligned}
&a\left(cm^2\right) = 3.48 \cdot 10^{-22} \\
&b = 1.229 \\
&c\left(cm^2\right) = 1.02 \cdot 10^{-19} \\
&d = 1.089 \\
&p\left(cm^3\right) = 2.98 \cdot 10^{-22} \\
&q = 1.016 \\
&r\left(cm^3\right) = 1.25 \cdot 10^{-18} \\
&s = 0.835
\end{aligned}
\tag{12.4}
$$

and for $\lambda = 1.55$ μm

$$
\begin{aligned}
&a\left(cm^2\right) = 8.88 \cdot 10^{-21} \\
&b = 1.167 \\
&c\left(cm^2\right) = 5.84 \cdot 10^{-20} \\
&d = 1.109 \\
&p\left(cm^3\right) = 5.40 \cdot 10^{-22} \\
&q = 1.011 \\
&r\left(cm^3\right) = 1.53 \cdot 10^{-18} \\
&s = 0.838
\end{aligned}
\tag{12.5}
$$

From the above values, it results that at 1.3 and 1.55 μm, it is possible to find a region of the carrier density around 10^{18} cm^{-3} in which the optical phase shift component in the waveguide is dominant with respect to the optical absorption component. It is therefore possible to obtain an optical phase shift of about π radians, as needed for optical switching in a Mach-Zehnder interferometer-based switching cell (see Sect. 12.3.1), at low loss and with a reasonably short length.

As an example, the characteristics of a phase shifter working at 1.3 μm wavelength with a carrier concentration (both holes and electrons) of 10^{18} cm^{-3} are calculated.

From the coefficients reported above, it is obtained for the change of the refractive index:

$$-\Delta n\left(1.3 \;\mu m\right) = 2.98 \; 10^{-22}\left(10^{18}\right)^{1.016} + 1.25 \; 10^{-18}\left(10^{18}\right)^{0.835} = 1.9 \; 10^{-3} \qquad (12.6)$$

The waveguide length for a π radian phase shift, L_π, can be obtained by the following formula:

$$L_\pi = \frac{\Delta\theta\lambda}{2\pi\Delta n} \qquad (12.7)$$

and by imposing $\Delta\theta = -\pi$, it is found: $L_\pi = 340$ µm.

The absorption coefficient variation is given by:

$$\Delta\alpha\left(1.3 \;\mu m\right) = 3.48 \; 10^{-22}\left(10^{18}\right)^{1.229} + 1.02 \; 10^{-19}\left(10^{18}\right)^{1.089} = 8.65 \; \text{cm}^{-1} \qquad (12.8)$$

Optical loss for a phase shifter with 340 µm length is given by:

$$\Delta\alpha L_\pi = 0.29 \qquad (12.9)$$

and it corresponds to an optical loss <1.5 dB.

It has to be noticed that holes have a much stronger effect (about 10×) than electrons on the change of refractive index.

In some optical switching cells based on Mach-Zehnder interferometers (see Sect. 12.3.1) electrically driven in push-pull configuration, the phase shift required on both arms is $\pi/2$, and the phase shifter length can be halved [7].

Plasma dispersion-based switches are implemented as p-i-n junctions operating in forward mode. In such structures, higly doped p- and n-regions are separated by an intrinsic region where the waveguide is formed [8]. By forward-biasing the p-i-n junction, free carriers are injected in the intrinsic waveguide region, as depicted in Fig. 12.1, changing its refractive index. The doped region of the silicon waveguide constitutes therefore a phase shifter, and the phase change depends on both the injection current and the length of the phase shifter. This phase shifter can be inserted in a waveguide-based switching cell, for instance, Mach-Zehnder interferometers or micro-ring resonators, for tuning or switching. The time response of the plasma dispersion effect in a forward biased p-i-n junction is limited by the carrier diffusion time in the injection region and is in the order of nanoseconds: this value complies with most optical packet switching requirements [9, 10]. Alternatively, the forward bias can be substituted by a carrier accumulation mechanism. Carrier accumulation occurs around a thin oxide region in the p-oxide-n structure. The thickness of the insulator region is a trade-off between bandwidth and driving voltage. The thinner the oxide region, the higher is the value of the capacitance and consequently the lower is the driving voltage but also the bandwidth would be limited. This solution is quite interesting because based on charge and discharge of the capacitor formed by the insulator and its interfaces. The index change depends therefore on the charge accumulation only, i.e., the charge of the capacitor, and may be of the

Fig. 12.1 Plasma dispersion effect in a silicon-on-insulator (SOI) rib waveguide
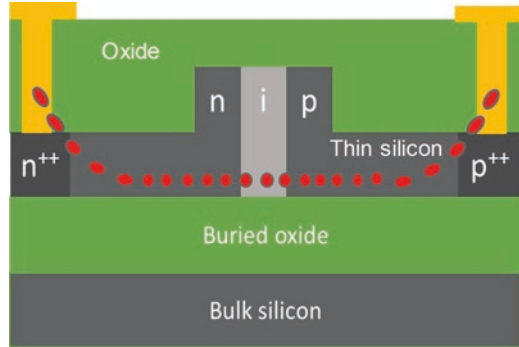
order of 10^{-3}. In this condition, there is no current flow, and the power consumption can be extremely reduced. In the forward biased p-i-n junction instead, the current flow is continuous. Presently this solution has been adopted for modulators only [11], and it is affected by a nonnegligible loss that in optical switching matrices eventually limits the scalability.

12.2.2 Thermo-optic Effect

A second physical effect used in silicon photonics optical switching devices is the thermo-optic effect.

Bulk silicon has a quite large thermo-optic coefficient defined as the change in refractive index n with temperature T:

$$\frac{\partial n}{\partial T} = 1.86 \times 10^{-4} / K \ \text{ at 300 K,}$$ (12.10)

and thermal conductivity:

$$k_{\text{Si}} = 148 \ \text{W} / (\text{mK})$$ (12.11)

These parameters, together with the high index contrast (between waveguide core and cladding) of silicon photonics, allow the realization of highly miniaturized optical waveguide phase shifters with micrometric size and low switching power (in the mW range) made by placing micro-heaters in the vicinity of the optical waveguide in order to change its local temperature and consequently the refractive index. These thermally actuated phase shifters, placed in one or both arms of a Mach-Zehnder interferometer (MZI) or along a micro-ring resonator, could act as active elements in a switching cell of a big integrated optical switch matrix.

Two types of micro-heaters have been developed so far: silicon doped [12] and metallic [13].
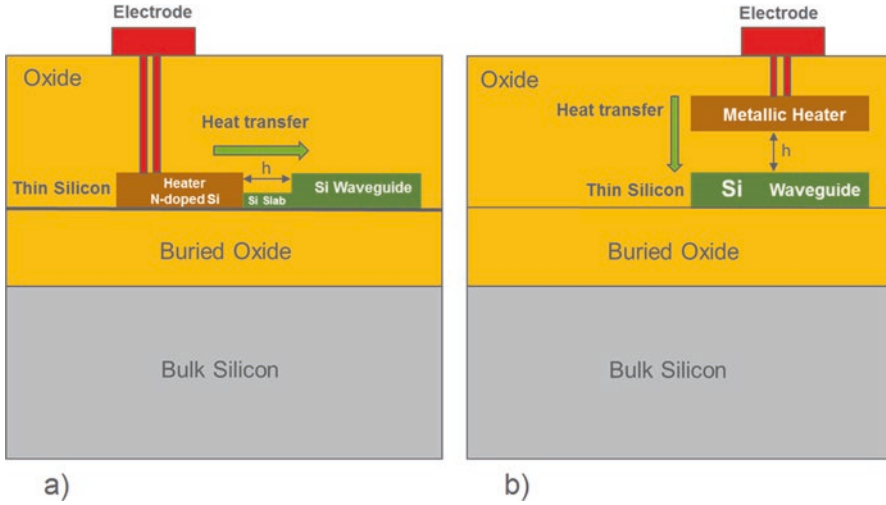
Fig. 12.2 Thermo-optic effect in a silicon-on-insulator (SOI) optical waveguide. (**a**) Silicon doped micro-heaters, (**b**) metallic micro-heater

A phase shifter with silicon-doped micro-heater is depicted in Fig. 12.2a. At one side of the silicon optical waveguide, surrounded by the buried oxide (BOX) layer and cladding material, a micro-heater made by N-doped silicon is implemented. A silicon slab of width h could be inserted, in some designs, between the waveguide and the doped heater to increase the thermal conductivity, the slab being low enough to avoid optical leakage through it. To activate the phase shifter, a current is injected into the heater that works as a resistor, increasing the temperature of the adjacent optical waveguide and changing its refractive index.

In Fig. 12.2b, a phase shifter is made of a metal line with a suitable width and thickness to ensure the expected value of resistivity, and it is placed at a certain distance h (less than 1 μm) above the silicon optical waveguide. The metal line is, for instance, made by Ti/TiN, and the current flows through the metal resistor causing the increase of temperature and the generation of the heat necessary to change the refractive index of the silicon waveguide core. In both heater configurations, the heat transport by conduction is defined by the following equation [13]:

$$\nabla\left(-k\nabla T\right) + \rho c \frac{\partial T}{\partial t} = q_s \tag{12.12}$$

where k is the thermal conductivity of the used materials, c is the heat capacity, ρ is the material density, q_s is the heat flux density, and T is the temperature. Since ρ is fixed and it depends on the materials, the design parameters that have to be optimized to achieve a fast time response, a high power efficiency, and a low optical loss of a waveguide phase shifter are mainly k and c. They depend mostly on the thickness of the BOX and the cladding layers. Thinner BOX and cladding layers give a faster response time and a better power efficiency, but a minimum thickness of about 1 μm has to be set for both BOX layer and cladding to avoid loss increase

due to leakages of the optical field into the underneath silicon substrate and optical absorption by the metal line of the heaters.

The thermo-optic effect, differently from the plasma dispersion effect, is inherently low loss and can be utilized in optical waveguide-based switching cells for tuning and switching photonic devices with negligible insertion loss. However, the response time of such thermally actuated switches is slower than the plasma dispersion-based counterparts, and it is usually of few microseconds limited by the heat diffusion process.

Power consumption of thermal heaters is a function of the current needed to reach the wanted temperature, and it depends on the thermal impedance of the insulator between the heater and the waveguide and on the distance between the silicon core and the heat sink that usually is the silicon substrate. The insulator thickness on top of the silicon core is designed to avoid loss due to optical mode overlap with the heater. Typically, metal heaters are placed at 0.7–1 μm above the silicon core. When the time response of the heater is not critical, an underetch of the buried oxide below the silicon core can help in reducing power consumption, i.e., the underetch serves to thermally insulate the waveguide, and the reduced heat exchange serves to maintain the steady-state temperature of the waveguide core. A comparison between thermo-optic- and p-i-n junction-based phase shifters used for a $N = 64$ port switch is reported in [14]. The time response is in favor of p-i-n junctions, but the insertion loss is much lower in thermo-optic-based switches. For $N = 64$, 8.5 dB of insertion loss for the current-driven thermo-optic switch and 17 dB [15] or 29 dB [16] for the carrier-injection switches have been reported.

12.3   Integrated Switching Cell Technologies

The key building block in an integrated optical switching matrix is the switching cell, that is, the single *switching element* (normally a 2×2 switch or in some cases a 1×2 switch) interconnected to many other switching elements of the same type in a two-dimensional matrix. The switching cell characteristics of bandwidth, loss, and extinction ratio are crucial to realize a scalable, high-performance, integrated switching matrix. The switching cell states can be identified either with *bar* and *cross* (if related to the optical path through the switching cell) or alternatively with *on* and *off* (if related to the state of the electrical control signal), as depicted in Fig. 12.3. The cell characteristics in the two alternative states are generally different.

Loss of a switching cell is defined as the reduction in the signal power from input (P_i) to output (P_o) port of the wanted channel (see Fig. 12.3).
Extinction ratio of a switching cell is the ratio of the signal power level at the output port of interest (P_o) to the signal power level at the unwanted port (P_x) (see Fig. 12.4).
Crosstalk is the ratio of total power in the disturbing signals to that in the wanted signal.
While the extinction ratio is a property of the switching cells, "crosstalk" is reserved for the description of system effects of a complete switching matrix and may comprise many unwanted signals interfering with the wanted signal.
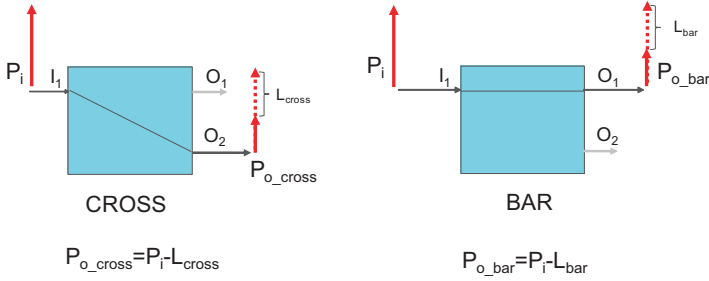
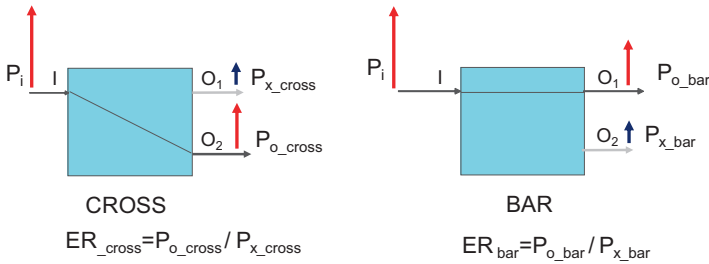**Fig. 12.3** Loss of a switching cell in *cross* and *bar* state

Fig. 12.4 Extinction ratio of a switching cell in *cross* and *bar* state

Crosstalk is the ratio of total power in the disturbing signals to that in the wanted signal.

In the following, the most relevant switching cells are presented and discussed.

12.3.1 Mach-Zehnder Interferometer (MZI) Switching Cell

The switching cell based on *Mach-Zehnder interferometers* (MZI) is shown in Fig. 12.5. It consists of an optical interferometer with an input 3 dB coupler, two arms equipped with phase shifter sections, and an output 3 dB coupler. The cell works with the following principle: the optical power of the input signal is split by the first coupler into two equal portions that interfere at the output coupler depending on the relative phase shift. If the phase difference among the two arms is 0 radians, as depicted in Fig. 12.6, a constructive interference occurs at the crossover port, and the signal entering at I_1 goes out at O_2, and similarly the signal at I_2 port goes out at O_1 port: in this condition, the switch is defined to be set on *cross* state. When the phase difference among the arms is changed to π radians, activated by an electrical control signal, the constructive interference occurs at the through port, and the signal entering at I_1 goes out at O_1 (see Fig. 12.6), while the signal entering at port I_2 goes out at O_2: in this condition, the switch is defined to be in *bar* state. This switch cell can be activated by using either the thermo-optic effect or the
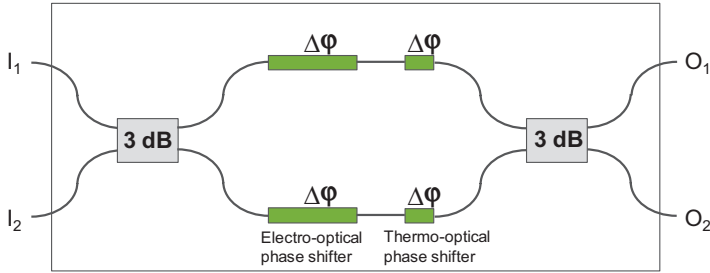
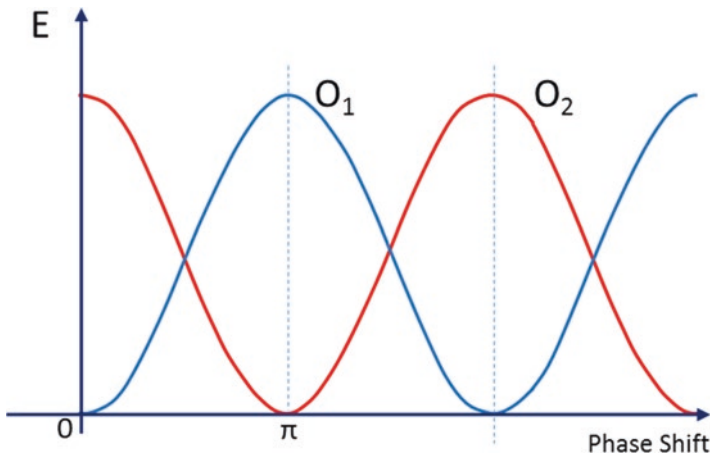**Fig. 12.5** Mach-Zehnder interferometer switching cell

Fig. 12.6 Electrical field amplitude vs phase shift between the two arms at output ports O_1 and O_2 of the MZI when the input signal is injected at port I_1

plasma dispersion effect (see Sect. 12.2) or both to change the refractive index in the waveguides of the phase shifter sections: the selection of the switching mechanism depends on the switching speed requirements that should be in the microsecond range for the thermo-optic effect and nanosecond range for the plasma dispersion effect. In some high-speed switch designs, both types of phase shifter can be used to improve the extinction ratio performances with the plasma dispersion-based phase shifters activated for fast switching and the thermo-optic phase shifters tuned to compensate interferometer unbalances due to production imperfections without introducing significant excess losses.

The switching cells working with plasma dispersion effect are normally designed to be in *cross* state with no activation signal (*off* state), and for that reason, they have, in general, better loss and extinction ratio performance in *cross* than in *bar* state that needs current injection with the relative increase of loss and decrease of extinction ratio.

In most of the integrated switch design, the π relative phase shift between the two arms of the MZI, needed to set the switch in *bar* state, is actuated by two phase shifters, one per each arm driven in push-pull manner. In this condition, only $\pi/2$ phase

shift is needed per phase shifter, and this results in a lower loss with respect to the MZI configuration with only one shifter in one arm. In this configuration, the carrier density can be halved with consequent improvement of loss and extinction ratio due to a better power balance between the two interfering signals at the MZI output.

12.3.2 Resonant Switching Cell

A second type of monolithically integrated silicon photonics switching cell is the one based on waveguide-coupled *micro-ring resonators* (MRR) [17]. This is a resonant structure consisting of two bus waveguides (W_1 and W_2) and one or more equal MRRs coupled to each other (see Fig. 12.7). The MRR has periodic frequency response repeating itself each free spectral range (FSR). If the wavelenght of the signal going into port I_1 is aligned with the resonance of the MRR (*on-resonance*) (see Fig. 12.7a), then that signal from W_1 couples into the first ring, couples subsequently to the other intermediate rings and finally couples out from the last ring into W_2 and exits the device at the drop port O_1. If the input signal instead is *off-resonance* with the rings (see Fig. 12.7b), it remains in W_1 and exits at port O_2 (through port) nearly unperturbed. At the same time, in *off-resonance* state, a signal going into port I_2 remains in W_2 and exits port O_1 unperturbed.

The resonance condition is according with the following equation:

$$2\pi R n_{\text{eff}} = m\lambda \tag{12.13}$$

in which R is the ring radius, n_{eff} is the effective refractive index of the waveguide, λ is the signal wavelength, and m is an integer number.

The switching principle of the MRR is shown in Fig. 12.8a.

Micro-ring resonator switching cell is narrowband, and if a single micro-ring is used, it has Lorentzian shape with slow roll-off of the resonance passband resulting in a relatively low switch extinction ratio.
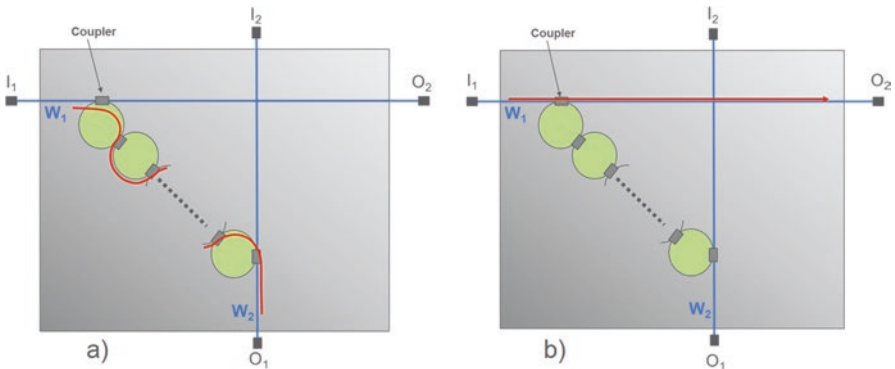

Fig. 12.7 Resonant switching cell states: cell set (**a**) *on-resonance* with the signal, (**b**) *off-resonance* with the signal
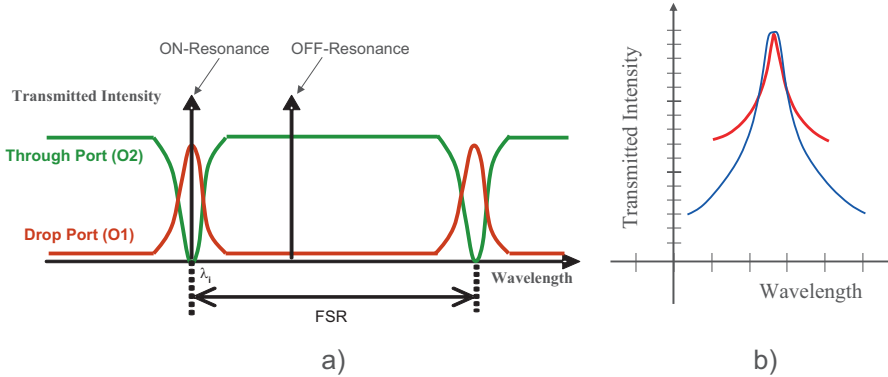
Fig. 12.8 (**a**) Transmitted intensity at ports O1 and O2 with the MRR *on-resonance* and *off-resonance*; (**b**) MRR frequency response of a single micro-ring (*red curve*) and two-coupled micro-rings (*blue curve*)

Higher-order MRR-based filters are required to improve both the passband width and the extinction ratio. In this case, a filter with high-order-coupled micro-rings can be suitably synthesized [18]. The frequency response of a two-coupled micro-ring switching cell is shown in Fig. 12.8b, and it is compared with that of a single micro-ring.

This switching cell can be activated by an electrical control signal to change the effective refractive index n_{eff} of the ring waveguides in order to match the resonance condition (see formula 12.13). This is achievable using either the plasma dispersion effect or the thermal effect, as discussed in Sect. 12.2. With the former, electrical carriers are injected into the ring waveguides, and the switch time response is very fast in the nanosecond range, while with the latter, the local temperature of the ring waveguide is changed using a micro-heater, and in this case, the response time is in the microsecond range. Generally, this type of switching cells is set as *on-resonance* when activated (*on-state*) and *off-resonance* when deactivated (*off-state*), and they have better loss and extinction ratio in this switch's last state since the optical path is shorter.

12.3.3 Micro-electromechanical System (MEMS) Switching Cell

The key building block in silicon *MEMS*-based optical switching cells is the comb electrostatic actuator. It has been widely used in MEMS devices because of easy fabrication and mass manufacturability, and it has the function of translating movable micrometric parts with high precision level [19].

Fig. 12.9 Comb electrostatic MEMS actuator: (**a**) actuator in *on*, (**b**) actuator in *off*

It consists of two plates each with a number of fine interdigitated fingers, the fix comb and the movable comb (see Fig. 12.9)—by applying a voltage between them, the fixed comb attracts the movable comb with a force given by:

$$F = \frac{1}{2}\frac{\partial C}{\partial x}V^2 \qquad (12.14)$$

where C is the capacitance between the plates and V is the applied voltage and x is the axis of translation.

Since

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \qquad (12.15)$$

where ϵ_0 is the permittivity of the free space, ϵ_r is the relative permittivity of the material between plates, A is the overlapping plates area, and d is the plate separation, the more numerous are the fingers, the larger is the capacitance surface and hence the higher is the force. An interesting advantage of this type of actuator is the fact that the electric circuit is capacitive, and hence the driving current needed to load the capacity is very low even if the voltage is high.

In the electrostatic actuator shown in Fig. 12.9, the fixed comb that is totally anchored to the substrate is indicated in green, while the movable comb, supported by a spring, is indicated in orange, and it translates to left when a driving voltage is applied between the conductive plates. The movable comb is free to move except at the right end where it is also anchored to the substrate, so that the actuator can come back to its initial position with no applied voltage, thanks to the spring force.

Optical switching cells based on silicon MEMS consist of a fixed waveguide section and a movable waveguide section, and the light coming from the fixed waveguide is coupled to two alternative movable optical waveguides under the comb actuator control. This type of switching cell based on moving waveguides can easily achieve high extinction ratio by providing enough separation between the alternative waveguides to which the output signals are to be coupled.

12.4 Integrated Matrices with μs Response Time for Optical Circuit Switching

Optical circuit switching has been researched as an attractive technology to increase the bandwidth and reduce latency and power consumption in intra-data center networking. Optical switching matrices have unsurpassed capability in routing high-capacity dataflows of 100 Gbps, 400 Gbps, or more with high energy efficiency and bit rate and protocol transparency, but, differently from electrical switch matrix counterparts, they cannot process a data stream bit by bit in the optical domain. Hence, hybrid switching architectures have been proposed in [1, 20] in which bursty and latency-sensitive traffic (mice flows) is switched by electrical packet switches, while long-lasting dataflows (elephant flows) are routed by optical circuit switches (OCS). It has been found that the addition of an optical switching layer working in cooperation with the electrical packet switching (EPS) layer improves the data center networking performances. However, in such hybrid networks, the data throughput is affected by the optical switch response time, and optical switches with speed in the order of microseconds are needed. If the switch response time is fast enough, they could also be used in optical burst switching (OBS) [21]: according to this technique, optical packets with the same destination, before switching, are wrapped into longer burst frame lasting for many microseconds to reduce the impact of the switch reconfiguration time on the bandwidth utilization efficiency and latency. In the following, the architectures and technologies for integrated circuit switches are presented and discussed.

12.4.1 Crossbar Switch Architecture

An N × M integrated optical *crossbar switch matrix* is a photonic network with N horizontal optical waveguides and M vertical optical waveguides containing N × M optical switching cells (crosspoint switch elements), each one placed at the crossing point between a vertical waveguide and a horizontal waveguide, as depicted in Fig. 12.10. The input signals traverse a number of cascaded switching cells until they arrive at the output ports. Along this path, only one crosspoint cell is activated, and it is the one deviating the signals from the horizontal waveguide to the vertical waveguide. In Fig. 12.10, the internal switch connection from I_2 to O_3 is indicated by the orange line, and it is obtained by activating the crosspoint cell S_{23}.

The schematic block diagram of the 2 × 2 crosspoint switching cell is shown in Fig. 12.11. It has two input ports I_1 and I_2 and two output ports O_1 and O_2, and if the switch cell state is in *off* (switching cell deactivated), the input signals entering from I_1 and/or I_2 proceed straight on its direction toward O_1 and O_2, respectively. When the switch cell is set *on*, the signal from I_1 is deviated to the output port O_2, while the ports I_2 and O_1 remain unconnected.
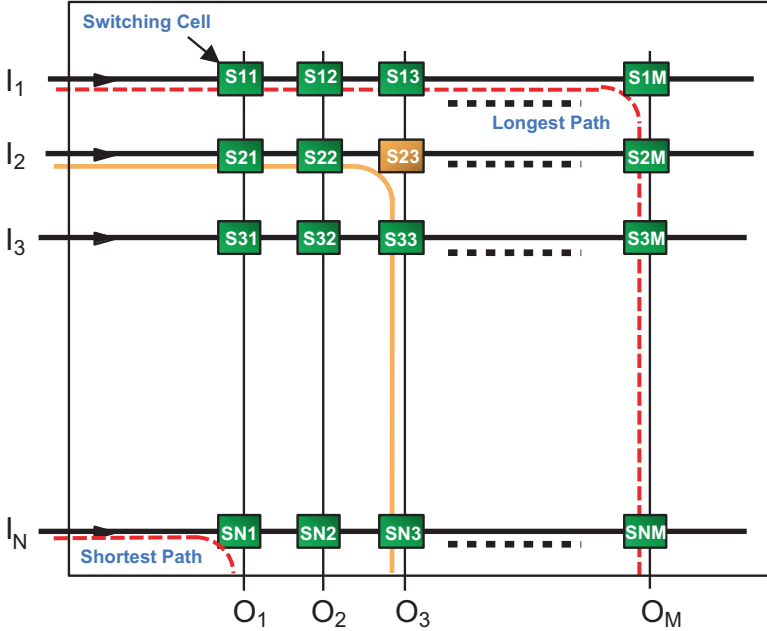
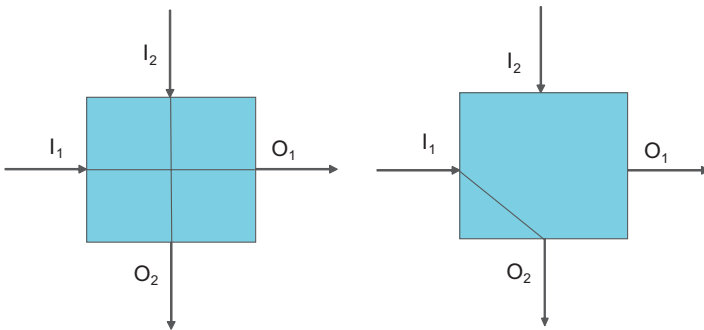**Fig. 12.10** N × M optical crossbar switch matrix

Fig. 12.11 2 × 2 crosspoint switching cell

Optical crossbar switches have been realized with the same architecture of electrical CMOS counterparts that are commercially available with 160×160 ports at 12 Gbps gigabit rates [22] and 16×16 ports at 28 Gbps rate [23]. In these electrical crossbar matrices, CMOS gates are placed at the crossing points to interconnect two electrical lines.

In a crossbar matrix architecture, each switching cell is dedicated to a specific input to output connection, and hence it is always possible to connect idle inputs to arbitrary idle outputs independently of the already established input to output connections: this

results in a strictly non-blocking (SNB) characteristic and low power consumption since only one switching cell is activated for each input signal.

Crossbar switching matrices have different insertion loss experienced by the input signals travelling through the matrix due to different optical paths and different number of switching cells traversed. In Fig. 12.10, the lowest loss is for the signal that enters at I_N and gets out at port O_1, while the highest loss is for the signals I_1-O_M (see red dashed lines). To develop scalable crossbar matrices, the loss of the waveguide crossing circuits and that of the switching cell when set in *off* must be very low (few hundredths of a dB for waveguide crossing and few tenths of a dB for the cell set in *off* in a 64 × 64 matrix); this is because all the cells traversed by the signals are set in *off* but one.

In crossbar switch, the extinction ratio requirement of the switching cell must also be high to keep the crosstalk low. This is because the various signals travelling through the horizontal lines of the matrix leak a portion of power at each of the switched *off* traversed cells, due to non-ideal extinction ratio. These unwanted leakages propagate along the vertical lines together with the wanted signal and disturb it as unwanted crosstalk.

In a N × M switch matrix, the number of switching cells is equal to N × M, while the maximum number of activated switching cells is equal to N.

Two types of silicon-integrated optical crossbar switch matrices have been investigated and demonstrated recently: the 64 × 64 digital silicon photonics MEMS switch and the 8 × 7 switch matrix based on resonant switching cells. They are presented and discussed in the following.

12.4.1.1   64 × 64 Digital Silicon Photonics MEMS Switch Matrix

A new type of monolithically integrated MEMS switch matrix in *silicon photonics* has been demonstrated and reported in [24–27]. The switching cell is based on vertical adiabatic couplers actuated by MEMS (see Fig. 12.12a).

The 64 × 64 optical crossbar switch matrix [27] was fabricated on two stacked silicon optical layers: a first 220 nm thick crystalline silicon layer on top of a 3 μm thick buried oxide (BOX) layer in a SOI wafer and a second deposited polysilicon layer.

The matrix of passive rib optical waveguides with 60 nm ridge height and 600 nm width is patterned in the crystalline silicon layer, and a multimode interference (MMI) waveguide crossing is placed at each matrix crossing point in order to achieve low loss and high isolation.

In the top polysilicon layer, a MEMS electrostatic actuator is patterned together with a vertical adiabatic coupler made by a ridge waveguide with core thickness of 300 nm and ridge height of 200 nm.

When the switching cell is in *off* (see Fig. 12.12b), the adiabatic coupler is positioned 1 μm above the passive waveguide crossing, and no coupling occurs in the top polysilicon circuit layer: the light entering in the switch cell at the "input" port
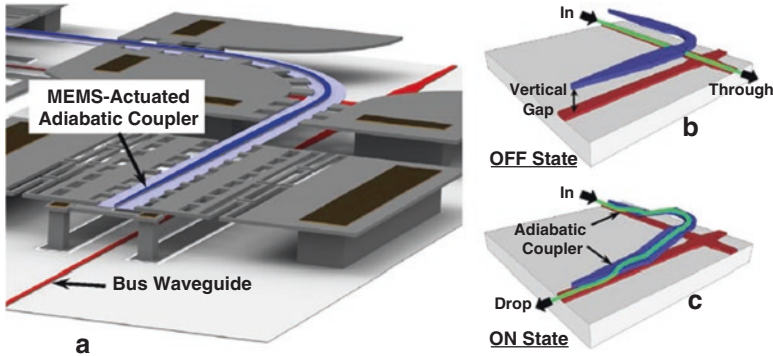
Fig. 12.12 Silicon photonics MEMS switching cell [27]: (**a**) overview of the cell, (**b**) cell set in *off*, (**c**) cell set in *on*

proceeds propagating in the passive waveguide layer toward the "through" port with very low disturbances. When the switch cell is set in *on* (see Fig. 12.12c) by imposing a control voltage at the electrodes of the electrostatic actuator, the adiabatic coupler is moved by the MEMS actuator toward the waveguide crossing, and the light in the bottom layer entering at the "input" port is coupled into the waveguide in the top layer by a first adiabatic coupler. After a rotation of 90°, obtained inside a curved waveguide, the light is coupled back in the bottom layer by a second adiabatic coupler and goes out at the "drop" port.

To digitally control the switch operations, mechanical stoppers are used to fix the vertical gap between the top waveguide and the bottom waveguide (at about 125 nm) when the switch is in *on*, while micro-springs are used to move waveguides away when the switch is in *off*.

Off-chip connection to optical fiber arrays is provided by integrated grating coupler at input and output ports.

This matrix comprises of 4096 MEMS-actuated switching cells with 110×110 μm^2 size. The switching cells have high extinction ratio of > 60 dB in *off* state.

The loss of the switch cell is 0.47 and 0.026 dB in *on* and *off*, respectively, while the loss of the waveguide crossing is 0.017 dB, and the chip propagation loss is 1.1 dB/cm. With these values, the on-chip loss, not including input and output fiber coupling losses, is path dependent spanning from about 0.47 dB for the shortest path (corresponding to one switch cell set in *on*) to 3.7 dB for the longest path (corresponding to 63 switch cell set in *off* with 0.026 dB/cell loss plus 1 cell set in *on*). The *on* and *off* switching time response is 0.91 and 0.28 μs, respectively. The total 64×64 matrix chip area, including grating couplers, is 8.6 mm × 8.6 mm. The switch cells are voltage controlled with a driving voltage of about 42 V, and the driving current needed to load the electrostatic MEMS actuator is very small due to the fact that electric circuit is purely capacitive. The operating wavelength range is as broad as 300 nm spanning from 1400 to 1700 nm.

This matrix is polarization dependent since it works correctly only with input signals having TE polarization, while for a practical system utilization, the improvement to a polarization-insensitive device is essential.

12.4.1.2 8 × 7 Switch Matrix Based on Resonant Switching Cells

An 8 × 7 crossbar switch matrix based on resonant switching cells has been demonstrated in [28]. The chip was fabricated in a SOI wafer having a 220 thick silicon layer over a 2 μm thick BOX layer. The waveguide dimensions are 220 nm × 500 nm, and the cladding layer on top of it is 1.2 μm thick.

The switching cell consists of a fifth-order ring resonator as shown in Fig. 12.13a. The five rings have a racetrack shape (to increase the coupling length and ensure a phase shift of π) with 5 μm bend radius and a free spectral range (FSR) of about 350 GHz. In Fig. 12.13b, the layout of the switching cell is shown including the optical waveguides and waveguide crossing (indicated in black) and the heaters (indicated in orange). Each ring is coupled with its neighbor by directional couplers. The crossing elements needed in each switching cell of the crossbar matrix are made by MMI waveguide crossing. The size of each switching cell is 100×115 μm^2.

Grating couplers are used for off-chip connection to optical fibers at input and output ports.

The physical effect used for switching is the thermo-optic effect with the rings heated by metal Ti/Pt micro-heaters placed on top of the ring waveguides and separated by a 1.2 μm silica cladding layer.

The switching cells have a passband of 100 GHz centered at wavelength 1551.35 nm, the loss is about 0.9 dB in *off* state and about 2 dB in *on* state, and each switching cell needs to be calibrated both for *on* and *off* operation by setting the bias voltage. The switch matrix extinction ratio is >19 dB, and the total loss is path
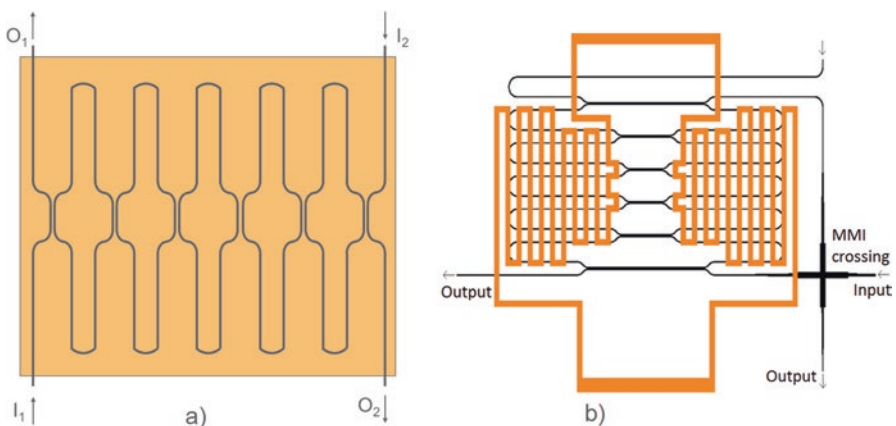

Fig. 12.13 Switching cell based on five-coupled micro-ring-resonators: (**a**) coupled rings, (**b**) layout of the complete switching cell (Courtesy of COBRA Research Institute)

dependent spanning from 14 dB for the shortest path to 25 dB in the longest path (including input and output coupling losses that count 12 dB). The *on* and *off* response time is 17 μs and 4 μs, respectively.

The drawback of this switch matrix comes from the fact that the switching cell has a limited bandwidth corresponding to the bandwidth of the micro-ring resonance. To work properly this matrix requires either a complex resonance calibration procedure at the start-up, a tuning range wide enough to comprise the system wavelength range and resonance locking to the channel wavelength during operation, or the use of fixed wavelength transmitter. This makes the matrix less attractive unless its characteristic is advantageously exploited for wavelength selective switching. The demonstrated matrix must operate with TE polarized input signals while polarization independent characteristics are necessary since the interconnect infrastructure in data center is based on single mode fibers.

12.4.2 PILOSS Switch Architecture

In crossbar switch matrices, as described above, the different signals experience different insertion losses depending on their internal path through the matrix. This aspect limits the scalability unless very low loss of few hundredths of a dB is achieved for the switching cells set in *off*. That is because a high differential loss between the signals at the matrix output results in a crosstalk increase especially in multistage optical switching fabric systems. To avoid this detrimental effect, channel power equalization has to be implemented with consequent increase in loss and device complexity. Alternatively, a *path-independent insertion loss (PILOSS) matrix* architecture may be adopted. It was proposed originally in [29] and is schematically presented in Fig. 12.14. Each cell in the matrix is connected to the four similar cells at the corners of the square surrounding that cell, and only the cells in the first and last rows are connected to the adjacent cells in the same row. The switching cell (see Fig. 12.15) is a 2×2 switch in which, in *off* state, signals at inputs I_1 and I_2 follow the diagonal paths to O_2 and O_1, respectively, while with the switch cell set in *on*, the signal at I_1 is transferred to O_1 and that at I_2 to O_2.

In a $N \times N$ PILOSS switch matrix, the number of cells the signals traverse is always constant, is independent to the path, and is equal to N. Similar to the crossbar architecture, for each path, only one switching cell is set in *on*. As an example, three path setups, namely, I_1–O_3, I_3–O_7, and I_5–O_4, are shown in Fig. 12.16 for an 8×8 PILOSS matrix.

PILOSS matrix, like the crossbar counterpart, is strictly non-blocking, and the number of switching cells in a $N \times N$ matrix is equal to N^2. The same considerations made above for the scalability of crossbar matrices are valid here, concerning the requirements of very low loss and high extinction ratio of the switching cells and waveguide crossing.

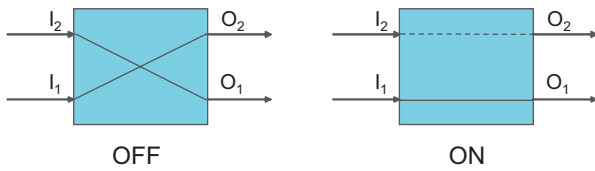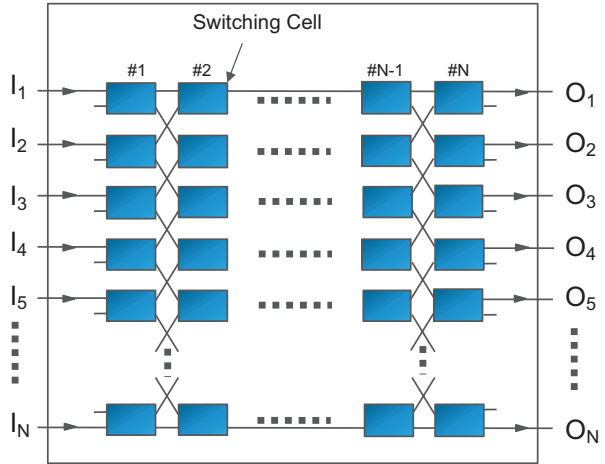**Fig. 12.14** PILOSS switch matrix architecture

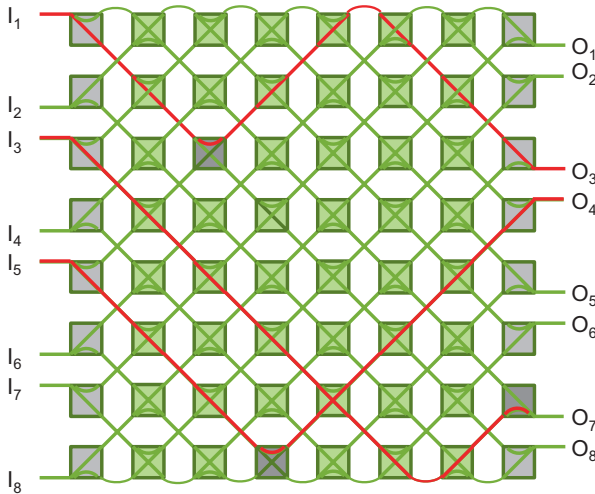
Fig. 12.15 PILOSS 2 × 2 switching cell

Fig. 12.16 Example of three optical path setups (*red lines*), I_1–O_3, I_3–O_7, and I_5–O_4, in an 8 × 8 PILOSS matrix: switching cells in *on* are indicated with *dark boxes*
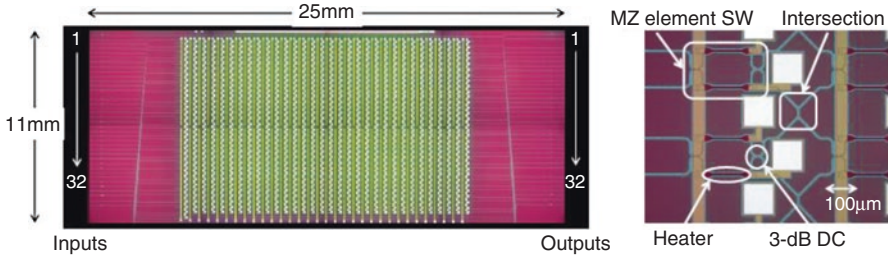
Fig. 12.17 32 × 32 Si-wire switch chip images [31]

Two types of silicon-integrated PILOSS switch matrices have been investigated and proposed recently: the 32 × 32 Si-wire switch [30, 31] and the micro-opto-electro-mechanical system (MOEMS) [32].

12.4.2.1   32 × 32 Si-Wire Switch Matrix

The 32 × 32 PILOSS matrix [30, 31] is based on the 2 × 2 MZI switching cell type described above. It was fabricated on 300 mm SOI wafer using a CMOS-compatible process. The chip integrates 1024 MZI cells (see Sect. 12.3.1), each thermally controlled by a TiN micro-heater on both arms of the interferometer and 961 waveguide crossings. The chip area is 11×25 mm^2 (see Fig. 12.17). In the MZI cells, the 3 dB couplers are directional couplers working with the TM mode. The waveguides are 430 nm wide and 220 nm high, buried in a 1.5 μm thick SiO$_2$ cladding. The waveguide crossings are made by 0 dB directional couplers (in which all the power is transferred to the adjacent waveguide) with simulated loss and isolation of 0.1 dB and 45 dB, respectively. The estimated loss of the switching cell (including one waveguide crossing) is 0.44 dB, and the extinction ratio is <35 dB but in a bandwidth of only 2.3 nm centered at wavelength 1545 nm, due to the use of wavelength-sensitive directional couplers. The complete device has an on-chip insertion loss of about 15 dB (not including fiber coupling loss), and the worst case crosstalk is estimated to be about –20 dB in a band of 1.8 nm. The switch response time is of about 30 μs, and the electrical power to set the switch cell in *on* is 45 mW, while the power to keep it in *off* is 1.5 mW (that is the power to trim the MZI).

This matrix is polarization sensitive since the directional couplers have been designed for TM polarization. Future efforts should be dedicated to widen the operating bandwidth of the device (due to the directional couplers), to reduce the on-chip loss, and to provide polarization insensitivity. A very recent work has been published in [60] reporting on a smaller size 8×8 Si-wire switch matrix with improved bandwidth and polarization diversity architecture.
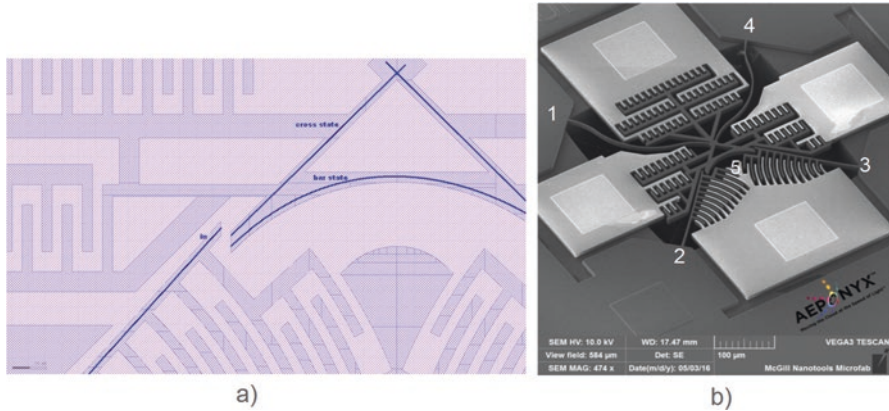
Fig. 12.18 MOEMS switching cell, (**a**) details of the waveguide coupling, (**b**) SEM picture of the switching cell (Courtesy of Aeponyx)

12.4.2.2 Micro-Opto-Electro-Mechanical Switch (MOEMS) Matrix

A new type of silicon-integrated switching cell for use in a PILOSS matrix has been proposed in [32]. It is based on a micro-opto-electro-mechanical system (MOEMS) in which comb electrostatic actuators are used to move optical waveguide ends causing light coupling into two alternative paths: the one with the straight wave-guide or the one with the curved waveguide (see Fig. 12.18a). The cell consists of a suspended element including the crossing waveguide segments 1 and 4 together with a curved waveguide segment 5 and a fixed part that includes the waveguide segments 2 and 3 (see Fig. 12.18b). When the switch cell is in *off* (*cross* state), the ends of waveguides 1 and 4 in the suspended part are aligned to the ends of wave-guides 2 and 3 of the fixed part, respectively, and the two input signals (e.g., at waveguides 2 and 3) cross the cell with very low coupling loss (going out through waveguides 1 and 4). With the switch cell in *on* (*bar* state), the ends of the wave-guides 2 and 3 in the fixed parts are aligned to the left and right ends of the curved waveguide 5 in the suspended part, and the input signal at waveguide 2 is redirected to output waveguide 3 with low coupling loss. The waveguide alignment occurs through a thin air gap of about 50 nm or less.

The alignment procedure works as follows, and it applies for setting either *on* or *off* state: firstly, the left and right actuators at the bottom of Fig. 12.16a rotate the waveguides in the fixed part to open the two air gaps. Secondly, the suspended part with the crossing and curved waveguides translates up or down. Finally, the wave-guides in the fixed part rotate back to close the air gaps.

The waveguides are composed of a Si_3N_4 core and a SiO_2 cladding to ensure low propagation losses and polarization-independent operation. The expected cell loss is about 0.2 dB (including the cell internal waveguide crossing loss and the loss in the thin air gap between fixed and movable waveguides) in *off* (corresponding to *cross* state) and 0.5 dB in *on* (corresponding to *bar* state) with a slight increase with respect to the *cross* state due to the propagation in the curved waveguide [58].
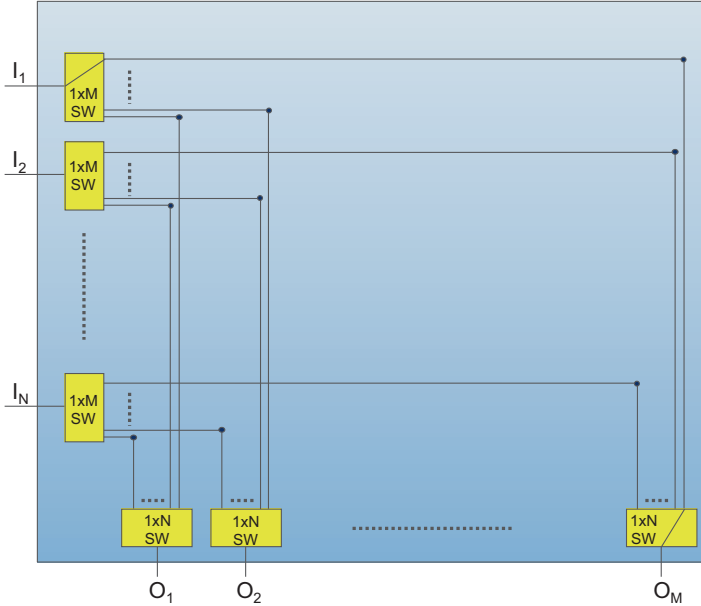
Fig. 12.19 N × M switch and select architecture

The waveguide crossing loss is estimated to be about 0.01 dB, and the propagation loss in the waveguide is estimated to be 0.6 dB/cm.

A high cell extinction ratio (>60 dB) can be easily achieved by separating the curved and straight waveguides in the suspended part by few μm.

The cell dimensions are 350×350 μm^2, and the cell response time is <200 μs.

The switch is controlled by analog voltage signals of about 150 V for the gap closer actuator (once optimized could be reduced to 100V) and about 200 V for the actuator that translates the suspended part. A 48×48 switch matrix based on the MOEMS switch elements described above is under development and the total estimated insertion loss is about 12 dB including 0.6 dB of input and output edge coupling loss. The operating bandwidth is in principle very wide, limited only by the Si_3N_4 transparency.

This matrix is slightly larger and has a longer response time with respect to the matrices presented above based on Si nanowires, but it has the relevant advantage of being polarization insensitive.

12.4.3   Switch and Select Architecture

The N × M *switch and select matrix architecture* is depicted in Fig. 12.19. It comprises of an array of N 1 × M input switches, a large passive interconnect network, and an array of M 1 × N output switches.

The input to output connections are established by appropriate selection of the paths at both the input switch array and the output switch array as indicated in the Fig. 12.19 in which the connection between I_1 and O_M is shown.

The switching elements here, instead of being distributed across the two-dimensional matrix, like in crossbar and PILOSS architectures, are concentrated in two linear switch arrays. In this switch and select architecture, each couple of switches (in the input and output arrays) is dedicated to a specific input to output connection, and hence, like the crossbar and PILOSS, it is strictly non-blocking (SNB) as it is always possible to connect idle inputs to arbitrary idle outputs independently of the already established input to output connections.

Considering a N × N switch matrix, the 1 × N switches in the two arrays could be made by cascading a number of 1 × 2 MZI-based switching cells, similar to the ones shown in Fig. 12.5 but with only one input port. The number of 1 × 2 cells in the matrix scales with the number of ports as 2 N*(N − 1). All input to output connections traverse a constant number of 1 × 2 switching stages (switching cells), like in PILOSS architecture, but here this number is lower being equal to 2*$\log_2$N instead of N. This is obtained by increasing the complexity of the passive interconnect network between the two switch arrays that must interconnect N^2 input waveguides to N^2 output waveguides. This represents the fundamental limitation to the scalability of this architecture as long as it is implemented in single optical layer photonic chips. In such an architecture, some signals, in the worst case, must traverse up to $(N − 1)^2$ waveguide crossing points resulting in a big insertion loss and in high differential loss between those unfortunate signals and the lucky signals that do not traverse any crossing. In a 64 × 64 switch matrix, the number of waveguide crossing traversed by the signals in the worst case is up to 3969, and even using waveguide crossings with very low loss of about 0.01 dB, the insertion loss and differential loss experienced by the signals could easily reach up to 40 dB that is an unacceptable value for an optical switch.

However, this architecture could be attractive in the future if multilayer photonic chip will be developed. 3D heterogeneous photonic integrated circuits have been presented in [33], and multilayer photonic chips compatible with CMOS fabrication processes and based on a Si_3N_4-SOI platform have been investigated in [34]. With a two-photonic-layer chip, the large passive interconnect network of Fig. 12.19 could be realized with the vertical connection laid out in one layer and the horizontal connections on the other layer in such a way that waveguide crossings are completely avoided and the signals could exchange layer by means of low-loss optical vias.

12.4.3.1 8 × 8 Switch and Select Optical Matrix

An 8 × 8 switch and select matrix has been implemented and reported in [35]. The 1 × 8 switch in the arrays is implemented with three stages of 1 × 2 MZI-based switching cells, each one using thermally tuned phase shifters on both arms and two adiabatic power splitters having a bandwidth wider than directional coupler-based 3 dB power splitters and a loss lower than MMI-based 3 dB power splitters. The

phase shifters have etched trench and partially removed silicon to reduce power consumption and thermal crosstalk, and they are controlled by 224 heaters made by a thin TiN layer. The passive interconnecting network is implemented on a single layer, and the waveguides are joined by the use of low-loss tight bends. The waveguide crossings are the most critical circuit in this architecture, and they have a simulated loss of 0.015 dB and a crosstalk of about −40 dB at 1550 nm wavelength. The on-chip loss, not including the fiber coupling loss, was estimated as 4 dB for the longest path, and it includes losses of 3 + 3 stages of MZI, waveguide bend, and propagation in a 1.6 cm long waveguide.

The extinction ratio of the switching cell is >16 dB in an 80 nm bandwidth from 1500 to 1580 nm. Due to the fact that for establishing an input to output connection, the path selection is made by cascading an input and an output switch, the port to port isolation of this switch matrix is increased to >30 db. The chip footprint is 8 mm × 8 mm, and the power needed by the 1 × 2 MZI switching cell is as low as 1.5 mW, while the power consumption of the matrix when all the eight connections are established is about 70 mW. The high energy efficiency is due to the isolation trenches and substrate removal in the phase shifters, but the thermal isolation affects also the response time that increased to 250 μs.

This switch, as most of the other types of demonstrated silicon photonics switching matrices presented above, works with the fundamental TE mode only, and for a practical use, it needs to be enhanced with polarization-independent characteristics. High port count in this matrix can be achieved with a photonic chip having two layers of waveguide (one for vertical and one for horizontal waveguides) in order to avoid waveguide crossings with the related losses.

12.5 Integrated Matrices with ns Response Time for Optical Packet Switching

Integrated switching matrices with very fast response time of the order of nanoseconds have recently captured high interest since, by leveraging on silicon photonics integration, they allow the implementation of optical packet switching (OPS). In OPS short data packets are exchanged between servers in a performance optimized data center (POD) entirely in the optical domain. For this application, a short reconfiguration time of the switch is needed [36, 37]. OPS enables a high energy efficiency intra-data center networking since there is no need of electro-optical and optical-electrical conversion prior to an electrical packet switch (EPS), and it also permits to obtain a lower latency. With respect to optical circuit switching (OCS), OPS has a more efficient bandwidth utilization, and it could become, in the future, the ultimate and sole switching technology replacing the electrical packet switching for intra-data center networking.

In the following, the architectures and technologies for silicon-integrated optical packet switch matrices are presented and discussed.

12.5.1 Benes Switch Architecture

The optical switch matrix architectures presented in Sect. 12.4, used for optical circuit switching, are all strictly non-blocking. In these architectures, the number of traversed switching cells is equal to N for PILOSS, 2N − 1 for the worst case in crossbar. To obtain a good scalability in such architectures characterized by a large number of traversed cells, the cell loss must be very low, as already discussed in the above sections. Switching cells based on MEMS and micro-ring resonators have loss as low as few tenths of a dB in through port (*off* state), while the loss in *cross* is less critical due to the fact that only one cell is activated for each input to output connection.

Switching cells based on MZI have been proposed in PILOSS architectures in conjunction with micro-heaters as active element since the loss introduced by the presence of the heaters on top of the waveguides is quite low. But in high-speed switching matrices, the plasma dispersion effect has to be exploited to activate the switching cells, and the total losses become too high and limit the matrix scalability to few ports (8×8 or 16×16). This is due to the fact that by injecting carriers in the phase shifters of the MZI switching cells, not only the refractive index is changed but, as non-wanted effect, the optical loss is increased due to free carrier absorption (see Sect. 12.2).

For this reason, the fast optical switching matrices proposed and experimentally demonstrated so far, instead of being SNB, adopt rearrangeable non-blocking architectures (RNB) because of a reduced number of traversed switching cells and waveguide crossings, resulting in a lower loss and lower crosstalk. However, the drawback is that, even if it is always possible to connect an idle input port to an arbitrary output port, in some cases, it may be necessary to apply an internal rearrangement of the connections already established. This drawback implies the implementation of complex switching control algorithms and it does not affect the switch performances only in switching matrices operating in synchronous time slotted mode. In such matrices all the connections are set up and torn down periodically at the same time as in the system architecture presented in [37]: only in this condition an RNB matrix becomes SNB [40].

RNB matrix architectures adopted in silicon photonics switches are the Benes architecture [38–40]. They are attractive for the low-cost index (number of switching cells in a matrix) that increases asymptotically as $O[N \log_2 N]$, to be compared with the cost index of crossbar and PILOSS that increases as $O[N^2]$.

The *Benes silicon photonics switch matrix* is constructed starting from the 2×2 MZI switching cell, already presented in Sect. 12.3.1 and shown in Fig. 12.5. A Benes matrix with an arbitrary size of $N \times N$ is recursively constructed starting from a top Benes sub-matrix of size $N/2 \times N/2$ and an equal bottom Benes sub-matrix of equal size. The two sub-matrices are interconnected by N/2 2×2 MZI switching cells included in two extra-symmetrical stages, named Banyan stages. In the Banyan stages, one port of each 2×2 switching cell is connected to the top sub-matrix and the other to the bottom sub-matrix, as depicted in Fig. 12.20.
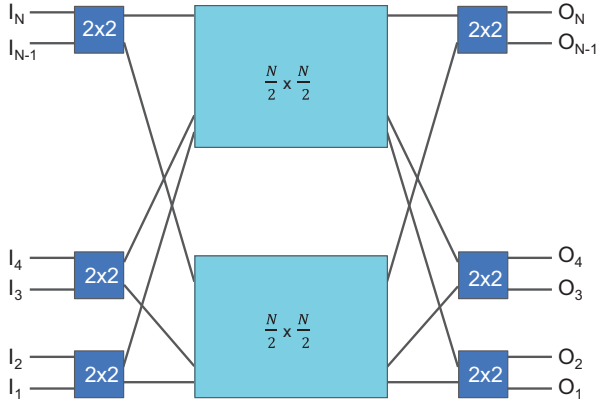
Fig. 12.20 Construction of an arbitrary size Benes switching matrix

A N × N Benes switch matrix has a number of stages equal to:

$$S_N = \left(2\log_2 N - 1\right) \tag{12.16}$$

The number of switching cells in each stage is:

$$C_S = 2^{(\log_2 N - 1)} \tag{12.17}$$

An example of the Benes matrix scaling is depicted in Fig. 12.21 starting with the 2 × 2 MZI-based switching cell and then showing the 4 × 4 matrix and the 8 × 8 matrix.

Two Benes switch matrices have been demonstrated recently and are reported in the following.

12.5.1.1 16 × 16 Benes Switching Matrix

A 16×16 integrated silicon photonics switching matrix based on MZI cells with Benes architecture has been presented in [41]. It comprises seven stages and eight switching cells on each stage and it was fabricated on a SOI wafer with a thin 220 nm silicon layer on top of a 2 μm thick BOX layer. The MZI switching cells were similar to the type shown in Fig. 12.5 with two broadband MMI-based 3 dB couplers and two arms of equal length: one arm is equipped with both a high-speed p-i-n phase shifter and a thermo-optic phase tuner, while the other arm is equipped with the thermo-optic phase tuner only. The thermo-optic tuner sections are used for compensating phase error due to fabrication and to set *cross* state at the initialization. They are made by TiN micro-heaters with 300 μm length placed on top of the waveguides. Air trenches surrounding the waveguides are used to improve
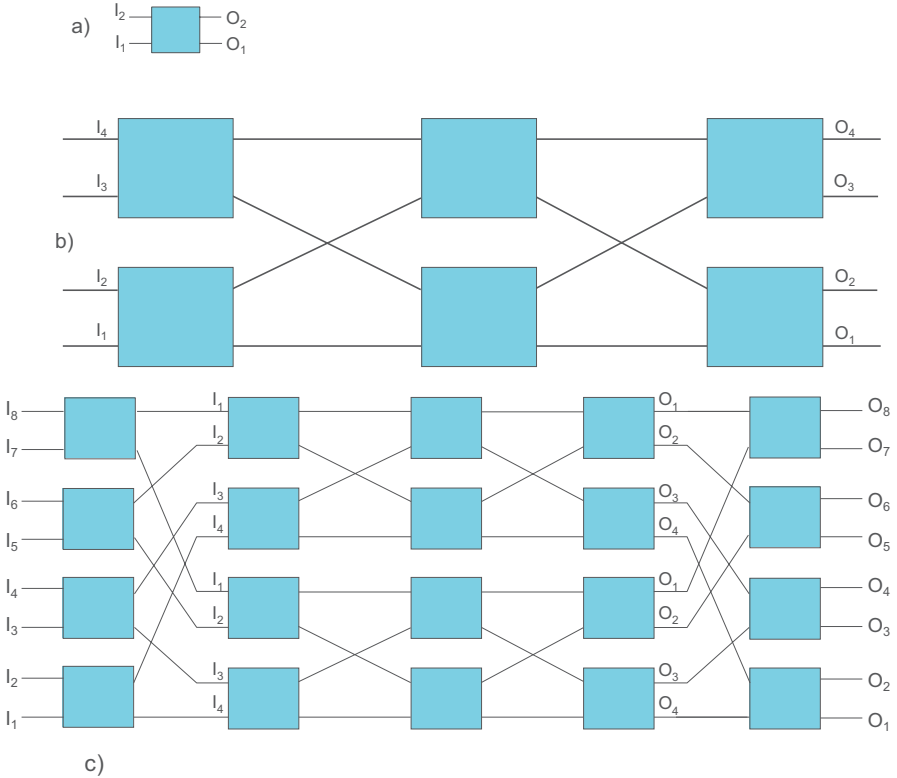
Fig. 12.21 Scaling a Benes matrix: (**a**) 2×2 MZI switching cell, (**b**) 4×4 Benes matrix, (**c**) 8×8 Benes matrix

energy efficiency of the phase tuner. The p-i-n diode phase shifter, used for fast switching, has a length of 380 μm and heavily doped $p+$ and $n+$ regions with carrier concentration of about 10^{20} cm^{-3}.

The switching cell average loss when the state is in *cross* is about 0.4 dB in the wavelength range of 1530–1590 nm, and the extinction ratio is >30 dB in a 30 nm wavelength band. When the switching cell is in *bar* state, the loss increases to 1 dB, and the extinction ratio decreases to 18 dB due to free carrier absorption in the p-i-n phase shifter. The on-chip insertion loss (not including input and output coupling loss) is 6.7 dB for a path of all *cross* states and 14 dB for a path of all *bar* state. The chip crosstalk is −20 dB for all *cross* states and −10 dB for all *bar* states. The response time is about 3 ns and the chip area is 10.7 x 4.4 mm². The worst case power consumption of the thermo-optic tuners is 881 mW and that of the plasma dispersion-based phase shifters is 289 mW. This device works with TE polarized input signals.

12.5.1.2   32 × 32 Benes Switching Matrix

A higher-radix, high-speed monolithically integrated silicon photonics matrix has been demonstrated in [42]. Similar to the previous matrix, it also has Benes architecture and MZI-based switching cells. The matrix is composed of 9 stages with 16 switching cells at each stage. The chip was fabricated with a 180 nm CMOS production process and comprised of 144 switching cells and 416 waveguide crossing with a chip area as small as 12.1×5.2 mm^2. The cells are made by two MMI 3 dB couplers and two p-i-n-based phase shifter at both arms of the interferometer having 200 μm length and 450 nm width, driven in push-pull configuration.

The matrix insertion loss was 12.8 dB, and the crosstalk was in the range from -19.2 to -25.1 dB in a 50 nm wavelength bandwidth from 1525 to 1575 nm.

This device to operate correctly needs TE polarized input signals and the response time of the MZI switching cells is 1 ns.

In [42] together with this 32×32 fast switching matrix, a 64×64 Benes matrix based on MZI cells is presented using the thermo-optic effect as switching mechanism. It has lower loss (12.8 dB) and lower crosstalk (<30 dB) in the 50 nm wavelength bandwidth from 1525 to 1575 nm and a slower response time.

12.6   Silicon Photonics Wavelength-Selective Switch Matrix

In many of the optical switching network architectures proposed so far for data center networking [43–46], wavelength division multiplexing has been introduced in order to increase the link capacity of each single fiber connection. In such architectures, *wavelength selective switches* (*WSS*) work in conjunction with optical space switches to provide connectivity among data center equipments (compute and storage nodes).

Similarly, to the space switch matrices presented and discussed in the above sections, also for wavelength selective switching, high-capacity, highly integrated, and low-cost devices are needed.

A promising technology for the realization of large-scale integration silicon photonics WSS is the one based on micro-ring resonator (MRR) switch elements and researched in the EU FP7 project IRIS[1] (Integrated Reconfigurable silicon photonic-based optical Switch) [47]. The IRIS switch device has been implemented as 4×8 transponder aggregator (TPA) block of a colorless-directionless-contentionless reconfigurable optical add drop multiplexer (*CDC ROADM*), but a similar switch architecture can be used for a NxN WSS device for data center applications.

The schematic block diagram of the IRIS WSS switch is depicted in Fig. 12.22.
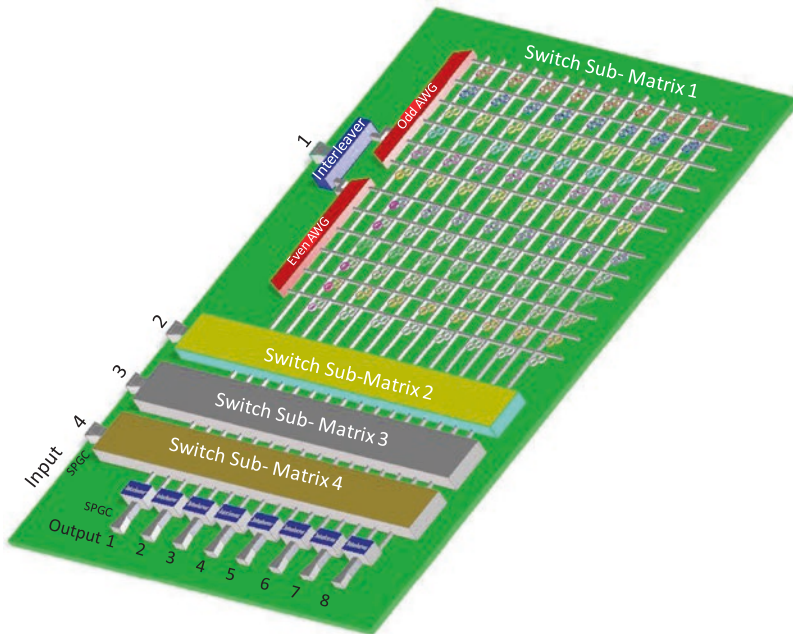
Fig. 12.22 IRIS switch architecture

It has four input line ports and eight output local ports. At each input line port, it receives a comb of 12 multiplexed wavelengths, 200 GHz spaced. Single polarization grating couplers (SPGC) are used to couple the optical signals from the input fiber array to the chip silicon waveguides. Interleaver circuits separate the input channels into odd and even in order to double the channel spacing and relax the channel isolation requirement of the following arrayed waveguide grating (AWG)-based demuxes and that of the switch matrix. Two AWG demux circuits, the odd one and the even one, are used to separate the various channels in the wavelength combs received at the device input. At the demux output, the individual signals are sent to the switching matrix constituted by a crossbar of optical waveguides equipped with micro-ring resonator (MRR) switch elements at each crosspoint. The matrix has 4×12 rows (each row dedicated to a certain wavelength) and 8×2 columns (one column for odd wavelengths and one for even wavelengths). In the switching matrix, the channels travel along the row corresponding to the wavelength until they intersect the column connected to the wanted local output port to which the channel has to be dropped. At this crossing point, by thermally tuning the corresponding MRR in resonance with the signal wavelength, the signal is transferred to the corresponding drop column (see Fig. 12.23). Note that an interleaver recombines the odd and even wavelengths coming from two distinct columns before the drop port. SPGCs are used at the drop ports coupling the output signals to the optical fibers. The same device described above can be used in the reverse direction to add wavelengths from local ports to line ports.
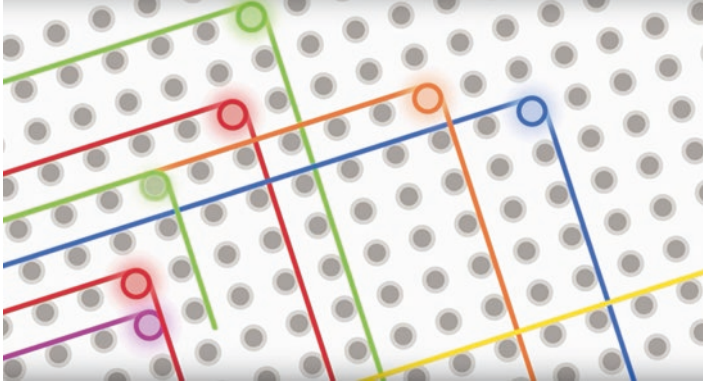
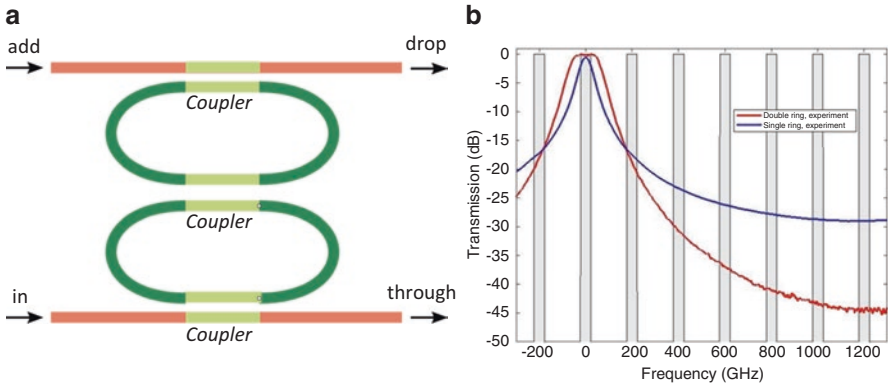**Fig. 12.23** Working principle of the IRIS wavelength selective switch matrix

Fig. 12.24 Double ring circuit (**a**), single and double ring frequency response (**b**). *Gray bars* indicate 50 GHz bandwidth

In a TPA device, only one wavelength is dropped on each column due to the fact that a TPA connects the line switch to the transponders, while in a NxN wavelength selective switch for data center, more than one wavelength can be dropped on each column.

The IRIS switch has been implemented on a 8" SOI wafer with 220 nm thin silicon layer on a 2 μm BOX layer. The main waveguides of the circuits are 480 nm width strip waveguides.

High ER of the switching cell in *off* state is achieved by shifting the MRR far enough from the channel wavelength. In order to achieve a wide-enough 1-dB bandwidth of about 50 GHz and a high-enough ER > 35 dB, the MRR-based switch elements are made with two-coupled micro-rings as shown in Fig. 12.24a. In Fig. 12.24b, the spectral response of the MRR switching cell is shown for both single ring (blue curve) and two-coupled rings (red curve) .
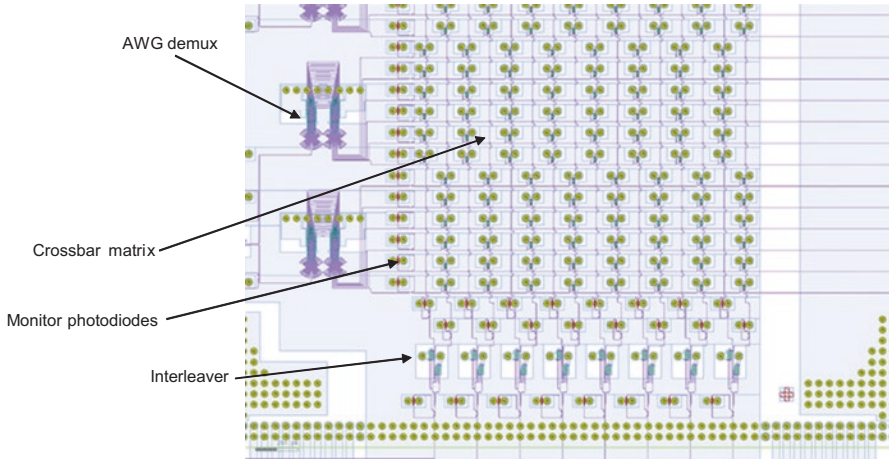
Fig. 12.25 IRIS circuit layout details
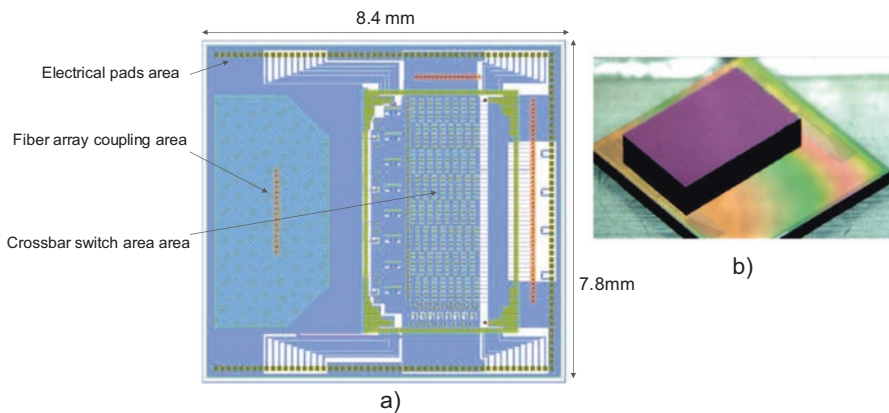
Fig. 12.26 (**a**) IRIS chip layout, (**b**) 3D integration with the control electronic chip (Courtesy of LETI fab)

Details of one section of the chip including the optical circuits are shown in Fig. 12.25.

The chip size is 8.4 mm × 7.8 mm (see Fig. 12.26a). A large portion of the chip area is dedicated to fiber coupling and electrical pads, while a smaller portion comprises photonic circuits.

The two-coupled ring loss with the switch element in *off* is <0.02 dB, while the loss when the switching cell is in *on* is <1 dB. MRR ER at 1000 GHz shift is >40 dB, and the tuning efficiency is 23 mW/FSR (with an FSR of about 20 nm). Crossing loss is <0.03 dB.

The interleavers are infinite impulse response (IIR) filters consisting of a MZI and a ring resonator on one arm [48]. Interleaver channel isolation is >20 dB, while the loss is <1 dB [49]. The AWG channel separation is 400 GHz, the insertion loss is <3 dB, and the channel isolation is >25 dB.

3D integration of the photonic chip with its control electronic chip is shown in Fig. 12.26b: it has been realized by the use of micro-pillar interconnect arrays.

Like most of the silicon photonics switching matrices demonstrated so far, also IRIS switch works with input signals having TE polarization, and further developments are needed for a polarization-insensitive device.

12.7   Switch Matrices Comparison Table

The characteristics of the various switch matrices discussed in the above sections are summarized in Table 12.1.

All matrices are polarization sensitive but one, and they need a further development step to implement polarization-insensitive devices.

For optical circuit switching, the 64 × 64 digital MEMS switch has the lowest on-chip loss and fastest switching time with good performances in terms of extinction ratio and crosstalk but it is polarization sensitive. The MOEMS switch has promising performances in terms of loss, extintion ratio and polarization insensitivity even if it has a larger size and slower response time but a high radix switch matrix is still under development. The 8 × 7 resonant cell matrix is fundamentally narrowband, and it is more suitable for wavelength selective switching, while the 32 × 32 Si-wire switch has a limited spectral response and it is polarization sensitive but very promising improvements in terms of bandwidth and polarization insensitivity have been achieved very recently on a 8 × 8 matrix. The 8 × 8 switch and select matrix has scalability issue, but it could be an interesting option in case of implementation in a multilayer photonic chip. Fast 16 × 16 and 32 × 32 Benes matrices are interesting candidates for optical packet switching applications provided that they become polarization insensitive. The same is valid for IRIS switch that is an attractive technology for integrated wavelength selective switching devices.

12.8   Perspectives and Research Directions

The advancements reported above in the implementation of scalable, highly integrated optical switching matrices in silicon photonics are encouraging for the future realization of commercial products that could enable a pervasive use of optical switching in data centers. These optical matrices will have a high port count (64x64 or more), low power consumption in the order of few watts, high speed either in the order of microseconds for optical circuit switching or of nanoseconds for optical packet switching, low chip area of about tens of squared mm, low cost, wide

Table 12.1 Integrated switch matrices comparison

| Switch type | Parameter | | | | | | | |
	Cell loss (dB)	Pol. independent	Cell size (μm^2)	ER (dB)	Blocking perf.	Speed (μs)	Bandwidth (nm)	Refs.
64 × 64 Digital MEMS	0.026/0.47 (*off/on*)	No	110 × 110	>60 (in *off*)	SNB	0.28/0.91 (*off/on*)	300	[27]
8 × 7 Resonant cells	0.9/2 (*off/on*)	No	100 × 115	>19.5 (all matrix)	SNB	4/17 (*off/on*)	0,8	[28]
32 × 32 Si-wire	0.44	No		>35	SNB	30	2.3	[30, 31]
MOEMS	0.2/0.5 (*off/on*)	Yes	350 × 350	>60	SNB	200	Very wide (Si_3N_4 transparency)	[32, 58]
8 × 8 Switch and select	<4 (all matrix)	No	8 × 8 mm² (all matrix)	>30	SNB	250	80	[35]
16 × 16 Benes	0.4/1 (*cross/bar*)	No	10.7 × 4.4 mm² (all matrix)	>30/18 (*cross/bar*)	RNB	0.003	60	[41]
32 × 32 Benes	12.8 (all matrix)	No	12.1 × 5.2 mm² (all matrix)	>−19.2 (crosstalk of all matrix)	RNB	0.001	50	[42]
IRIS switch	0.02/1 (*off/on*)	No	100 × 100	>40 (in *off*)	SNB	<4	0.4	[47]

transmission band supporting switching of high-speed signals of >100 Gbps, and wide wavelength operating range (>30 nm).

However, some technical challenges have to be met for the realization of commercial devices in the near future.

The switch matrix loss should be further reduced by improving the loss characteristics of the switching cells and reducing the fiber coupling loss. Heterogeneous integration of optical gain blocks in the switch matrix to compensate for internal losses has been proposed. Demonstration of semiconductor optical amplifier (SOA) array integration and packaging for a scalable silicon photonics switching matrix has been presented in [50]. The integration of SOAs in a high radix switching matrix has the drawback of increasing significantly the power dissipation in the chip and it requires an appropriate packaging for the heat removal that impacts the device form factor. However, it could allow not only the use of simpler optical transceivers with relaxed power budget but also the realization of higher radix strictly non-blocking matrix architectures since a higher number of cascaded switching cells are permitted by the loss compensation. The impacts on the optical signal integrity caused by ASE noise accumulation in the cascaded SOA, especially in a large multi-stage optical switch fabric, should be investigated.

In some of the presented switching cell types, the extinction ratio, the bandwidth, and the operating wavelength range must be improved to become really attractive. Since the switch matrix performances are determined not only by the characteristics of the switching cells but also by the matrix topology, new matrix architectures able to reduce crosstalk without increasing too much the loss and complexity needs to be investigated. In [59] a 32 × 32 silicon photonics matrix of thermally controlled MZI switching cells has been realized by modifying a dilated Benes architecture. It has low crosstalk but it is reconfigurable non blocking and for use in optical circuit switching blocking could occur and has to be minimized to avoid limitations in the full utilization of the switch capacity.

Most of the integrated switching matrices demonstrated so far are polarization sensitive, while polarization insensitivity is an absolute characteristic for use in data centers since the optical fiber infrastructure is made by single-mode fibers: future efforts should be dedicated to realize large-scale integration devices with polarization-insensitive characteristics. This can be achieved either by implementing polarization diversity schemes [51, 52] or, when possible, by designing the waveguide circuits and the switching cell structures [53] with low polarization sensitivity.[2]

An effective integration between the optical chip and its control electronic complement is fundamental. Due to the very high interconnection density required, two different approaches have been investigated, the monolithic integration of control electronics with the photonics [54–56] and the 3D hybrid integration with the electronic chip on top of the optical chip, interconnected to each other by micro-solder bumps [47]. Both approaches need further development to reach the maturity required for commercial deployment.

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[2] After the preparation of the manuscript an interesting paper has been published presenting a work on a polarization insensitive silicon photonics 50 × 50 switch matrix [53].

The manufacturing processes should be improved to reduce the fabrication imperfections of the integrated optical circuits that require fine tuning to compensate with the consequent increase in power consumption and calibration complexity. Moving the silicon photonics fabrication to more advanced CMOS nodes and the use of silicon wafer with a better thickness uniformity are strongly recommended.

Last but not the least is the packaging issue. Due to the high impact of packaging on the device cost and since the number of input and output fiber interfaces is high, new technological advances are definitely needed. Two packaging aspects should be researched: the realization of a high-density I/O connection of silicon photonic chip with optical fibers and the realization of low-cost, removable, low-loss, and mass-manufacturable optical connectors. Experiments on a high-dense optical packaging for a high-radix silicon photonic switch are reported in [57] using a hexagonal pitch-reducing optical fiber array (PROFA).

The implementation of silicon photonics high-radix switching matrices is a research area in a rapid evolution, and it may be envisaged that completely new types of switching cells based on new technologies and with low loss and low crosstalk, suitable for large-scale integration, will be invented in the near future.

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