Efficient transistor level implementation of selected fuzzy logic operators used in control systems

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Abstract. The paper presents a novel, transistor level, implementation of selected fuzzy set operators suitable for fuzzy control systems realized in low-power hardware. We propose a fully digital, asynchronous realization of basic fuzzy logic (FL) functions, such as the bounded sum, bounded difference, bounded product, bounded complement, fuzzy logic union (MAX) and fuzzy logic intersection (MIN). All of the proposed operators has been implemented in the CMOS TSMC 180nm Technology and verified by means of transistor level simulations in Hspice environment. The proposed structures of the FL functions can easily be scaled to any signal resolutions.

Keywords: fuzzy systems, fuzzy operators, CMOS implementation

1 Introduction

A large interest in the fuzzy systems (FSs) and their possibilities are mainly due to the fact that the surrounding world is inherently fuzzy. Using only bivalent logic we are unable to properly describe many real world problems. The bivalent logic allows us for only a hard selection between the TRUE and the FALSE values. Such approach is insufficient in most systems, including, for example, control systems used in the automotive industry. Fuzzy sets offer more natural description of various problems, important for example from the point of view of vehicle control, however there is a demand for efficient rules how to process fuzzy logic (FL) data. Even if such rules are already known, and well described,

W. Mitkowski et al. (Eds), *Trends in Advanced Intelligent Control, Optimization and Automation*, Advances in Intelligent Systems and Computing 577, DOI 10.1007/978-3-319-60699-6_76

there is still a demand for their efficient implementation in hardware with limited resources, e.g. in embedded systems or in application specific integrated circuits (ASIC).

The properties of the fuzzy set theory resulted in its widespread use in many fields of automatic and control systems [1], in electric and electronic engineering [2], [3], [4], [5] in medicine in forecasting, planning and decision-making [6], [7].

It frequently happens also that FSs cooperate with neural networks (NNs) in control systems, leading to even better results [8]. There are also known such cases, in which the NN only supports the work of the FS. In this case we say about the neuro-fuzzy networks [9], [10]. A characteristic feature of these networks is their ability to use fuzzy inference methods to calculate the values of output signals. In contrast to conventional fuzzy systems (fuzzy logic), the systems in which NNs are involved offer adaptive selection of selected parameters, e.g. the shapes and parameters of the membership functions.

Fuzzy systems can be implemented using different techniques. The most popular way is their software realization. This is due to the ease of such implementation and test execution, as well as their large flexibility - modification abilities. On the other hand, such realizations are not suitable for many industry applications that require miniaturization, low energy consumption and low cost per unit.

Hardware implementations of FSs play an important role in many industrial applications in which FL is being used [11]. Such realizations include programmable devices such as microcontrollers (μC) [12] and FPGAs (Field Programmable Gate Arrays) [11], [13], [14]. FL systems are also realized as analog [15], [16], [17], [18], digital or mixed [19] ASICs. In case of analog approach the circuits are usually realized using the current-mode technique, in which summing and subtracting operations (commonly used in FL) are realized simply in junctions.

In the comparison with analog circuits, digital circuits offer several important advantages. The inherent regeneration of logic levels in logic gates involves high noise immunity and low sensitivity to the variance of transistor parameters. This allows for accurate and reliable data and signal processing. Additionally binary data can be easily stored even for a long period of time. This facilitates the realization of even very large, programmable, multi-stage fuzzy data processing.

In case of digital solutions a frequently asked question is whether to use the standard cell or the full-custom technique. The first approach is convenient, as in this case the designer usually only cares about the behaviour of the circuit (the logic), while generation of the layout is done automatically by design environment. The full-custom methodology, on the other hand, is much more flexible, as the designer can decide about every aspect of both the circuit and the layout design. In general, in both cases the target is layout, while the basic question is who is able to design a circuit with better parameters (human or machine). To our best knowledge, FL operators were not implemented as digital full-custom ASICs so far. We decided to use this technique, as particular FL operators proposed in this paper offer simple structure and can be very quickly designed

without using standard-cell approach. Additionally, in standard-cell technique we are limited to existing cells, which is often insufficient especially if there is foreseen a close cooperation of digital blocks with analog components.

To enable usage of FSs in modeling of real processes, it is important to implement families of parametric FL operators that can be easily tuned, in order to obtain better simulation results of the FSs. On-board and real-time applications of FSs require larger data processing rates. To achieve these objectives, we work on programmable, fast, miniaturized FL operators realized in hardware.

In this paper we present the realization of main FL operators, such as: bounded sum, bounded difference, bounded product, bounded complement, fuzzy logic union (MAX) and fuzzy logic intersection (MIN). In next Section we provide formulas describing these operators, as well as the proposed circuits representing them. In following Section we present transistor level verification of the proposed solutions in the 180 nm CMOS technology.

2 Basic Fuzzy Logic functions and their hardware implementation

The FL functions are defined in terms of the membership functions μ_A and μ_B. In the literature on can find more than ten basic FL functions [16], [18]. We focus on selected functions of this group as presented in this Section. All these functions have been implemented by us in the TSMC CMOS 180 nm technology using only basic digital combinational circuits that include standard AND, OR, XOR, NOT gates, as well as more complex circuits, designed from scratch, shuch as multi-bit full adder and subtractors that in some cases play the role of digital the comparators.

The proposed designs, presented below, can be very easily scaled down to any newer CMOS technology.

2.1 Fuzzy logic union(MAX) and Fuzzy logic intersection (MIN)

The FL union and intersection functions, as described using two formulas, respectively:

$$\mu_{A\vee B} = \max(\mu_A, \mu_B) \tag{1}$$

and

$$\mu_{A\wedge B} = \min(\mu_A, \mu_B) \tag{2}$$

Both these operators have a similar structure. For this reason we propose a programmable circuit, shown in Fig. 1, that can be easily switched over between both these functions. A multi-bit full subtractor (MBFS) is used in the role of the comparator (CMP). This component is realized a chain of 1-bit full subtractors (1BFS), coupled through the borrow in (B_{IN}) and borrow out (B_{OUT}) signals (not shown in the Figure). The B_{OUT} signal from the most significant 1BFS

becomes '1' in case, if the signal provided to the positive input of the comparator is smaller than its negative input signal. The B_{OUT} signal trough the XOR gate controls the multiplexer, which provides to the outputs of the overall FL circuit either the smaller or the larger input signal.

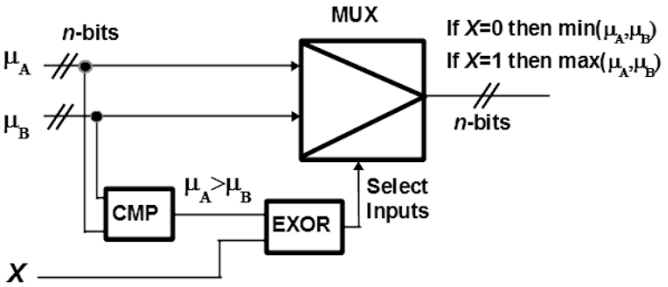

Fig. 1. Hardware implementation of the MIN and MAX FL functions.

2.2 Bounded complement

The bounded complement FL function is a multivalued extension of the binary NOT operation. It can be described using the formula:

$$\bar{\mu_A} = \mathbb{1} - \mu_A \tag{3}$$

The proposed corresponding circuit is shown in Fig. 2. It is based on the MBFS that subtracts the input signal μ_A from the maximum possible value, for a given signal resolution, n (in bits). The maximum value, equal to 2^n-1, is represented by the $\mathbb{1}$ symbol in 3. For example cases of 4 and 8 bits, the $\mathbb{1}$ equals (in HEX) 0xF or 0xFF, respectively.

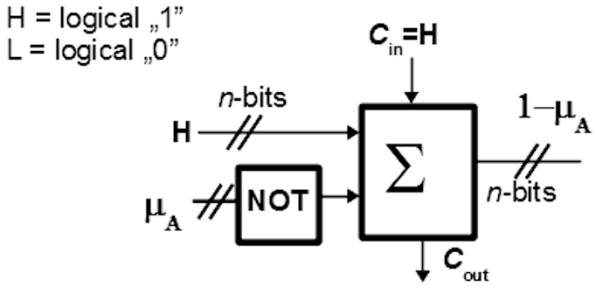

Fig. 2. Hardware implementation of the fuzzy complement function

2.3 Bounded sum

The bounded sum FL function is defined as follows:

$$\mu_{A \oplus B} = \min[\mathbb{1}, (\mu_A + \mu_B)] \tag{4}$$

The proposed circuit that is an example implementation of 4 is shown in Fig. 3. In the circuit, a multi-bit full adder (MBFA) is used to calculate the sum of both input signals. It is composed of a chain of 1-bit full adders (1BFAs), coupled through the carry-in (C_{IN}) and carry-out (C_{OUT}) signals (not shown for the simplicity).

If $\mu_A + \mu_B > \mathbb{1}$ then the C_{OUT} from the most significant 1BFA becomes 1 and this signal through the OR logic gate sets all output signals to '1'. The resolution of the output signal equals the resolution of the μ_A and the μ_B signals. It is so, to avoid the situation in which any operator increases or decreases the resolution of the original input signals.

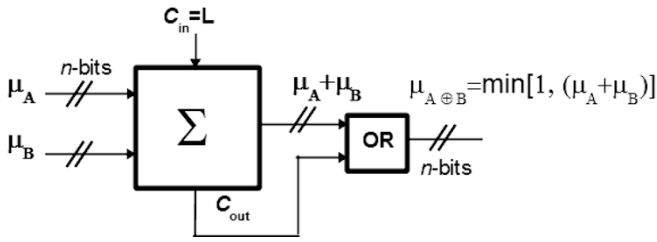

Fig. 3. Hardware implementation of the bounded sum function

2.4 Bounded difference

The bounded difference FL function is defined as follows:

$$\mu_{A \ominus B} = \max[0, (\mu_A - \mu_B)] \tag{5}$$

An example corresponding circuit is shown in Fig. 4. Here the structure of the circuit is a bit similar to the circuit shown in Fig. 3. Instead of using MBFA we use MBFS. If $\mu_A < \mu_B$ then $B_{\mathrm{OUT}} = 1$ which throughout the NOT and the AND gates sets all outputs of the circuit to '0'.

2.5 Bounded product

Bounded product FL function is the last one presented in this paper. It is described using the formula:

$$\mu_{A \odot B} = \max[0, (\mu_A + \mu_B - \mathbb{1})] \tag{6}$$

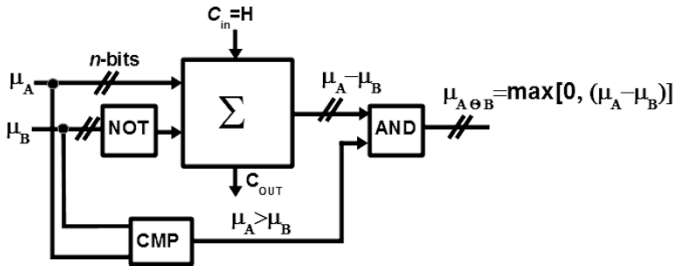

Fig. 4. Hardware implementation of the bounded difference function

The structure of the proposed circuit requires a bit more explanation. Here we have two add / sub operations: $\mu_A + \mu_B - \mathbb{1}$. The $\mathbb{1}$ equals the maximum value, for example 0xFF for the resolution of 8 bits. To subtract this number from the $\mu_A + \mu_B$ term, we can add its reversed and complemented value (U2 code) to the $\mu_A + \mu_B$ term. Independently on the signal resolution, the reversed and complemented value always equals '1', so it is sufficient to add the '1' signal at the least significant position. This allows to substitute the full scale MBFA with an incrementing circuit, that features a substantially simpler structure and thus consumes less power. An example corresponding circuit is shown in Fig. 5

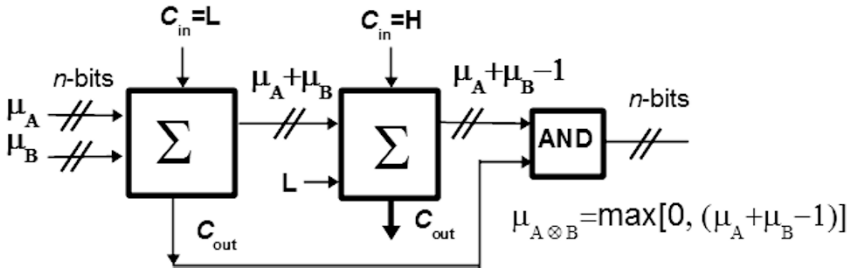

Fig. 5. Hardware implementation of the bounded product function

3 Transistor level verification of the proposed FL circuits

Verification of the proposed circuits have been made in Hspice simulation environment in the CMOS 180 nm technology. We performed the, so called, corner analysis in which the proposed circuits have been verified against the process, voltage and temperature (PVT) variation. A series of performed tests covered several transistor models, namely typical (T), fast (F) and slow (S), for temperatures varying in-between -20 and 100 °C and different values of the supply voltage (from 1.2 to 1.8 V). The signal resolution in the tests shown in Figs. 6–11

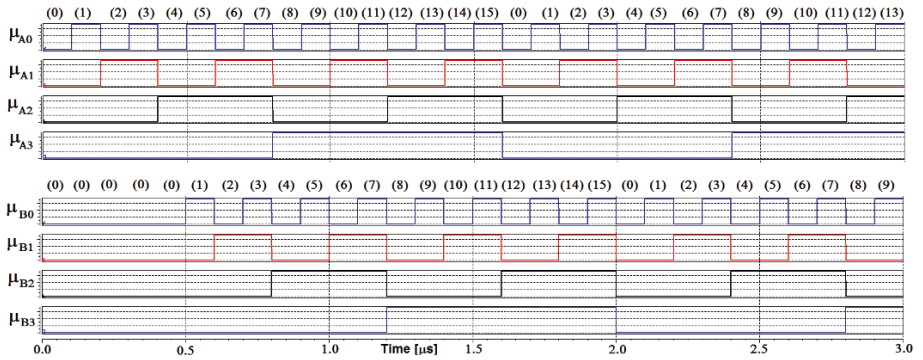

Fig. 6. Input signals

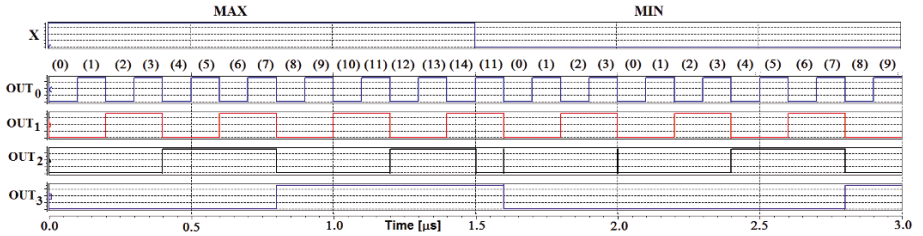

Fig. 7. Verification of the MIN and the MAX FL functions.

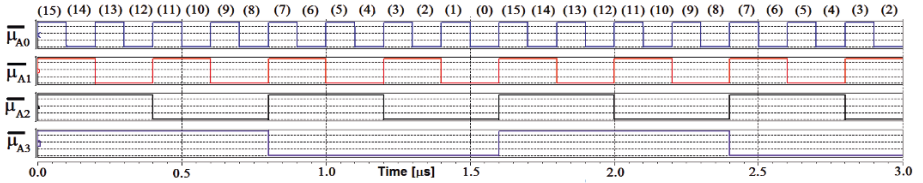

Fig. 8. Verification of the fuzzy complement function

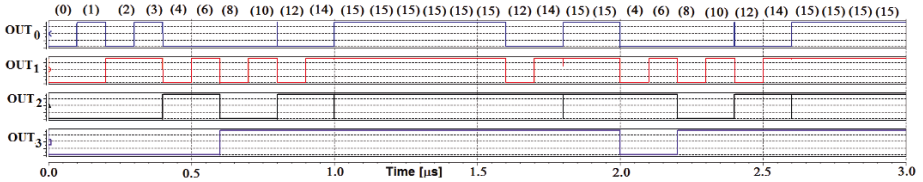

Fig. 9. Verification of the bounded sum function

was 4 bits, i.e. the real value of $\mathbb{1}$ was 0xF. During the tests the input signals varied from 0 to 0xF.

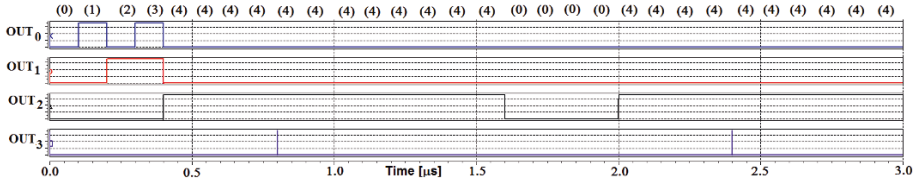

Fig. 10. Verification of the bounded difference function

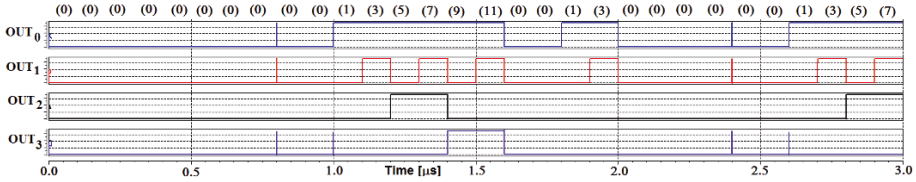

Fig. 11. Verification of the bounded product function

Verification on the logic level is an obvious test, and all the circuits worked properly. Our goal was to check also dynamic parameters i.e. delays introduced by particular operators, as well as the consumed energy. Selected results are shown in Fig. 12. The response time of particular operators varied from 0.25 ns for the complement operator to 0.6 ns for the bounded difference operator. There was also observed an influence of the PVT parameters. The difference between the worst case (S/1.2) and the best case (F/1.8 V) scenarios was about 120 %, however in each of the tested cases the circuit worked properly (at the logic level). Since the circuits are designed in the CMOS technology, therefore the static current is very small, while the circuits consume energy mostly during changing their state. For this reason, independently on data rate, the energy consumed per a single calculation is almost constant and varies from 0.54pJ to 1.26pJ, for bounded complement and bounded product, respectively. Taking the presented values into account, it can be estimated that in case of larger fuzzy systems in which, for example, ten operators are used in chains, the expected data rate will be even 200-400 MSamples/s.

4 Conclusions

In the paper we present a novel transistor-level implementation of selected fuzzy logic operators, suitable for very fast, low power dissipation applications. The proposed circuits operate fully asynchronously, which means that no clock generator is required to perform particular FL operations. The circuits can be used in larger fuzzy systems working in parallel, with whole chains of the operators working asynchronously.

Particular operators, designed in the CMOS 180 nm technology, are very fast and offer data rates at the level of even several GSamples/s. These parameters

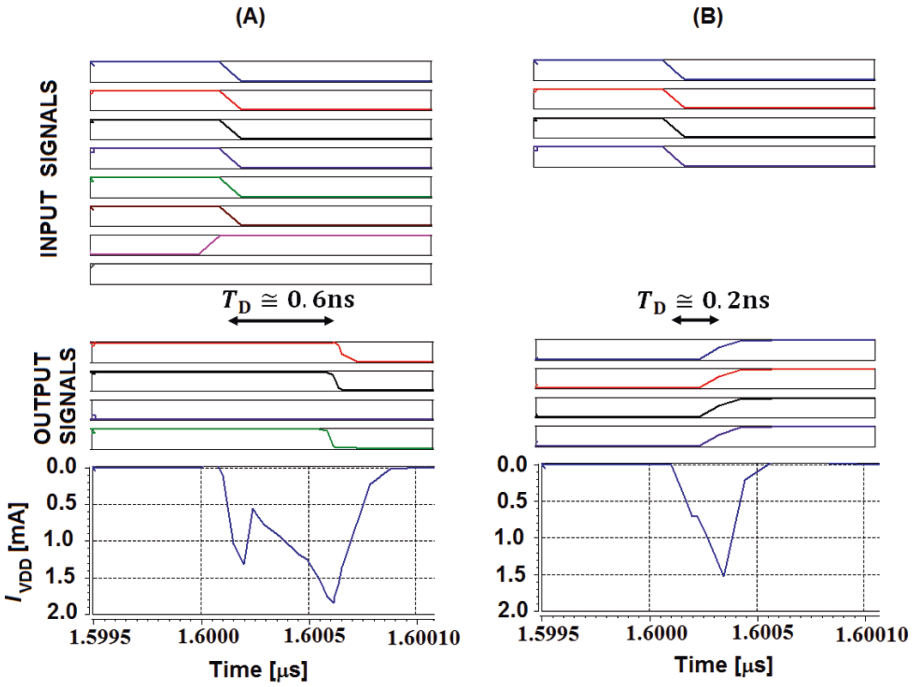

Fig. 12. Illustration of the delay introduced by the bounded product and bounded complement operator and corresponding current consumption. (A) - bounded product (B) - bounded complement

can be substantially improved if the circuits will be redesigned in newer CMOS technologies. The circuits were designed in full-custom style. The structures of the used full adders and full subtractors have been proposed by the authors. The aim was minimization of the number of transistors in these circuits.

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