A Method to Reduce Resources for Quantum Error Correction

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Abstract. In a quantum logic circuit, the minimum number of qubits required in a quantum error-correcting code (QECC) to correct a single error was shown by Laflamme to be five. Due to the presence of multi-control gates in the circuit block for a 5-qubit QECC, this block cannot be readily implemented with present day technology. Further, the fault-tolerant decomposition of the QECC circuit block requires a large number of quantum logic gates (resources). In this paper, we (i) propose a smaller 5-qubit error detection circuit which can also correct a single error in 2 of the 5 qubits, and (ii) establish how to use a 3-qubit error correction circuit to correct the single errors when detected in the other 3 qubits. This approach to quantum error-correction circuit design, functionally equivalent to a 5-qubit QECC, yields a significant reduction in the number of quantum logic gates. For a given quantum logic circuit, we also provide a scheme to decide the locations where these error detection and error correction blocks are to be placed in attaining reduction in gate requirement compared to the case where the original 5-qubit QECC block is used. A comparative study of the resource requirement for the benchmark circuits shows that the proposed method outperforms even Shor and Steane codes in terms of resources. Thus, our proposed method provides quantum error correction with minimum qubit requirement and reduced resource requirement on the average.

1 Introduction

The evolution of a quantum state is mathematically represented by a unitary transformation. Quantum computing is reversible since any unitary matrix U has an inverse which is equal to its complex conjugate ($U^\dagger$). However, the state of interest, which is referred to as the system, may be coupled with some other quantum state, which is referred to as the environment. When this composite system undergoes some unitary evolution, the evolution of the constituent states may not be unitary. This incorporates error in the quantum system. An error is nothing but an operator. It is best represented when the state of the system is denoted by the density matrix notation [1,2] as $\rho = \sum_i p_i |\psi_i\rangle\langle\psi_i|$ where p_i is the

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probability that the system is in the state $|\psi_i\rangle$. For a pure state $|\psi\rangle$, the density matrix is simply $|\psi\rangle\langle\psi|$. If an error E occurs on the state ρ with probability p, then the evolution of the state is denoted as

$$E(\rho) = (1-p)\rho + p.E\rho E^{\dagger} \tag{1}$$

A quantum error correcting code $\mathcal{R}$ is a mapping such that the composition of $\mathcal{R}$ with E gives back the original quantum state, i.e.,

$$(\mathcal{R} \circ E)(\rho)(E^{\dagger} \circ \mathcal{R}^{\dagger}) = \rho \tag{2}$$

An error in a quantum system can also be modelled as a quantum channel. Some quantum error models include Amplitude damping channel, Phase damping channel and Pauli channel [1,2]. In this paper, we have considered the Pauli channel as the error model. The Pauli matrices $\mathbb{I}$, X, Z and Y form the basis for 2×2 dimensional operator space [1]. Hence a code which can correct the Pauli errors can also correct any linear combination of them, i.e., all errors in the 2×2 space. If the error probability is p and the probability of each of X, Z and Y errors is considered to be equal ($\mathbb{I}$ implies no error and hence is not considered), then the evolution of the quantum system is given as

$$E(\rho) = (1-p)\rho + \frac{p}{3}(X\rho X^{\dagger} + Z\rho Z^{\dagger} + Y\rho Y^{\dagger}) \tag{3}$$

2 Resource Requirement for 5-Qubit QECC

A quantum operation may be realized by one or more quantum gates forming a network of gates or a circuit. Given a quantum system for performing certain operations, a quantum circuit has to be obtained with minimum number of gates, which are also termed as resources. The depth of the circuit and the number of operations to be executed are also important factors in designing a quantum circuit. Additionally, such a circuit requires quantum error correcting code (QECC) for error-free operations. But the QECC also requires a circuit block to be designed appropriately.

Several QECCs have been proposed in the literature to correct a single error in a qubit [3–6]. Gottesman has provided a group theoretic model of errors in a quantum system. His stabilizer formulation provides an operator-level mechanism for correcting quantum errors [7]. It has been shown by Laflamme et al. [5] that in order to correct a single error in a qubit, the information of the qubit must be distributed into at least 5 qubits. An important aspect of this code by Laflamme is that the encoding and the decoding circuits are identical. Furthermore, it is extremely difficult to maintain the superposition of a qubit. Hence, the 5-qubit code provides a better option for error correction than the other codes [3,4,6].

The encoding and decoding circuits of the 5-qubit code, proposed by Laflamme [5], has a number of multi-control gates, which cannot be implemented readily in modern day technologies. Due to the presence of these multi-control

operations, the fault-tolerant decomposition requires a large number of gates. Also these gates can be noisy, and incorporate errors in the circuit. Moreover, the error correction requires a significant amount of time due to more gate operations and thus hinders the speed of the computation. FTQLS [8] provides the fault-tolerant decomposition of any quantum circuit in different technologies viz. Ion Trap (IT), Quantum Dot (QD), Linear Photonics (LP), Non-linear Photonics (NP), Neutral Atom (NA) and Superconductor (SC). In Table 1, we compare the number of gate operations and the number of cycles per operation for Shor, Steane and Laflamme codes for each of the six available technologies, as obtained from FTQLS. It is evident from Table 1 that while the qubit requirement of Laflamme code is low, the gate count is significantly larger than for the other two codes.

Table 1. Comparison of gate count and number of cycles of both encoding and correction circuits for QECCs of Shor, Steane and Laflamme respectively

QECC	Technology	Qubits	Ancilla	Total number of qubits	Gate count	Cycles
Shor	IT	9	8	9 + 8 = 17	105	24
Steane		7	6	7 + 6 = 13	85	30
Laflamme		5	-	5	1641	1432
Shor	QD	9	8	9 + 8 = 17	133	116
Steane		7	6	7 + 6 = 13	127	191
Laflamme		5	-	5	3353	19602
Shor	LP	9	8	9 + 8 = 17	56	164
Steane		7	6	7 + 6 = 13	55	172
Laflamme		5	-	5	1751	2310
Shor	NP	9	8	9 + 8 = 17	56	196
Steane		7	6	7 + 6 = 13	55	206
Laflamme		5	-	5	2437	2566
Shor	NA	9	8	9 + 8 = 17	87	22
Steane		7	6	7 + 6 = 13	95	29
Laflamme		5	-	5	1892	1657
Shor	SC	9	8	9 + 8 = 17	84	196
Steane		7	6	7 + 6 = 13	85	242
Laflamme		5	-	5	2604	9070

In order to overcome these shortcomings, we have proposed a smaller 5 qubit circuit for error detection which can also correct errors in 2 of the 5 qubits. Given a quantum circuit, one can insert this detection circuit block at certain points in the given circuit so that if an error is likely to be detected, only then the correction circuit block is also placed. We have computed the time interval for placing this error detection block to obtain reduction in resources. We

have also shown the percentage savings in the resource requirement for different benchmark circuits using this proposed technique.

Shor and Steane codes require more qubits for error correction than the code by Laflamme (refer Table 1). However, the resource requirement of the former two is much less than for the 5 qubit code. Hence once can argue that these two codes be used rather than the proposed technique which requires both detection and correction steps in the worst case. However, we show that in average case, our proposed technique requires less resources than the Shor and Steane codes too. Hence, this technique is superior both in terms of qubits as well as resources.

The paper has been organised as follows. In Sect. 2 we propose a new quantum circuit for error detection and compute the time interval for placing this block in a quantum circuit. Section 3 shows the use of the error detection circuit along with a 3 qubit error correction circuit to replace the error correction circuit of the 5 qubit code. We also show the percentage savings provided by this method. In Sect. 4, we show the percentage savings in different benchmark circuits. We conclude in Sect. 5.

3 5-Qubit Quantum Error Detection Circuit

In classical computing, error may cause the bit to flip from 0 to 1 or vice versa. However, in quantum computing, a qubit can incur bit flip or phase flip errors, or both [9]. Thus quantum error correction has two requirements: detection of the type of error and detecting the location of the error. While the former operation is possible using 4 qubits only [10], at least 5 qubits are necessary for both operations [5]. A code which is capable of detecting only the type of error is called a quantum error detection code, while a quantum error correction code can both detect the type and its location. Qubit is an essential resource which must be minimized in quantum computation. This is because it is difficult to preserve the superposition nature of a qubit. Any modification of the original superposition results in loss of information [1]. So using 5-qubit code is preferable for error correction since it requires the minimum number of qubits. However, Table 1 shows that this code has significantly large resource requirement.

In this paper, our proposal is to place a quantum error detection block at certain points in the circuit. If error is likely to be detected, only then the correction block is also placed there. However, the 4-qubit error detection code is not applicable here because encoding the information of a single qubit into 4 qubits only will not allow to correct errors when necessary. The qubit should be encoded using the 5-qubit code by Laflamme to allow error correction whenever necessary.

We propose a 5-qubit error detection block as shown in Fig. 1. This block can act on the 5-qubit system which has been encoded using Laflamme code. In Fig. 1, $|q_0\rangle$ up to $|q_4\rangle$ are the data qubits and the last four are ancilla qubits. $|q_5\rangle, |q_6\rangle$ check for bit error while $|q_7\rangle, |q_8\rangle$ check for phase errors. This block checks whether the first four and the last four qubits are in the same state. If they are not, then an error is detected. Instead of the error correcting block in [5],

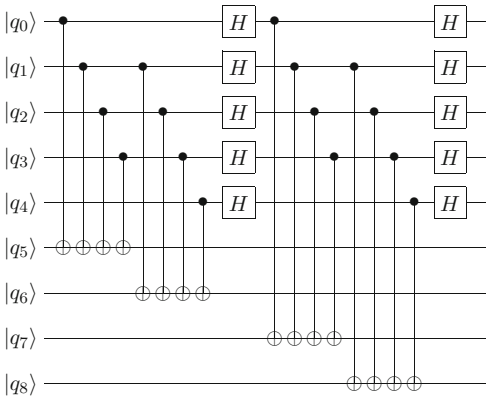

Fig. 1. Proposed 5-qubit error detection block

we place the detection block of Fig. 1 after certain time interval. The correction block is placed at the location where an error is likely to be detected.

A salient question arises here: at which locations should the error detection and the error correction blocks be placed in a given quantum circuit? We provide a bound on the time interval that can be allowed between two error detection blocks, in terms of the probability of error. This time interval may vary with the technology used, since the probability of error at a quantum gate or of decoherence (memory error) differs with the technology for implementing it. Furthermore, if the error detection block is placed at intervals greater than this bound, then the larger error correction block is mandated and hence resource reduction cannot be achieved.

Let p be the error probability per nanosecond (ns), D and C be the gate count of the 5-qubit detection circuit and the 5-qubit correction circuit respectively. We consider that we check for errors at interval of n ns. The probability of no errors occurring after n ns is $(1-p)^n$, and hence the error probability is $(1-(1-p)^n)$. When a single error occurs, then the resource requirement is $(D+C)$ since both error detection as well as correction block must be placed. It is only D when there is no error. So the resource requirement for each time error correction is performed, is

$$(1-p)^n.D + (1-(1-p)^n).(D+C) \tag{4}$$

If this technique is not used, then after each time interval only the correction block is placed, i.e., the resource requirement is C each time. For our proposed method to be advantageous, the resource requirement of this method should be at most C, i.e.,

$$(1-p)^n.D + (1-(1-p)^n).(D+C) \leq C \tag{5}$$

A simple calculation gives us the following inequality

Table 2. Gate counts D and C for error detection and correction in various technologies

Technology	# Gates for error correction (C)	# Gates for error detection (D)	$\frac{D}{C}$
IT	843	36	0.043
SC	1301	34	0.026
LP	874	26	0.03
NP	1217	26	0.021
NA	900	34	0.038
QD	1518	52	0.034

$$(1-p)^n \geq \frac{D}{C} \tag{6}$$

We have used FTQLS [8] to obtain the fault-tolerant version of the error correction block [5] and the error detection block (Fig. 1). The ratio of D to C is provided in Table 2. Note here that in Table 1, we reported the total gate count for both encoding and correction blocks. However, since the encoding block remains same in both cases, in Table 2 we have the gate count of the error correction block of the Laflamme code only to compare with the proposed error detection block.

In [11], the authors have addressed error tracing in quantum circuits. They have placed error correction blocks only when the error probability exceeds a predefined threshold. This technique has allowed them to reduce the required number of error correction blocks significantly compared to the ideal case. Similarly, we propose that error correction can be performed after certain time gap of n *ns*. For different values of p, the inequality of (6) enables us to the find the maximum permissible value of n for obtaining a circuit with very low probability of error. In Table 3, we give the estimated error probability in different technologies as obtained from [12].

Table 3. Probability of worst gate and memory error in different technologies [12]

Technology	Probability of gate error	Memory error (per ns)
QD	9.89×10^{-1}	3.47×10^{-2}
NA	8.12×10^{-3}	0.00
LP	1.01×10^{-1}	9.80×10^{-4}
NLP	5.20×10^{-3}	9.80×10^{-5}
SC	1.00×10^{-5}	1.00×10^{-5}
IT	3.19×10^{-9}	2.52×10^{-12}

In Table 4, we show the values of n for different values of p in the technologies considered. We have varied p from 10^{-8} to 10^{-1}. However, certain error

Table 4. Time interval $n(ns)$ of error detection with error probability p ranging from 10^{-5}/ns to 10^{-1}/ns) for different technologies

Technology	$p = 10^{-8}$	$p = 10^{-7}$	$p = 10^{-6}$	$p = 10^{-5}$	$p = 10^{-4}$	$p = 10^{-3}$	$p = 10^{-2}$	$p = 10^{-1}$
IT	84397007	8439701	843970	84397	8440	844	84	9
SC	×	×	3649657	364965	36495	3648	364	35
LP	×	×	×	350655	35064	3505	349	34
NP	×	×	3863231	386322	38631	3862	385	37
NA	×	32701690	3270168	327016	32701	3269	326	32
QD	×	×	×	×	×	3380	337	33

probabilities are too low for some of the technologies; for example $p = 10^{-9}$ for QD (see Table 3) is not feasible. Such entries in Table 4 are denoted by a '×'.

Thus Table 4 provides an upper bound of the time interval between placing two error detection blocks in a quantum circuit for a particular technology.

4 Savings in Resources by Our Proposed Method

We consider the proposed quantum error detection circuit of Fig. 1 once more. After the quantum error detection block is placed, one needs to check the syndromes in the 4 ancilla qubits, of which first two indicate bit error and last two indicate phase error. We consider only the bit flip error syndrome for the time being. If the syndrome is 00, it indicates that the circuit is free of bit error. If the syndrome is 10, it indicates that the last four qubits are in the same state, but the 1st four qubits are not. This is possible only if error has occurred in the 1st qubit. Similarly, if 01 is the syndrome, then it is possible to determine that the 5th qubit has error. However, if the syndrome is 11, then it is not possible to determine which of the remaining 3 qubit is erroneous. The similar is true for syndromes for phase flip errors too. Thus when there is any error on the 1st or last qubit, this error detection block can both identify the error type and its position; hence can correct it.

If error is in one of the other 3 qubits, then this proposed error detection circuit can detect it, but cannot determine its position uniquely. So we need to place the error correction block. However, when the error syndrome is 11, we are sure that the error is not in the first or last data qubit. Hence it is not necessary to place the 5-qubit error correcting block to correct errors in one of 3 qubits. Rather, we place a 3-qubit error correction block as shown in Fig. 2.

We now consider the worst case scenario, where an error has been detected by the error detection block of Fig. 1 but this block cannot correct it. So we need to place the 3-qubit error correcting block of Fig. 2. In this scenario our proposed technique requires the maximum resource (5-qubit error detection + 3-qubit error correction). In Table 5, we show the percentage savings that the worst case scenario of our proposed technique gives over the ideal situation of placing a 5-qubit error correction block. From the table we see that for all technologies, our proposed technique provides an average reduction of 94.70% with respect to [5].

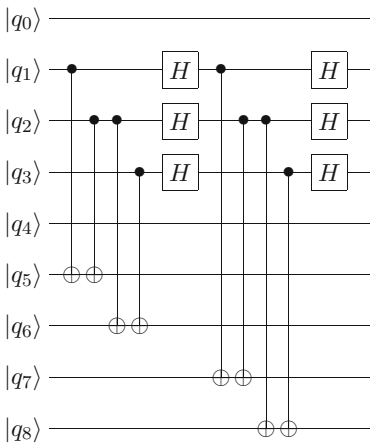

Fig. 2. 3-qubit error correcting block

Table 5. Percentage savings by using the proposed technique over the 5-qubit QECC

Technology	Ideal 5-qubit EC	Detection block	3-qubit EC	Total	Savings (%)
IT	843	36	28	64	92.4
SC	1301	34	22	56	95.7
LP	874	26	14	40	95.4
NP	1217	26	14	40	96.7
NA	900	34	22	56	93.8
QD	1518	52	36	88	94.2
Average savings (%) with respect to [5]					94.70

5 Resource Savings Analysis

In Table 5, we have shown the percentage savings compared to Laflamme code for worst case scenario. However, it is not expected that each time both the detection and correction block need to be placed. At a location where the probability of error is almost zero, placing the detection block alone is sufficient. In this section, we provide an analysis of the resource requirement.

In [11], the authors have introduced the mechanism of error tracing for linear and concatenated Bacon-Shor [6], Steane [4] and Knill C_4 code [13]. 5-qubit error correction code was not used for error tracing purpose. Here, we use a similar approach for different error thresholds and compute the percentage savings in resources. Using the technique of [11], we propose placing the error correction and detection block after some predefined threshold. Let the error threshold be p_{th}. So, we place both the detection and correction block only when the error

Table 6. Comparative study of savings in different benchmark circuits

Circuit Name	PMD	Threshold	# QECC in [11]	Resource in [11]			Our resource	Savings (%) with respect to Steane Code
				9 qubit	7 qubit	5 qubit		
2 qubit Grover's Search	IT	0.001	0	0	0	0	0	-
		0.01	0	0	0	0	0	-
		0.1	0	0	0	0	0	-
	SC	0.001	0	0	0	0	0	-
		0.01	0	0	0	0	0	-
		0.1	0	0	0	0	0	-
	LP	0.001	20	840	760	17480	521	31.45
		0.01	20	840	760	17480	523	31.18
		0.1	20	840	760	17480	548	27.89
	NP	0.001	21	882	798	25557	547	31.45
		0.01	9	378	342	10953	236	30.99
		0.1	0	0	0	0	0	-
	NA	0.001	21	1218	1050	18900	715	31.90
		0.01	10	580	500	9000	343	31.40
		0.1	1	58	50	900	37	26.00
	QD	0.001	33	3036	2277	50094	1718	24.55
		0.01	33	3036	2277	50094	1728	24.11
		0.1	33	3036	2277	50094	1835	19.41
4 qubit Reversible Adder	IT	0.001	0	0	0	0	0	-
		0.01	0	0	0	0	0	-
		0.1	0	0	0	0	0	-
	SC	0.001	2	116	100	2602	69	31.00
		0.01	0	0	0	0	0	-
		0.1	0	0	0	0	0	-
	LP	0.001	104	4368	3952	90896	2706	31.55
		0.01	104	4368	3952	90896	2719	31.20
		0.1	104	4368	3952	90896	2850	27.90
	NP	0.001	104	4368	3952	126568	2706	31.55
		0.01	51	2142	1938	62067	1334	31.16
		0.1	7	294	266	8519	192	27.82
	NA	0.001	127	7366	6350	114300	4321	31.95
		0.01	57	3306	2850	51300	1950	31.58
		0.1	19	1102	950	17100	688	27.58
	QD	0.001	189	17388	13041	286902	9835	24.59
		0.01	189	17388	13041	286902	9897	24.10
		0.1	189	17388	13041	286902	10509	19.42
4 qubit quantum Fourier Transform Circuit	IT	0.001	0	0	0	0	0	-
		0.01	0	0	0	0	0	-
		0.1	0	0	0	0	0	-
	SC	0.001	5	290	250	4215	171	31.6
		0.01	0	0	0	0	0	-
		0.1	0	0	0	0	0	-
	LP	0.001	233	9786	8854	203642	6062	31.54
		0.01	233	9786	8854	203642	6091	31.20
		0.1	233	9786	8854	203642	6385	27.88
	NP	0.001	233	9786	8854	283561	6062	31.54
		0.01	117	4914	4446	142389	3059	31.20
		0.1	15	630	570	18255	411	27.89
	NA	0.001	237	13746	11850	213300	8064	31.95
		0.01	117	6786	5850	105300	4004	31.56
		0.1	18	1044	900	16200	652	27.56
	QD	0.001	558	51336	38502	847044	29037	24.58
		0.01	558	51336	38502	847044	29217	24.11
		0.1	558	51336	38502	847044	31025	19.42
3 qubit Bernstein Vazirani search circuit	IT	0.001	0	0	0	0	0	-
		0.01	0	0	0	0	0	-
		0.1	0	0	0	0	0	-
	SC	0.001	0	0	0	0	0	-
		0.01	0	0	0	0	0	-
		0.1	0	0	0	0	0	-
	LP	0.001	21	882	798	18354	547	31.45
		0.01	21	882	798	18354	549	31.20
		0.1	21	882	798	18354	576	27.81
	NP	0.001	21	882	798	25557	547	31.45
		0.01	9	378	342	10953	236	30.99
		0.1	0	0	0	0	0	-
	NA	0.001	19	1102	950	17100	647	31.90
		0.01	8	464	400	7200	274	31.50
		0.1	1	58	50	900	37	26.00
	QD	0.001	23	2116	1587	34914	1197	24.58
		0.01	23	2116	1587	34914	1205	24.07
		0.1	23	2116	1587	34914	1279	19.40
Average savings (%) with respect to Steane Code								28.34

probability $p = p_{th}$. From Eq. 4, the expected resource requirement for placing the detection and/or correction block each time is

$$(1 - p_{th})D + (1 - (1 - p_{th}))(D + C) = D + p_{th}C.$$

This equation gives the expected resource requirement when the error detection and/or correction block(s) are placed. In Table 6, we show the expected percentage savings in resource for different benchmark quantum circuits. In addition to comparing our technique with the ideal situation of placing the 5-qubit error correcting code, we also compare our proposed technique with Shor and Steane codes.

It can be observed from Table 6 that Steane code has the minimum resource requirement of the three codes (Shor, Steane and Laflamme). The percentage savings shown in this table is with respect to Steane code only, since it has the minimum resource requirement. Our proposed technique shows an average resource reduction of 28.34% over Steane code [4].

Another observation from the benchmark table is that with the increase in probability threshold, the percentage savings decreases, i.e., the resource requirement of our proposed technique increases. This is natural because if when the error threshold is increased, the probability of error occurring increases. Hence, it is more likely to detect errors for higher threshold. So the probability that both detection and correction block needs to be placed increases with the increase in error threshold. Hence the resource requirement of the proposed technique also increases, resulting in a decrease in the percentage savings.

The resulting values from the benchmark circuits (Table 6) clearly show that our proposed technique has minimal resource requirement and minimum qubit requirement and hence is superior to all the three error correcting codes considered (Shor, Steane, Laflamme).

6 Conclusion

In this paper we have proposed a technique to replace the 5 qubit error correction code. Though this code requires the minimum number of qubits, its resource requirement is extremely high since it contains a few multi-control gates. These gates cannot be directly implemented in a fault-tolerant manner, and the fault-tolerant decomposition requires a large number of gates. Our proposed technique uses two steps: error detection, and if error is likely to be detected, then error correction. The total qubit requirement does not increase in this technique. One can still perform error correction with 5 qubits only. However, in the original 5 qubit code [5], no ancilla qubits are required for error correction. But our proposed technique requires 4 ancilla qubits. Nevertheless, these qubits are all initialized to $|0\rangle$ and the superposition property of these qubits are not necessary for the proposed mechanism. Hence effectively they behave like reversible bits and can be reused more than once.

We have shown the percentage savings that the technique proposed here provides. Furthermore, we have used our technique on some benchmark circuits

too and have shown the savings in gate count. Hence, this method provides a way for performing error correction using the minimum number of qubits and also reduces the gate count significantly. A future prospect will be to find the minimum resource requirement for quantum error correction and to check where our proposed technique stands compared to it.

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