Chapter 9
ASIC Design

This chapter deals with the final steps for a prototype development, according to the methodology introduced in Sect. 2.1:

12 Study of a suitable architecture to be integrated into an ASIC, based on results obtained from validation of concept with discrete components electronics.
13 Design and production of a low-noise position sense interface based on a standard CMOS technology.
14 Experimental characterization of a multi-chip prototype.

9.1 Architecture

In order to develop a final system for detection of earth magnetic field some more considerations must be taken into account to design an ASIC with respect to the first demonstrative prototype based on discrete components, as shown in Chap. 8. First set of measures followed an accurate phase of electromechanical characterization of devices useful to make a selection of fully working parts and detect their resonance frequencies. MEMS are then glued close to readout electronics and used for magnetic field measures. Thus, it is known for each device the precise frequency to be used for current excitation at resonance. This procedure works well during a research and prototyping phase but it is affordable to follow the same procedure for industrialization and mass production, due to amount of parts to be characterized and related costs.

These remarks lead to the need to evaluate whether a closed-loop or an open-loop control is preferable for the final two chips system [1]. The first control type, closed-loop, requires a feedback network to drive the driving block and adjust the driving frequency around device resonance frequency. In this way, neglecting variation which can be due to device to device quality factor variation, any device is driven at the correct frequency always providing the maximum output signal and so

C. Buffa, *MEMS Lorentz Force Magnetometers*,
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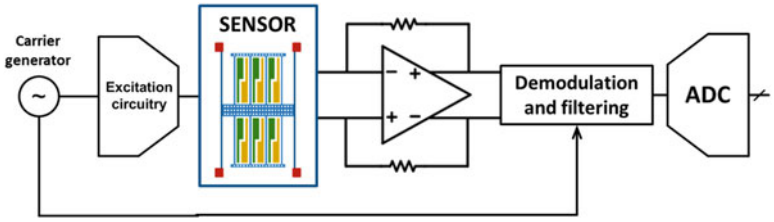

Fig. 9.1 Simplified block diagram of an open-loop implementation. Oscillator signal is used both to drive excitation circuit and as a reference for a synchronous demodulation filtering technique

guaranteeing a relatively good repeatability among samples. On the other hand, in an open-loop system, driving frequency must be set directly tuning oscillator parts or, in case a digital to analog converter (DAC) is used for excitation, storing the correct value of driving frequency in a memory (i.e., with an initial calibration after production; any sensor usually has an initial calibration/self-test after production).

The choice about loop typology is mainly made according to power consumption considerations, as they represent an extremely important specification for systems to be embedded in battery powered devices. Main blocks of driving and readout electronics (at least as far as frontend is concerned) are in common for both open-loop and closed-loop control. This latter has a higher power consumption due to the feedback network to tune oscillation frequency, in addition to a larger ASIC occupied area. Taking into account this general system level remarks, an open-loop architecture is implemented (schematically shown in Fig. 9.1). The problem related to driving frequency tuning still remains.

As emerged with electromechanical tests, even once the magnetometer type is chosen, it is not reliable to set a priori a driving frequency. To this problem, two possible solutions can be proposed: an auxiliary circuitry measures the device resonance frequency either after production as final test before commercialization or when the compass application is executed. Even in this second case, the additional power consumption related to self-test would not affect the overall power consumption during application execution. In this way, the main problem related to open-loop control could be overcome.

After deciding control system type, frontend electronics must be chosen. As sensors are based on a differential capacitive scheme, a differential readout electronic architecture is consequently chosen. Analysis reported in Sect. 8.2 still applies to ASIC development with the exception that a fully differential operational amplifier should be used (instead of two single-ended stages) to minimize phase shift between the two channels, to reduce noise contribution, and to avoid active gain stages mismatches which might affect the overall closed-loop transfer function of positive and negative inputs.

In case of Lorentz force magnetometers driving current signal, which is at resonance, represents a “high-frequency” carrier which is amplitude modulated by capacitance variation and so by magnetic field. With an approach based

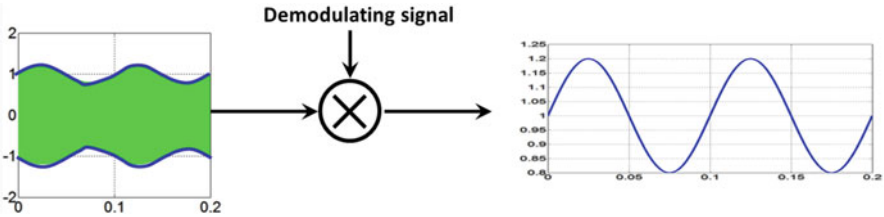

Fig. 9.2 Schematic representation of a synchronous demodulation scheme to detect carrier envelope containing magnetic field information

on synchronous demodulation, before analog to digital conversion, the envelope containing magnetic field information can be extracted (Fig. 9.2). Demodulation circuit depends on driving signal type: either a sine wave or a square wave. A typical demodulator for the first case is based on Gilbert cells with the main drawback of higher power consumption not negligible with respect to analog frontend. The latter, instead, can be demodulated using a set of switches to multiply by $+1$ and -1; it can be implemented using MOSFET gated by a reference signal controlled from oscillator. A sinusoid driving signal has main advantages to avoid noise folding and require a lower bandwidth in analog chain. Yet, circuitry to generate a sine wave and for related demodulation is usually more complex. Thinking of a final integrated system, the choice of a square wave based driving allows to save power consumption.

A final remark about system design is related to minimum and maximum magnetic field to be sensed and so the dynamic range of the system. A full scale range (FSR) of ± 100 μT is requested according to given specifications (for magnetic field measurement with good linearity) but it is a good design strategy to increase further to cope with external magnetic field which may saturate the device:

$$\begin{aligned} \text{FSR} &= \pm 1.2 \text{ mT} \\ B_{\text{min}} &\sim 1 \text{ μT} \end{aligned} \tag{9.1}$$

and the corresponding dynamic range is:

$$\text{DR} = 20 \cdot \log\left(\frac{2.4 \text{ mT}}{1 \text{ μT}}\right) = 67.6 \text{ dB} \tag{9.2}$$

9.2 A Continuous-Time Fully Differential Transresistance Amplifier

An integrated circuit was implemented aiming at improving resolution and demonstrating the feasibility of a double-chip (MEMS + ASIC) magnetic field sensing system for consumer applications. A first prototype of VLSI, based on a topology

similar to the one used for discrete components circuitry, has been designed in a standard CMOS 150 nm process. A negative feedback double-channel transresistance amplifier is designed using a fully differential operational amplifier; a simplified schematic is shown in Fig. 9.3. This choice rejects all mismatches that would occur when using two separate single-ended stages. In the differential configuration indeed offset drifts, temperature effects, and long term stability of the active component affect the two channels in the same way. In order to design the first analog stage to couple to MEMS the following blocks are required:

- high-gain, ultra-low-noise, fully differential amplifier with a suitable feedback network;
- common mode feedback network to set and stabilize both input and output biasing levels;
- output buffers to monitor signals without loading the outputs of the amplifier.

9.2.1 ASIC Noise

As calculated in Sect. 4.3, the overall noise budget for ASIC is:

$$\sqrt{S_{B_{\text{eln}}}} = \sqrt{S_{B_{\text{mech}}}} = \sqrt{\frac{S_{B_{\text{TOT}}}}{2}} = 223 \text{ nT}/\sqrt{\text{Hz}} \,. \tag{9.3}$$

which must account for:

- Analog interface noise: the complete analog signal path between sensor and ADC (if it is a digital product) or output PAD (for an analog product);
- ADC quantization and thermal noise (if a digital output is needed);
- Digital post-processing noise (i.e., quantization noise).

ADC and digital post-processing will not be discussed in this manuscript but their noise must be accounted for. A possible design approach is to equally split noise budget between analog interface and ADC, under the assumption that digital noise is almost negligible. Alternatively, sensor analog interface sets the SNR of the full signal chain and ADC noise is negligible. This type of optimization depends on architectures, area, and power consumption considerations for each specific case. ASIC noise budget reported in Eq. (9.3) can be converted in terms of capacitance resolution according to:

$$\begin{aligned} \sqrt{S_{C,\text{eln}}} &= 2C_0 \cdot \frac{\sqrt{S_{x,\text{eln}}}}{g} \\ &= 2C_0 \cdot \frac{Q}{k} \cdot \frac{I \cdot L \cdot \sqrt{S_{B,\text{eln}}}}{g} \\ &= 158 \text{ zF}/\sqrt{\text{Hz}} \,, \end{aligned} \tag{9.4}$$

for an optimized device.

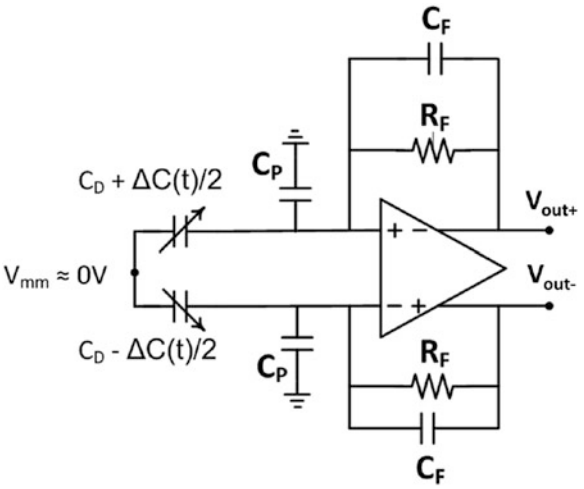

Fig. 9.3 Fully differential transresistance amplifier with MEMS modelled as a differential variable capacitor

9.2.1.1 Analog Interface Noise

The first amplifier in the signal path is typically the most important block to set the desired SNR: capacitive coupling to the sensor and the noise of the amplifier itself must be taken into account. It is now assumed that the full ASIC noise budget is accounted for the input stage, a fully differential transresistance amplifier reported in Fig. 9.3. This circuit is negative looped and so the two input pins of the operational amplifier can be considered virtual grounds whose value is fixed by a common mode feedback network (required in all fully differential schemes). Differential output voltage, $V_{\text{out}} = V_{\text{out}+} - V_{\text{out}-}$ using Laplace domain is:

$$\begin{aligned} V_{\text{out}+} - V_{\text{out}-} &= V_{\text{BIAS}} \cdot \left[\frac{1}{\frac{1}{s\left(C_0 - \frac{\Delta C(t)}{2}\right)}} - \frac{1}{\frac{1}{s\left(C_0 + \frac{\Delta C(t)}{2}\right)}} \right] \cdot \frac{R_F}{1 + sR_F \cdot C_F} \\ &= \frac{R_F}{1 + sR_F \cdot C_F} \cdot V_{\text{BIAS}} \left[sC_0 - s\frac{\Delta C(t)}{2} - sC_0 - s\frac{\Delta C(t)}{2} \right], \end{aligned} \tag{9.5}$$

and with some reductions output voltage vs. input differential capacitance variation transfer function is obtained:

$$\frac{V_{\text{out}}(t)}{\Delta C(t)} = -V_{\text{BIAS}} \cdot \frac{sR_F}{1 + sR_F \cdot C_F}. \tag{9.6}$$

Ideally, output voltage does not depend on input parasitic capacitances and on MEMS rest value. This transfer function is useful to convert output noise into an equivalent input noise in terms of minimum differential capacitance variation which can be detected. The main noise sources in a fully differential continuous-time

transresistance amplifier are given by feedback resistors and MOSFETs of input differential pair and related active load. These two contributions are now detailed.

Feedback Resistor Noise

Output voltage noise due to feedback resistors of differential transresistance amplifier is:

$$S_{\text{out},R_F,n} = 2 \cdot \frac{4k_B \cdot T}{R_F} \cdot \frac{R_F^2}{(1 + sR_F \cdot C_F)^2} \left[\frac{\text{V}^2}{\text{Hz}} \right], \tag{9.7}$$

where the factor 2 takes into account two independent noise sources from feedback resistors. Equation (9.7) can be converted into a corresponding $\Delta C_{R_F,n}$ using the input vs. output transfer function (Eq. (9.6)):

$$S_{C_R,n} = \frac{S_{\text{out},R_F,n}}{|T(j\omega)|^2} = \frac{8 \cdot k_B T}{R_F} \cdot \frac{1}{\omega_r^2 \cdot V_{\text{BIAS}}^2} \left[\frac{\text{F}^2}{\text{Hz}} \right], \tag{9.8}$$

Under the hypothesis that noise due input pair transistors of the operational amplifier is negligible with respect to noise of feedback resistors (this hypothesis is verified in Sect. 9.2.1.1), at the nominal frequency of 28.3 kHz the following values of R_F are estimated to meet noise analog interface noise specifications:

- $R_F \approx 4.6$ MΩ considering a $V_{\text{BIAS}} = 3$ V;
- $R_F \approx 18.6$ MΩ considering a $V_{\text{BIAS}} = 1.5$ V;

Here comes one of the main drawbacks of choosing a transresistance amplifier in an integrated CMOS technology: the implementation of high value resistors requires large active areas and possible solutions for this implementation can be done with:

- Integrated resistors;
- MOSFET working in ohmic region or subthreshold/off condition;
- Resistors implemented using switching capacitors.

A solution based on integrated resistors, compared to the implementation of a high ohmic resistance with MOSFETs in subthreshold/off region reg has main advantages in terms of better linearity, signal full scale, and noise with the drawback of occupied active area. Considering a standard CMOS technology with the possibility to implement polysilicon resistors with a sheet resistance in the range of 300 Ω/sheet, a rough estimation of the required area for a resistor value of about 5 MΩ is:

$$\left(\frac{L}{W} \right)_{\text{Poly-Si}} = \frac{2 \cdot R_F}{R_{\text{sheet}}} = \frac{2 \cdot 5 \cdot 10^6}{300} = 3.3 \cdot 10^5 \tag{9.9}$$

and so with a width dimension of 1 μm, the area occupied by feedback resistors is estimated to be approximately $A_{\text{Poly-Si}} = 190\ \mu\text{m} \times 190\ \mu\text{m}$. Width dimension must be chosen larger than minimum allowed dimension in order to have a good matching.

Input Stage Noise

In a typical (fully differential) operational amplifier main sources of noise are transistors of input pair and of its active load. These sources must now be compared to feedback resistor noise and, possibly, make them negligible. Voltage noise due to transistors is:

$$S_{V,\text{MOSFETs}} = \frac{2 \cdot 4\gamma \cdot k_\text{B} T}{g_m} \quad \left[\text{V}^2/\sqrt{\text{Hz}} \right] . \tag{9.10}$$

This voltage noise spectral density can be transferred to the output of the TIA and then converted into an equivalent resolution in terms of capacitance variation as done for R_F noise:

$$\begin{aligned} S_{C,\text{MOS}_n} &= \frac{2 \cdot 4k_\text{B} T \cdot \gamma}{g_m} \cdot \frac{1 + \omega^2 \cdot R_F^2 \cdot (C_F + C_\text{in})^2}{\omega_r^2 \cdot R_F^2 \cdot V_\text{BIAS}^2} \\ &= \frac{2 \cdot 4k_\text{B} T \cdot \gamma}{\sqrt{2 \cdot \mu C_\text{ox} \cdot \frac{W}{L} \cdot I_D}} \cdot \frac{1 + \omega^2 \cdot R_F^2 \cdot (C_F + C_\text{in})^2}{\omega_r^2 \cdot R_F^2 \cdot V_\text{BIAS}^2} . \end{aligned} \tag{9.11}$$

Considering a very conservative case due to the following strict working conditions:

- Width $W = 1.5\ \mu\text{m}$;
- Length $L = 0.9\ \mu\text{m}$;
- $\mu C_\text{ox} = 42\ \mu\text{A/V}^2$;
- $\gamma = 2$;
- Drain current $I_D = 0.5\ \mu\text{A}$;
- Resonance frequency $f_r = 28.3\ \text{kHz}$;
- Feedback resistance $R_F = 5\ \text{M}\Omega$;
- Feedback capacitance $C_F = 90\ \text{fF}$;
- Input parasitic capacitance $C_\text{in} = 2\ \text{pF}$;
- Stators biasing voltage $V_\text{BIAS} = 3\ \text{V}$;

an equivalent noise of about $76\ \text{zF}/\sqrt{\text{Hz}}$ is estimated which is, as previously supposed, negligible with respect to resistors noise. Noise due to the two transistor forming the active load of the input pair can be made negligible with an optimization of overdrive voltages and dimensions.

9.2.2 *Fully Differential Operational Amplifier*

Figure 9.4 shows the transistor level of a typical fully differential operational transconductance amplifier (OTA). The core transistors of the used technology are powered at 1.8 V which does not provide high enough swing to design a telescopic cascoded amplifier (this latter would have the main advantage of a lower power consumption). For this reason and to obtain a high open-loop gain a folded cascode amplifier is implemented.

In this configuration the open-loop gain of the amplifier is:

$$A_0 = \frac{V_{\text{out},a} - V_{\text{out},b}}{V_{\text{in},a} - V_{\text{in},b}} = g_{m_1} \cdot R_{\text{out}} \,, \tag{9.12}$$

and its bandwidth is:

$$f_p = \frac{1}{2\pi \cdot R_{\text{out}} \cdot C_{\text{out}}} \,, \tag{9.13}$$

being:

$$R_{\text{out}} = [g_{m_7} \cdot r_{0_7} \cdot (r_{0_3} \parallel r_{0_1})] \parallel [g_{m_9} \cdot r_{0_9} \cdot r_{0_11}] \tag{9.14}$$

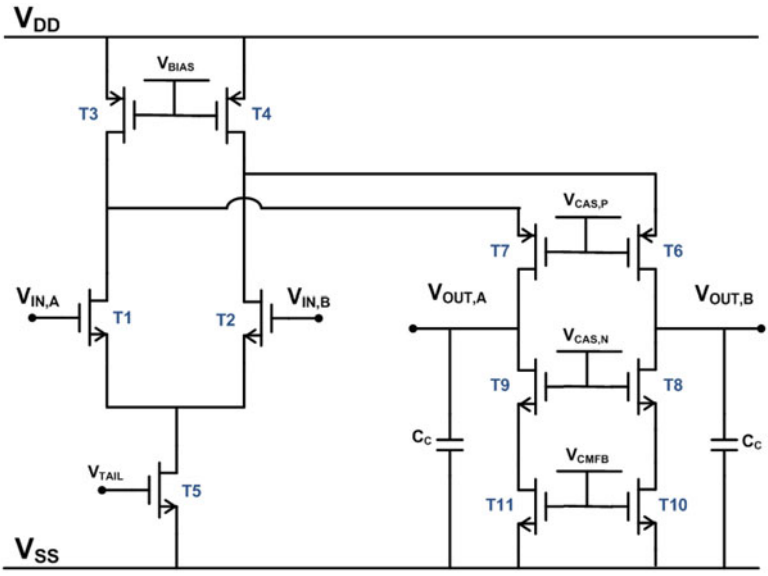

Fig. 9.4 Transistor level schematic of the fully differential operational amplifier

Below, some of the adopted design considerations to maximize the loop gain (90 dB) and minimize noise are summarized:

- a general constraint used in the design was to keep 15–20 mV of overdrive for all the transistors, to guarantee operation at least in the weak inversion region [2];
- the length of N-type input transistors pair T1 and T2 is chosen to avoid short channel effect ($\geq$2 μm). The N-type choice is due to their higher transconductance with respect to the P-type, while holding similar $1/f$ noise performances. Moreover, being the input signal modulated at >20 kHz
- the tail current is chosen to minimize the input-referred noise and to increase the overdrive voltage of transistors T3 and T4, so that their noise is almost negligible compared to the input pair. The same is done for the noise of T10 and T11, which are the cascode current generators. Input transistor areas are further increased to reduce the flicker noise;
- the biasing voltages of the cascode transistors (VCAS,N and VCAS,P in Fig. 9.4) are chosen to symmetrically increase the output dynamic range. The current in the cascode stage and the transistors sizes are set to achieve the desired gain as described above;
- finally, an estimation of a compensation capacitance at the outputs is done to guarantee a minimum phase margin of 60° in case of a buffer feedback. This compensation capacitance value will be revised considering common mode stability too.

Figure 9.5 shows the amplitude and phase of the open-loop gain with a compensation capacitance of 400 fF. The amplifier achieves a low, frequency open-loop gain of 90 dB, a GBWP of 4.4 MHz, a phase margin of 62°, and a current consumption of 4.4 μA.

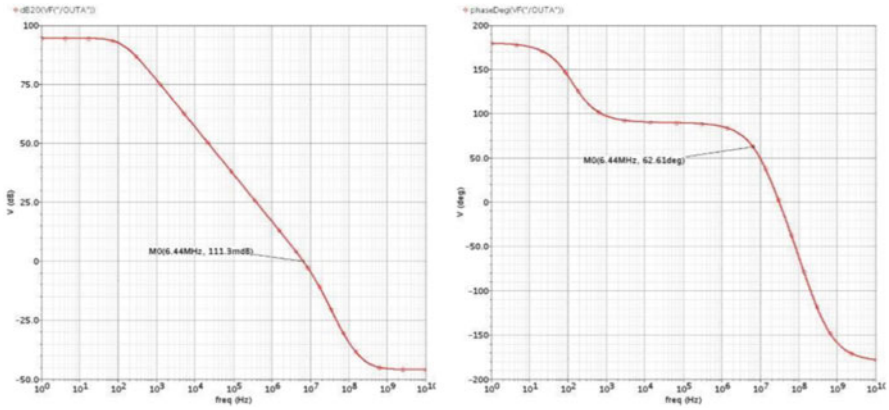

Fig. 9.5 Bode diagrams of fully differential folded cascode, with 400 fF compensation capacitance

9.2.2.1 Common Mode Feedback Network

As previously discussed, the magnetic field produces a differential signal between the input nodes; in order to reject all possible common mode contributions, that can lead to a shift in the polarization values—and can consequently change the behavior of the OTA—a common mode feedback network (CMFB) is needed.

Different solutions for the CMFB network can be implemented. The chosen solution monitors the output nodes, compares them with a reference voltage and acts on the folded cascode current generator to compensate the output DC level drift. The input nodes are DC stabilized by the feedback network. A schematic of this CMFB network is shown in Fig. 9.6.

If there is a positive common mode signal on the outputs of the amplifier, both T20 and T23 gatesource voltages are reduced, so that the currents in T27 and T26 are unbalanced, with $I_{T,27} < I_{T,26}$. The current of T26 is mirrored in the cascode current generators, reducing the current that flows on the outputs resistances. This leads in turn to a reduction of the amplifier outputs voltages, closing the negative feedback and correcting the common mode behavior of the OTA. In case of a differential signal, the sum of the currents that flows in T20 and T23 remains constant, and the same occurs in T26, so that the CMFB network circuit does not influence the differential behavior of the OTA. All the DC currents are chosen in order to have a 1:1 ratio in the folded cascode current mirror.

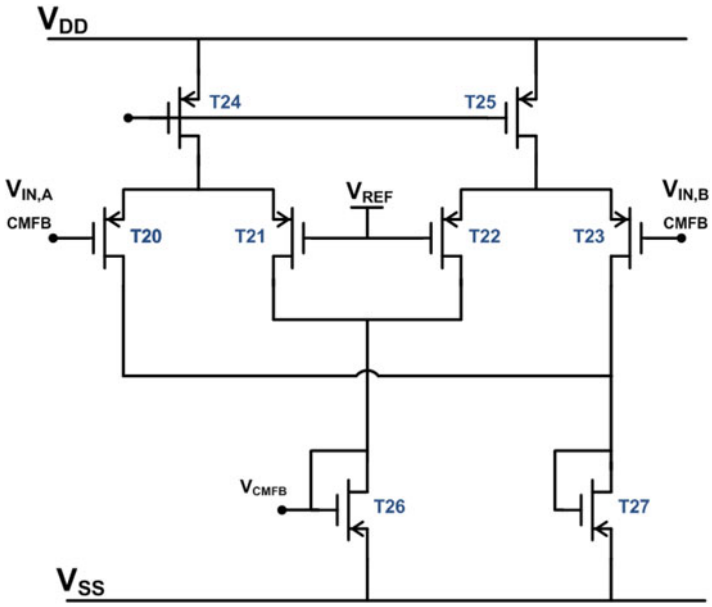

Fig. 9.6 Transistor level schematic of common mode feedback (CMFB) network. $V_{\text{in},a_{\text{CMFB}}}$ and $V_{\text{in},b_{\text{CMFB}}}$ correspond, respectively, to the outputs $V_{\text{out},a}$ and $V_{\text{out},b}$ of the differential amplifier of Fig. 9.4

The CMFB compensation capacitance is connected at the outputs of the fully differential amplifier, since this is the node with the highest impedance. It is possible to separate the compensation of the amplifier and of the CMFB network by connecting multiple capacitances either differentially between the two outputs or between the outputs and V_{SS}. The compensation capacitances are chosen to guarantee the stability of both differential and common mode amplifiers even in case of unity gain connection. An overall current consumption of less than 1 μA is estimated for this CMFB solution.

9.3 Verilog—A Model for Cadence® Environment

Models to simulate magnetometers (and more generally MEMS) taking into account physics, geometry, and technological constraints are implemented in a first phase of this project using Simulink® tool and they turned out to be very helpful in system design. It is however not straightforward to include in Simulink simulations secondary effects such as the presence of noise, parasitic capacitances, electronics nonidealities, etc.

In order to better analyze the overall performance and power dissipation from a fully coupled-system point of view and to prepare a custom tool for ASIC design, alternative solutions for sensor modelling are analyzed with an eye on languages compatible with integrated circuits simulators. Electromechanical coupled simulations are getting of deeper interest right for the design of ASIC for MEMS: sensor modelling inside one single simulation environment (Cadence®) allows to optimize electronic frontend considering mechanical nonidealities and sensor vs. electronics interference. As an ASIC must be designed inevitably using the software for which technology design-kit is available, a detailed magnetometer model has been integrated directly in the VLSI simulation environment. Verilog-AMS is a derivative of Verilog hardware description language which includes analog and mixed signal extensions to describe behavior of devices. For this specific case, Verilog-A, a continuous-time subset of Verilog-AMS, is used. A Verilog project consists of a hierarchy of modules, each one with a set of inputs, outputs, and bidirectional ports called “disciplines” (real, electrical, kinematic, thermal, magnetic, etc.). Each module can be associated to a schematic symbol the parameters of which can be changed in the object properties windows. A typical Verilog-A listing consists of:

- Inclusion of files required for code compilation;
- Additional “nature” declaration or change of default settings;
- Definition of modules inputs, outputs, and parameters;
- *analog begin/end* block where are reported sequential instructions which describe the model.

Two main blocks are developed to describe MEMS magnetometer behavior and their corresponding two symbols are placed in a schematic as if they were embedded libraries circuit parts, as shown in Fig. 9.7:

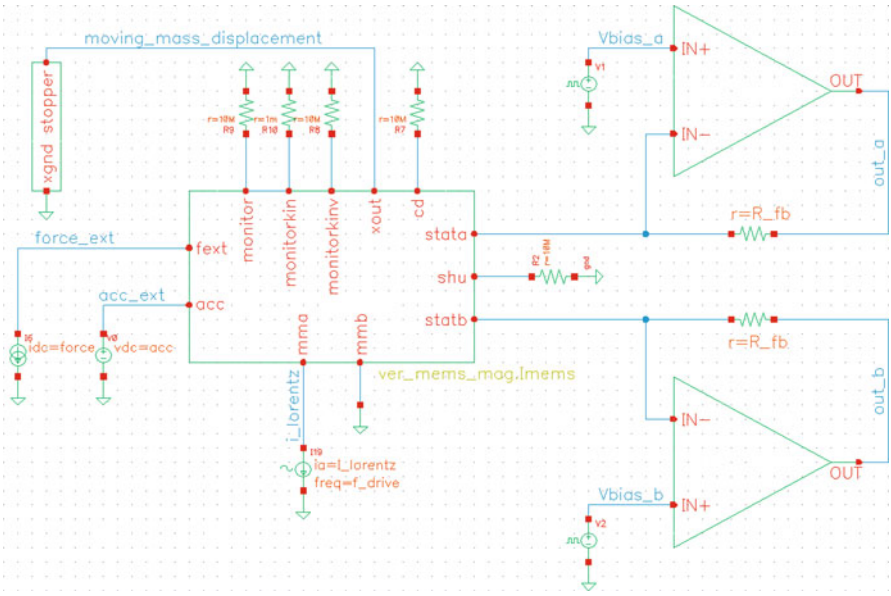

Fig. 9.7 Cadence® schematic where symbols (one for the sensors itself and one to simulate the mechanical stopper) associated to MEMS magnetometer are placed together with other electrical components

– *MEMSMAIN* which includes mechanical and electrical behavior of magnetometer, based on the balance of forces acting on the moving mass;
– *STOPPER* which is a behavioral implementation to simulate mechanical stoppers which are implemented to avoid moving mass collapsing to stators in case of pull-in or high acceleration shocks.

9.3.1 MEMS MAIN Module

The first implemented block is *MEMS MAIN*. Bidirectional ports which define this module are:

– *mma* and *mmb* are springs ends to which moving shuttle is anchored. They represent both inputs and outputs because Lorentz current is pumped into them but it is also interesting to monitor the resulting voltage because of their resistance. They are *electrical* discipline and so they are associated to Voltage "V" and Current "I";
– *stata*, *statb* are the two stators and *shu* is the rotor even though it does not actually have a direct connection with the package. This port is implemented to monitor the voltage of central point of flexures and so analyze effects due to springs mismatches. The two ports associated to readout electrodes are bidirectional as current due to motion must be sensed and a voltage must be forced. Also they are electrical.

- *fext* is an additional port to apply an external force different from Lorentz force. It is a *kinematic* discipline whose access functions are *Pos* (position) and *F* (force);
- *acc* is an input which allows to apply an external acceleration of value $g = 9.8\ \mathrm{m/s^2}$. It is a *customkinematic* discipline which is not native in the language but it is implemented for the purpose of this model. Associated access function is*Accel*;
- *xout* represents moving mass displacement with respect to rest position. It is a *kinematic* output;
- *cd* is differential capacitance variation. It is a non-native *Electronics* discipline. The associated nature is *Cap*;
- *monitor*, *monitorkin*, and *monitorkinv* are auxiliary output for variables monitoring during design phase. They are, respectively, associated to: *electrical*, *kinematic*, and *kinematicv*(speed).

Parameters of this block which can be modified using the graphic interface of Cadence® environment (i.e., opening the object properties editor directly from the schematic) are:

- C_0, sensor rest capacitance;
- *gap*, gap between rotor and stators at rest;
- *damp*, damping coefficient;
- *mass*, effective mass of the device;
- *km*, elastic stiffness;
- *Lspring*, spring length;
- *B*, external magnetic field;
- *R*1*L*, *R*2*L*, *R*1*R*, and *R*2*R* resistances associated to each of four suspending elements.

Each of these parameters has a default value which can be modified according to the specific device and simulation; a range of allowed values is set (Fig. 9.8).

After this preliminary phase to define variables and parameters of the model, MEMS behavioral description is implemented. After calculating electrostatic forces both due to driving signal and stators biasing, balance of forces is solved and the resulting value of *xout* is used for capacitance variation calculation and current flowing through stators.

9.3.2 STOPPER Module

Stopper module is defined as a block with two bidirectional ports *xgnd* and *stopper* of *kinematics* type. This block monitors the displacement of the moving mass and in case of an external force generating pull-in, stopper block activates and limits the displacement to the value *diststop* which can be set in object properties and it is set, as default, to the same distance as implemented devices.

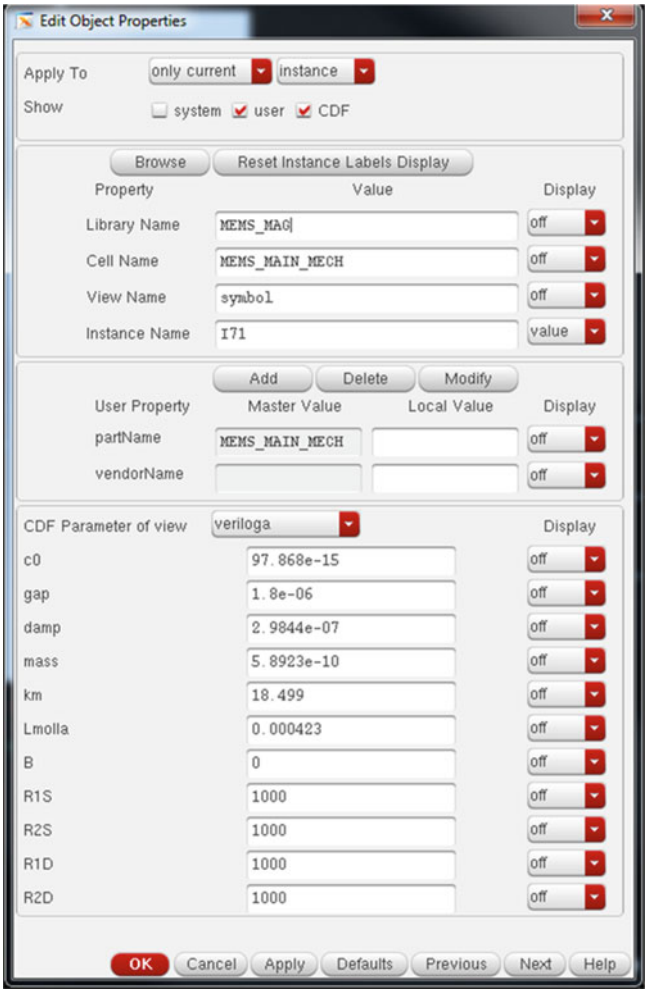

Fig. 9.8 The MEMS device can be added in the Cadence®—Virtuoso simulation tool as a basic building block of the circuit and its mechanical parameters can be set in object properties window

An *if/else* structure is used to distinguish when the moving mass is moving, in one direction or the other, beyond the maximum allowed displacement and, if that is the case, its movement is stopped. In order to check that behavioral implementation of the stopper is correct a sinusoid force is applied to the device to generate displacements larger than *diststop*. Figure 9.9 shows *xout* with respect to simulation time and it can be seen that when the moving mass reaches *diststop* $= 1.6$ µm, the displacement is stopped and limited as long as the force gets lower and the balance of forces gives a displacement lower than *diststop*.

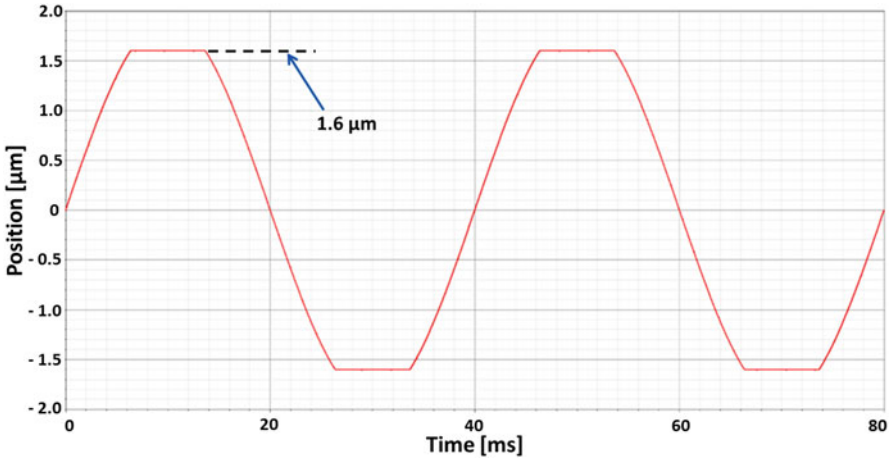

Fig. 9.9 Moving mass position with respect to time: when the maximum allowed displacement value is reached stopper module blocks the moving mass

9.3.3 Simulations and Model Verification

In order to verify a good implementation for the described Verilog-A model, a set of simulations are performed and more significant results are here reported. Simulations are based on magnetometer $N = 4$. As a first check, MEMS transfer function is simulated and reported in Fig. 9.10 with a correct value of resonance frequency, low-frequency value, and quality factor.

Further tests are executed in time domain comparing results with ones obtained by the same kind of simulation performed using Simulink®. For the sake of verification it is useful to compare Verilog-A model with the previously presented Simulink® model. Figure 9.11 reports two simulations, one performed using Simulink model and one with Verilog-A model in Cadence® environment, with an input acceleration. Indeed, this model is useful not only to simulate the device in presence of a magnetic field (purpose of this kind of sensor) but also in presence of other unwanted external forces, like accelerations.

9.4 Magnetic Field Measures: MEMS + ASIC

Magnetic field experimental measurements are performed with the implemented circuits and first generation of devices. MEMS is glued on a ceramic carrier and the ASIC is on top of the MEMS with stators wire-bonded to ASIC inputs and moving mass electrodes wire-bonded to carrier for external current excitation.

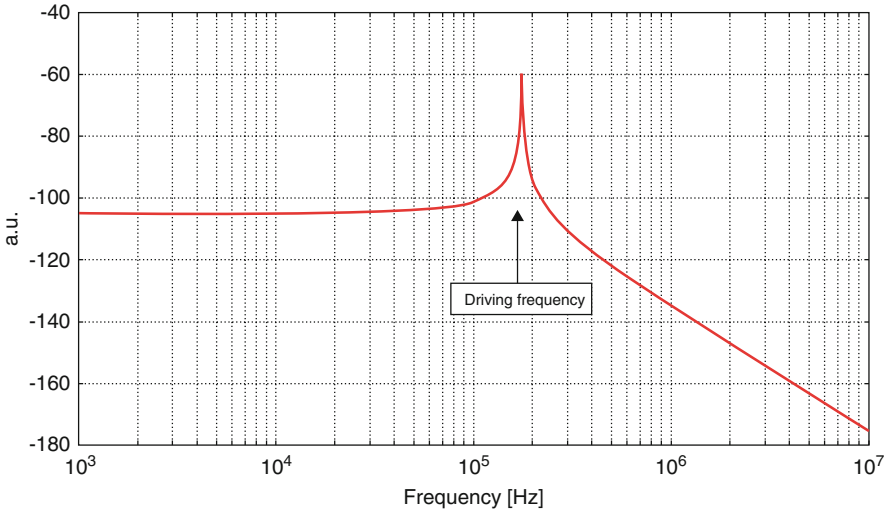

Fig. 9.10 Cadence® simulation using the Verilog-A magnetometer model, coupled to a CMOS frontend. The transfer function, solved by *Spectre* circuit simulator, is here simulated as the modulus of the differential capacitance variation vs. frequency

Figure 9.12 shows the transfer function of the fully differential transresistance amplifier for four different samples: resonance peaks are right below 30 kHz in agreement with measures previously done on devices and discrete electronics. Moreover, the circuit closed-loop bandwidth is at about 200 kHz in line with the pole set by feedback network.

Sensitivity measurements are performed applying three different values of magnetic field and measuring the resulting output signal of transresistance amplifier. Figure 9.13 shows, for three samples with 5 MΩ feedback resistance, that the peak is proportional to magnetic field intensity and measures have a good repeatability. As a comparison, one sample with 20 MΩ feedback resistor is reported and its output signal is four times higher than the others, on a fixed value of magnetic field. Measured sensitivity with 5 MΩ feedback resistors is 100 $\mathrm{nV}/\mu\mathrm{T}$ in agreement with theoretical predictions and system simulations. ASIC resolution is set by feedback resistors noise and for a biasing voltage of 5 V corresponds to 200 $\mathrm{nT}\cdot\mathrm{mA}/\sqrt{\mathrm{Hz}}$.

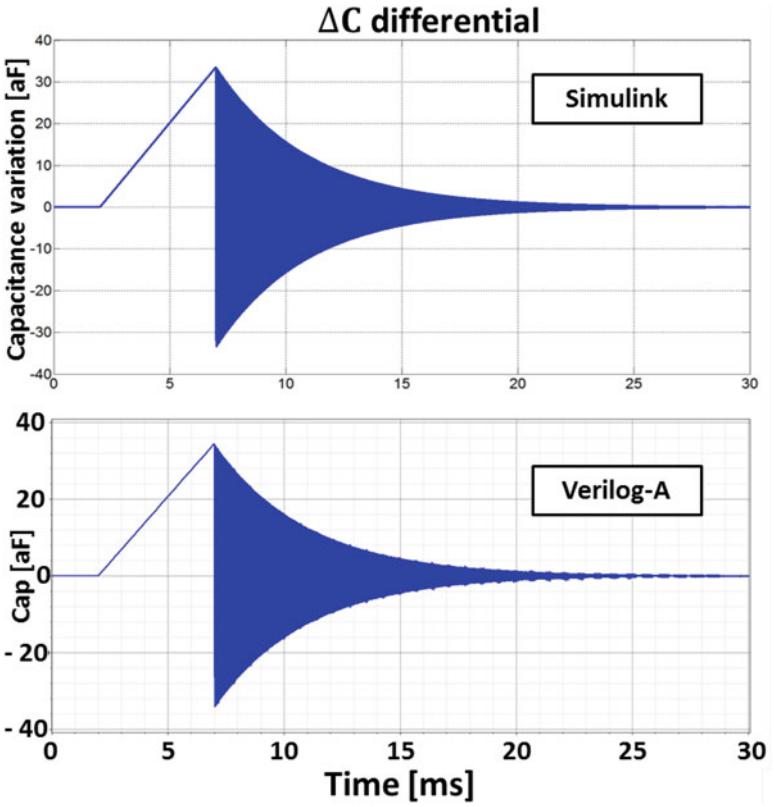

Fig. 9.11 Simulink and Verilog-A simulations of the effect of an external acceleration onto a magnetometer

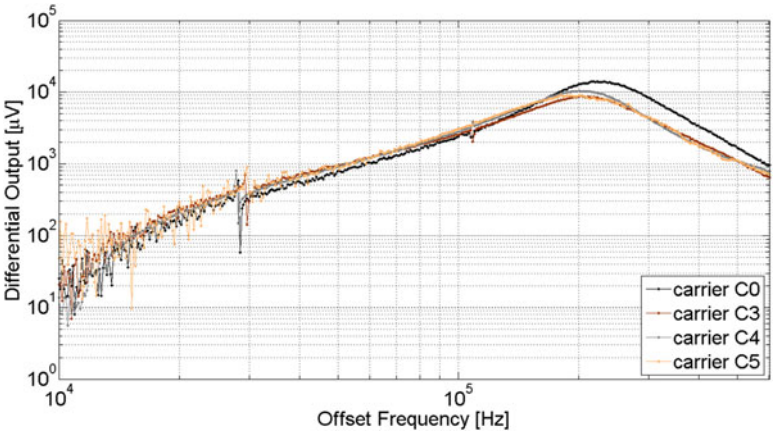

Fig. 9.12 Transresistance differential output voltage with respect to frequency for a fixed magnetic field. MEMS resonance peaks are close to 30 kHz and closed-loop bandwidth is at about 200 kHz in very good agreement with simulations

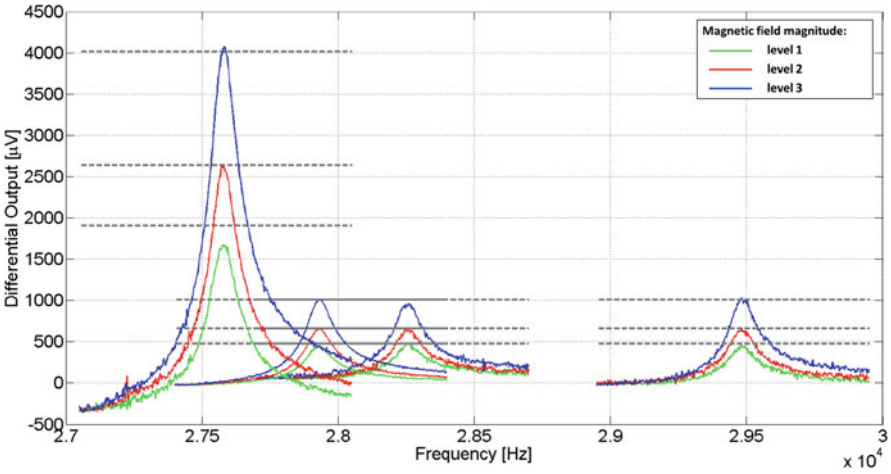

Fig. 9.13 Transresistance differential output voltage with respect to frequency. MEMS resonance peaks are close to 30 kHz and closed-loop bandwidth is at about 200 kHz in good agreement with simulations

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