A Novel Flux-Controlled Memristive Emulator for Analog Applications

Abdullah G. Alharbi, Mohammed E. Fouda and Masud H. Chowdhury

Abstract Emerging memristor technology is drawing widespread attention during the recent time due to its potential diverse applications in nanoelectronic memories, logic and neuromorphic computer architectures. Due to the absence of a practical memristive device, most of the research works in this area are still based on memristor emulator circuits that can be of current-controlled or voltage-controlled type. In this chapter, we introduce two emulator circuits for flux-controlled memductor and memristor. These emulator circuits have been built based on second generation current conveyer (CCII+), one multiplier and a square circuit to mimic the hysteresis behavior of the memristor. The proposed memristor emulator circuits can not only emulate memristive and plasticity function but also can be configured for floating configurations characteristic. Furthermore, we present the mathematical modeling, SPICE simulation and experimental results of the proposed emulator circuits. The series and parallel connectivity of these emulator circuits have been also studied, In addition to frequency analysis of their behavior.

Keywords Memrisitor · Non-linear Circuit · Memristor emulator · Hysteresis · Floating emulator · CCII+

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1 Introduction

Memristor is a two terminal non-linear passive element, which was first introduced theoretically by Leon Chua in 1971 (Chua 1971; Chua and Kang 1976). He showed that memistor is the only non-linear passive element, which can relate the missing link between flux and electrical charges. In the I-V plane, it shows a unique pinched hysteresis loop that shrinks at higher frequency. Later in 2008, the two terminal nanoscale memristor device has been successfully fabricated by HewlettPackard (HP) lab (Strukov et al. 2008). Since then, memristor has been getting widespread attention from the scientific community due to its revolutionary potential in memory and various other systems. The most important physical property of the memristive device is that it does not discharge even after the applied voltage is removed and remains in its pre-charged state. This property can be utilized for memory application. Memristor can be of two types: charge-dependent or current-controlled and flux-dependent or voltage-controlled. However, in order to call any device a memristor, some substantial fingerprints are required that distinguish it from other devices (Adhikari et al. 2013). These fingerprints are discussed in details in Sect. 2. Moreover, in the last decade, many research projects and publications mentioned the dynamic nature and the potential applications of memristor. Some of the applications include implementation of high-speed memory arrays like resistive random access memory (RRAM), analog and digital circuits, sinusoidal and relaxation oscillators, neuromorphic circuits, adaptive filters (Zidan et al. 2014; Ascoli et al. 2014; Radwan and Fouda 2015; Vourkas and Sirakoulis 2016) and Chaotic oscillator (Vaidyanathan and Volos 2016a, b).

Since there is no physical memristive device available in the experimental labs or commercial design houses, most of the research are still at the theoretical stage. To validate the applications of memristor, we need precise behavior and SPICE macro models. In fact, numerous micro models are being developed using the equations of memristor proposed by the HP lab (Shin et al. 2010; Biolek et al. 2009; Garcia-Redondo 2016; Batas and Fiedler 2011; Berdan et al. 2014; Abdalla and Pickett 2011). In addition, a comparison between some of these model can be found in Ascoli et al. 2013. However, these models have many limitations for which it cannot mimic the physically developed memristor. Most of these models are only applicable to computer aided simulation of ideal memristor. In the absence of any practical memristive device, research community focuses on developing emulator circuits to mimic the dynamic behavior of memristor to explore the design issues and potential applications. Therefore, many emulator circuits have been proposed and designed based on different design methodologies using off-the-shelf active and passive devices that are commercially available. Some of them are implemented using analog components like Op-amps, second generation current conveyer (CCII), transistors, analog multiplier, floating capacitor, JFET, zener diodes, BJTs, diodes, and Differential Difference Current Conveyors, microcontroller unit, analog to digital converter and digital to analog converter. For instance, the memristor emulator circuit introduced in Pershin and Ventra 2010 uses a microcontroller unit and analog-to-digital, digital to ana-

log converters. This emulator is topologically complex which limits their application in connecting with active and passive devices. In addition, a memristor emulator circuit based on Operational Transconductance Amplifier has been proposed in Kumngern and Moungnoul 2015. However, the experimental results of this emulator circuit do not satisfy the condition of memristor. A memristor emulator circuit based on an exponential amplifier and a CCII is presented in Alharbi et al. 2015b. The memristor emulator presented in Sánchez-López et al. 2014 uses five second generation current conveyors (CCII+), analog multiplier, five resistors and one capacitor. In addition, the emulator circuit proposed in Yeşil et al. 2014 requires four resistors, one Differential Difference Current Conveyors (DDCC) blocks, one grounded capacitor and one analog multiplier. Another memristor emulator introduced in Biolek et al. 2011 uses two current-feedback operational amplifiers (CFOAs) and one voltage-feedback operational amplifier, a large number of passive elements and a light-dependent resistor (LDR). Moreover, the emulator circuit presented in Abuelmaatti and Khalifa 2014 uses two current-feedback operational amplifiers (CFOAs), one diode, four resistors, two grounded capacitors. Voltage and current controlled mermsitor emulator is presented in Elwakil et al. 2013. Also, a CMOS based memristor emulator has been introduced in Hussein and Fouda 2013; Yener and Kuntman 2014. In addition, the memristor emulator uses two second generation current conveyer (CCIIs), two diode connected transistors and one resistor is provided in Alharbi et al. 2015d. This emulator has been improved in Alharbi et al. 2015c. A floating memristor emulator based relaxation oscillator is presented in Yu et al. 2014. Another floating emulator circuit is introduced in Shin et al. 2013. The emulator circuit uses an operational transconductance amplifiers (OTAs) and second generation current conveyors (CCIIs) is introduced in Sözen and Çam 2016. Simple floating and grounded voltage-controlled emuator are presented (Fouda and Radwan 2014; Alharbi et al. 2016). Furthermore, in Kim et al. 2012 an emulator for the memristor has been proposed, which is comprised of an adder, ten transistors, five OP-AMPs and eight resistors. Also, Electromechanical Emulator of Memristive Systems is introduced in Asapu and Pershin 2015. In addition, a cubic flux-controlled memristor is introduced in Liu et al. 2015 based on the cubic nonlinearity in Zhong 1994. However, most of these emulators have some drawbacks. Some are very complex and require rigid conditions. Some emulators do not exhibit or satisfy the three characteristic fingerprints of a memristor as discussed in Adhikari et al. 2013. The emulator circuit can be customized for different memristor models by selecting appropriate circuit elements is introduced in Alharbi et al. 2015a.

The rest of the chapter is organized as follows. In Sect. 2, a review of the fundamental properties of memristor is presented. In Sect. 3, we present our model and the emulator circuit development approach. The experimental results are shown in Sect. 4. Section 5 presents the frequency analysis of the flux-controlled memductor. In section Sect. 6, flux-controlled memristor circuit is introduced. Section 7 demonstrates the results and the analysis. Finally, Sect. 8 concludes the chapter with a highlight of future work.

2 Memristor Properties

For a device to be considered as a memristor it must have three significant fingerprints (Adhikari et al. 2013). Therefore, any memristor emulator circuit must also comply with these three fingerprints or defining characteristics. In this section, we have briefly summarized these fingerprints to establish the intellectual merits of the proposed emulator circuit.

- Memristor Fingerprint 1: Pinched Hysteresis Loop
  The first significant signature of the memristor is its unique pinched hysteresis loop which distinguishes it from any device that is not memristive in the (I-V plane).

(a) In I-V plane, the Lissajous figure of all memristors, having positive memristance and operated by sinusoidal signal of any amplitude and frequency, have to go through the origin.
(b) The value of $v(t)$ and $i(t)$ in the Lissajous figure should be same only when it will pass through origin, however, for rest of the times, V-I should have different values.

- Memristor Fingerprint 2: Hysteresis loop area decreases as frequency increases.
  The second vital signature of the memristor is the inversely proportional relationship between the frequency of periodic operating signal and memristors hysteresis lobe area. It states that with the increment of frequency, the lobe area will decrease.
- Memristor Fingerprint 3: No loop at infinite frequency.
  As we keep increasing the frequency, at some point, the lobe area will be reduced so much that there will no longer remain any loop, which means the memristors will behave as a linear device like resistor. At a very high frequency, memristor loses its unique non-linearity and the value of V and I remain same for all times in the I-V plane.

3 Proposed Flux-Contolled Memductor Emulator

The proposed emulator circuit for flux controlled memrductor has been designed with voltage difference circuit, voltage integrator and analog multiplier as shown in Fig. 1. In addition, the voltage difference circuit and the integrator are built based on the second generation current conveyer (CCII+).

3.1 Mathematical Analysis of the Proposed Emulator

The characteristics of an ideal CCII+ can be represented as in (1).

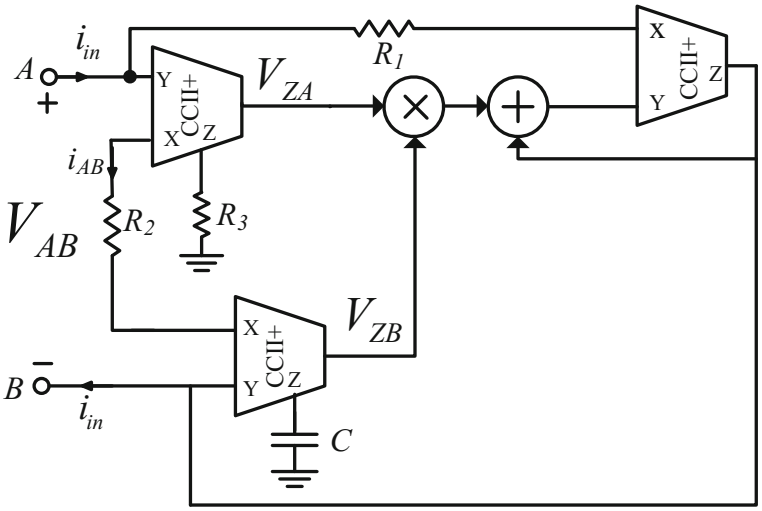

Fig. 1 The Proposed floating emulator circuit for flux controlled memductor

$$V_Y\ (t) = V_X\,(t) \text{ and } \quad i_X\,(t) = i_Z\,(t) \tag{1}$$

The input current to the circuit can be written as in (2)

$$i_{AB}(t) = \frac{v_A - v_B}{R_2} \tag{2}$$

Based on (1), the output voltage of first CCII+, V_{ZA}, is given by (3)

$$V_{ZA} = V_{AB}\frac{R_3}{R_2} \tag{3}$$

and the second CCII+ works as integrator where the current i_{AB} is integrated through the capacitor. Hence, V_{ZB} is given by (4)

$$V_{ZB} = \frac{-\alpha}{R_2 C}\int_0^t V_{AB}(\tau)d\tau + V_Z \tag{4}$$

The voltages V_{ZA} and V_{ZB} are multiplied, α is the multiplier constant, and summed to V_Z of the third CCII which represents V_B. Consequently, the voltage of Y terminal of third CCII is $V_Y = V_{ZA} + V_{ZB} + V_B$. The input current, I_{in}, is given by (5)

$$i_{in}(t) = \frac{V_A - (V_{ZA}V_{ZB} + V_B)}{R_1} \tag{5}$$

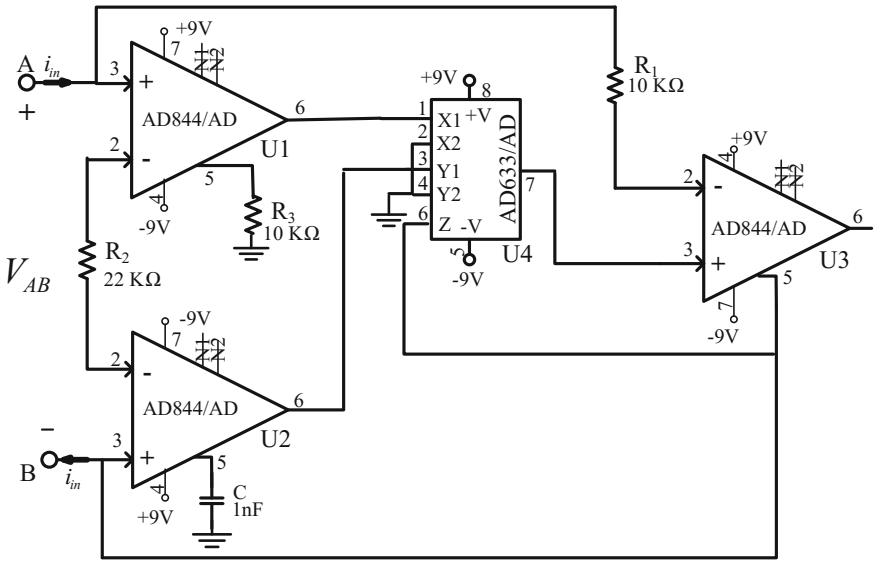

Fig. 2 Emulator circuit implementation of the flux controlled memductor model

By rearranging this equation, we obtain (6)

$$i_{in}(t) = \frac{V_{\mathrm{AB}} - V_{ZA} V_{ZB}}{R_1} \tag{6}$$

This current is mirrored to the input terminal V_B, so the input current to node A is the same as the output current of node B. Hence, this emulator represents a floating memristor emulator. So the current-voltage relation is given as in (7)

$$i_{in}(t) = V_{AB}\left(\frac{1}{R_1} + \frac{\alpha R_3}{R_2^2 R_1 C}\int_0^t V_{AB}(\tau)d\tau\right) \tag{7}$$

Thus, the input transconductance of the emulator, $G_m = i_{in}(t)/V(t)_{in} = i_{in}/V_{AB}$ representing memductance (memory transconductance) can be given by (8)

$$G_m = \frac{1}{R_1} + \frac{\alpha R_3}{R_2^2 R_1 C}\varphi(t) \tag{8}$$

It is clear that the memductance G_M is a function of the flux $\varphi(t)$. So, this model is referred as flux-controlled memductance

4 Circuit Realization and Experimental Validation

In order to ensure the validity and efficiency of the proposed memristor emulator circuit, the circuit shown in Fig. 1 has been realized and implemented in the lab from off-the-shelf components using AD844AN (constructed by the commercial AD844 current feedback operational amplifiers CFOA) as second-generation current conveyor (CCII+) and AD633 as a multiplier. Here, the used values of the passive elements are $R_1 = 10\,\text{k}\Omega, R_2 = 22\,\text{k}\Omega, R_3 = 10\,\text{k}\Omega$ and $C = 1nF$ as shown in Fig. 2. We used DC supply voltages $= \pm 9V$. In order to plot the I-V curves, the current was sensed using an instrumentation amplifier sensing the differential voltage across the resistance R_1. We have used the Digilent Electronics Explorer board (EE board) and from PC-based WaveFormsTM software the experimental data has been exported and redrawn using MATLAB without alteration, to draw the hysteresis loop.

Figure 3 shows nonlinearity and hysteresis loop in the I-V plane for the floating voltage controlled memristor emulator. it is clearly evident that the emulator circuit exhibits the unique the fingerprints of a real memristor. In addition, at low frequencies, the circuit shows nonlinearity in the (I-V) plane. However, at high frequency this nonlinearity gradually decreases. Moreover, our findings indicate that the proposed emulator circuit exhibits the fingerprints of a memristor as introduced in Adhikari et al. 2013. In addition, it is seen that the memristor emulator acts as a non-linear device and pinched hysteresis loop is found in the I-V plane for a particular range of frequency. However, it is clearly evident that as we keep increasing the frequency, the lobe area of the hysteresis loop tends to shrink. At a certain point, the loop becomes a straight line and the emulator acts like a linear resistor as shown in Fig. 3a. Moreover, Fig. 3b shows the behavior of the proposed emulator under triangular input for 5 kHz and 8 kHz in the I-V plane.

We have also analyzed the memductance of the proposed circuit of Fig. 1. It is observed from Fig. 4a that the memductance varies with time for applied sinusoidal

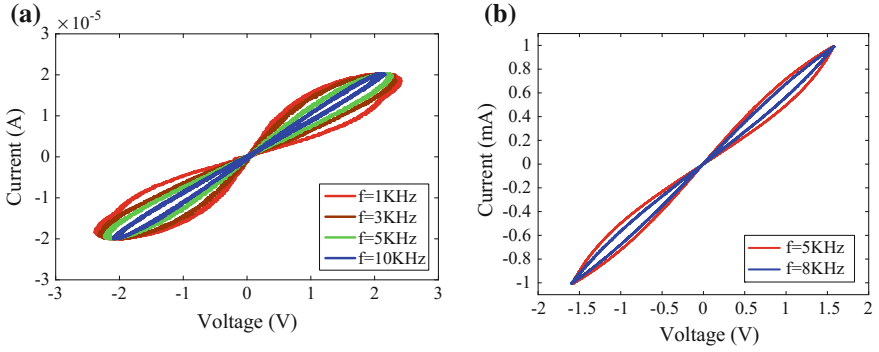

Fig. 3 Experimental results of the pinched hysteresis loop of the emulator circuit with various frequencies **a** sinusoidal input and **b** triangular input

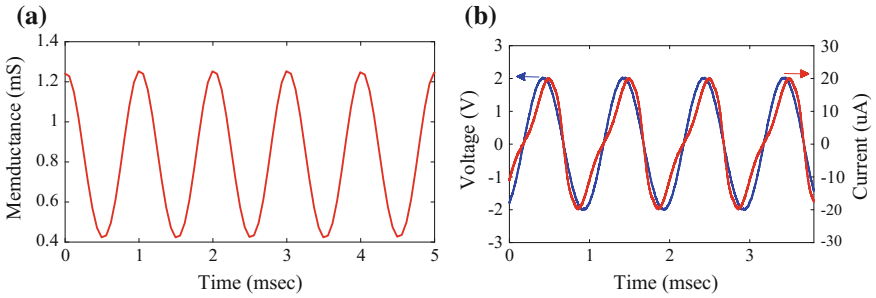

Fig. 4 SPICE transient simulation of proposed emulator signals at 1 kHz **a** Transient waveforms of memductance and **b** waveform of input voltage $v(t)$ (*blue*) and the input current $i(t)$ (*red*)

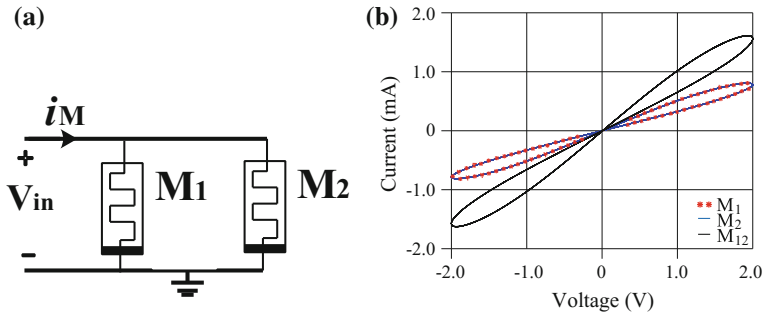

Fig. 5 Pinched hysteresis loops of two parallel connected emulators at 3 kHz

signal with amplitude 2 V and frequency 1 kHz. Furthermore, we can observe that the memductance changes from 0.42 mS to 1.23 mS.

As it is well known that the memristor is resistive so there is no phase shift between the current and the voltage, which is clear in the proposed emulator as shown in Fig. 4b. Clearly, the current is zero whenever the voltage is zero, which is the signature of a memristor. If a phase shift exists this means that there is a reactive element attached to the device. This implies that the proposed memristor emulator circuit is clearly resistive without any reactive element attached. In addition, in order to prove the proposed circuit functionality, two of the emulators are connected in parallel/series to make sure that the current/voltage is divided equally. Figure 5 shows the voltage and current relation (pinched hysteresis) in the I-V plane of the proposed emulator circuit in parallel connection. It is clearly evident that the current is divided equally between them. Whereas, Fig. 6 shows the series connection of two emulators where the input voltage is divided across the two memristors equally.

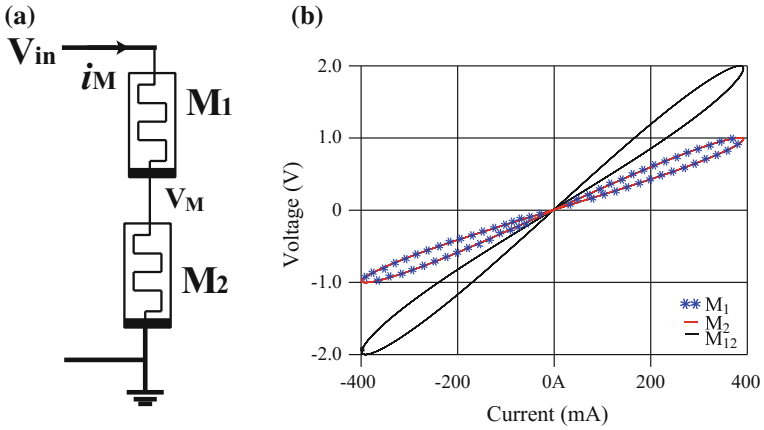

Fig. 6 Pinched hysteresis loops of two series connected emulators at 3 kHz

5 Frequency Analysis of the Flux-Controlled Memductor Emulator

In order to ensure the accuracy of the proposed emulator, we have studied the frequency analysis of the proposed emulator as in Sánchez-López et al. 2014. By applying a sinusoidal signal $V_{in} = Asin(\omega t)$, the memductance is given by (9)

$$G_m = \frac{1}{R_1}\left(1 + \frac{\alpha R_3 A(1 - cos(\omega t))}{R_2^2 C\omega}\right) \tag{9}$$

According to this equation, the minimum and maximum achievable memductances are given as follows (10)

$$G_{min} = 1/R_1 \; and \qquad G_{max} = \frac{1}{R_1}\left(1 + \frac{2\alpha R_3 A}{R_2^2 C\omega}\right) \tag{10}$$

As shown, the more the frequency, ω, increases, the more memristance decreases (Fingerprint 2). When ω tends to ∞, R_{max} tends to R_{min} which is a constant value meaning there is no hysteric behavior (Fingerprint 3). However, when ω tends to 0, R_{max}tends to ∞ which is not practical since the R_{max} saturates to certain value due to supply voltages which is corresponding to R_{on} and R_{off} in the fabricated devices.

It is obvious from (9) that the memductance equation is based on two terms, the first terms is constant resistance which is time invariant and the second one is time-varying resistor. The time varying term changes with function of the frequency and time constants of the integrator. The ratio between magnitude of both terms, β, can be defined as in (11):

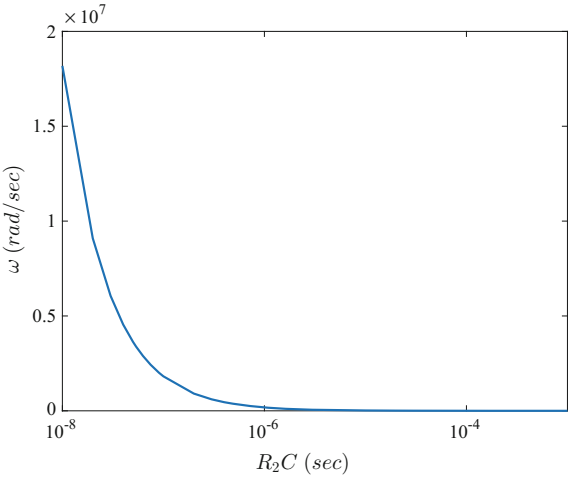

Fig. 7 Frequency behavior for $\beta = 0.5$ and $A = 1$

$$\beta = \frac{2\alpha R_3 A}{R_2^2 C\omega} = \beta_o \frac{T}{\tau} \tag{11}$$

where $\beta_o = \alpha R_3 A/\pi R_2$, $\tau = R_2 C$ and $T = 2\pi/\omega$.

It is clear with increasing the frequency, the ratio β decreases. By studying β, we can observe that β tends to zero if the frequency tends to ∞ where the memristor behavior is dominated by the linear term which is R_1. Also, hysteresis loop disappears when the time constant of the integrator τ is much greater than T.

Figure 7 shows the effect of changing the time constants τ with the frequency while maintaining the same ratio $\beta = 0.5$. The more τ decreases, the more operating frequency is needed for the same β_o.

6 Proposed Flux-Controlled Memristor Emulator Circuit

The proposed emulator circuit is the modification and improved version of the original emulator circuit in Abuelmaatti and Khalifa 2015. The emulator circuit shown in Fig. 8 consists of a practical integrator, differentiator and square function. The practical integrator and differentiator are built by using two second-generation current conveyors (CCII+s). Here, the square function is used to achieve the required non-linearity for memristive behavior.

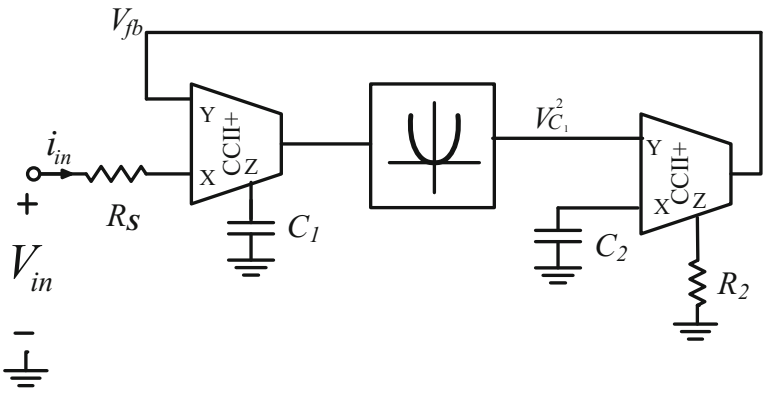

Fig. 8 Flux-controlled Memristor emulator circuit diagram with square function

6.1 Mathematical Analysis of the Proposed Emulator

The input current, i_{in}, is created by subtracting the feedback voltage, V_{fb} from the input voltage, V_{in} which can be written as in (12)

$$i_{in} = \frac{V_{in} - V_{fb}}{R_s} \tag{12}$$

Then, this current is imposed in the capacitor C_1, so the voltage across the capacitor is given by (13)

$$V_C = \frac{-1}{R_s C_1} \int_0^t (V_{in} - V_{fb}) d\tau \tag{13}$$

where V_{fb} represents the feedback voltage (output of second CCII+). This voltage is squared using squarer circuit, or multiplied by itself using multiplier as done in our circuit. Then, the output voltage of the multiplier is differentiated using the second CCII given the feedback voltage (14).

$$V_{fb} = \alpha R_2 C_2 \frac{dV_C^2}{dt} \tag{14}$$

where α is the multiplier gain. By substituting into (13), V_C is given as in (15)

$$V_C = \frac{-1}{R_S C_1} \int_0^t (V_{in} - \alpha R_2 C_2 \frac{dV_C^2}{dt}) d\tau = \frac{1}{R_S C_1} \left(\alpha R_2 C_2 V_C^2 - \varphi_{in} \right) \tag{15}$$

By rearranging the equation,

$$\alpha R_2 C_2 V_C^2 - R_S C_1 V_C - \varphi_{in} = 0 \tag{16}$$

It is second order equation of V_C, then the voltage V_C can be written as in (17)

$$V_C = \frac{R_S C_1 \pm \sqrt{R_S^2 C_1^2 + 4\alpha R_S C_2 \varphi_{in}}}{2\alpha R_2 C_2} \tag{17}$$

The feedback voltage is function of dV_C^2/dt where the derivative of V_C is given as in (18)

$$\frac{dV_C}{dt} = \pm \frac{V_{in}}{\sqrt{R_S^2 C_1^2 + 4\alpha R_2 C_2 \varphi_{in}}} \tag{18}$$

by applying the chain rule, the derivative of V_C^2 is given as follows (19):

$$\frac{dV_C^2}{dt} = 2V_C \frac{dV_C}{dt} = \pm 2V_C \frac{V_{in}}{\sqrt{R_S^2 C_1^2 + 4\alpha R_2 C_2 \varphi_{in}}}, \tag{19}$$

and the feedback voltage is given by (20)

$$V_{fb} = \alpha R_2 C_2 \frac{dV_C^2}{dt} = \left(1 \pm \frac{R_S C_1}{\sqrt{R_S^2 C_1^2 + 4\alpha R_2 C_2 \varphi_{in}}}\right) V_{in} \tag{20}$$

By subistuting into (12), and simplifying the expression, the input current can written as in (21)

$$i_{in} = \frac{C_1}{\sqrt{R_S^2 C_1^2 + 4\alpha R_2 C_2 \varphi_{in}}} V_{in} \tag{21}$$

and the input memristance is given by (22)

$$R_m = R_S \sqrt{1 + \frac{4\alpha R_2 C_2 \varphi_{in}}{R_S^2 C_1^2}} \tag{22}$$

As we can see that this equation is the same closed form solution of HP model. By comparing this equation and HP model solution, the initial memristance is R_s and the memristor speed term, k', is

$$k' = \frac{\alpha R_2 C_2}{C_1^2} \tag{23}$$

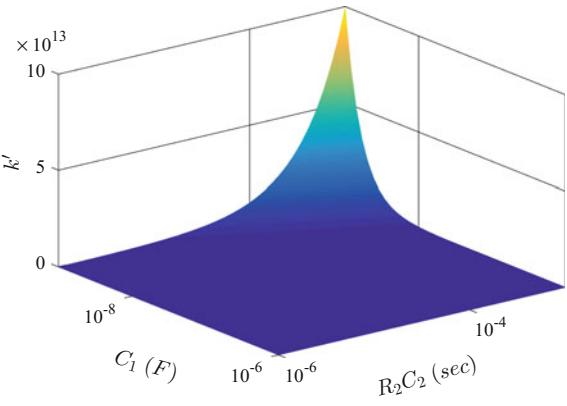

Fig. 9 Effect of changing circuit parameters on the memristor speed for $\alpha = 0.1$

As clear that the Memristor speed decreases quadratically with increasing C_1 and increases with the increasing the differentiator time constant R_2C_2. Figure 9 shows a 3D plot with changing the circuit components values.

6.2 *Implementation of the Emulator Circuit*

The proposed emulator circuit is simple and designed from the off-the-shelf components. This emulator circuit has been realized and implemented using AD844AN as second-generation current conveyors (CCII+), and the square function is implemented using a commercial AD633 (voltage multiplier) and some passive elements: $R_s = 1.5\,\text{k}\Omega, R_2 = 2\,\text{k}\Omega$, $C_1 = \mu F$ and $C_2 = 1\mu F$ as shown in Figs. 10a and 11. We

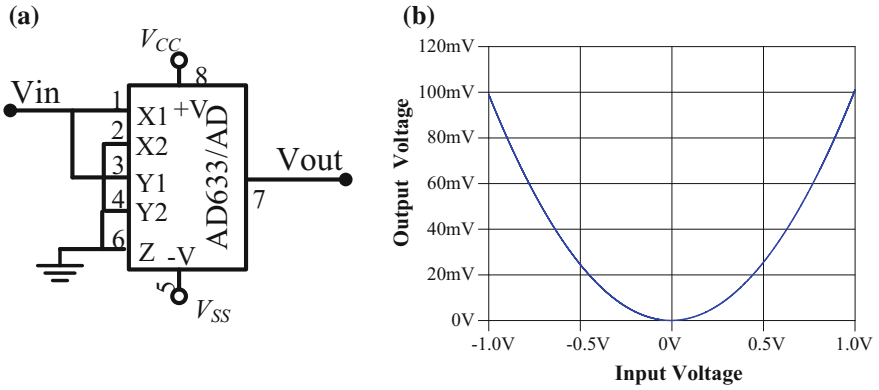

Fig. 10 Proposed implementation of the square function: **a** circuit diagram. **b** SPICE simulation of the Lissajous curve of the proposed square function

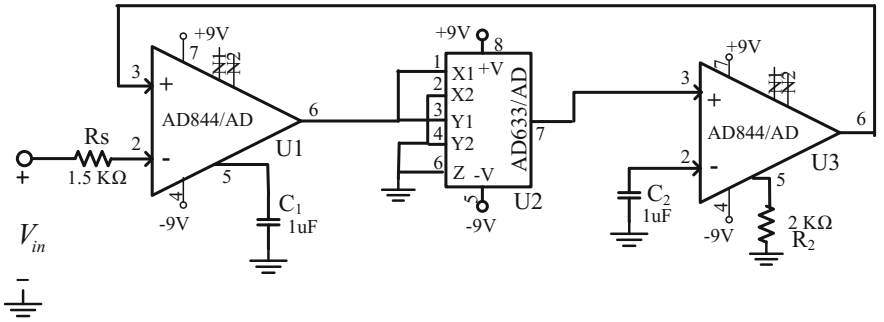

Fig. 11 The schematic diagram of flux controlled emulator circuit of memristor

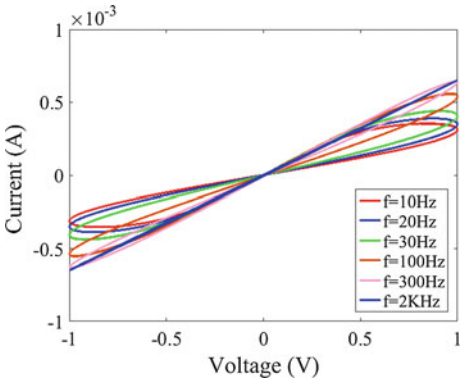

Fig. 12 Experimental results of the pinched hysteresis loop of the proposed memristor emulator circuit

have used $\pm 9V$ as supply voltages. In addition, we have used the Digilent Electronics Explorer Board and WaveFormsTM software to perform the experimentation. The data has been exported directly to MATLAB without alteration to draw the hysteresis loop. Figure 10b shows the Lissajous curves of the proposed square function obtained from SPICE simulation conducted on the implemented square function circuit.

Now, if we use the proposed square function circuit of Fig. 10a into the proposed emulator circuit model of Fig. 8, we achieve a emulator circuit implementation for flux controlled Memristor as shown in Fig. 11. Furthermore, the hysteresis loops obtained from the experimental data for the proposed emulator circuit of Fig. 11 are shown in Fig. 12. It is observed that the emulator has a pinched hysteresis loop in the I-V plane as expected. Moreover, at low frequencies the circuit shows nonlinear hysteresis in the (I-V) plane. However, with the increase of frequency of the input signal this nonlinearity gradually shrinks. Beyond 2 kHz, the emulator starts to behave like a linear resistor, which satisfies Chuas condition in Chua 2014.

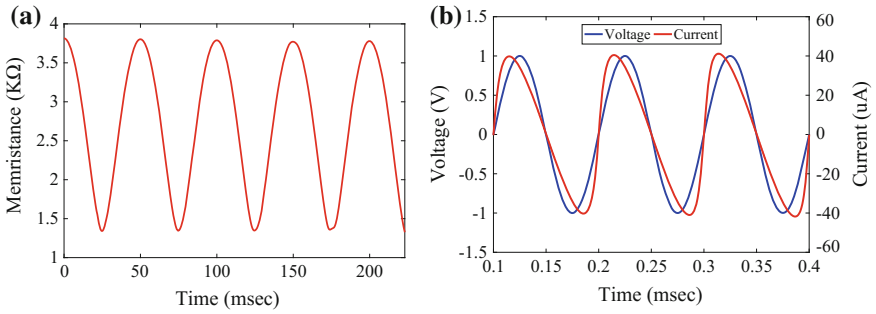

Fig. 13 **a** Transient memristance at 30 Hz **b** input voltage $v(t)$ (*blue*) and the input current $i(t)$ (*red*) for the proposed memristor at 30 Hz

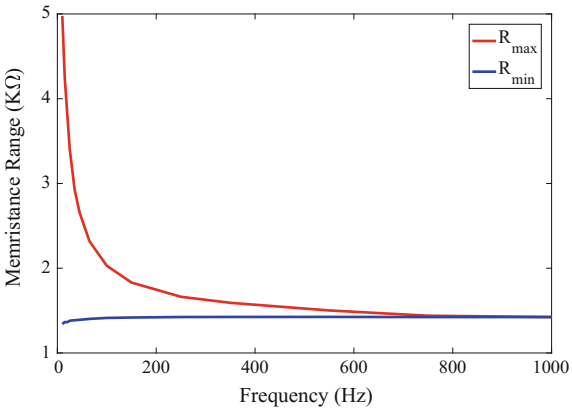

Fig. 14 Maximum and Minimum achievable memristance versus the frequency

It can be observed from Fig. 13a that the memristance changes with time as we apply the sinusoidal signal having 30 Hz of frequency and 1 V of amplitude. In addition, it is also significant to notice that the nature of changing the memristance is also sinusoidal. Furthermore, In addition, Fig. 13b demonstrates the waveform of the voltage and current of the proposed memristor emulator circuit. Moreover, there is no phase shift between the current and voltage. It is also seen that no current exists when the voltage is zero which validates a significant property of the memristor. Hence, we can conclude that our proposed emulator circuit is purely resistive element. Figure 14 shows the maximum and the minimum achievable memristance, which changes with the frequency. Here, Rmin is almost constant and it represents Rs. R_{max} decreases gradually with the applied frequency of the sinusoidal input signal and at one point it coincides with R_{min}. This indicates that beyond certain frequency the emulator circuit starts to behave like a linear resistor.

7 Frequency Analysis of the Voltage-Controlled Memristor Emulator

In order to ensure the accuracy of the proposed emulator, we have studied the frequency analysis of the proposed emulator. By applying a sinusoidal signal $V_{in} = Asin(\omega t)$, the memristance is given by (24)

$$R_m = R_S\sqrt{1 + \frac{4\alpha R_2 C_2 A(1 - \cos(\omega t))}{\omega R_S^2 C_1^2}} \tag{24}$$

According to this equation, the minimum and maximum acheivable memristance are given as follows (25)

$$R_{min} = R_S \; and \quad R_{max} = R_S\sqrt{1 + \frac{8\alpha R_2 C_2 A}{\omega R_S^2 C_1^2}} \tag{25}$$

As clear with increasing the frequency ω, the memristance decreases (Fingerprint 2). When ω tends to ∞, R_{max} tends to R_{min} which is a constant value meaning there is no hysteric behavior (Fingerprint 3). However, when ω tends to 0, R_{max} tends to ∞ which is not practical since the R_{max} saturates to certain value as shown in Fig. 14 due to supply voltages which is corresponding to R_{on} and R_{off} in the fabricated devices.

It is obvious from (24) that the memristance equation is based on two terms, the first terms is constant resistance and the second one is time-varying resistor. The time varying term changes with function of the frequency and time constants of the differentiator and integrator. The ratio between magnitude of both terms, β, can be defined as follows (26):

$$\beta = \frac{8\alpha R_2 C_2}{R_s^2 C_1^2}\frac{A}{\omega} = \beta_o \frac{\tau_2 T}{\tau_1^2} \tag{26}$$

where $\beta_o = 8\alpha A/2\pi$, $\tau 1 = R_s C_1$, $\tau_2 = R_2 C_2$, and $T = 2\pi/\omega$.

It is clear with increasing the frequency, the ratio β decreases. By studying β, we can observe that β tends to zero if the frequency tends to ∞ where the memristor behavior is dominated by the linear term which is *Rs*. Also, hysteresis loop disappears when the time constant of the integrator τ_1 is greater than $\sqrt{T}$. However, by increasing the differentiator time constant τ, the hysteresis becomes larger.

Figure 15 shows the effect of changing the time constants τ_1 and τ_2 with the frequency while maintaining the same ratio $\beta = 0.5$. The more τ_1 decreases, the more operating frequency is needed for the same τ_2 since they have quadratic relation. However, the more τ_2 decreases, a lower operating frequency is needed for the sam τ_1.

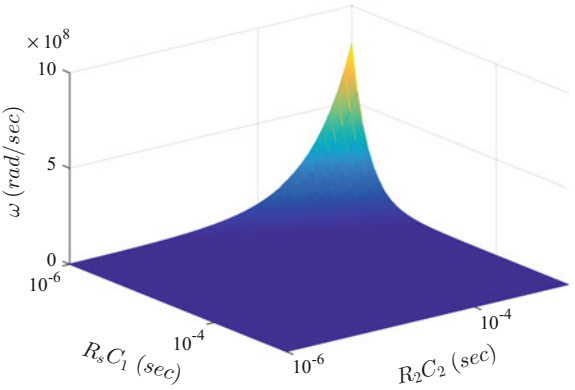

Fig. 15 Frequency behavior for $\beta = 0.5$ and $A = 1$

8 Conclusion and Future Work

We have presented a practical memristor emulator circuit development technique to mimic the nonlinear behavior of the memristor. We have demonstrated two different emulator circuits for the flux-controlled memristor. Our numerical analysis and simulation using SPICE and the experimental testing match very well, which indicate that the proposed circuits can accurately imitate the behavior of a memristor and satisfy all the three fingerprints of a memristor. The proposed circuit model of Fig. 1 is a floating memristor emulator, which is suitable for use in many digital and analog applications as a 2-terminal device. Moreover, in the absence of a real solid-state device for the memristor, these emulator circuits will be very useful to investigate the properties and potential applications of memristors. Hence, our emulator circuits have the potential to be used in many practical applications in the analog and digital world. The proposed circuits are practical and simple to design compared to many other emulator circuits proposed by different groups. Therefore, the proposed emulator circuit development technique would have significant impact on the development and educational aspects of this new direction of research.

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