Analysis of Dynamic Linear Memristor Device Models

Balwinder Raj and Sundarapandian Vaidyanathan

Abstract The aim of this book chapter is to provide a comprehensive review report on the Memristor device. Development of linear model for memristor and analysis of memristor are the prime focus as its current requirement for high speed and low power circuits design. Detailed discussion about memristor device physics, structure, operation, mathematical modeling and TCAD simulations have been carried out for better understand of memristor. Moore's law, the semiconductor industry's obsession with the shrinking of transistors with the commensurate steady doubling on chip about every two years, has been a source of about 50 year technical and economic revolution. Numerous innovations by a large number of scientists and engineers have helped significantly to sustain Moore's law since the beginning of the Integrated Circuit (IC) era. As the cost of computer power to the consumer reduces, the cost of production for producers to sustain Moore's law follows an opposite trend, i.e. Research, Development, Manufacturing, and Test costs are increasing continuously with each new generation of chips. This had led to the reason for existence of Moore's second law, also called Rock's law, which is that the capital cost of a semiconductor fabrication also increases exponentially over time. The formation of memristor is a great achievement in semiconductor industry considering Moore's second law because of its very easy and less steps of fabrication which is the reason for memristor being so cheap, while its nano scale size is new direction to attain Moore's first law. Therefore, the modelling and simulation of memristor is essential to analyze more advanced features of memristor without spending a lot of money on fabrication and testing.

Keywords Memristor · Memristive device · Logic design · Linear model · Modeling · Simulation

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1 Introduction

Today, most electronic devices in technology inventions and all other applications use semiconductor components. The study of semiconductor devices is known as a branch of solid-state physics, whereas the designing and construction of the circuits to solve practical problems is included in electronics engineering (Raj et al. 2009; Sharma et al. 2014; Chua 1971). Moore's law, the semiconductor industry's obsession with the shrinking of transistors with the commensurate steady doubling on chip about every two years, has been a source of about 50 year technical and economic revolution. Whether this scaling paradigm will last for 10 or 15 years more, it will finally come to an end. The emphasis in electronic design will have to shift to devices that are not just increasingly infinitesimal but increasingly capable. Numerous innovations by a large number of scientists and engineers have helped significantly to sustain Moore's law since the beginning of the Integrated Circuit (IC) era (Raj et al. 2013; Pattanaik et al. 2012; Raj 2014; Gergel-Hackett et al. 2009; Bhushan et al. 2013).

Innovations listed below are examples of breakthroughs that have played a critical role in the advancement of integrated circuit technology by more than seven orders of magnitude in less than five decades:

i. The invention of the Integrated Circuit itself is the foremost contribution and the reason for existence of Moore's law, credited equally to Jack Kilby at Texas Instruments and Robert Noyce at Fairchild Semiconductor (Noyce 1961; Prodromakis and Papavassiliou 2011).
ii. The invention of the Complementary Metal–Oxide–Semiconductor (CMOS) in 1963 enabled extremely dense and high performance ICs (Wanlass 1967; Johnson 2010).
iii. Invention of the Dynamic Random Access Memory (DRAM) technology in 1967 made fabrication of single-transistor memory cells possible (Dennard 1968; Raj et al. 2009; Larrieu and Han 2013).
iv. The invention of deep UV excimer laser photolithography decreased the smallest features in ICs from 500 nm in 1990 to 32 nm in 2012. The trend is expected to reach smallest feature below 10 nm in next decades (Jain et al. 1982; Biolek et al. 2009).

Some of the new directions in research that may allow Moore's law to continue are:

i. Using deep-ultraviolet excimer laser photolithography- IBM researchers claimed to develop a technique to print circuitry only 29.9 nm wide using 193 nm Argon Fluoride excimer laser lithography (La Fontaine 2010; Raj et al. 2008; Joglekar and Wolf 2009).
ii. In April 2008, researchers at HP Labs successfully created a working memristor, whose existence had previously only been theorized. The memristor's unique properties permit the creation of smaller and better-performing electronic devices (Strukov et al. 2008; Raj et al. 2011).

iii. In February 2010 a breakthrough in transistors with the design and fabrication of the world's first Junctionless Transistor was announced. The researchers claim that the Junctionless transistors can be produced at 10 nm scale using existing fabrication techniques (Raj et al. 2008; Vishvakarma et al. 2007; Mohsin 2010).
iv. In April 2011, development of Single-Electron Transistor (SET) was announced, which was 1.5 nm in diameter and made out of oxide based materials (Fuechsle et al. 2012; Raj et al. 2011; Volos et al. 2015).
v. In February 2013, the development of the first working transistor consisting of a single atom placed precisely in a silicon crystal (not just picked from a large sample of random transistors) announced (Larrieu and Han 2013).

2 Background Study: Memristor Review

The analysis of Memristor fabricated on polymer sheet by simple techniques is done by Gergel-Hackett et al. (2009). The fabricated memristor was with ratio of ON/OFF resistance (R_{on}/R_{off} = 10000:1), life = ~14 days, and was able to show good characteristics even with >4000 flexes and requires V < 10 V for stability with thermal effects. The device was providing following advantages-

i. Both soft switching and hard switching compatible
ii. Behavior is not ambient dependent
iii. Suitable for flexible memory component
iv. Portable physically flexible device

Varghese and Gandhi (2009) have proposed a design for a low area differential pair which substantially reduces cubic distortion, provide better Total Harmonic Distortion and hence wide linear range with the help of memristor using in place of nonlinear resistor to provide better nonlinearity. The advantage of exploiting the nonlinearity was evident due to the reason that the memristor is 10^6 times more nonlinear at nanoscale as compared to micro scale. The possibilities of logic design using memristors are discussed in literature (Raja and Mourad 2010). Memristor as state element is analysed, also basic logic operation on two memristor with both inverting and non-inverting configuration is observed. Logic implementation on multiple memristor (wired AND) and memristor crossbar logic design for implementation of NAND gate is shown (Raja and Mourad 2010).

Figure 1 shows an example of Crossbar Array, where all possible combinations for state of a switch is shown and also the case if no switch is present. One switch is realized here with one memristor working as a memory cell. As a memristor does not consume area more than required for two perpendicular wires and power to save its state in standby mode, memristor is a best option for a switch based memory cell in Crossbar Architectures. Selection of a memory cell (memristor) is done by

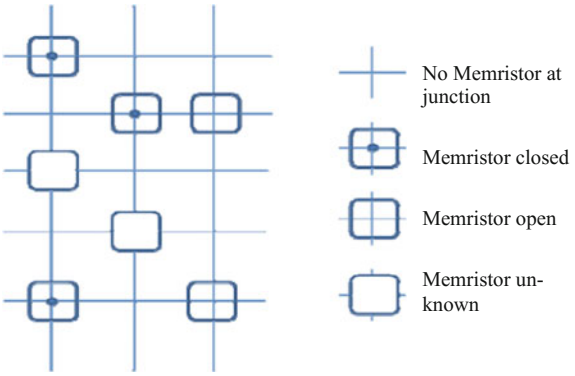

Fig. 1 Memristor crossbar array

applying voltage on those selected wire/lines. Wired AND, NAND, XOR, SOP implementation using memristor crossbar is given in Fig. 2a and future work includes-

i. Multiple output implementation
ii. Multi crossbar architecture
iii. Implication logic

Equivalent circuit for a NAND gate works in following three stages:

i. Latch input operation- In this stage, the input data from the three input terminals A, B, C is stored in the memristors M1–M3. Here, we have to apply a writing voltage (V_w) at the input terminal IN. Assuming that the inputs A, B, C are outputs of other memristors; the logic state of signals A, B, C is latched into M1–M3 respectively.
ii. Copy inputs & close AND- Here we are copying data from M1–M3 to M4–M6 and closing M7 by applying V = 0 at IN, K and V_w at AND. M7 will be used in next stage as this is inverting stage configuration.

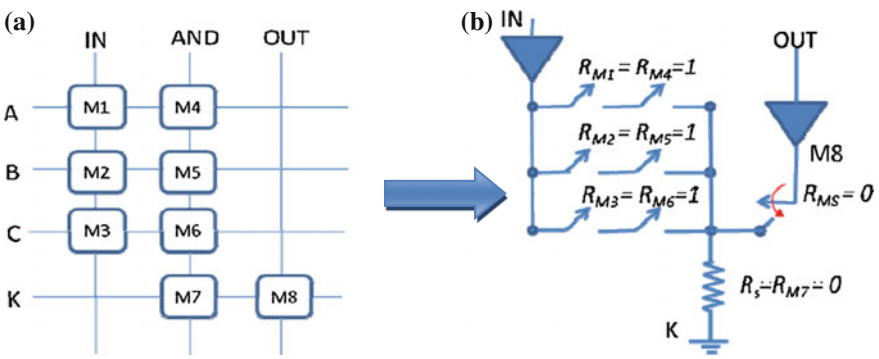

Fig. 2 Memristor crossbar with a 3-input NAND gate. **a** The crossbar with a 4 × 3 tile. **b** The equivalent circuit of NAND gate

iii. Evaluate and Capture- Here we have to apply read voltage (Vr) at IN and V_w at OUT.

In order to read the output of the memristor M8, we need to disable the memristor M7 by applying a large negative voltage on AND to open memristors M4–M7 first and then the memristor M8 can be read out by applying a voltage $V = 0$ at OUT and using the output terminal as an input to a subsequent crossbar logic gate. Figure 2b is showing Evaluate and Capture stage of 3-input NAND gate implementation. Memristor can have many resistance levels, we can use some discrete value as different logic levels and thus can use in multi value logic system as reported by Mohsin (2010). The memristor is basically a resistor whose resistance increases when current flows from one direction and decreases when current flows from opposite direction, So small pulses of current can be applied to change its resistance level to up or down depending on duration, direction and strength of current pulse. Both Hard switching and Soft Switching can be done on the device for binary or multilevel storage respectively. After storing values there is no need of refreshing as data is in resistance value form, therefore no external power source is required to save data for very large time duration.

Liu et al. (2010) propose a behavioral modeling method by constructing two different workable memristor models. The models proposed are based on experimental measured data of Au/Ti_2O_5/Au and Pt/TiO_2/Al memristor, fabricated in their lab. Curve fitting in MATLAB is also used. The proposed modeling method can be used efficiently to choose different memristor materials or fabrication technique, and the usefulness of which will be amplified by pursuing system-level analyzing and large scale design of memristor arrays. Compact models for current controlled and voltage controlled memristor implementable in SPICE, verilog-A and Spectre, which are suitable for frequency dependent memristive hysteresis behavior reported by Shin et al. (2010). This shows unique boundary assurance to simulate memristors whether they behave memristive or resistively. Parameter extraction, simulation results with macro model shown. Discussion given on- dependency of model on type of excitation signal and nonlinear dopant drift effect.

da Costa et al. (2012) were implemented the model in verilog- AMS and simulated in mentor graphics with AMS support. Switching between memristive and resistive states occurs when the potential barrier that separates the doped and undoped regions moves totally to one of sides and return only when the stimulus is inverted. The model can be used for mixed-signal or multi-domain simulation in circuit designs using memristor.

Figure 3 shows voltage and current output response for memristor model with input voltage frequency $f_0 = 1$ Hz, input voltage amplitude $V_0 = 1$ V, dopant ion mobility $\mu_v = 10^{-10}$ $cm^2 s^{-1} V^{-1}$, device length D = 10 nm and off to on resistance ratio $R_{off}/R_{on} = 160$. It is clear from the Fig. 3 that if the input biasing is applied for a time period more than required for full length boundary movement, then the resistance of memristor will be saturated to one of its boundary value (either R_{off} or R_{on} depending upon biasing polarity) and will remain at it until the input bias polarity is reversed. The memristor will not show any nonlinearity in the case and

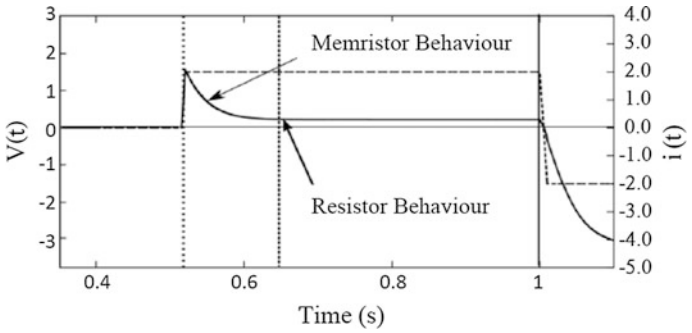

Fig. 3 Variation in stability memristor switching

will work as simple resistor. Changing the biasing will again change the resistance of memristor to other boundary value as shown in Fig. 3.

A preliminary SPICE macro model of memristor to develop models for the SPICE based analysis tools like HSPICE and Spectre was reported by author Mohanty (2013). An interpretation of the memristor device recalling the quasi-static expansion of Maxwell's equations and a review on Chua's argumentation about the memristor relating to the electromagnetic theory was also given. They have concluded that the Von-Neumann architecture, which is the base of all current computer systems, is not capable for carrying out computations with nano-devices and materials. There are lots options as different components but they are poor at mimicking the human brain. However, the memristor motivates future work in nano-electronics and nano-computing based on its capabilities.

3 Variables and Circuit Elements

Variables and circuit elements are important key components for any type of advanced system design. Fundamental variables and basic circuit elements had been evolution from many decades ago. New elements envisioning for the sake of completion of a physical system is not without scientific precedent. Indeed, the well known discovery of the periodic table for chemical elements by Mendeleef in 1869 is a case in point. From the circuit theory point of view, the relationship between two of four fundamental circuit variables; namely current (i), voltage (v), charge (q), flux-linkage (φ), define three basic two terminal elements (Sharma et al. 2015). Figure 4 shows the relationships between these variables and circuit elements.

Out of the six possible combinations of these variables, five are well known relationships. Two of these relationships are given by $q(t) = \int_{-\infty}^{t} i(\tau)d\tau$ and $\varphi(t) = \int_{-\infty}^{t} v(\tau)d\tau$. Other three relationships are given by axiomatic definition of the

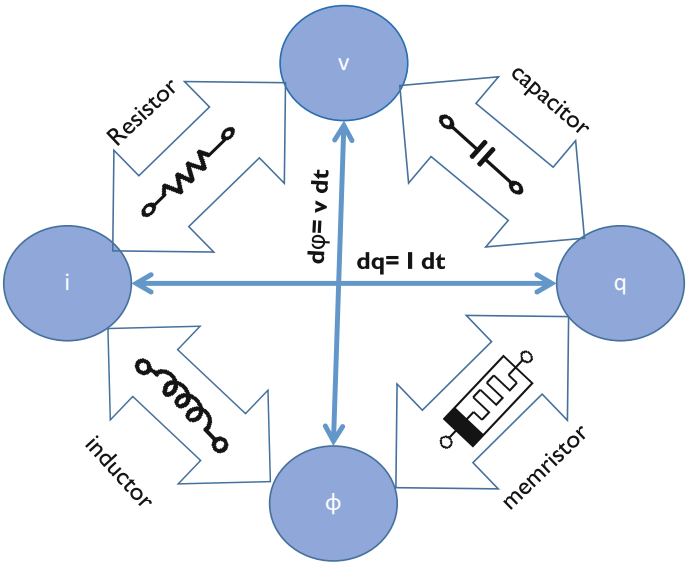

Fig. 4 Variables and circuit elements

Fig. 5 Memristor symbol

three fundamental circuit elements, namely, Resistor ($R = \frac{v}{i}$; relation between voltage and current), Capacitor ($v(t) = \frac{1}{C}q(t)$; relation between charge and voltage) and inductor ($i(t) = \frac{1}{L}q(t)$; relation between flux and current). For the sake of completeness from logical and axiomatic point of view, Prof. Leon O. Chua argued for the *Memristor* (a contraction for Memory resistor because it behaves somewhat like a nonlinear Resistor with memory) to set up a mathematical relationship between electric charge and magnetic flux (Chua 1971).

The memristor device is characterized by a nonlinear relation between charge and flux, i.e. time integrals of voltage and current. The symbol of memristor is shown in Fig. 5.

4 Linear Model of Memristor

There are two models of memristor, viz. linear model and non-linear model.

In this chapter, we shall discuss only the linear model of memristor in detail. The linear model of memristor is described for simple dopant ion drift kinetics in the memristor which is not including any type of nonlinearity issues for the case of

simplicity. The modelling is done on MATLAB and results are presented in subsequent sessions. This chapter deals with the proposed linear model and discussion of its results. Further output analysis in terms of state variable has been done here with different driving voltage waveforms. In Sect. 5, the shortcomings of the linear model with output waveforms are being analysed. All the input parameters associated with the model are explained here.

First, the mathematical model of linear model is developed and explained below:

4.1 Mathematical Linear Model of Memrisror

In 1971, (Chua 1971) proposed memristance as the functional property of memristors; that correlates charge and flux, i.e.

$$M = \frac{d\varphi}{dq} \tag{1}$$

Since the flux is integration of voltage and charge is integration of current, the memristance has the same units as resistance. Later on, Chua and Kang (1976) generalized the concept to memristive systems, i.e.

$$v = R(x)i \tag{2}$$

$$\frac{dx}{dt} = f(x, i) \tag{3}$$

where v is the voltage, i is the current, and $R(x)$ is the instantaneous resistance that is dependent on the internal state variable x of the device. This state variable x is bounded within the interval [0, 1], and it is simply the normalized width of the doped region $x = \frac{w}{D}$ with D being the total thickness of the switching bilayer and w is width of doped region at the instant. At time t, the width of the doped region w depends on the amount of charge that has passed through the device; thus, the time derivative of w is a function of current, which can be described as

$$\frac{dw}{dt} = V_d = \mu E = \mu R_{on} \frac{i(t)}{D} \tag{4}$$

where V_d is the speed at which the boundary drifts between the doped and undoped regions, μ is the average dopant mobility, μE is the electric field across the doped region in the presence of current $i(t)$, R_{on} and R_{off} are the net resistances of the device when the active region is completely doped and undoped respectively.

The definition of memristance can be generalized as follows:

$$v(t) = M(t)i(t) \tag{5}$$

$$M(t) = R_{on}x(t) + R_{off}(1 - (x(t)) \tag{6}$$

$$v(t) = \left[R_{on}x(t) + R_{off}(1 - (x(t))\right]i(t) \tag{7}$$

$$\frac{dx}{dt} = \mu \frac{R_{on}}{D^2} i(t) \tag{8}$$

It is clear from above Eq. (8) that memristive effect is considerable in nanoscale devices due to the D^2 factor in denominator, which shows that memristive effect is 10^6 times better in nanoscale devices as compared to micro scale devices.

The MATLAB model simulation results, based on this mathematical model, are shown in Fig. 6 for sinusoidal Driving Voltage waveform.

The time axis is showing here the step number, as the time period $T = 1.5$ s is divided in 1000 steps due to the reason that MATLAB is a Digital Environment Programming Language and all the operations like integration and differentiation are performed here with difference equations and hence steps are required for the same. The driving voltage for this linear model is $v(t) = V_o \sin(2\pi ft)$ with $V_0 = 1.5$ V. As the signature characteristics of memristor (Chua 1971) is its pinched hysteresis loops in current-voltage characteristics, the output waveforms (I–V curves) in Fig. 6 are enough for validation of model by showing a pinched

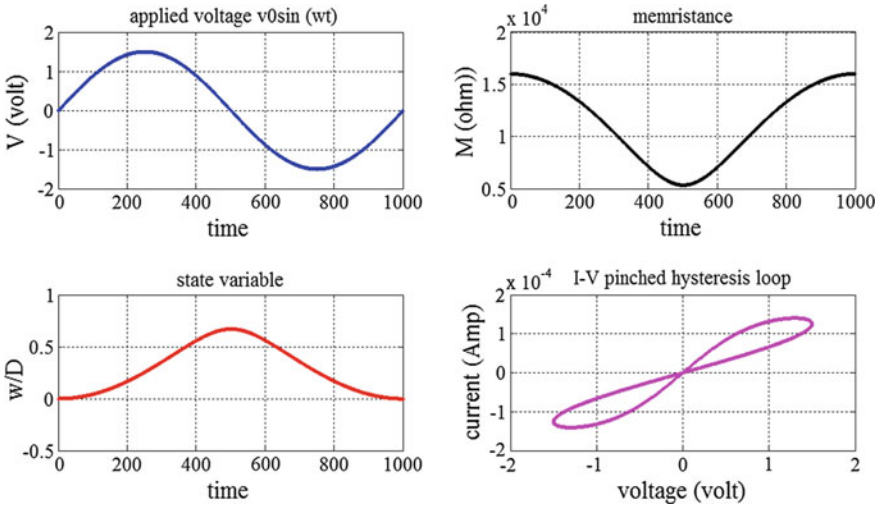

Fig. 6 Simulation curves for linear model with $V_0 = 1.5$ V, $T = 1.5$ s, $D = 10$ nm, $\mu = 10^{-14}\text{m}^2/\text{V.Sec}$, $R_{on} = 100\ \Omega$, $R_{off} = 16\ \text{K}\Omega$

hysteresis loop. The model is showing resistance switching between the predefined range, viz. $[R_{on}, R_{off}]$. Here the state variable x is having its maximum value ~ 0.65 and corresponding to this value the memristance of the device is $\sim 550\,\Omega$.

4.2 Boundary Movement Condition

The maximum value of state variable is not equal to 1. That is, the voltage amplitude is not sufficient for full length conductive layer, as it can be seen in Fig. 6. However, it also depends on the initial value of the state variable. We are assuming the initial value of the state to be zero, i.e. $x(0) = 0$.

Therefore, increasing the voltage amplitude increases the maximum value that can be obtained by the state variable keeping the time period of the driving voltage wave constant.

From the Eqs. (7) and (8), we have

$$\frac{dx}{dt} = \mu \frac{R_{on}}{D^2} \frac{v(t)}{\left[R_{on}x(t) + R_{off}(1 - x(t))\right]} \tag{9}$$

We know that $R_{off} \gg R_{on}$ and $0 < x(t) < 1$.

Thus, we can assume that $R_{on}x(t) + R_{off} \approx R_{off}$.

With this assumption, we can simplify Eq. (9) as follows:

$$\frac{dx}{dt} = \mu \frac{R_{on}}{D^2} \frac{v(t)}{R_{off}[1 - x(t)]} \tag{10}$$

We define $k = \mu \frac{R_{on}}{D^2 R_{off}}$ and $\beta = \frac{R_{off}}{R_{on}}$.

Then we can write Eq. (10) as follows:

$$[1 - x(t)]\, dx(t) = kv(t)\, dt \tag{11}$$

We integrate Eq. (11) with the initial condition $x(0) = 0$. Thus, we get

$$x(t) - \frac{[x(t)]^2}{2} = k\varphi(t) \tag{12}$$

For the full length travel of boundary between doped and undoped layers, we can take the final condition for the state variable as $x(T) = 1$.

From Eq. (12), it is clear that for maximum value of state variable $x(t) = 1$,

$$\text{flux } \varphi(t) = \frac{1}{2k} = \frac{\beta D^2}{2\mu} \tag{13}$$

Equation (13) is representing the amount of flux required for full length travel of the boundary between doped and undoped layers for any driving voltage.

In this work, we take $\beta = 160, D = 10^{-8}$ m, and $\mu = 10^{-14}$ m^2/V.sec. Also, the flux value $\varphi(t) = 0.8$ Weber for t being the time instant when $x(t) = 1$.

4.3 *Linear Model Results with Driving Voltage*

The Flux is defined as area under the voltage-time curve. We will now see the boundary movement for different types of driving voltage waveforms. For same Flux value the amplitude and shape of voltage wave changes. Correspondingly, the state variable value pattern also changes.

4.3.1 Sinusoidal Wave

For a sinusoidal voltage input, flux in positive half cycle is-

$$\int_0^{T/2} v(t)dt = \varphi\left(\frac{T}{2}\right) = V_0 \frac{T}{\pi} \tag{14}$$

with $T = 2$ s and $V_0 = 1.29$ V, the following wave output in Fig. 7 is obtained with the linear memristor model. The area under the driving voltage curve is obtained as $\varphi\left(\frac{T}{2}\right) = 0.821$ and the maximum value of state variable is obtained as $x\left(\frac{T}{2}\right) = 0.96$.

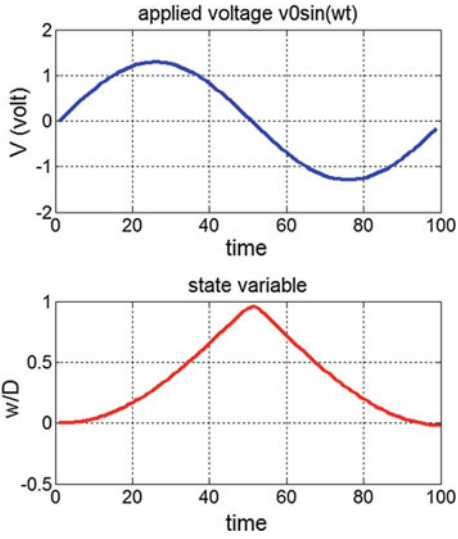

Fig. 7 The state variable response for sinusoidal voltage input

4.3.2 Triangular Wave

For a triangular voltage input, flux in positive half cycle is obtained as

$$\int_0^{T/2} v(t)dt = \varphi\left(\frac{T}{2}\right) = V_0\frac{T}{\pi} \tag{15}$$

with $T = 1.5$ s and $V_0 = 2.19$ V, the following wave output in Fig. 8 is obtained with the linear memristor model. The area under the driving voltage curve is obtained as $\varphi\left(\frac{T}{2}\right) = 0.821$ and the maximum value of state variable is obtained as $x\left(\frac{T}{2}\right) = 0.96$.

It is clear from Figs. 7 and 8 that the output response for both the triangular wave and sinusoidal wave input type is almost of same shape and so the maximum attainable value of state variable for the same flux (area under the curve) is also same. The case will be different for the input waves with abrupt changes (Fig. 9).

4.3.3 Square Pulse

- **Returning Zero type-** For a square pulse (RZ) voltage input, flux in positive half cycle is obtained as

$$\int_0^{T/2} v(t)dt = \varphi\left(\frac{T}{2}\right) = \int_0^{T/4} v(t)dt + \int_{T/4}^{T/2} v(t)dt = V_0\frac{T}{4} \tag{16}$$

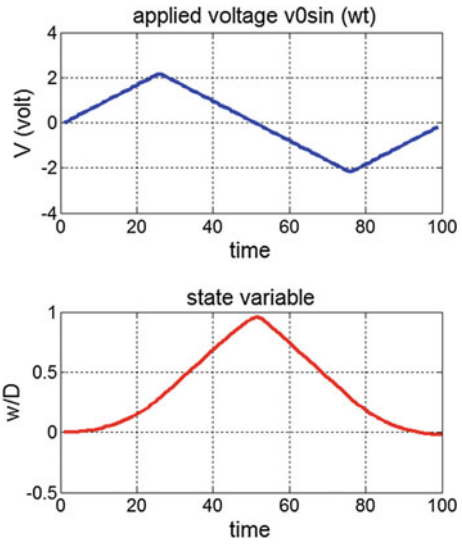

Fig. 8 The state variable response for triangular voltage input

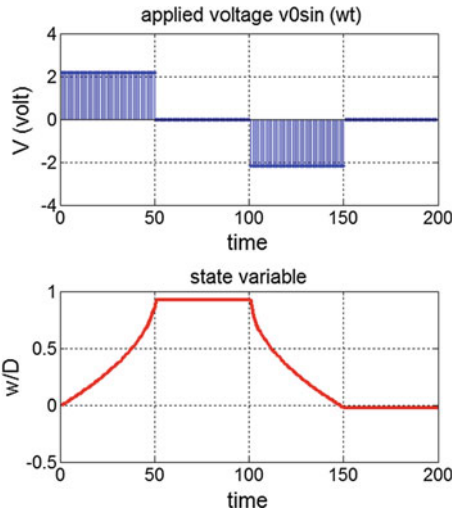

Fig. 9 The state variable response for square pulse (RZ) voltage input

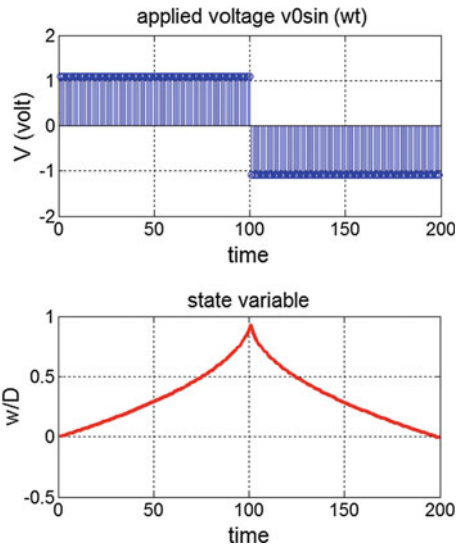

Fig. 10 The state variable response for square pulse (NRZ) voltage input

with $T = 1.5$ s and $V_0 = 2.183$ V, the following wave output in Fig. 10 is obtained with the linear memristor model. The area under the driving voltage curve is obtained as $\varphi\left(\frac{T}{2}\right) = 0.818$ and the maximum value of state variable is obtained as $x\left(\frac{T}{2}\right) = 0.87$.

Non-Returning Zero Type- For a square pulse (NRZ) voltage input, flux in positive half cycle is-

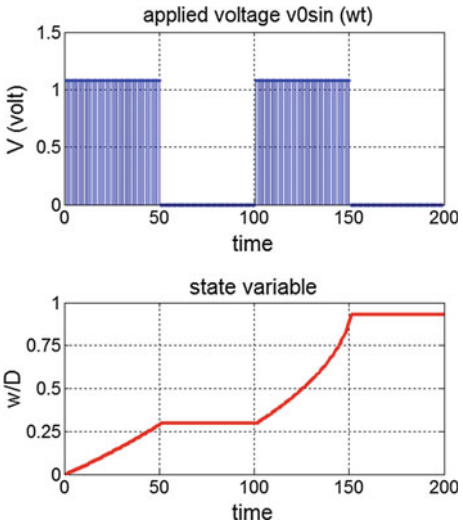

Fig. 11 The state variable response for two pulse (Digital) voltage input

$$\int_0^{T/2} v(t)dt = \varphi\left(\frac{T}{2}\right) = \frac{T}{2}V_0 \tag{17}$$

with $T = 1.5$ s and $V_0 = 1.09$ V, the following wave output in Fig. 11 is obtained with the linear memristor model. The area under the driving voltage curve is obtained as $\varphi\left(\frac{T}{2}\right) = 0.817$ and the maximum value of state variable is obtained as $x\left(\frac{T}{2}\right) = 0.91$.

4.3.4 Two Pulse

For a two pulse (Digital) voltage input, flux in positive voltage part is-

$$\int_0^T v(t)dt = \int_0^{T/4} v(t)dt + \int_{T/4}^{T/2} v(t)dt + \int_{T/2}^{3T/4} v(t)dt + \int_{3T/4}^{T} v(t)dt = \varphi(T) = \frac{T}{2}V_0 \tag{18}$$

with $T = 1.5$ s and $V_0 = 1.05$ V, the following wave output in Fig. 11 is obtained with the linear memristor model. The area under the driving voltage curve is obtained as $\varphi(T) = 0.788$ and the maximum value of state variable is obtained as $x(T) = 0.84$.

4.3.5 Four Pulse

For a Four pulse (Digital) voltage input, flux in positive voltage part is given by

$$\int_0^T v(t)dt = \varphi(T) = \frac{T}{2}V_0 \tag{19}$$

with $T = 1.5$ s and $V_0 = 1.05$ V, the following wave output in Fig. 12 is obtained with the linear memristor model. The area under the driving voltage curve is obtained as $\varphi(T) = 0.788$ and the maximum value of state variable is obtained as $x(T) = 0.84$.

This is clear from state variable responses for all above waveform types of Driving Voltage full length boundary movement can be achieved with a certain flux value. This Flux value can be calculated from the Eq. (13) for given set of parameter (β, μ, D) values. For abrupt changes in input voltage values there is significant nonlinear effect in the output response and for input types with continuous value changes the output response is not showing any nonlinearities and so the maximum attainable state variable value is more near to 1 in the same case.

The overview of results for all above types of waveforms is given in Table 1 below including maximum attainable state variable value and the Flux applied (Area under the Driving Voltage Curve) for the same.

The Table 1 clarifies that for maximum attainable state variable value, which is showing here full length boundary movement, the required Flux is almost same for all types of waveforms and this itself is almost equal to the theoretically calculated value of Flux for full length boundary Movement from (13).

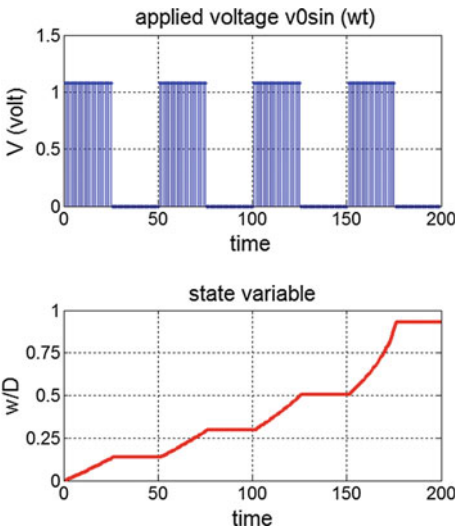

Fig. 12 The state variable response for Four pulse (Digital) voltage input

Table 1 Flux requirement for maximum attainable state variable value for different waveforms

Waveform shape	Area of positive cycle	Time period T (s)	Amplitude V_0(V)	Flux in positive cycle	$X_{max} = (w/D)_{max}$
Sinusoidal	$(1/\pi)V_0.T$	2	1.29	0.821	0.96
Triangular	$(¼)V_0.T$	1.5	2.19	0.821	0.96
Square NRZ	$(½)V_0.T$	1.5	1.09	0.817	0.91
Square RZ	$(¼)V_0.T$	1.5	2.183	0.818	0.87
2 Pulse	$(½)V_0.T$	1.5	1.05	0.787	0.84
4 Pulse	$(½)V_0.T$	1.5	1.05	0.787	0.84

The same calculation procedure can be applied for any certain value of state variable value. The only difference will be the value of $x(t)$ in (12) for which we are analyzing the model. We analyze the linear memristor model for the same set of parameter values, i.e. $\beta = 160$, $D = 10\,\text{nm}$, $\mu = 10^{-14}$ $\text{m}^2/\text{V.Sec}$ with the final state variable value $x(t) = 0.27$. The corresponding flux value is obtained as

$$\varphi(t) = \frac{1}{k}\left[x(t) - \frac{x(t)^2}{2}\right] = 1.6\left[0.27 - \frac{(0.27)^2}{2}\right] = 0.374 \tag{20}$$

the driving voltage wave we are considering here is square pulse (RZ) with $V_0 = 1$ V and $T = 1.5$. For these values, the area under the curve is obtained as $V\left(\frac{T}{4}\right) = 0.375$, which is again equal to the theoretically calculated required flux value given in (20). The state variable response is shown in Fig. 13.

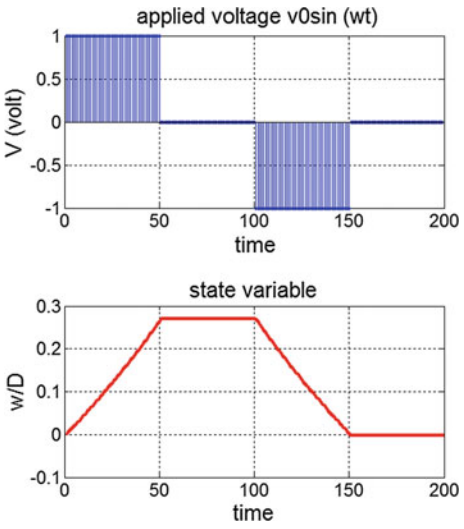

Fig. 13 The state variable response for square pulse (RZ) voltage input

Figure 13 clarifies that, except for the end positions, the nonlinear effects are insignificant for middle part of the device as the nonlinearities in output response are very less even for the input voltage wave with abrupt changes in the magnitude.

5 Shortcomings of the Linear Memristor Model

The shortcomings of the linear memristor models are its terminal state problem, boundary issues and nonlinear effects. These are as explained below:

5.1 The Terminal State Problem

After a limit of the voltage amplitude the state variable value goes out of the defined limit, i.e. [0,1]. This is named as '*The Terminal State Problem*' as after a limit the state variable cannot come to the range defined even if negative voltage is applied.

Figure 14 clarifies that in first positive half cycle the memristance is decreasing while the state variable is going towards maximum value and vice versa for the next negative half cycle. It can be seen that the maximum value of state variable is not exactly equal to 1. We expect that the voltage amplitude is not sufficient for full length conductive layer (moreover it also depends on the initial value of the state variable, but here we are assuming it to be zero).

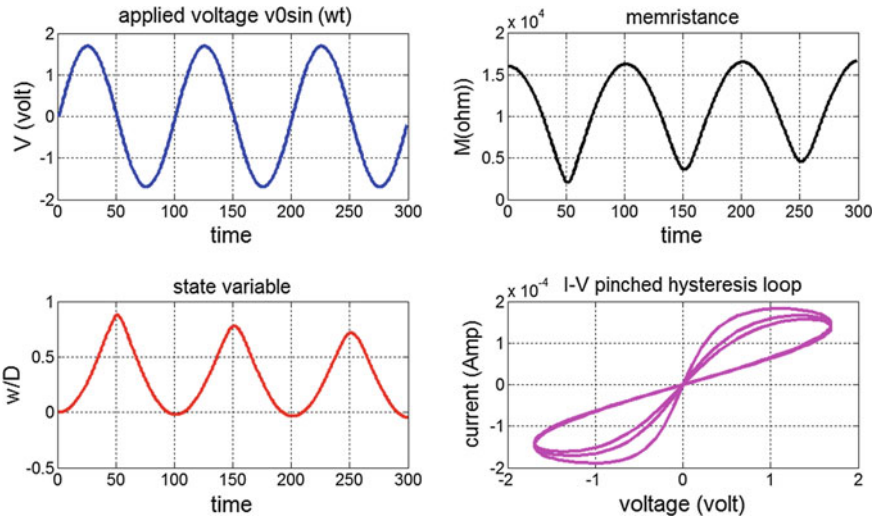

Fig. 14 Simulation curves for linear model with $V_0 = 1.69\,\text{V}, T = 1.5\,\text{s}$, Steps = 100/cycle

Table 2 First maximum and minimum value of state variable with increasing voltage amplitude

V_0	$X_{max\cdot 1}$	X_{min1}	X_{min2}
1.69	0.86	0	–0.03
1.7	0.9	0	–0.04
1.71	0.93	–0.02	–0.04
1.72	0.953	–0.02	–0.05
1.725	0.99	–0.025	–0.055
1.73	2	1.2	1.2

Increasing the voltage amplitude increases the maximum value that can be obtained by the state variable, but up to an extent only and after that terminal state problem arises.

Table 2 shows the corresponding maximum values of state variable. We can see from Table 2 that voltage amplitude value 1.73 is showing terminal state problem as the minimum value of state variable is also 1.2, which is not in the predefined range [0, 1]. Figure 15 clarifies the terminal state problem more clearly.

There are also other problems observed in Table 2 such as the negative minimum values of state variable. This is due to the programming in Digital Environment. Here application of sinusoidal driving voltage on memristor is done with 100 time steps and these steps are taking the value of $V_0 \sin(\omega t)$ for total step period which is at the starting instant of the step. So there is arising some asymmetry in wave in positive and negative half cycle.

Figure 16 depicts this phenomena with number of steps equal to 20 and 100.

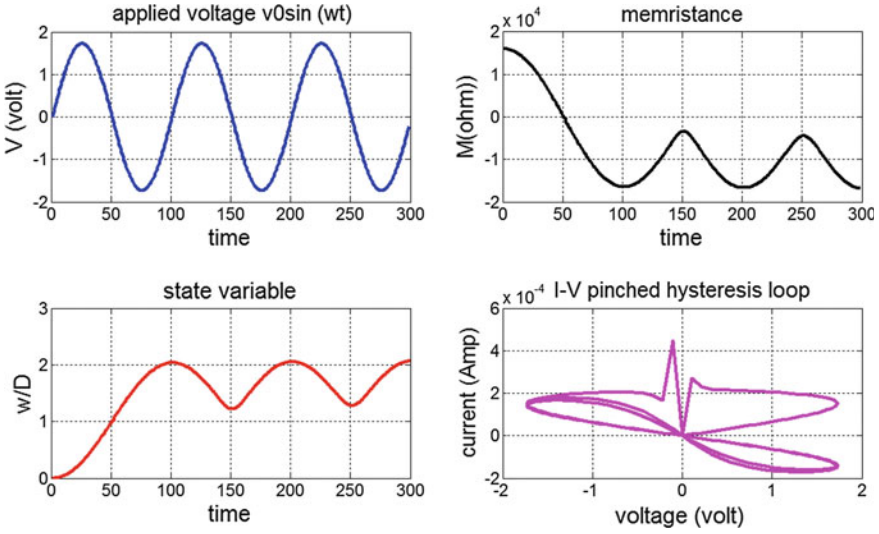

Fig. 15 Simulation curves for linear model showing The Terminal State Problem, with $V_0 = 1.73$ V, $T = 1.5$ s, Steps = 100/cycle

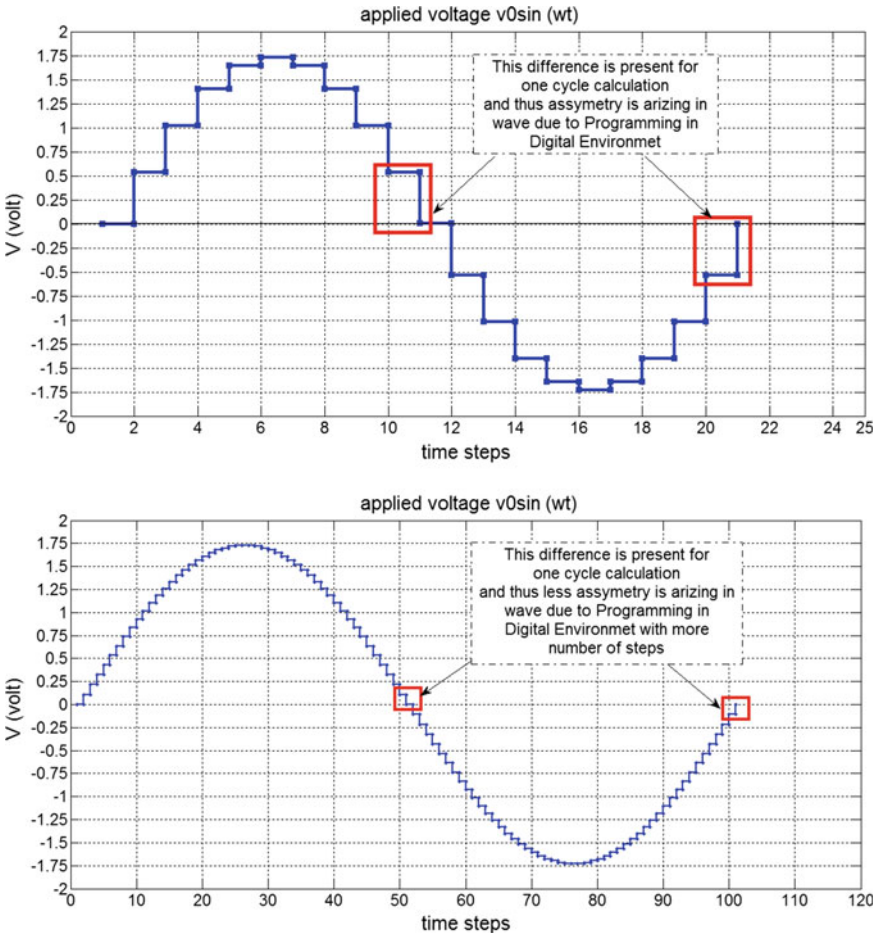

Fig. 16 Asymmetry in biasing voltage waveforms due to digital environment

5.2 Boundary Issues and Nonlinear Effects

When assuming that the generated electric field is small enough, the linear dopant drift model can approximate the dynamics of a memristor. However, this model is invalidated at boundaries when the boundary between doped and undoped regions is at either of end, i.e. when w $\gtrsim$ 0 or w $\lesssim$ D. This is due to the influence of a non-uniform electric field that significantly suppresses the drift of the dopants. The limitations of this model are revealed when, for example, driving a TiO_2/TiO_{2-x} memristor (Ron = 100 Ω, Roff = 16 kΩ, w_0 = 5 nm, D = 10 nm, and $\mu = 10^{-14}$ m^2/V s) into its extreme states, i.e., saturation ($w = D$) and depletion ($w = 0$). In the case of saturation, w exceeds the limit value of D (10 nm), whereas the device's memristance falls below the 100 Ω cut-off value (Ron). Likewise, in depletion,

w can take negative values with the memristance exceeding the upper limit of 16 kΩ (Roff), which is clearly erroneous. At the edges of device some fringing fields also exists and over the length of the device also some nonlinearities exists. Applying a nonlinear drift over dopants at the edges of device to get rid of boundary issues is called Non-linear dopant drift model.

6 Frequency-Voltage Relationship

The Linear Memristor model analysis shows that the increase in the frequency of Driving Voltage decreases the Flux in one cycle with the same magnitude of voltage. As we have discussed in Table 1, the flux required for movement of boundary up to a certain position or more clearly flux required for a certain state variable value is constant if the parameters are taken not varying their value. So for applying same Flux with higher Driving Voltage frequency we have to increase the peak value of the Driving Voltage wave. The relation between this peak voltage value and frequency is linear and given by

$$x(t) - \frac{[x(t)]^2}{2} = k\varphi(t), \quad k = \mu \frac{R_{on}}{D^2 R_{off}}, \beta = \frac{R_{off}}{R_{on}} \tag{21}$$

We take two different cases with $x(t) = 1$ and $x(t) = 0.5$ both with $x(0) = 0$. The flux values for these boundary positions are 0.8 Wb and 0.6 Wb respectively. Figures 17a, b show the frequency voltage curves for these two cases with sinusoidal biasing inputs for both linear and nonlinear memristor models. The flux in positive half cycle for a sinusoidal input is obtained as

$$\varphi\left(\frac{T}{2}\right) = V\frac{T}{\pi} = 0.8 \tag{22}$$

Thus, the relation between frequency and voltage for full length boundary movement can be expressed as

$$V = \frac{0.8\pi}{T} \text{ or } V = 2.512f \tag{23}$$

The relation (23) between V and f is linear. Thus, the curve $V = mf$ is expected to be linear with slope $m = 2.512$. The nonlinear model is less compatible with the theoretical model but is showing more nearby values with practically measured data, as we will see later. The initial boundary value for these cases in nonlinear models is $x(0) = 0.01$. Similarly, the second case of $x(t) = 0.5$ is giving Frequency Voltage relationship $V = 1.884\,\mathrm{f}$, which is linear again as expected.

It is clear from Fig. 17 that the nonlinear model is showing less correlation with the theoretical model as compared to the linear model. While Fig. 17b shows that

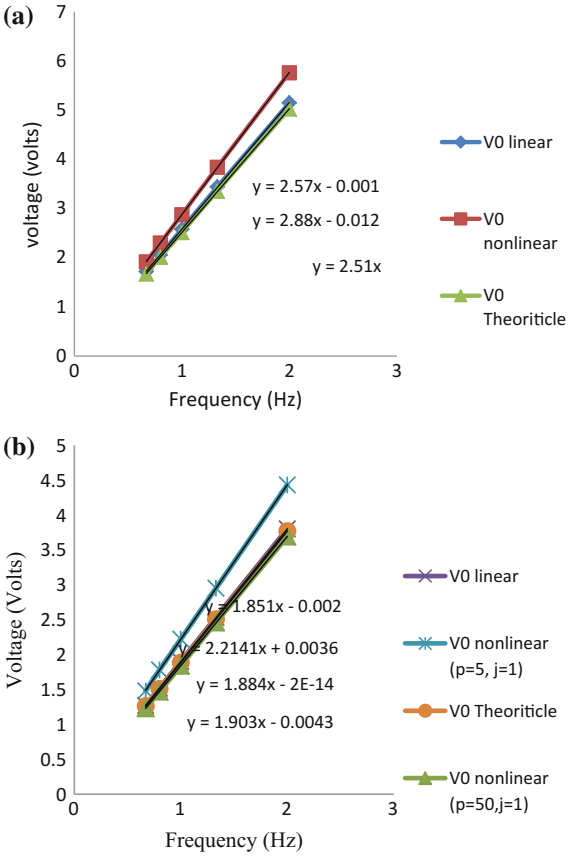

Fig. 17 Frequency voltage relationship for linear and nonlinear models for state variable value **a** $x(t) = 1$ and **b** $x(t) = 0.5$ with $\beta = 160$, $\mu = 10^{-14}$ m^2/v.sec

with higher values of p, the correlation nonlinear model response and theoretical model can be increased. The equation of linear curves are (shown in graphs above) more clearly showing the correctness of the model.

7 Effect of Parameters on F-V Curves

The reason behind the linear relationship between frequency and voltage is the dependence of flux only on the initial and final boundary position. The flux in fact depends upon the parameter values also i.e. the total device length (D), the off to on resistance ratio (β) and the mobility of charged dopant ions (μ). To observe the effect of these parameters on the flux or more clearly on frequency-voltage relationship, here one parameter is changing, keeping others constant.

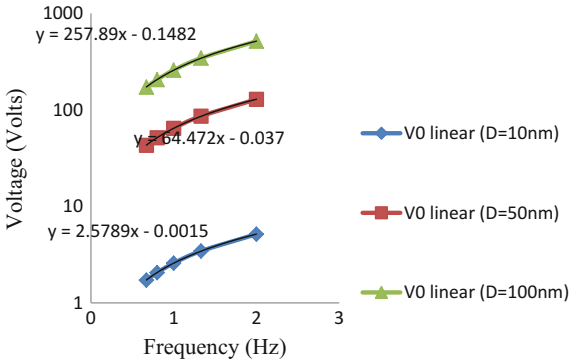

Fig. 18 Dependency of frequency-voltage curves on device length D

7.1 *Effect of Device Length (D)*

Figure 18 shows the effect of device length on frequency-voltage curves (with $\beta = 160$, $\mu = 10^{-14}$ m^2/v.sec).

For theoretical understanding of dependence on D for full length boundary movement condition, we can say

$$x(t) - \frac{[x(t)]^2}{2} = \frac{\mu}{D^2\beta}\varphi(t) \tag{24}$$

Thus, we have

$$\varphi(t) = \frac{0.5D^2(160)}{10^{-14}} = V\left(\frac{T}{\pi}\right) \tag{25}$$

or

$$V = (251.2)D^2 f \times 10^{14} \tag{26}$$

For $D = 10$ nm, 50 nm, 100 nm, the frequency-voltage relationship in Eq. (26) becomes $V = 2.51$ f, $V = 62.75$ f, $V = 251$ f, respectively.

The graphs of curves in Fig. 18 show good correlation with these theoretical equations defining the relation between voltage and frequency.

7.2 *Effect of R_{Off} to R_{On} Ratio (β)*

Figure 19 shows the effect of R_{Off} to R_{On} Ratio on frequency-voltage curves (D = 10 nm, μ = 10^{-14} m^2/v.sec). For theoretical understanding of dependence on β for full length boundary movement condition, we can say

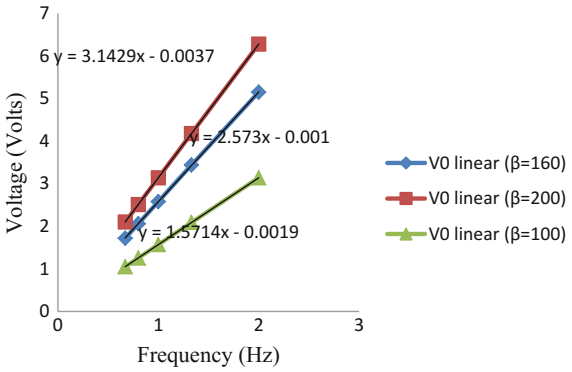

Fig. 19 Dependency of frequency-voltage curves on R_{Off} to R_{On} Ratio (β)

$$x(t) - \frac{[x(t)]^2}{2} = \frac{\mu}{D^2\beta}\varphi(t) \tag{27}$$

Thus, we have

$$\varphi(t) = \frac{0.5D^2(10^{-16})}{10^{-14}} = V\left(\frac{T}{\pi}\right) \tag{28}$$

or

$$V = (0.0157)\beta f \tag{29}$$

For $\beta = 160$, 100, 200, the frequency-voltage relationship in Eq. (29) becomes $V = 2.51\,\mathrm{f}, V = 1.57\,\mathrm{f}, V = 3.14\,\mathrm{f}$, respectively.

The graphs of curves in Fig. 19 show good correlation with these theoretical equations defining the relation between voltage and frequency.

7.3 *Effect of Charged Dopant Mobility (μ)*

Figure 20 shows the effect of Charged Dopant Mobility (μ) on frequency-voltage curves ($D = 10$ nm, $\beta = 160$). For theoretical understanding of dependence on μ for full length boundary movement condition, we can say

$$x(t) - \frac{[x(t)]^2}{2} = \frac{\mu}{D^2\beta}\varphi(t) \tag{30}$$

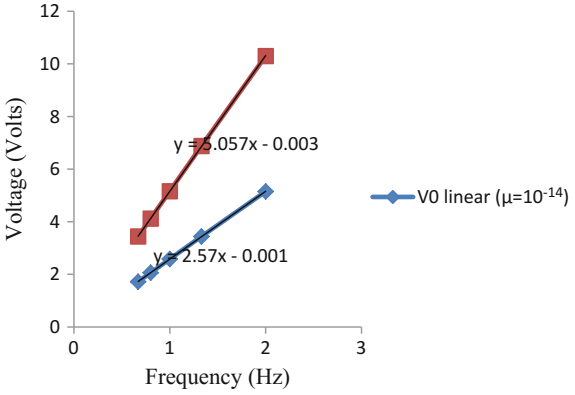

Fig. 20 Dependency of frequency-voltage curves on Charged Dopant Mobility (μ)

Thus, we have

$$\varphi(t) = \frac{0.5 \times 160 \times 10^{-16}}{\mu} = V\left(\frac{T}{\pi}\right) \tag{31}$$

or

$$V = \left(\frac{251.2 \times 10^{-16}}{\mu}\right) f \tag{32}$$

For $\mu = 10^{-14}$ $m^2/v.sec$, 5×10^{-15} $m^2/v.sec$, the frequency-voltage relationship in Eq. (32) becomes $V = 2.51\,f$, $V = 5.02\,f$, respectively. The graphs of curves in Fig. 20 show good correlation with these theoretical equations defining the relation between voltage and frequency.

7.4 *Effect of Driving Voltage Wave*

This is clear from state variable response for all waveform types of Driving Voltage that full length boundary movement can be achieved with a certain flux value. This Flux value can be calculated for given set of parameter ($\beta = 160, D = 10$ nm, $\mu = 10^{-14}$ $m^2/v.sec$) values. The overview of results for all above types of waveforms is given in Fig. 21 including maximum attainable state variable value and the Flux applied (Area under the Driving Voltage Curve) for the same.

The chart shows that for full length boundary movement, with given set of parameter values, the required flux value is $\varphi(t) = 0.8$ wb, but the maximum boundary position x_{max} cannot be equal to 1 for all types of waves due to some nonlinearities present in the device for those specific waves.

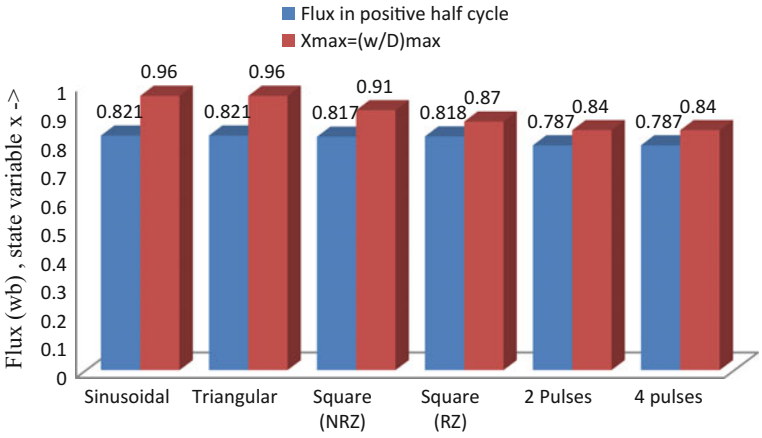

Fig. 21 Effect of driving voltage wave shape on maximum attainable boundary position

The required flux for achievable maximum boundary position can be defined by the following equation

$$x(t) - \frac{[x(t)]^2}{2} = \frac{\mu}{D^2\beta}\varphi(t) \tag{33}$$

For 2 pulse type biasing voltage, $x_{\max} = 0.84$ and the required flux for the same is $\varphi(t) = 0.78$. Also, the simulated flux value in the chart is in good coordination with the theoretical value.

8 Applications of Memristor

Recently there has been an increased interest in research on memristors due to the demonstration of memristor manufacturing as well as their potential applications. Research is in full swing to use memristors in computer memory, analog circuits, sensors, and digital logic. Memristor models need to be made available for the design engineers to use the memristor as a circuit element during design exploration. The following areas are where researchers getting interest and so getting familiar with memristor-

(i) Application of memristor in programmable logic designing
(ii) Memristor crossbar array formation
(iii) Memristor based nonvolatile memory designing and analysis
(iv) Artificial intelligence
(v) Thinking machine

(vi) Realization of artificial neural networks
(vii) Signal processing and control systems
(viii) Other analog and digital applications

9 Summary

A brief background of memristor and its development as a device and logic design are discussed first in this chapter. A linear model of memristor is proposed. Next, mathematical modelling and simulation results are presented for the linear model of memristor. The memristor has been modelled in various tools in VLSI Design including the nonlinear effects but till now only linear model is available for MATLAB. The conclusions have been drawn from the simulation results. The final boundary position depends on the flux passed through the device and initial boundary position for constant parameter (β, μ, D) values. So the boundary will definitely come to its initial position if the net applied flux is zero. The final state variable value does not depend upon the driving voltage wave shape if the flux corresponding to all the wave shapes is same. The terminal state problem can be successfully overcome by a lesser value of scaling parameter, both for hard current and soft current applications. Memristor is new device having both linear and non-linear behaviour. Linear model for memristor is discussed in detail in this chapter and non-linear model may considered as future work for memristor development.

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