Memristor and Inverse Memristor: Modeling, Implementation and Experiments

Mohammed E. Fouda, Ahmed G. Radwan and Ahmed Elwakil

Abstract Pinched hysteresis is considered to be a signature of the existence of memristive behavior. However, this is not completely accurate. In this chapter, we are discussing a general equation taking into consideration all possible cases to model all known elements including memristor. Based on this equation, it is found that an opposite behavior to the memristor can exist in a nonlinear inductor or a nonlinear capacitor (both with quadratic nonlinearity) or a derivative-controlled nonlinear resistor/transconductor which we refer to as the inverse memristor. We discuss the behavior of this new element and introduce an emulation circuit to mimic its behavior. Connecting the conventional elements with the memristor and/or with inverse memeristor either in series or parallel affects the pinched hysteresis lobes where the pinch point moves from the origin and lobes' area shrinks or widens. Different cases of connecting different elements are discussed clearly especially connecting the memristor and the inverse memristor together either in series or in parallel. New observations and conditions on the memristive behavior are introduced and discussed in detail with different illustrative examples based on numerical, and circuit simulations.

Keywords Circuit theory · Memristor · Inverse memristor · Pinched hysteresis

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1 Introduction

Since postulating the existence of the memristor in 1971 by Leon Chua, a huge number of publications have been published. These publications address modeling (Radwan et al. 2010a, b), and analysis. Chua (1971); Kozma et al. (2012); Radwan and Fouda (2015); Adamatzky and Chua (2013); Fouda and Radwan (2015a, b). In addition, memristors have been used in many applications such as sinusoidal oscillators (Talukdar et al. 2011a, b, 2012), relaxation oscillators (Fouda et al. 2013; Khatib et al. 2012; Fouda and Radwan 2015c; Zidan et al. 2011, 2014), nonlinear control systems (Vaidyanathan and Volos 2016b), chaotic systems (Vaidyanathan and Volos 2016a; Gambuzza et al. 2015; Radwan et al. 2011), digital and analog circuits (Radwan and Fouda 2015; ElSlehdar et al. 2015). Memristors have a unique behavior which distinguish them from voltage–current other nonlinear devices. They exhibit pinched hysteresis in the plane. The hysteresis lobe area of memristor decreases monotonically as the excitation frequency increases. Also, the pinched hysteresis loop should shrink to a single-value when the frequency tends to infinity. This means that the lobe area declines with increased frequency. These characteristics should exist in a device to be referred to as a memristor (Biolek et al. 2011; Adhikari et al. 2013).

There are two categories of memristor models, current- and voltage-controlled models. The current-controlled memristor has a state variable that is function of the current passing through the memristor such as the HP model (Joglekar and Wolf 2009), and Picket model (Pickett et al. 2009). On the other hand, the state variable of the voltage-controlled memristor is a function of the voltage across the memristor (Kozma et al. 2012; Radwan and Fouda 2015). Some of these models are simple and some of them are complex but all of them capture the main memristor characteristics which should exist regardless of the memristor type.

There is another way to distinguish between memristor types which is based on the ideality of the device. According to this, we have two main types of the memristor; ideal and nonideal memristors. The memristor is called ideal if the self cross point is the origin. Otherwise, it is called nonideal memristor (Biolek et al. 2015). The non-ideality may appear in the devices due to the existence of reactive elements as will be discussed in detail in this chapter.

The inverse memristor is a system that exhibits self crossing pinched hysteresis. Contrarily with memristors, the memristor hysteresis widens with increasing the applied frequency (Fouda et al. 2015). The inverse memristor can be modeled as a nonlinear inductor or a nonlinear capacitor (with quadratic nonlinearity) in series with a resistor. As a conclusion, pinched hysteresis is a necessary but not a sufficient condition to prove the memristivity. Other conditions should be satisfied as well.

Considering memristor and inverse memristor in circuit theory is essential. That's why, many publications have been published to discuss the memristor inside conventional circuits. The memory existence inside memristive devices gives new characteristics. By adding the memristor to well known circuits, new responses and behaviors are obtained due to the unique behavior of the memristor (Radwan and Fouda 2015).

This chapter is organized as follows: section I introduces a generalized mathematical model for all the possible cases for circuit elements. Memristor is the special case of this modeling equation as deduced in section II. In section III, based on the generalized equation, we find a new element which has the opposite characteristics of the memristor. This element is discussed in details with some circuit emulators to proof the concept. In section IV, different circuit configurations are discussed and its effect on the hysteresis. Finally, conclusions are given.

2 Generalized Equation Model

A general equation can be defined as follows:

$$y = ax + (b + ex)\frac{dx}{dt} + (d + cx)\int_0^t x(\tau)d\tau \tag{1}$$

where y is a normalized output, x is a normalized input signal, and (a, b, c, d, e) are scaling constants. Equation (1) describes the different cases of applying an input signal and/or effect of integrating and differentiating the input signal.

This equation contains the definitions of all known circuit elements as we will discuss later. But firstly, let's study the behavior of this modeling equation under a sinusoidal excitation assuming $x(t) = ksin(\omega t + \phi)$. Therefore,

$$\frac{dx}{dt} = k\omega cos(\omega t + \phi) = \pm\omega\sqrt{k^2 - x^2} \tag{2}$$

and

$$\int_0^t x(\tau)d\tau = \frac{1}{\omega}\left(kcos(\phi) \mp \sqrt{k^2 - x^2}\right) \tag{3}$$

Substituting into (1) and using trigonometric identities, one obtains

$$y = ax + k(d + cx)\frac{cos(\phi)}{\omega} \pm \left(\left(e\omega - \frac{c}{\omega}\right)x + \left(b\omega - \frac{d}{\omega}\right)\right)\sqrt{k^2 - x^2} \tag{4}$$

This equation has the following properties:

1. There exists a line of odd-symmetry given by the first order relation between y and x
$$y = ax + k(d + cx)\frac{cos(\phi)}{\omega} \tag{5}$$
2. A pinched-double loop hysteresis behavior is observed in the x-y plane. The double-loop intersects itself at a point known as the pinch-point (x_p, y_p) obtained

by equating $\sqrt{k^2 - x^2}$ to zero; yielding

$$x_p = \frac{b\omega^2 - d}{c - e\omega^2},\ y_p = ax_p + k(d + cx_p)\frac{cos(\phi)}{\omega} \tag{6}$$

At high frequency, this pinched point reduces to $\left(\frac{-b}{e}, \frac{-ab}{e}\right)$ while at low frequency it reduces to $\left(\frac{-d}{c}, 0\right)$. It is obvious that some scaling coefficient are amplified with increasing the frequency; namely b and e while other coefficients vanish with increasing the applied frequency like c and d. Changing the frequency does not affect the coefficient a.

3. Generally, (4) will pass by the four boundary points:

$$\left(0, \frac{dkcos(\phi)}{\omega} \pm \left(b\omega - \frac{d}{\omega}\right) k\right) \text{ and } \left(\pm k, k\left(\mp a + \frac{cos(\phi)(d \mp ck)}{\omega}\right)\right). \tag{7}$$

The basic circuit elements can be obtain easily from this equation as follows:

- Resistor: Resistance can be obtained by putting all the coefficients equal to zero except a. Either x or y represents the current or the voltage. Then we have a linear relation between current and voltage representing the resistor.
- Capacitor: Capacitance is the linear relation between voltage and charge. So, by putting $x(t) = i(t)$ and $y(t) = v(t)$, the capacitance is $1/d$ where the other coefficients are zero.
- Inductor: Inductance can be given by putting $x(t) = i(t)$ and $y(t) = v(t)$, then inductance is b when the other coefficients are zero.

Based on (1), we can generate other elements such as memristor with symmetric and asymmetric behavior. Also we can anticipate new behaviors such as inverse memristor.

3 Deduced Memristive Equation

The self-crossing (pinched) hysteresis loop was shown to be a necessary characteristic of all memristive devices. However, (Adhikari et al. 2013) added two more conditions on memristive devices which are (i) starting from some critical frequency, the hysteresis lobe area should decrease monotonically as the excitation frequency increases and (ii) the pinched hysteresis loop should shrink to a single-valued function when the frequency tends to infinity. This means that the lobe area declines with increased frequency. So, any memristor should have these characteristics.

As a special case of (1), a simple equation for the symmetrical and asymmetric double-loop hysteresis behavior can be developed which was introduced in (Elwakil et al. 2013; Radwan and Fouda 2015). This equation has the basic memristor characteristics and is given as follows:

$$y(t) = x(t)\left(a + c\int_0^t x(\tau)d\tau\right) + b\frac{dx(t)}{dt}, \tag{8}$$

where a represents the initial state of the memristor.

This equation represents a symmetric behavior when $b = 0$, so let's discuss the symmetric case first.

3.1 Symmetrical Memristive Model

One of the test bench marks of the memristor it that the pinched hystersis decreases with increasing the applied input frequency. Figure 1 shows the observed double-loop behavior for $a = c = 1$ when $x(t) = cos(\omega t)$ and $\omega = 1$. Note that two cases are plotted in Fig. 1; namely the positive/ negative a and c cases of (8) with $b = 0$ resulting in either a positively inclined loop or a negatively inclined loop, respectively. Two more cases; (a, c) are$(+, -)$ and $(-, +)$ are also possible and lead, respectively, to similar positively inclined and negatively inclined loops. It is clear that for $x(t) = cos(\omega t)$, $\frac{y(t)}{x(t)} = a + \frac{1}{T\omega}sin(\omega t) \in [a - \frac{1}{T\omega}, a + \frac{1}{T\omega}]$. Therefore, $y = ax$ is a symmetry line and the polarity of a determines the quadrant in which the hysteresis loop appears.

The implementation of the double-loop hysteresis could be done using current or voltage signals; when $x(t)$ is represented by a current and $y(t)$ is represented by a voltage the implementation is current-controlled. Alternatively when $y(t)$ is represented by a current and $x(t)$ is represented by a voltage; a voltage-controlled memristive device is obtained. It is worth noting that the authors of (Biolek et al. 2011) have

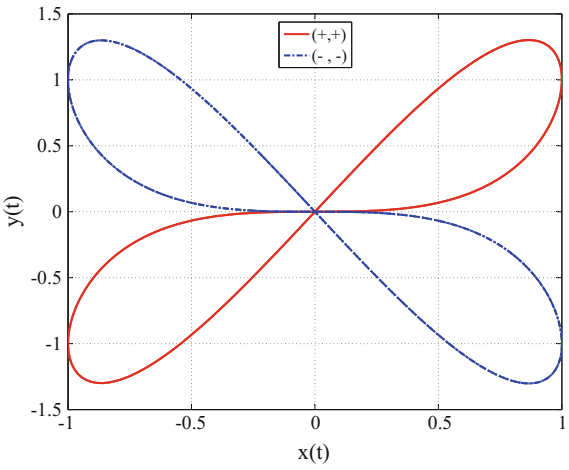

Fig. 1 Double-loop hysteresis for $a = c = 1$ and $x(t) = cos(t)$ in (8)

recently proposed conditions for symmetric pinched hysteresis. The model above satisfies these conditions and is simpler than the one in (Biolek et al. 2011).

3.1.1 Current-Controlled Memristor

Setting $x(t) = \frac{i(t)}{I_{ref}}$, $y(t) = \frac{v(t)}{I_{ref}R_s}$, where I_{ref} is an arbitrary reference current and R_s is an arbitrary resistance, and substituting into (8), the current-controlled memristor equation is given by

$$v(t) = \pm i(t)R_s \pm \frac{i(t)R_s}{TI_{ref}} \int_0^t i(\tau)d\tau = \pm i(t)R_s \pm \frac{i(t)R_s}{TI_{ref}} q(t), \tag{9}$$

and hence the memristance $R_m = v(t)/i(t)$ is given by

$$R_m = \pm R_s \pm \frac{R_s}{TI_{ref}} q(t). \tag{10}$$

It is seen here that R_m is a function of the accumulated current which is essentially the charge $q(t)$; similar to HP modeling equation (Elwakil et al. 2013). In terms of the four different possibilities for R_m, which (a, c) are $(+,+), (+,-), (-,+)$ and $(-,-)$ they respectively represent incremental/decremental R_m and incremental/decremental negative R_m; as demonstrated below.

3.1.2 Voltage-Controlled Memristor

Setting $x(t) = \frac{v(t)}{V_{ref}}$, $y(t) = \frac{i(t)}{V_{ref}G_s}$, where V_{ref} is an arbitrary reference voltage and G_s is an arbitrary transconductance, and substituting into (8), the voltage-controlled memristor equation is given by

$$i(t) = \pm v(t)G_s \pm G_s \frac{v(t)}{TV_{ref}} \int_0^t v(\tau)d\tau = \pm v(t)G_s \pm G_s \frac{v(t)}{TV_{ref}} \varphi(t), \tag{11}$$

and hence the trans-memristance G_m is

$$G_m = \pm G_s \pm \frac{G_s}{TV_{ref}} \varphi(t), \tag{12}$$

where $\varphi(t)$ is the accumulated flux. Similarly, there are four different possibilities representing incremental/decremental G_m and incremental/decremental negative G_m, respectively.

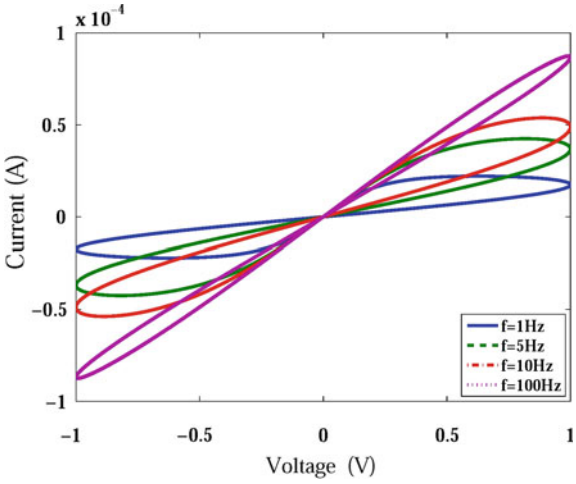

Fig. 2 I-V characteristics of an incremental R_m at different frequencies with $I_{ref} = 1\mu A$ and $R_s = 10\,k\Omega$

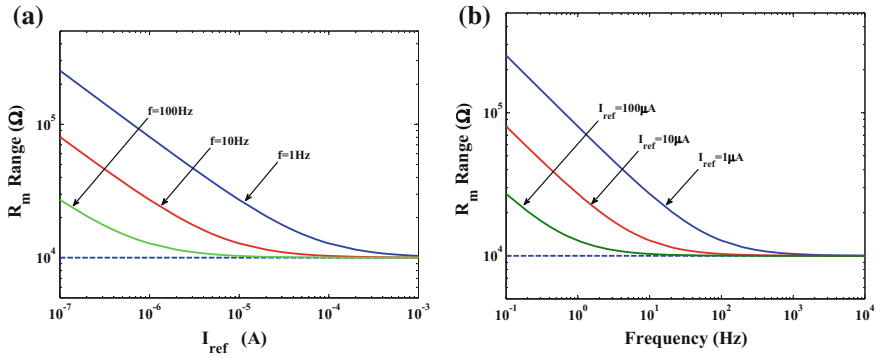

Fig. 3 Maximum and minimum incremental R_m when $R_s = 10\,k\Omega$

Figure 2 shows the I-V characteristics for an incremental R_m for four different frequencies of the sinusoidal input current $i(t)$ with $I_{ref} = 1\mu A$ and $R_s = 10\,k\Omega$. The maximum and minimum values of R_m are shown respectively in Fig. 3; plotted once for the range of I_{ref} spanning from $1\mu A$ to 0.1 mA and another for the frequency range $1-100$ Hz of the input signal. In Fig. 4, the I-V characteristics for an incremental but negative R_m is also shown for four different frequencies of the sinusoidal input current $i(t)$ with $I_{ref} = 1\mu A$ and $R_s = 10\,k\Omega$.

As a proof of concept, different circuit emulators have been introduced based on this model and discussed in detail (Radwan and Fouda 2015).

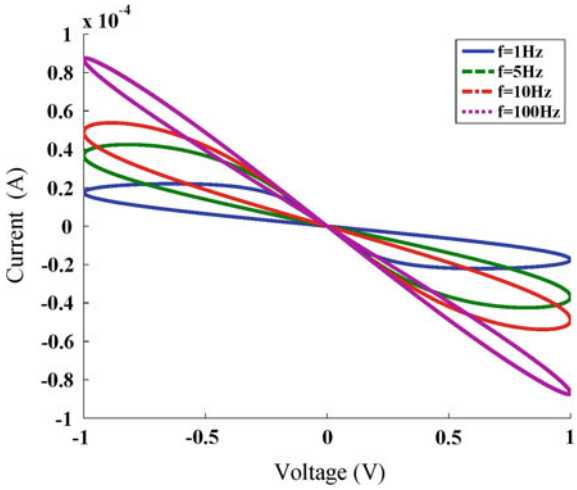

Fig. 4 I-V characteristics of an incremental negative R_m at different frequencies with $I_{ref} = 1\mu A$ and $R_s = 10\,k\Omega$

3.2 Continuous Non-symmetrical Model

Adding the derivative term to the symmetric equation makes the pinched hysteresis asymmetric. If $x(t) = cos(\omega t)$ then (8), with nonzero elements, yields

$$y(t) = ax(t) \mp (b\omega - \frac{c}{\omega}x(t))\sqrt{1 - x^2(t)}. \tag{13}$$

It can be shown that the pinch-off point, which corresponds to the vanishing of the second term of (13), is given by

$$[x_p, y_p] = [\frac{b}{c}\omega^2, (\frac{ab}{c}\omega^2)], \tag{14}$$

where $x_p \leq 1$. Moreover, the generated loop always passes by the three points: $(x, y) = (1, a), (-1, -a)$ and $(x, y) = (0, \pm b\omega)$. Figure 5a shows the observed non-symmetrical loops for different values of a when $b = c = 1$ at $f = 0.1$ Hz. A 3D view of these non-symmetrical loops for different values of c when $a = 0, b = 1$ is shown in Fig.5b while Fig. 5c shows the case when $a = b = 1$; both figures at $f = 0.5$ Hz. Note that if $x_p = \frac{b}{c}\omega^2 > 1$ then there is no pinched point and a single loop is observed.

4 Deduced Inverse Memristive Equation

A simple inverse memristive equation can be deduce from (1) by putting $b = c = 0$ as follows:

$$y = ax + (b + ex)\frac{dx}{dt} \tag{15}$$

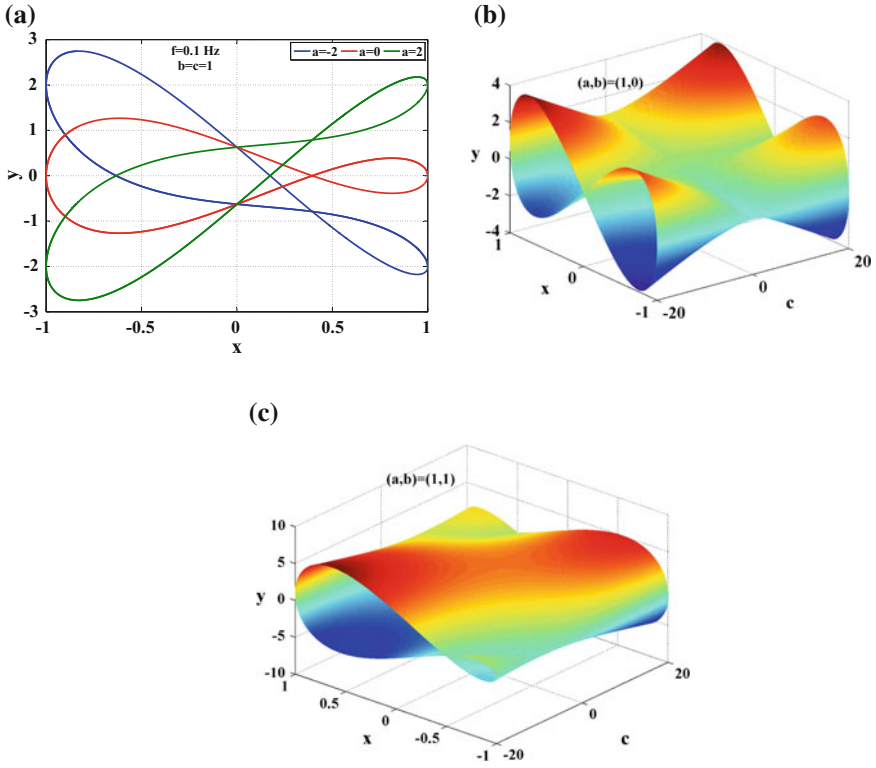

Fig. 5 Non-symmetrical loops when **a** $(b, c) = (1, 1)$, **b** $(a, b) = (0, 1)$, and **c** $(a, b) = (1, 1)$

Under a general sinusoidal excitation where $x(t) = k.sin(\omega t + \varphi)$, and by using trigonometric identities, we obtain

$$y = ax \pm (b + ex)\sqrt{k^2 - x^2} \tag{16}$$

4.1 Inverse Memristor Properties

This equation has the following properties:

1. There exists a line of symmetry given by the first order equation $y = ax$. Evidently, for $a = 0$, the y-axis is the line of symmetry.
2. A pinched double-loop hysteresis behavior is observed in the xy plane. The double-loop intersects itself at a point known as the pinch-point (x_p, y_p) given by

$$(x_p, y_p) = \frac{-b}{e}(1, a) = (0, 0)|_{b=0} \tag{17}$$

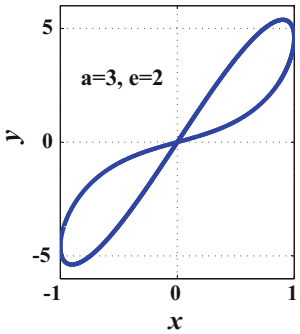

Fig. 6 Pinched hysteresis from (15) when $b = 0$

which is independent of ω. Figure 6 is a plot of the pinched loop for $(a, b, e) = (3, 0, 2)$.

3. The double-loop will always pass by the boundary points: $\omega(0, \pm bk)$ and $k(\pm 1, \mp a)$. For $b = 0$, the first two points coincide with the pinch point $(x_p, y_p) = (0, 0)$.
4. The area inside the two lobes of the pinched hysteresis is given by

$$A = 4\int_0^k \left(\omega(b + ex)\sqrt{k^2 - x^2}\right) dx = 2k^2\left(\pi b + \frac{2}{3}ek\right) \tag{18}$$

Hence, it is clear that A is directly proportional to ω ; i.e. maximizing the hysteresis loop area requires increasing ω. This represents inverse-memristor frequency characteristics since the condition in (Adhikari et al. 2013) implies that for a memristor the lobe area should decrease monotonically as the excitation frequency increases; shrinking to a single valued function when the frequency tends to infinity.

A non-symmetrical-loop may be obtained using (15) and also by adding an integral term in the form. For example, if $b = 0$, then

$$y = ax + ex\frac{dx}{dt} + d\int_0^t x(\tau)d\tau \tag{19}$$

for which the line of symmetry and pinch-point are, respectively, given by

$$y = ax + kd\frac{cos(\varphi)}{\omega} \quad and \quad (x_p, y_p) = \left(\frac{d}{e\omega^2}, \left(\frac{ad}{e\omega^2} + kd\frac{\varphi}{\omega}\right)\right) \tag{20}$$

both of which are frequency dependent. Since $|x_p| < k$, then $|d/e\omega^2| < k$ and therefore the frequency

$$\omega_c = \sqrt{\frac{|d/e|}{k}} \tag{21}$$

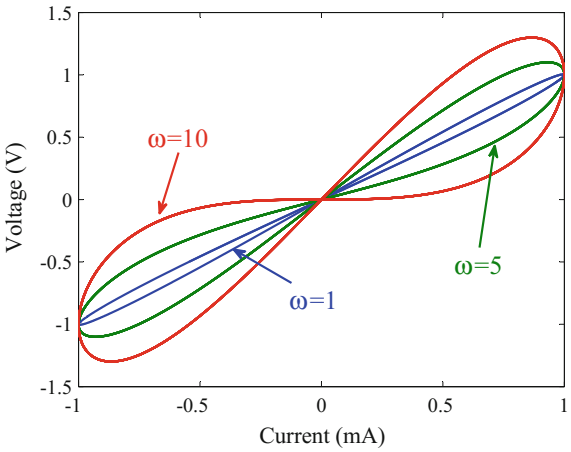

Fig. 7 Pinched hysteresis of an inverse memristor widens as frequency is increased

is the critical frequency at which the non-symmetrical double loop is born. The area of the this double-loop increases for $\omega > \omega_c$. This will be demonstrated further in the experimental results section.

From an electrical circuit point of view, Eq. (15) can represent different types of circuits based on the nature of x and y. Restricting ourselves to the $v(t) - i(t)$ plane, the possible choices of $x(t)$ and $y(t)$ are either a voltage $v(t)$ or a current $i(t)$. When $x(t) = i(t)$ and $y(t) = v(t)$ then (15) can be translated into series connected components. Alternatively, if $x(t) = v(t)$ and $y(t) = i(t)$ then (15) can be translated into parallel connected components as mentioned previously.

It is important to note that in case of $x(t) = i(t)$ and $y(t) = v(t)$, a nonlinear inductor with quadratic current dependence can be obtained where $\int v(i)dt = e/2i^2(t)$ where e has the units of Henry/Ampere and can be termed pseudo-inductance. Note that if $b = 0$, then (15) can be considered to collectively represent single derivative-controlled nonlinear resistor $R_d(i(t))$ where

$$v(t) = \left(a + e\frac{di(t)}{dt}\right).i(t) = R_d.i(t) \tag{22}$$

Figure 7 shows the observed pinched hysteresis loop in this special case for three different frequencies with $a = 1k\Omega, e = 100H/mA, b = 0$ and $k = 1mA$. The values of a, e and k were chosen to obtain a current in mA and a voltage in Volts. Note the widening of the loop as ω is increased since according to (18), $A_{b=0} = \frac{4}{3}ek^3\dot{\omega} \approx \omega/562.5$. In a conventional memristor, the loop area declines as ω is increased. Recall that $\left(\frac{4}{3}ek^3\right)$ represents the energy stored in the device and has the units of $(\mu H \times A^2)$. If we compare this to the expression of the energy stored in an effective inductor $(E_L = 0.5L_{eff}i^2)$, we can calculate the effective inductance $L_{eff} = 267\mu\text{H}$.

In case of $x(t) = v(t)$ and $y(t) = i(t)$, a nonlinear capacitor with quadratic voltage dependence is obtained, where $\int i(t)dt = e/2v^2(t)$ and e has the units of Farad/Volt

and can be termed pseudo-capacitance. Also, if $b = 0$, then (15) can be considered to represent a single derivative-controlled nonlinear transconductor $G_d(v(t))$ where

$$i(t) = \left(a + e\frac{dv(t)}{dt}\right).v(t) = G_d.v(t) \tag{23}$$

The energy stored in this device is also $\left(\frac{4}{3}ek^3\right)$ with the units of $(F \times V^2)$. As expected, this device mimics a capacitor with a stored energy of $(0.5C_{eff}v^2)$ resulting in $C_{eff} = (8e/3)F$. This device will be emulated and experimentally validated in the next subsection.

4.2 Inverse Memristor Circuit Emulator

Due to the lack of solid-state samples, researchers are developing emulation circuits to mimic the behavior of either current-controlled memristors or voltage-controllled memristor (Hussein and Fouda 2013; Radwan and Fouda 2014; Alharbi et al. 2015a, b, c). In (Fouda et al. 2015), a simple emulator circuit for inverse memristor is developed based on (23) where an applied voltage V is differentiated using a floating differentiator circuit and then used to control a voltage-controlled transconductance G_m through its control voltage V_c. Transconductance is implemented using an LM13700 chip where G_m is proportional to a bias voltage V_c given by

$$G_m = \left(0.64V_c + 8.6885\right)\frac{R_A}{R_B} \quad (m\Omega^{-1}) \tag{24}$$

and R_A, R_B are external biasing resistors. If the control voltage V_c is forced to be equal to the derivative of the applied voltage V then G_m in (24) can realize G_d in (23). This is achieved using the circuit shown in Fig. 8 with three op amps (TL084) controlling the bias voltage Vc of the LM13700. Consequently, (23) is realized with $a = 8.6885R_A/R_B(m\Omega^{-1})$ and $e = 064R_A/(R_BRC)(m\Omega^{-1}V^{-1}s)$.

This circuit was experimentally constructed as shown in Fig. 8 after selecting (C, R, R_B, R_A) equal to $(1mF, 10\,k\Omega, 100\,k\Omega, 10\,k\Omega)$. A $0.25V$ input voltage was applied at different frequencies. A current-to-voltage converter with equivalent resistance $56\,k\Omega$ was used to observe the current flowing into the two-terminal device. The observed loop is confirmed to widen as the frequency is increased in the sequence $300, 500, 700$ and $900\,Hz$ as shown in Fig. 9a, b. Further, we verified (19), which indicates that by adding a capacitor in series with G_d, non-symmetrical pinched loops can be obtained. This is shown in Fig. 10 using a $0.047\mu F$ capacitor at $500\,Hz$ and at $700\,Hz$, respectively. Note the widening of lobe area as frequency is increased and using (21), the pinched loop is born at approximately $410\,Hz$.

Figure 11a shows the effect of connecting a $10H$ inductor in parallel with the inverse memristor. It is clear that the pinch point lies in the first quadrant. By

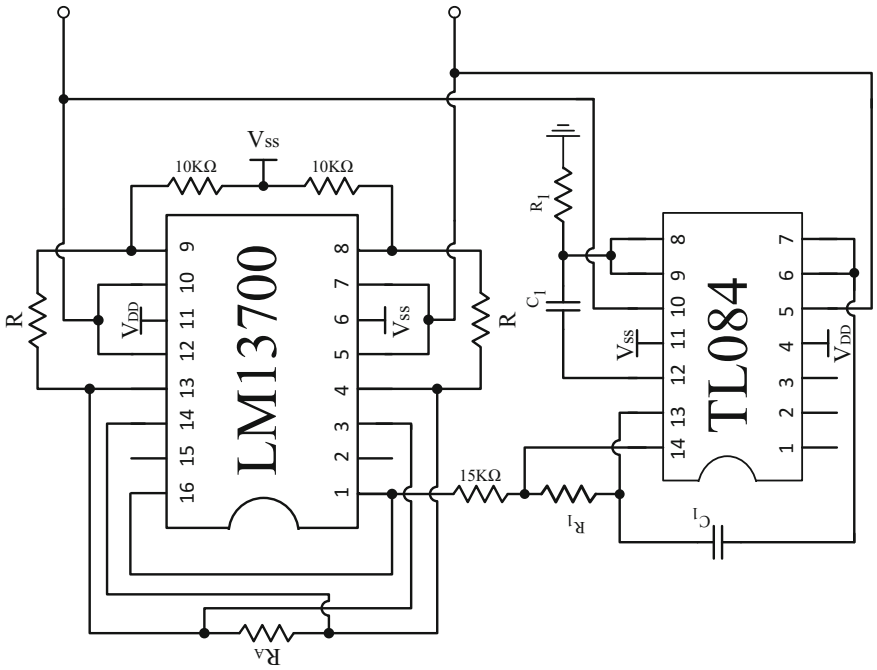

Fig. 8 Emulation circuit of voltage-controlled inverse memristor (Fouda et al. 2015)

increasing the value of the inductance, the pinched point moves up until the loop becomes elliptic without any intersection which means that the inductance dominates the behavior of the circuit. Unlike Fig. 11b where the pinched point lies in the third quadrant, by increasing the capacitance value, the pinch point moves down until it gets out of the boundaries and the loop becomes inclined elliptic where the capacitance behavior dominates the inverse memristor behavior.

5 Circuit Identification

Briefly, from a circuit point of view, (1) can represent two different types of circuits; based on the nature of x and y. When $x(t) = i(t)$ and $y(t) = v(t)$ then (1) can be translated into five series connected impedances, as shown in Fig. 12a. Alternatively, if $x(t) = v(t)$ and $y(t) = i(t)$ then (1) can be translated into five parallel connected admittances, as also shown in Fig. 12b. In Fig. 12a, the five impedances are identified respectively as

- a linear resistance R corresponding to the linear proportional coefficient a in (1) ($R = a$).

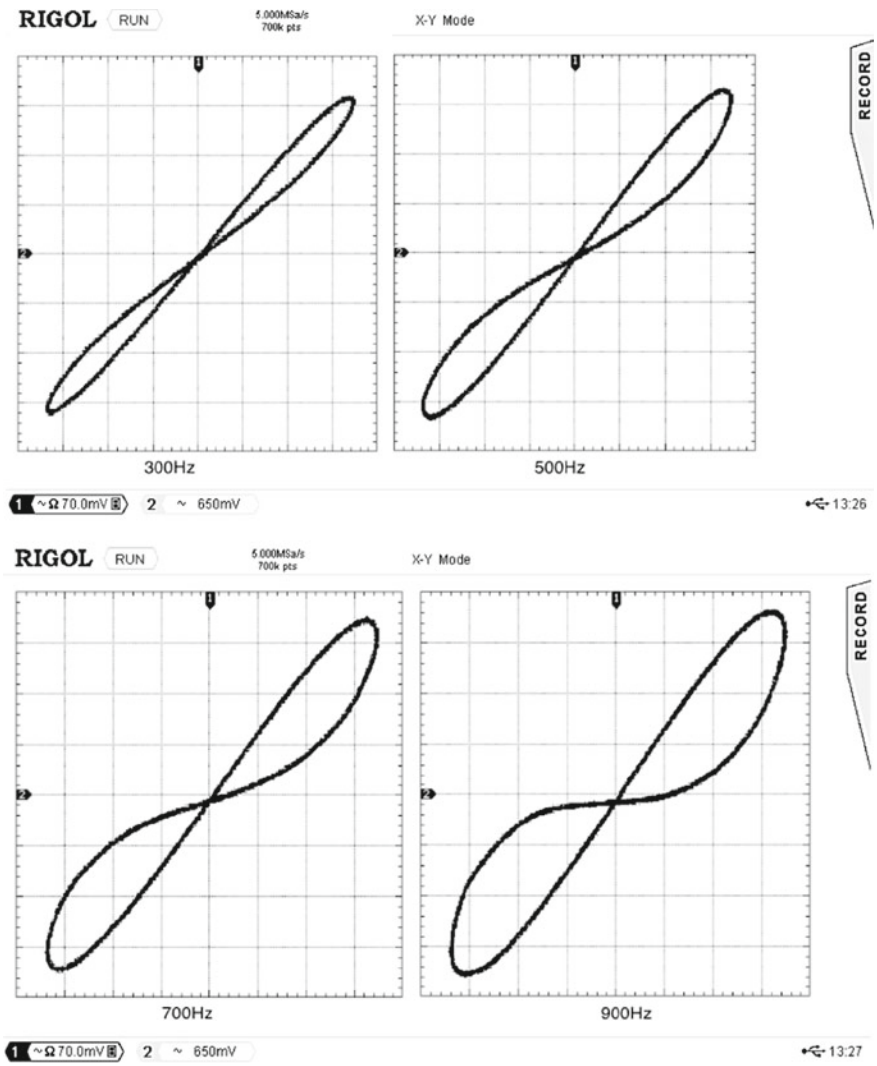

Fig. 9 Experimental verification of the circuit in Fig. 8 at 300, 500, 700 and 900 Hz. X-axis is $v(t)$ and Y-axis is $i(t) \times 56\,\mathrm{k}\Omega$

- a linear inductance L corresponding to the linear derivative coefficient b in (1) ($L = b$).
- a linear capacitance C corresponding to the linear integration coefficient d in (1) ($C = 1/d$).
- a memristor M corresponding to the nonlinear integral term with coefficient c in (1). From (1), $M(q) = c \int i(\tau)d\tau$. Under sinusoidally exciting $i(t)$, the charge $q(t)$

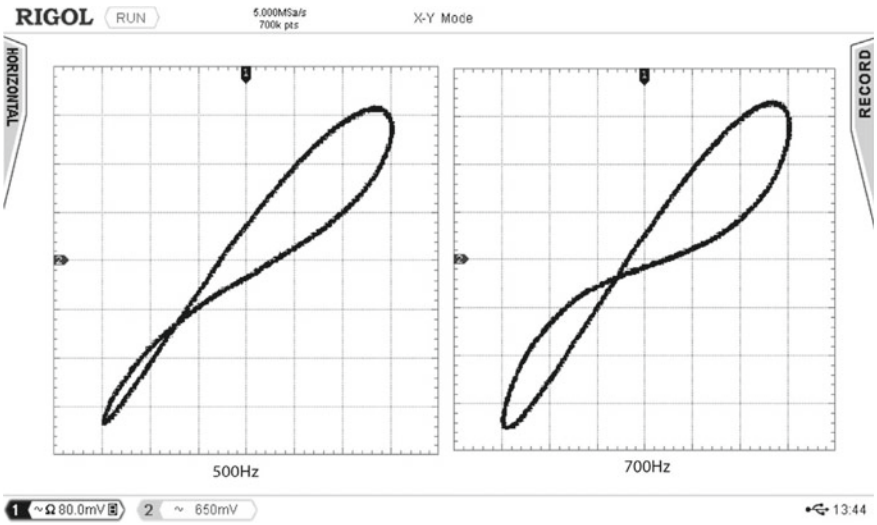

Fig. 10 Experimental results showing non-symmetrical loops at 500 and 700 Hz

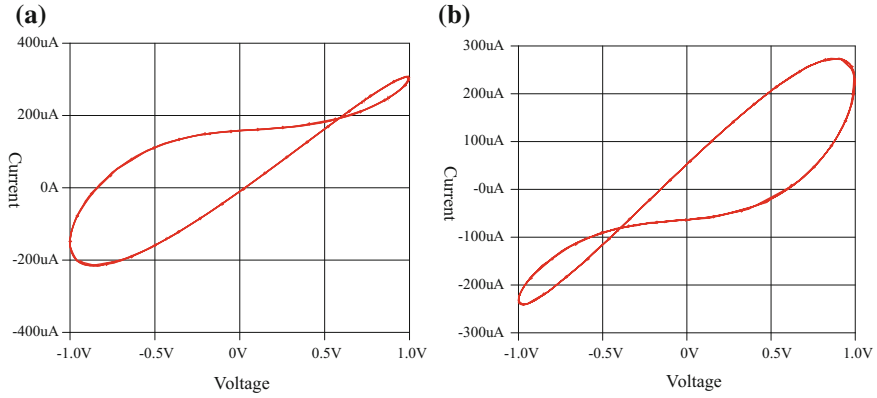

Fig. 11 SPICE simulation of parallel inverse memristor with **a** 10H inductor and **b** 50 nF capacitor

is inversely proportional to the frequency ω and hence the memristance decays with increasing frequency (Adhikari et al. 2013).

- a new element, which we term the inverse memristance $\overline{M}$, corresponding to the nonlinear derivative term with coefficient e in (1). From (1), $\overline{M}(q) = edi(t)/dt$. Under sinusoidal $i(t)$, $\overline{M}$ increases proportional to ω.

All series-connected cases are summarized in Table 1. Similarly, the same five impedances can be transformed into their admittance equivalents in Fig. 12b.

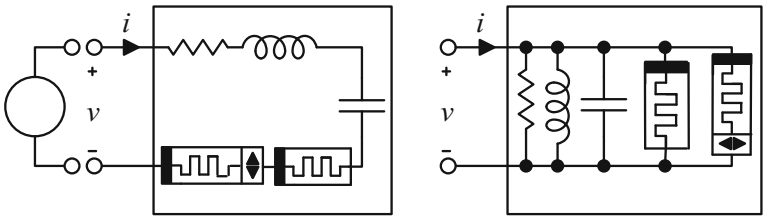

Fig. 12 Series and parallel connections of the five impedances $(R, L, C, M, \overline{M})$

Table 1 A summary of some special cases of the proposed Eq. (1)

Case	(x_p, y_p)	Boundary points	Double-loop
$b = d = e = 0$	$(0, 0)$	$(0, 0)$ $(\pm k, \pm k(a + ck\frac{cos(\phi)}{\omega}))$	$\Delta(\frac{y}{x})_{max} = \frac{ck}{\omega}$
$b = c = d = 0$	$(0, 0)$	$(0, 0)$ $(\pm k, \pm ak)$	$\Delta(\frac{y}{x})_{max} = ek\omega$
$b = d = 0$	$(0, 0)$	$(0, 0)$ $(\pm k, \pm k(a + ck\frac{cos(\phi)}{\omega}))$	$\Delta(\frac{y}{x})_{max} = k(e\omega - \frac{c}{\omega})$
$d = e = 0$	$x_p = \frac{b\omega^2}{c}$ $y_p = ax_p + \frac{kdcos(\phi)}{\omega}$	$(0, \pm kb\omega)$ $(\pm k, \pm k(a + ck\frac{cos(\phi)}{\omega}))$	Non-symmetrical $y \approx (a + \frac{ckcos(\phi)}{\omega})x$
$b = c = 0$	$x_p = \frac{d}{e\omega^2}$ $y_p = ax_p + \frac{kdcos(\phi)}{\omega}$	$(0, \frac{kd}{\omega}(cos(\phi) \pm 1))$ $(\pm k, \pm k(a + ck\frac{cos(\phi)}{\omega}))$	Non-symmetrical $y \approx ax + \frac{kdcos(\phi)}{\omega}$

5.1 Impedance Analysis

Referring to the first row in Table 1 where $a \neq 0$ and $c \neq 0$, while $b = d = e = 0$, (1) then represents a current-controlled memristor M with initial memristance equals $cq(0)$ in series with a resistor a. This connection represents a memristor with memristance $R_m = R_i + cq(t)$ and R_i representing the initial memristance and equals $a - cq(0)$. The pinched hysteresis of this memristor shrinks with increasing frequency and eventually disappears since it can be shown that $\triangle(y/x)_{max} = ck/\omega$. Therefore, maximizing the hysteresis behavior requires minimizing ω.

The second row in Table 1, where $a \neq 0, e \neq 0$ and $b = c = d = 0$ corresponds to the inverse memristor $\overline{M}$. A symmetric pinched hysteresis loop is also observed and is stimulated with increasing the frequency and vanishes as $\omega \to 0$ since it can be shown that $\triangle(y/x)_{max} = ek\omega$. Hence, maximizing the hysteresis loop requires increasing ω.

Row 3 in Table 1 shows the case of a memristor and inverse memristor connected in series; in which case only $b = d = 0$ and $\triangle(y/x)_{max} = k(e\omega - \frac{c}{\omega})$. Note the existence of a critical frequency $\omega_o = \sqrt{c/e}$ at which the hysteresis loop disappears and reduces to a straight line. Higher or lower than this critical frequency, the area of the hysteresis loop increases. This is illustrated in Figs. 13a, b respectively for

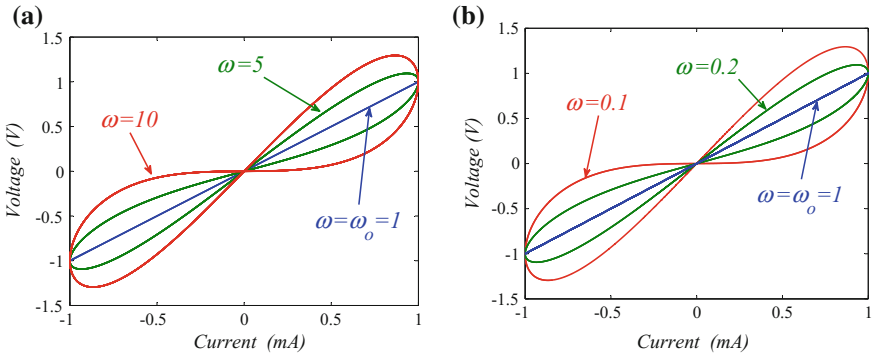

Fig. 13 Behaviour of an $M - \overline{M}$ series connection **a** increasing ω above ω_o and **b** reducing ω below ω_o

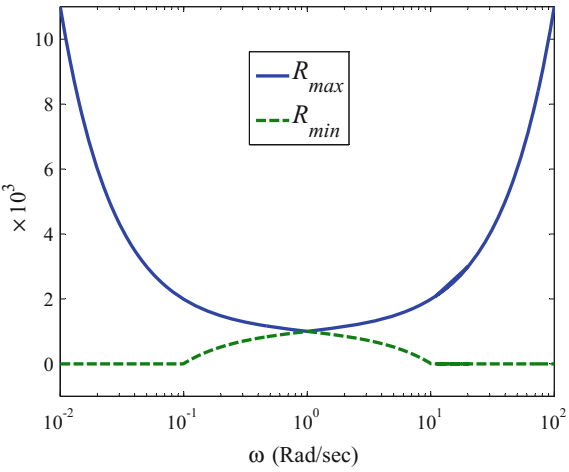

Fig. 14 Maximum and minimum resistances for a series $M - \overline{M}$ connection

$a = 10^3, c = e = 10^5, k = 10^{-3}$ and $\phi = \pi/2$; which yields $\omega_o = 1$. The maximum and minimum resistance (R_{max}, R_{min}) with this series $M - \overline{M}$ connection is shown in Fig. 14.

Adding a reactive element (capacitor or inductor) in series with M or $\overline{M}$ makes the hysteresis loops asymmetric. Figure 5 shows the effect of varying a when $b = c = 1$ and $\omega = 0.2\pi$ on the case represented in row 4 of Table 1. This case corresponds to an inductor in series with a memristor (series $L - M$). Note that all loops in Fig. 15 are asymmetric but with the same pinch point. Finally, the case in row 5 of Table 1 is that of a capacitor in series with a memristor (series $C - M$). Table 2 represents a summary of the complex impedances that can be obtained from (1) along with their circuit representations.

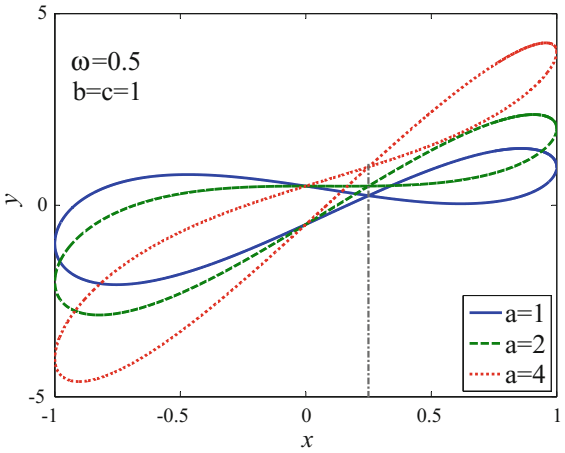

Fig. 15 Asymmetric double-loop hysteresis corresponding to row 4 of Table 1 (an inductor in series with a memristor) for variable *a*

Table 2 Impedances from (1)

Non-zero	Element(s)	Circuit Model
a	*R*	
b	*L*	
d	*C*	
a, *b*	*RL*	
a, *d*	*RC*	
a, *b d*	*RLC*	
a, *c*	*M*	
a, *e*	$\overline{M}$	
a, *b*, *c*	*ML*	
a, *c*, *d*	*MC*	
a, *b*, *c*, *d*	*MLC*	
a, *b*, *e*	$\overline{M}L$	
a, *b*, *d*, *e*	$\overline{M}LC$	
a, *b*, , *c*, *d*, *e*	$M\overline{M}LC$	

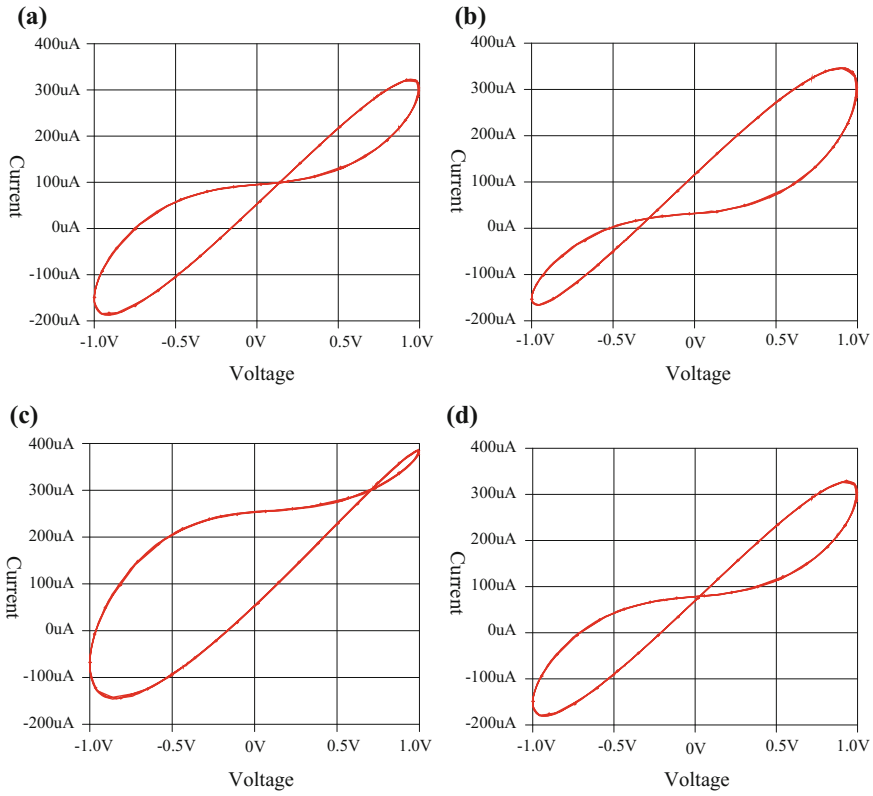

Fig. 16 SPICE simulation of parallel inverse memristor with parallel LC

5.2 Admittance Analysis

By setting $y = i(t)$ and $x = v(t)$, (1) reads as

$$i(t) = [a + c\int_0^t v(\tau)d\tau + e\frac{dv}{dt}]v(t) + b\frac{dv}{dt} + d\int_0^t v(\tau)d\tau \tag{25}$$

where the coefficient a has transconductance unit (℧), b has capacitance unit (F), d has inverse inductance unit (H^{-1}), c has unit $(sec \cdot V \cdot \Omega)^{-1}$, and e has the unit of $(sec/V \cdot \Omega)$. Similar to the impedance formation, different complex admittance can be obtained. For example, when $a \neq 0, c \neq 0$ and $b = d = e = 0$, the previous equation represents a voltage-controlled memristor with initial memductance equal to $a - c\phi(0)$. While when $a \neq 0, e \neq 0$ and $b = c = d = 0$, it represents a voltage-controlled inverse memristor. It is straightforward to build a table similar to Table 2 for all cases.

In case of connecting parallel $\overline{M}$LC circuit, the hysteresis loop can be either pinched or not depending on the values of b and d. The hysteresis would be pinched with double loops if $|x_p| < A$ where A is the input voltage amplitude and single loop for $|x_p| > A$. The pinch point can be in the first or the third quadrant depending on the values of b and d where for $\omega < \sqrt{\frac{d}{b}}$, the pinch point lies in the first quadrant and vice versa. Figure 16 is plotted by applying $v(t) = sin(400\pi t)$ where Fig. 16a, b showing the effect of changing the parallel capacitance 50 nF and 100 nF at $L = 10$ H. However, Fig. 16c, d show the effect of changing the parallel inductance from 10 H and 5 H at $C = 50$ nF. At the parallel resonance $\omega_o = \sqrt{\frac{1}{LC}}$, the coordinates of the pinch point is $(0, \frac{1}{L\omega})$ at $\omega = 400\pi, L = 10$ H and $C = 63.357$ nF.

6 Conclusion

In this chapter, A mathematical model to represent all the linear elements has been discussed. Different special cases have been introduced and verified using numerical, and circuit simulations. As we discussed, the statement "if it is pinched, it is memristor" is not valid anymore since we proved that inverse memristor has pinched hysteresis but it has the opposite behavior. Also the inverse memristor can be obtained by a nonlinear capacitor or nonlinear inductor. Connecting any reactive element to ideal symmetric pinched device gives asymmetric behavior. Thus, the asymmetric pinched devices can be modeled as symmetric devices with a reactive element. Moreover, according to the discussion, the series and parallel connection of the conventional elements in addition to the memristor and inverse memristor especially memristor-inverse memristor connection give new properties. These properties are new to the circuit theory.

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