Memristive-Based Neuromorphic Applications and Associative Memories

C. Dias, J. Ventura and P. Aguiar

Abstract The recent realization of memristors opened the possibility to fabricate novel neuromorphic computational systems, including highly scalable and low power artificial neural networks. In fact, it has been shown that memristors can be used as an artificial synapse or to build the spiking core of an artificial neuron. The high resemblance between memristor and synaptic dynamics offers exciting possibilities in two major research fields: on one hand, memristors can be used to advance our understanding of the human brain, by supporting very-large-scale integration (VLSI) models where experiments can be performed and hypothesis tested in an in silico testbed. On the other hand, memristors have the potential to support novel advances in computing by providing the building blocks to bio-inspired computing paradigms, alternative to the von Neumann architecture, where storage and processing are supported by the same substrate. This chapter reviews the neuromorphic properties of memristors, comparing them with the key players of neuronal computations, synapses and neurons. The presentation is extended to more complex systems, where multiple computing units are combined in networks to achieve more elaborated dynamics. Emphasis is given to memristive-based associative memories, a bio-inspired content addressable memory system which relevant properties such as distributed storage and noise correction.

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1 Introduction

Building computers capable of learning and adapting to new environments has for long been an aspiration of the scientific community and is an essential step towards the realization of artificial intelligence. Modern-day computers, based on the deterministic von Neumann architecture, where memory and processing are physically separated, cannot accomplish this goal in an efficient and practical way. A novel approach is thus necessary and there is no better model than the human brain itself. The brain relies on a non-deterministic approach with massive parallelism of simple processing units—neurons—which take the role of essential building blocks in learning and decision-making. This distributed computing results in a significant power efficiency, adaptation and resilience to unit failure, all of which might be the keys to the creation of intelligent machines.

The communication between neurons is established by synapses and it is well known that synaptic strength is used to store information in brains. Learning is accomplished by modifying (either increasing or decreasing) this strength through a mechanism called synaptic plasticity. Emulating the biological synapse in an electronic circuit is the biggest challenge to the fabrication of a neuromorphic (brain-like) system. Fortunately this is now closer to becoming a reality, with the recent realization of memristors (Chua 1971; Strukov et al. 2008), a device with properties resembling those of biological synapses.

The memristor is a non-volatile two-terminal device, a metal-insulator-metal structure, characterized by a nonlinear relationship between the histories of current and voltage. Its response to a periodic voltage (or current) input is a "pinched hysteretic loop". The dynamic resistance and nanosized of memristors make them exciting candidates for electronic synapse applications and have inspired the neuromorphic community to explore their potential for building low-power intelligent machines. Noteworthy, different experimentally verified synaptic learning rules, such as spike timing dependent plasticity (STDP), have been faithfully reproduced in memristive devices.

Similar to what happens in biology with synaptically connected neural networks, synthetic memristive-based neural networks can be developed for purposes of machine learning and cognitive science. The presence of memristors allow these synthetic networks to be trained and to learn how to perform complex computations such as pattern recognition. One particular type of network architectures with computational interest is associative memory networks. These networks have the ability to store (learn) and recall (remember) associations between unrelated data items. Importantly, they work as content-addressable memories, where pairs of input/output patterns are stored in such a way that, if the input is presented, the output is readily given. Moreover, associative memory networks have robustness to

noise: the system is able to recall the correct output pattern even if the presented input is a partial/noisy version of the original pattern (learnt during storage phase). The memristor fast speed, adaptive properties and small size meet the necessary specifications for these type of applications. Thereupon, memristor technology has the potential to revolutionize computing and scientific research in the coming decades.

The rest of the chapter is organized as follows. The next Sect. 2 provides a brief introduction to the key neurobiological mechanisms supporting information processing and information storage. Section 3 discusses the neuromorphic properties of memristors and their ability to mimic fundamental computational properties from single neurons and synapses. Then, Sect. 4 extends the discussion to the network level, where more complex computational capabilities can be achieved by combining a large number of memristive-based units. Section 5 is dedicated to a particularly relevant network architecture, the content-addressable associative memories. Finally, Sect. 6 outlines the conclusions of this chapter and discusses some of the open challenges for memristive-based neuromorphic computations.

2 Neural Computation

2.1 Brain Architecture and Operation

Two fundamental units of the human brain, the neuron and the synapse (Fig. 1), play essential roles in learning and memory formation. Neurons are electrically excitable cells which are able to respond to stimuli, to conduct impulses, and to communicate with each other. Synapses are specialized junctions between neurons that allow the rapid transmission of electrical and chemical signals so that neurons can communicate with each other (Shi et al. 2011). When an action potential generated by a neuron reaches a pre-synaptic terminal, a cascade of events leads to the release of neurotransmitters that give rise to a flow of ionic currents into or out of the post-synaptic neuron. The magnitude of these currents are subject to modulation—driven by synaptic plasticity mechanisms—allowing learning in the neuronal circuits. The amplitude or strength of a synapse is usually described as *synaptic weight*.

Figure 1 illustrates the basic structure of neurons and of their connection by synapses. The pre-synaptic neuron sends an action potential through one of its axons to the synaptic junction producing a response in the post-synaptic neuron. Action potentials, commonly named *spikes*, are fast (stereotyped) depolarizations in the neuron's membrane electrical potential which propagate, without attenuation, through axons. At rest, the membrane potential is close to −70 mV (and the membrane is said to be polarized; the reference is the extracellular space), and during a spike the membrane potential may be close to +30 mV (giving an amplitude of roughly 100 mV).

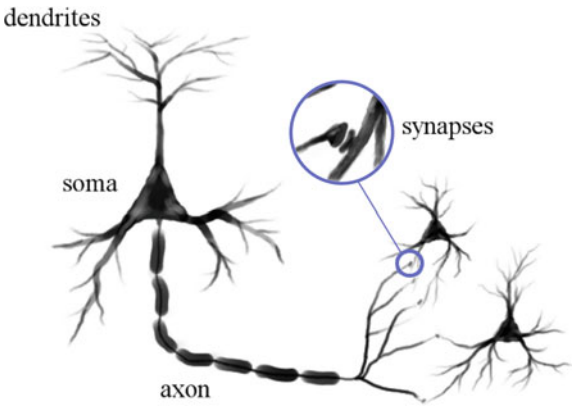

Fig. 1 Structure of a neuron showing the cell body, dendrites and synapses

2.2 Learning and Memory

Learning and memory are the capabilities to gain new information and store it in a recallable way. Although alternative mechanisms to store information have been studied (Conde-Sousa and Aguiar 2013), the current dogma in neuroscience is that information in the human brain is mostly stored in the synaptic strength (weight), with learning being accomplished by modifying (either increasing or decreasing) this strength. Synaptic plasticity makes it then possible to store information and to react to inputs based on past knowledge (Kandel et al. 2003).

2.2.1 Hebbian Learning

Conditions which are consistently experienced together tend to become associated. As a consequence, future exposure to one of the conditions automatically activates the response to the second condition (Kandel et al. 2003). One of the most famous experiments related to associative memory is Pavlov's experiment on classical conditioning. In this experiment, salivation of a dog is first set by the sight of food. Then, if the sight of food is accompanied by a sound (bell) over a certain period of time, the dog learns to associate the sound to the food, and salivation can start to be triggered by the sound alone (Kozma et al. 2012). In 1949, D. Hebb addressed this learning postulate at the neural level: "neurons that fire together, wire together" (Shi et al. 2011). Thus, when two connected neurons are active at the same time, the weight of the connecting synapse increases to reinforce that correlation. This learning rule, however, is incomplete since it provides a rule for increasing synaptic weight but not for decreasing it; also it does not specify the effective time window between pre- and post-synaptic activity that will result in potentiation.

2.2.2 Spike Timing Dependent Plasticity

Spike timing dependent plasticity (STDP) is an experimentally verified biological phenomenon in which the precise timing of spikes affects the sign and magnitude of changes in synaptic strength. STDP contains two distinct plasticity windows defining long-term potentiation (LTP) and long-term depression (LTD). In the former, synapses increase their efficiency as a pre-neuron is activated shortly (in the order of milliseconds) before a post-neuron; in the latter synapses decrease their efficiency as a post-neuron is activated shortly before a pre-neuron (Seo et al. 2011). While the association rule produced by Hebbian learning can be seen as supporting a correlation measure, STDP goes a step further in complexity by providing a (temporal) causality measure. As depicted in Fig. 2, the interspike interval between action potentials in the pre- and post-synaptic cells modulates STDP. The smaller the timing difference between pre- and post-synaptic spikes, the larger will be the induced plasticity change in either LTP or LTD. On the other hand, longer intervals (above 50 ms) produce little or no change in synaptic strength (Choi et al. 2011; Karmarkar and Buonomano 2002). This shows the existence of a causality window within the events and that, outside this causality temporal window, no changes are produced. The relative synaptic conductance change $\Delta G = (G_{after} - G_{before})/G_{before}$ [where G_{before} (G_{after}) is the conductance before (after) the pre- and post-spike pair], has a range of [0, +1[for potentiation and [1, 0] for depression (Choi et al. 2011; Yu et al. 2011). Another reason for the importance of STDP relies on the fact that it addresses both questions left open by Hebb: it establishes a critical time window in which pre- and

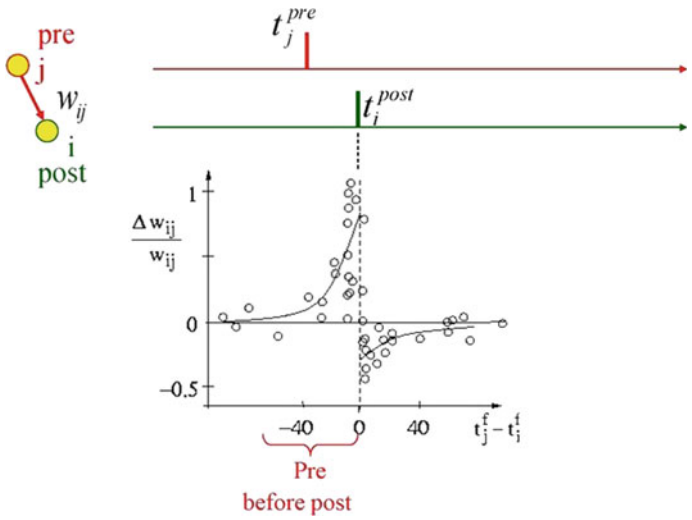

Fig. 2 STDP diagram showing the relative change in synaptic connection as a function of the time between pre- (t_j) and post-synaptic spikes (t_i) (Courtesy of *Scholarpedia Copyright* Owner © Wulfram Gerstner)

post-synaptic activity must occur to produce long-term changes in synaptic strength, and it provides a simple learning rule that decreases synaptic strength.

2.2.3 Short- and Long-Term Plasticity

The synaptic plasticity mechanisms in the human brain are diverse and occur at different time scales. Important computing properties can be achieved with synaptic modifications which are lost not long after the onset conditions. Therefore, in addition to long-term potentiation/depression (LTP/D) mechanisms, neurons also exhibit short-term potentiation/depression (STP/D). Short-term plasticity is mostly a modulation of the release probability of the pre-synaptic vesicles. As opposed to most synapses in the peripheral nervous system, which are deterministic, many types of synapses in the central nervous system are probabilistic: upon the arrival of an action potential at the synapse there is a probability p that a signal will be carried to the post-synaptic neuron. This stochasticity has deep implications in learning and optimization, especially because this release probability is modulated by short-term plasticity rules: a progressive, but temporary increase in p (increase in vesicle availability) is associated with STP, whereas a progressive decrease in p (depletion of the vesicles' pool) is associated with STD. In either cases, the changes in the release probability p are temporary, decaying to its initial state in scales of seconds to minutes. However, in situations where there is a strong consistency in the stimulation pattern, a different plasticity mechanism can be triggered (involving modifications in both in pre- and post-synaptic sites) and long-term changes can be produced, lasting from hours to days, and even beyond (lasting a lifetime). For example, repeated stimulation can cause a permanent change in the synaptic connection to reach LTP and shorter repetition intervals enable efficient LTP formation from fewer stimuli (Wang et al. 2012; Hasegawa et al. 2012; Ohno et al. 2011). On the other hand, consistent low frequency stimulation can lead to LTD. Note however that it is erroneous to associate S/LTP to learning and S/LTD to forgetting—information storage and memory formation in the nervous system involves plasticity in both directions (just as forgetting).

3 Neuromorphic Properties of Memristors

3.1 Memristive Synapses and Bio-inspired Learning Rules

3.1.1 Spike Timing Dependent Plasticity

Since the first proposals that resistive switching structures could mimic relevant properties of biological synapses, including spike timing dependent plasticity, short- and long-term potentiation/depression (Hu et al. 2013a, b; Snider 2008;

Kim et al. 2012a, b) and their integration in hybrid memristor-CMOS neuromorphic circuits (Indiveri et al. 2013), there has been a tremendous effort in experimentally demonstrating learning rules in these novel devices. To relate memristance to traditional biological spike timing dependent plasticity, one requires a voltage/flux controlled bipolar memristor with voltage threshold (below which no variation of the resistance is observed) and an exponential behavior beyond threshold (above which a continuous increment/decrement of the resistance takes place). It was also found that the strength of STDP learning in memristors (i.e. the induced conductance change) can be modulated by the amplitude or shape of the electric spikes. This means that the conductivity can be tuned depending on the precise timing between the pre- and post-synaptic spikes and the learning window by changing the shape of the pulses (Zamarreño-Ramos et al. 2011). Different STDP learning rules can also be obtained depending on the physical origin of resistance switching (Serrano-Gotarredona et al. 2013). For filamentary switching, where the memristor's conductance varies due to the formation and rupture of metallic filaments within the oxide, one expects a quadratic STDP learning rule, in which the synaptic strength update is proportional to the square of the synaptic strength. On the other hand, in interfacial or *domain wall* switching, related with uniform variations in the conductance of the oxide, the synaptic strength update is independent of the memristor's conductance (additive STDP update rule). Recently, a SPICE model able to account for STDP and synaptic dynamics in memristors was also implemented (Li et al. 2015).

Jo et al. were the first to demonstrate STDP in nanoscale memristors (Jo et al. 2010). Their crossbar memristive structure consisted in bottom tungsten and top chrome/platinum nanowire electrodes and a co-sputtered Ag and Si active layer in which the Ag/Si ratio varied along the depth (Fig. 3a). The authors then showed that the sample's conductance continuously increased (decreased) during the positive (negative) voltage sweeps, and that the current-voltage (I-V) slope of each subsequent sweep picks up where the last sweep left of (Fig. 3b). Instead of the usual abrupt, two level switching, in the co-sputtered memristor, the applied bias led to analog switching in which there is a continuous motion of the conduction front (Ag ions moving from the Ag-rich region to the Ag-poor region or vice-verse). This allowed the first demonstration of STDP in a memresistive structure. Figure 3c shows the change in the conductance (synaptic weight) of the memristor synapse as a function of the timing difference (Δt) between spikes arising from pre-synaptic and post-synaptic CMOS integrate-and-fire neurons. When the pre-synaptic neuron spikes before the post-synaptic neuron, the memristor conductance increases (potentiation behavior). The opposite (depressing behavior) is observed when the post-synaptic neuron spikes before the pre-synaptic neuron. Furthermore, the smaller the timing difference between the pulses, the larger is the change in the memristor conductance. Both these characteristics follow extremely well the STDP function of biological synapses, as can be seen in Fig. 2.

Since then, synaptic behavior was observed in several memristive structures, including in TiO_{2-x}/TiO_y bilayer systems showing multilevel conductance due to the movement of oxygen between the TiO_{2-x} and TiO_y layers (Seo et al. 2011),

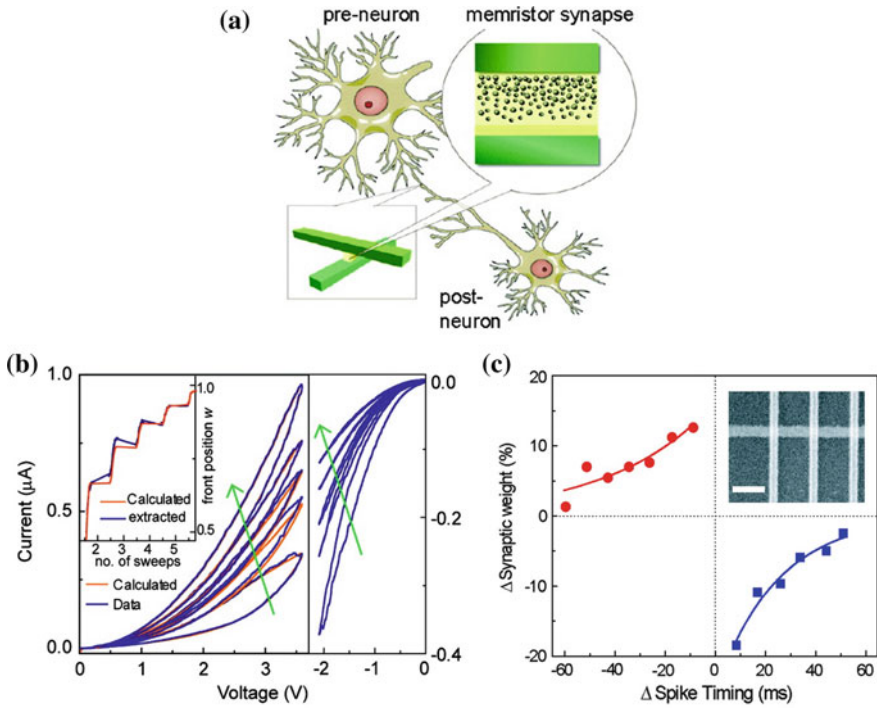

Fig. 3 **a** Schematics of the structure of the fabricated memristor with a gradient of Ag concentration. **b** Measured (*blue*) and calculated (*orange*) I-V characteristics and **c** corresponding memristor synaptic weight as a function of the relative timing of the neuron spikes. *Inset* SEM image of the crossbar array (scale: 300 nm; Reprinted with permission from (Jo et al. 2010). Copyright 2010 American Chemical Society)

$PrCaMnO_3$-based memristors, in which the fabrication of a 1 kbit synaptic array allowed to confirm the possibility to build a neuromorphic system for pattern recognition (Park et al. 2012), asymmetric memristors showing single-sided hysteresis (Williamson et al. 2013), Ag/conducting polymer/Ta memristive systems (Li et al. 2013), volatile and nonvolatile rectification in WO_{3-x}-based nanoionic devices (Yang et al. 2012), Ni-doped graphene oxide (Pinto et al. 2012), nanoparticle organic memory field-effect transistors (Alibart et al. 2012) or exploring multilevel switching in metal oxide memories (Yu et al. 2011).

Choi et al. fabricated Pt/Cu_2O/W metal-insulator-metal (MIM) structures and experimentally demonstrated the successful storing of biological synaptic weight variations (Choi et al. 2011). They also showed the reliability of plasticity by varying the amplitude and pulse-width of the input voltage signal, matching their results with biological plasticity. A practical issue before the industrial implementation of memristors in actual large-scale neural networks is the dependence of the change of the memristive synaptic weight on its initial conductance. Nevertheless, experiments carried out with Pt/Al_2O_3/TiO_{2-x}/Ti/Pt memristors in a

12 × 12 crossbar array, were able to demonstrate STDP behavior with self-adaptation of the average memristor conductance, making plasticity insensitive to the initial conductance state of the devices (Prezioso et al. 2016).

The implementation of STDP was also achieved in a second-order memristor (Kim et al. 2015). Kim et al. showed that the dynamics of $Pd/Ta_2O_{5-x}/TaO_y/Pd$ structures could be well explained considering two sets of state-variables. The first-order state-variable is related with the size of the conduction filament region (w) due to the diffusion of oxygen vacancies that sets the memristor conductance, while the second-order state-variable is the local temperature of the device that changes the dynamics of the diffusion process (Fig. 4a). The characteristic short times of temperature dynamics give rise to an internal timing mechanism and the possibility to affect w by providing close enough pulsed stimuli that device

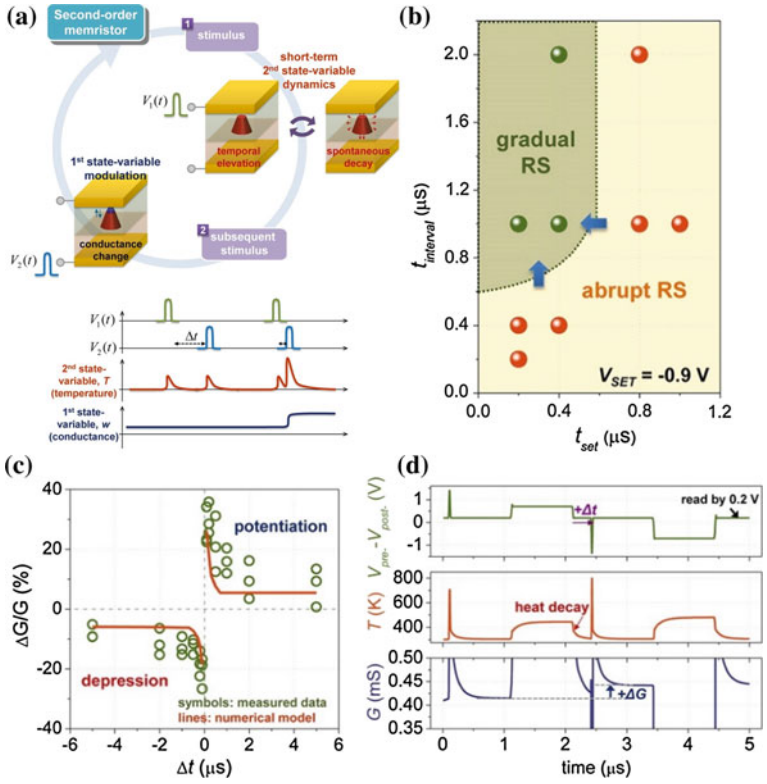

Fig. 4 **a** Operation principles of a second-order memristor in which the modulation of the 2nd-order state-variable (temperature) can trigger changes in the 1st-order state-variable (electrical conductance). **b** The obtained t_{Set} versus $t_{interval}$ operating window for gradual/abrupt resistive switching. **c** Observation of spike-timing dependent plasticity in a second-order memristor (measurements—*symbols* and simulation—*solid lines*). **d** Simulations on the evolution of the internal temperature of a second-order memristor when stimulated by two consecutive spikes (Reprinted with permission from (Kim et al. 2015). Copyright 2015 American Chemical Society)

temperature is still above its steady state value when the second pulse is triggered. This is closer to the case of biological than the first-order memristor, as in biological synapses the weight is also not directly modulated by the spikes, but rather by secondary state-variable(s) such as the postsynaptic calcium ion (Ca^{2+}) concentration. By providing a set of pulses to the fabricated structures, the authors determined the conditions (Set pulse duration t_{Set} and time interval between pulses, $t_{interval}$) for which the conductance showed a gradual variation which enables plasticity (Fig. 4b). Long pulses (>800 ns) always led to abrupt switching because of the large amount of generated heat. The same was observed for sets of short Set pulses at low $t_{interval}$ due to the accumulation of heat that fastens filament growth and thus leads to abrupt switching. However, for sufficiently large $t_{interval}$ and small t_{Set}, the heat generated by each pulse is dissipated before the next one arrives and intermediate states can be obtained (gradual switching occurs). This allowed the observation of frequency-dependent weight changes and STDP using non-overlapping input spikes with a biorealistic implementation (Fig. 4c). The input consisted in a long, low voltage heating pulse which resulted in a significant temperature increase, but no change in conductance and a short, high voltage programming pulse. Although each pulse could not change the memristor conductance by itself, the rise in temperature caused by the first pulse enhanced the effect of the second (Fig. 4d), so that STDP could be obtained.

Another second-order memristor implementation considered as state variables the area of the conducting filament between the two electrodes and the mobility of oxygen vacancies that was found to increase when a stimulation pulse was applied (Du et al. 2015). This allowed the observation of different synaptic behaviors such as spike timing dependent plasticity, paired-pulse facilitation or experience dependent plasticity.

STDP was also replicated in a purely electronic Ti/ZnO/Pt memristor (Pan et al. 2016). In this case, regulation of the current compliance during Set and maximum applied voltage during Reset allowed tuning the carrier trapping/detrapping level and thus the sample's conductance. Resistive switching based on homogeneous barrier modulation induced by oxygen ion migration was also shown to lead to neuromorphic properties (Wang et al. 2015). In fact, it was found that the resistance of $Ta/TaO_x/TiO_2/Ti$ structures could be modulated by the migration of O_2^- towards the TaO_x layer under negative bias (Reset) and towards the Ta/TaO_x interface under positive bias (Set). This allowed measuring and modelling spike timing dependent plasticity related with non-filamentary O_2^- evolution during potentiation and depression. Paired-pulse facilitation (PPF), a form of biological short-term synaptic plasticity in which synaptic weight changes are correlated with the time interval between two consecutive potentiating pulses (Fig. 5a) was also observed in these $Ta/TaO_x/TiO_2/Ti$ structures. The paired-pulse facilitation ratio was calculated using:

$$PPF = \frac{(G_2 - G_1)}{G_1} = C_1 e^{-t/\tau_1} + C_2 e^{-t/\tau_2}, \quad (1)$$

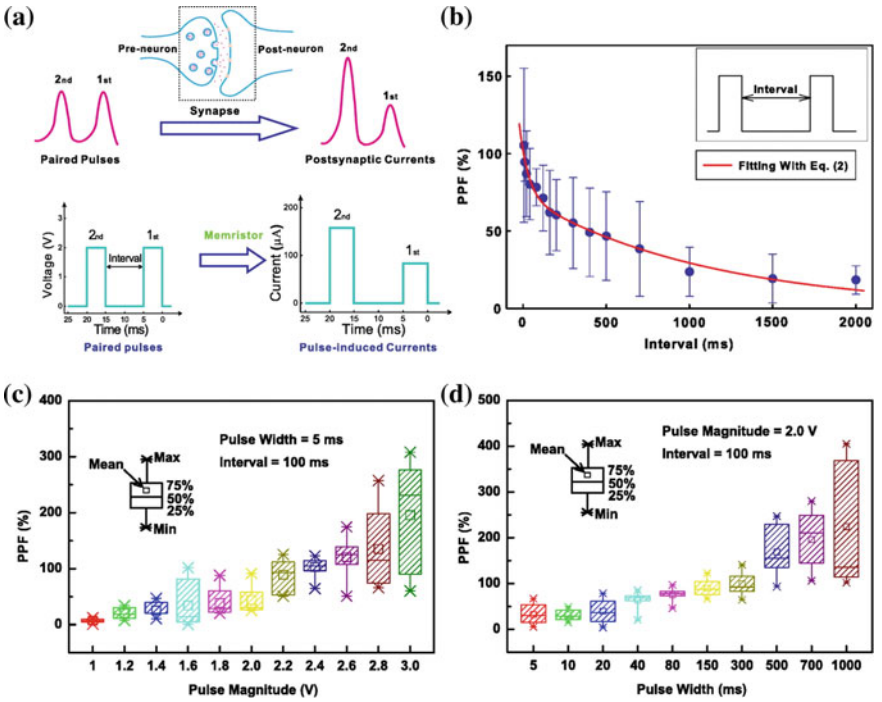

Fig. 5 Paired-pulse facilitation of **a** a biological synapse (*top*) and a NiO_x-based memristor (*bottom*). Dependence of the paired-pulse facilitation [Eq. (2)] of the memristor on **b** the pulse interval (for a pulse magnitude and width of 1.8 V and 5 ms), **c** pulse magnitude (for a pulse width and interval of 5 ms and 100 ms), and **d** pulse width (for a pulse magnitude and interval of 2.0 V and 100 ms; Reprinted from (Hu et al. 2013a, b), with the permission of AIP Publishing)

where G_1 and G_2 are the sample's conductance after the first and second pulses, respectively and C_1, C_2, τ_1 and τ_2 are fitting constants. The values obtained for the fast ($\tau_1 = 45$ ms) and slow ($\tau_2 = 800$ ms) time constants are in good agreement with those found in biological synapses. The emulation of biological PPF was also achieved in NiO_x-based memristors (Hu et al. 2013a, b). As in biological synapses, the change in the memristor's conductance induced by the second pulse is enhanced when compared with that of the first one (Fig. 5a). Again, the PPF magnitude decreases as the interval between the two pulses increases (Fig. 5b), going from 105.4% for 5 ms to 18.3% for 2000 ms. PPF also depended on the magnitude and width of the pulse pair (Fig. 5c, d). With both increasing pulse magnitude (from 1 to 3 V) and width (from 5 to 1000 ms) the average PPF value was also found to increase. These results were explained by the formation of conductive filaments of metallic Ni phases whose number or size increased with the application of the second pulse. However, the effect of the first pulse somehow fades away gradually, as the conductance change induced by the second pulse decreases with the pulse interval. Higher pulse voltages or longer pulses could also lead to the formation of more filaments or the growth of existing ones.

3.1.2 Short- and Long-Term Memory

Short-term memory (STM) and long-term memory (LTM), and the transition from STM to LTM through repetitions (rehearsal), have also been recreated in memristive devices. While STM can only be sustained by constantly rehearsing the same stimulus, LTM, despite the presence of natural forgetting, can be maintained for a longer period without follow-up stimuli (Fig. 6a). The terms short-term plasticity (STP) and long-term plasticity (LTP) are used in neuroscience, whereas STM and LTM are used to describe psychological phenomena (Ohno et al. 2011); plasticity is typically used in the context of localized changes (e.g. a synapse) and memory typically refers to system level changes (e.g. a neuronal population).

Depending on the input voltage pulses, different memorization behaviors were observed in memristive devices (Chang et al. 2011). Using memristors based on WO_x thin-films whose low resistance state showed a spontaneous loss of retention due to the random motion of oxygen vacancies following a stretched-exponential

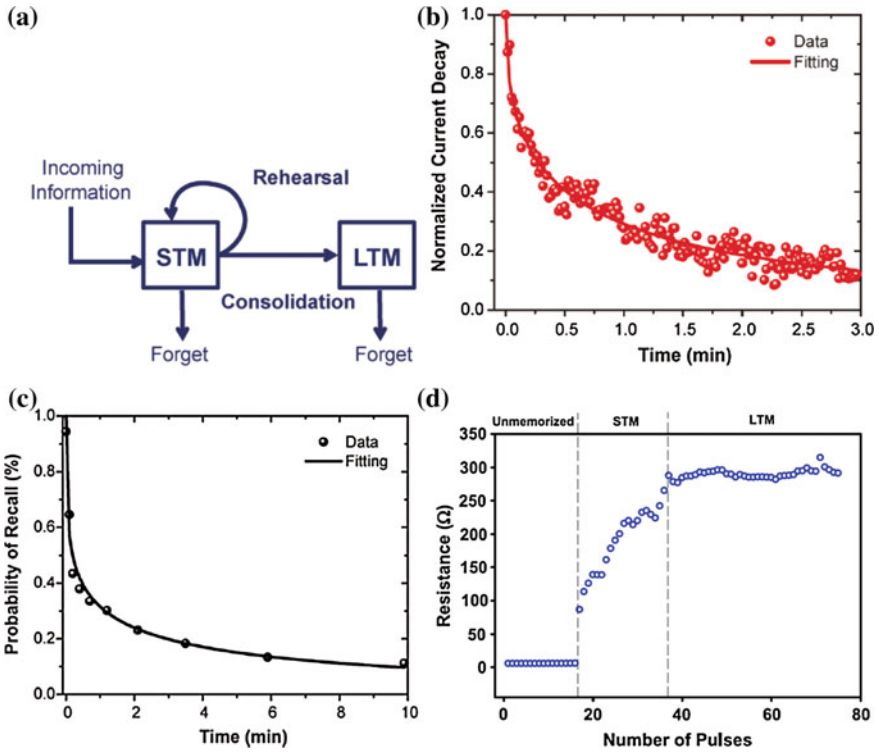

Fig. 6 **a** Schematic of the multi-store memory model, **b** WO_x-based memristor retention curve and **c** forgetting curve of human memory (Reprinted with permission from (Chang et al. 2011). Copyright 2011 American Chemical Society). **d** Three memory stages observed in NiO_x memristors upon application of consecutive voltage pulses (0.5 V in height, 0.1 s in width; Reprinted with permission from (Liu et al. 2011). Copyright 2011 American Chemical Society)

function law (Fig. 6b), Chang et al. demonstrated artificial properties close to those of memory loss in biological structures (Fig. 6c). However, if repeated stimulus are given, both the overall conductance and the retention time of the device are enhanced with increasing number of stimulus and stimulation rate, showing similarities with paired-pulse facilitation and post-tetanic potentiation. The transition between short-term and long-term memory was then suggested based on the existence of two memory regimes with short and long retention times.

As shown in Fig. 6d, three memory stages (unmemorized, STM and LTM) were also observed in a Ni-rich nickel oxide device by Liu et al. (2011). Memorization from STM to LTM is obtained by increasing the number of pulses. Behaviors such as STM, LTM, STDP and spike-rate dependent plasticity were also observed in Ta/PEDOT:PSS/Ag (Li et al. 2013). Tsuruoka et al. found LTM in an Ag/Ta_2O_5/Pt cell under voltage bias for a high repetition rate of input pulses, which is analogous to the behavior of biological synapses (Tsuruoka et al. 2012) and Wan et al. mimicked STM and LTM in nanogranular phosphorus-doped SiO_2 films by tuning the pulse gate voltage amplitude (Wan et al. 2013). The compliance current during electroforming was also shown to have an impact on the retention and analog properties of FeO_x based memristors (Wang et al. 2016).

Wang et al. reported a spontaneous decay of the synaptic weight in an amorphous InGaZnO memristor (Wang et al. 2012). The decay is very fast in the initial stage and then gradually slows down, which is consistent with the human "forgetting curve". Their results also indicate that in synaptic devices with "learning-experience", re-learning is easily achieved (Fig. 7). Also, with increasing

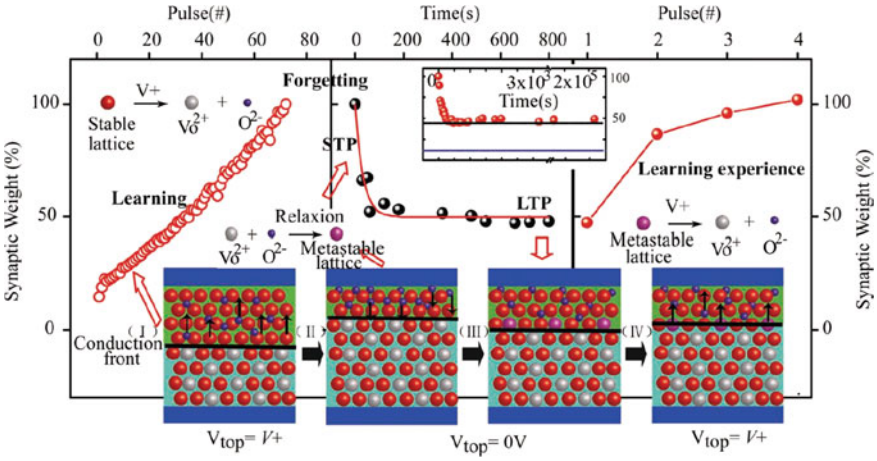

Fig. 7 **a** InGaZnO memristor conductance (synaptic weight) increase with the number of applied pulses. **b** Spontaneous relaxation of the conductivity (forgetting curve) upon removal of the stimulus and corresponding fit to an exponential function. **c** Re-stimulation upon voltage decay, showing now the need for only four pulses to reach the high conductance state. *Bottom inset* shows the proposed oxygen ion migration model (From (Wang et al. 2012), Advanced Functional Materials, Copyright © 2012 by [John Wiley & Sons, Inc.]. Reprinted by permission of [John Wiley & Sons, Inc.])

number of stimulation pulses, the relaxation time increases from several seconds to tens of seconds and tends to saturate beyond 100 stimulations, indicating a decreasing forgetting rate (Wang et al. 2012).

Using TiO_2 bipolar memristors, R. Berdan et al. demonstrated short-term plasticity with protocols similar to those used for biological synapses (Berdan et al. 2016). Figure 8a shows that the application of voltage pulses initially leads to volatile switching, in which the memristors conductance decays back to its low value. However, the successive application of voltage pulses eventually leads to non-volatile switching to the high conductance state. Two cases of short-term facilitation were emulated by providing three consecutive voltage pulses: in the first (Fig. 8b), the memristor's conductance is increased by each of the applied pulses (classical short-term facilitation; STP-F); however, in some particular situations, the conductance after the second and third pulses decreased with respect to that obtained after the first voltage spike (Fig. 8c); saturation short-term facilitation STP-S]. The latter effect was explained in terms of a mobility saturation of oxygen vacancies near a partially formed filament. Spatio-temporal computation was also achieved using these memristive synapses and an exponential integrate-and-fire neuron. The built circuit was able to differentiate two spatio-temporal patterns each consisting of three −4 V, 10 μs pulses separated by 250 ms applied first to a static resistance and then to the memristive synapse (AB) or vice-versa (BA). A discrimination success rate of 67.5% with 15% false positives was obtained.

3.1.3 Spintronic Memristors

Memristive behavior has also been found in spintronic devices, particularly MgO-based magnetic tunnel junctions (MTJs). These are two-terminal devices constituted by two ferromagnetic (FM) layers separated by an MgO thin insulator (Parkin et al. 2004; Yuasa et al. 2004; Ikeda et al. 2010; Teixeira et al. 2011). While the magnetization of one of the ferromagnetic layers is pinned by an antiferromagnet, the other is free to reverse under a small external magnetic field. This allows obtaining two different resistance states associated with the parallel (when the magnetization of the two FM layers point in the same direction) and anti-parallel (when they are opposite) configurations by simply applying an external magnetic field. Furthermore, the discovery of the Spin Transfer Torque (STT) effect opened the possibility to switch the magnetization of the MTJ by passing a sufficiently high spin polarized current through the stack or to induce persistent magnetization precession in the GHz range (Spin Torque Nano Oscillators; STNOs) (Locatelli et al. 2014; Kiselev et al. 2003; Kubota et al. 2008). However, besides magnetic switching, these structures also display resistance variations of non-magnetic origin arising from ionic migration within the ultra-thin insulating barrier: resistive switching (Krzysteczko et al. 2009a, b, 2012; Teixeira et al. 2009; Ventura et al. 2007; Yoshida et al. 2008).

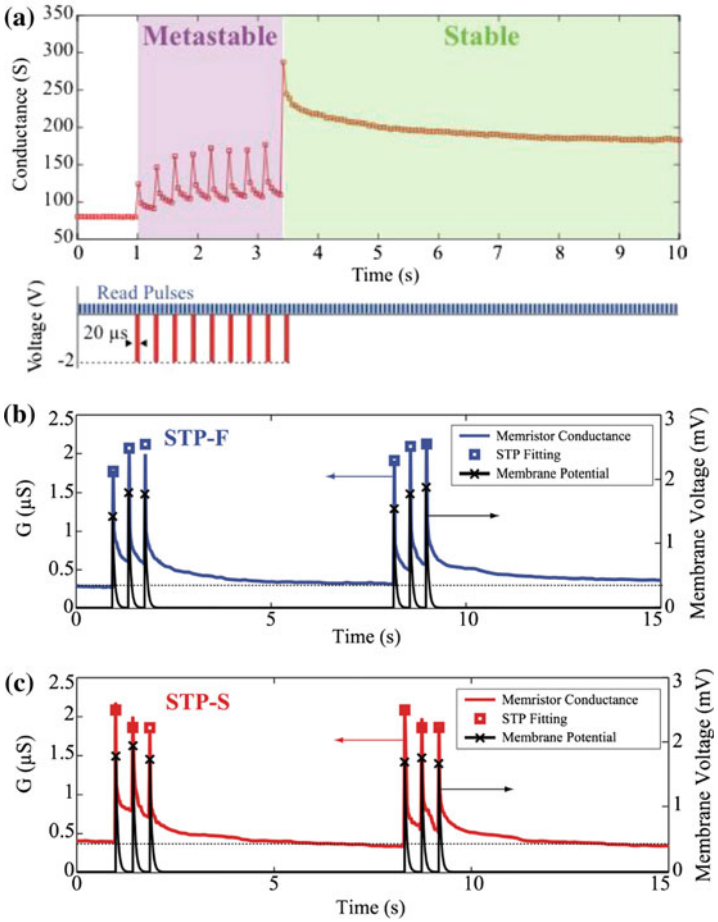

Fig. 8 **a** Metastable and stable conductance states in TiO_2-based memristors as function of voltage stimulus. Short-term plasticity and of a memristor acting as a **b** facilitating (STP-F) and **c** saturated (STP-S) synapse and corresponding fitting (Reprinted from Berdan et al. 2016; used in accordance with the Creative Commons Attribution (CC BY) license)

Krzysteczko et al. were the first to demonstrate that MTJs possess the characteristics of both of synapses (arising from non-magnetic resistive switching) and neurons (driven by STT effects; see below) (Krzysteczko et al. 2012). Figure 9a shows their observation of STDP in magnetic tunnel junctions given a proper choice of the amplitudes of the voltage function. When the time interval between the pulses (Δt) is high, the joint effect of the two spikes does not exceed the threshold voltage for switching, so that no variation of the conductance is seen. On the other hand, for low Δt, the applied voltage goes above the threshold and increasingly larger conductance variations are seen with decreasing pulse interval. The same work also reported that, by applying an electrical current large enough to

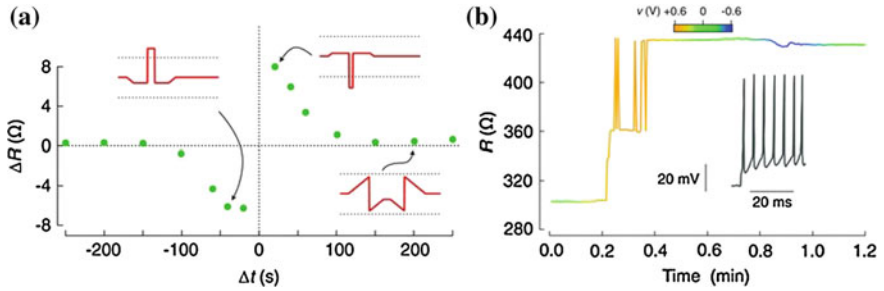

Fig. 9 **a** Spike Timing Dependent Plasticity of an MgO-based magnetic tunnel junction and **b** Spin Transfer Torque driven stochastic switching between two magnetic configurations. The *inset* shows the spiking behavior of a pyramidal neuron (From Krzysteczko et al. 2012, Advanced Materials, Copyright © 2012 by [John Wiley & Sons, Inc.]. Reprinted by permission of [John Wiley & Sons, Inc.])

induce STT effects, the magnetization of the free layer switched back-and-forward between an intermediate and the antiparallel state (back-hopping; Fig. 9b). Such stochastic current spikes showed a large similitude to the spiking of biological neurons and were proposed to emulate inter-neuronal communication.

Fully magnetic spintronic memristors were proposed in 2009 based on the spin transfer torque effect that offers a path for energy efficient, high-speed magnetization switching in nanoscale MTJs (Dimitrov 2009). These included magnetic tunnel junctions with perpendicular anisotropy under spin-torque excitations or STT-driven domain wall motion of the free layer of a spin valve or MTJ. A four terminal device based on spin-orbit torque by joining a heavy metal and a magnetic tunnel junction displaying spike-timing dependent plasticity was also recently proposed (Sengupta et al. 2015). An alternative proposal for spin based synapses is to use the inherent stochastic nature of the binary switching (parallel/antiparallel resistance states) of magnetic tunnel junctions that depends on the voltage amplitude and duration of the STT pulse (Vincent et al. 2015; Kavehei and Skafidas 2014). Following such proposal, it was possible to implement a simplified STDP rule, in which STDP occurs only when an output neuron spikes and the STT-switching of the MTJ conductance is stochastic rather than deterministic. System level simulations of a crossbar array of MTJs following the developed model demonstrated the possibility to train the network to learn to detect vehicle in a video. The impact of device-to-device variations of the parallel/antiparallel conductances and tunnel magnetoresistance on the detection rate of the vehicle counter was also studied and found to be robust for relative standard deviation (one-sigma) up to 17%.

3.1.4 Atomic Switches

In atomic switches, sometimes also called electrochemical metallization cells, or conductive-bridge random-access memories, resistive switching is related with the migration of metallic cations (M) from the active electrode (usually Cu or Ag) through an ionic conductor and the formation/annihilation of a conductive filament (Hasegawa et al. 2012; Jana et al. 2015; Goux and Valov 2016; Valov et al. 2011). Under the action of a positive bias (with the inert electrode grounded), ions from the active electrode (anode) are oxidized and diffuse towards the inert cathode where they are reduced. This ultimately results in the formation of a metallic filament and thus the high conductance state. The application of a reverse voltage results in the oxidation of the metallic ions from the filament and their reduction at the active electrode, resulting in the dissociation of the metallic filament and thus the low conductance state.

The first observation of learning abilities in atomic switches was achieved in silver rich Ag_2S-based structures (Hasegawa et al. 2010). In this case, an Ag protrusion grows between the Ag_2S and Pt electrodes across a vacuum gap by the action of an applied voltage, ultimately bridging the two, with learning/unlearning occurring with the widening/thinning of the Ag atomic bridge. With the same type of structure, Ohno et al. were able to emulate both STP and LTP depending on the stimulation rate (Fig. 10) (Ohno et al. 2011). When stimulated with a low repetition rate (at 20 s intervals), the conductance of the atomic switch increases to a high conductance state but spontaneously decreases to the low conductance state after each pulse is removed rate (Fig. 10a). This was related with the formation of an incomplete metallic bridge that dissolves when the applied bias voltage is removed and can be associated with short-term plasticity of biological synapses. On the other hand, the application of high repetition rates (2 s intervals) results in the formation of a robust atomic bridge between the electrodes (persistent high conductance state) and thus to a transition to LTP (Fig. 10b). The authors also showed the possibility to implement the so called multistore model: sensory information is initially stored as a sensory memory and then selected information is transferred from a temporary short-term state to a permanent long-term state through rehearsal, depending on the amplitude and width of the voltage stimulus (Ohno et al. 2011). For this, two images were stored in a 7×7 array of Ag_2S atomic switches (Fig. 10c). While the image of the number '2' was stored using well separated voltages pulses (20 s; corresponding to the STP case), that of number '1' was stored using closer pulses (2 s; which led to LTP). Initially both numerals were present, but '2' started to disappear as soon as the voltage pulses were removed due to the prompt decay of the conductance associated with the STP state and only the '1' image was transferred to the LTM mode and remained after stimulus stopped. The short-term dynamics of Ag_2S atomic switches was also used to encode input spike patterns (Ma et al. 2015).

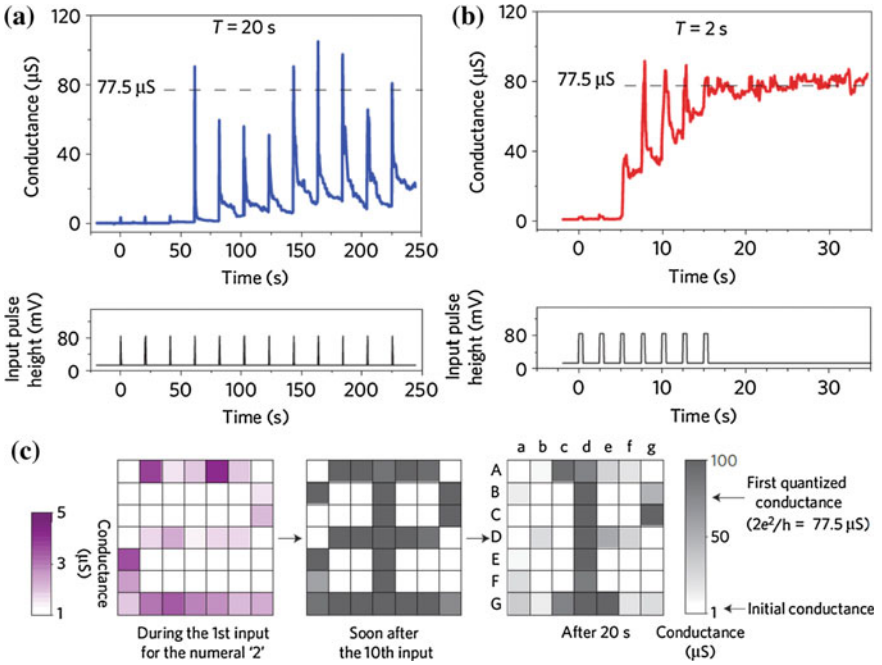

Fig. 10 Conductance variation of an Ag_2S atomic switch for **a** low and **b** high repetition rates (for 80 mV pulses) showing STP and LTP, respectively. **c** Storage of the numerals '1' (in the LTM mode) and '2' (in the STM) in a 7 × 7 array and the decay of the '2' memory 20 s after short-term memorization (Reprinted by permission from Macmillan Publishers Ltd: Nature Materials (Ohno et al. 2011), copyright 2011)

Furthermore, Barbera et al. showed that the STP/LTP transition could be tuned by both the used current compliance during SET (I_c; switching from the low to the high conductance states) and the number of excitatory pulses that can be independently changed (Fig. 11) (Barbera et al. 2015). It was shown that higher current compliances led to larger ON state conductance due to an increased density or width of the formed (dendritic) filaments. By measuring the relaxation time (τ) of the ON state conductance after the device was exposed to a train of potentiation pulses with varying number of pulses (from 15 to 150), it was possible to observe that samples with higher conductance before relaxation (G_{max}; obtained using either higher number of pulses or compliance current) had shorter relaxation time constants (Fig. 11a). As G_{max} increased, so did the stability of the filaments which then lead to higher τ-values and to a transition from STP to LTP. The same overall result can be seen in (Fig. 11b), where G_{100s} stands for the conductance value 100 s after the train of potentiation pulses was applied and $G_{100s} \approx G_{max}$ indicates that no relaxation of the conductance took place, i.e. long-term plasticity.

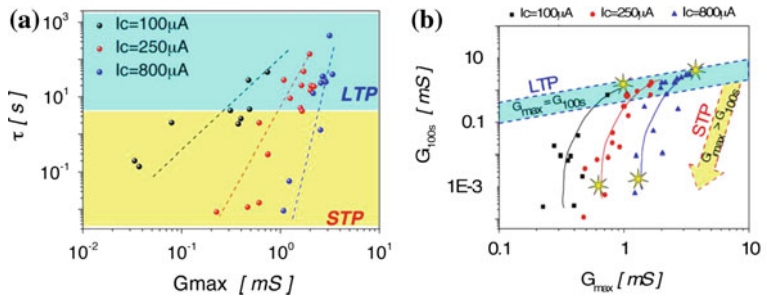

Fig. 11 **a** Relaxation time constant as a function of the conductance value after a train of potentiation pulses with varying number of pulses (from 15 to 150) is applied (G_{max}) for different compliance currents. **b** Conductance measured 100 s after the application of the train of potentiation pulses for different compliance currents (Adapted with permission from (Barbera et al. 2015). Copyright 2015 American Chemical Society)

An alternative proposal was recently reported based on stochastic learning rules using GeS_2-atomic switches (Suri et al. 2013). Taking into account the intrinsic stochastic switching behavior of atomic switches at low applied voltage, a stochastic STDP rule, similar to that presented for spintronic magnetic tunnel junctions (Sect. 3.1.3), was developed and used for auditory and visual pattern extraction.

3.2 *Neuristors*

A neuristor is a circuit capable of performing neural functions, since it successfully generates an action potential upon sufficient excitation, and emulates its propagation through an axon following the conditions of threshold action, refractory period and constant propagation. The term was carved in 1960 by H.D. Crane and, to implement it, one only requires three components: an energy source, an energy-storage element and a negative resistance (active) device (Crane 1960; Lu 2012; Pickett and Williams 2013).

The neuristor is a dynamical spiking device where the logic '1' is the existence of a spike and '0' its absence. It is a system able to compute all Boolean functions, so that it is said to be logically complete, allowing the duplication of any logic system (Crane 1960) and enabling massive parallel bio-inspired computing architectures (Pickett and Williams 2013). Following this idea, in 2012 Pickett et al. fabricated a neuristor based on two Mott memristors exhibiting neural functions, where an insulating-to-conducting phase transition (in NbO_2) takes place due to Joule heating and results in the creation of a conductive channel between the two electrodes (Fig. 12) (Pickett et al. 2012). The implemented circuit (Fig. 12a) is composed by two units: one equivalent to the sodium channels and the other to the potassium ones. Each capacitor serves to build up charge and the memristor in

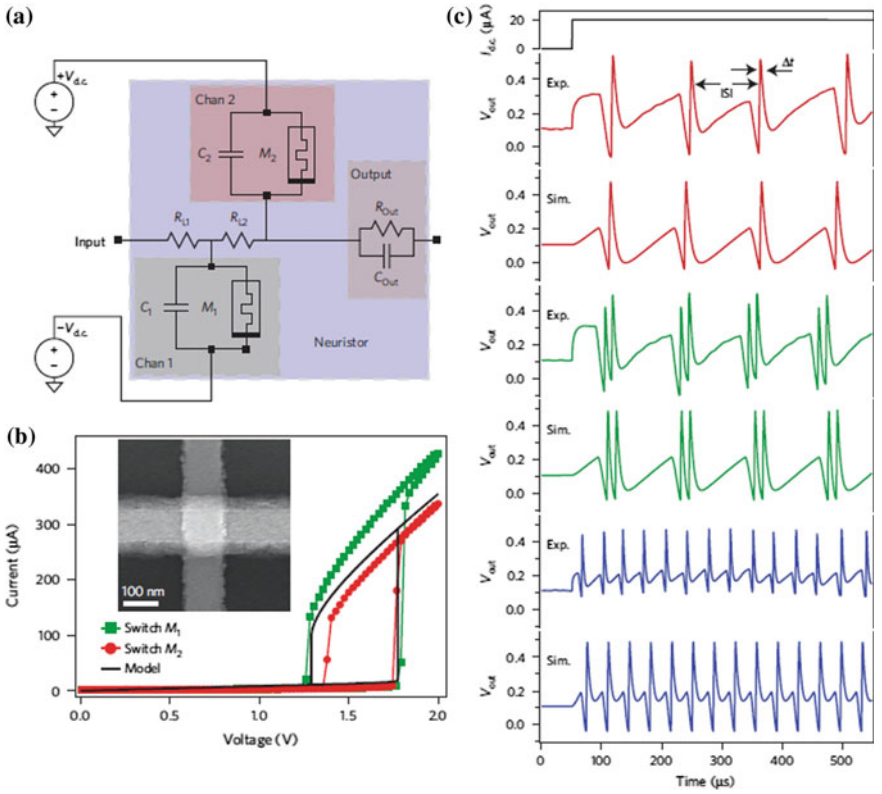

Fig. 12 **a** Neuristor diagram and **b** Mott memristors characteristics, **c** experimental and simulated spikes for different inter-spike interval (ISI) and spike width (Δt) (Reprinted by permission from Macmillan Publishers Ltd: Nature Materials (Pickett et al. 2012), copyright 2012)

parallel to release it suddenly. When a voltage threshold is exceeded, the Mott insulators change into the metallic phase (Fig. 12b), discharging the capacitors and spikes of activity that emulate an axon action potential are produced (Fig. 12c). Changing the components values, a variety of spiking behaviors were achieved, both experimentally and in simulations. Mott memristors turning ON and OFF can therefore be seen as electronic and inorganic analogues of the biological neuronal ion channels opening and closing. These neuristors can be downscaled and either be integrated with existing circuits or implemented in transistorless designs. With this scalable implementation, there is no need for a comparator and a logic element in the artificial neuron design (Chabi et al. 2014; Zhou and Ramanathan 2015). Furthermore, these schemes should allow a deep study of the nervous system (Pickett et al. 2012).

Mehonic et al. also implemented a simplified circuit model to emulate the neuron electrical activity using a SiO_x memristor (Mehonic and Kenyon 2016). They observed voltage spiking and a dynamic voltage output when applying a constant or

pulsed current input. Gale et al. studied non-ideal memristive networks and concluded that the richness and dynamics complexity of spiking circuits increases for three memristors in anti-series and/or anti-parallel, when compared to systems with only two memristors (Gale et al. 2014). However, if the three memristors have the same polarity, the circuit is stable and does not spike. They further simulated eight circuit compositions of up to three memristors both in series and in parallel. Notice that, in all these cases, memristive devices are used to assume the functions of a neuron, a complement to the synapse behavior to be used in neuromorphic systems.

4 Synthetic Neural Networks

As in conventional electronics, significant processing power and complexity is achieved in the human brain by combining multiple simpler computational units (i.e. synapses and neurons) into large network systems with well-defined architectures. There has been, therefore, several attempts to mimic the biological learning rules in artificial synapses and to construct artificial neural networks (ANNs) capable of performing complex functions. A network is based on the transmission of events from one source node (neuron) to multiple nodes by edges (synapses; see examples in Fig. 13). In most ANN models, synapses are dynamical two-terminal entities that connect a pre- (source) to a post-synaptic neuron (sink). The source emits a signal that is modified by a synaptic transfer function and delivered to the sink. To facilitate the communication between neurons, the action potential is propagated as a digital pulse (Schemmel and Grubl 2006). The output of a neural network node is a function of the sum of all input signals (Ha and Ramanathan 2011). The sink has a state variable that partially depends upon the history of incoming signals received from synapses that drive it. This variable along with the source signal determine the evolution of the synaptic state variable.

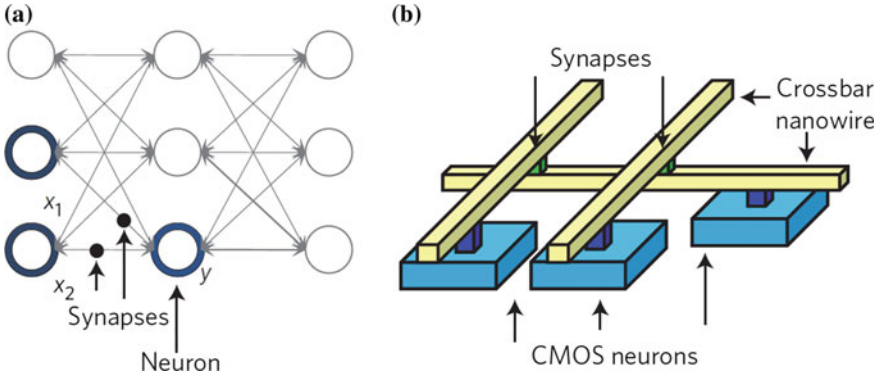

Fig. 13 **a** Graph and **b** crossbar network architectures (Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology (Yang et al. 2013), copyright 2013)

A radical approach in the construction of artificial neural networks is to use very large scale integration (VLSI) to implement directly in silicon the required computational model of a neural system. IBM researchers built a complex chip using 5.4 billion transistors to simulate 1 million neurons and 256 million synapses (Merolla et al. 2014).

In neuromorphic implementations, the key challenge is to design circuits with large time constants while keeping the neuronal structure simple, occupying small silicon area and using only one electronic device as an artificial synapse. However, the silicon area occupied by the synaptic circuit can vary significantly, as it depends on the choice of layout design solutions and more conservative solutions use large transistors. Implementing the large connectivity of the brain with transistors on a single chip is a major challenge, since a large number of transistors are needed (Shi et al. 2011; Seo et al. 2011). Therefore, the electronic conventional implementation is not practical and a simple and scalable device able to emulate synaptic functions is required (Seo et al. 2011). As we have seen, the memristor displays such properties, making it the most promising candidate to be used in scalable neural networks.

Examples of different network architectures are discussed here, presenting configurations, which support operations such as classification (perceptron) or in-formation storage/memories.

4.1 Perceptron

In 1957, F. Rosenblatt developed a simple NN for pattern classification problems of linearly separable patterns: the perceptron (Fig. 14) (Rosenblatt 1957). It is the simplest kind of NN capable of learning and parallel processing (Wang et al. 2013). It consists of a main neuron that accepts several inputs from sensory neurons, connected by adjustable synaptic weights, and sums all weighted inputs (Fig. 14a). Depending on the result this neuron will fire (or not) if the result is positive (or negative), based on error-correlation learning (Park 2006; Haykin 2009; Daumé III 2012). The learning process for pattern classification occupies a finite number of iterations. Rosenblatt also proved that, if the patterns (vectors) used to train the perceptron are drawn from two linearly separable classes, then the perceptron algorithm converges and positions the decision surface in the form of a hyperplane between the two classes (Haykin 2009), a division of space into two halves by a straight line, where one half is "positive" and the other is "negative" (Fig. 14b) (Daumé III 2012).

The learning algorithm of the perceptron is based on the information that, in brains, many neurons encode stimuli intensity in terms of their firing rate (which in turn defines how "activated" the neuron is). Therefore, based on how much the input neurons fire and how strong the neural connections are, the main neuron will respond accordingly. Note that learning is nothing more than neurons becoming connected with each other and adapting their connection strength over time (Daumé III 2012).

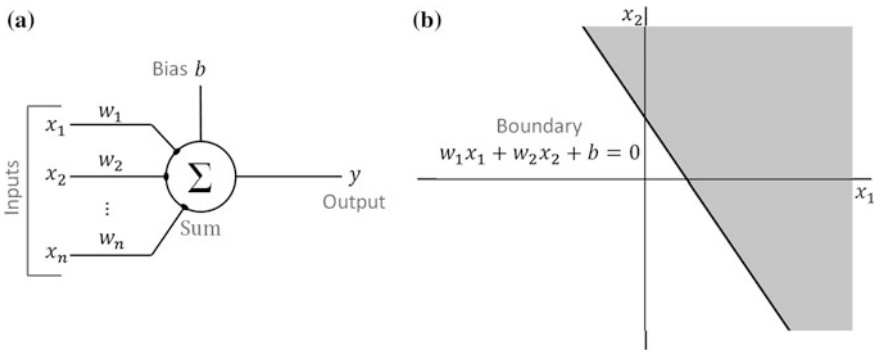

Fig. 14 **a** Single layer perceptron and **b** illustration of the hyperplane for a two-dimensional classification problem

Mathematically, the perceptron can be modulated as an input vector $x = x_1, x_2, \ldots, x_n$ arriving from n neurons, with n stored weights, $w_1, w_2, \ldots, w_n$, at the main neuron that computes a sum, a. Also, it is often convenient to have a non-zero threshold, which is achieved introducing a single scalar bias term into the neuron, so that activation is always increased by some fixed value b. The overall sum a, parameterized by n weights, and a bias value b is given by (Daumé III 2012):

$$a = \left[\sum_{i=1}^{n} w_i x_i\right] + b. \tag{2}$$

The weights are easy to interpret: if one input has a zero weight, then the activation is the same regardless of its value. Furthermore, positive (negative) weights are indicative of positive (negative) examples because they cause the activation to increase (decrease). This is the first learning algorithm in which the abilities of learning and pattern classification were achieved by Artificial Intelligence (Park 2006) and one of those algorithms that is incredibly simple and yet works amazingly well for some types of problems (Daumé III 2012).

As a classifier, perceptron applications include pattern recognition (fingerprint and iris) (Wang et al. 2013; Ashidi et al. 2011; Gatet et al. 2009), classification of medical images (Wang et al. 2013) (cancer classification for example Rosenblatt 1957) or gene array analysis (Bo et al. 2006), surface classification, object detection, distance measurement (Gatet et al. 2009), and forecast ozone and nitrogen dioxide levels measurement in real-time (Agirre-Basurko et al. 2006). The perceptron can thus be determinant in many fields such as obstacle detection for autonomous robots or vehicles, identification, surveillance, security systems, medical applications, industrial processes and navigation (Wang et al. 2013; Gatet et al. 2009). As an example, imagine for the medical case that you have databases from previous diagnosed patients for different disease indicators, each with a certain

influence on the diagnosis. You can then train your perceptron to learn to identify the given disease and even make it more probable to give false positives than false negatives or vice-versa.

As we have seen, memristors are highly attractive for this purpose due to its reconfigurable and analogue resistance, nanoscale size, automatic information storage and non-volatility (Wang et al. 2013). Alibart et al. achieved pattern classification using a single-layer perceptron network implemented with a TiO_2 memristive crossbar circuit (Alibart et al. 2013). This shows the possibility of fabricating new, dense and high performance information processing systems.

4.2 Memristive Artificial Neural Network

The recent progress in the experimental realization of memristive devices has renewed the interest in artificial neural networks (Thomas 2013) and many different learning laws have been proposed for edges (Snider 2007). Adjustable edge weights are the defining characteristic of neural networks and are the origin of their broad adaptive functionality (Ha and Ramanathan 2011). An edge's conductance changes as a function of the voltage drop across the edge induced by forward spikes from the source node and back spikes from the sink node. Using memristive nanodevices to implement edges, conventional analog and digital electronics to implement nodes, and pairs of bipolar pulses (spikes), to implement communication, it is possible to develop fully electronic neural networks (Snider 2007). For a very large number of synapses, a practical implementation of an artificial network using memristors allows the weights to be updated in parallel due to the high interconnectivity. For this, the logic value of the input ('1' and '0') is multiplied by the memristance value (Ha and Ramanathan 2011; Strukov and Kohlstedt 2012; Rose et al. 2011). It should be noted that, for ANNs, the density of the memristive devices is the most important property. Also, ANNs are resilient to variations in synapses and neurons (Strukov and Kohlstedt 2012). For example, instead of a single pulse, the average effect of hundreds of parallel synapse inputs into one neuron determines whether the neuron will fire or not (Yu et al. 2011).

One of the possible applications of memristor-based ANNs is to carry out position detection. This was simulated in Ref. (Ebong and Mazumder 2012), using ANNs that combine winner-take-all and STDP learning rules. Random networks of polymer coated Ag and oxide passivated Ni nanowires (Fig. 15), where their placement is not important and differences in properties are averaged out, also presented I-V memristive-like behavior (Nirmalraj et al. 2012). Atomic switch networks of $Ag/Ag_2S/Ag$ with random topology nanowires similar to Turing's B-Type unorganized machine were also fabricated using SU-8 photoresist and Ag_2S nanowires where filaments formation takes place at the atomic level (Fig. 16a, b; see Sect. 3.1.4) (Stieg et al. 2012; Stieg and Avizienis 2014). After an electroforming step, the electrical characterization of the whole network of highly interconnected atomic switches using macroscopic electrodes reproducibility

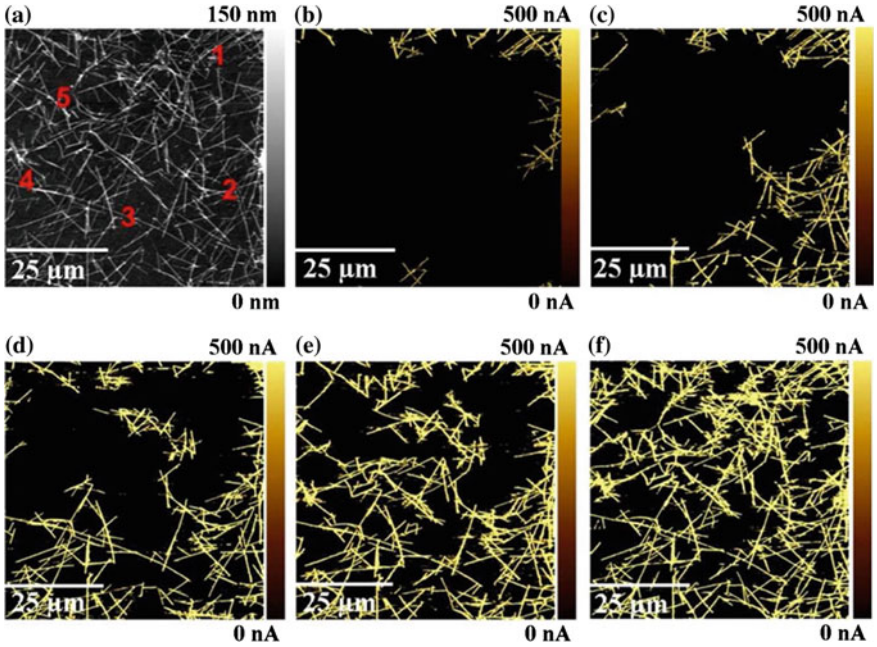

Fig. 15 **a** Topography of a random network of Ag nanowires. A metal coated atomic force microscope tip was used to locally activate sites in the network by applying a voltage pulse. The current maps shown in **b**–**f** are the result of applying the voltage pulses at selected regions (marked 1–5 on the topographic map; Reprinted with permission from (Nirmalraj et al. 2012). Copyright 2012 American Chemical Society)

showed pinched hysteresis loops similar to those of single devices (Fig. 16c). Furthermore, infra-red imaging confirmed the presence of distributed power dissipation throughout the network (Fig. 16d) and thus the formation of a functional network. Finally, emergent behavior, i.e. a behavior that is not found or associated with a single unit of the network, similar to that of neuron assemblies was also inferred from the observation of a large number of metastable conductance states resulting from discrete configurations of the network (Fig. 16e, f).

4.2.1 Crossbar Memory Arrays

A possible architecture for brain-based nanoelectronic computation is the crossbar array. Passive crossbar memory arrays are simple matrices consisting only of pre- and post-neuron connecting lines and a resistive switch at each junction acting as a synapse (Kügeler et al. 2011; Linn et al. 2012). In a crossbar structure, a two-terminal memristor synapse is formed at each crosspoint connecting pre- and post-synaptic neurons (Jo et al. 2010; Linn et al. 2012). Every neuron in the pre-neuron layer of the crossbar configuration is directly connected to every neuron

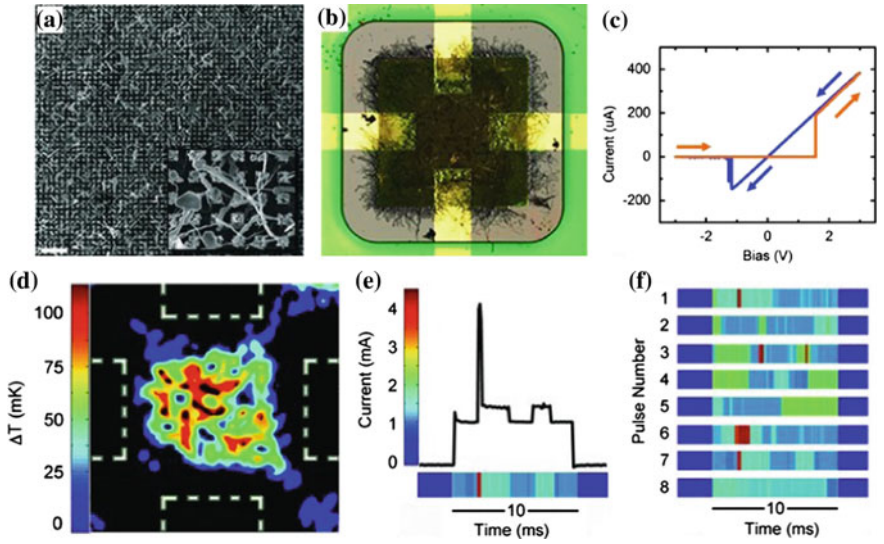

Fig. 16 **a** Zoomed and **b** enlarged view of an Ag/Ag_2S/Ag network of random nanowires. **c** Pinched hysteresis loops associated with the electrical behavior of the whole network. **d** Infra-red imaging of the network under an applied voltage displaying distributed power dissipation. **e**, **f** Switching between metastable conductance states as the network's response to voltage pulses (From (Stieg et al. 2012). Advanced Materials, Copyright © 2012 by [John Wiley & Sons, Inc.]. Reprinted by permission of [John Wiley & Sons, Inc.])

in the post-neuron layer (Jo et al. 2010; Kügeler et al. 2011). This 2D ANN can be seen in a generic manner as mapping sets of input patterns into specific output patterns fully connected through adaptive synapses. The information can be stored changing the value at the edges through an applied voltage between the nodes that they link and can have the meaning of a memory representation (data storage) or of a function representation (computation). Furthermore, higher memory density can be achieved in crossbar architectures than in CMOS architectures and, with 3D stacking, the memory density can be further increased (Chen 2011).

As shown in Fig. 17a, Prezioso et al. used Al_2O_3/TiO_{2-x} to fabricate a highly dense 12 × 12 (200 nm × 200 nm) memristors crossbar (free of transistors) (Prezioso et al. 2015). They used it to implement a stable single layer perceptron 10 (inputs) × 3 (outputs) that successfully performed pattern classification of 3 × 3-pixel images corresponding to three classes of letters, by in situ learning of 23 iterations on average. The operation is based on the self-tuning of the memristor conductance that is assured by its STDP behavior (Prezioso et al. 2016). A critical step was the optimization of the current-voltage nonlinearity through the aluminum oxide thickness to achieve devices with very low variability (Fig. 17b).

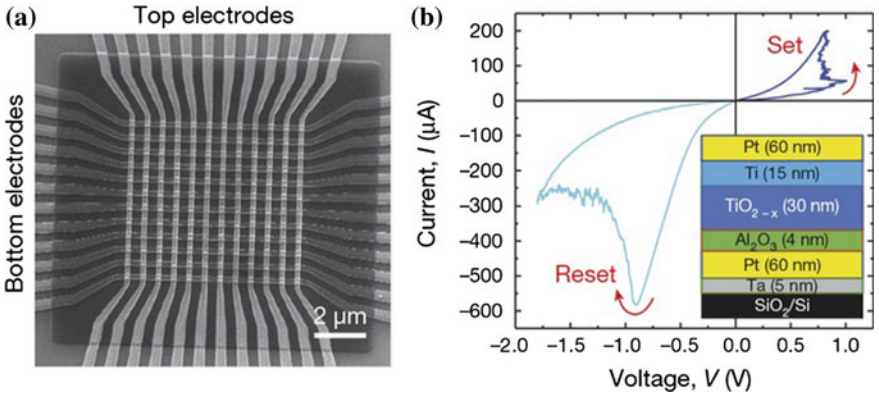

Fig. 17 **a** Memristors crossbar and **b** I-V curve of a single memristor (Reprinted by permission from Macmillan Publishers Ltd: Nature (Prezioso et al. 2015). copyright 2015)

Mostafa et al. also implemented a 8 × 8 (60 μm × 60 μm) hybrid CMOS-memristor perceptron based on an extended STDP rule connecting each two silicon neurons by a TiO_{2-x} memristor (Mostafa et al. 2015). Their rule has the advantage of not involving a post-synaptic spike timing, but instead a correlation between pre-synaptic spikes and signals from the post-synaptic neuron (membrane potential). This means that there is no need to generate temporally long waveforms on both synaptic sides. In both cases, each memristor was electrically prepared before being used as an artificial synapse by an individual electroforming process.

5 Associative Memories

In biological systems, neuronal circuits are deeply involved in the transmission, processing and storage of information. Importantly, and as previously mentioned, these three operations are supported by the same wetware substrate. While the mechanisms supporting efficient and reliable information transmission in neurons are known already since the early 50 s (Hodgkin and Huxley 1952) only more recently were the first steps given on understanding how information may be stored in neuronal populations (Willshaw et al. 1969; Hopfield 1982) The simplest models for information storage in neuronal populations assume that each unit (neuron) can be in one of two states: active or inactive. The information content of a neuronal population can then be seen as the spatiotemporal patterns of activity of its neurons: given a population of neurons, which neurons are active (spatial coding) at a specific time (temporal coding) encodes the information being handled in the network. This section focuses on memory systems relying of spatial coding only, in other words, static neuronal activation patterns in which a particular memory state is represented by a specific constellation of active neurons (no temporal dynamics

included). In a population of N neurons, and assuming each memory is represented by M active neurons, a total of $\binom{N}{M}$ different patterns can be considered (number of M-combinations from a population with N elements). Assuming a 5% activation in a population with 1000 neurons, there are on the order of 10^{85} different (spatial) activation patterns.

With information being encoded in the spatial patterns of activity, a simple associative memory system consists of associating particular activity patterns in an input population of neurons to other particular activity patterns in an output population of neurons. A list of associations may be stored, linking input activity patterns to output activity patterns, and the information is stored in the connections between neurons. In this feedforward connection architecture, the system is called an hetero-associative memory as it involves two distinct neurons populations (Willshaw et al. 1969). The alternative is when a single population, with recurrent connectivity, acts both as input and output, in which case the system take the name of auto-associative memory (Hopfield 1982).

The storage of information and memory formation in the nervous system has multiple properties which are very interesting from the engineering point of view. In particular, and as opposed to the standard man-made storage systems, neuronal based memory systems are distributed, meaning that elements of information are encoded across groups of units. These memory systems are therefore capable of graceful degradation: the progressive loss of individual storage units (neurons) does not lead to an abrupt failure of the memory system. Another important feature is that neuronal memory systems are content-addressable memories—information retrieval is achieved not with the presentation of a reference/memory address, but instead it is triggered by the presentation of part of the stored information (cue). Standard man-made memory systems are reference addressable instead. In the case of a hard drive, this implies the existence of a file allocation table (FAT, or a modern form of it) associating file contents to disk cluster addresses—simply damaging/eliminating the allocation table impairs information retrieval (a strategy which was commonly used by computer viruses). Neuronal based memory systems are also intrinsically robust to noise and capable of auto-completion; that is, a modified version of the original input pattern can be used to trigger the recall of the originally associated output pattern. This important property links associative networks to the problem of pattern recognition. All together, these properties (summarized in Table 1) make biology inspired associative networks extremely attractive from the engineering point of view.

Memristors are in a unique favorable position to support the fabrication of efficient and reliable associative memories mimicking the key features of their biological counterparts. Memristors have been shown to be adequate for the implementation of both hetero-associative (Dias et al. 2015) and auto-associative (Hu et al. 2015a, b; Duan et al. 2016; Guo et al. 2015) memories.

Table 1 Comparison between neuronal and standard man-made memory systems

	Neuronal associative memory systems	Standard man-made memory systems
Access	Content-addressable	Reference-addressable
Storage	Distributed	Local
Intrinsic robustness to noise	Yes	No
Intrinsic auto-completion	Yes	No
Low power	Yes	Yes, in some implementations
Response to units loss	Graceful degradation	Potential memory corruption
Storage capacity	Low[a]	High

[a]Current experimental/theoretical evidence points to a storage capacity (as a function of the number of storage units or number of connections) which is lower than standard man-made memory systems (Treves and Rolls 1991) (but see also Alme et al. 2014)

5.1 Principles of Operation

In both types of associative memory architectures, full connectivity is typically assumed between the input and output populations: this means that each neuron in the output population receives one connection from each neuron in the input population (in the case of the auto-associative memory all neurons are connected with all neurons except with themselves). In the simplest associative networks, not only the neuronal state is binary (silent or active) but also the connection strength (weak or strong). Analogously with the read/write modes in man-made systems, current models for associative memories also assume two operation modes: storage and recall (or retrieval). A proper separation, in terms of mechanism, between these operations is necessary to avoid information corruption. Memory storage and retrieval is governed by the neuronal units' dynamics as well as by synaptic modification (learning) rule. The common (and the original) choice for the neuronal dynamics in the discrete associative memory is the McCullock-Pitts model (McCulloch and Pitts 1943) in which the output state of the neuron is 1 (active) only if the weighted sum of its inputs is equal or above a predefined threshold value T; otherwise the output state is 0 (silent) (Fig. 18). As for the learning rule applied in the storage phase, the typical choice is the Hebb rule. It should be noted, nonetheless, that in general this is not an optimal learning rule in terms of storage capacity – higher memory storage capacities can be achieved using slightly modified learning rules (see for example Refs. Dayan and Willshaw (1991); Storkey (1997)). The Hebb rule has however the advantage of being easily recreated with simple memristor dynamics.

In memristive-based implementations of associative memories, memristors are used to establish the network connections while controlled voltage sources (Dias et al. 2015) or operational amplifiers (Hu et al. 2015a, b) are used to represent the state of input neuron units. A simple memristive-based hetero-associative memory

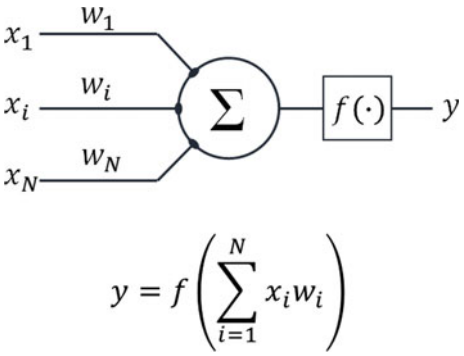

Fig. 18 Diagram of the McCulloch-Pitts neuron. Input signals x are weighted by the corresponding synaptic strengths *w* and a non-linear transfer function f (e.g. a threshold function) is used to set the output signal *y*

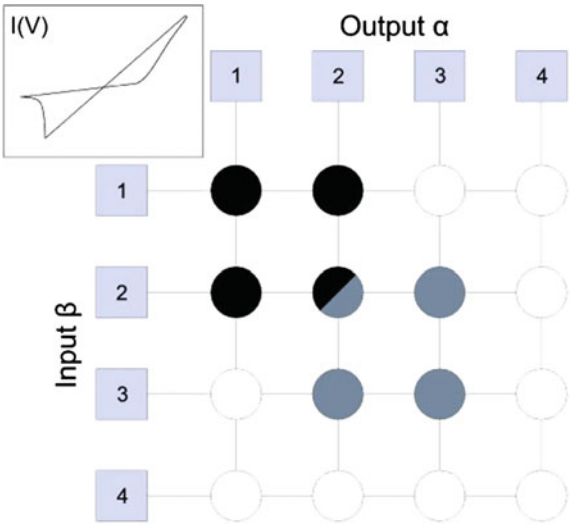

Fig. 19 Hetero-associative memory architecture. *Squares* represent neuron units and *circles* represent memristors (low conductance state, *empty circles*; and high conductance states, *shaded circles*). Two associations were stored in this network: $\{\beta_1, \beta_2\} \rightarrow \{\alpha_1, \alpha_2\}$ and $\{\beta_2, \beta_3\} \rightarrow \{\alpha_2, \alpha_3\}$ (Reprinted from (Dias et al. 2015). with the permission of AIP Publishing)

is show in Fig. 19. Squares represent neuron units from two populations (input β and output α) while circles represent memristors (empty circles represent low conductance state and shaded circles represent high conductance state). In this representation, the following associations are intended: $\{\beta_1, \beta_2\} \rightarrow \{\alpha_1, \alpha_2\}$ and $\{\beta_2, \beta_3\} \rightarrow \{\alpha_2, \alpha_3\}$. During storage, memristors conductances are modified according to the learning rule. In the case of Hebb learning and binary synapses, the memristor state is changed from low to high conductance state only when both input and output units are active. During retrieval, the activation of a stored input pattern leads (with the appropriate threshold T settings) to the recall of the associated output pattern. Naturally, with the increasing number of stored associations comes interference between patterns. With random, sparse activity patterns, the capacity of this memory system scales with $\frac{N_\alpha N_\beta}{M_\alpha M_\beta}$, where N is the total number of units in each population, and M is the number of active units in each patterns

(Willshaw et al. 1969). Intuitively, maximum capacity is achieved when half of the memristors where modified to the high conductance state. After this stage, storage of additional association leads to a fast memory performance degradation.

5.2 Coping with Faulty Memristors

Presently, memristor fabrication is still far from a 100% yield (Strukov and Likharev 2007) and some variability is expected between units. Implementations of associative memories based on memristor technology cannot rely on the assumption that all memristor units perform equally well. A source of inspiration and insights on how to cope with faulty memristors comes from the associative memories literature addressing the issues of partial connectivity and different threshold setting strategies (Buckingham and Willshaw 1993; Graham and Willshaw 1996).

In the context of memristors emulating connections with binary weights, a common defect resulting from lithography processes is the inability to switch between resistive states. This leaves the memristors device permanently ("stuck at") on the high, or in the low, resistive state. The situation of stuck at high resistance is comparable to the absence of connections. Given the intrinsic resilience of associative memories (distributed information, soft degradation, noise robustness) it has been shown (Dias et al. 2015) that under appropriate operation strategies, the presence of a significant fraction of faulty units (5%) does not necessarily imply catastrophic failure of the memory system. Moreover, knowing a priori the expected percentage of faulty units after the fabrication process, it is possible to devise threshold setting strategies (different thresholds for each output unit) (Buckingham and Willshaw 1993) which mitigate the reduction in memory capacity.

5.3 Unlearning and Palimpsest Memories

The information retrieval performance in conventional associative memory systems collapses after the storage capacity has been exceeded. Statistically speaking, if R is the memory system capacity, the number of correctly recalled patterns approaches R as storage/recall cycles progress, and then abruptly falls to very low values. If one wants to produce effective memristor-based associative memories, one needs to surpass this problem. In the field of neuronal networks, several approaches have been proposed to address this, introducing different forms of erasing, unlearning or "forgetting" old and no more used associations. In the case of a memristive device with filamentary switching, unlearning can be seen for example as the thinning of the filament by applying an opposite bias polarity (Hasegawa et al. 2010). In general, one interesting approach to address the memory collapse problem introduces the concept of palimpsest memories (Sandberg et al. 2000; Sterratt and Willshaw 2008). A palimpsest was a medieval manuscript that was repeatedly

reused over time by inscribing text over the previous existing, being only the most recent writing visible. The analogy with new memories replacing older ones can be done (Henson 1993). There is not a catastrophic forgetting, but instead these forgetful learning rules select the older memories to forget in order to store the new ones (Storkey 2015).

There are three main strategies using palimpsest considering forgetting approaches in the Willshaw network. The first is random resetting, where random switches are turned off with a (small) random probability. The second is weight ageing, in which switches are turned off with a probability that depends on the age of the switch which in turn is the time since it was last triggered. The last one is generalized learning, the only that is not random but dependent on the patterns presented at a given time (Henson 1993).

While memristors can in principle support the construction of palimpsest associative memory systems, this subject has not yet been appropriately addressed.

6 Conclusions and Outlook

Memristors exhibit noteworthy properties which make them excellent building blocks to construct neuromorphic systems. They are low power devices, nanosized, have good scalability properties and above all they mimic core aspects of the dynamics of ion channels present at synapses and neuron membranes. As a result, they are able to reproduce, *in silico*, many of the mechanisms associated with neural computation, such as classification, decision-making, learning and memory. The human brain is the result of more than 4.5 billion years of evolution and optimization, and is therefore Nature's solution to fast and efficient information processing and information storage. By copying features of the human brain uncovered by recent advances in neuroscience, one hopes to produce innovations in computing technology and memory storage devices. Current computing paradigms face major scalability problems, one of them being electric power demand. It is forecasted that, by 2040, computing electric power demand will surpass the amount generated (ITRS 2015). The human brain, capable of pattern recognition, precise motor control, and other complex information processing tasks, has a remarkably low power consumption (Sengupta and Stemmler 2014), in the range of 25 watts (Kandel et al. 2003). Memristors have the potential to enable novel bio-inspired computing paradigms.

Since the memristor hypothesis by Leon Chua, the realization of a physical model by HP's researchers, and through the many recent exciting results regarding theory and fabrication, the field has made tremendous progress and the time is ripe to explore the possibilities opened by memristors. Simulating or even discriminating actual neural activity (Gupta et al. n.d.) of the human brain, and getting inspiration of it to produce novel computing systems is certainly one of the most promising applications. But there are still many open challenges in memristive-based neuromorphic systems: mathematical models of memristors'

dynamics need to be consolidated and validated, the physical implementation of small memristive-based circuits needs to become more consistent and reliable, circuits to drive learning processes (as well and information storage/retrieval) in memristive systems need to be improved, efficient coding/decoding mechanisms for memristor memory systems need to be explored, just to name a few. As in all other fields in science, challenges are also opportunities, and memristive-based neuromorphic systems offers many exciting possibilities to the research groups willing to tackle them.

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References

Agirre-Basurko, E., Ibarra-Berastegi, G., & Madariaga, I. (2006). Regression and multilayer perceptron-based models to forecast hourly O_3 and NO_2 levels in the Bilbao area. *Environmental Modelling & Software*, *21*(4), 430–446.

Alibart, F., et al. (2012). A memristive nanoparticle/organic hybrid synapstor for neuroinspired computing. *Adv. Funct. Mater., 22*(3), 609–616.

Alibart, F., Zamanidoost, E., & Strukov, D. B. (2013). Pattern classification by memristive crossbar circuits using ex situ and in situ training. *Nature Communications*, *4* (2072).

Alme, C. B., et al. (2014). Place cells in the hippocampus: Eleven maps for eleven rooms. *Proceedings of the National Academy of Sciences of the USA, 111*(52), 18428–18435.

Ashidi, N., et al. (2011). Clustered-hybrid multilayer perceptron network for pattern recognition application. *Applied Soft Computing, 11*(1), 1457–1466.

Barbera, S. La, Vuillaume, D., & Alibart, F. (2015). Filamentary switching: Synaptic plasticity through device volatility. *ACS Nano, 9,* 941–949.

Berdan, R., et al. (2016). Emulating short-term synaptic dynamics with memristive devices. *Scientific Reports*, *6*, 18639 (November 2015).

Bo, L., Wang, L. & Jiao, L. (2006). Multi-layer Perceptrons with embedded feature selection with application in Cancer Classification. *Chinese Journal of Electronics*.

Buckingham, J., & Willshaw, D. (1993). On setting unit thresholds in an incompletely connected associative net. *Network, 4,* 441–459.

Chabi, D., et al. (2014). Robust learning approach for neuro-inspired nanoscale crossbar architecture. *ACM Journal on Emerging Technologies in Computing Systems, 10*(1), 1–20.

Chang, T., Jo, S., & Lu, W. (2011). Short-term memory to long-term memory transition in a nanoscale memristor. *ACS Nano, 5*(9), 7669–7676.

Chen, A. (2011). Ionic memory technology. In *Solid state electrochemistry II: Electrodes, interfaces and ceramic membranes* (pp. 1–18).

Choi, S. J., et al. (2011). Synaptic behaviors of a single metal-oxide-metal resistive device. *Applied Physics A, 102*(4), 1019–1025.

Chua, L. (1971). Memristor-the missing circuit element. *IEEE Transactions on Circuit Theory, 18* (5), 507–519.

Conde-Sousa, E., & Aguiar, P. (2013). A working memory model for serial order that stores information in the intrinsic excitability properties of neurons. *Journal of Computational Neuroscience, 35*(2), 187–199.

Crane, H. D. (1960). The Neuristor. *IRE Transactions On Electronic Computers, 9,* 370–371.

Daumé III, H. (2012). The perceptron. In *A course in machine learning* (pp. 37–50).

Dayan, P., & Willshaw, D. J. (1991). Optimising synaptic learning rules in linear associative memories. *Biological cybernetics*, *65*(4), 253–265.

Dias, C., et al. (2015). Memristor-based Willshaw network: Capacity and robustness to noise in the presence of defects. *Applied Physics Letters, 106*(22), 223505.

Dimitrov, D. (2009). Spintronic memristor through spin-torque-induced magnetization motion. *IEEE Electron Device Letters, 30*(3), 294–297.

Du, C., et al. (2015). Biorealistic implementation of synaptic functions with oxide memristors through internal ionic dynamics. *Advanced Functional Materials, 25*(27), 4290–4299.

Duan, S., et al. (2016). Small-world Hopfield neural networks with weight salience priority and memristor synapses for digit recognition. *Neural Computing and Applications, 27*(4), 837–844.

Ebong, I. E., & Mazumder, P. (2012). CMOS and memristor-based neural network design for position detection. *Proceedings of the IEEE, 100*(6), 2050–2060.

Gale, E., Costello, B. D. L., & Adamatzky, A. (2014). Emergent spiking in non-ideal memristor networks. *Microelectronics Journal, 45*(11), 1401–1415.

Gatet, L., Tap-Béteille, H., & Bony, F. (2009). Comparison between analog and digital neural network implementations for range-finding applications. *IEEE Transactions on Neural Networks, 20*(3), 460–470.

Goux, L., & Valov, I. (2016). Electrochemical processes and device improvement in conductive bridge RAM cells. *Physica Status Solidi (A) Applications and Materials Science*, *213*(2), pp. 274–288.

Graham, B., & Willshaw, D. (1996). Information efficiency of the associative net at arbitrary coding rates. In *Artificial neural networks—ICANN 96* (pp. 35–40).

Guo, X., et al. (2015). Modeling and experimental demonstration of a hopfield network analog-to-digital converter with hybrid CMOS/memristor circuits. *Frontiers in Neuroscience*, *9*, 1–8(Dec).

Gupta, I., et al. (n.d.) Memristive integrative sensors for neuronal activity. arXiv:1507.06832.

Ha, S. D., & Ramanathan, S. (2011). Adaptive oxide electronics: A review. *Journal of Applied Physics, 110*(7), 071101.

Hasegawa, T., et al. (2012). Atomic switch: Atom/ion movement controlled devices for beyond von-neumann computers. *Advanced materials (Deerfield Beach, Fla.)*, *24*(2), 252–67.

Hasegawa, T., Ohno, T., Terabe, K., Tsuruoka, T., Nakayama, T., Cimzewski, J. K., et al. (2010). Learning abilities achieved by a single solid-state atomic switch. *Advanced Materials, 22*(16), 1831–1834.

Haykin, S. (2009). Rosenblatt's perceptron. In *Neural networks and learning machines* (pp. 47–67). Pearson.

Henson, R. (1993). *Short-term associative memories*.

Hodgkin, A. L., & Huxley, A. F. (1952). A quantitative description of membrane current and its application to conduction and excitation in nerves. *Journal of Physiology, 117,* 500–544.

Hopfield, J. J. (1982). Neural networks and physical systems with emergent collective computational abilities. *Proceedings of the National Academy of Sciences of the USA, 79*(8), 2554–2558.

Hu, S. G., et al. (2013a). Design of an electronic synapse with spike time dependent plasticity based on resistive memory device. *Journal of Applied Physics*, *113*(11).

Hu, S. G., et al. (2013b). Emulating the paired-pulse facilitation of a biological synapse with a NiO_x-based memristor. *Applied Physics Letters*, *102*(18).

Hu, S. G., et al. (2015a). A memristive Hopfield network for associative memory. *Nature Communications, 6,* 7522.

Hu, S. G., et al. (2015b). Associative memory realized by a reconfigurable memristive Hopfield neural network. *Nature Communications, 6*(May), 7522.
Ikeda, S., et al. (2010). A perpendicular-anisotropy CoFeB–MgO magnetic tunnel junction. *Nature Materials, 9*(9), 721–724.
Indiveri, G., et al. (2013). Integration of nanoscale memristor synapses in neuromorphic computing architectures. *Nanotechnology, 24*(38), 384010.
ITRS. (2015). *International technology roadmap for semiconductors 2.0.*
Jana, D., et al. (2015). Conductive-bridging random access memory: Challenges and opportunity for 3D architecture. *Nanoscale Research Letters, 10*(1), 188.
Jo, S. H., et al. (2010). Nanoscale memristor device as synapse in neuromorphic systems. *Nano Letters, 10*(4), 1297–1301.
Kandel, E. R., Schwartz, J. H., & Jessell, T. M. (2003). *Principles of neural science*. Manole.
Karmarkar, U. R., & Buonomano, D. V. (2002). A model of spike-timing dependent plasticity: One or two coincidence detectors? *Journal of Neurophysiology, 88*(1), 507–513.
Kavehei, O., & Skafidas, E. (2014). Highly scalable neuromorphic hardware with 1-bit stochastic nano-synapses. In *Proceedings—IEEE International Symposium on Circuits and Systems*, pp. 1648–1651.
Kim, H., Sah, M. P., et al. (2012a). Memristor bridge synapses. *Proceedings of the IEEE, 100*(6), 2061–2070.
Kim, H., Sah, M. P., et al. (2012b). Neural synaptic weighting with a pulse-based memristor circuit. *IEEE Transactions on Circuits and Systems, 59*(1), 148–158.
Kim, S., et al. (2015). Experimental demonstration of a second-order memristor and its ability to biorealistically implement synaptic plasticity. *Nano Letters, 15*(3), 2203–2211.
Kiselev, S. I., et al. (2003). Microwave oscillations of a nanomagnet driven by a spin-polarized current. *Nature, 425*(6956), 380–383.
Kozma, R., Pino, R. E., & Pazienza, G. E. (2012). *Advances in neuromorphic memristor science and applications*, Springer Publishing Company, Incorporated.
Krzysteczko, P., Kou, X., et al. (2009a). Current induced resistance change of magnetic tunnel junctions with ultra-thin MgO tunnel barriers. *Journal of Magnetism and Magnetic Materials, 321*(3), 144–147.
Krzysteczko, P., Reiss, G., & Thomas, A. (2009b). Memristive switching of MgO based magnetic tunnel junctions. *Applied Physics Letters, 95*(11), 112508.
Krzysteczko, P., et al. (2012). The memristive magnetic tunnel junction as a nanoscopic synapse-neuron system. *Advanced Materials (Deerfield Beach, Fla.)*, *24*(6), 762–766.
Kubota, H., et al. (2008). Quantitative measurement of voltage dependence of spin-transfer torque in MgO-based magnetic tunnel junctions. *Nature Physics, 4*(1), 37–41.
Kügeler, C., et al. (2011). Materials, technologies, and circuit concepts for nanocrossbar-based bipolar RRAM. *Applied Physics A, 102*(4), 791–809.
Li, Q., et al. (2015). A memristor SPICE model accounting for synaptic activity dependence. *PLoS ONE, 10*(3), e0120506.
Li, S., et al. (2013). Synaptic plasticity and learning behaviours mimicked through Ag interface movement in an Ag/conducting polymer/Ta memristive system. *Journal of Materials Chemistry C, 1*(34), 5292.
Linn, E., et al. (2012). Beyond von Neumann–logic operations in passive crossbar arrays alongside memory operations. *Nanotechnology, 23*(30), 305205.
Liu, Y., et al. (2011). Self-learning ability realized with a resistive switching device based on a Ni-rich nickel oxide thin film. *Applied Physics A, 105*(4), 855–860.
Locatelli, N., Cros, V., & Grollier, J. (2014). Spin-torque building blocks. *Nature Materials, 13*(1), 11–20.
Lu, W. (2012). Memristors: Going active. *Nature Materials, 12*(2), 93–94.
Ma, W., et al. (2015). Temporal information encoding in dynamic memristive devices. *Applied Physics Letters, 107*(19), 193101.
McCulloch, W. S., & Pitts, W. (1943). A logical calculus of the ideas immanent in nervous activity. *The Bulletin of Mathematical Biophysics, 5*(4), 115–133.

Mehonic, A., & Kenyon, A. J. (2016). Emulating the electrical activity of the neuron using a silicon oxide RRAM cell. *Frontiers in Neuroscience*, *10*, article 57.

Merolla, P. A., et al. (2014). A million spiking-neuron integrated circuit with a scalable communication network and interface. *Science, 345*(6197), 668–673.

Mostafa, H., et al. (2015). Implementation of a spike-based perceptron learning rule using TiO_{2-x} memristors. *Frontiers in Neuroscience, 9,* 357.

Nirmalraj, P. N., et al. (2012). Manipulating connectivity and electrical conductivity in metallic nanowire networks. *Nano Letters, 12*(11), 5966–5971.

Ohno, T., Hasegawa, T., Nayak, A., et al. (2011a). Sensory and short-term memory formations observed in a Ag_2S gap-type atomic switch. *Applied Physics Letters, 99*(20), 203108.

Ohno, T., Hasegawa, T., Tsuruoka, T., et al. (2011b). Short-term plasticity and long-term potentiation mimicked in single inorganic synapses. *Nature Materials, 10*(8), 591–595.

Pan, R., et al. (2016). Synaptic devices based on purely electronic memristors. *Applied Physics Letters, 108*(1), 013504.

Park, H. (2006). Multilayer perceptron and natural gradient learning. In *New generation computing* (pp. 79–95).

Park, S., et al. (2012). RRAM-based synapse for neuromorphic system with pattern recognition function. In *2012 international electron devices meeting* (pp. 10.2.1–10.2.4). IEEE.

Parkin, S. S. P., et al. (2004). Giant tunnelling magnetoresistance at room temperature with MgO (100) tunnel barriers. *Nature Materials, 3*(12), 862–867.

Pickett, M. D., Medeiros-Ribeiro, G., & Williams, R. S. (2012). A scalable neuristor built with Mott memristors. *Nature Materials, 12*(2), 114–117.

Pickett, M. D., & Williams, R. S. (2013). Phase transitions enable computational universality in neuristor-based cellular automata. *Nanotechnology, 24*(38), 384002.

Pinto, S., et al. (2012). Resistive switching and activity-dependent modifications in Ni-doped graphene oxide thin films. *Applied Physics Letters, 101*(6), 063104.

Prezioso, M., et al. (2016). Self-adaptive spike-time-dependent plasticity of metal-oxide memristors. *Scientific Reports, 6*(February), 21331.

Prezioso, M., et al. (2015). Training and operation of an integrated neuromorphic network based on metal-oxide memristors. *Nature, 521*(7550), 61–64.

Rose, G. S., Pino, R., & Wu, Q. (2011). A low-power memristive neuromorphic circuit utilizing a global/local training mechanism. In *The 2011 international joint conference on neural networks* (pp. 2080–2086). IEEE.

Rosenblatt, F. (1957). *The perceptron, a perceiving and recognizing automation*.

Sandberg, A., et al. (2000). A palimpsest memory based on an incremental Bayesian learning rule. *Neurocomputing, 32–33,* 987–994.

Schemmel, J., & Grubl, A. (2006). Implementing synaptic plasticity in a VLSI spiking neural network model. In *International joint conference on neural networks* (pp. 1–6).

Sengupta, A., et al. (2015). Spin-orbit torque induced spike-timing dependent plasticity. *Applied Physics Letters, 106*(9), 093704.

Sengupta, B., & Stemmler, M. B. (2014). Power consumption during neuronal computation. *Proceedings of the IEEE, 102*(5), 738–750.

Seo, K., et al. (2011). Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device. *Nanotechnology, 22*(25), 254023.

Serrano-Gotarredona, T., et al. (2013). STDP and sTDP variations with memristors for spiking neuromorphic learning systems. *Frontiers in Neuroscience*, *7*(7 Feb), 1–15.

Shi, L. P., et al. (2011). Artificial cognitive memory-changing from density driven to functionality driven. *Applied Physics A, 102*(4), 865–875.

Snider, G. (2008). Spike-timing-dependent learning in memristive nanodevices. In *Nanoscale architectures, 2008. NANOARCH 2008* (pp. 85–92).

Snider, G. S. (2007). Self-organized computation with unreliable, memristive nanodevices. *Nanotechnology, 18*(36), 365202.

Sterratt, D. C., & Willshaw, D. (2008). Inhomogeneities in heteroassociative memories with linear learning rules. *Neural Computation, 20*(2), 311–344.

Stieg, A., & Avizienis, A. (2014). Self-organized atomic switch networks. *Japanese Journal of Applied Physics*, *53*, 01AA02.

Stieg, A. Z., et al. (2012). Emergent criticality in complex turing B-Type atomic switch networks. *Advanced Materials, 24*(2), 286–293.

Storkey, A. (1997). Increasing the capacity of a Hopfield network without sacrificing functionality. *Artificial Neural Networks – ICANN'97* (pp. 451–456).

Storkey, A., 2015. Palimpsest memories: A new high-capacity forgetful learning rule for Hopfield networks. *Electrical Engineering* (July), 1–14.

Strukov, D. B., et al. (2008). The missing memristor found. *Nature, 453*(7191), 80–83.

Strukov, D. B., & Kohlstedt, H. (2012). Resistive switching phenomena in thin films: Materials, devices, and applications. *MRS Bulletin, 37*(02), 108–114.

Strukov, D. B., & Likharev, K. K. (2007). Defect-tolerant architectures for nanoelectronic crossbar memories. *Journal of Nanoscience and Nanotechnology, 7,* 151–167.

Suri, M., et al. (2013). Bio-inspired stochastic computing using binary CBRAM synapses. *IEEE Transactions on Electron Devices, 60*(7), 2402–2409.

Teixeira, J. M., et al. (2009). Electroforming, magnetic and resistive switching in MgO-based tunnel junctions. *Journal of Physics. D. Applied Physics, 42*(10), 105407.

Teixeira, J. M., et al. (2011). Resonant tunneling through electronic trapping states in thin MgO Magnetic junctions. *Physical Review Letters, 106*(19), 196601.

Thomas, A. (2013). Memristor-based neural networks. *Journal of Physics. D. Applied Physics, 46,* 093001.

Treves, A., & Rolls, E. (1991). What determines the capacity of autoassociative memories in the brain? *Network: Computation in Neural Systems, 2*(4), 371–397.

Tsuruoka, T., et al. (2012). Conductance quantization and synaptic behavior in a Ta_2O_5-based atomic switch. *Nanotechnology, 23*(43), 435705.

Valov, I., et al. (2011). Electrochemical metallization memories-fundamentals, applications, prospects. *Nanotechnology, 22*(28), 289502.

Ventura, J., et al. (2007). Three-state memory combining resistive and magnetic switching using tunnel junctions. *Journal of Physics D Applied Physics, 40*(19), 5819–5823.

Vincent, A. F., et al. (2015). Spin-transfer torque magnetic memory as a stochastic memristive synapse for neuromorphic systems. *IEEE Transactions on Biomedical Circuits and Systems, 9* (2), 166–174.

Wan, C. J., et al. (2013). Memory and learning behaviors mimicked in nanogranular SiO_2-based proton conductor gated oxide-based synaptic transistors. *Nanoscale, 5*(21), 10194–10199.

Wang, C., et al. (2016). Investigation and manipulation of different analog behaviors of memristor as electronic synapse for neuromorphic applications. *Scientific Reports*, 6(November 2015), p. 22970.

Wang, L., Duan, M., & Duan, S. (2013). Memristive perceptron for combinational logic classification. *Mathematical Problems in Engineering, 2013*(1), 1–7.

Wang, Y.-F., et al. (2015). Characterization and modeling of nonfilamentary $Ta/TaO_x/TiO_2/Ti$ analog synaptic device. *Scientific Reports, 5,* 10150.

Wang, Z. Q., et al. (2012). Synaptic learning and memory functions achieved using oxygen ion migration/diffusion in an amorphous InGaZnO memristor. *Advanced Functional Materials, 22* (13), 2759–2765.

Williamson, A., et al. (2013). Synaptic behavior and STDP of asymmetric nanoscale memristors in biohybrid systems. *Nanoscale, 5*(16), 7297–7303.

Willshaw, D. J., Buneman, O. P., & Longuet-Higgins, H. C. (1969). Non-holographic associative memory. *Nature, 222*(5197), 960–962.

Yang, J. J., Strukov, D. B., & Stewart, D. R. (2013). Memristive devices for computing. *Nature Nanotechnology, 8*(1), 13–24.

Yang, R., et al. (2012). On-demand nanodevice with electrical and neuromorphic multifunction realized by local ion migration (SI). *ACS Nano, 6*(11), 9515–9521.

Yoshida, C., Kurasawa, M., & Lee, Y. (2008). Unipolar resistive switching in CoFeB/ MgO/CoFeB magnetic tunnel junction. *Applied Physics Letters, 92,* 113508.

Yu, S., Wu, Y., & Jeyasingh, R. (2011). An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation. *IEEE Transactions on Electron Devices, 58*(8), 2729–2737.

Yuasa, S., et al. (2004). Giant room-temperature magnetoresistance in single-crystal Fe/MgO/Fe magnetic tunnel junctions. *Nature Materials, 3*(12), 868–871.

Zamarreño-Ramos, C., et al. (2011). On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex. *Frontiers in neuroscience, 5,* 26.

Zhou, Y., & Ramanathan, S. (2015). Mott memory and neuromorphic devices. *Proceedings of the IEEE, 103*(8), 1289–1310.