Circuit Techniques for IoT-Enabling Short-Range ULP Radios

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This chapter addresses the design of cost-aware ultra-low-power (ULP) radios for both 2.4-GHz and sub-GHz ISM bands. Starting from the system aspects that provide the essential insights, effective circuit techniques are presented to improve the radio performances and power efficiency, while minimizing the die area and number of external components.

14.1 ULP Wireless Nodes in the IoT Landscape

Smart cities, environmental monitoring, energy management and healthcare systems, just to name a few, are all inside the gigantic landscape of Internet of Things (IoT) (Stankovic 2014) or Internet of Everything (IoE). The estimated IoT market by 2020 will be close to hundreds of billion dollars (annually ~16 billions). To accelerate the proliferation of IoT products in different application sectors, it is opportune to develop *ultra-low-cost software-defined ULP radios* that are flexible to support different data rates (e.g., from kb/s to a few Mb/s), different standards [e.g., *ZigBee and Bluetooth Low Energy* (*BLE*)] and a wide range of frequency (e.g., sub-GHz and 2.4-GHz ISM bands), while occupying a small die area and entailing a minimum number of external components. These next-generation ULP radios will be decisive for a wide variety of products that have strong competition among cost, performance and time-to-market. Nevertheless, the tradeoff analysis between cost, size and power for an ULP wireless link can involve many parameters that must be co-designed, implying that deeper understanding of the system aspects and effective circuit techniques are both essential to reach an optimum solution.

14.2 System Aspects of Short-Range ULP Radios

Focusing on short-range connectivity with a RF link budget of ~80 to 90 dB, the physical (PHY) layer specifications of Zigbee and BLE are not particularly tough for modern RF skills. Yet, traditional textbook RF and analog techniques can unlikely help to bring down the radio's power by orders of magnitude, while allowing it to be universal enough to serve multiple bands without resorting from costly external components. The following sub-sections briefly discuss the PHY layer of Zigbee and BLE standards. The pros and cons of opting different frequency bands and supply voltages (VDD) are

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Table 14.1 Key PHY specifications of ZigBee and BLE standards

	ZigBee	BLE
Frequency (GHz)	0.3, 0.4, 0.7, 0.9, 2.4	2.4
Bandwidth (MHz)	2	1
Channel Spacing (MHz)	5	2
Modulation	BPSK, OQPSK	GFSK
Range (m)	10 to 200	10 to 100
Data Rate (Mbps)	0.25	1
Network Topology	Star/Mesh	Star/P2P

also mentioned; all are correlated to the overall cost, size and power efficiency of the radios.

14.2.1 ZigBee and Bluetooth Low Energy (BLE) Standards

Both ZigBee and BLE standards are suitable for short-range ULP communication as they draw low peak and average power. Their key features are briefed next.

ZigBee was developed as a wireless personal-area network (WPAN) standard with the IEEE 802.15.4 to define the PHY and Media Access Control (MAC) layers. It can operate at a very low duty cycle (<1%) and is allowed in three different frequency bands. The first band (868 MHz) is for Europe only offering only a single channel. It supports a low bit rate of 20 kbps using binary phase-shift keying (BPSK) modulation. The second band (915 MHz) permits 10 channels and is widely adopted in North America, Australia, New Zealand, and some countries in South America. Each channel supports 40 kbps using BPSK modulation. The third band is 2.4 GHz available worldwide, and has a total of 16 channels with 250 kbps each. Unlike the sub-GHz bands, this third band exploits offset quadrature phase-shift keying (OQPSK) with half sine-wave shaping for its modulation. Beyond these three bands, the IEEE 802.15.4c/d study groups also considered to open 314 to 316 MHz, 430 to 434 MHz, and 779 to 787 MHz bands for use in China, and 950 to 956 MHz for use in Japan. Obviously, an international market will be opened if the ULP radio can be reconfigured to support multiple bands from sub-GHz to 2.4 GHz. The key PHY specifications of ZigBee and BLE standards are summarized in Table 14.1.

BLE is a prospective short-range wireless standard ratified in 2009. It supports 40 channels in the 2.4-GHz band, each of which is 2-MHz wide. It is based on Gaussian frequency-shift keying (GFSK) modulation with an index of 0.5. The state-of-the-art 2.4-GHz receiver (Liu et al. 2014) achieves an energy efficiency of ~1.2 nJ/b at 2 Mb/s. Unsurprisingly, >40% of the receiver power is dissipated by the forefront low-noise amplifier (LNA) and mixer to maximize the sensitivity (−92 dBm). Such a high sensitivity seems overkill, but it is indeed effective to reduce the power consumption of the transmitter which normally has a lower energy efficiency to fulfill an RF link budget of ~90 dB. Thus, it is highly desired to develop circuit techniques for better LNA, mixer and voltage-controlled oscillator (VCO) for a better overall energy efficiency. In fact, for the 2.4-GHz band, Zigbee and BLE share a similar PHY, and modern solutions can easily support both. For the sub-GHz bands, multi-band operation poses additional challenges. To achieve this without leveraging the cost, a fully-integrated RF-tunable ULP radio will be of great relevance.

14.2.2 Cost, Size and Power

Ultra-scaled CMOS technologies are still the best platform for full integration of ULP radios that have RF (transceiver), analog (sensor and power management) and digital (microcontroller and memory). Established technology nodes (e.g., 90 or 65 nm) are regaining lots of interest for low-cost fast-to-market IoT products, as they can

leverage more reasonably between the manufacturing cost, development time and power consumption. Apparently, the system cost and size can be optimized by reducing the chip area, number of external components and battery volume that depends on the targeted lifetime of the system. Although using on-chip passives (inductors and transformers) can help to reduce the VDD and system power, we will describe later that recent cost-aware ULP RF and analog circuits can balance better the power, chip area and cost. For instance, a fully-integrated input matching network not only can reduce the cost and system form factor of an ULP receiver, but also enhance its power efficiency. Also, the matching network can offer passive pre-gain to enhance the sensitivity of the receiver. Other low-power techniques such as current-reuse and function-reuse are will be introduced later in this chapter.

14.2.3 Frequency Bands: 2.4 GHz vs. Sub-GHz

Most existing ULP radios were designed for the 2.4-GHz band as it is available worldwide and has a smaller antenna size suitable for integration. Yet, the sub-GHz ISM bands offer other advantages such as longer propagation distance and less interference that are worth to be considered when the power budget is the priority.

Communication range—In highly congested environments, the 2.4-GHz signal can weaken rapidly, which adversely affects the signal quality. To quantify the influence of frequency on path loss with respect to the wavelength λ, we can use the simplified Friis transmission equation,

$$L = 20\log_{10}\left(\frac{4\pi d}{\lambda}\right) \qquad (14.1)$$

Hence, it can be calculated that the path loss at 2.4 GHz is 8.5 dB higher than that at 900 MHz. This translates into a 2.67× longer range for a 900-MHz radio. Since the range almost doubles with every 6 dB increment of power, a 2.4-GHz radio will entail an increment of power budget (by 8.5 dB), in order to match the range of a 900-MHz radio. Besides, biological tissues absorb RF energy as a function of frequency. Lower frequencies can penetrate the body easily without being absorbed, meaning a better RF link for sub-GHz when compared to 2.4 GHz for body-area networks.

Interference—The 2.4-GHz band has a high chance to come across interferences due to the co-existence of other wireless standards, degrading the link reliability. For example, the IEEE 802.11 (WiFi) can transmit an output power 10x to 100x higher than the ZigBee. Signals from Bluetooth-enabled computer, cell phone peripherals and microwave ovens can also be considered as "jammers", which have a much lower output power. Sub-GHz ISM bands are mostly used for proprietary low-duty-cycle links and are not as likely to interfere with each other. A quieter spectrum means easier transmissions and fewer retries, which is more efficient to save the battery power. In fact, due to the limited power budget, it is hard for an ULP radio to tolerate large out-of-channel blockers.

Antenna size—One disadvantage of sub-GHz operation is the larger antenna size since most antenna types are designed to be resonant at their intended operation frequency. Since the antenna size is inversely proportional to the frequency, a small wireless node would prefer the 2.4-GHz band. Communication distance, low potential interference and low power consumption are the obvious advantages of the sub-GHz bands.

14.2.4 Supply Voltage (VDD)

To minimize the system size, short-range ULP radios should run preferably from a tiny battery, thus sub-2 V supply voltages are highly desired. Radios that work down to 1.2 V allow extra flexibility in sensors' design and reduce the power management constraints (Rajan 2012). Besides, low peak current and sub-1 V VDD also benefit wireless sensors that run from harvested energy sources which will enhance flexibility, lower the maintenance cost, and

open up more applications. For example, on-chip solar cells only can provide an output voltage between 200 and 900 mV, while thermoelectric generators exhibit an even lower VDD (50–300 mV) (Bandyopadhyay et al. 2011). Although boost converters can be employed to boost up the output voltage, their efficiency is still quite limited (~75%). Besides, a low peak current consumption will ease the design of the power management. Furthermore, radio operating at higher VDD is only required when a higher output power is entailed. This is not the case for short-range communications, as the output power rarely exceeds 0 dBm. Thus, a low VDD is in general the simplest way to reduce the power consumption at the system level.

In a low VDD design, however, due to the limited dynamic range, for the given parameters such as third-order intercept point (IIP3), noise-figure (NF), gain etc., the current should be larger than that with a high VDD. For example, for the given NF requirement, the current-reuse P-type metal-oxide-semiconductor (PMOS) and N-type metal-oxide-semiconductor (NMOS) self-biased amplifier with a VDD of 1 V consumes half of the current of a single NMOS (or PMOS) without current-reuse and with a VDD of 0.5 V. This constraint is even tighter if a small chip area and/or no/limited external components are imposed for cost reduction. As an example, inductors/transformers can help to boost the operating frequency and bias the circuit with lower voltage headroom and noise. If inductors/transformers cannot be used due to the limited area budget, only resistors or transistors can be adopted instead. This imposes a hard trade-off with IIP3, NF and bandwidth. Thus, to balance the VDD, current, area and external components with the key performance metrics (NF and out-of-band (OB) IIP3), effective system-to-circuit-level co-design, RF and analog circuit techniques become highly important and correlated. The next two sections present the key circuit techniques applied into two state-of-the-art cost-aware ULP receivers: one for the 2.4-GHz band and one for the sub-GHz bands.

14.3 Current-Reuse ULP Receiver Techniques for the 2.4-GHz ISM Band

Nanoscale CMOS offers sufficiently high f_t and low V_t favoring the design of ULP receivers via stacking the RF-to-baseband (BB) functions in one cell, while sharing the smallest possible bias current. Also, the signals can be conveyed in the current domain to enhance the area efficiency (i.e., no AC-coupling capacitor), RF bandwidth and linearity at those inner nodes. The proposed Zigbee receiver (Lin et al. 2013, 2014a) is inspired by the above hypothesis, and its block diagram is depicted in Fig. 14.1.

The single-ended RF input (V_{RF}) is taken by a low-Q input-matching network before reaching the Balun-LNA-I/Q-Mixer (Blixer). Merging the Blixer with the hybrid filter not only saves power, but also reduces the voltage swing at internal nodes benefitting the linearity. The wide-band input-matching network is also responsible for the passive pre-gain to reduce the NF. Unlike the LMV cell that only can utilize single-balanced mixers (Tedeschi et al. 2010), here the balun-LNA featuring a differential output ($\pm i_{LNA}$) allows the use of double-balanced mixers (DBMs). Driven by a 4-phase 25% LO, the I/Q-DBMs with a large output resistance robustly correct the differential imbalances of $\pm i_{LNA}$. The balanced BB currents ($\pm i_{MIX,I}$ and $\pm i_{MIX,Q}$) are then filtered directly in the current domain by a current-mode Biquad stacked atop the DBM. The Biquad features in-band noise-shaping centered at the desired intermediate frequency (IF, 2 MHz). Only the filtered output currents ($\pm i_{rLPF,I}$ and $\pm i_{rLPF,Q}$) are returned as voltages ($\pm V_{o,I}$ and $\pm V_{o,Q}$) through the complex-pole load, which performs both image rejection and channel selection. Out of the current-reuse path there is a high-swing variable-gain amplifier (VGA). It essentially deals with the gain loss of its succeeding 3-stage passive RC-CR polyphase filter (PPF), which is responsible for large and robust image rejection over mismatches and process variations. The

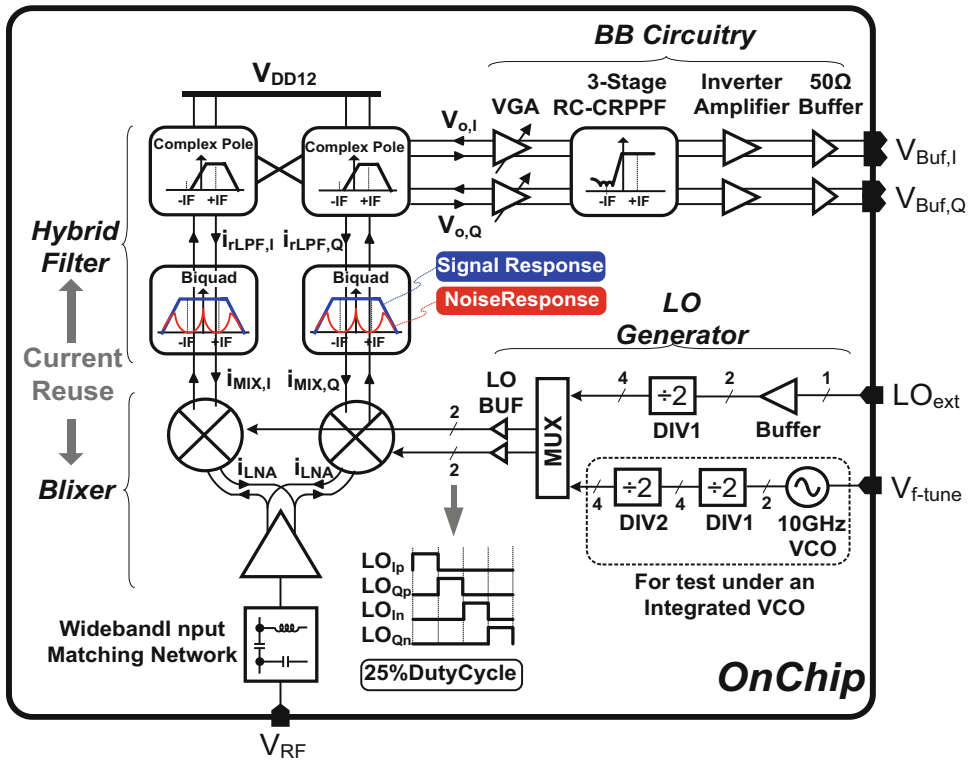

Fig. 14.1 Proposed RF-to-BB-current-reuse ULP 2.4-GHz receiver

final stage is an inverter amplifier before 50-Ω test buffering. The 4-phase 25% LO can be generated by an external 4.8-GHz reference (LO_{ext}) after a divide-by-2 (DIV1) that features 50%-input 25%-output, or from an integrated 10-GHz VCO after DIV1 and DIV2 (25%-input 25%-output) for additional testability.

14.3.1 Circuit Implementation

Wideband Input-Matching Network—As shown in Fig. 14.2a, a low-Q inductor (L_M) and 2 tapped capacitors (C_p and C_M) can be employed for impedance down-conversion resonant and passive pre-gain. A high-Q inductor is unnecessary since the Q of the LC matching is dominated by the low input resistance of the LNA. Thus, a low-Q inductor results in area savings, while averting the need of an external inductor for cost savings. L_M also serves as the bias inductor for M_1. R_p is the parallel shunt resistance of L_M. C_p stands for the parasitic capacitance from the pad and ESD diodes. R_{in} and C_{in} are the equivalent resistance and capacitance at node V_{in}, respectively. R'_{in} is the downconversion resistance of R_{in}.

L_{BW} is the bondwire inductance and R_s is the source resistance. To simplify the analysis, we first omit L_{BW} and C_{in}, so that L_M, C_p, C_M, R_S and R_T ($= R_p//R_{in}$) together form a tapped capacitor facilitating the input matching. Generally, $S_{11} \leq -10$ dB is required and the desired value of R'_{in} is from 26 to 97 Ω over the frequency band of interest. Thus, given the R_T and C_M values, the tolerable C_p can be derived from $R'_{in} = R_T\left(\frac{C_M}{C_M+C_p}\right)^2$. The pre-gain value ($A_{pre,amp}$) from V_{RF} to V_{in} is derived from $\frac{V_{in}^2}{2R_T} = \frac{V_{RF}^2}{2R_S}$, which can be simplified as $A_{pre,amp} = \sqrt{\frac{R_T}{R_S}}$. The –3-dB bandwidth of $A_{pre,amp}$ is related to the

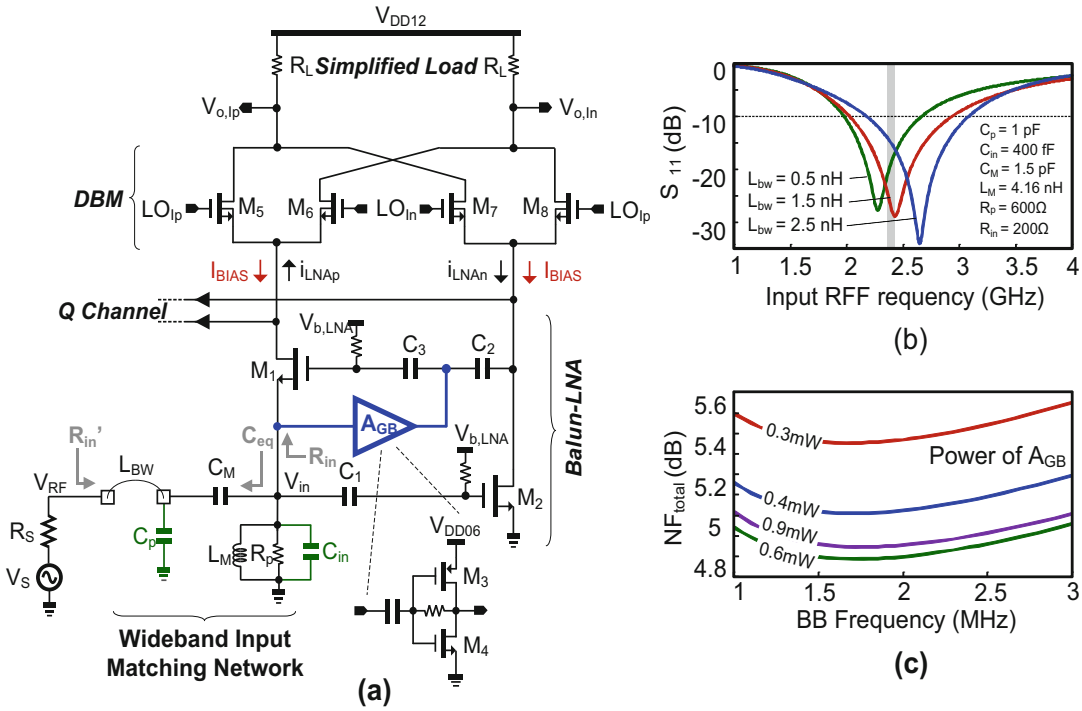

Fig. 14.2 (**a**) Proposed wideband input matching network, balun-LNA and I/Q-DBMs (Q channel is omitted and the load is simplified as R_L). (**b**) Variation of S_{11}-bandwidth with bondwire inductance L_{BW}. (**c**) Power of A_{GB} versus NF

network's quality factor (Q_n) as given by: $Q_n = \frac{R_T}{2\omega_0 L_M} = \frac{\omega_0}{\omega_{-3dB}}$, with $\omega_0 = \frac{1}{\sqrt{L_M C_{EQ}}}$ and $C_{EQ} = \frac{C_M C_p}{C_M + C_p}$.

In our design ($R_T = 150\ \Omega$, $C_M = 1.5$ pF, $L_M = 4.16$ nH, $R_p = 600\ \Omega$, $C_p = 1$ pF and $R_{in} = 200\ \Omega$), $A_{pre,amp}$ has a passband gain of ~4.7 dB over a 2.4-GHz bandwidth (at RF = 2.4 GHz) under a low Q_n of 1. Thus, the tolerable C_p is sufficiently wide (0.37 to 2.1 pF). The low-Q L_M is extremely compact (0.048 mm^2) in the layout and induces a small parasitic capacitance (~260 fF, part of C_{in}). Figure 14.2b demonstrates the robustness of S_{11}-bandwidth against L_{BW} from 0.5 to 2.5 nH. The variation of C_{in} to S_{11}-bandwidth was also studied. From simulations, the tolerable C_{in} is 300 to 500 f. at $L_{BW} = 1.5$ nH.

Balun-LNA—The common-gate (CG) common-source (CS) balun-LNA (Blaakmeer et al. 2008a) avoids the off-chip balun and achieves a low NF by noise canceling, but the asymmetric CG-CS transconductances and loads make the output balancing not wideband consistent. In Blaakmeer et al. (2008b), output balancing is achieved by scaling M_{5-8} with cross-connection at BB, but that is incompatible with this work that includes a hybrid filter. In Mak and Martins (2011), by introducing an AC-coupled CS branch and a differential current balancer (DCB), the same load is allowed for both CS and CG branches for wideband output balancing. Thus, the NF of such a balun-LNA can be optimized independently. This technique is transferred to this ULP design, but only with the I/Q-DBMs inherently serves as the DCB, avoiding a high VDD (Mak and Martins 2011). The detailed schematic is depicted in Fig. 14.2a. To maximize the voltage headroom, M_1 (with $g_{m,CG}$) and M_2 (with $g_{m,CS}$) were sized with non-minimum channel length (L = 0.18 μm) to lower their V_T. The AC-coupled gain stage is a self-biased inverter amplifier (A_{GB}) powered at 0.6-V (V_{DD06}) to enhance its transconductance ($g_{m,AGB}$)-to-current

ratio. It gain-boosts the CS branch while creating a loop gain around M_1 to enhance its effective transconductance under less bias current (I_{BIAS}). This scheme also allows the same I_{BIAS} for both M_1 and M_2, requiring no scaling of load (i.e., only R_L). Furthermore, a small I_{BIAS} lowers the supply requirement, making a 1.2-V supply (V_{DD12}) still adequate for the Blixer and hybrid filter, while relaxing the required LO swing (LO_{IP} and LO_{In}). $C_{1–3}$ for biasing are typical metal-oxide-metal (MoM) capacitors to minimize the parasitics.

The balun-LNA features partial-noise canceling. To simplify the study, we ignore the noise induced by DBM (M_5–M_8) and the effect of channel-length modulation. The noise transfer function (TF) of M_1's noise ($I_{n,CG}$) to the BB differential output ($V_{o,Ip} - V_{o,In}$) can be derived when LO_{Ip} is high, and the input impedance is matched,

$$TF_{I_{n,CG}} = -\frac{1}{2}(R_L - R_{in}G_{m,CS}R_L) \qquad (14.2)$$

where $G_{m,CS} = g_{m,CS} + g_{m,AGB}$. The noise of M_1 can be fully canceled if $R_{in}G_{m,CS} = 1$ is satisfied. However, $R_{in} \approx 200\ \Omega$ is desired for input matching at low power. Thus, $G_{m,CS}$ should be $\approx$5 mS, rendering the noises of $G_{m,CS}$ and R_L still significant. Thus, device sizings for *full* noise cancellation of M_1 should not lead to the lowest total NF (NF_{total}). In fact, one can get a more optimized $G_{m,CS}$ (via $g_{m,AGB}$) for stronger reduction of noise from $G_{m,CS}$ and R_L, instead of that from M_1. Although this noise-canceling principle has been discussed in Bruccoleri et al. (2004) for its single-ended LNA, the output balancing was not a concern there. Here, the optimization process is alleviated since the output balancing and NF are decoupled. The simulated NF_{total} up to the $V_{o,Ip}$ and $V_{o,In}$ nodes against the power given to the A_{GB} is given in Fig. 14.2c. NF_{total} is reduced from 5.5 dB at 0.3 mW to 4.9 dB at 0.6 mW, but is back to 5 dB at 0.9 mW. Due to the use of passive pre-gain and a larger R_p that is ~3 times of R_{in}, the noise contribution of the inductor is <1% from simulations. The simulated NF at the outputs of the LNA and test buffer are 5.3 and 6.6 dB, respectively.

Double-Balanced Mixers Offering Output Balancing—The output balancing is inherently done by the I/Q-DBMs under a 4-phase 25% LO. For simplicity, this principle is described for the I channel only under a 2-phase 50% LO, as shown in Fig. 14.3, where the load is simplified as R_L. During the first-half LO cycle when LO_{Ip} is high, i_{LNAp} goes up and appears at $V_{o,Ip}$ while i_{LNAn} goes down and appears at $V_{o,In}$.

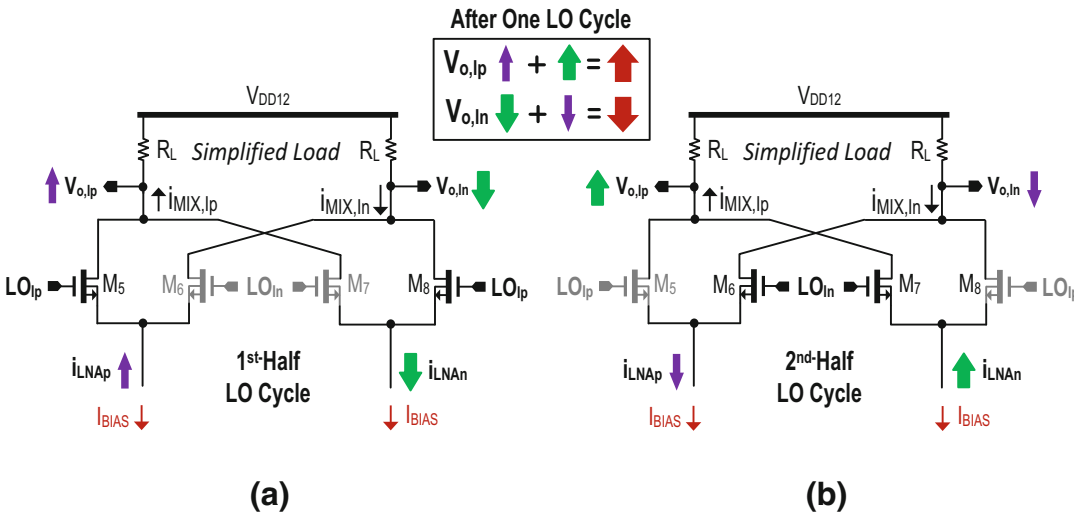

Fig. 14.3 Operation of the I-channel DBM. It inherently offers output balancing after averaging in one LO cycle as shown in their (**a**) 1st-half LO cycle and (**b**) 2nd-half LO cycle

In the second-half LO cycle, both of the currents' sign and current paths of i_{LNAp} and i_{LNAn} are flipped. Thus, when they are summed at the output during the whole LO cycle, the output balancing is robust, thanks to the large output resistance (9 kΩ) of M_5-M_8 enabled by the very small I_{BIAS} (85 μA). To analytically prove the principle, we let $i_{LNAp} = \alpha I_A \cos(\omega_s t + \varphi_1)$ and $i_{LNAn} = -I_A \cos(\omega_s t + \varphi_2)$, where I_A is the amplitude, ω_s is the input signal frequency, α is the unbalanced gain factor and φ_1 and φ_2 are their arbitrary initial phases. When there is sufficient filtering to remove the high-order terms, we can deduce the BB currents $i_{MIX,Ip}$ and $i_{MIX,In}$ as given by,

$$\begin{aligned} i_{MIX,Ip} &= \frac{2}{\pi}\alpha I_A \cos(\omega_s t + \varphi_1) \\ &\times \cos\omega_0 t + \frac{2}{\pi} I_A \cos(\omega_s t + \varphi_2) \times \cos\omega_0 t \\ &= \frac{\alpha I_A}{\pi}\cos(\omega_s t - \omega_0 t + \varphi_1) \\ &+ \frac{I_A}{\pi}\cos(\omega_0 t - \omega_s t + \varphi_2) \end{aligned} \tag{14.3}$$

$$\begin{aligned} i_{MIX,In} &= -\frac{I_A}{\pi}\cos(\omega_s t - \omega_0 t + \varphi_2) \\ &-\frac{\alpha I_A}{\pi}\cos(\omega_0 t - \omega_s t + \varphi_1) \\ &= -i_{MIX,Ip} \end{aligned} \tag{14.4}$$

and a consistent proof for I/Q-DBMs under a 4-phase 25% LO is obtained. Ideally, the DBM can correct perfectly the gain and phase errors from the balun-LNA, independent of its different output impedances from the CG and CS branches. In fact, even if the conversion gain of the 2 mixer pairs (M_5, M_8 and M_6, M_7) does not match (e.g., due to non-50% LO duty cycle), the double-balanced operation can still generate balanced outputs (confirmed by simulations). Of course, the output impedance of the DBM can be affected by that of the balun-LNA [Fig. 14.2a], but is highly desensitized due to the small size of R_L (i.e., the input impedance of the hybrid filter) originally aimed for current-mode operation. Thus, the intrinsic imbalance between $V_{o,Ip}$ and $V_{o,In}$ is negligibly small (confirmed by simulations).

For devices sizing, a longer channel length (L = 0.18 μm) is preferred for M_{5-8} to reduce their 1/f noise and V_t. Hard-switch mixing helps to desensitize the I/Q-DBMs to LO gain error, leaving the image rejection ratio (IRR) mainly determined by the LO phase error that is a tradeoff with the LO-path power. Here, the targeted LO phase error is relaxed to ~4°, as letting the BB circuitry (i.e., the complex-pole load and 3-stage RC-CR PPF) to handle the IRR is more power efficient.

Hybrid Filter 1st Half—Current-Mode Biquad with IF Noise-Shaping—The current-mode Biquad [Fig. 14.4a] proposed in Pirola et al. (2010) is an excellent candidate for current-reuse with the

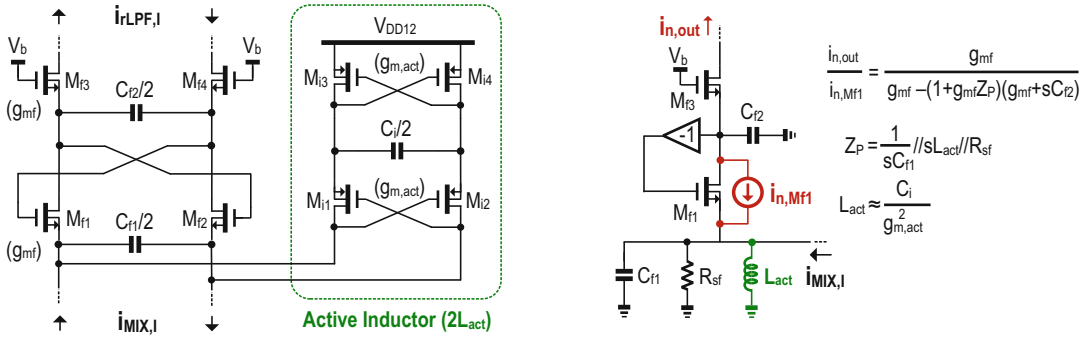

Fig. 14.4 (**a**) Proposed IF-noise-shaping Biquad and (**b**) its small-signal equivalent circuit showing the noise TF of M_{f1}

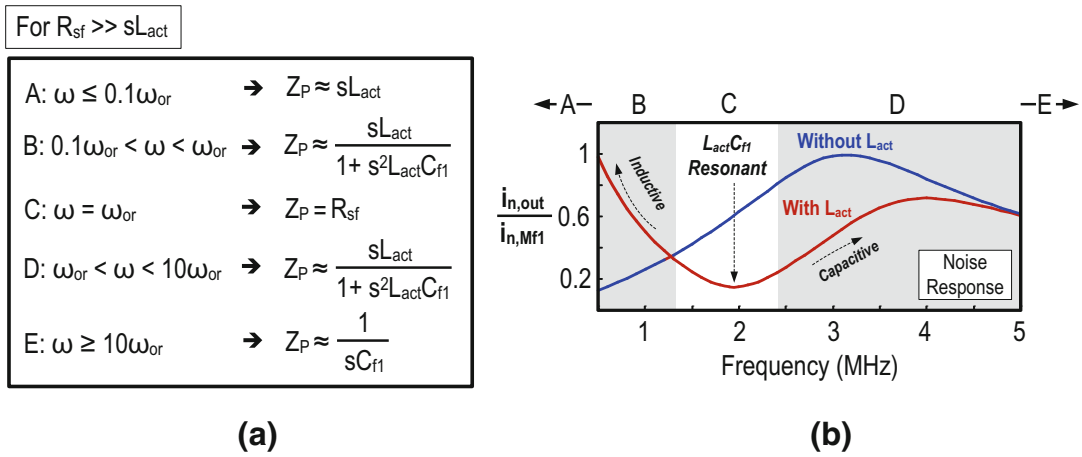

Fig. 14.5 (**a**) Equivalent impedance of Z_P versus ω_{or}, and (**b**) simulated noise TF of $\frac{i_{n,out}}{i_{n,Mf1}}$ with and without L_{act}

Blixer for channel selection. However, this Biquad only can generate a noise-shaping zero spanning from DC to $\sim 2\pi 0.1Q_B\omega_{0B}$ MHz for M_{f1}–M_{f2}, where Q_B and ω_{0B} are the Biquad's quality factor and –3-dB cutoff frequency, respectively. This noise shaping is hence ineffective for our low-IF design having a passband from ω_1 to ω_2 (= ω_{0B}), where $\omega_1 > 0.1Q_B\omega_{0B}$. To address this issue, an active inductor (L_{act}) is added at the sources of M_{f1}–M_{f2}. The $L_{act}C_{f1}$ resonator shifts the noise-shaping zero to the desired IF. The cross-diode connection between M_{i1}–M_{i4} (all with $g_{m,act}$) emulate $L_{act} \approx C_i/g_{m,act}{}^2$ (Ler et al. 2008; Chen et al. 2012). The small-signal equivalent circuit to calculate the noise TF of $i_{n,Mf1}/i_{n,out}$ is shown in Fig. 14.4b. The approximated impedance of Z_P in different frequencies related to ω_{0r} is summarized in Fig. 14.5a, where $\omega_{0r} = \frac{\omega_1+\omega_2}{2}$ is the resonant frequency of $L_{act}C_{f1}$ at IF. The simulated $i_{n,Mf1}/i_{n,out}$ is shown in Fig. 14.5b. At the low frequency range, Z_P behaves inductively, degenerating further $i_{n,Mf1}$ when the frequency is increased. At the resonant frequency, $Z_P = R_{sf}$, where R_{sf} is the parallel impedance of the active inductor's shunt resistance and DBM's output resistance. The latter is much higher when compared with R_L thereby suppressing $i_{n,Mf1}$. At the high frequency range, Z_P is more capacitive dominated by C_{f1}. It implies $i_{n,Mf1}$ can be leaked to the output via C_{f1}, penalizing the

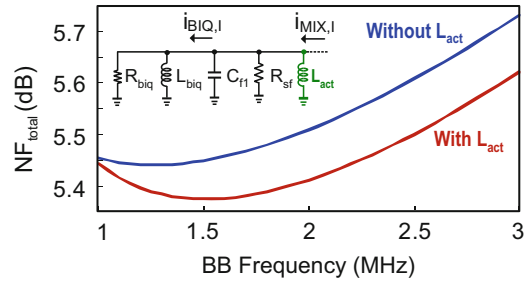

Fig. 14.6 Simulated NF_{Total} (at $V_{o,Ip}$ and $V_{o,In}$) with and without L_{act}

in-band noise. At even higher frequencies, the output noise decreases due to C_{f2}, being the same as its original form (Pirola et al. 2010).

The signal TF can be derived from Fig. 14.6. Here $R_L = \frac{1}{g_{mf}}$, $L_{biq} = \frac{C_{f2}}{g_{mf}^2}$. For an effective improvement of NF, $L_{act} \gg L_{biq}$ should be made. The simulated NF_{total} at $V_{o,Ip}$ and $V_{o,In}$ with and without the L_{act} is shown Fig. 14.6, showing about 0.1 dB improvement at the TT corner (reasonable contribution for a BB circuit). For the SS and FF corners, the NF improvement reduces to 0.04 and 0.05 dB, respectively. These results are expected due to the fact that at the FF corner, the noise contribution of the BB is less significant due to a larger bias current; while at the SS corner, the IF noise-shaping circuit will add more noise by itself, offsetting the NF improvement. Here M_{f1}–M_{f4} use isolated P-well

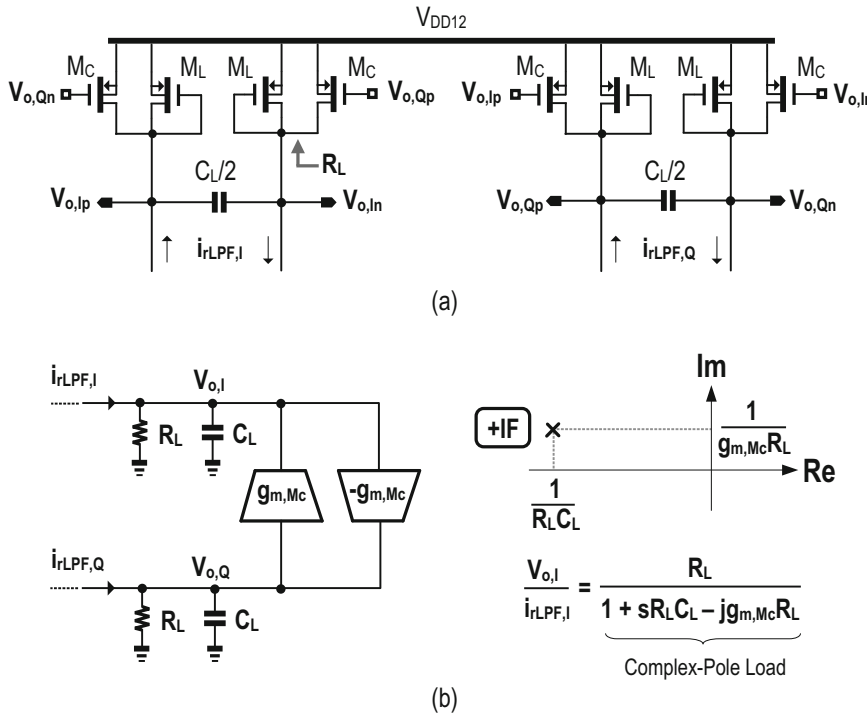

Fig. 14.7 (**a**) Proposed complex-pole load and (**b**) its small-signal equivalent circuit and pole plot

for bulk-source connection, avoiding the body effect while lowering their V_T.

Hybrid Filter 2nd Half—Complex-Pole Load—Unlike most active mixers or the original Blixer (Blaakmeer et al. 2008a, b) that only use a RC load, the proposed "load" synthesizes a 1st-order complex pole at the positive IF (+IF) for channel selection and image rejection. The circuit implementation and principle are shown in Fig. 14.7a and b, respectively. The real part (R_L) is obtained from the diode-connected M_L, whereas the imaginary part ($g_{m,Mc}$) is from the I/Q-cross-connected M_C. The entire hybrid filter offers 5.2-dB IRR, and 12-dB (29-dB) adjacent (alternate) channel rejection as shown in Fig. 14.8 (the channel spacing is 5 MHz). Similar to g_m-C filters the center frequency is defined by $g_{m,Mc}R_L$. When sizing the –3-dB bandwidth, the output conductances of M_C and M_L should be taken into account.

Current-Mirror VGA and RC-CR PPF—Outside the current-reuse path, $V_{o,I}$ and $V_{o,Q}$ are AC-coupled to a high swing current-mirror

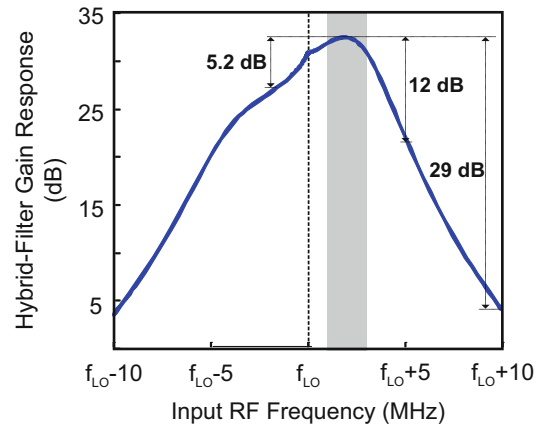

Fig. 14.8 Simulated hybrid-filter gain response

VGA formed with M_L [Fig. 14.7a] and a segmented M_{VGA} (Fig. 14.9), offering gain controls with a 6-dB step size. To enhance the gain precision, the bias current through M_{VGA} is kept constant, so as its output impedance. With the gain switching of M_{VGA}, the input-referred noise of M_{VGA} will vary. However, when the RF signal

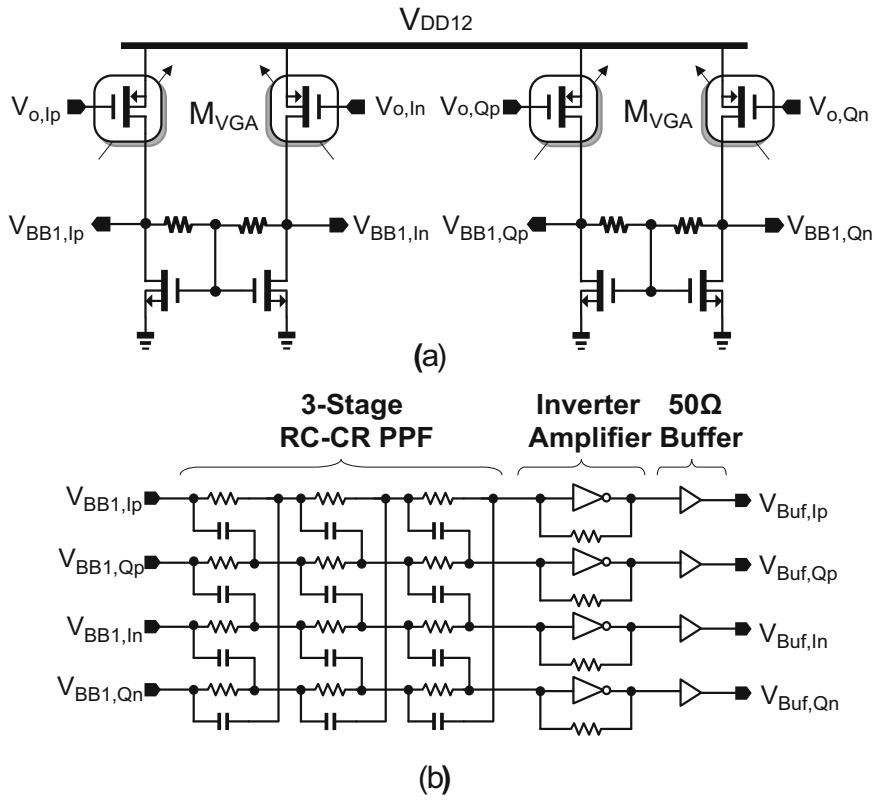

Fig. 14.9 Schematics of the BB (**a**) VGA, and (**b**) 3-stage RC-CR PPF, inverter amplifier and 50-Ω buffer

level is low the gain of the VGA should be high, rendering the gain switching not influencing the receiver's sensitivity. The VGA is responsible for compensating the gain loss (30 dB) of the 3-stage passive RC-CR PPF that provides robust image rejection of >50 dB (corner simulations). With the hybrid filter rejecting the out-band blockers the linearity of the VGA is further relaxed, so as its power budget (192 μW, limited by the noise and gain requirements).

A 3-stage RC-CR PPF can robustly meet the required IRR in the image band (i.e., the –IF), and cover the ratio of maximum to minimum signal frequencies (Kaykovuori et al. 2008; Behbahani et al. 2001). In our design, the expected IRR is 30 to 40 dB and the ratio of frequency of the image band is f_{max}/f_{min} (=3). However, counting the RC variations as large as ±25%, the conservative $\Delta f_{eff} = f_{max\_eff}/f_{min\_eff}$ should be close to 5. The selected RC values are guided by Behbahani et al. (2001)

$$\frac{\sigma(\text{Image Out})}{\text{Desired Out}} = 0.25\sqrt{\left(\frac{\sigma_R}{R}\right)^2 + \left(\frac{\sigma_C}{C}\right)^2} \tag{14.5}$$

Accordingly, the matching of the resistors (σ_R) and capacitors (σ_C) can be relaxed to 0.9% (2.93%) for 40-dB (30-dB) IRR with a 3σ yield. Here, ~150-kΩ resistors are chosen to ease the layout with a single capacitor size (470 fF), balancing the noise, area and IRR. The simulated worst IRR is 36 dB without LO mismatch, and still over 27 dB at a 4° LO phase error checked by 100x Monte-Carlo simulations. Furthermore, if the 5-dB IRR offered by the complex-pole load is added the minimum IRR of the IF chain should be 32 dB. The final stage before 50-Ω output buffering is a self-biased inverter amplifier (power = 144 μW), which embeds one more real pole for filtering. The simulated overall IF gain response is shown in Fig. 14.10, where the notches at DC offered by the AC-coupling

network, and around the –IF offered by the 3-stage RC-CR PPF, are visible. The IRR is about 57 dB [=52 dB (RC-CR PPF) + 5 dB (complex-pole load)] under an ideal 4-phase 25% LO for the image band from [f_{LO} – 3, f_{LO} – 1] MHz.

VCO and Dividers and LO Buffers—To fully benefit the speed and low-V_t advantages of fine linewidth CMOS, the entire LO path is powered at a lower supply of 0.6 V to reduce the dynamic power. For additional testability, an on-chip VCO is integrated. It is optimized at ~10 GHz to save area and allows division by 4 for I/Q generation. The loss of its LC tank is compensated by complementary NMOS-PMOS negative transconductors.

The divider chain [Fig. 14.11a] cascades two types of div-by-2 circuits (DIV1 and DIV2) to generate the desired 4-phase 25% LO, from a 2-phase 50% output of the VCO. The two latches (D1 and D2) are employed to build DIV1 that can directly generate a 25% output from a 50% input (Razavi et al. 1995), resulting in power savings due to less internal logic operation (i.e., AND gates) and load capacitances. Each latch consists of two sense devices, a regenerative loop and two pull up devices. For 25%-input 25%-output division, DIV2 is proposed that it can be directly interfaced with DIV1. The 25% output of DIV1 are combined by M_{D1} to M_{D4} to generate a 50% clock signal for D3 and D4.

For testing under an external LO_{ext} source at 4.8 GHz, another set of D1 and D2 is adopted. The output of these two sets of clocks are combined by transmission gates and then selected. Although their transistor sizes can be reduced aggressively to save power, their drivability and robustness in process corners can be degraded. From simulations, the sizing can be properly optimized. The four buffers ($Buf_{1–4}$) serve to reshape the pulses from DIV2 and enhance the

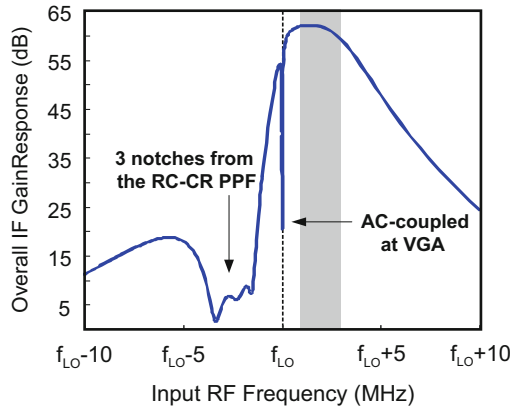

Fig. 14.10 Simulated overall IF gain response

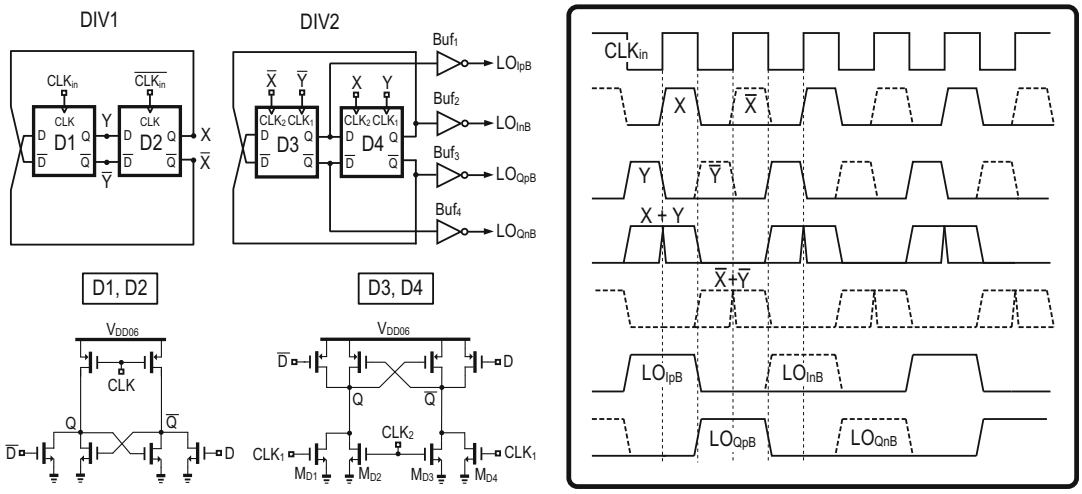

Fig. 14.11 (**a**) Schematics of DIV1 and DIV2, and (**b**) their timing diagrams

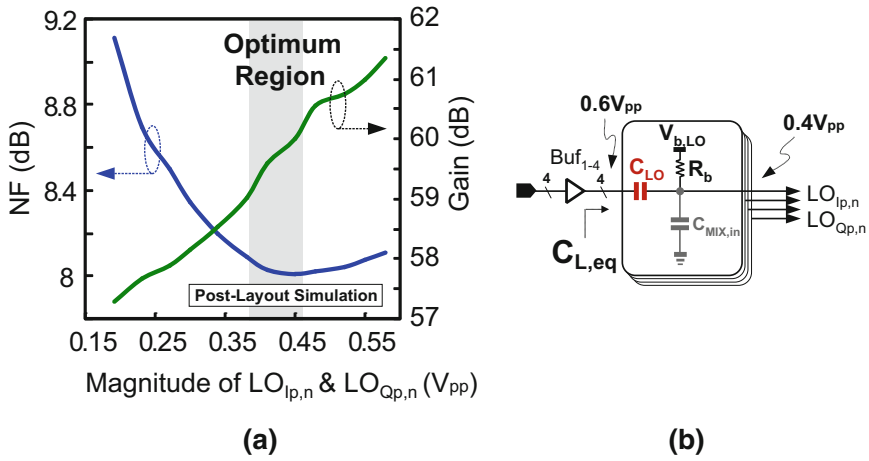

Fig. 14.12 (**a**) Post-layout simulation of NF and gain versus LO's amplitude, and (**b**) additional C_{LO} generates the optimum LO's amplitude

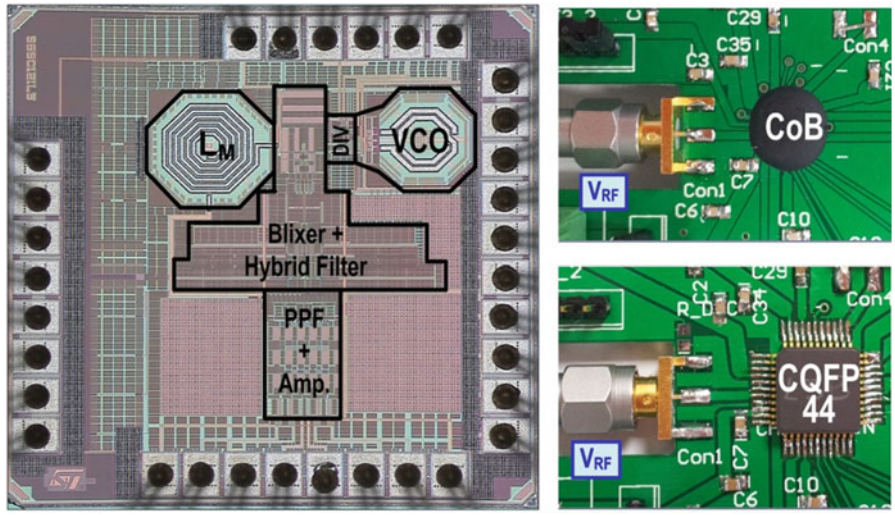

Fig. 14.13 Chip micrograph of the receiver. It was tested under CoB and CQFP44 packaging. No external component is entailed for input matching

drivability. The timing diagram is shown in Fig. 14.11b. Due to the very small I_{BIAS} for the I/Q-DBMs, a LO amplitude of around 0.4 V_{pp} is found to be more optimized in terms of NF and gain as simulated and shown in Fig. 14.12a. To gain benefits from it C_{LO} is added to realize a capacitor divider with $C_{MIX,in}$ (input capacitance of the mixer) as shown in Fig. 14.12b. This act brings down the equivalent load ($C_{L,eq}$) of $Buf_{1–4}$ by ~33%.

14.3.2 Experimental Results

The ZigBee receiver was fabricated in 65-nm CMOS (Fig. 14.13) and optimized with dual supplies (1.2 V: Blixer + hybrid filter, 0.6 V: LO and BB circuitries). The die area is 0.24 mm^2 (0.3 mm^2) without (with) counting the LC-tank VCO. Since there is no frequency synthesizer integrated, the results in Fig. 14.14a–d were measured under LO_{ext} for accuracy and data

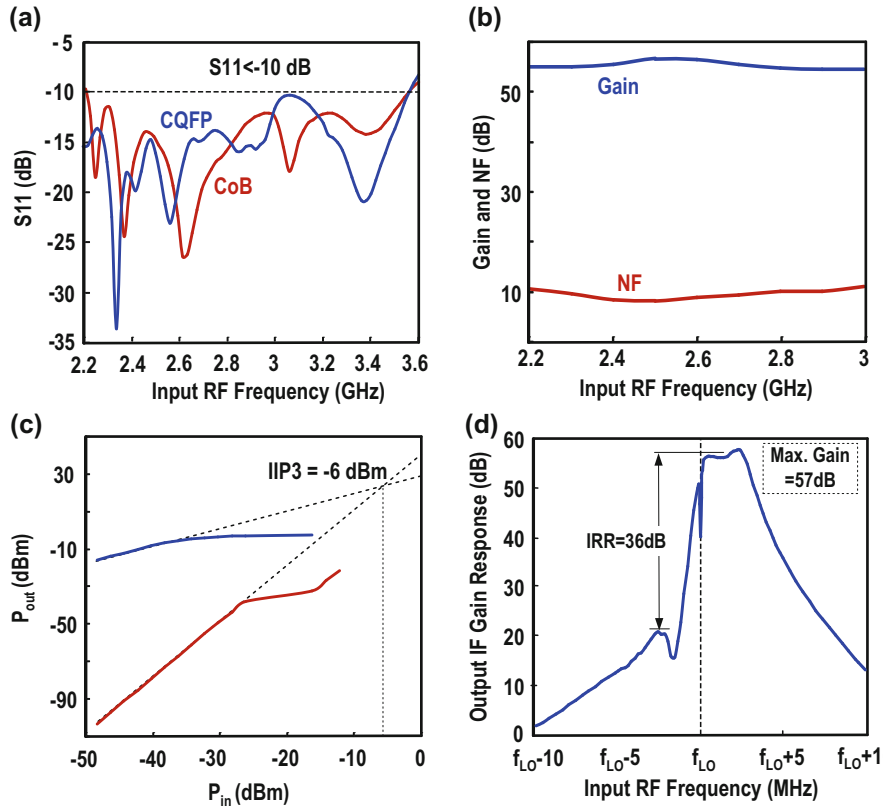

Fig. 14.14 Measured (**a**) S_{11}, (**b**) wide band gain and NF, (**c**) $IIP3_{out\text{-}band}$, and (**d**) low-IF filtering profile

repeatability. The S_{11}-BW (<–10 dB) is ~1.3 GHz for both chip-on-board (CoB) and CQFP-packaged tests [Fig. 14.14a], which proves its immunity to board parasitics and packaging variations. The gain (55–57 dB) and NF (8.3–11.3 dB) are also wideband consistent [Fig. 14.14b]. The gain peak at around 2.4–2.5 GHz is from the passive pre-gain. Following the linearity test profile of Tedeschi et al. (2010), two tones at [LO + 12 MHz, LO + 22 MHz] are applied, measuring an $IIP3_{out\text{-}band}$ of –6 dBm [Fig. 14.14c] at the maximum gain of 57 dB (there is 24-dB gain loss in Fig. 14.14c associated with the test buffer and used 1:8 transformer). This high IIP3 is due to the direct current-mode filtering at the mixer's output before signal amplification. The asymmetric IF response [Fig. 14.14d] shows 22-dB (43-dB) rejection at the adjacent (alternate) channel, and 36-dB IRR. Differing from the simulated IF frequency response that has three notches at the image band under an ideal LO, the measured notches are merged. Similar to Behbahani et al. (2001), this discrepancy is likely due to the LO gain and phase mismatches, and the matching and variations of the RC-CR networks. The layout design is similar to Behbahani et al. (2001) that uses dummy to balance the parasitic capacitances. The filtering rejection profile is ~80 dB/decade. The spurious free dynamic range (SFDR) is close to 60 dB according to Tedeschi et al. (2010),

$$\mathrm{SFDR} = \frac{2(\mathrm{P_{IIP3}} + 174\mathrm{dBm} - \mathrm{NF} - 10\log\mathrm{BW})}{3} - \mathrm{SNR_{min}} \tag{14.6}$$

where $\mathrm{SNR_{min}} = 4$ dB is the minimum signal-to-noise ratio required by the application, and BW = 2 MHz is the channel bandwidth.

The receiver was further tested at lower voltage supplies as summarized in Table 14.2. Only the NF degrades more noticeably, the IIP3, IRR and BB gain are almost secured. The better IIP3 for 0.6-V/1-V operation is mainly due to the narrower –3-dB bandwidth of the hybrid filter. For the 0.5-V/1-V operation, the degradation of $IIP3_{out\text{-}band}$ is likely due to the distortion generated by A_{GB}. Both cases draw very low power down to 0.8 mW, being comparable with other ULP designs such as Herberg et al. (2011).

The LC-tank VCO was tested separately. Its power budget is related with its output swing and is a tradeoff with the phase noise, which measures—114 dBc/Hz at 3.5 MHz that has an enough margin to the specifications (Liscidini et al. 2008) [Fig. 14.15a]. Porting it to the simulation results, it can be found that the corresponding VCO's output swing is 0.34 V_{pp} and the total LO-path power is 1.7 mW (VCO + dividers + BUFs). Such an output swing is adequate to lock DIV1 as shown in its simulated sensitivity curve [Fig. 14.15b].

The chip summary and performance benchmarks are given in Table 14.3, where (Tedeschi et al. 2010) is a current-reuse architecture and (Zhang et al. 2013) is an ultra-low-voltage design. For this work, the results measured under a 10-GHz on-chip VCO are also included for completeness, but they are more sensitive to test uncertainties. The degraded NF and IRR are mainly due to the phase noise of the free-running VCO. In both cases, this work succeeds in advancing the $IIP3_{out\text{-}band}$, power and area efficiencies, while achieving a wideband S_{11} with zero external components. Particularly,

Table 14.2 Key performances of the receiver at different supply voltages

Supply voltage (V)	0.6/1.2	0.6/1	0.5/1
Power (mW)	1.7	1.2	0.8
Gain (dB)	57	58	57.5
$IIP3_{out\text{-}band}$ (dBm)	−6	−4	−8
NF (dB)	8.5	11.3	12
IRR (dB)	36	38	35

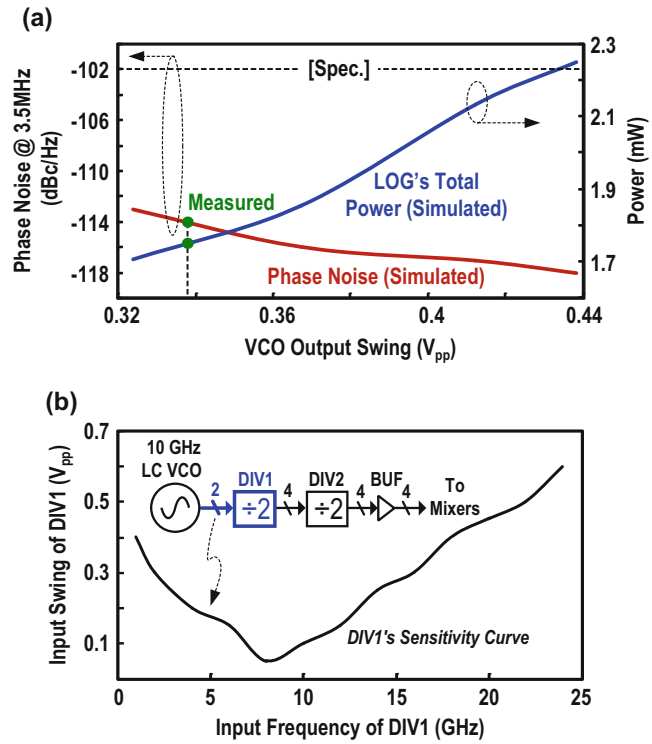

Fig. 14.15 (**a**) The measured phase noise has enough margin to the specifications. From simulations, it can be shown that it is a tradeoff with the power budget according to the VCO's output swing. (**b**) Simulated sensitivity curve of DIV1 showing its small input-voltage requirement at ~10 GHz

Table 14.3 Performance summary and benchmark with the state-of-the-art

	This work (Lin et al. 2013, 2014a)		JSSC '10 (Tedeschi et al. 2010)	ISSCC '13 (Zhang et al. 2013)
Application	ZigBee		ZigBee	Energy Harvesting
Architecture	Blixer + Hybrid-Filter + Passive RC-CR PPF		LMV Cell + Complex Filter	LNA + Mixer + Frequency-translated IF Filter
BB Filtering	***1 Biquad + 4 complex poles***		3 complex poles	2 real poles
External I/P matching components	***zero***		1 inductor, 1 capacitor	2 capacitors, 1 inductor
$S_{11} < -10$ dB Bandwidth (MHz)	***1300 (2.25 to 3.55 GHz)***		<300 (2.3 to 2.6 GHz)	>600 (<2 to 2.6 GHz)
Integrated VCO	No	Yes	Yes	Yes
Gain (dB)	57	55	75	83
Phase Noise (dBc/Hz)	NA	−115 @ 3.5 MHz	−116 @ 3.5 MHz	−112.8 @ 1 MHz
NF (dB)	8.5	9	9	6.1
$IIP3_{out\text{-}band}$ (dBm)	***−6***	***−6***	−12.5	−21.5
IRR (dB)	36 (worst of 5 chips)	28	35	N/A
SFDR (dB)	***60.3***	***60***	55.5	51.6
LO-to-RF Leak (dBm)	−61	−61	−60	N/A
Power (mW)	***1.7***[a]	***2.7***	3.6	1.6
Active Area (mm^2)	***0.24***	***0.3***	0.35	2.5
Supply Voltage (V)	0.6/1.2		1.2	0.3
Technology	65 nm CMOS		90 nm CMOS	65 nm CMOS

[a]Breakdown: 1 mW: Blixer + hybrid filter + BB circuitry, 0.7 mW: DIV1 + LO Buffers

when comparing with the recent work (Zhang et al. 2013), this work achieves 8x less area and 15.5 dBm higher IIP3, together with stronger BB channel selectivity.

14.4 Function-Reuse ULP Receiver Techniques for the Sub-GHz ISM Bands

Differing from the previous design that is for single band, the function-reuse receiver (Lin et al. 2014b, c) to be described here can flexibly support multiple bands (433/860/915/960 MHz) and can operate at a single low VDD. It features a gain-boosted N-path switched-capacitor (SC) network embedded into a function-reuse RF front-end, offering concurrent RF (common-mode) and BB (differential-mode) amplification, LO-defined RF filtering, and input impedance matching with zero external components. The details are presented next.

14.4.1 Receiver Architecture

Specifically, the gain-boosted 4-path SC network [Fig. 14.16a] separates the output of each gain stage G_m (G_m has a transconductance of g_{m3}, output resistance of $4R_{L,}$ and feedback resistor of R_{F3}) with capacitor C_o that is an open circuit at BB. The I/Q BB signals at $V_{B1,I\pm}$ and $V_{B1,Q\pm}$ are further amplified along the Path C [Fig. 14.16b] by each G_m stage. With the memory effect of the capacitors, the functional view of the gain response is shown in Fig. 14.16c. In order to achieve current-reuse between the RF LNA and BB amplifiers without increasing the VDD, the circuit published in Han and Gharpurey (2008) with an active mixer has a similar function. However, the BB NF behavior and the RF filtering behavior are different from the N-path passive mixer applied here that is at the feedback path. For the BB amplifiers, it is one G_m with one R_{F3}, balancing the BB gain and OB-IIP3. After considering that the BB amplifiers have been

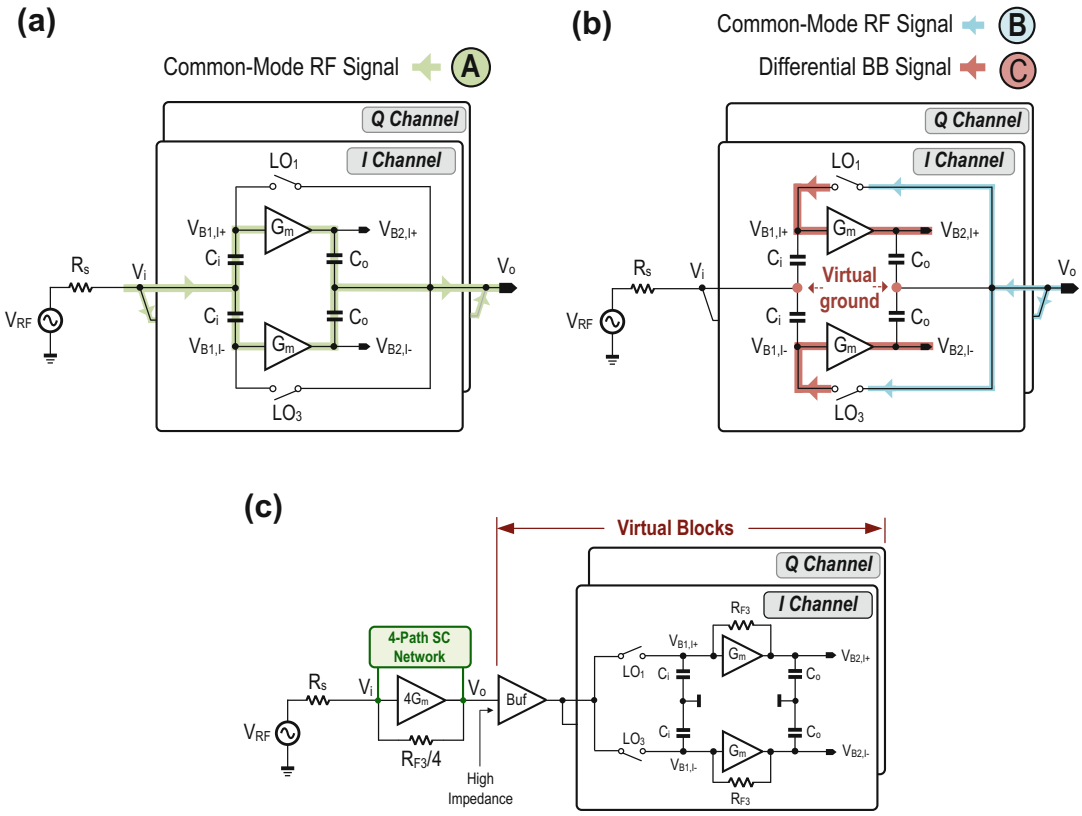

Fig. 14.16 (**a**) Function-reuse receiver embedding a gain-boosted 4-path SC network and its operation for RF signal, (**b**) BB signals and (**c**) its functional view to model the gain response

absorbed in the LNA, the I/Q passive mixers and capacitors absorbed by the 4-path SC network, the blocks after the LNA can be assumed virtual. These virtual blocks reduce the power, area and NF. To validate the above viewpoint, the gain and noise performances under two sets of R_{F3} are simulated. Here, the virtual blocks in Fig. 14.16c are implemented with physical transistors and capacitors for the BB amplifiers and the mixers while the buffer is ideal. Thus, the power of the modeled receiver is at least 2x larger than the proposed receiver. For the IB BB gain at $V_{B2,I\pm}$ ($V_{B2,Q\pm}$) between the proposed function-reuse receiver and its functional view, the difference is only 1 dB at a large R_{F3} of 150 kΩ [Fig. 14.17a]. For a small R_{F3}, the gain error goes up to 2 dB [Fig. 14.17b], which is due to the gain difference between the model of the N-path tunable LNA [Fig. 14.16c] and the implementation of the function-reuse receiver that has AC-coupling. For the NF difference (ΔNF), with a large (small) R_{F3}, it is ~0.8 dB (3.5 dB) as compared in Fig. 14.18a, b. This is due to the lower gain at the LNA's output, forcing the input-referred noise from the downconversion passive mixers and the BB amplifiers to increase with a small R_{F3}. Either with a small or large R_{F3}, it is noteworthy that the variation of BB NF is small (i.e., for $R_{F3} = 20$ kΩ it is 3.6 dB while for $R_{F3} = 150$ kΩ it is 3.4 dB), because the BB NTF has a weak relation with R_{F3}. It also indicates that the BB NTF is weakly related with the gain at the LNA's output, which is dissimilar to the usual receiver where the NF should be small when the LNA's gain is large. Similarly, the NF at the LNA's output (now shown) can be larger than that at BB due to the different NTFs.

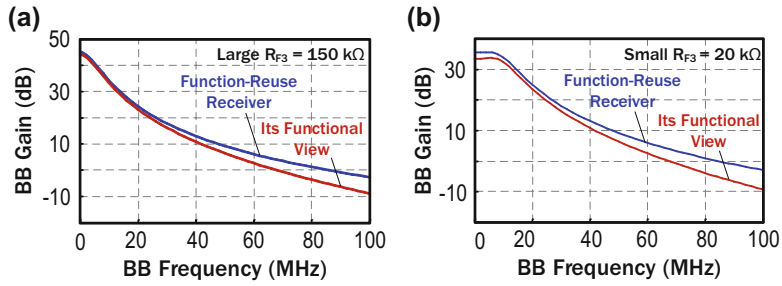

Fig. 14.17 Simulated BB gain response of the function-reuse receiver and its functional view with (**a**) a large R_{F3} and (**b**) a small R_{F3}

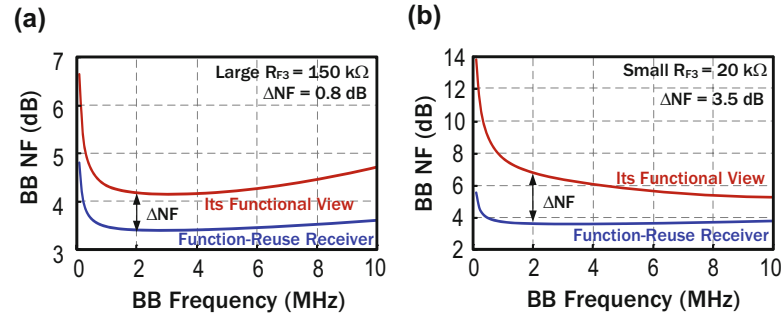

Fig. 14.18 Simulated BB NF of the function-reuse receiver and its functional view with (**a**) a large R_{F3} and (**b**) a small R_{F3}

14.4.2 Low-Voltage Current-Reuse VCO-Filter

In order to further optimize the power, the VCO is designed to current-reuse with the BB complex low-IF filter (Fig. 14.19). The negative transconductor of the VCO is divided into multiple M_v cells. The aim is to distribute the bias current of the VCO to all BB gain stages (A_1, $A_2 \ldots A_{18}$) that implement the BB filter. For the VCO, M_V operates at the frequency of $2f_s$ or $4f_s$ for a div-by-2 or div-by-4 circuit. Thus, the VCO signal leaked to the source nodes of M_V ($V_{F1,I+}$, $V_{F1,I-}$) is pushed to very high frequencies ($4f_s$ or $8f_s$) and can be easily filtered by the BB capacitors. For the filter's gain stages such as A_1, M_b (g_{Mb}) is loaded by an impedance of ~$1/2g_{Mv}$ when L_p can be considered as a short circuit at BB. Thus, A_1 has a ratio-based voltage gain of roughly g_{Mb}/g_{Mv}, or as given by $4Tg_{Mb}/G_{mT}$, where G_{mT} is the total trans-conductance for the VCO tank. The latter shows how the distribution factor T can enlarge the BB gain, but is a tradeoff with its input-referred noise and can add more layout parasitics to $V_{vcop,n}$ (i.e., narrower VCO's tuning range). The –R cell using cross-coupled transistors is added at $V_{F1,I+}$ and $V_{F1,I-}$ to boost the BB gain without loss of voltage headroom. For the BB complex poles, $A_{2,5}$ and C_{f1} determine the real part while $A_{3,6}$ and C_{f1} yield the imaginary part. There are three similar stages cascaded for higher channel selectivity and image rejection ratio (IRR). R_{blk} and C_{blk} were added to avoid the large input capacitance of $A_{1,4}$ from degrading the gain of the front-end.

14.4.3 Experimental Results

Two versions of the receiver were fabricated in 65-nm CMOS (Fig. 14.20) and optimized with a single 0.5-V VDD. With (without) the LC tank for the VCO, the die area is 0.2 mm^2 (0.1 mm^2). Since the measurement results of both are similar, only those measured with VCO in Fig. 14.21a–d are reported here. From 433 to 960 MHz, the measured BB gain is 50 ± 2 dB. Two tones at [f_s + 12 MHz, f_s + 22 MHz] are applied, measuring an OB-IIP3 of –20.5 ± 1.5 dBm at the maximum gain. The IRR is

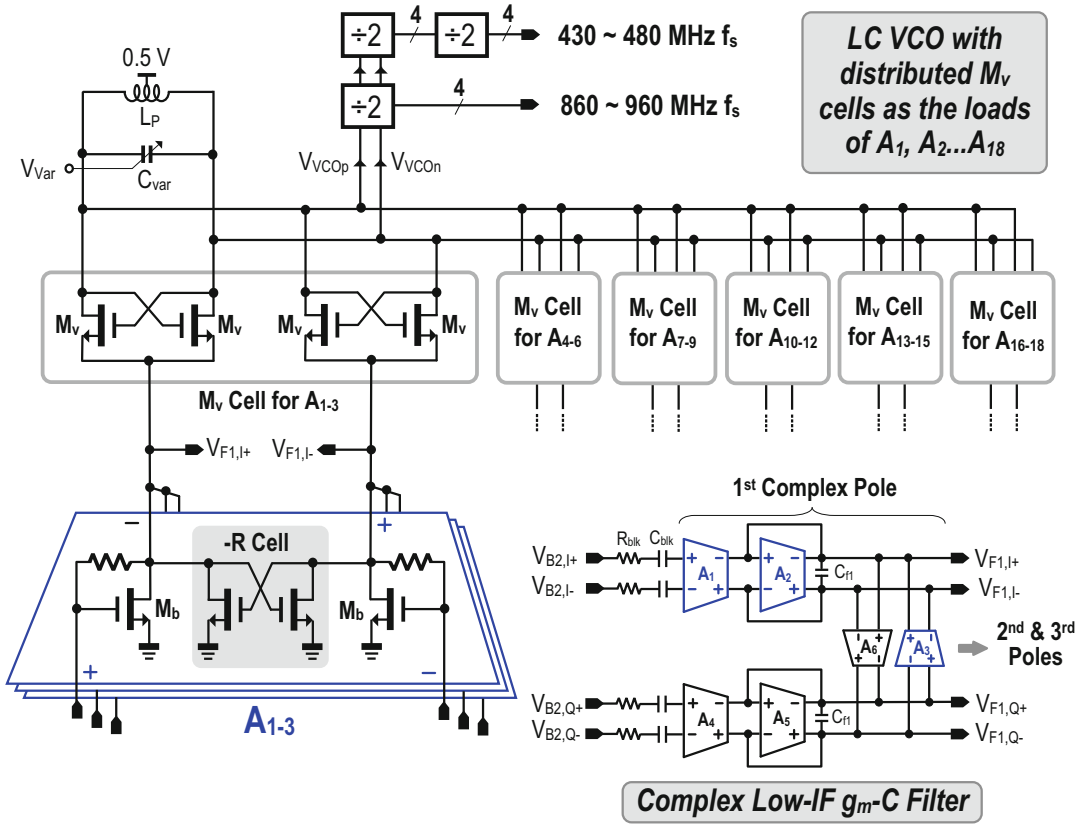

Fig. 14.19 Proposed low-voltage current-reuse VCO-filter

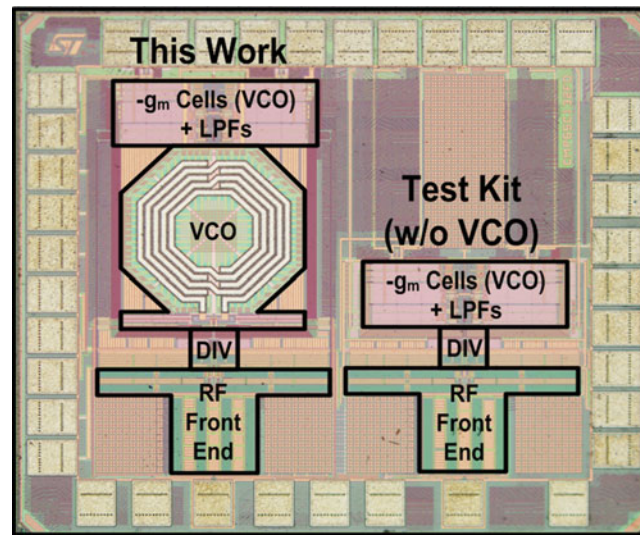

Fig. 14.20 Chip micrograph of the function-reuse receiver with a LC-tank for the VCO (*left*) and without it (*right*)

20.5 ± 0.5 dB due to the low-Q of the VCO-filter. The IIP3 is mainly limited by the VCO-filter. The measured NF is 8.1 ± 0.6 dB. Since the VCO is current-reuse with the filter, it is interesting to study its phase noise with the BB signal amplitude. For negligible phase noise

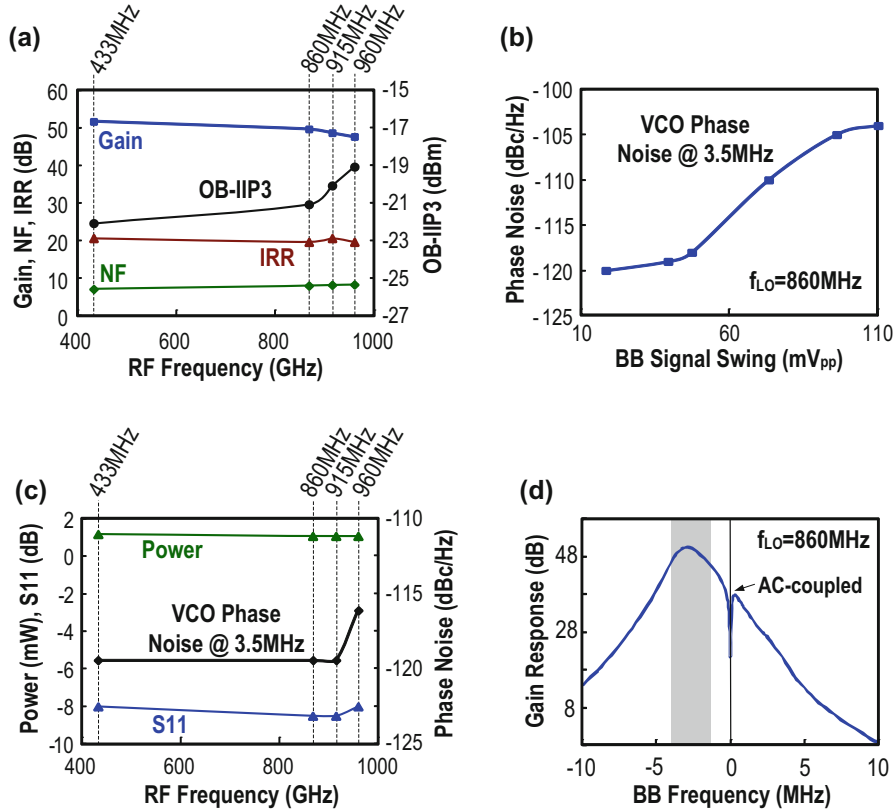

Fig. 14.21 Measured key performance metrics: (**a**) Gain, NF, IRR and OB-IIP3. (**b**) VCO phase noise versus BB signal swing. (**c**) S11, power and VCO phase @ 3.5-MHz offset. (**d**) BB complex gain response centered at –2-MHz IF

degradation, the BB signal swing should be <60 mV_{pp}, which can be managed by variable gain control. If a 60-mV_{pp} BB signal is insufficient for demodulation, a simple gain stage (e.g., inverter amplifier) can be added after the filter to enlarge the gain and output swing. The total power of the receiver is 1.15 mW (0.3 mW for the LNA + BB amplifiers and 0.65 mW for VCO-filter and 0.2 mW for the divider), while the phase noise is –117.4 ± 1.7 dBc/Hz at 3.5-MHz frequency offset. The S_{11} is below –8 dB across the whole band. The asymmetric IF response shows 24-dB (41-dB) rejection at the adjacent (alternate) channel.

To study the RF filtering behavior, the P_{1dB} and blocker NF are measured. For the in-band signal, the P_{1dB} is –55 dBm while with a frequency offset frequency of 20 MHz, it increases to –35 dBm, which is mainly due to the double-RF filtering [Fig. 14.22a]. For an offset frequency of 60 MHz, the P_{1dB} is –20 dBm, limited by the current-reuse VCO-filter. For the blocker NF, with a single tone at 50 MHz, the blocker NF is almost unchanged for the blocker <–35 dBm. With a blocker power of –20 dBm, the NF is increased to ~14 dB [Fig. 14.22b].

This work is compared with the prior art in Table 14.4, where (Lin et al. 2013) is the current-reuse architectures described previously, while (Zhang et al. 2013) is the cascade architecture with ULV supply for energy harvesting. For this work, the results measured under an external LO are also included for completeness. In both cases, this work succeeds in advancing the power and area efficiencies with multi-band convergence, while achieving tunable S_{11} with zero external components. When comparing with the most recent ULV design (Zhang et al. 2013), this

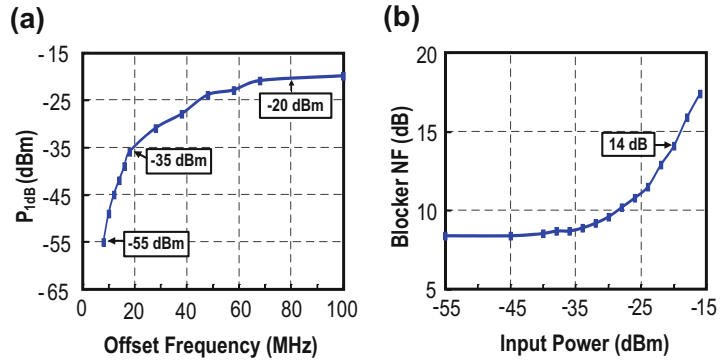

Fig. 14.22 Measured (**a**) P_{1dB} versus input offset frequency and (**b**) blocker NF versus input power

Table 14.4 Performance summary and benchmark with the state-of-the-art RXs

	This work (Lin et al. 2014b)	ISSCC '13 (Lin et al. 2013)	ISSCC '13 (Zhang et al. 2013)
Application	**433/860/915/960 MHz (ZigBee/IEEE802.15.4c/d)**	2.4 GHz (ZigBee/IEEE 802.15.4)	2.4 GHz (Energy Harvesting)
Architecture	Function-Reuse RF Front-End + N-path Tunable LNA + Current-Reuse VCO-Filter	Blixer + Hybrid Filter + Passive RC-CR Filter + LC VCO	CG LNA + Passive Mixers + N-Path SC IF Filter + LC VCO
BB Filter	3 complex poles	1 Biq., 4 complex poles	2 real poles
Input matching technique	**On-chip N-path SC (tunable by LO, high Q)**	On-chip LC (fixed, low Q)	Off-chip LC (fixed, low Q)
External components	**zero**	zero	2 caps, 1 inductor
Input matching BW and tunability	**433 to 960 MHz (tunable by LO)**	2.25 to 3.55 GHz (fixed)	~2 to 2.6 GHz (fixed)
Active Area (mm^2)	**0.2 (0.1[a])**	0.3	2.5
Power (mW) @V_{DD}	**1.15 ± 0.05 @ 0.5 V**	2.7 @ 0.6/1.2 V	1.6 @ 0.3 V
Gain (dB)	50 ± 2 (51 ± 3[a])	55	83
NF (dB)	8.1 ± 0.6 (8 ± 1[a])	9	6.1
OB-IIP3 (dBm)	−20.5 ± 1.5 (−23 ± 1[a])	−6	−21.5
IRR (dB)	20.5 ± 0.5 (21 ± 0.5[a])	28	N/A
VCO Phase Noise (dBc/Hz)	−117.4 ± 1.7 @ 3.5 MHz	−115 @ 3.5 MHz	−112 @ 1 MHz
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS

[a]Results measured from the test kit that has no VCO

work saves more than 10x of area while supporting multi-band operation with zero external components.

14.5 Sub-1 V ULP 2.4GHz Transmitter

This section briefly covers an ongoing-design of a sub-1 V ULP 2.4-GHz transmitter (TX) with scalable output power (P_{out}) and system efficiency for ZigBee and other Internet-of-Things wireless solutions.

To improve the system efficiency of a TX, which normally consists of a VCO (or DCO) and a power amplifier, it is worth to consider a current-reuse topology between the two blocks. The current-reuse VCO-PA (Li et al. 2015) has demonstrated good system efficiency (17.5%), but has a limited P_{out} (-1 dBm) after stacking.

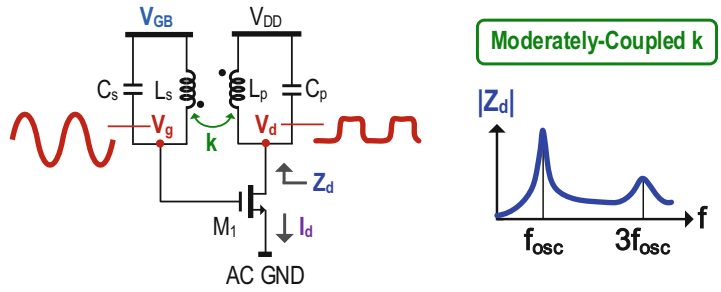

Fig. 14.23 Class-F VCO (Babaie et al. 2013)

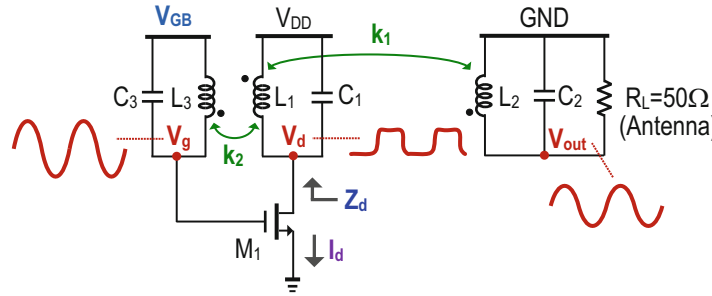

Fig. 14.24 Ongoing work on a Class-F VCO driving up the antenna (Peng et al. 2016)

Table 14.5 Brief summary of this work with respect to the state-of-the-art TXs

Parameters	This work (Peng et al. 2017)	ISSCC '15 (Liu et al. 2015a)	ISSCC '15 (Prummel et al. 2015)
Applications	2.4 GHz ZigBee	2.4 GHz BLE/ZigBee/2 M Proprietary	2.4 GHz BLE
Architectures	Class-F VCO	Class-D PA + LC-DCO	Class-D PA + LC-VCO
On-chip inductor or transformer	1 (Shared by VCO, PA and O/P Matching)	2 (1 for LC-DCO, 1 for O/P Matching)	3 (1 for LC-VCO, 2 for O/P Matching)

Thus, our recent work (Peng et al. 2017) reported a function-reuse DCO-PA that not only shares bias current, but also upholds a full VDD for both the DCO and PA operation.

Here, the basic circuit is inspired by the class-F oscillator (Fig. 14.23), which is attractive for its high FoM of 192 dBc/Hz (Babaie et al. 2013). It features a resonant tank (L_pC_p, L_sC_s) with a moderately-coupling k to peak up the drain impedance (Z_d) at both 1st and 3rd harmonics, resulting in a pseudo-square drain voltage (V_d) to reduce the oscillator's impulse sensitivity function. Although V_d and the drain current (I_d) are alike a square-wave, the tank's resonant response recovers a sine V_g by suppressing the harmonic components, while offering a passive gain to V_g under step-up ratioing ($L_s > L_p$). These properties are preserved when it is modified as a class-F VCO that can directly up the antenna (Fig. 14.24). This scheme reuses the amplifying device (M_1) to unify the DCO and PA functions for power and area savings (Table 14.5).

L_{1-3} form a transformer enabling self-oscillation and boosts up V_g by step-up ratioing ($L_3 > L_1$), and output-impedance matching to deliver adequate P_{out} (>0 dBm) to R_L. The coupling coefficients can be customized for optimum performance.

14.6 Conclusions and Future Perspectives

This chapter described the system aspects and circuit techniques of building cost-aware ultra-low-power (ULP) radios for both 2.4-GHz and

sub-GHz ISM bands. We demonstrated that effective co-design between the system and circuit levels, as well as RF and analog block levels, are decisive to concurrently balance the cost and power budgets, while keeping up the radio performance without resorting from external components. Other state-of-the-art techniques are summarized in Lin et al. (2016) and Yu et al. (2017).

For future development, to cope with the fast market shift and many upcoming applications, multi-band multi-standard ULP radios with flexible data rate will become promising for the future IoT growth. In addition to the obvious goal of high energy efficiency during the active mode of the radios, they should also be designed for very low sleep/leakage power, preferably in the range of pW (Paidimarri et al. 2015), such that after heavily duty cycling, the average system power can be minimized. The technology choices also offer the flexibility of using low-V_t thin-oxide transistors for core circuits such that a lower VDD can be used to save power, whereas high-V_t or thick-oxide transistors can be used to suppress the sleep current. Mixed-VDD design can be a chip-level strategy for power savings (Mak and Martins 2012).

To save power, it is possible to avoid the RF PLL for channelization by using a temperature-compensated thin-film bulk-acoustic-wave resonator (FBAR) that assists the RF-to-IF downconversion. Thus, the channel selection can be delayed to lower frequency (Wang et al. 2014).

The average power is critical for a long battery lifetime, as it will dominate the maintenance cost of massive-scale wireless sensor networks. This fact urges the need of highly autonomous ULP radios that can survive with mainly/only energy harvesting. To this point, fully-integrated ULP power management units and multi-source energy harvesters will be of great importance (Masuch et al. 2013).

For the transceiver, although the sensitivity of a state-of-the-art ULP receiver is better than −90 dBm (Liu et al. 2014), their tolerability to large out-of-band blockers should have room to be further improved. The gain-boosted N-path filtering technique (Lin et al. 2014c) can be a helpful technique to enhance the resilience of the receiver. For the state-of-the-art transmitters, their power efficiency is still not that high (Liu et al. 2015a) at a 0-dBm output power. Thus, it is worth to revisit the design of ULP PA and VCO as described in (Peng et al. 2017).

LO generation can consume significant power and area when approaching multi-band operation. For example, for a universal radio to cover the 2.4 GHz and sub-GHz ISM bands, the tuning range of the VCO should be 57% if a 2.4-GHz VCO is selected and followed by a divide-by-4 circuit. Such a wide tuning range should consume more power than the single-band design. In fact, from area and tuning range's viewpoint, a ring oscillator can be more attractive. However, to meet the required phase noise, ULP consumption is still challenging. Time-interleaved ring oscillator (Yin et al. 2016a, b) with effective phase noise reduction offers the potential to alleviate this tradeoff.

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