Ultra-Low Power Analog Interfaces for IoT

12

Jerald Yoo

This chapter addresses the challenges and design strategies in Analog Front-End (AFE) interface circuit design with an umbrella of IoT. A stringent energy constraint in IoT means the circuit specification must take into account the energy-efficient operation. Also, at the same constraint, the dynamic and static offset/noise compensation should be done effectively.

12.1 Introduction

Internet-of-Things (IoT) has variety of applications, including but not limited to, biomedical sensors, MEMS, environmental sensors and sensor networks. The interface circuits bridges between the physical world and the electrical signal, and it is a crucial component in IoT system. Common constraints on these applications are limited form factor and the consequent limited power/energy sources. Therefore, it is very important we understand the constraints and draw the specification of the interface circuit that meets the IoT needs.

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12.1.1 Unique Environment

Let us cover in details several important challenges that Interface circuit faces under IoT environment. These challenges lead to the design requirements and trade-offs.

Limited Power/Energy Source: As an example, a state-of-the-art MEMS piezoelectric power generator, thermoelectric generators (TEG) or photovoltaic cells (PV) is capable of generating ~100s of μW in a form factor smaller than 1 cm^3; let us not forget that these energy harvesting sources are, most of time, not "always available", in other words, average power that we can draw may be even smaller (See Table 12.1 for more details). On the other hand, if we choose a coin-cell battery, we have tens of mAh in the budget, which is still very limited.

Noise and Offset: IoT interface circuit may have near DC up to hundreds of kHz as its bandwidth. In this bandwidth, there are intruders that we refer to as "in-band noise". As shown in Fig. 12.1, these include *1/f* noise, 50/60 Hz noise, thermal noise and static/dynamic offset. In many cases, the noise well embeds the weak signal. Hence noise-aware design is of crucial.

1/f Noise: Flicker noise, often referred to as *1/f* noise, is unavoidable in all CMOS amplifiers, caused by charge carriers randomly trapped/released between the gate oxide and the substrate.

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Table 12.1 Estimated power output values per harvesting methods (Table from Belleville et al. (2009))

Source		Source characteristics	Physical efficiency	Harvested power
Photovoltaic				
Office		0.1 mW/cm^2	10–24%	10 μW/cm^2
Outdoor		100 mW/cm^2		10 mW/cm^2
Vibration/motion				
Human		0.5 m@1 Hz 1 m/s^2@50 Hz	Maximum power is source dependent	4 μW/cm^2
Industry		1 m@5 Hz 10 m/s^2@1 kHz		100 μW/cm^2
Thermal energy				
Human		20 mW/cm^2	0.10%	25 μW/cm^2
Industry		100 mW/cm^2	3%	1–10 mW/cm^2
RF				
GSM	900 MHz	0.3–0.03 μW/cm^2	50%	0.1 μW/cm^2
	1800 MHz	0.1–0.01 μW/cm^2		

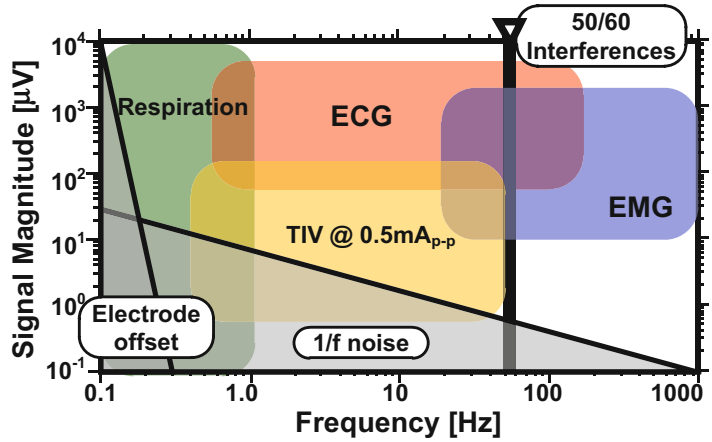

Fig. 12.1 Example IoT noise and signal bandwidth: case of wearable sensor applications (figure courtesy of Dr. Long Yan, Samsung Electronics)

The average power of *1/f* noise is given by Eq. (12.1):

$$\overline{V_n^2} = \frac{\kappa}{C_{ox}WL} \cdot \frac{1}{f} \tag{12.1}$$

The existence of *1/f* noise is problematic because it overlaps with many IoT application's signal bandwidth; specifically, the *1/f* nature of the noise makes the dominant component near DC. As Eq. (12.1) shows, in order to decease the 1/f, we need to have larger device (with larger WL), or use dynamic offset cancellation technique, which will be discussed in detail in Sect. 12.3.

12.1.2 Design Requirement and Performance Metrics

System Resolution: Depending on what are the back-end and post-processing needs, we can decide the system resolution. For example, a wearable physiological sensor may require >10b signal accuracy, therefore the A/D Converter (ADC) should have >10b resolution.

ADC Reference Voltage and Interface Amplifier Gain: Once the ADC bit widths is decided, the Least-Significant Bit (LSB) system resolution can be calculated by the ADC reference voltage. For

example, if 1.10 V is used as a ADC voltage reference, and the ADC is 10b, then the LSB resolution becomes 1.07 mV. At this point, if we want to have the minimal signal level that we can detect to be 1 μV, the interface amplifier need to have at least 60 dB gain; a 60 dB gain means we need a multi-stage amplifier. Note that the minimal signal level is related to the noise floor, where Signal-to-Noise Ratio (SNR) becomes 1.

Sampling Rate: ADC's sampling speed is strictly related to the signal processing throughput at the back-end. Also, for the AFE perspective, this impacts the anti-aliasing filter specification. Considering the stringent energy/power and form factor (area), we need to choose the right order (roll-off factor). Choosing too high order will increase the power and area consumption.

Common Mode Rejection Ratio (***CMRR***): The interface circuitry may be composed of off-chip devices such as capacitors and resistors in the signal path. In such cases, CMRR has two components: on-chip AFE ($CMRR_{AFE}$) and the off-chip interface ($CMRR_{IF}$), where the overall $CMRR_{SYS}$ is determined by Eq. (12.2) (Yoo 2014):

$$\frac{1}{CMRR_{SYS}} = \frac{1}{CMRR_{AFE}} + \frac{1}{CMRR_{IF}} \tag{12.2}$$

It should be noted that in general off-chip devices have limited matching, which makes it challenging to have $CMRR_{IF}$ of over 60 dB; consequently, as Eq. (12.2) shows, however high the $CMRR_{AFE}$ would be, the $CMRR_{IF}$ will determine the overall $CMRR_{SYS}$. The message here is clear: when it comes to IoT system, integrate as many components on-chip as possible.

Noise Efficiency Factor (***NEF***): One of the performance metric we can use for the IoT AFE is NEF. Due to variety of gains that different amplifiers have, it is not fair to compare the output noise directly. Instead, we divide the output noise with the gain of the amplifier, and this is called the Referred-to-Input (RTI) noise. Note that noise RTI exists regardless of technology node we use, and there is a theoretical lower limit on the power consumption of the amplifier, dependent on the noise spectral density requirement.

To probe this further, we can start the noise analysis with a Bipolar Junction Transistors (BJTs), which has a lower noise spectral density RTI than CMOS transistors have for a given bias current. For a single common-emitter amplifier, a short-circuit voltage noise density is well known as in Eq. (12.3):

$$V_{ni,RMS} = \sqrt{\frac{\pi q V_t^2 BW}{I_C}} \tag{12.3}$$

Where $V_{ni,RMS}$ is the RMS value of the noise RTI integrated over a bandwidth of BW, I_C is the collector current, q is the charge on an electron, and V_t is the thermal voltage of kT/q. With this, we can now compare the performance of the different amplifiers to that of the theoretical limit of a single BJT; this is called the Noise Efficiency Factor (NEF) (Steyaert et al. 1987):

$$NEF = V_{ni,RMS}\sqrt{\frac{I_{overall}}{\pi V_t 4kT\, BW}} \tag{12.4}$$

The NEF shows the trade-off between the current consumption and the noise of an amplifier. Note that the NEF of a single BJT having only thermal noise equals to 1, where a differential BJT is $\sqrt{2} = 1.414$. Since we know that CMOS amplifier in general have worse noise spectral density for a given bias current, we can expect that NEF of a CMOS amplifier will be higher than that of a BJT.

12.2 Ultra Low Power/Energy Interface Design

We should keep in mind that in IoT applications, we have a very tight power and energy constraint. As probed earlier, we have largely two scenarios in power source: energy harvesting/scavenging, and battery. With this in mind, in this Sect. 12.2, we will take a closer look at the interface circuit design, in power and energy

perspective. We will also cover design strategies for low-cost, energy-efficient filter.

12.2.1 Power Vs. Energy: Choosing the Right Goal

When an energy harvesting/scavenging is used for the IoT power supply, it is very important to design the circuitry not to exceed the instantaneous current driving capability of the power source. Table 12.1 shows the estimated output values of energy harvesting (for different sources). Depending on the IoT application, the harvested power amount varies significantly. We should not forget that these amount are optimistic values on average; for example, in PV, if there is an instantaneous blockage of the cell, the generated power will drop abruptly. Therefore, if the circuit needs continuous operation, the designer may want to introduce a secondary energy storage such as super capacitor or battery.

Nevertheless, when using the harvesting/scavenging as the main source, keeping the "peak power consumption" of the circuitry well below that of the generator's limit should be the key design target. This is aligned with what we saw from Sect. 1.3.1.

With this in mind, it is helpful to see what will be the consequences of designing lower power interface circuit. First of all, the amplifier will be impacted significantly. The bias current cannot exceed the limit set by the supply, therefore the thermal noise will increase. Available power level of μW order means the transistors will likely operate in weak inversion (or -sub-threshold), which will be prone to Voltage and Temperature variation. Also, the impact of dynamic offset will become more serious. Strategies to overcome these issues will be described in detail in Sect. 12.3.

Now let us consider the case where we use battery as the main power supply. A coin cell battery, or a small flexible battery, will have the capacity of tens to hundreds of millamp-hour (mAh). Compared to energy harvesting/scavenging case, we have more room for maximum allowable current. However, as we discussed in Sect. 1.3.1, now the energy consumption (or the average power consumption) of the circuity will determine the system lifetime. This means, when the battery is the power supply, then minimizing the "energy consumption", or the average power consumption, should be the target goal. Systematic approach to achieving energy efficiency was already covered in Sects. 1.3 and 2.3. Also, in Sect. 12.3, we will see the design strategies for power- and energy-efficient analog interface circuit design.

12.2.2 Top-Down Approach for Power and Energy Efficiency

Especially for IoT system/sensor, it is very important we design the system in to-down approach to meet the power and energy requirement. This means, when designing such system, we should answer the following questions, from top to bottom:

- What is the application we are targeting for?
- What is the energy source? (Harvesting/Scavenging/Battery/Hybrid/etc.)
- What are the system components that will be included/excluded? (analog interface, filters, voltage reference, analog-to-digital converter, post processing, communication block, memory)
- What is the available power budget for each block?
- What is the performance requirement for each block?
- What are the constraints/bottleneck in achieving such performance under such environment?
- Defining the specification of each block, and start designing.

Without considering the system perspective, one might end up designing the lowest-power consuming analog interface circuit, but that block is only a small fraction of overall system power consumption; as a result, in such cases, the total system power consumption would not decrease much. This can be avoided by breaking down the system power budget from the beginning.

12.2.3 Small Form Factor, Efficient Filter Design

Because of the very strict power budget in IoT, often the filter design becomes an issue in interface circuits. Not only the power and energy, but also the area is of concern. Most of time we do not have luxury of using high order filters in such area- and power- constrained system. Therefore, approaching from a system perspective is very crucial.

As previously described in Sect. 12.1, this becomes particularly important in dynamic offset compensation circuit, where extensive filtering is needed. Here are some strategies we can take for an area- and energy-efficient filter design:

- Active filtering of ripple-induced noise by real-time sampling and subtracting (Fan et al. 2011): suitable for an area-constrained environment. The amplifier features a ripple-reduction loop (see Fig. 12.18) to sample the noise and subtract it in real time; by doing so, we can avoid using area-consuming high-order filters.
- Balance of analog interface and digital processing filtering (Altaf et al. 2015; Yoo et al. 2013): Choose the oversampling rate and chopping frequency to use only 2nd order filter in analog interface; then the digital processor also aids filtering.

12.3 Noise-Aware Interface Circuit Design

In this subsection, we will look into details of the interface circuit design for IoT. We will start with basic instrumentation amplifier (IA), compare the strengths and weaknesses. After that, we will see the two widely used dynamic offset compensation techniques: Auto-Zeroing and Chopper-Stabilization.

12.3.1 Instrumentation Amplifier Basics

Now let us look into the Instrumentation Amplifier (IA) basics. Understanding the IA basics is crucial for expanding the perimeter to IoT applications.

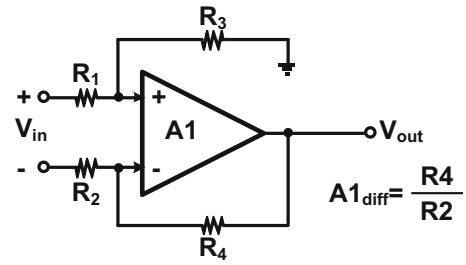

Fig. 12.2 Single-amp IA

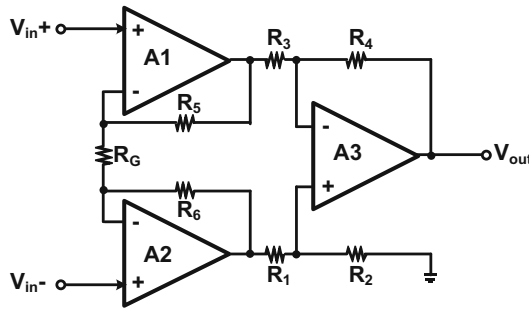

Fig. 12.3 Three-amp IA

Single-Amp IA: The simplest IA is a Single-amp IA shown in Fig. 12.2. The gain is defined by R4/R2 with a large input voltage range. However, this structure has a fundamental problem: low input impedance. The input impedance is determined by R_1 and R_2, but we cannot increase them too much, because otherwise the gain will be limited. Hence, loading effect may become an issue in IoT applications. More importantly, in IoT, with stringent low power requirement (low bias current), the thermal noise may be large enough to corrupt the input signal, and there is no mitigation technique of it.

Three-Amp IA: The classical 3-amp IA shown in Fig. 12.3 solves the low input impedance problem of a Single-amp IA. This is done by adding buffer amplifiers (A1 and A2) to each input of the differential amplifier (A3).

Here, the gain is defined as shown in Eq. (12.5):

$$Gain = \left(1 + \frac{R_5 + R_6}{R_G}\right)\left(\frac{R_4}{R_3}\right) \tag{12.5}$$

Note that when R_G is removed, A1 and A2 will operate as a unity-gain buffer amplifier. By adding R_G, and additional gain is achieved. On top of

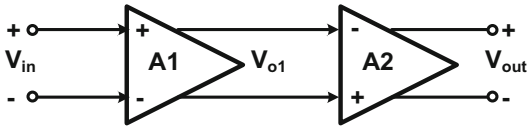

Fig. 12.4 CMRR of a multi-stage amplifier

that, R_G is free from matching issues, since only one resistor is added. This is why this structure is widely adopted to-date in IA domain.

However, for IoT, this is still not enough due to lack of dynamic offset removal—the offsets will be a problem on top of that, with such low power requirement, the bias current cannot be high, and subsequently noise is significant.

CMRR of a multi-stage IA: It is also worth remembering that in a multi-stage amplifier, CMRR of each stage will impact differently in overall CMRR performance. Let us assume that the 2-stage amplifier shown in Fig. 12.4 has gain of A1 and A2, with CMRR of each stage to be $CMRR_1$ and $CMRR_2$, respectively.

Now let us assume the input voltage of $V_{in} = V_{id} \pm \frac{V_{ic}}{CMRR_1}$ is applied, where V_{id} and V_{ic} are the differential and common mode component of the input, respectively. Then, in Fig. 12.4, V_{o1} can be expressed as $V_{o1} = A1 \cdot V_{in}$. Therefore, V_{out} will become:

$$V_{out} = A2\left(V_1 \pm \frac{V_{ic}}{CMRR_2}\right)$$

$$= (A1 \cdot A2) \cdot V_{id} \pm \left(\frac{A1 \cdot A2}{CMRR_1} + \frac{A2}{CMRR_2}\right) \cdot V_{ic} \qquad (12.6)$$

Observing Eq. (12.6), we find that the differential gain is $(A1 \cdot A2)$ and the common-mode gain becomes $\left(\frac{A1 \cdot A2}{CMRR_1} + \frac{A2}{CMRR_2}\right)$. Since CMRR is the ratio of differential gain to the common mode gain, now the CMRR of the overall amplifier becomes as in Eq. (12.7):

$$\frac{1}{CMRR_{amp,overall}} = \frac{1}{CMRR_1} + \frac{1}{A1 \cdot CMRR_2} \qquad (12.7)$$

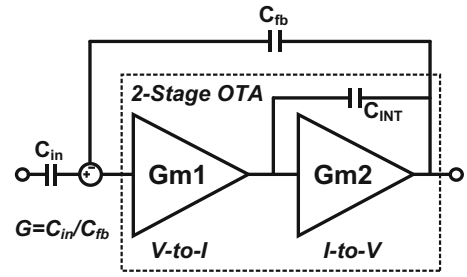

Fig. 12.5 IA with a capacitive gain element

This gives us an important message: in a multi-stage amplifier, the CMRR of the first stage will dominate the overall CMRR performance! Hence, in an IoT AFE/IA design, it is very important we give an attention on the low-noise yet high-CMRR performance of the first stage amplifier.

Capacitive Coupled IA (***CCIA***): Noting that in general capacitors have better matching than the resistor has, the amplifier shown in Fig. 12.5 utilizes capacitive gain element (Harrison and Charles 2003). Here, the gain is defined as C_{in}/C_{fb}. This type of an amplifier is called Capacitive Coupled IA (CCIA).

Using capacitive gain element has another very strong advantage: C_{in} blocks DC and therefore the amplifier accepts rail-to-rail input. Since then, this simple-but-powerful idea is widely adopted in IA domain.

Aforementioned amplifier types—single-amp, three-amp or CCIA—has a fundamental limit, when it comes to IoT applications: static and dynamic offset. None of above amplifiers have the offset mitigation scheme, and especially in low power (with low bias current) environment, the dynamic offset including *1/f* noise becomes a series issue.

12.3.2 Auto-Zeroing

Aforementioned issues in IA—especially the dynamic offset—must be mitigated in IoT applications. One technique to overcome the issue is Auto-Zeroing (Enz and Temes 1996). The concept of the auto-zeroing is simple:

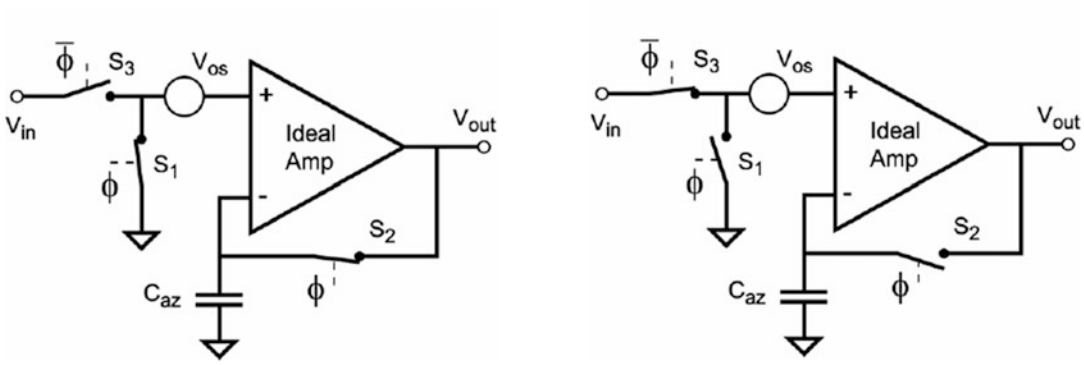

Fig. 12.6 Auto-zeroing concept: sampling phase (*left*), and amplification phase (*right*) (figure from Makinwa et al. (2007))

sample the offset (from either input or output), and then subtract it. This is illustrated in Fig. 12.6.

In auto-zeroing, there are two phases: Sampling Phase (shown in left), and Amplification Phase (right). Assuming an ideal amplifier in Fig. 12.6, during the sampling phase S1 and S2 are closed (forming a buffer amplifier), and the offset of the amplifier is sampled at the output and stored into the storage capacitance C_{az}. Alternatively, in other structures, intermediate or input offset can be sampled.

Now in the amplification phase, S1 and S2 are open, and S3 is closed. Since the C_{az} stores the offset value, and is connected to the negative input, the offset is removed and only the signal component will be amplified.

The auto-zeroing can be explained in sampled signal perspective as well. Let us consider the auto-zeroing system as a sample-and-hold (S&H) structure as shown in Fig. 12.7. Here, the $V_{n,az}$ $z(f) = V_n(f) \cdot (1 - H(f))$, where $H(f)$ is the transfer function of the S&H block. S&H is gate function in time domain, and therefore $H(f) = sinc(\pi f / f_S)$. Noting that sinc function acts as a low-pass filter (LPF) with passband in DC, 1-$H(f)$ is a high-pass filter (HPF). This is why the auto-zeroing mitigates the *1/f* noise (near DC) and the other offset as well.

Auto-zeroing also has one limitation and that is the noise folding into baseband. This is due to limited bandwidth of the S&H; during the sampling

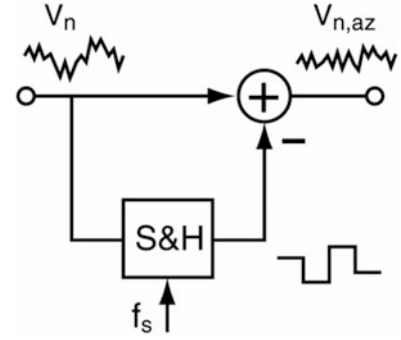

Fig. 12.7 Auto-zeroing in signal processing perspective (figure from Makinwa et al. (2007))

phase, the higher frequency component (mostly thermal noise) will be under sampled, and this will be folded into baseband during amplification.

Regardless of the limitation, the auto-zeroing can be widely used in IoT applications, especially those with sampled system or with applications having single-ended signals as their inputs.

12.3.3 Chopper Stabilization

Chopper-stabilization (Enz and Temes 1996) is another commonly used dynamic offset cancellation technique that suits well with IoT application. In a nutshell, chopper stabilization modulates the input signal into higher frequency before the 1/f and other dynamic offset corrupts the signal.

Figure 12.8 illustrates a chopper-stabilized amplifier in time domain. It is composed of a differential amplifier (Amp), a modulator/demodulator pair, and a low pass filter (LPF). The signal drawn in blue, denoted as V_{IN}, is differential. As the input chopper swaps V_{IN}^{+} and V_{IN}^{-} with the chopping frequency f_{chop}, the input of the differential amplifier will be amplitude modulated (shown as a square wave in Fig. 12.8 at the amplifier input). After the amplifier, the modulated input signal is amplified, and the dynamic offset such as *1/f* noise, denoted by red dotted line, is added to the output. Then the "modulated and amplified" input signal, plus the noise, are demodulated at the frequency f_{chop}. At this stage, the signal is demodulated (with an image at $2 \times f_{chop}$), and the noise is "up modulated" at f_{chop}. After filtering out the higher frequency component, clean amplified signal is obtained. This is just as in amplitude modulation/demodulation.

Figure 12.9 shows the same in frequency domain. Again, the signal component is denoted by blue (and the gray shade in spectrum), and the aggressors are in red. Since the demodulation leaves harmonics at higher frequencies, careful design of LPF is needed. f_{chop} should be higher than the *1/f* corner frequency, in order to sufficiently mitigate it. One may think that choosing higher f_{chop} will ease the filter specification, because Fig. 12.9 implies having baseband as far away from f_{chop} will enable using lower order filters. However, doing so will also introduce more frequent chopping induced spikes due to charge injection, which in turn translates to a residual offset. Therefore, balancing the filtering specification and chopping frequency becomes a crucial design choice! It should be also noted that the choosing f_{chop} is also dependent on the *1/f* corner frequency and the Gain Bandwidth (GBW) of the amplifier—the amplifier BW should be sufficiently higher than the f_{chop} to avoid gain errors.

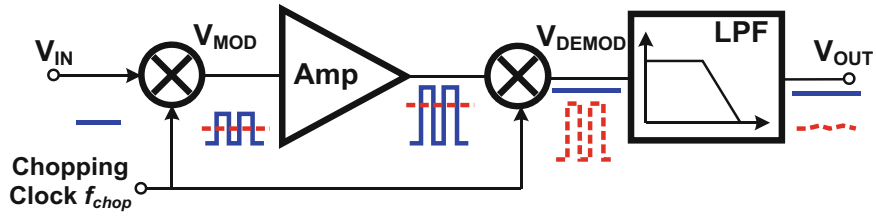

Fig. 12.8 chopper-stabilization (time domain)

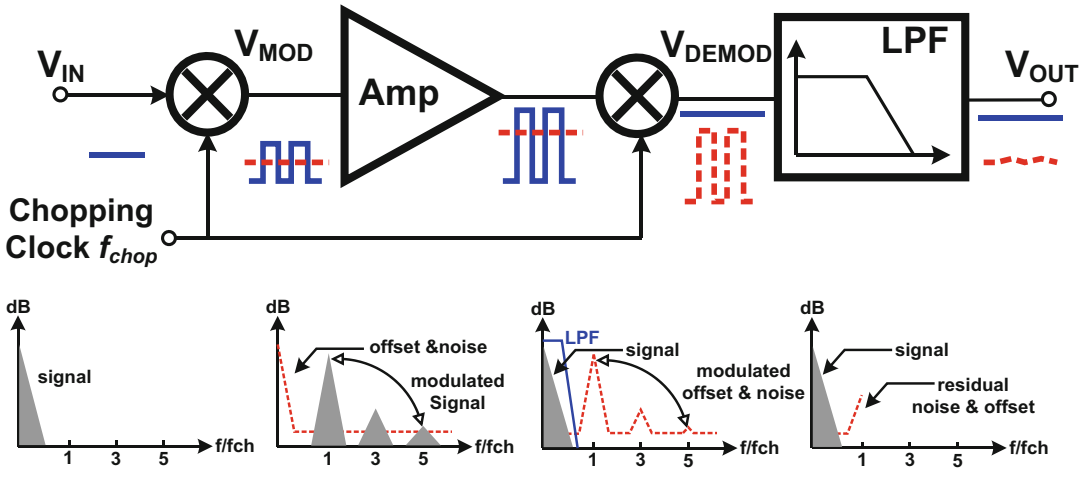

Fig. 12.9 Chopper-stabilization (frequency domain)

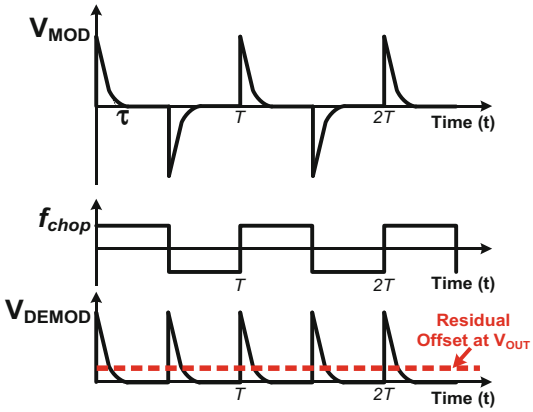

Fig. 12.10 Chopper-induced residual offset (figure from Yan et al. (2010))

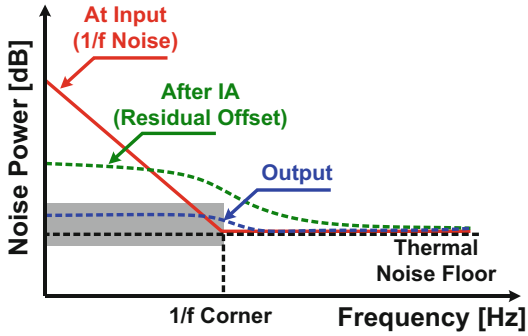

Fig. 12.11 Noise power in spectrum

Figures 12.10 and 12.11 denotes the chopper-induced spikes and its residual offset. An ideal chopper switch would not induce such issues; however, in real world, due to the parasitic capacitance between the gate and source/drain, clock feedthrough and the chopper induced spikes will show up at the chopper output, as in V_{MOD}. After the demodulation and the LPF, these spikes will show up as a DC offset—in this text, we denote this as the "residual DC offset". Of course, the higher the f_{chop}, the more frequent the spikes happen, and the more residual DC offset we will get.

The residual DC offset will incur the distortion and gain error, hence we need to mitigate it. First of all, we should remember the source of

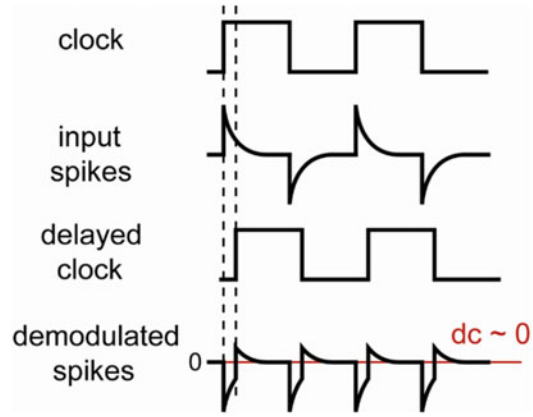

Fig. 12.12 Delayed sampling (figure from Makinwa et al. (2007))

such spikes are from parasitic capacitance between gate and drain/source; hence, using smaller switch will reduce the parasitic capacitance, consequently reduce the spike strength. However, using smaller switch means the on resistance of the switch becomes higher, which maybe an issue for a given application.

To mitigate the residual offset in more active way, delayed sampling (Menolfi et al. 1999) can be used. Shown in Fig. 12.12, a demodulator matched to a modulator is operated by a "delayed clock" with respect to the modulator clock. The amount of delay is controlled in a such way that the demodulated spikes, when averaged out, will have DC offset of nearly zero. Controlling the delayed timing is difficult, however, due to PVT variation and load-dependent spike amount.

Another technique is nested chopping (Bakker et al. 2000), as shown in Fig. 12.13. The inner chopper, operating at f_{CHOP_H}, performs the *1/f* and offset mitigation. This will generate chopper-induced spikes. The outer chopper, operating at f_{CHOP_L}, embraces the spikes to alternate and swap the group of spikes, as shown in the figure. This will effectively average out the spikes, thereby reducing the residual DC offset. We should keep in mind, however, that the nested chopping will reduce the bandwidth considerably, because now the signal bandwidth is bound by f_{CHOP_L}, but not by f_{CHOP_H}.

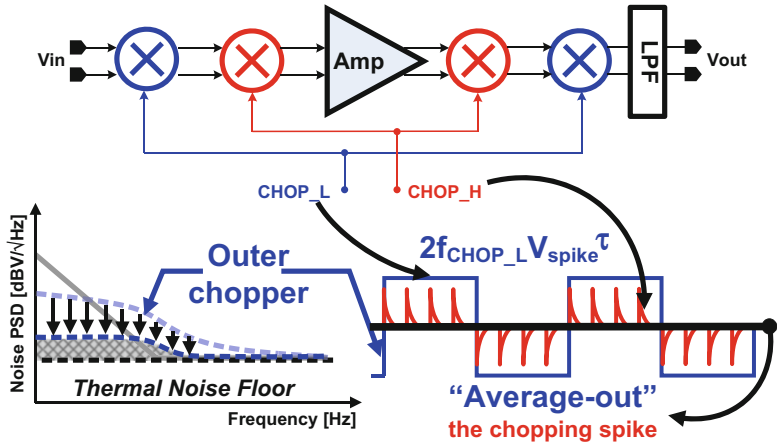

Fig. 12.13 Nested chopping (figure from Yan et al. (2010))

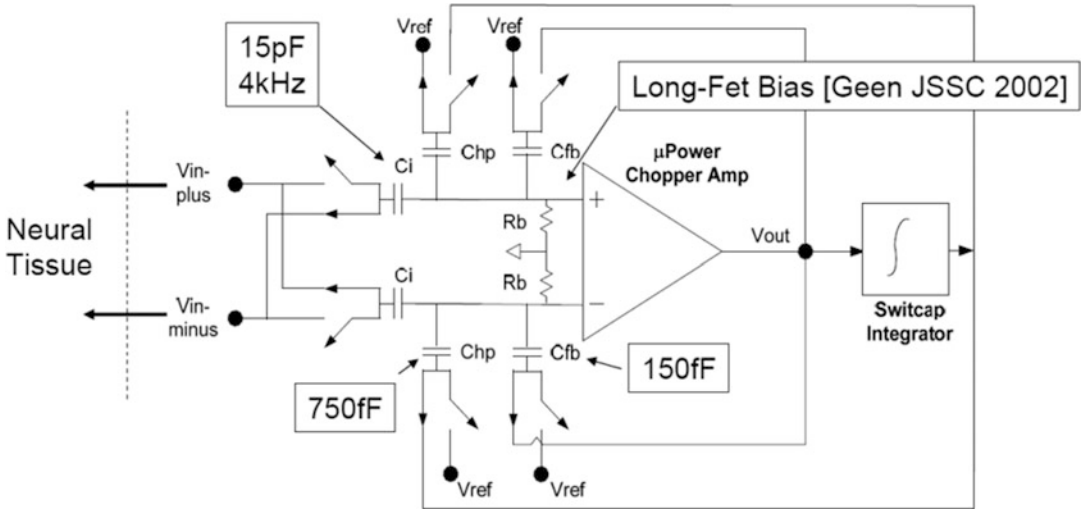

Fig. 12.14 Chopper-Stabilized Capacitive-Coupled IA (CS-CCIA) with chopper switch moved before the DC blocking capacitance (Denison et al. 2007)

12.3.4 State-of-the-Art IA Design

In this subsection, we will explorer several state-of-the-art IA design, adopting low-noise, low-power and low-energy topologies. Pros and cons of each design is also presented.

12.3.4.1 Chopper-Stabilized Capacitive-Coupled IA (CS-CCIA) with Chopper Ahead of Input Capacitor: High CMRR, Low Noise

The amplifier shown in Fig. 12.14 has the input chopper prior to DC the input capacitor (C_i) (Denison et al. 2007). By doing so, any mismatch on C_i can be modulated and mitigated. With the capacitive-coupled structure with capacitive gain element, the amplifier has very high CMRR (100 dB), low integrated input referred noise (0.98 μV_{rms} for 0.5–100 Hz), and well-defined gain with excellent high-pass corner is obtained.

One limitation of the strcuture, though, is the exitance of chopper at the input stage drops the differential input impedance ($Z_{in,diff}$) of the amplifier; the parasitic capacitance within the chopper switch, combined with high frequency switching, degrades the $Z_{in,diff}$ significantly. As a result, the amplifier has only $Z_{in,diff}$ of 8 MΩ.

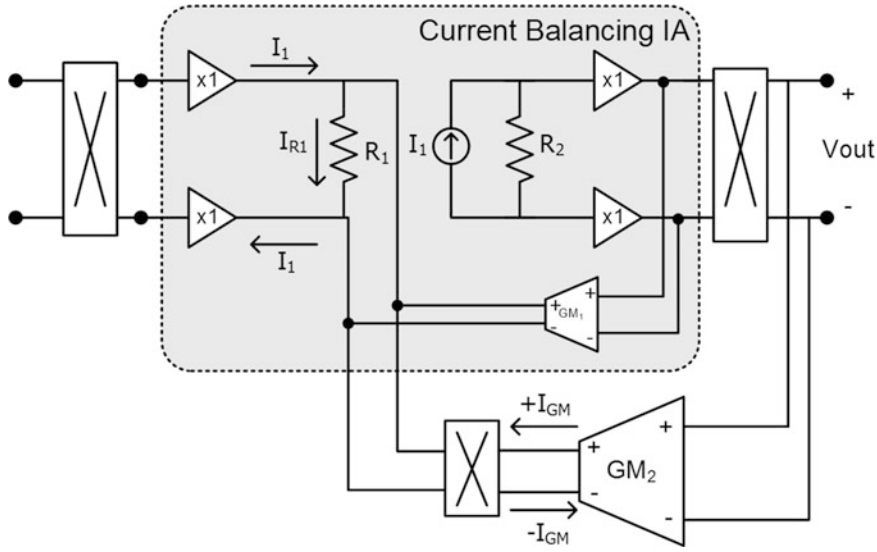

Fig. 12.15 Chopper-stabilized resistive IA with DC servo loop

This is perfectly okay in the application of the amplifier (Denison et al. 2007), which is an implantable device; however, for other IoT applications, this may not be suitable due to loading effect from input side.

12.3.4.2 Chopper-Stabilized Resistive IA: DC Offset Removal with a Servo Loop

Figure 12.15 shows a chopper-stabilized IA that uses resistive gain element (Yazicioglu et al. 2011). It introduces a IA offset reduction loop (GM1) to reduce the IA offset. Additionally, it samples the output DC level with a DC servo loop (GM2), which provides a negative feedback to stabilize and mitigate the DC offset. This smart approach mitigates the chopper induced offset as well as the DC offset caused by mismatch at the sensor interface (in this example, DC offset mainly due to electrode mismatch). As a result, the amplifier shows excellent low noise performance (noise floor of 60 nV/√Hz), high input impedance (>100 MΩ), well defined gain and a DC offset removal.

One downside of the structure is the limited DC headroom by the current-based DC servo loop; in some IoT applications, where rail-to-rail input is required, this structure may impose major limitation.

12.3.4.3 Chopper-Stabilized Capacitive-Coupled IA (CS-CCIA) with Chopping at Virtual Ground: High Input Impedance

To improve the limited $Z_{in,diff}$ of a CS-CCIA, a groundbreaking structure was proposed in (Verma et al. 2010). Shown in Fig. 12.16, the amplifier moves the chopper to the input virtual ground, which boosts the $Z_{in,diff}$ to a very high value. Also note that now the $Z_{in,diff}$ will include the impedance of the capacitors C_{IN} as well. Therefore, this structure is free from loading effect, and ideal for many IoT applications. Also, using capacitive gain component means it has well defined gain of C_{IN}/C_{FB}. Additionally, the bias resistors are implemented by switched capacitors with high resistance (15 GΩ) to save power. The amplifier shows excellent low noise performance (noise floor of 60 nV/√Hz), high input impedance (>700 MΩ), well defined gain and a rail-to-rail input.

The only downside of the strcuture, though, is that the off-chip capacitor C_{IN}. Since C_{IN} are outside the chopper modulation, any mismatch

in the devices will affect the CMRR; as we discussed in Sub-section 12.1 and in Eq. (12.2), the offchip device typically has worse matching than the on-chip device has. As a result, the CMRR of the overall system in (Verma et al. 2010) is limited at 60 dB.

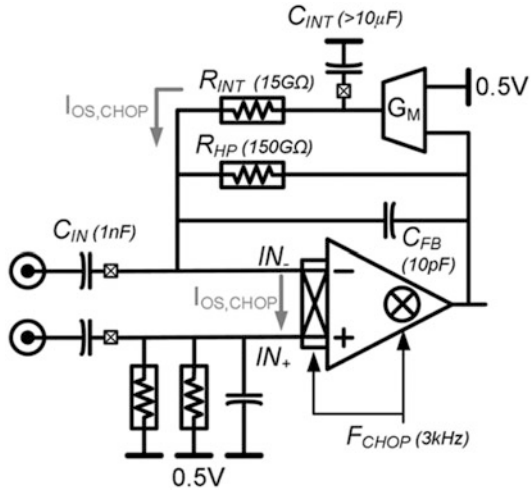

Fig. 12.16 chopping at virtual ground to improve input impedance

12.3.4.4 Chopper-Stabilized Capacitive-Coupled IA (CS-CCIA) with Active Filtering, Impedance Boosting Loop and a Ripple Reduction Loop: Low Noise, High Input Impedance and Small Area

In order to resolve the limited $Z_{in,diff}$ of a CS-CCIA with chopper at input stage, the CS-CCIA in Fig. 12.17 introduces a ground-breaking concept of using positive feedback impedance boosting loop [FSH14]. The amplifier samples the output and forms a positive feedback loop (PFL), which aids the input signal current. Hence, the amount of current needed to achieve desired output swing is dropped, and $Z_{in,diff}$ is effectively boosted. It inherits all the features of CS-CCIA, so it has extremely low-power (1.8 μW), low-noise (60 nV/√Hz) operation, and therefore ideal for many IoT applications.

To further suit for an area-constrained environment, a ripple-reduction loop can be used (Wu et al. 2009). As shown in Fig. 12.18, the amplifier samples the output of the CS-CCIA (with the chopper-induced ripple denoted as $V_{out,ripple}$). It is then passed through C_4, CH_6 then to $Gm6/C_{int}$ to a residual DC offset. This is

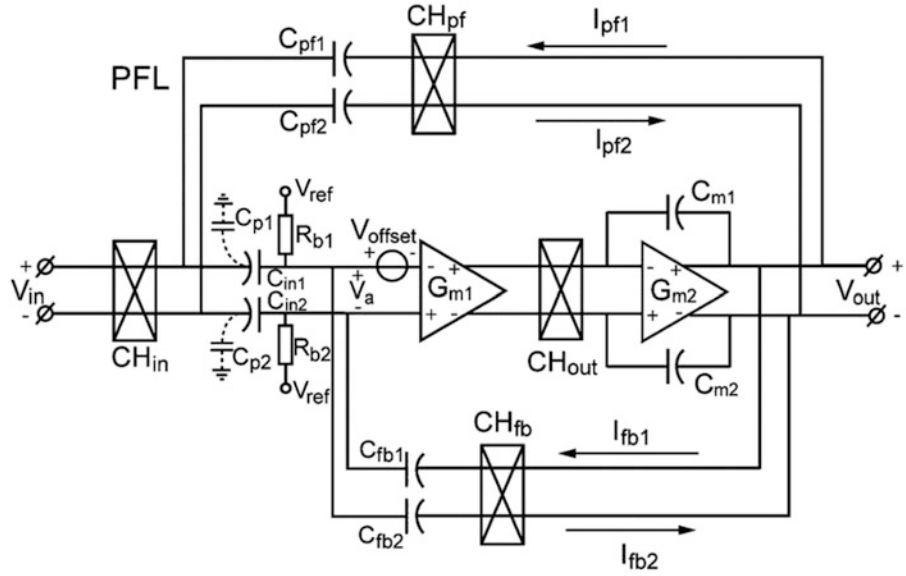

Fig. 12.17 Improving $Z_{in,diff}$ with a positive feedback impedance boosting loop

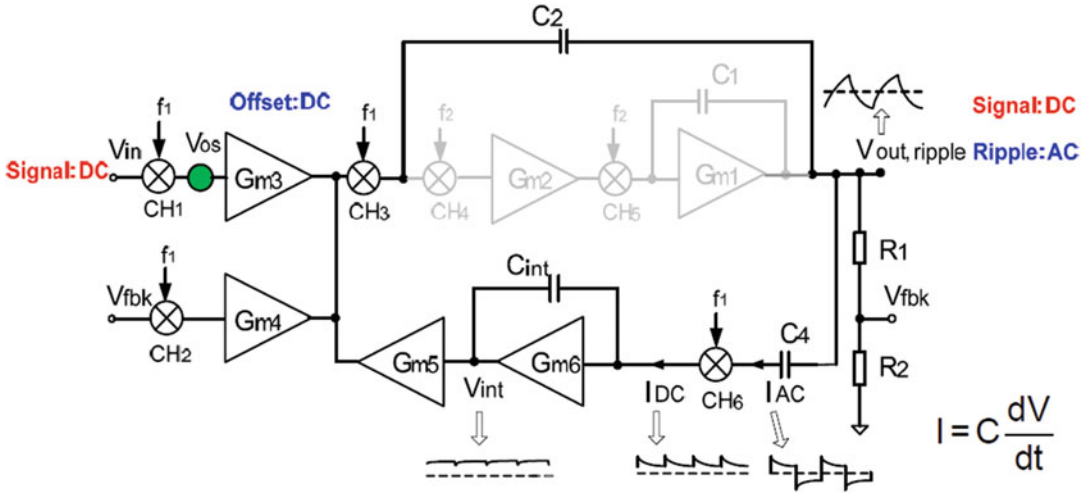

Fig. 12.18 Reducing the chopper-induced ripple with ripple-reduction loop, removes the area-consuming high-order filters

then given as a negative feedback at the input of the amplifier, which effectively removes the residual DC offset at the output stage. With this scheme, use of high-order passive filter can be removed, and significant area reduction can be achieved. This scheme is particularly helpful in IoT where stringent power and area filtering is needed.

12.3.4.5 Chopper-Stabilized Capacitive-Coupled IA (CS-CCIA) with An Additional Chopper at DC Servo Loop: Lower Noise, Small Area and High Input Impedance

As we have seen so far, using DC servo loop to remove DC offset is an effective means to remove DC offset (Fan et al. 2011; Verma et al. 2010; Yoo et al. 2013), but an issue with such structure is that the DC servo loop feedback is applied to an "up modulated" signal; this means, even after the demodulation, the DC servo loop-induced noise cannot be removed. To solve this issue, along with dynamic offset cancellation, the amplifier shown in Fig. 12.19 uses another chopper (operating at lower frequency f_L) around the DC servo loop to effectively remove the elevated noise (Altaf and Yoo 2016). Unlike the nested chopper case, this additional chopper does not affect the main amplifier signal bandwidth, since the DC servo loop is primarily used to remove the DC component, and hence the passband of the loop itself is can be extremely low.

Additionally, the amplifier has a ripple reduction loop and an impedance boosting loop; therefore, the amplifier achieves extremely low power (1.1 μA), low noise (0.81 μVrms for 0.5–100 Hz) while having high input impedance (>500 MΩ).

12.4 Summary and Future Perspectives

So far we have explored the challenges, requirements and design techniques of analog interface circuit for IoT. In this section, we will look into future perspectives of the IA for IoT, and summarize what we have covered so far.

12.4.1 Future Trends on IoT Interface Circuits

With more and more IoT devices being used, recent research on analog interface circuits for IoT shows direction towards power and area efficiency with system-level design consideration; here, we will see two good examples.

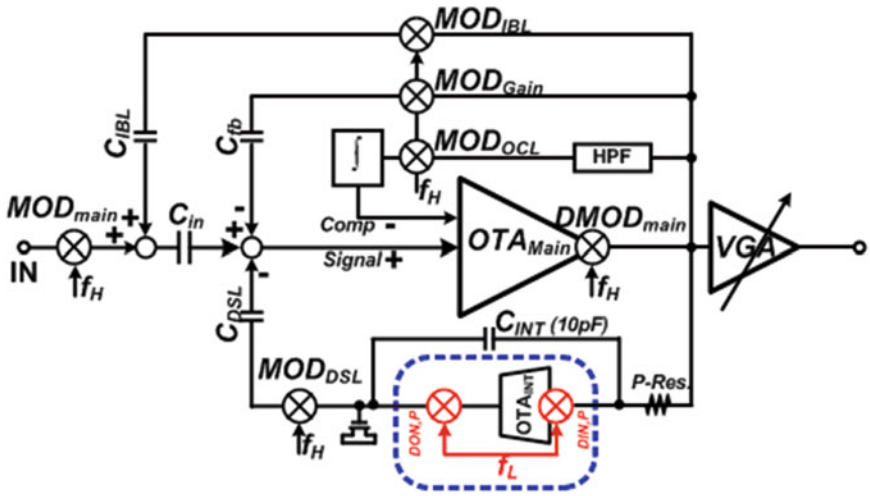

Fig. 12.19 CS-CCIA with ripple-reduction loop, impedance boosting loop and chopped DC servo loop

12.4.1.1 Bulk Switching

Chopper-stabilized IAs described in previous section may suffer from low input impedance, which causes loading effect with high-impedance signal source. We have seen the amplifiers with positive-feedback impedance boosting loop (Fan et al. 2011; Yoo et al. 2013) may mitigate the issue, but at the cost of additional control circuitry and careful design of stability test. To overcome this, a new concept of Bulk Switching was recently introduced (Han et al. 2015). Figure 12.20 shows the concept applied to a CS-CCIA.

The amplifier core (PMOS input pair) has its bulk terminal switched on and off with frequency f_s. As we can observe from the figure, the gate of the input pairs are free from chopper switch, so the input impedance of the amplifier is very high. With the bulk of the input pair switched on and off, the transistor is also turned on and off, thereby decreasing the *1/f* noise. This smart approach solves the low input impedance issue of chopper-stabilized amplifiers with chopper switch at the input, without adding any complex circuitry. As a result, the measurement shows the amplifier has NEF of 2.2, input referred noise of 0.75 μV_{rms} over 1–200 Hz for an 100 kΩ source impedance,

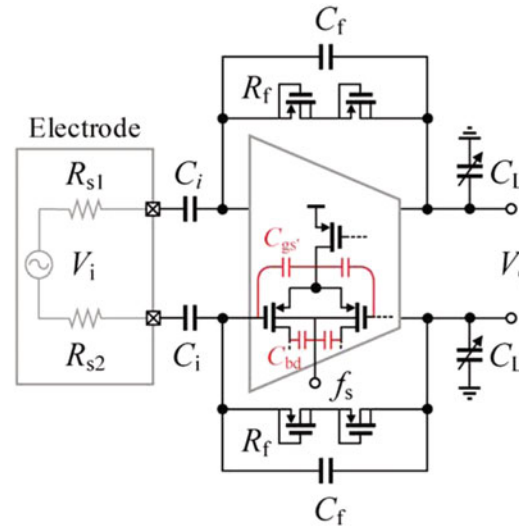

Fig. 12.20 Bulk switching CS-CCIA

while consuming only 3.96 μW from 1.2 V supply. The amplifier occupies 0.053 mm^2 in 65 nm CMOS, which is by far one of the smallest in IAs with this performance.

The bulk switching is a good example of the research directions in IA for IoT, where area- and power-efficiency are both an important design metric.

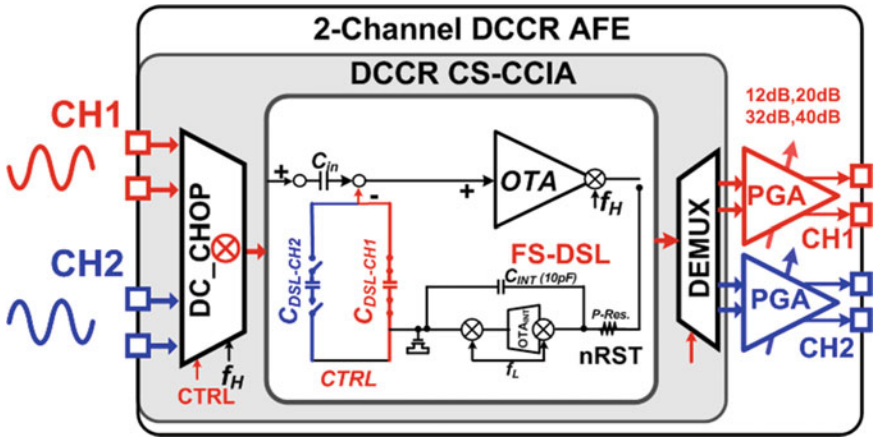

Fig. 12.21 Channel sharing: Dual Channel Charge Recycled (DCCR) CS-CCIA

12.4.1.2 Channel Sharing

An aggressive approach of saving power and area in an IA was recently proposed (Altaf et al. 2015). The Dual Channel Charge Recycled (DCCR) CS-CCIA, switches among two channel, as shown in Fig. 12.21. The idea is to have an IA shared and time-multiplexed among two separate channels.

To avoid bias settling issues, the amplifier core (OTA) samples and stores the bias point. That is, when C_{DSL_CH1} is in amplification phase, the C_{DSL_CH2} and the OTA internal bias storing capacitance hold its bias point; in the next phase, C_{DSL_CH1} holds its bias point and C_{DSL_CH2} resumes its amplification. This effectively "recycles" the bias current of OTA, thereby decreasing the power consumption significantly.

An advantage of such this method is that we do not need to have a separate circuitry to multiplex the channels. Rather, the Dual Channel Chopper (DC_CHOP) (Fig. 12.22) is employed. The DC_CHOP uses two gated clocks, which are originated from a single chopper clock, to perform chopping function and multiplexing function at once!

The implementation and measurement results (Fig. 12.23) show that there is minimal impact on integrated noise (10% increase) while amplifying two channels with a single amplifier. The input is 180-degrees out-of-phase between channels (one of the worst case for multiplexing). The improvement is very clear: 43% and 28% reduction in current consumption (per channel) and in area (per channel), respectively, when compared to using two separate IAs. As a result, it comes only 1.62 μW/channel, integrated input referred noise of 0.9 μV_{rms} (0.5–100 Hz), NEF of 3.29/channel, CMRR of 97 dB while occupying 0.716 mm^2 in 0.18 μm CMOS.

The channel sharing IA is a breakthrough concept in IA for IoT; this is another good example where system-level design consideration and ideas, balanced with the IA's circuit idea, improves the overall system performance.

12.4.2 Summary

As we have seen so far, designing an analog interface for IoT faces many challenges, especially towards the strict power, energy and area constraint. It is very important that system-level consideration is made prior to designing each component. Therefore, top-down approach is highly recommended.

IoT covers many different applications, from environmental sensing/monitoring to wearable healthcare applications, with sensing/processing/communication/storing functions. Each application has different needs, and it is crucial that the IA performance meets the proper target within the application. These metrics include system resolution, sampling rate, CMRR, power/energy consumption, noise performance, NEF and area.

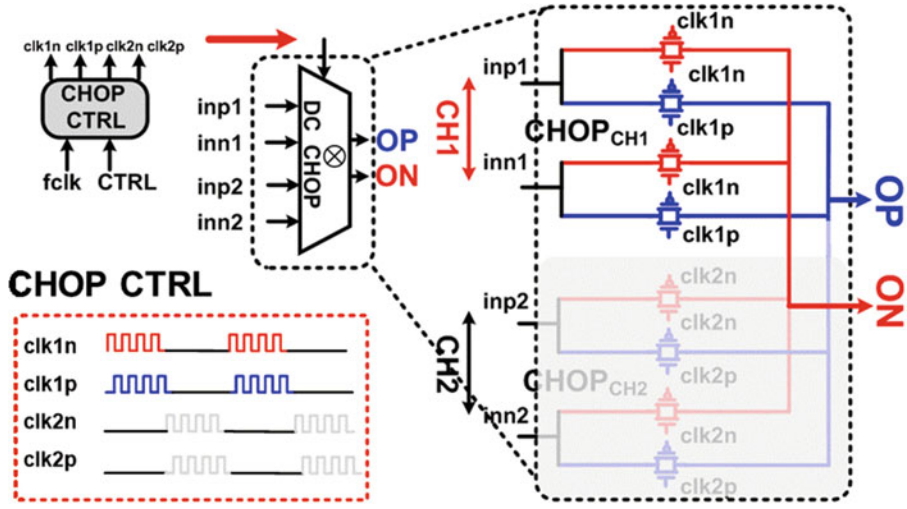

Fig. 12.22 Dual channel chopper switch

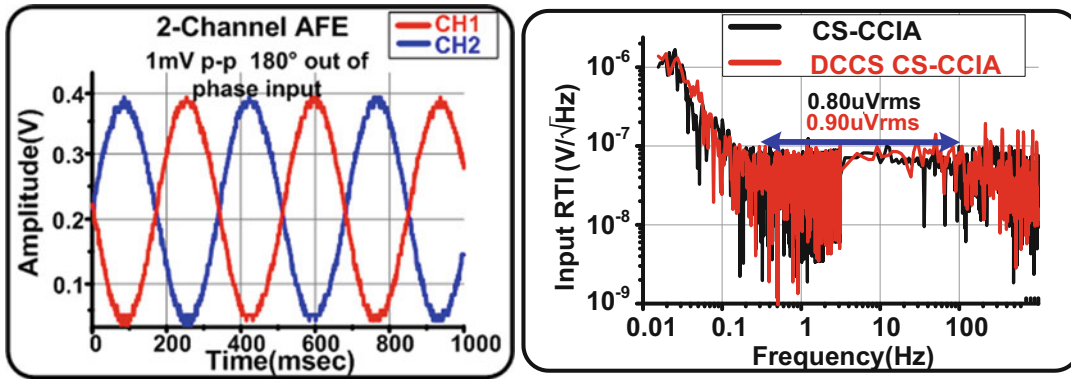

Fig. 12.23 Time-domain output of out-of-phase inputs, and the IA's input-referred noise

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