Chapter 2
Challenge of High Performance Bandgap Reference Design in Nanoscale CMOS Technology

Zhang Jun-an, Li Guangjun, Zhang Rui-tao, Yang Yu-jun, Li Xi, Yan Bo, Fu Dong-bing, and Luo Pu

2.1 Introduction

Reference circuit is a critical block in analog and mixed-signal circuits such as A/D converters, D/A converters or SOCs, and it can be used as an accurate reference signal or a steady bias source. Based on the development of semiconductor technology, IC's power supply voltage is becoming lower, so as the analog signal swing. But the resolution demands (by data converters for an example) may be constant, and that means the demand for reference signal is actually more critical. Most of the reference circuit concentrates on its DC performance than its AC performance, so the fast speed benefit from technology improvement had done nothing to a reference circuit design. On the contract, there are many negative effects in bandgap reference design caused by technology shrinking, such as low source voltage, large temperature coefficient of on-chip resistors, low EARLY

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voltage, large drain leakage current, etc., that will cause a great challenge to achieve a high performance bandgap reference circuit among a large temperature variation range.

This chapter is arranged as follows. Sect. 2.2 discusses five negative effects of nanoscale CMOS technology in bandgap reference design. Sect. 2.3 presents a bandgap reference circuit implementation with measurement results and comparison. Sect. 2.5, conclusion.

2.2 Negative Effects of Nanoscale CMOS Technology in Bandgap Reference Design

2.2.1 Voltage Headroom Decrease

As CMOS technology is shrinking, MOSfet's power supply voltage is becoming lower, as shown in Fig. 2.1, there are not enough voltage headroom to achieve the conventional bandgap reference circuit.

To deal with this problem, many low voltage reference circuit schemes are presented in recent published literatures [1–18]. Figure 2.2 shows the first kind of low voltage bandgap reference circuit named current-mode bandgap reference [1] which utilizes a reference current (temperature independent) and a resistor to generate a reference voltage. The value of reference current and resistor can be choosed freely, so the reference voltage output will not be limited by the source

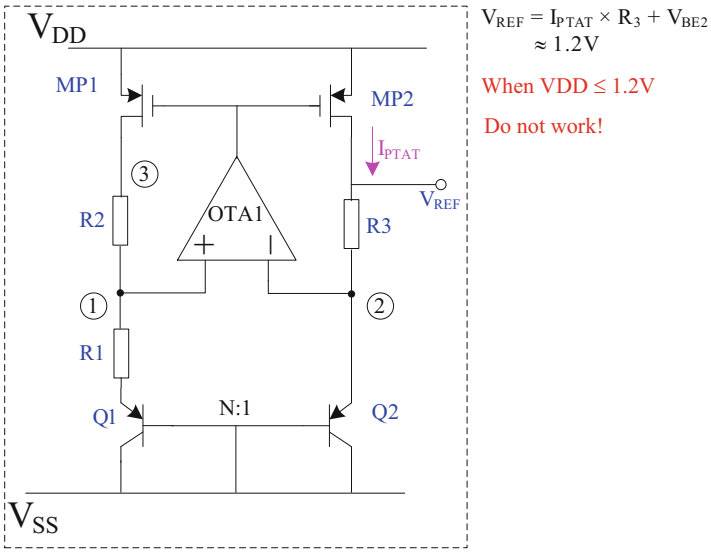

Fig. 2.1 Conventional bandgap circuit

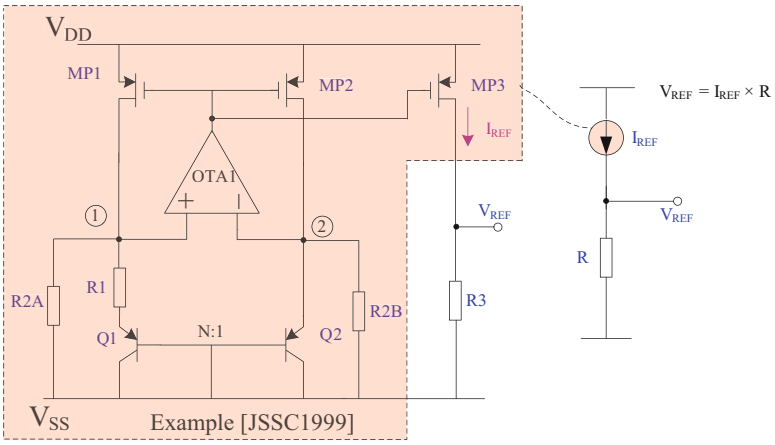

Fig. 2.2 Curent-mode low voltage bandgap reference circuit

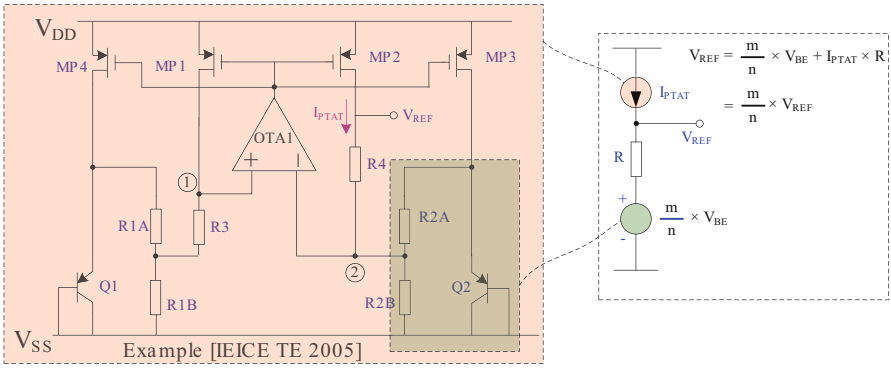

Fig. 2.3 Fractional low voltage bandgap circuit

voltage headroom. The lowest source voltage of the example circuit is about $V_{BE} + V_{DSAT}$ which can be lower than 1 V (regardless OTA's limitation).

Figure 2.3 shows the second kind of low voltage bandgap reference circuit named fractional bandgap reference [2] which utilizes a fraction of the P-N junction voltage (V_{BE}) added a PTAT voltage (which is achieved by a PTAT current with a resistor) to generate the reference voltage. The value of reference voltage is a fraction of the conventional bandgap voltage (≈1.2 V), and it also can be lower than 1 V. The lowest source voltage of the example circuit [13] is the minimum of $V_{REF} + V_{DSAT}$ with $V_{BE} + V_{DSAT}$ (regardless OTA's limitation).

Figure 2.4 shows the third kind of low voltage bandgap reference circuit which principle likes the output common voltage extraction in full differential operational amplifier [3]. The common voltage of a PTAT voltage and a CTAT voltage will achieve a temperature independent reference voltage if the opposite temperature coefficient can be counteracted perfectly. The value of reference voltage is 1/2 of

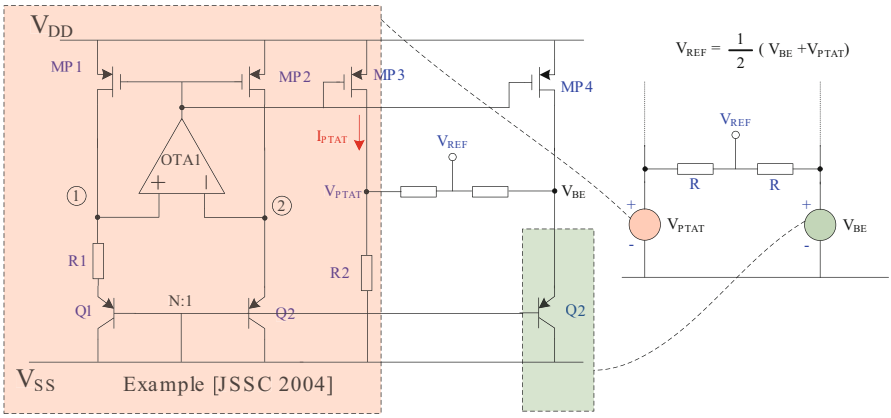

Fig. 2.4 Common voltage extraction method bandgap circuit

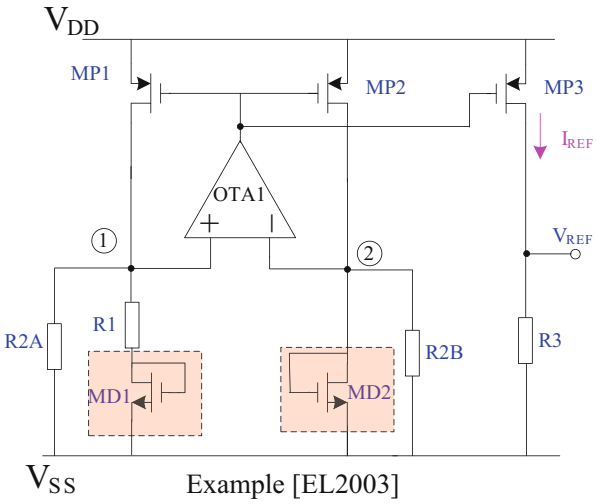

Fig. 2.5 Current-mode bandgap reference circuit with MOSfet

conventional bandgap voltage (≈0.6 V). The lowest source voltage of the example circuit is the minimum of $V_{PTAT} + V_{DSAT}$ with $V_{BE} + V_{DSAT}$ (regardless OTA's limitation).

MOSfet can be used to replace the bipolar transistor, because the threshold voltage (V_{TH}) has the similar temperature characters as P-N junction voltage (V_{BE}). As shown in Fig. 2.5, MD1 and MD2 have been used to replace the bipolar transistor [4]. Due to the threshold voltage of MOSfet is lower than P-N junction voltage, the source voltage of reference circuit can be even lower. Figure 2.5 shows that the current-mode bandgap reference circuit's lowest source voltage is $V_{TH} + V_{DSAT}$ (regardless OTA's limitation). Comparing with P-N junction voltage, the threshold voltage of MOSfet is considered as unsteady, the variation range of process corner is large, so some extra process step must be utilized to adjust it.

There are many other architectures and methods of low voltage reference circuit. Some method utilizes special devices (DTMOS [5]) and some others utilize special technology (CMOS/SOI [6], hybrid with Germanium diode [7]). In now days, the level of source voltage decreasing is slowed down, but the trend is inevitable. In the future, some new architectures and methods would be innovated continuously.

2.2.2 Large Temperature Coefficient of On-Chip Resistors

As shown in Fig. 2.1, the conventional bandgap reference circuit output a reference voltage directly, and it can be expressed as Eq. (2.1):

$$V_{REF} = \frac{R_3}{R_1} V_T \ln N + V_{BE2} \tag{2.1}$$

When R_1 and R_3 use the same type of resistor, temperature coefficient of the resistors will not affect the reference voltage (V_{REF}).

But the current-mode bandgap reference circuit can only get a reference voltage through a reference current, and it can be expressed as Eq. (2.2) and Eq. (2.3):

$$I_{REF} = \frac{V_T \ln N}{R_1} + \frac{V_{BE2}}{R_{2A}} \tag{2.2}$$

$$V_{REF} = I_{REF} \times R_3 \tag{2.3}$$

Temperature coefficient of the R_3 will directly affect the reference voltage (V_{REF}). Current-mode bandgap reference circuit cannot obtain a high performance reference voltage if the used resistor's temperature coefficient are a large. On the other hand, when utilize the conventional bandgap circuit's reference voltage and a resistor to generate a reference current, this reference current will be affected by the resistor's temperature coefficient too.

Unfortunately, all the on-chip resistors provided by nanoscale CMOS technology have a large temperature coefficient. As shown in Fig. 2.6, the temperature sweep simulation results of all the resistors which is provided by a 65 nm CMOS technology.

As shown in Fig. 2.7, the smallest temperature coefficient on-chip resistor the variation value is $\Delta R = 2.4\%$ among -55 to 125°C which temperature coefficient is about 133 ppm/°C. This temperature coefficient is still large compared with a one-order bandgap reference.

As shown in Fig. 2.2, if R_3 set as only the smallest temperature coefficient on-chip resistor cannot achieve a high performance reference voltage.

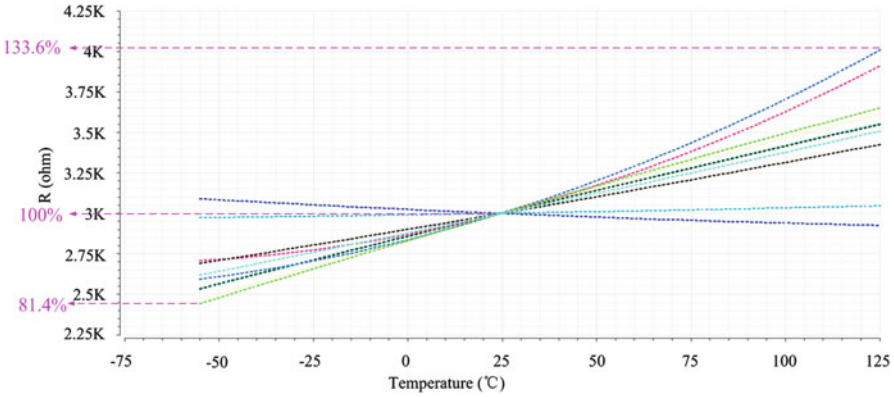

Fig. 2.6 Temperature performance simulation result of on-chip resistors

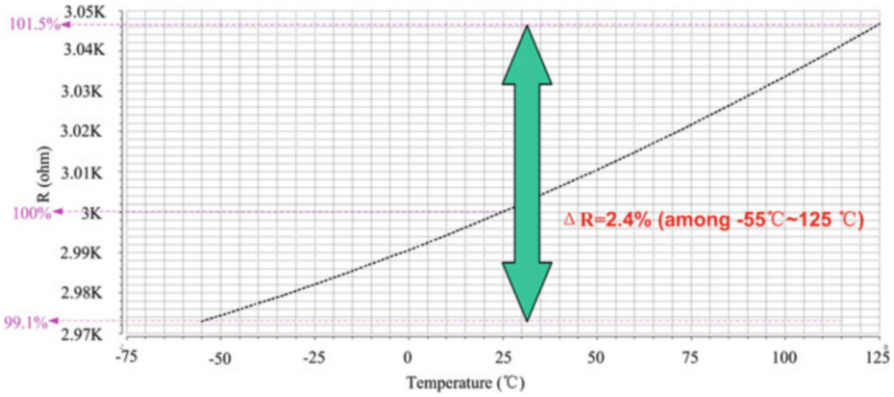

Fig. 2.7 The smallest temperature coefficient on-chip resistor

2.2.3 EARLY Voltage Decreasing

As CMOS technology is shrinking, MOSfet's EARLY voltage is becoming lower. As shown in Figs. 2.8 and 2.9, a PMOSfet V-I curve comparison between a 65 nm CMOS technology and a 0.18μm CMOS technology. It can be seen from Fig. 2.8 that in 65 nm CMOS technology EARLY voltage of PMOSfet with the smallest gate length decreased sharply. It can be seen from Fig. 2.9 that in different technology, even choosing the same transistor size the EARLY voltage is still different.

The negative effect of EARLY voltage decreasing to a reference design is when using one stage current mirror [8, 9, 14] (even cascode current mirror [13] which needs more voltage headroom) with small gate length can not achieve an accurate current replication. Even large gate length MOSfet (which means large V_{TH}

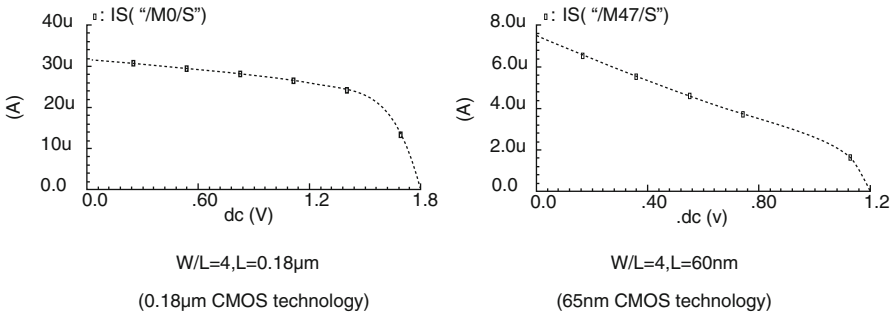

Fig. 2.8 PMOSfet V-I curve of different CMOS technology (smallest gate length)

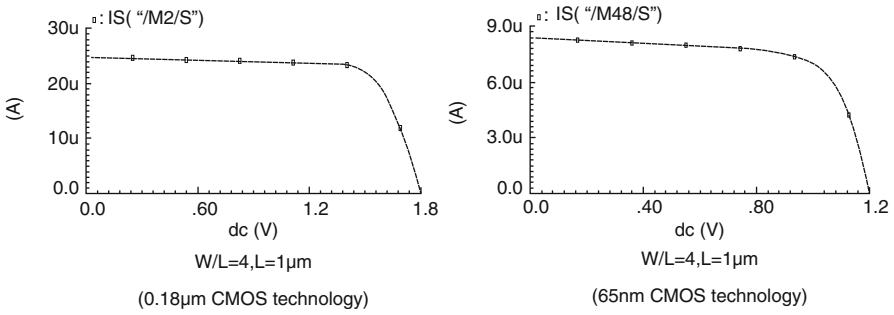

Fig. 2.9 PMOSfet V-I curve of different CMOS technology (same gate length)

consumed more voltage headroom) also cannot achieve an accurate current replication here. The reason is that the drain voltage of MP2 is a P-N junction voltage (V_{BE}), and the drain voltage of MP3 is expected to be a temperature independent voltage (V_{REF}). Due to V_{BE} has a large variation range among −55°C to 125°C, and with the EARLY voltage decreasing, one stage current mirror can not copy a current accurately.

Figure 2.10 shows the method which utilizes one stage current mirror to generate V_{REF}. Figure 2.11 shows the MP2 and MP3's drain current simulation result of Fig. 2.10, the length of MP2 and MP3 is set as 2 μm. The replication error is very large.

As shown in Fig. 2.12, a cascode current mirror is used for I_{REF} current replication. MP4's gate length is set as 2 μm too. The bias voltage of MP4 is generated from a diode-connected PMOSfet with a drain current which has a certain ratio with I_{D2}.

Figure 2.13 shows the MP2 and MP3's drain current simulation result of Fig. 2.12. The replication error is smaller than one stage current mirror, but for a high performance reference circuit this accuracy level is not enough.

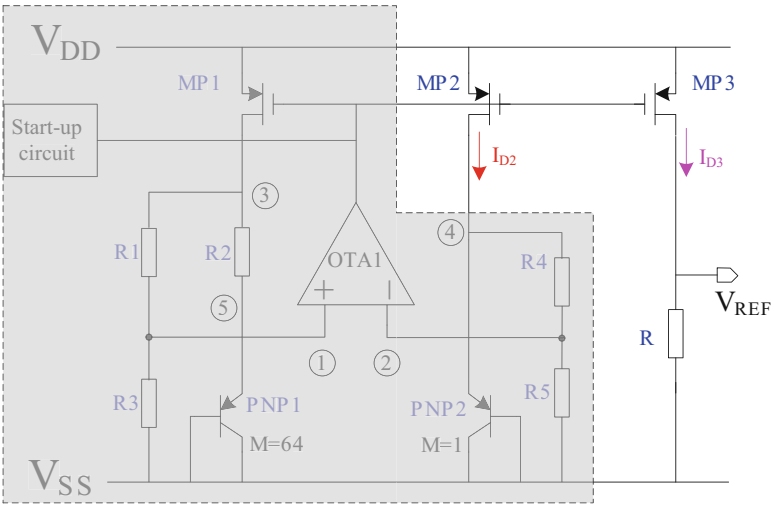

Fig. 2.10 One stage current mirror for V_{REF}

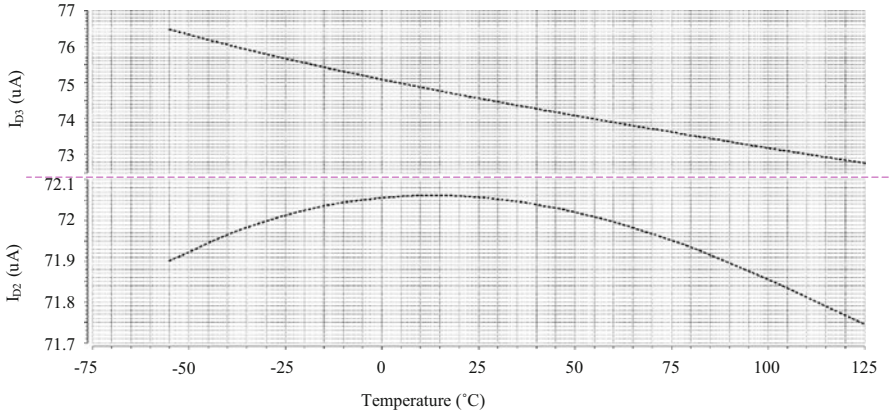

Fig. 2.11 Current replication performance by one stage current mirror

2.2.4 *Effect to DC Operation Points at Extreme Low Temperature*

Due to P-N junction voltage (V_{BE}) and MOSfet's threshold voltage (V_{TH}) all have a negative temperature coefficient, and a low voltage design is difficult to maintain suitable DC operation points in an extremely low temperature condition. Most of the published literatures' temperature range were not lower than −40°C [1–18].

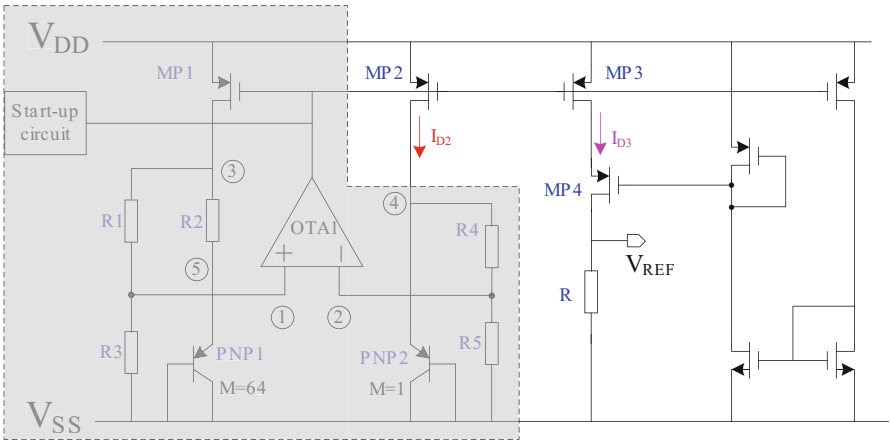

Fig. 2.12 Cascode current mirror for V_{REF}

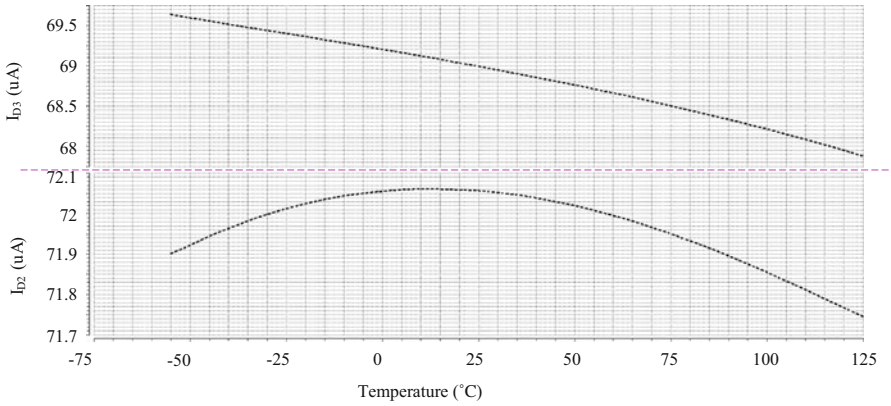

Fig. 2.13 Current replication performance by cascode current mirror

As mentioned in Sect. 2.2.1, all the lowest source voltages of the example reference circuits are regardless OTA's limitation. As Fig. 2.14 shows the lowest source voltage must fulfil Eq. (2.4):

$$V_{BE} + V_{TH\_P4} + V_{DSAT\_P4} + V_{DSAT\_P6} \leq V_{DD} \tag{2.4}$$

This is much larger than $V_{BE} + V_{DSAT}$ (the lowest source voltage limitation regardless of OTA), and the MOSfets of OTA may exceed the saturation zone in the extreme low temperature, so the OTA must be carefully designed.

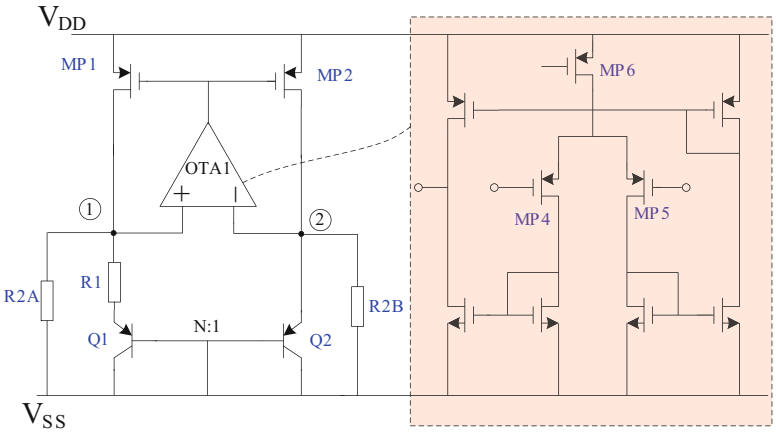

Fig. 2.14 Curent-mode low voltage bandgap reference circuit

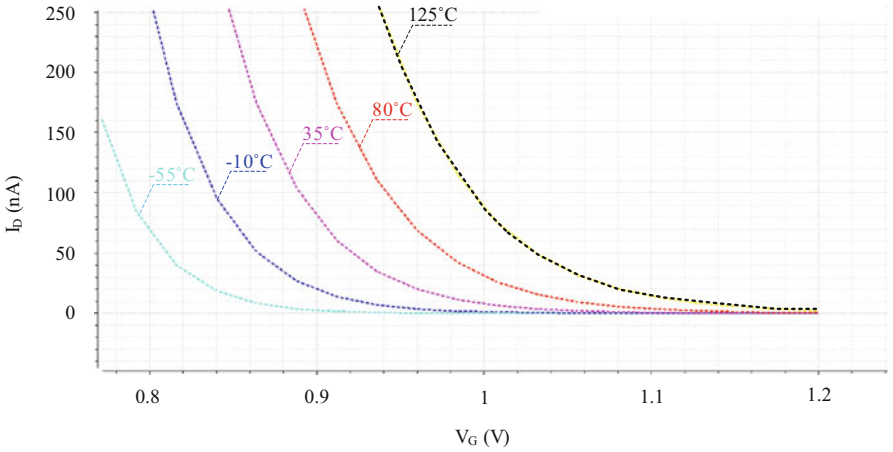

Fig. 2.15 Curent-mode low voltage bandgap reference circuit

2.2.5 Large Drain Leakage Current

Another negative effect in nanometer CMOS technology is the MOSfet's large drain leakage current. As shown in Fig. 2.15, a PMOSfet with a size as 300 nm/60 nm, and the source voltage (V_S) is 1.2 V, and the drain voltage (V_D) is 0 V. The gate voltage is swept from 0 V to 1.2 V in different temperature. The simulation result shows that in the temperature of 125°C V_{GS} is 0.2 V, the drain leakage current is beyond 100 nA.

The negative effect of large drain leakage current to a reference design is mainly the startup circuit. That because the start-up circuit will be designed as lower power

as possible, the operation current of the startup circuit may be less than 1 uA. If the leakage current and start-up circuit's operation current are at the same quantity level, the start-up circuit may lose its effectiveness, or the output state may be flipped and then affect the reference circuit's normal operation.

2.2.6 Summary

The discussed five effects caused by nanoscale CMOS technology are negative for a high performance reference circuit design. The only positive fact caused by CMOS technology shrinking is the higher manufacture accuarcy which means a smaller element mismatch. But the quantitative level of mismatch improvement cannot compensate all the negative effects. Furthermore, when a large temperature variation range is demanded, many reference circuits may not maintain a suitable DC operating point at every process corner and source voltage corner, and that will affect the circuit's yield. So, to design a high performance bandgap reference circuit among a large temperature variation range in nanoscale CMOS technology is very difficult.

2.3 A Bandgap Reference Circuit in 65 nm CMOS

2.3.1 Circuit Implementation

Figure 2.16 shows the schematic of the presented bandgap reference circuit. The bandgap core uses a classic low voltage bandgap architecture as literature [8], but due to low threshold voltage NMOSfets are utilized, the OTAs can use a simple architecture.

The principle of bandgap core can be explained as follows: MP1 and MP2 have the same W/L, and the emitter area ratio of PNP1 to PNP2 is set as 64. The node voltage $V_1 \approx V_2$ because of the feedback of OTA1, and lets $R_1 = R_4$, $R_3 = R_5$, so it can get $V_3 \approx V_4 \approx V_{BE2}$. The drain current of MP1(and MP2) can be expressed as Eq. (2.5):

$$I_D = \frac{V_3 - V_5}{R_2} + \frac{V_3}{R_1 + R_3} = \frac{V_{BE2} - V_{BE1}}{R_2} + \frac{V_3}{R_1 + R_3} = \frac{V_T \ln 64}{R_2} + \frac{V_{BE2}}{R_1 + R_3} \quad (2.5)$$

When a suitable value of R_1–R_5 is set, I_D can be temperature independent. It needs to be considered that the temperature coefficient of R_1–R_5 can not affect I_D's temperature characteristic if all the resistors are the same type (this will be verified by the measured results in Sect. 2.3.2).

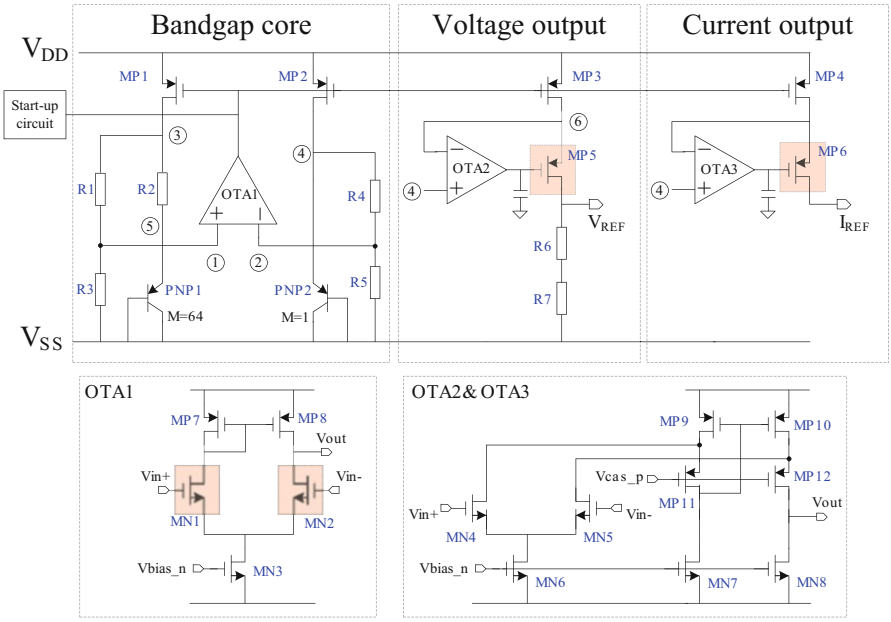

Fig. 2.16 The presented bandgap reference architecture

The input common-mode voltage of OTA1 (V_1/V_2) is a fraction of V_{BE2}, and this voltage must fulfil the Eq. (2.6):

$$V_1 \geq V_{DSAT\_N3} + V_{TH\_N2} + V_{DSAT\_N2}$$
$$\frac{R_3}{R_1 + R_3} V_{BE2} \geq V_{DSAT\_N3} + V_{TH\_N2} + V_{DSAT\_N2} \tag{2.6}$$

V_{DSAT} is the drain-source saturation voltage of MOSfet. V_1/V_2 may not fulfil Eq. (2.6) under extreme low temperature, to avoid this case, the input MOSfets of OTA1 (MN1/MN2) are choosed as low threshold voltage NMOSfet. PMOSfet input OTA also can be used here as literature [8], but in order to fulfil the output voltage range of OTA, two stage architecture must be utilized.

As Fig. 2.16 shown, the presented reference voltage output and current output circuit utilize the familiar architecture. OTA2 and OTA3 are used to obtain an accurate current replication and high DC PSRR performance. The principle is that let the drain voltage of MP3 and MP4 tracking MP1 and MP2 (and the gate voltage and source voltage of MP1–MP4 are equal) can obtain an accurate current replication under every PVT corner even the gate length of MP1–MP4 are small. Figure 2.17 shows the simulation result of current replication performance, compared with Fig. 2.11 and Fig. 2.13, the accuracy of the current replication are significantly improved.

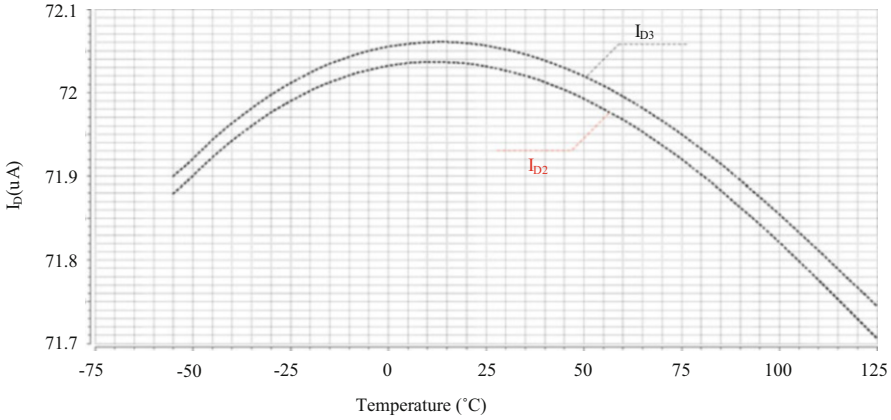

Fig. 2.17 Current replication performance by OTAs are utilized

The input common-mode voltage of OTA2 and OTA3 (V_4/V_6) is V_{BE2}, so MN4 and MN5 can utilize normal threshold voltage NMOSfet. The output voltage of OTA2&OTA3 must fulfil the Eq. (2.7) and Eq. (2.8):

$$\begin{aligned} V_6 &\geq V_{TH\_P5} + V_{DSAT\_P5} + V_{DSAT\_N8} \\ V_{BE2} &\geq V_{TH\_P5} + V_{DSAT\_P5} + V_{DSAT\_N8} \end{aligned} \tag{2.7}$$

$$\begin{aligned} V_6 - V_{REF} &\geq V_{DSAT\_P5} \\ V_{REF} &\leq V_{BE2} - V_{DSAT\_P5} \end{aligned} \tag{2.8}$$

V_{REF} is the reference output voltage. In order to fulfil the output voltage range of OTA2&OTA3, the MP5 and MP6 are choosed as low threshold voltage PMOSfet.

As shown in Fig. 2.18, R_6 and R_7 have the opposite temperature coefficient which is connected in series with suitable ratio to obtain a one-order temperature independent characteristic. This series connection's temperature curve also achieve a curvature which is inverse to the curvature of reference current's, as shown in Fig. 2.19, so a weak curvature compensation effect for voltage reference can be achieved.

Comparing with normal MOSfets, low threshold voltage MOSfets have many disadvantages such as large parameter variation range under PVT corners, large leakage current under very high temperature, inaccurate simulation model, etc. In this design, low threshold voltage MOSfets are only used in the feedback loop, and all those negative effects will be alleviated by OTA's close-loop feedback.

2.3.2 Measurement Results and Comparison

Figure 2.20 shows the photograph of this bandgap reference, and the chip is implemented in a 65nm CMOS technology, occupies 0.75 mm × 0. 67 mm

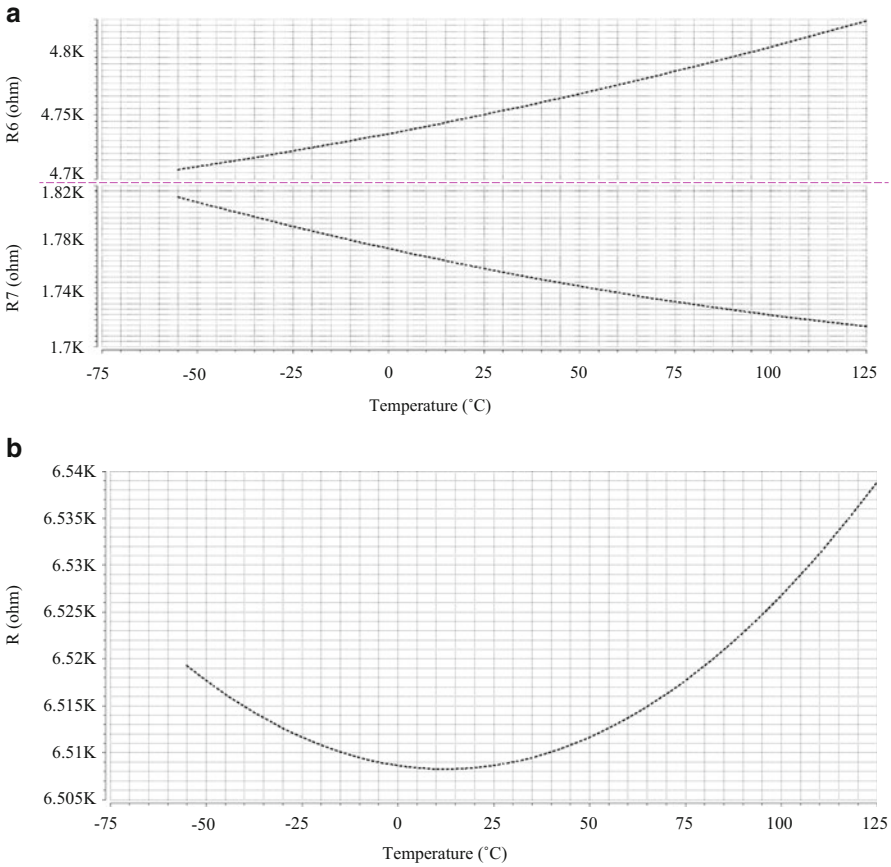

Fig. 2.18 One-order temperature independent resistor. (**a**) R6 and R7 with opposite TC. (**b**) TC of R6 and R7 in series connection

including bond pads, bonded in a D16S package. Test equipments include: Agilent 34401 multimeter, Agilent N6705B DC power analyzer, and THERMOJET-ES environmental testing apparatus.

Figure 2.21a shows the measured result of sampler1's current output, and Fig. 2.21b shows sampler1's voltage output. When measuring the current output, an external resistor is utilized to set the drain voltage of MP6 as similar as MP5's, and the external resistor is put outside of the temperature control box, so the temperature coefficient of external resistor will not affect the temperature performance of current output, and the measurement of current output's PSRR (DC) also utilizes this external resistor.

Figure 2.22a shows the measured DC power supply rejection performance of samplers1' current output under three temperature, and Fig. 2.22b shows the measured DC power supply rejection performance of samplers1' voltage output under three temperature.

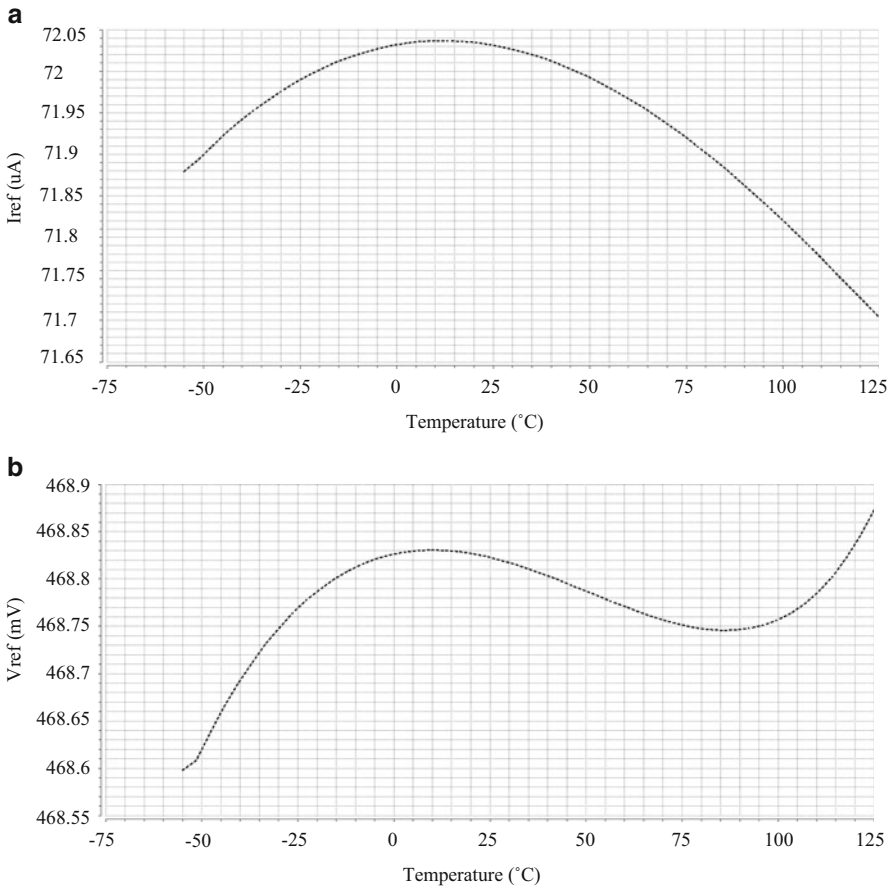

Fig. 2.19 Temperature performance of iref and vref 's simulation result. (**a**) Temperature Performance of IREF. (**b**) Temperature Performance of VREF

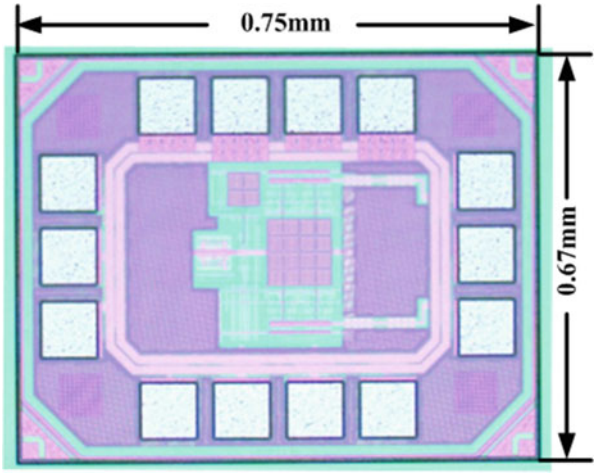

Fig. 2.20 Photograph of the bandgap reference chip

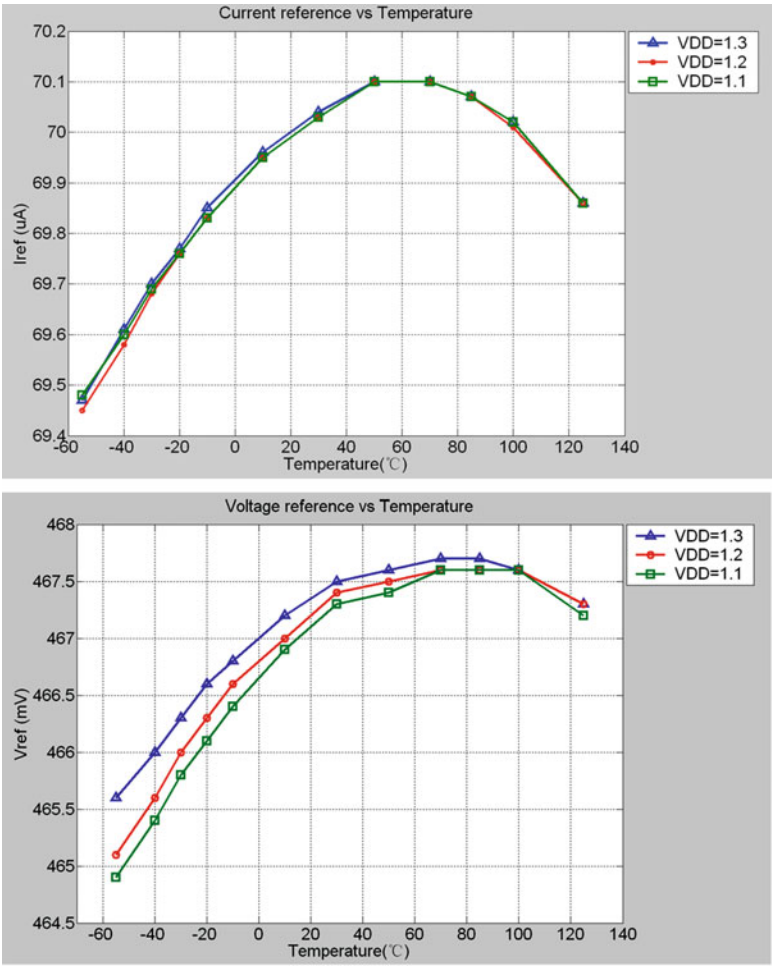

Fig. 2.21 Measured result of the bandgap reference (sampler1). (**a**) Temperature performance of current output. (**b**) Temperature performance of voltage output

Figure 2.23 shows the measured temperature performance of all 5 samplers' current output as $V_{DD} = 1.2$ V.

As shown in Fig. 2.23, all the five samplers' current output temperature curve is symmetric, that because the reference current output's temperature characteristic is based on a ratio of one type of resistor as mentioned in Sect. 2.3.1.

Figure 2.24 shows the measured temperature performance of all 5 samplers' voltage output as $V_{DD} = 1.2$ V.

As shown in Fig. 2.24, most of the five samplers' voltage output temperature curve is asymmetric, that because the reference voltage output's temperature

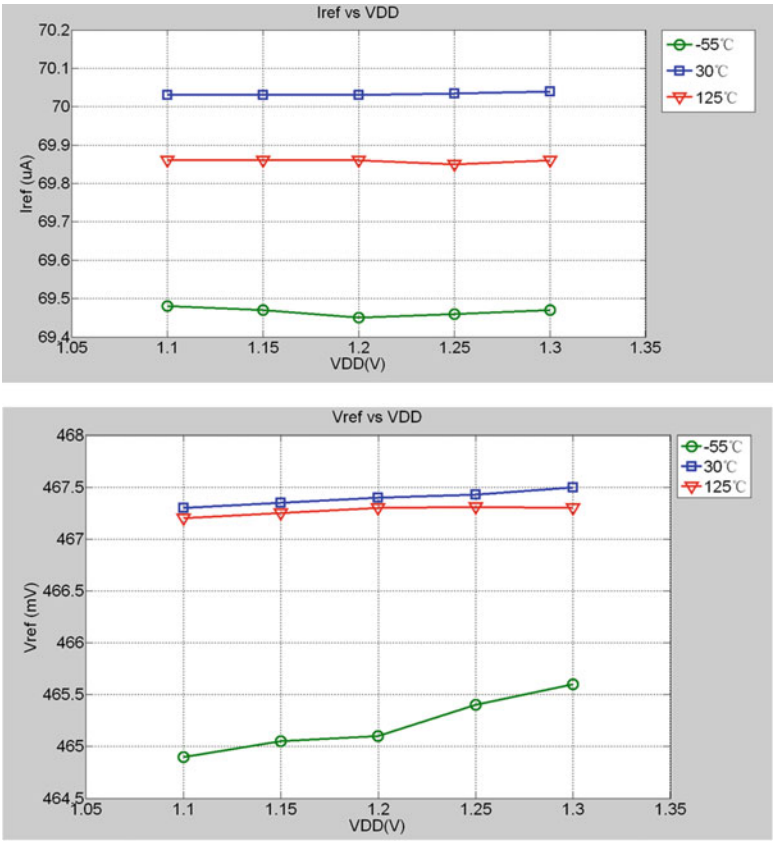

Fig. 2.22 Measured result of the bandgap reference (sampler1). (**a**) PSSR performance of current output. (**b**) PSSR performance of voltage output

characteristic is based on two types of resistors in series connection. Good matching for two types of resistors at only one time is nearly impossible, so a layout optimization can be done in the next manufacture to trimming this temperature curve, and an improved temperature performance can be expected.

Figure 2.25 shows the measured DC power supply rejection performance of all 5 samplers' current output as T = 30°C.

Figure 2.26 shows the measured DC power supply rejection performance of all 5 samplers' voltage output as T = 30°C.

Figure 2.27 shows the measured temperature performance of all 5 samplers' current and voltage output as $V_{DD} = 1$ V.

From Fig. 2.27, when $V_{DD} = 1$ V, all the 5 samplers start becoming invalid as the temperature below 0°C, and this is due to the unsuitable DC operation points.

Table 2.1 summarizes the measured performance.

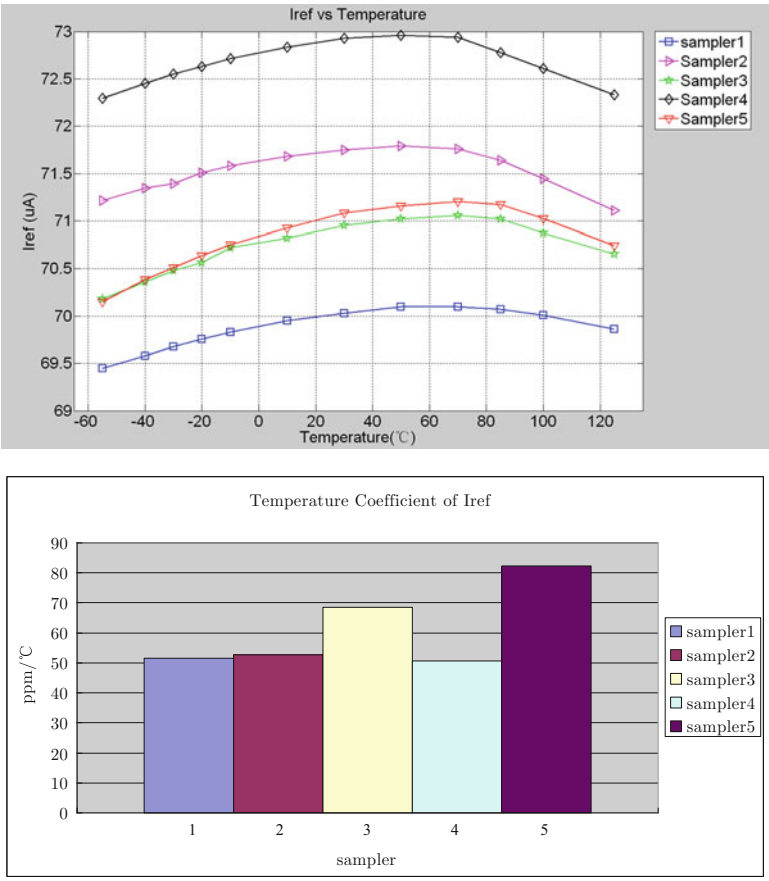

Fig. 2.23 Measured temperature performance of current output (5 samplers, VDD = 1.2 V). (**a**) Temperature performance of current output. (**b**) Temperature coefficient of current output

Table 2.1 compares the measured performance of the bandgap reference with several other published literatures'.

As shown in Table 2.2, because of low threshold voltage MOSfets are utilized, temperature range of the presented bandgap reference is larger than all of the listed literatures, and it can operate at the extreme low temperature (−55°C). The temperature coefficient of voltage output is better than current output, that due to the weak curvature compensation effect. DC PSRR also achieves a high performance as OTAs are utilized.

2.3.3 Summary

The presented bandgap reference circuit is implemented in 65 nm CMOS. To achieve a larger temperature range and a higher DC power supply rejection rate

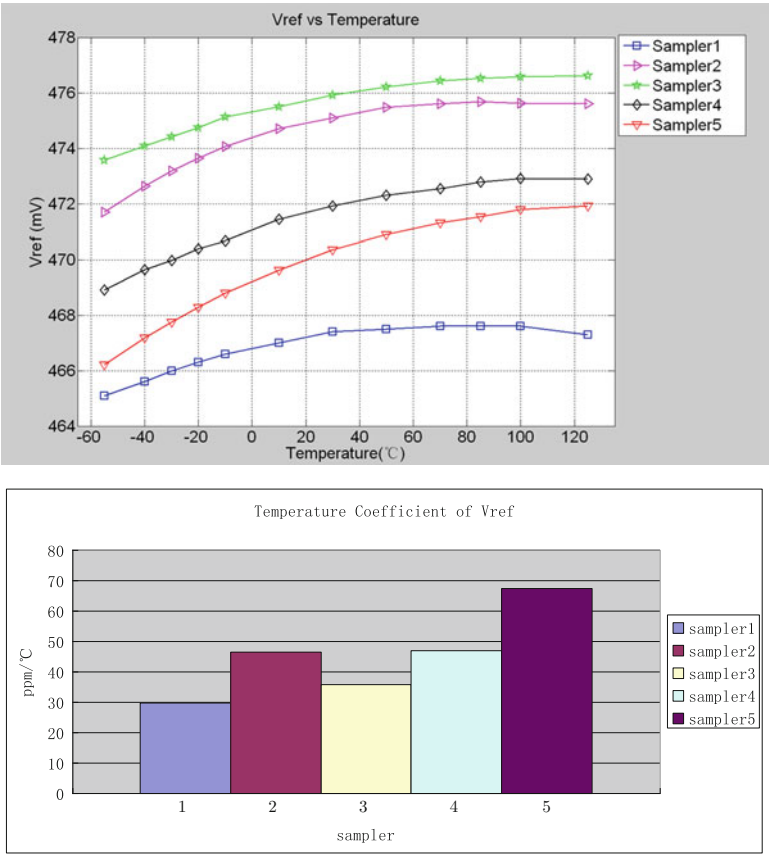

Fig. 2.24 Measured Temperature performance of voltage output (5 samplers, VDD = 1.2 V). (**a**) Temperature performance of voltage output. (**b**) Temperature coefficient of voltage output

(PSRR), low threshold voltage MOSfet and operational transconductance amplifiers have been utilized. A weak curvature compensation effect for reference voltage's generation have been achieved by two opposite temperature coefficient resistors in series connection. The measured results shows that the bandgap reference achieves all the design targets.

2.4 Conclusion

In this chapter, the authors discuss five negative effects caused by CMOS technology shrinking in high performance bandgap reference design, and then present a bandgap reference circuit implemented in a 65 nm CMOS with both voltage output and current output. The design includes three tips: first, low threshold voltage

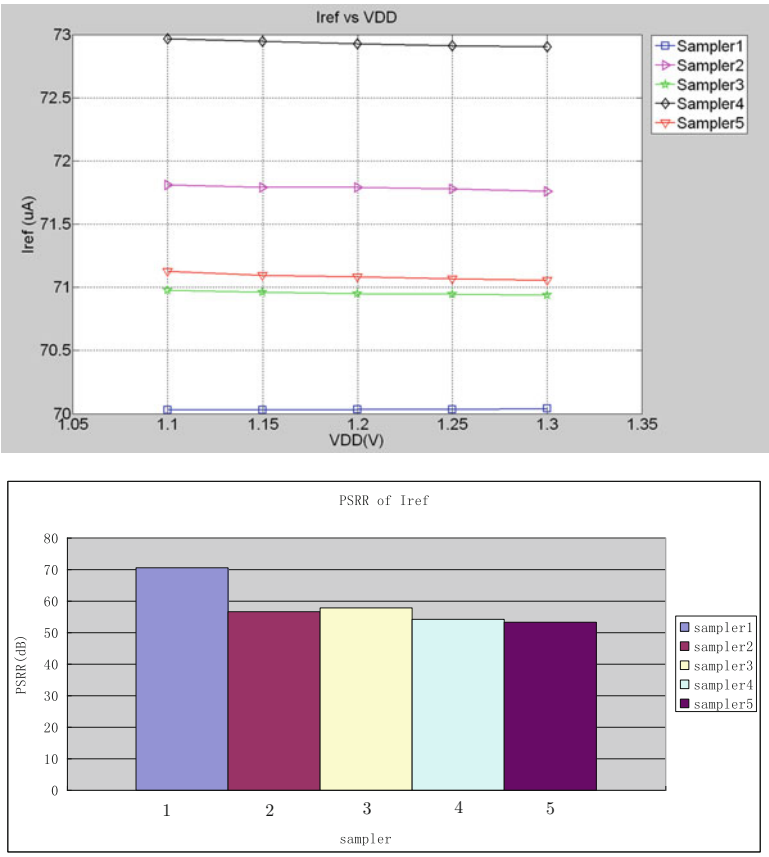

Fig. 2.25 Measured DC power supply rejection performance of current output (5 samplers, T = 30°C). (**a**) Reference current output versus VDD. (**b**) DC PSRR performance of current output

MOSfet have been utilized to obtain a suitable DC operating point at low temperature. Second, OTA has been used to obtain an accurate current copy and a high DC PSRR. Third, two opposite temperature coefficient resistors have been connected in series to obtain a one-order temperature independent resistor which also achieves a weak curvature compensation effect for reference voltage's generation. The measured results shows that the reference circuit achieves a higher DC PSRR and a smaller temperature coefficient, and the temperature range is −55°C to 125°C which is larger than most of the published literatures.

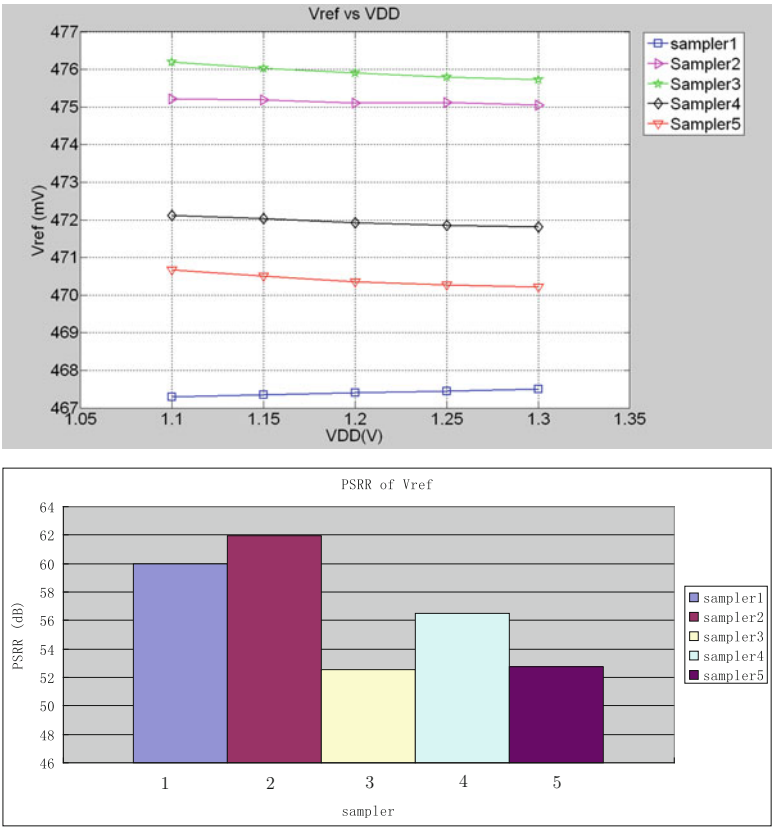

Fig. 2.26 Measured DC power supply rejection performance voltage output (5 samplers, T = 30°C). (**a**) Reference voltage output versus VDD. (**b**) DC PSRR performance of voltage output

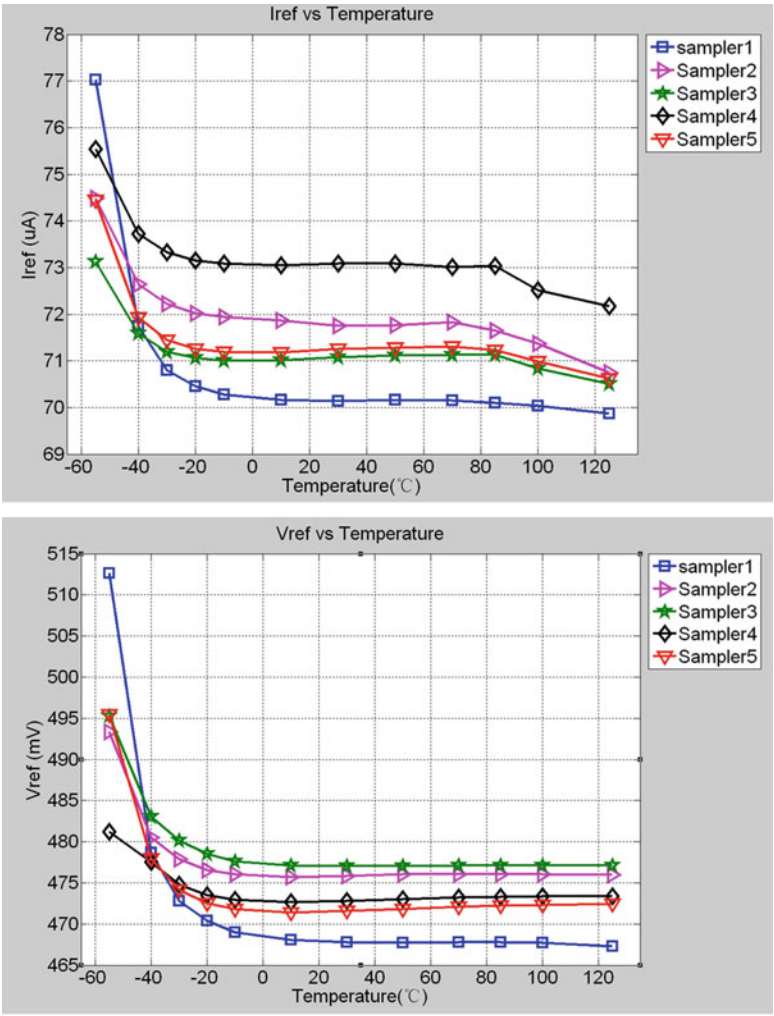

Fig. 2.27 Measured temperature performance of current and voltage output (5 samplers, VDD = 1 V). (**a**) Temperature performance of current output. (**b**) Temperature performance of voltage output

Table 2.1 Measured performance of the bandgap reference

Specification	Measured results
Technology	65 nm CMOS (with low V_{th} MOSfet)
Power supply	1.1–1.3 V (1.2 V typical)
Temperature range	−55–125°C
V_{REF}	468 mV
I_{REF}	70 uA
temperature coefficient	As shown in Table 2.2
PSRR (DC)	As shown in Table 2.2
Power consumption (1.2 V)	0.488 mW
Die area (including bond pads)	0.75 mm × 0.67 mm

Table 2.2 Comparison

Literature	V_{DD} V	TR °C	TC ppm/°C	Process nm	PSRR (DC) (room temp) dB
[8]	0.98–1.5	0–100	15	600	≈41[a]
[9]	1.2	−25–125	119	1200	40@5KHz
[10]	1.4	−20–100	12.4	350	68@100Hz
[11]	1	−40 to 125	11	500	≈86.4[b]
[12]	0.75	−20 to 85	40	130	≈86[b]
[13]	1.2	−40 to 120	4.5[c]	180	≈61[a]
[14]	0.9	0–100	19.5	250	≈30[a]
[15]	1.2/0.7	−40 to 120	147/114	180	≈33/43[a]
[16]	0.9	0–120	≈1030[d]	32	N/A
[17]	1.1	−40 to 125	6	28	≈81.5[b]
This work (V_{REF})	1.1–1.3	−55 to 125	30 (better)	65	60 (better)
			45 (average)		56 (average)
This work (I_{REF})	1.1–1.3	−55 to 125	52 (better)	65	70 (better)
			61 (average)		58 (average)

[a]Calculated from the literatures' temperature curve vs supply voltage
[b]Calculated from the literatures' line regulation, measurement result
[c]After trimming
[d]Calculated from the literatures' temperature curve

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