Chapter 1
High-k Dielectric for Nanoscale MOS Devices

Ling-Xuan Qian

1.1 Introduction

The Integrated Circuit (IC) industry has successfully followed the guidance of the Moore's law in the past decades: the number of transistors in a dense IC doubles approximately two years. Increasing integration level, reducing cost and power consumption while improving product performance has always been the primary goal of IC industry. In order to keep pace with the Moore's Law, it has been decades that device scaling is one of the essential focuses of the development of MOS technology.

After becoming the most important device for forefront high-density integrated circuits such as microprocessors and semiconductor memories, Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is becoming an important power device as well. Since 1970, the gate-length dimension of MOSFET in production ICs has been decreasing at a steady pace and will continue to scale down in the future, as shown in Fig. 1.1 [1].

However, as the scaling down of the MOS devices, the departures from long-channel behaviors, as known as the short-channel effects, are inevitable, leading to varieties of undesirable electrical phenomena. Up till now, the most widely used scaling rule to avoid short-channel effects is the "constant-field scaling", i.e. scale down all dimensions and voltage of a long-channel MOSFET so that the internal electric fields are kept the same [2]. In Fig. 1.2, the dimensions of MOSFET before and after scaling are compared, all dimensions including channel length (L), oxide thickness (T_{ox}), and junction depth (r_j) are ideally shrunk by a same scaling factor α. Noted that the doping level of the substrate increases by α and the applied voltages

L.-X. Qian (✉)
School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu, China
e-mail: lxqian@uestc.edu.cn

© Springer International Publishing AG 2017

T. Li, Z. Liu (eds.), *Outlook and Challenges of Nano Devices, Sensors, and MEMS*,
DOI 10.1007/978-3-319-50824-5_1

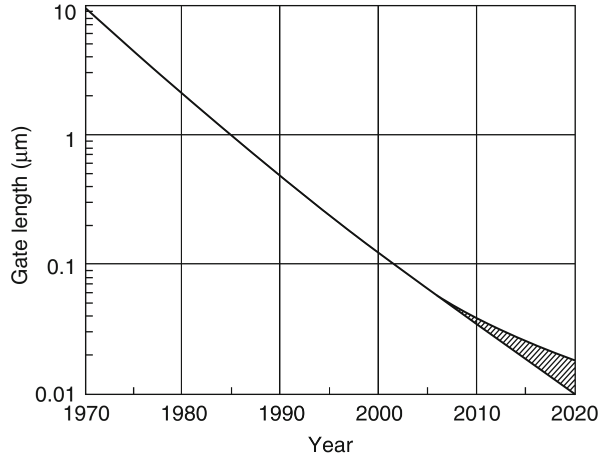


Fig. 1.1 Minimum gate length of MOSFET in commercial IC vs. the year of production [1]

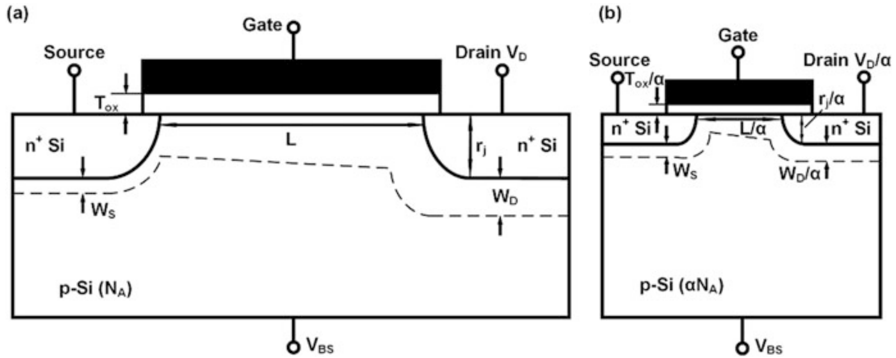


Fig. 1.2 Schematic diagram of MOSFET before and after scaling [2]. (**a**) Original device, (**b**) Scaled device

decreases by α, thus a reduction of the junction depletion width (W_D) by α occurs beneath the drain area. Unfortunately, the scaling factor in actual cases cannot achieve the ideal value because of the limitation of some other factors. Table 1.1 summarizes the ideal and actual scaling factors together with the limitation in scaling [2, 3].

Since the oxide thickness should also reduce with the device scales down according to Fig. 1.2 and Table 1.1, an oxide thickness of less than 3 nm is needed for MOS devices with channel length of 100 nm or less. Theoretically, the minimum physical thickness of SiO_2 is 0.7 nm with at least two layers of neighboring oxygen atoms to prevent the gate/SiO_2 and the SiO_2/Si interfaces from overlapping with each other, and thus make the gate insulator conductive [4]. But in fact, because of the quantum mechanical effects that carriers are capable of tunneling through the ultra-thin gate dielectric directly and leading to very large leakage

Table 1.1 Scaling factors and limitation factors of MOSFET

Parameters	Ideal scaling factor	Actual scaling factor	Limitation
Electric field	1	>1	–
Threshold voltage V_{th}	1/α	>>1/α	Leakage current
Gate length L	1/α	1/α	–
Oxide thickness T_{ox}	1/α	>1/α	Defects, tunneling
Junction depth r_j	1/α	>1/α	Resistance
Drain bias V_D	1/α	>>1/α	System and V_{th}
Substrate doping	α	<α	Junction breakdown

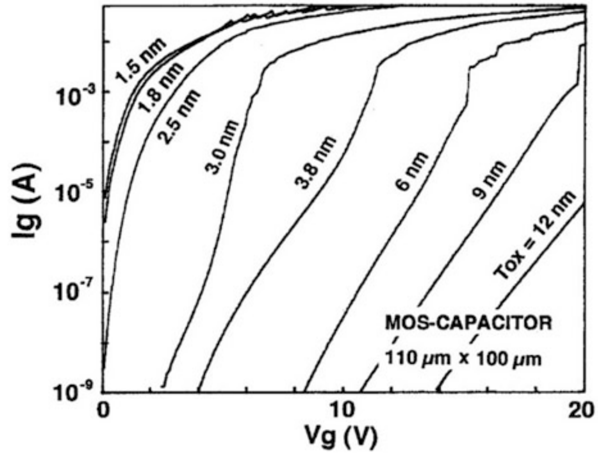


Fig. 1.3 Dependence of gate leakage current of MOS capacitors on the thickness of gate oxide [7]

current, the performance of the MOS devices are not suitable for actual application when the SiO_2 dielectric is thinner than 3 nm [5, 6]. Figure 1.3 shows the leakage current of MOS capacitors with different gate oxide thicknesses range from 12 nm down to 1.5 nm, it is obvious that capacitors with gate oxide thinner than 2.5 nm have a significant leakage component in low gate bias region caused by direct tunneling. Especially when $T_{ox} = 1.5$ nm, the leakage current reaches the order of 1×10^{-3} A/cm^2, which is not tolerable [7].

Apart from leakage current, device reliability is another essential factor that should not be ignored, the 10-year reliability criterion of CMOS technology cannot be guaranteed in devices with gate oxide thinner than 2 nm [8]. For example, a series of physical and chemical phenomena caused by dielectric degradation due to the emission of hot electrons at the Si/SiO_2 interface will eventually lead to the breakdown of the gate dielectric.

Back to 2007, in the reports of International Technology Roadmap of Semiconductors (ITRS), it was mentioned that equivalent gate oxide thickness (EOT) is the most difficult challenge associated with the future device scaling. For high-performance applications, EOT of less than 1 nm with adequate reliability is

needed, while on the other hand, for low-power applications, leakage current caused by ultrathin gate oxide must be decreased. Moreover, in the executive summary of 2013 ITRS, the reduction of EOT was mentioned still to be a difficult challenge in the near term.

With the advantages of thermodynamically and electrically stability, superior electrical isolation properties, low mid-gap interface state densities with Si (10^{10}/cm^2), high dielectric strength (15 MV/cm), etc. [9], thermally grown amorphous SiO_2 as gate dielectric has kept its predominance in the past decades. However, as the existence of the limiting factors mentioned above, measures must be taken in order to keep the scaling trend of integrated devices without sacrificing the performance of the devices. Therefore, the idea of replacing conventional SiO_2 with material with high dielectric constant is proposed.

1.2 High-k Dielectrics and Electrical Performance

1.2.1 Dielectric Constant

Dielectric constant (k), as known as relative permittivity, is a factor that reflects decreasing of the electric field between charges relative to vacuum, which can be defined by Eq. (1.1):

$$k = \frac{k(\omega)}{k_0} \tag{1.1}$$

where k(ω) is the complex frequency-dependent absolute permittivity of the material, and k_0 is the permittivity of vacuum. Since the accumulation capacitance per unit area (C_{ox}) of an MOS capacitor equals to:

$$C_{ox} = \frac{kk_0}{T_{ox}} \tag{1.2}$$

the k value of a material is usually calculated by Eq. (1.3):

$$k = \frac{C_{ox}T_{ox}}{k_0} \tag{1.3}$$

It is well known that the saturation current (I_D) of a MOSFET can be written as:

$$I_D = \frac{W}{2L}\mu C_{ox}\left(V_g - V_{th}\right)^2 \tag{1.4}$$

in which W and L are the channel width and length, μ is the carrier mobility, Vg is the gate bias and V_{th} is the threshold voltage of the MOSFET. Therefore, during

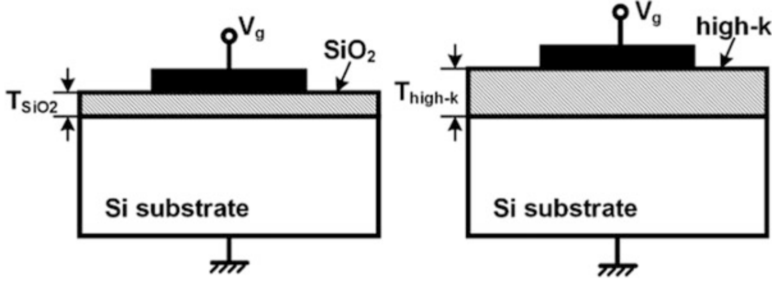


Fig. 1.4 Illustration of high-k material replacing SiO_2

scaling down, in order to maintain a certain level of drive current that can make the device functional, C_{ox} must be increased or at least be kept constant. As discussed in the last section, it is almost impossible to further decrease the thickness of SiO_2, replacing SiO_2 with other material with higher k value is the only way to increase C_{ox}. After replacement, the equivalent oxide thickness (EOT) can be calculated as:

$$EOT = \frac{k_{SiO2}}{k_{high-k}} T_{high-k} \tag{1.5}$$

meaning that the device with high-k material as gate dielectric is capable of achieving the same capacitance as the conventional SiO_2 based device but with larger physical thickness, which can also solve the problem of the unacceptable leakage current caused by direct tunneling, as shown in Fig. 1.4.

The first high-k material studied was silicon oxynitride (SiO_xN_y), K.S. Krisch et. al found that nitrogen can be effectively incorporated into SiO_2 by annealing the film in NH_3 or other gas contains nitrogen, and thus the reliability of the dielectric is improved [10]. Besides, doping N into SiO_2 is also reported to be able to reduce oxide charges and border traps [11]. However, if the N doping concentration is too high, the positive charges induced will cause large threshold voltage shift and interface degradation. In 2007 ITRS reports, it was mentioned that silicon oxynitride no longer meet the strict leakage current requirement anymore, therefore, material with high k value should be studied.

1.2.2 Selection of High-k Dielectric

Figure 1.5 demonstrates the k values together with band gaps of the promising candidates in high-k materials, however, it is never a simple job to determine which one is the best choice because there is always a trade-off between k value and the band offset that band gap of metal oxides tends to vary inversely with k value [12]. For example, as shown in Fig. 1.5, TiO_2 with k value of 80 has a band gap of only 3.3 eV, and the k value of one of the perovskite oxide $SrTiO_3$ can reach around

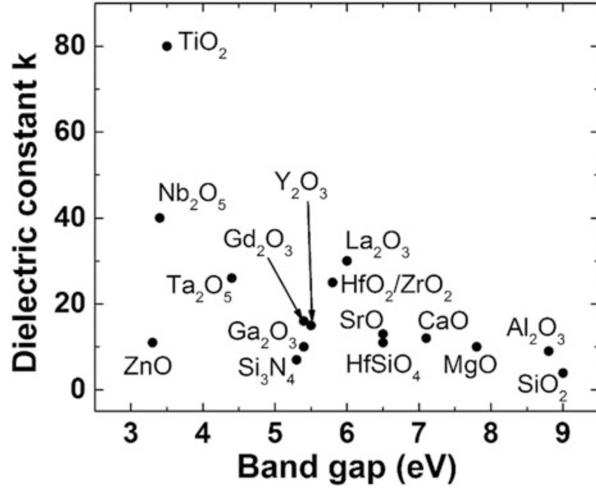


Fig. 1.5 k value vs. band gap of promising candidates as gate dielectric

2000, but its band gap is even smaller (3.2 eV). Therefore, apart from k value, band gap is also an important criterion of choosing dielectric material. Band gap should be large enough (usually over 5 eV) to make sure the dielectric material is an insulator, besides, the band offset with Si substrate should also be large enough (usually over 1 eV) so that the Schottky emission of carriers into the oxide band can be prevented [13].

Moreover, since the interface between high-k dielectric and Si substrate is the dominant factor that that influence the electrical performance of MOS devices, kinetic and thermodynamic stability should be considered as another important criterion. In ideal devices, there should be no reactions between the dielectric film and the substrate, and no interfacial layer should be formed either. Unfortunately, most high-k materials are compatible with Si at some certain processing conditions [14]. Assuming the high-k dielectric is M_xO_y, then there are basically four types of reactions between M_xO_y and Si [15–17]:

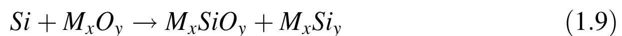
1. Silicon oxidation

$$Si + M_xO_y \rightarrow SiO_2 + xM \tag{1.6}$$

2. Silicide formation

$$Si + M_xO_y \rightarrow SiO_2 + M_xSi \tag{1.7}$$

$$Si + M_xO_y \rightarrow M_xSiO_y + M \tag{1.8}$$

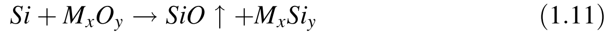


$$Si + M_xO_y \rightarrow M_xSiO_y + M_xSi_y \tag{1.9}$$

3. Silicon oxide layer might be formed on the Si surface during the growth of the dielectric film or annealing, which enables the formation of silicates

$$SiO_2 + M_xO_y \rightarrow M_xSiO_y \tag{1.10}$$

4. SiO gas formation at low oxygen pressures and diffuse through the oxide film



$$Si + M_xO_y \rightarrow SiO \uparrow + M_xSi_y \tag{1.11}$$

These reactions will induce large amount of dangling bonds, oxygen vacancies and traps that negatively impact the device performance, and the SiO_2 layer formed will decrease the k value of the gate stack and thus nullify the benefit of high-k dielectric. Therefore, it is essential to choose a dielectric with large Gibbs free energy and low oxygen diffusion coefficient to inhibit the reactions with Si and the formation of the low-k SiO_2 interfacial layer during annealing at high temperature [18, 19].

1.2.3 Defects and Interfaces of High-k Dielectrics

When compared with SiO_2, high-k oxides contain more defects because firstly, off-stoichiometry defects such as oxygen vacancies in SiO_2 are rare because of the high heat during its formation [20]. Secondly, unlike the covalent bonding SiO_2, high-k oxides have ionic bonding and have larger coordination number, making high-k oxides poor glass formers. Therefore, it is much easier for them to crystallize during high temperature annealing, as a result, it is difficult for the crystal network to relax and rebond to remove the defects [21].

In ionic oxides, the intrinsic defects are oxygen vacancies and oxygen interstitials. Forster et al. calculated the energy levels of the defects in HfO_2 and ZrO_2 as shown in Fig. 1.6, in which V^+ and V^{2+} represent positively charged oxygen vacancies and O^0, O^{20}, O^-, O^{2-} are oxygen interstitials which are negatively charged [22, 23]. It is found that the defects are capable of trapping electrons from Si substrates, but further work is still needed to study the mechanism of the defects.

Besides, hydrogen is another type of defect which comes from forming gas (N_2 + H_2) annealing or the deposition of high-k film using atomic layer deposition (ALD). Reports show that hydrogen acts as shallow donor in most of the oxide materials (HfO_2, ZrO_2, La_2O_3, Y_2O_3, TiO_2, $LaAlO_3$ and $SrTiO_3$, etc.), while in silicates, SiO_2 and Al_2O_3 hydrogen is deep donor and therefore a source of fixed charge [24, 25]. The sign of the fixed charges in different oxides depends on the position of H_0 energy level with respect to their band gaps. For example, in HfO_2, ZrO_2, La_2O_3, Y_2O_3, level of H_0 lies above the band gap of Si, so the hydrogen in these oxides tends to ionize as H^+ and donate electrons to Si, and thus positive fixed

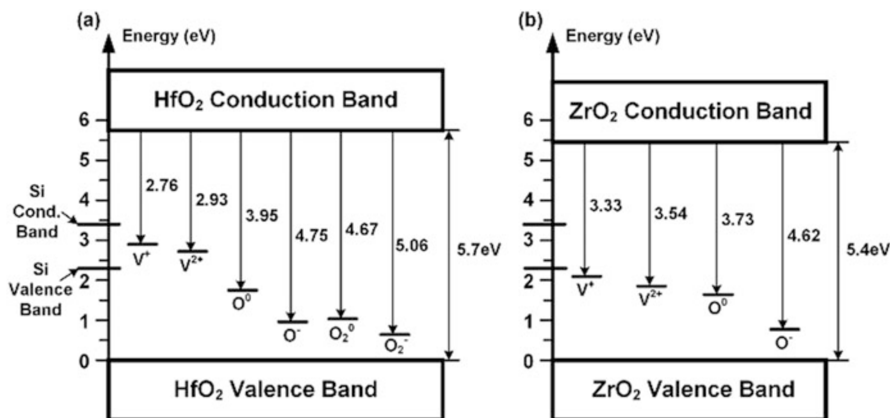


Fig. 1.6 Energy levels of the defects in (**a**) HfO_2 and (**b**) ZrO_2 [19, 20]

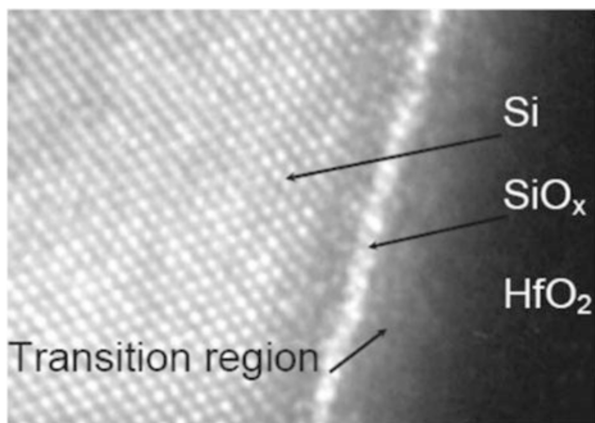


Fig. 1.7 TEM graph of HfO_2/Si interface [24]

charges are formed. Whereas, the H_0 level in Al_2O_3 locates below the band gap of Si and tends to capture electrons to form positive fixed charge. Therefore, in consistent with experimental results, the fixed charge in HfO_2 and ZrO_2 is usually positive but in Al_2O_3 it is negative [14, 26].

As mentioned in the previous section, most of the high-k oxides have poor kinetic and thermodynamic stability, leading to the formation of unstable and undesirable interfacial layer, and thus worsen the interface quality. For example, the low Gibbs free energy of Ta_2O_5 and TiO_2 makes them easy to react with Si at 1000 K [16], also, and interfacial layer SiO_x can be formed after depositing HfO_2 directly on Si (Fig. 1.7) [27]. These will cause a high interface charge density Dit. Reports show that most high-k dielectrics have high D_{it} (~10^{11}–10^{12} cm^{-2} eV^{-1}) and result in mobility degradation and flatband voltage shift [14]. Therefore, in order to improve the interface quality, the idea of adding a buffer layer between Si

and high-k material is proposed [28]. According to Gutowski et al. a stable interface silicate layer can be formed between HfO_2/ZrO_2 and Si if a thermal treatment is implemented after the deposition of the dielectric, and this silicate layer is frequently used as buffer layer [29].

Apart from the interface between high-k and Si substrate, the high-k/gate interface is also an important factor that influence the device properties. Since the capacitance degradation in the depleted polysilicon electrode cannot be ignored in ultrathin gate dielectric, plus most high-k materials are thermally unstable and easy to crystallize, polysilicon is no longer a suitable gate material and metal gates are needed [30]. The selecting criteria of metal gate includes work function, ease of processing, thermal stability, etc. Up till now, single metal (Al, Ti, W, Hf, Ta, Mo, Ru, Au, Ni and Pt), metal nitrides (TaN, TiN, MoN and WN), metal silicide (CoSi and NiSi) and metal oxide (RuO_2) have already been investigated.

Figure 1.8 shows the work functions of some common metals. It is known that mid-gap metals are not capable of providing suitable work function on high-k dielectrics and thus negatively impact the performance of the transistor. Therefore, mid-gap metals like W, Fe, Cr, Mo, etc. cannot be used as the gate of MOS devices. In order to achieve relatively low and symmetry threshold voltage for nMOS and pMOS devices, alloy materials with tunable work function are preferable [31]. Moreover, the work function can be further tuned by adding different content of nitrogen such as TiAlN [32, 33].

It is well known that a high-temperature annealing is usually needed for metal gates so that ohmic contact can be formed. For metal nitride gate, during the annealing, nitride tends to diffuse into the dielectric bulk, which is capable of reduce the density of oxide charges by passivating oxygen vacancies in the high-k layer and also decrease D_{it} at high-k/Si interface [34]. However, the intermixing of the metal atom and the high-k metal atom may happen at the same time, which will negatively influence the characteristic of the gate stack [34].

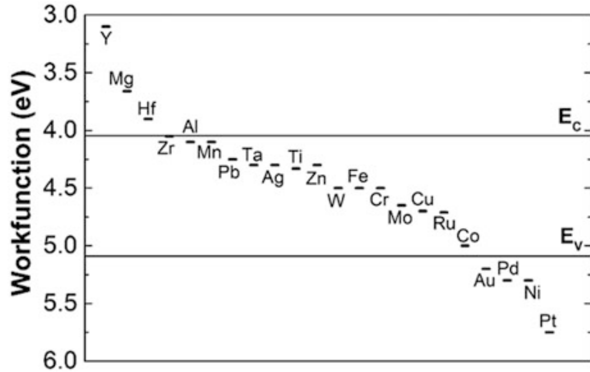


Fig. 1.8 Work functions of different metals

1.2.4 Mobility Degradation and Threshold Voltage Shift

Because of the existence of the defects in dielectric bulk and the interface states mentioned in the previous section, carrier mobility will be degraded due to various scattering mechanisms at both Si bulk and high-k/Si interface. The effective channel carrier mobility (μ_{eff}) is varies as a function of gate effective field and determined by Coulombic scattering (μ_{coul}), phonon scattering (μ_{ph}), and surface roughness (μ_{rough}) at low, moderate, and high fields respectively, which can be calculated by Eq. (1.12) according to Matthiessen's rule.

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{coul}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{rough}} \tag{1.12}$$

MOSFETs with high-k gate oxide exhibit lower electron mobility than FETs with SiO_2 gate oxide, as shown in Fig. 1.9 [26]. The exact cause of the degradation in mobility still needs more works to make sure, but several reasons can be deduced according to the studies up till now. Firstly, the higher oxide trap and interface trap of high-k oxide than that of SiO_2 enhances the Coulomb scattering. Secondly, a large amount of optical phonons in high-k oxides have low-lying soft polar mode, leading to a remote scattering of carriers, and thus limit the carrier mobility [35]. It has been reported that the soft phonon mechanism can be inhibited by using $HfSiO_4$ ($ZrSiO_4$) or adding a SiO_2 buffer layer to keep the high-k dielectric away from the channel [36, 37], however, this will inevitably increase EOT. In addition, high-k oxides have larger surface roughness than SiO_2 due to the longer bond length of metal-O and metal-Si than that of Si-Si.

Charge-trapping centers can be induced by the large amount of fixed charges locate in high-k materials, leading to a threshold voltage (V_{th}) shift which is another

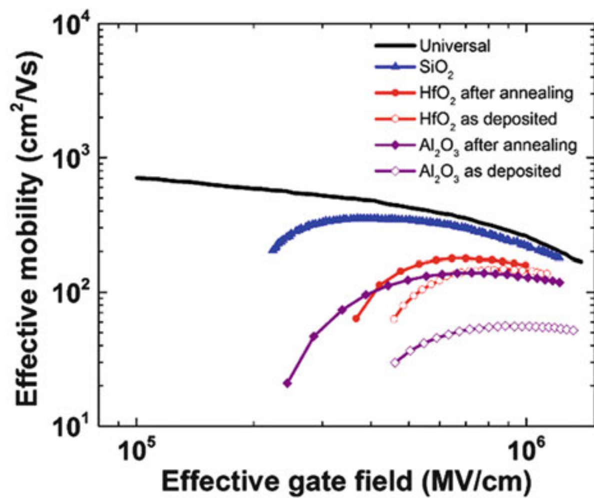


Fig. 1.9 Comparison of electron mobility in devices with high-k and SiO_2 dielectric [26]

concern of applying high-k oxides in MOSFETs. Besides, the reasons for V_{th} shift also include Fermi-level pinning effect at high-k/Si interface which can be modeled by the metal-induced gap states (MIGS) theory [38, 39]. In MIGS theory, the Schottky barrier height is given by:

$$\Phi_n = S_p(\Phi_m - \Phi_{CNL}) + (\Phi_{CNL} - \chi_S) \tag{1.13}$$

where Φ_{CNL} is the charge neutrality level, Φ_M and χ_S are the work function and the electron affinity of the semiconductor substrate, then the derivational Fermi-level pinning parameter S can be obtained as:

$$S = \frac{1}{1 + q^2 N_{it}\delta/\varepsilon_0\varepsilon_{Si}} \tag{1.14}$$

in which Nit is the interface states density per unit area and δ is their extent into the semiconductor. In ideal case, there is no interface states, so the parameter S = 1 and no Fermi-level pinning happens. On the contrary, if S approaches to 0, high density of states exist at/near the high-k/Si interface and the device will suffer from sever Fermi-level pinning, leading to the variation of Schottky barrier height and thus the shift of V_{th}.

Experimentally, take HfO_2 as an example, Fig. 1.10 is the comparison between C-V characteristics of MOS capacitors measured at different temperatures with HfO_2 as gate dielectric with and without nitrogen incorporation [40]. The large negative flat band voltage (V_{fb}) found in the sample without nitrogen proves the existence of positive fixed charges as discussed in Sect. 1.2.3. With nitrogen incorporation, the C-V curve shift to the positive direction and the stretch-out is decreased, besides, the temperature-dependent flat band shift is also decreased to a large extent, implying a significant improvement of the interface quality due to the

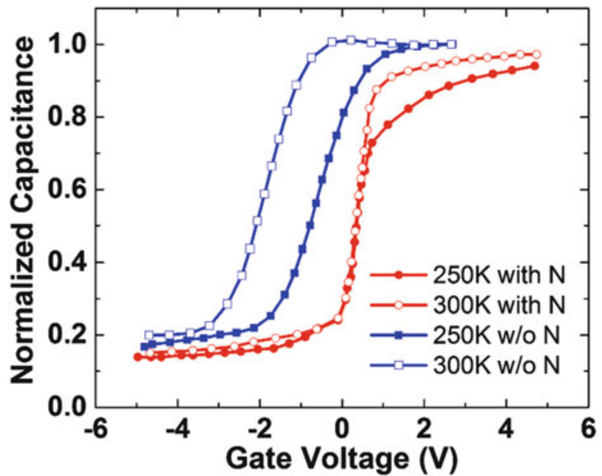


Fig. 1.10 High-frequency (1 MHz) C-V characteristics of HfO_2 films at different temperatures with and without nitrogen incorporation [40]

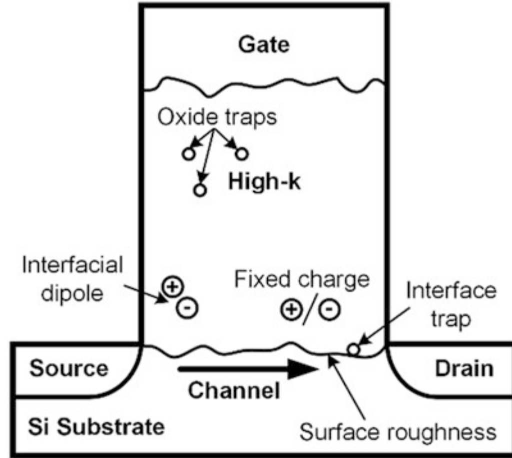


Fig. 1.11 Factors that cause mobility degradation and Vth shift [41]

converting of the Hf–Si bond to Hf–N. Apart from nitrogen implantation, thermal treatment and Al incorporation are two other methods to weaken the shift of Vfb by reducing the defects in the oxide bulk and/or at the high-k Si interface.

To sum up, the large amount of defects in the high-k oxide and the poor interface between high-k dielectric and Si are the main reasons that cause mobility degradation and V_{th} shift, as shown in Fig. 1.11. Therefore, the main challenge is to improve the bulk and interface quality of high-k dielectrics in order to optimize the performance of MOS devices.

1.3 Deposition

Being an essential factor that influence the densities of oxide defects and interface states, the quality of the high-k dielectric film must be paid sufficient attention. In order to guarantee acceptable performance of the resulting devices, grown dielectric films with good thickness uniformity, thermal stability and interfacial properties are required, therefore, correlating with the film quality and properties, deposition methods should be chosen carefully. Several deposition techniques have already been developed, the comparison of which are listed in Table 1.2 [41]. Chemical vapor deposition (CVD), Atomic layer deposition (ALD), and Physical vapor deposition (PVD) will be introduced in this section.

Basically, the chemical vapor deposition (CVD) is the transportation of the required materials from metallic-organic and some other precursors to the surface of the substrate. Through thermal, plasma or photo treatment, the precursors are decomposed with the materials needed deposit on the substrate. For example, trisdipyvaloylmethanato lanthanum ($La(C_{11}H_{19}O_2)^3$) can be used as the precursor

Table 1.2 Comparison of different deposition technologies

Method	ALD	MBE	CVD	Sputter	Evaporation	PLD
Uniformity	Good	Fair	Good	Good	Fair	Fair
Film density	Good	Good	Good	Good	Poor	Good
Step coverage	Good	Poor	Varies	Poor	Poor	Poor
Interface quality	Good	Good	Varies	Poor	Good	Varies
Multi-materials	Fair	Good	Poor	Good	Fair	Poor
Low-temp. deposition	Good	Good	Varies	Good	Good	Good
Deposition rate	Fair	Poor	Good	Good	Good	Good
Industrial applicability	Good	Fair	Good	Good	Good	Poor

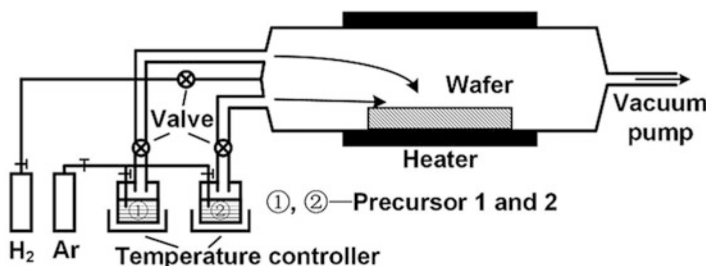


Fig. 1.12 Schematic diagram of a simplified ALD system

of growing La_2O_3, with a deposition temperature of 400–650°C in the ambient of O_2. However, uniformity problem is found in the La_2O_3 film and a silicate interfacial layer is formed at the La_2O_3 interface [42]. The major advantage of CVD is it is able to simply control the ratio of elements in tenary oxides, as reported by Y. Ohshita, et al. the percentages of Hf and Si in $Hf_{1-x}Si_xO_2$ can be controlled by varying the pressure, gas flows and temperature [43]. On the other hand, step coverage is one of the disadvantages of CVD, perfect coverage of steps cannot be obtained with aspect ratios larger than 10:1. Besides, relatively high temperature (400–850°C) is necessary during deposition, which is not good for materials with poor thermal stability such as rare earth oxides.

First known as atomic layer epitaxy (ALE) proposed in 1975 [44], it is developed to atomic layer deposit (ALD) with a wider range of materials and became the most widely used deposition method in actual application nowadays. The idea of ALD modifies the reaction of CVD by separating the two precursors into different containers. Figure 1.12 demonstrates a simple schematic diagram of an ALD system, high speed valves are used to strictly control the gas flow so that one single atomic layer can be deposited at a time. Therefore the thickness of the film can be determined by the number of transition cycles precisely, resulting in high quality film with excellent uniformity. The major disadvantages of ALD are (1) an interfacial low-k layer is still inevitable, (2) the poor stoichiometric control capability

Table 1.3 Different types of ALD

Type of ALD	Precursors	Target material	Temperature	Application
Catalytic ALD	(Metal)Cl_4, H_2O	Metal oxides	>32°C	High k dielectric layers, protective layers, anti-reflective layers
Al_2O_3 ALD	MCl_4, H_2O, Ti $(OiPr)_4$, $M(Et)_2$	Al_2O_3, Metal oxides	30–300°C	Dielectric layers, insulating layers, passivation layers
Metal ALD (Thermal chemistry)	$M(C_5H_5)_2$, $(CH_3C_5H_4)M(CH_3)_3$, $Cu(thd)_2$, $Pd(hfac)_2$, Ni $(acac)_2$, H_2	Metal fluorides, organometallics, catalytic metals	175–400°C	Conductive pathways, catalytic surface, MOS devices
ALD on particles	Various gases	BN, ZrO_2, CNT, polymer particles	25–100°C (polymer), 100–400°C (metal/alloy)	Insulative coating, optical and mechanical property modification, composite structures, conductive mediums
Plasma/radical-enhanced ALD	Organometallics, MH_2Cl_2, TBTDET, NH_3	Pure metals, metal nitrides	450–800°C	DRAM, MOSFET, capacitors

makes it difficult to deposit complex oxides with required doping concentration. Up till now, many types of ALD are available due to different mechanisms, some representative examples are listed in Table 1.3 [45–47].

Most of the precursors used in CVD and ALD tend to induce contamination to the dielectric films, besides, the reaction between precursors and Si substrate is inevitable, resulting in the formation of unstable low-k materials. Another technique called physical vapor deposition (PVD) including sputtering, evaporation, and molecular beam epitaxy (MBE) is proposed to deposit transition metal/rare earth metal oxides [48]. Argon or electron beam are used in PVD to sputter the required material from the metal or oxide target to the wafer. Since no other chemical is applied in PVD, much lower contamination from carbon, hydrogen and chlorine can be achieved when compared with CVD and ALD. When a metal target is used, oxygen ambient is necessary in order to deposit oxide dielectrics, resulting in the formation of interfacial SiO_x layer [49]. In addition, as long as the target is metal oxide, after being sputter away from the target, the elements of required material deposited on the wafer cannot be guaranteed to be the expected ratio, i.e. the film obtained might be Y_xO_y instead of Y_2O_3, leading to a high density of oxygen vacancies [50] that negatively impact the performance of the device as discussed in the previous sections. Summing up, PVD has the advantages of low contamination and compositional profile of the film, but owns the drawbacks of poor conformality for large aspect ratio steps and high traps and/or interface states density.

1.4 Current Alternative High-k Dielectrics

1.4.1 Hf-based Oxides

As discussed, SiO_2 have already reached its physical limit as gate dielectric, therefore, with relatively high k value, suitable band gap, and fewer reliability problems than other high-k materials, HfO_2 gate dielectrics with metal gate is now being applied in most of complementary metal-oxide-semiconductor field effect transistors (CMOSFETs). However, as the defects and interface states still exist in HfO_2 dielectric, plus the formation of crystalline structure of HfO_2 at low temperature can provide pathways for leakage current and lead to dielectric breakdown eventually, taking measures to make improvement in order to meet the requirement of further scaled MOSFETs is necessary.

The first strategy proposed is nitrogen incorporation. As discussed in Sect. 1.2.4, nitrogen is capable of passivating oxygen vacancies in high-k bulk and reducing interface states, this is consistent with experimental results that better characteristics including higher crystallizing temperature have been found in HfO_2 film, and thus the performance of MOS devices has been improved significantly [51, 52]. However, since the N 2p states lies above O 2p states, doping nitrogen also means decreasing band gap [53], besides, nitrogen-related traps might be induced [54], so the concentration of nitrogen should be considered and well controlled.

A second method is doping other oxides to optimize the film and interface quality, band gap offset, k value, as well as crystallization of HfO_2. SiO_2, Al_2O_3, Ta_2O_5, and La_2O_3 as dopants are discussed in this section according to the existing reports.

Since an unstable low-k SiO_x interfacial layer always appears in the HfO_2/Si gate stack and cause negative effects on interface quality and k value, doping SiO_2 into HfO_2 during the dielectric deposition is a feasible solution that inhibit the formation of the interfacial layer and give rise to the crystallization temperature of HfO_2 as well [55]. Also, doping nitrogen (HfSiON) can further improve the thermal stability as mentioned above. Unfortunately, reduction of k value is an unescapable consequence of doping SiO_2, therefore, this trade-off should be considered when selecting SiO_2 concentration.

Frequently, Al_2O_3 plays the role of improving the thermal stability of high-k oxides. In the case of HfO_2, the crystallization of HfO_2 and the out-diffusion of Si from the substrate to the dielectric can be effectively inhibited by Al_2O_3 incorporation [56]. As confirmed by Ref. [56], with Al_2O_3 concentration of 33%, the $HfAlO_x$ remains amorphous after post-deposition annealing at 900°C. Besides, according to M. S. Joo, et al. HfAlO also has good compatibility with metal nitride gate after PDA treatment at high temperature, as shown in Fig. 1.13 [57]. Another effect of Al_2O_3 is to passivate oxygen vacancies, T. J. Park reported that oxygen vacancies can be decreased by around 4% after Al incorporation [58]. Moreover, the bandgap structures of HfO_2 and HfAlO are compared in Fig. 1.14 according to Ref. [58], with Al incorporation, shallow defect states can be removed and thus the

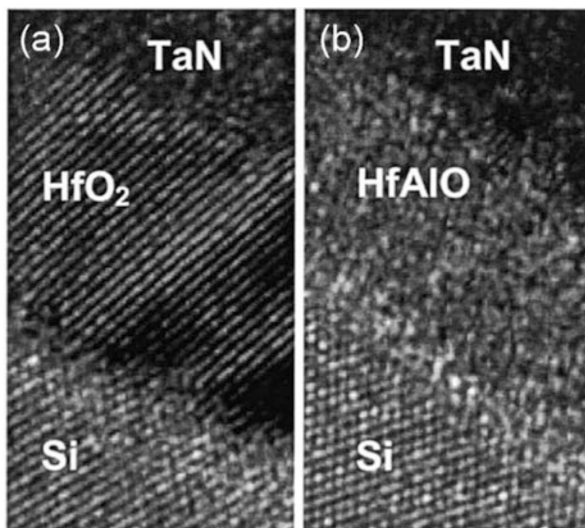


Fig. 1.13 TEM images of (**a**) HfO_2 and (**b**) HfAlO on Si after PDA treatment at 700°C [57]

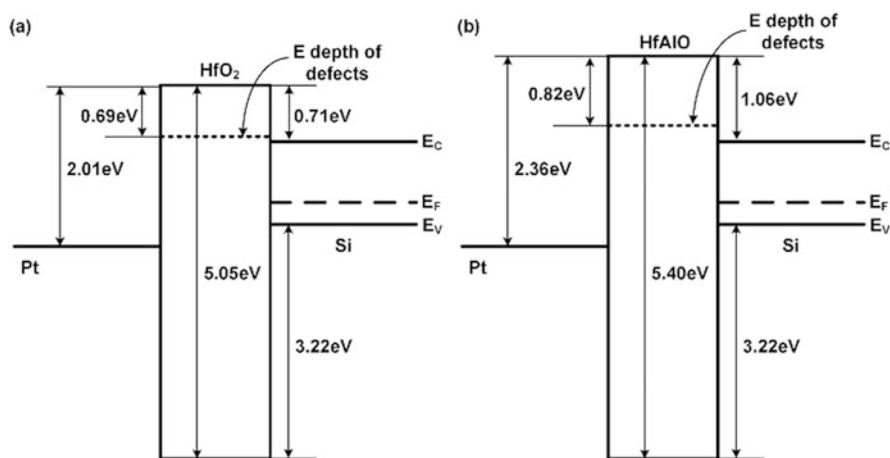


Fig. 1.14 Bandgap structures of gate stacks with (**a**) HfO_2 and (**b**) HfAlO as dielectric [58]

bandgap energy is increased, and the leakage current can be decreased accordingly. However, similar as SiO_2, the k value of Al_2O_3 (~9) is relatively low. In addition, Bae et al. pointed out negative fixed charges that degrades carrier mobility are introduced due to the accumulation of Al at the HfAlO/Si interface [59].

In order to improve the thermal stability of HfO_2 but meanwhile keep its relatively high k value, Ta_2O_5 (k ~26) incorporation is proposed. It has been proved by X. F. Yu, et al. that doping Ta_2O_5 effectively enhances the crystallization temperature of HfO_2. Figure 1.15 compares the cross sectional images of HfO_2

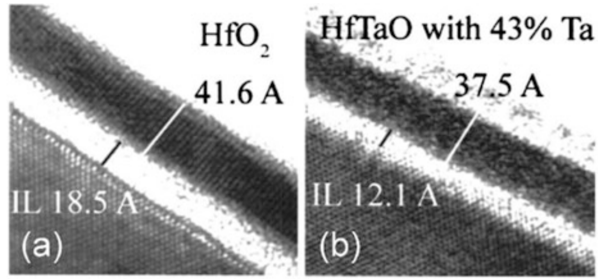


Fig. 1.15 TEM images of (**a**) HfO_2 and (**b**) HfTaO films after high temperature treatments [60]

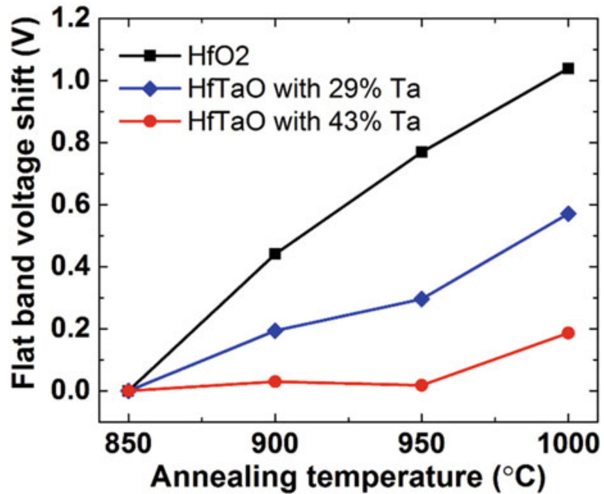


Fig. 1.16 Comparison of flat band voltage shift of pMOS capacitors with HfO_2 and HfTaO as gate dielectric after annealing at different temperatures [60]

and HfTaO after a PDA treatment at 700°C and an activation annealing at 950°C, obviously the crystal lines of HfO_2 are formed whereas HfTaO still remains amorphous [60]. Besides, in Fig. 1.15, the low-k interfacial layer formed on the surface of the HfO_2 sample is thicker than that of the HfTaO sample, implying that Ta_2O_5 incorporation is able to inhibit the intermixing of the dielectric and the Si substrate. Furthermore, in Ref. [60], the flat band voltage shift after high temperature annealing is also studied as shown in Fig. 1.16. The boron penetration-induced flat band voltage shift in HfO_2 film is dramatically suppressed by Ta_2O_5 incorporation, indicating less defects and interface states.

Rare earth elements like La is also a promising candidate as dopant to improve the properties of Hf-based high-k dielectric. Same as Ta_2O_5, doping La_2O_3 into HfO_2 can also increase crystallization temperature meanwhile keep the relatively high k value due to the high permittivity of La_2O_3 (above 20). A decrease of fixed charge density in the oxide film can be found after introducing La_2O_3 into HfO_2 by Y. Yamanoto et al. because the dependence of flat band voltage (V_{fb}) on capacitance equivalent thickness (CET) is very week according to Fig. 1.17 [61]. As

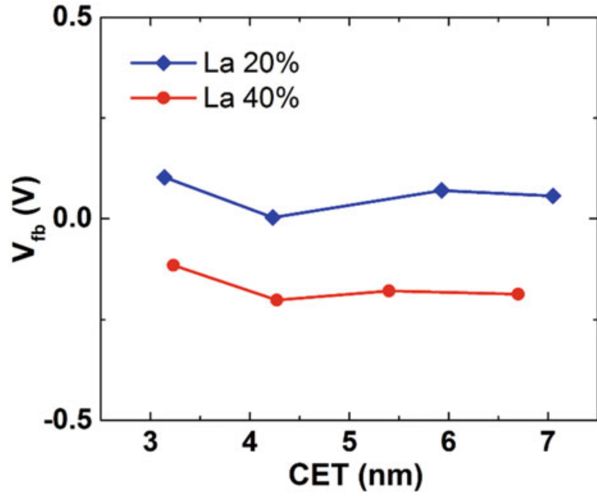


Fig. 1.17 Vfb vs. CET of MOS capacitors with $HfLaO_x$ as gate dielectric [61]

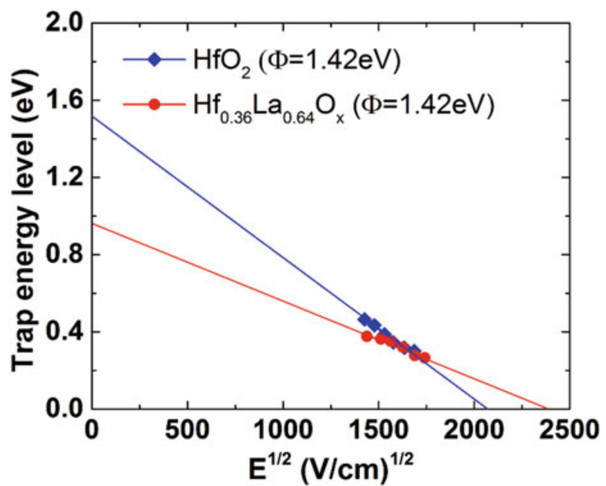


Fig. 1.18 Trap energy level vs. applied electric field of HfO_2 and HfLaO films [62]

confirmed by C. H. An, et al. in Fig. 1.18, the intrinsic trap energies in HfLaOx films are 1.42 eV, 1.34 eV, 1.03 eV, and 0.98 eV with La/(Hf + La) ratios of 0%, 42%, 57%, 64%, respectively, indicating a removing of shallow traps after doping La_2O_3 [62]. In addition, the metal work function of MOSFETs with TaN/$HfLaO_x$ or HfN/$HfLaO_x$ gate stacks can be tuned by varying the La concentration [63], which is preferred in achieving relatively low Vth as mentioned in Sect. 1.2.3. However, the major drawback of La_2O_3 is its hygroscopic nature, if the La_2O_3 possesses extremely high ratio in HfO_2, the film will absorb moisture easily and negatively influence the roughness of the dielectric and thus impact the carrier mobility.

1.4.2 *Rare-Earth Oxides*

Rare-earth oxide films are considered as promising candidates in varieties of applications such as luminescent materials, catalysts, buffer and protecting layer, constituents in oxide superconductors, and solid oxide fuel cell [64]. As dielectric material, rare-earth oxides own advantages of relatively high k value (La_2O_3 ~ 24–27, Y_2O_3 ~ 12–18, Lu_2O_3 ~ 12–19, etc.) excellent chemical stability on Si, and large band offset with Si. Besides, one other advantage that cannot be found in the commonly used HfO_2 is the higher electron effective mass and barriers in some rare-earth oxides can suppress tunneling current [65]. Unfortunately, the main concern of rare-earth oxides is the hygroscopicity, leading to poor stability of the film. In addition, formation of silicon-metal oxide mixtures or crystallized silicate phases easily happens due to the diffusion of Si from the substrate, which is a sever deterioration of the interface [66, 67].

Up till now, the most mature study on rare-earth oxides as gate dielectric is about La_2O_3 which will be discussed in this section as a representative of rare-earth oxides. As mentioned, the hygroscopic nature of the rare-earth oxides is the main concern in real application because during CMOS fabrication, wet processes and exposing to air are inevitable, therefore, the effects of moisture absorption is an important factor that influents the electrical properties of MOS devices. A moisture absorption experiment of La_2O_3 was carried out and it was found that after being exposed in the air for 12 h, La_2O_3 was totally replaced by $La(OH)_3$ [68]. Roughness of La_2O_3 film before and after being exposed in air is compared in Fig. 1.19, the surface roughness increases from 0.5 nm to 2.4 nm, one possible reason for which is that the density of hexagonal $La(OH)_3$ is smaller than that of hexagonal La_2O_3, resulting in volume expansion, therefore, nonuniform volume expansion happens due to the nonuniform moisture absorbing, leading to an increased roughness [68].

As for the influence of moisture absorption on the electrical properties of MOS devices, it is controversial on the direction of V_{fb} shift. S. Guha et al. hold the opinion that the replacement of O^{2-} by OH^- means an inducing of positive charges, resulting in a negative shift of V_{fb} [69]. However, in Ref. [68], V_{fb} of MOS capacitor with La_2O_3 as gate dielectric exhibits shift to the positive direction as shown in Fig. 1.20, which is explained by the formation of OH^- that contains negative charges during absorbing moisture. Moreover, Fig. 1.20 also illustrate the

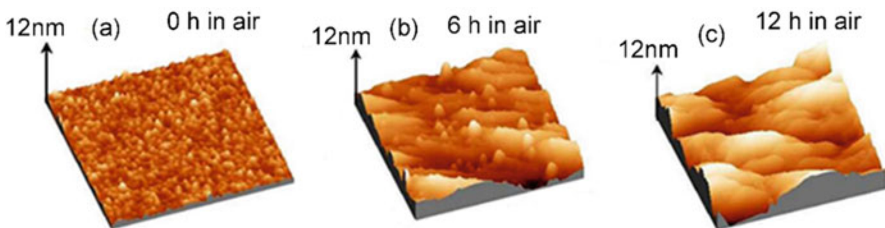


Fig. 1.19 Roughness of La_2O_3 film before and after being exposed in air [68]

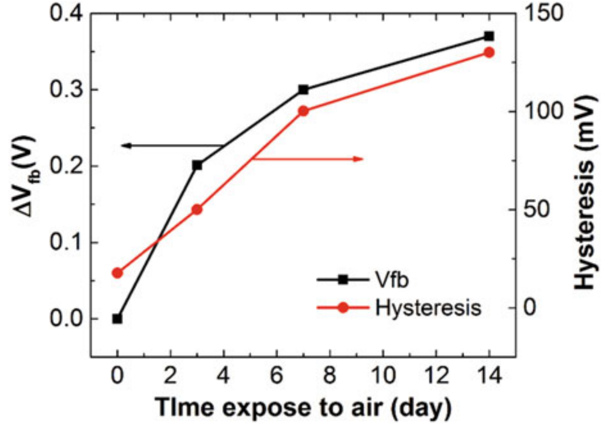
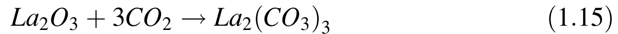


Fig. 1.20 V_{fb} shift and hysteresis of La_2O_3 film before and after exposed to air [65]

effect of moisture absorption on the hysteresis of C-V characteristic. Obvious increment of hysteresis can be found after being exposed in air, indicating the introduction of traps. Besides, leakage current of La_2O_3 is also found to be increased by several orders after moisture absorbing [68].

Apart from the hygroscoticity of La_2O_3, the absorption of carbon dioxide during post-deposition ambient exposure has also been reported [70], with reaction as followed:



$$La_2O_3 + 3CO_2 \rightarrow La_2(CO_3)_3 \tag{1.15}$$

However, the effect of CO_2 absorption is found much weaker than that of moisture absorption, and thus negligible.

Another concern of La_2O_3 as dielectric that should be paid attention to is its k value degradation due to the hygroscopicity of La_2O_3. Theoretically, the k value of La_2O_3 should be 20–30, but many literatures has reported much lower k value than the theoretical value. As mentioned, $La(OH)_3$ is formed after moisture absorption, the k value of $La(OH)_3$ can be calculated by the Clausius-Mossotti relationship:

$$k = \left(3V_m + 8\pi\alpha^T\right)/\left(3V_m - 4\pi\alpha^T\right) \tag{1.16}$$

in which Vm is the molar volume and αT is the total polarizability. According to the Shannon's additivity rule, αT equals to 12.81Å3 [71], and 71 Å3 can be plugged in as the value of V_m [72]. Therefore, the k value of $La(OH)_3$ is estimated to be ~10, leading to an obvious degradation in the k value of La_2O_3.

In order to explain the reason that causes La_2O_3 absorbs moisture, the concept of Lattice Energy (LE) should be introduced here. LE is the energy required to break the ionic bonds in an ionic lattice of a solid ionic compound and separate one molecule into gaseous ions completely. It has been found that the LE of ionic oxides is inversely proportional to the metal ion radius [73]. Meanwhile, smaller LE tends

to promote the reaction of moisture absorption [74]. Therefore, since La owns the largest ion radius among of the rare-earth metals, the LE of La_2O_3 is the smallest, and thus make La_2O_3 has very weak hygroscopic tolerance, indicating that enhancing the LE of La_2O_3 is the key point of suppressing its moisture absorption.

Doping other elements or oxides is the first idea, the dopant should own larger LE. Being in the same group with La, Y has many properties similar to La except that Y_2O_3 exhibits much lower crystallization temperature than La_2O_3 and thus able to achieve much larger LE. It is expected that Y_2O_3 might be a promising dopant and studies have been made on the properties of LaYO film. It has been reported that $La_{2-x}Y_xO_3$ films with 40–70% Y concentration has much larger lattice energy than La_2O_3 and high k value can be obtained with nearly no degradation after exposure, besides, MOS capacitor with $La_{2-x}Y_xO_3$ as gate dielectric shows better C-V behavior and smaller leakage current [68], indicating Y_2O_3 is indeed a good choice for dopant to enhance the hygroscopic tolerance of La_2O_3. However, the low crystallization temperature is usually not preferred. Apart from Y, Hf [75], Ta [76], and Nb [77] as dopant to La_2O_3 have also been tried with improved properties obtained.

Another idea is ultraviolet (UV) ozone treatment proposed by Ref. [68]. An experiment has been carried out comparing the influence of different treatment after La_2O_3 depositing on surface roughness with result shown in Fig. 1.21. The as-deposited sample and the 0.1% O_2 + N_2 sample show better moisture resistance than the N_2 annealing sample is possibly due to the decrease of oxygen vacancies in O_2 related ambient. Implying that the moisture absorbing tendency of La_2O_3 might has some dependency on the density of oxygen vacancies in the film. It has been reported that oxygen vacancies in oxide films can be passivated by UV ozone treatment at room temperature [78]. It is well known that charge transfer between La and O atoms tends to happen with the existence of oxygen vacancies and make

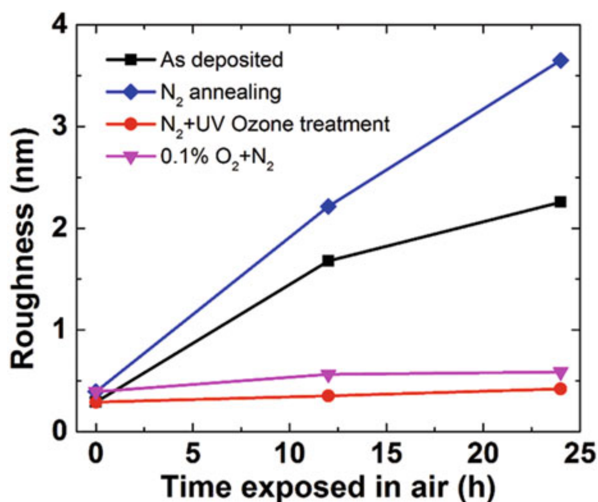


Fig. 1.21 RMS surface roughness of La_2O_3 vs. exposure time with different post deposition treatment [78]

the La–O bond more ionic, resulting in a decrease LE, so passivating oxygen vacancies can suppress the moisture absorbing at the same time. Therefore the N_2 + UV ozone treatment sample in Fig. 1.21 exhibit the best moisture resistance. Besides the formation of low-k interfacial layer can also be prevented because there is no need to provide high temperature.

1.4.3 Perovskite Structured Oxides

In recent years, perovskite structured oxide has received much attention for further device scaling due to their extremely high k values, especially $SrTiO_3$ (STO) [79–81]. In Ref. [79], relatively good results are obtained with the experimental STO k value of 45.2 and EOT of 5.4 Å. However, the main concern of STO is about leakage current due to its small band gap (3.2 eV) and conduction band offset with Si (~0 eV) [82]. The first idea to solve this problem is adding an interfacial layer with wider band gap, but usually a SiO_x layer is formed at the STO/Si interface after the deposition. This oxide layer with much larger band gap can be considered as a buffer layer to decrease the leakage current, which has been confirmed by R. Droopad, et al [83]. Based on the drain current curves in Fig. 1.22, the mobility of nMOS- and pMOSFET are 220 $cm^2\ V^{-1}\ s^{-1}$ and 62 $cm^2\ V^{-1}\ s^{-1}$ respectively, which are impressive. And the leakage current of these devices are also acceptable. But since SiO_x is not as stable as SiO_2 and might contains dangling bonds, the interface quality cannot be guaranteed and thus impact the carrier mobility.

In order to further decrease the leakage current of MOS device with STO as gate dielectric, the idea of doping Al into STO has been proposed to enlarge the band gap and meanwhile passivate oxygen vacancies. It has been proved that after doping Al

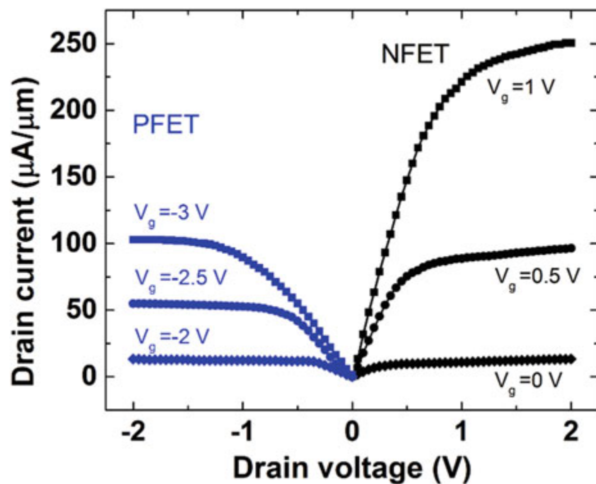


Fig. 1.22 Drain current curves of nMOS- and pMOSFET with STO as gate dielectric [83]

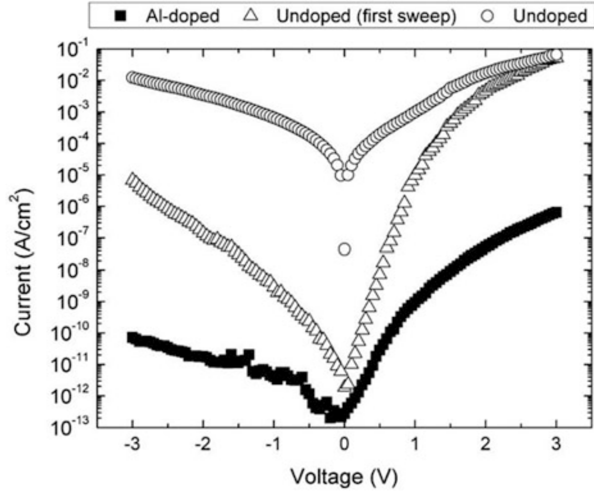


Fig. 1.23 Leakage current of 90Å-thick undoped and 20% Al-doped STO dielectric on Si [84]

with a ratio of 20%, the band gap of STO increases ~0.3 eV, and the leakage current decreases significantly as shown in Fig. 1.23 [84]. In addition, after the first voltage sweep, the leakage current of the undoped sample increases from 4×10^{-6} A/cm^2 to 8×10^{-4} A/cm^2 at 1V, whereas no increment is found in the Al doped sample (7×10^{-10} A/cm^2), indicating the oxygen vacancies are effectively passivated by Al. However, the poor thermal stability of STO is a fatal drawback that will impact the reliability of MOS device, so more studies should be made to achieve further improvement.

$LaAlO_3$ is another promising candidate with perovskite structure due to its large band gap (5.6 eV), relatively high k value (~24), large band offset and thermal stability with Si. High crystallization temperature of $LaAlO_3$ has already been confirmed (above 850°C) [85], besides, the formation of interfacial $LaAlSiO_x$ layer can be effectively suppressed if the $LaAlO_3$ film is deposited in N_2 ambient (LaAlON) [86]. Being consistent with the discussion of nitrogen incorporation in Sect. 1.4.1, LaAlON performs better than $LaAlO_3$ as gate dielectric of MOS device as proved by W. F. Xiang et al. in Fig. 1.24 [87]. Obvious improvement including higher k value, lower Vfb and leakage current is achieved by the LaAlON sample, which should be attributed to the reducing of interface states density by nitrogen and the more stable SiON interfacial layer than SiO_x formed at the high-k/Si interface.

The electrical performance and reliability of MOSFET with $LaAlO_3$ as gate dielectric has been studied by I. Y. Chang, et al [88]. Mobility of nearly 700 cm^2 V^{-1} s^{-1} and V_{th} of 0.35 V can be considered as impressive results. The temperature reliability of the device is illustrated by Fig. 1.25. It is well known that V_{th} is affected by the charges in the dielectric oxide and the states at/near the oxide/Si substrate as expressed in Eq. (1.16).

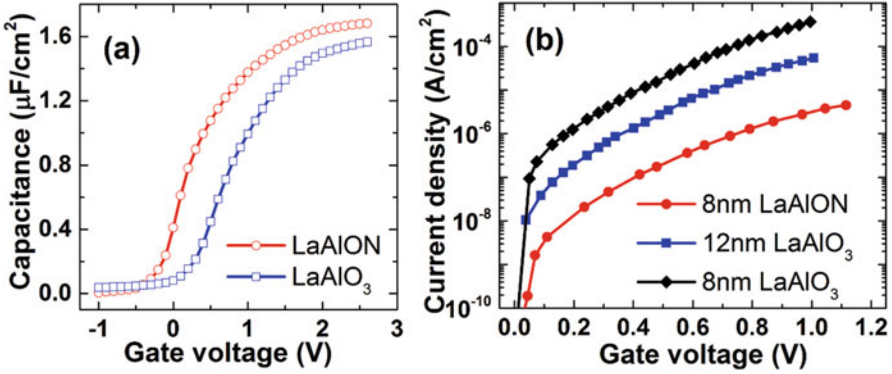


Fig. 1.24 Comparison of (**a**) C-V and (**b**) leakage current characteristics of MOS capacitors with $LaAlO_3$ and LaAlON as gate dielectric [87]

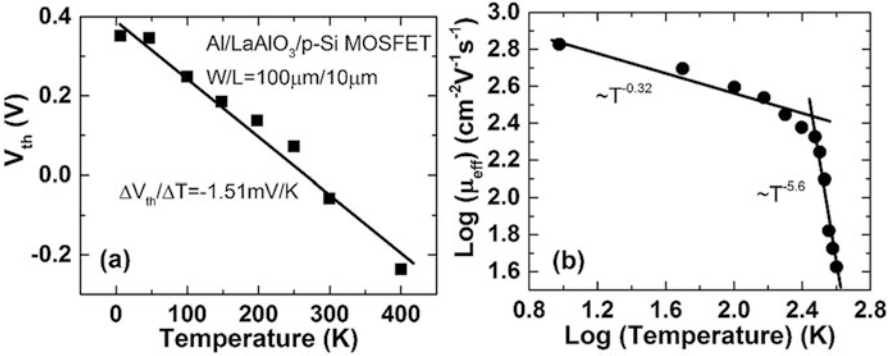


Fig. 1.25 Variation of (**a**) V_{th} and (**b**) mobility with the increase of temperature [89]

$$V_{th} = \Phi_{ms} + 2\psi_B + \frac{\sqrt{4\varepsilon_s q \psi_B N_A}}{C_{ox}} - \frac{Q_f + Q_{ot} + Q_m + Q_{it}}{C_{ox}} \tag{1.16}$$

where Φ_{ms} is the work function difference between the gate and the Si substrate, Q_f, Q_{ot}, and Q_m are the densities of fixed charges, oxide traps, and mobile ionic charges in the oxide layer, respectively, while Qit is the density of interface trapped charges. Since Φ_{ms}, Q_f, Q_m, and Q_{it} are independent with temperature, the variation of Vth¬ with temperature can be obtained by differentiating Eq. (1.17):

$$\frac{dV_{th}}{dT} = -\frac{1}{C_{ox}}\frac{dQ_{ot}}{dT} + \frac{d\psi_B}{dT}\left(2 + \frac{1}{C_{ox}}\sqrt{\frac{\varepsilon_s q N_A}{\psi_B}}\right) \tag{1.17}$$

Therefore, in the case of this section, the oxide density Q_{ot} is the determining factor of ΔV_{th}. In Fig. 1.25a, the temperature-dependent change rate of V_{th} ($|\Delta V_{th}/\Delta T|$) is 1.51 mV/K, larger than that of MOSFET with SiO_2 as gate oxide (1 mV/K), indicating larger amount of oxide charges in $LaAlO_3$. On the other hand, the electron mobility is proportional to $T_{-5.6}$ at high temperature, since the comparative value for device with SiO_2 is $T_{-1.75}$, conclusion of $LaAlO_3$ induces severer phonon scattering than SiO_2 can be drawn [89].

To sum up, perovskite structured oxides have the drawbacks of small bandgap and relatively poor thermal stability, nevertheless, they are attracting broad attention recently due to their extraordinary electronic and magnetic properties such as extremely high k value, high-T_c superconductivity, colossal magnetoresistance, and multiferroic behavior. Apart from the STO and $LaAlO_3$ introduced in this section, materials like $BaTiO_3$, $BaTi_{0.5}(Fe_{0.33}Mo_{0.17})O_3$, Sr_2MgMoO_6, etc. are being studied in varieties of areas such as memory, solar cell, and solid oxide fuel cell. Therefore, more studies needs to be done to make further improvement in the applications with perovskite oxides.

1.5 Applications

1.5.1 DRAM Cell Capacitors

It is well known that it is capacitor that DRAM uses to determine a bit value of 0 or 1 by whether the capacitor is charged or not. Since the capacitance of a parallel capacitor with an oxide layer as insulator is calculated by:

$$C = \frac{k\varepsilon_0 A}{T_{ox}} \tag{1.18}$$

with the scaling down of the device, the capacitance (C) will inevitably decreases with the decreasing of electrode area (A). However, a DRAM capacitor must guarantee a minimum capacitance of ~ 25 f. per cell to provide enough sensing margin and data retention time, so measures should be taken to increase C. In order to achieve an EOT of less than 1 nm, high-k materials have to be introduced as the insulating layer. Metal-insulator-metal (MIS) structured DRAM with Al_2O_3 insulator deposited by ALD is the first case with enhanced capacitance and relatively low leakage current [90, 91]. After that, Ta_2O_5 has become the most widely used high-k material and has been put in production due to its high k value, high breakdown fields, good compatibility with Si and strong ability of charge storing [92].

Besides, perovskites structured materials such as STO and $BaSrTiO_3$ have also been studied for the purpose of significantly increasing k value, however, as discussed in Sect. 1.4.3, the inevitable interfacial SiO_x layer is the fatal factor

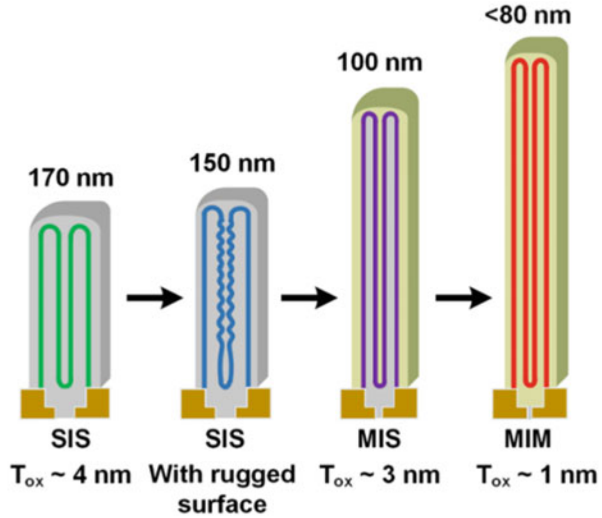


Fig. 1.26 DRAM capacitor evolution [95]

that impact the capacitance. Therefore, the replacement of MIS structure with metal-insulator-metal (MIM) structure is proposed to prevent the formation of the low-k interfacial layer. A record low leakage current density of 10^{-6} A/cm^2 with EOT of 0.4 nm have been obtained from the MIM DRAM with ALD deposited STO as insulator and Ru as bottom electrode, which enables the scalability of DRAM to the 3X nm mode [93]. Consequently, Al_2O_3 doped ZrO_2 and sandwich structured (ZrO_2/Al_2O_3/ZrO_2) stack with TiN as electrode MIM DRAM are reported to be able to achieve excellent reliability [94]. Figure 1.26 is a summary of the development of DRAM, more new materials and structures are still being studied [95].

1.5.2 Nonvolatile Memories

Nonvolatile memory typically plays the role of secondary storage or long-term persistence storage in modern electronic systems and evolves from read only memory (ROM), electrically programmable ROM (EPROM), electrically erasable programmable ROM (EEPROM) to flash memory. Flash memory has kept its dominating position in recent years due to its small cell size and the ability of operating program/erase more than 10^5 times with high reliability.

The first successful type is floating gate flash memory with control gate/inter-poly dielectric (IPD)/floating gate (FG)/tunneling layer (TL)/Si substrate stack. With the advantages of high program/erase speeds, low operating voltage and low power consumption, floating gate flash memory has continuously scaling

down to increase the data-storage density, however, a relatively thick tunneling oxide (6–7 nm) and IPD layer (9–10 nm) are needed to guarantee the reliability due to the leakage caused by the possibility that charges stored in the floating gate tunneling through the IPD and TL with the assistant of defects. Oxide/nitride/oxide (ONO) stack or high-k materials as TL and/or IPD have been studied for a period to solve the leakage issue [96]. Unfortunately, temperature instability is found in ONO stack and the ionic defects (e.g. oxygen vacancy) in high-k materials tend to give rise to varieties of reliability issues. Therefore, novel structures and/or materials have to be investigated for further scaling.

Ferro-electric random-access memory (FeRAM) defines ‘0’ and ‘1’ by the remnant polarization of ferroelectric dielectrics through the control of an external field [97]. $Pb(Zr_xTi_{1-x})O_3$ (PZT) and $SbBi_2Ta_2O_9$ (SBT) are the most widely used ferroelectrics for FeRAM. High random access operating speed and low power consumption are the major advantages for FeRAM, but the rewriting operation after each read process is a severe problem that cause extra consumption [97].

Another type of flash memory that makes use of high-k material is discrete charge-trapping memory (CTM), in which ‘0’ or ‘1’ is defined by removing or adding charges from the charge-storage layer. The typical structure of CTM is based on the metal/oxide/nitride/oxide/Si (MONOS) gate stack, corresponding to gate/blocking layer (BL)/charge trapping layer (CTL)/tunneling layer (TL)/substrate stack, as shown in Fig. 1.27. The conventional SiN-based CTM has a trade-off between high program/erase speeds and good data retention, so band engineering is needed. The blocking layer contact directly with Si substrate plays the role of preventing the diffusion of carriers in the charge trapping layer back to the Si substrate, so the choice of high-k material has criteria of large band gap, few defects and trap in the bulk and at the interface, and good stability and compatibility with CMOS technology. With large band gap (8.8 eV) and excellent thermal stability, Al_2O_3 becomes the best choice for the blocking layer [14]. In order to further

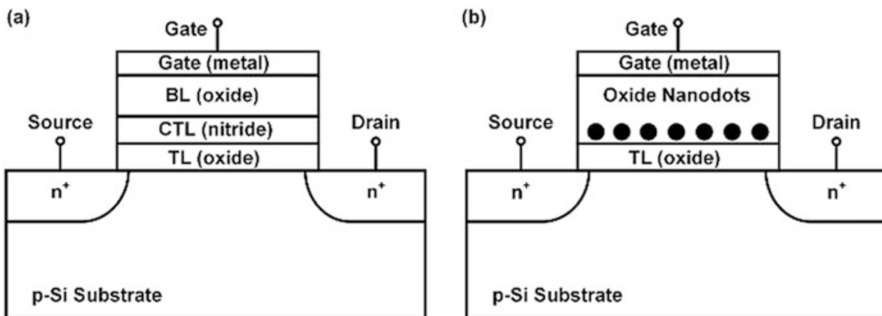


Fig. 1.27 Schematic diagrams of (**a**) nitride-based and (**b**) nanocrystal-based charge trapping memory

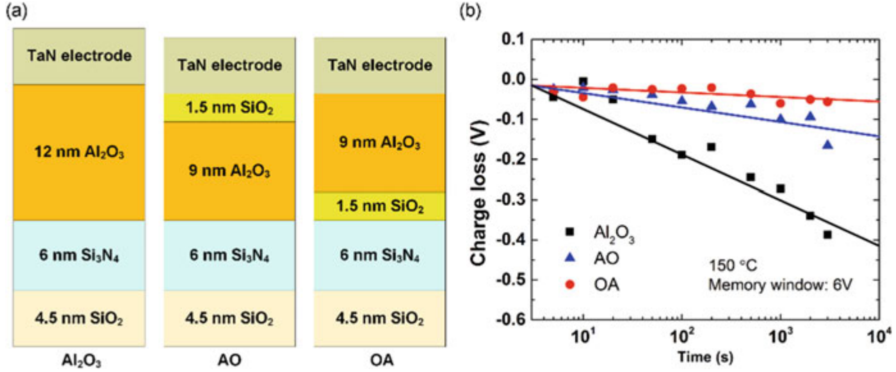


Fig. 1.28 (**a**) Gate stacks of CTMs with Al_2O_3 and Al_2O_3/SiO_2 as blocking layer. (**b**) Charge loss vs. time duration for the devices in (**a**) [101]

increase the k value, compound dielectrics such as Gd^- [98], La^- [99], and Y^- [100] doped Al_2O_3 have been studied with improvements in program speed, saturation window and breakdown characteristic have been made. An Al_2O_3/SiO_2 double layer is another idea for the blocking layer to improve the device properties due to the lower density of defects and larger barrier height of SiO_2, which is proved by H. Park et al in Fig. 1.28b, the SiO_2 layer effectively weaken the loss of stored data [101].

In terms of the charge trapping layer, shallow-level trap density should be as low as possible to maintain enough conduction band offset with the tunneling layer. Various high-k dielectrics (e.g. La_2O_3, Y_2O_3, ZrO_2, Ta_2O_5, etc.) have been investigated to replace conventional Si_3N_4 due to their deep-level traps and stronger scaling ability [102–105]. Recently, compound high-k materials as charge trapping layer are widely being studied such as LaTiON [106], Nb doped La_2O_3 [107], fluorinated STO [108], and Zr doped BTO [109].

Nanocrystals (NC) including Si, Ge, Pt, Au, etc. embedded in a dielectric matrix is another promising medium for trapping charges in CTMs as shown in Fig. 1.28b. Metal NCs own higher deep-level trap density and wider range of work function than their semiconductor NCs counterparts, but their poor thermal stability and contamination are fatal disadvantages [110, 111]. Therefore, high-k materials start to be applied in NC based memories due to their high deep-trap density and compatibility with MOS process, devices with Ga_2O_3 [112], Al_2O_3 [113], $TiAl_2O_5$ [114], etc. as NC charge trapping layer exhibit excellent memory properties.

Furthermore a bandgap-engineered (BE) barrier with an oxide/nitride/oxide stack as TL consists of low-k and high-k has been investigated in order to maintain good retention by enhancing the tunneling of carriers during the program/erase operating and thus inhibit the charge loss in retention mode [115]. BE barriers using Si_3N_4/SiO_2 [116] and HfO_2/SiO_2 [117] etc. have already been tried.

1.5.3 Novel Channel Materials

1.5.3.1 Ge

According to Eq. (1.4) in Sect. 1.2.1, the channel carrier mobility μ is another important factor that affects the drive current of MOS devices. Besides, as mentioned in Sect. 1.2.4, mobility degradation is inevitable when high-k dielectric is applied on Si. The measure of replacing conventional Si substrate has been taken so that the mobility issue can be solved, and thus further enhance the drive capability of MOS devices. This replacement begins with strained Si and SiGe, but limitations in mobility and V_{th} still exists for the high performance and low power consumption requirements in the future, and that is when Ge becomes attractive because of its superior intrinsic electron and hole mobility. The comparison between Si and Ge listed in Table 1.4 illustrates the advantage of Ge in mobility over Si.

High-k materials including HfO_2 [118], HfTiON [119], and LaTiON [120], etc. have been tried with the highest k value of over 30 obtained, however, the main challenges of Ge substrate with high-k dielectrics are poor high-k/Ge interface, Fermi-level pinning near valance band, and the easily formed unstable and water-soluble native oxide, so the interface quality still need to be improved. Post deposition treatment is always a good choice to decrease the defects and/or traps in the dielectric bulk and at the interface, which has been confirmed by Ref. [119] and [121] using wet N_2 annealing and fluorine incorporation respectively. Besides, it has been found that pulsed laser annealing is also capable of positively influence the quality of the high-k film and the interface (Fig. 1.29) [122]. With no need of high temperature, the risk of crystallization is also eliminated.

An ultrathin passivation interfacial layer is another method that is being widely investigated. It is important to choose materials with large bandgap and good thermal stability as passivation layer. Up till now, varieties of high-k oxides/oxynitrides have been applied with improvement obtained, including Y_2O_3 [123], TaON [124], LaTaON [125], and $GeSnO_x$ [118] etc.

1.5.3.2 III-V Compound Semiconductors

According to Table 1.4, Ge has much higher carrier mobility than Si, but the lower breakdown field is not suitable for high-voltage applications. Meanwhile, although the smaller band gap is preferable for low-voltage operation devices, large leakage

Table 1.4 Comparison of properties between Si and Ge

Property	Mobility ($cm^2V^{-1}s^{-1}$) Electron	Hole	Breakdown field (V/cm)	Band gap (eV)	k value	Saturation velocity (10^7 cm/s)	Melting point (°C)
Si	1350	500	3×10^5	1.12	11.9	1.0	1415
Ge	3900	1900	10^5	0.66	16.0	0.5	937

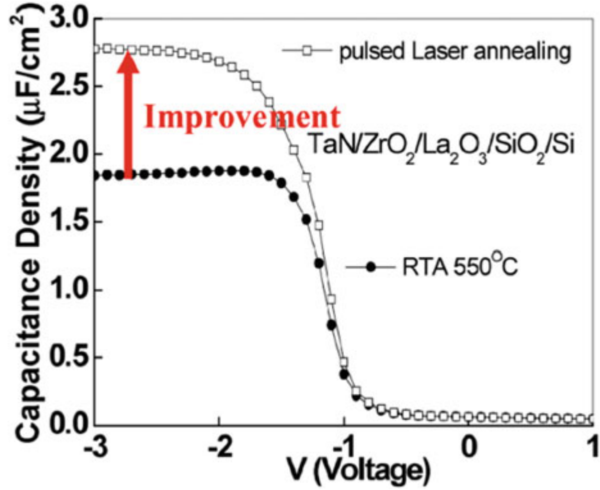


Fig. 1.29 C-V characteristics of Ge MOS capacitors with pulsed laser annealing and conventional thermal annealing [122]

Table 1.5 Basic parameters of major III-V compound semiconductors

Materials	Electron mobility ($cm^2V^{-1}s^{-1}$)	Hole mobility ($cm^2V^{-1}s^{-1}$)	Band gap (eV)	Lattice constant (Å)
Si	1400	450	1.12	5.43
GaAs	8500	400	1.42	5.65
InAs	4×10^4	500	0.37	6.03
$Ga_{0.53}In_{0.47}As$	1.2×10^4	850	0.85	5.87
InSb	7.7×10^4	300–400	0.17	6.48
InP	5400	200	0.35	5.87

current is also caused which will increase power consumption. Therefore, III-V compound semiconductors with even higher mobility have been proposed and paid much attention recently (Table 1.5 [41]). Among of the III-V compounds, GaAs with electron mobility around five times than Si and larger band gap and breakdown field has received most attention and is the most representative member up till now.

When high-k oxides deposited on GaAs (e.g. HfO_2), the Ga– and As– dangling bonds cannot fully saturated, mid-gap states will be induced by the partially saturated bonds and cause Fermi-level pinning, meanwhile, the dangling bonds at the interface might form unstable Ga–O, As–O, As–As, Ga–Hf, and As–Hf interfacial bonds during fabrication process. Therefore, similar with Ge, GaAs also suffers from the easily formed unstable native oxide and high density of interface states (D_{it}), mobility degradation and instability of devices, which makes surface passivation of the GaAs surface the most essential factor of optimizing the performance of MOS devices.

It has been found by F. S. Aguirre-Tostado et al. that sulfur passivation by treating GaAs surface with $(NH_4)_2S$ is capable of reducing interfacial space charges

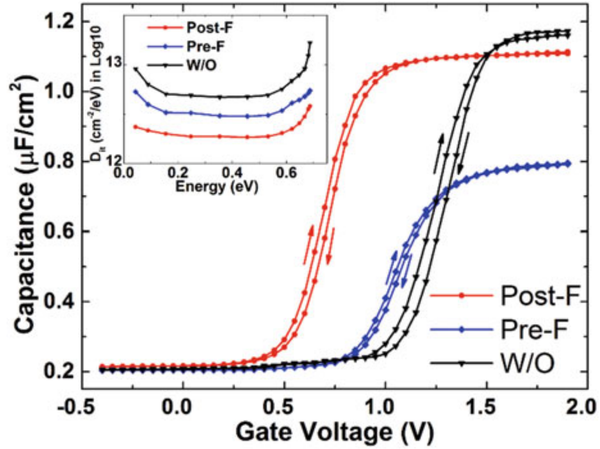
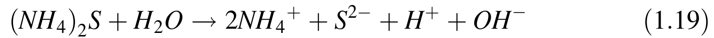
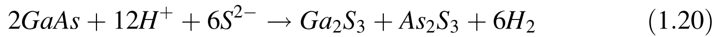


Fig. 1.30 C-V curves of GaAs capacitors with and without fluorine treatment [128]

[126]. With reactions [1.19] and [1.20] happens, Ga_2S_3 and As_2S_3 are formed at the GaAs surface, thus decreases the Ga- and As-related vacancies [127].



$$(NH_4)_2S + H_2O \rightarrow 2NH_4{}^+ + S^{2-} + H^+ + OH^- \quad (1.19)$$



$$2GaAs + 12H^+ + 6S^{2-} \rightarrow Ga_2S_3 + As_2S_3 + 6H_2 \quad (1.20)$$

In addition, post-deposition fluorine treatment can also effectively passivate oxygen vacancies in high-k oxides and suppress the formation of GaAs native oxide [128]. Figure 1.30 compares the C-V characteristics of GaAs MOS capacitors with post- and pre-deposition fluorine treatment, the Vfb and Dit of the post treatment sample is decreased significantly, overweighs a slightly loss in k value probably due to the high bonding energy between metal atom and incorporated F atoms [128].

Similarly, passivation layer is another effective solution of the poor interface quality. With the same criteria of passivation layer on Ge, Si, Ge, AlON, TaON, nitride $Ga_2O_3(Gd_2O_3)$, and LaTaON have been studied with improved performance obtained [129, 130].

1.5.3.3 Metal Oxide Thin Film Transistor (TFT)

Tremendous efforts have been made in the past few decades on thin film transistors (TFTs) because of its application in flat-panel display. Since the invention of TFT in 1962 using polycrystalline CdS as semiconductor material, the active layer of TFT has developed from a-Si: H, poly Si, SnO_2, and ZnO to meet the requirement of the increasing display panel size, consequently, in order to further increase the mobility, TFT with amorphous InGaZnO (a-IGZO) deposited at room temperature as channel material has been reported by Nomura et al. in 2004 with a mobility of

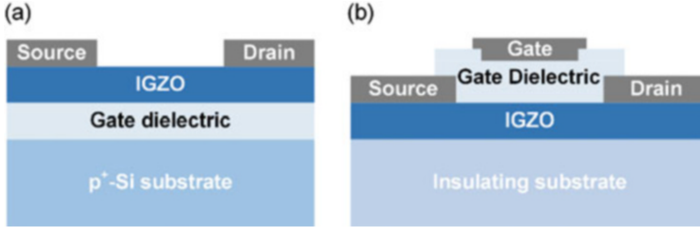


Fig. 1.31 Schematic diagrams of (**a**) top contact bottom gate and (**b**) top contact top gate structured IGZO TFT

~8.3 cm^2 V^{-1} s^{-1} [131]. Up till now, due to its advantages including high carrier mobility compatible with large panel size display, good stability, low-temperature fabrication process and high transparency, a-IGZO is still placed in the dominant position as the channel material of TFT.

Figure 1.31 shows the two typical structures of IGZO TFT. The top contact bottom gate structure (Fig. 1.31a) has simpler fabricating process with only one mask needed for the source/drain electrodes. As for the top gate in Fig. 1.31b, since there is no exposure of the IGZO surface, the device degradation can be significantly inhibited. In order to meet the future requirement of low power consumption, the subthreshold slope (SS) (defined and calculated by Eq. (1.21) should be decreased so that the operating voltage range can be narrowed down [132]. That is why the replacement of SiO_2 with high-k materials with larger Cox as gate dielectric layer in TFT happens.

$$SS = \frac{dV_{GS}}{d(\log I_D)} = \frac{kT\ln 10}{q}\left(1 + \frac{qN_t}{C_{ox}}\right) \tag{1.21}$$

Dielectrics such as Al_2O_3 [133], HfO_2 [134], Y_2O_3 [135] and BaSrTiO [136] have been studied but the degradation in carrier mobility mentioned in Sect. 1.2.4 is still inevitable due to the large polarization of high-k oxides. In Eq. (1.21), Nt is the trap density at/near the dielectric/a-IGZO interface which directly influences SS. Hence, methods of suppressing current leakage, formation of defect-related traps and interfacial reaction are still being explored to optimize the performance of IGZO TFT. It is well known that the quality of high-k bulk and interface varies with different conditions of post deposition treatment, and so does the performance of the TFT. Experimental results show that both post deposition annealing (PDA) and fluorine treatment are capable of optimizing the properties of the devices. L. X. Qian et al. have done investigations on different annealing time and ambient of a-IGZO TFT with HfLaO as gate dielectric, with results listed in Tables 1.6 and and 1.7 [137, 138].

According to Ref. [137] (Table 1.6), negative oxide charges can be effectively reduced by PDA in O_2, with acceptor-like border and interface traps removed as

Table 1.6 Electrical properties of a-IGZO TFTs with different annealing time in O_2

Annealing time (min)	0	10	30	60	120
μ_{sat} ($cm^2V^{-1}s^{-1}$)	4.3	15.7	35.2	25.7	24.9
SS (V/dec)	0.310	0.231	0.292	0.378	0.350
V_{th} (V)	4.3	3.5	2.8	1.7	1.7
ΔV_{th} (V)	1.8	0.4	−1.1	−2.1	−1.7
I_{on}/I_{off}	7.5×10^5	2.5×10^6	5.2×10^6	6.9×10^6	6.2×10^6
C_{ox} ($\mu F/cm^2$)	0.266	0.264	0.267	0.294	0.286

Table 1.7 Electrical properties of a-IGZO TFTs with different annealing ambient

Annealing ambient	w/o	O_2	N_2	NH_3
μ_{sat} ($cm^2V^{-1}s^{-1}$)	4.3	15.7	35.1	19.3
SS (V/dec)	0.310	0.231	0.206	0.315
V_{th} (V)	4.3	3.5	3.3	1.9
ΔV_{th} (V)	1.8	0.4	−0.03	−0.82
I_{on}/I_{off}	7.5×10^5	2.5×10^6	5.1×10^6	6.1×10^6
C_{ox} ($\mu F/cm^2$)	0.266	0.264	0.241	0.275

well, so the electrical properties of the device is improved significantly after PDA with saturation mobility increases from 4.3 $cm^2\ V^{-1}\ s^{-1}$ to 35.2 $cm^2\ V^{-1}\ s^{-1}$. However, the influence of annealing becomes negligible beyond 60 min and a decrease of mobility is found. As for Table 1.7, N_2 shows the most effective effect of oxygen vacancies are filling together with electron concentration decreasing in a-IGZO, and thus obtains the best electrical performance.

In addition, multicomponent dielectric is always a good choice according to the discussion in several previous sections. Doping SiO_2 into Ta_2O_5 for leakage reducing and oxygen vacancy passivating has been investigated in Ref. [139], as shown in Fig. 1.32, improvement in drive current, V_{th}, leakage current and SS can be found in the TaSiO sample when compared with the Ta_2O_5 one. Furthermore, multicomponent high-k dielectric such as HfLaO [137], LaTaO [140], and NbLaO [77] have all been investigated and proved to be promising candidates. For example, the saturation mobility as high as 39.8 $cm^2\ V^{-1}\ s^{-1}$ has been realized in the fluorinated a-IGZO/HfLaO TFT [141], as exhibited in Fig. 1.33.

1.5.3.4 Other Novel MOS Devices

In planar MOSFET, even though the replacement of SiO_2 with high-k materials can solve the leakage issue, problems caused by short channel such as drain-induced barrier lowering (DIBL) is no longer negligible with the relentless scaling. Hence the idea of multi-gate field effect transistor (MGFET) is proposed to increase the effective channel area. FinFET, one type of MGFET has now been considered as

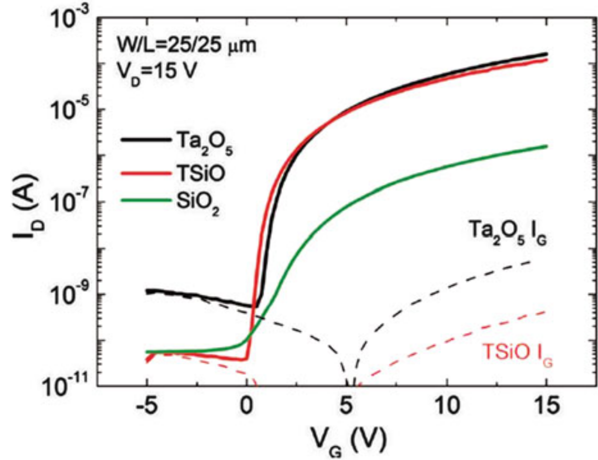


Fig. 1.32 Comparison of I-V characteristics of IGZO TFTs with Ta_2O_5, TaSiO, and SiO_2 as gate dielectric [139]

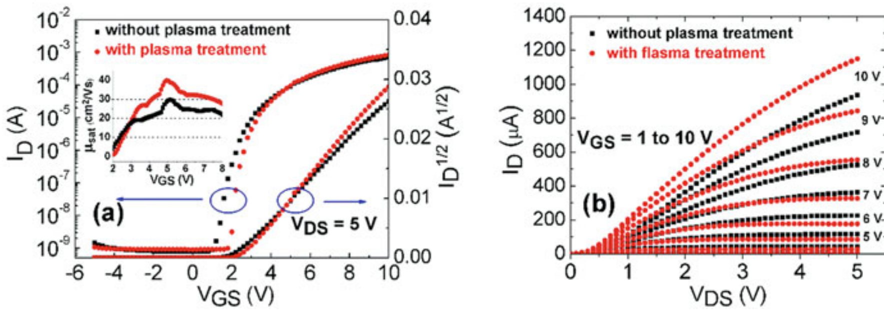
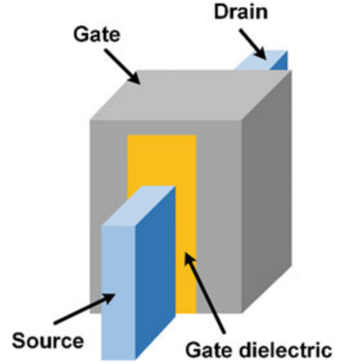


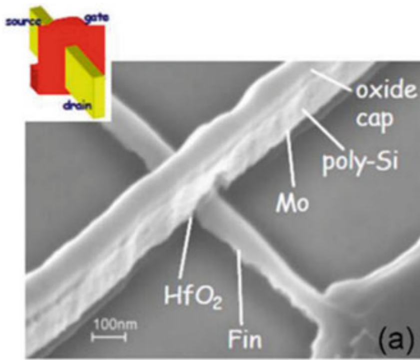
Fig. 1.33 Transfer (**a**) and output (**b**) characteristics of the a-IGZO/HfLaO TFTs with or without CHF_3/O_2 plasma treatment [141]

the most desirable alternative to planar MOSFET due to its simple structure and fabrication process with the simplified structure shown in Fig. 1.34 [142] and has already been adopted in 22 nm technology node by companies like Intel and TSMC.

Same as planar MOSFET, high-k gate dielectrics are also needed to suppress the increasing of leakage current as the devices scale down. FinFET with HfO_2 as dielectric and Mo as metal gate with and without nitrogen incorporation into Mo has been investigated by D. Ha, et al. with SEM image and transfer characteristic demonstrated in Fig. 1.35 [143]. Low leakage current density is achieved for EOT of 1.72 nm, and impressive Vth and SS are obtained. When comparing the I-V curve of the samples with and without nitrogen implant into Mo, a V_{th} shift of 0.45 V is found, indicating a work function modification of Mo, however, the reduction in work function by nitrogen of Mo on HfO_2 is lower than that of Mo on SiO_2 which is probably due to the Fermi-level pinning and nitrogen diffusion into HfO_2 [143], which needs future works to improve.

Fig. 1.34 Simplified structure of FinFET [142]





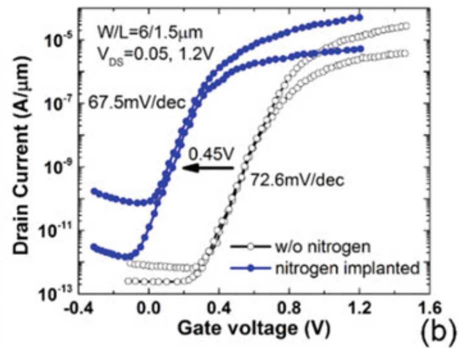


Fig. 1.35 (**a**) SEM image and (**b**) I–V characteristic of HfO_2 FinFET [143]

III-V compound semiconductors have also been applied as the substrate of FinFET. For example, GaAs FinFET with Al_2O_3 as gate dielectric is fabricated and evaluated in Ref. [144]. As shown in Fig. 1.36b, relatively large $I_{on/off}$ ratio (2.54×10^5), small V_{th} (−0.25V), low SS (80 mV/dec at $V_{DS} = 1$V), and weak DIBL are exhibited by the sample, implying great potential of GaAs or other III-V compounds based FinFET in device scaling in the future.

Recently, nano-materials such as graphene, carbon nanotubes, nanowires based MOSFETs have attracted much attention due to their even higher carrier mobility [145, 146]. As a representative, nanowire based FET will be introduced in the section. ZnO nanowire FET with Al_2O_3 as dielectric with the device structure shown in Fig. 1.37a is investigated [147]. Carrier mobility can reach 127 $cm^2V^{-1}s^{-1}$ when the thickness of Al_2O_3 is 21.2 nm and the value decreases with the increase of Al_2O_3 thickness which is probably caused by the decrease of transconductance. The relatively low V_{th} and acceptable leakage current plus the high carrier mobility indicates the potential of ZnO nanowire FET with high-k as gate dielectric, which has been proved by D. Yeom, et al. through the application in NOT and NAND logic circuits [148].

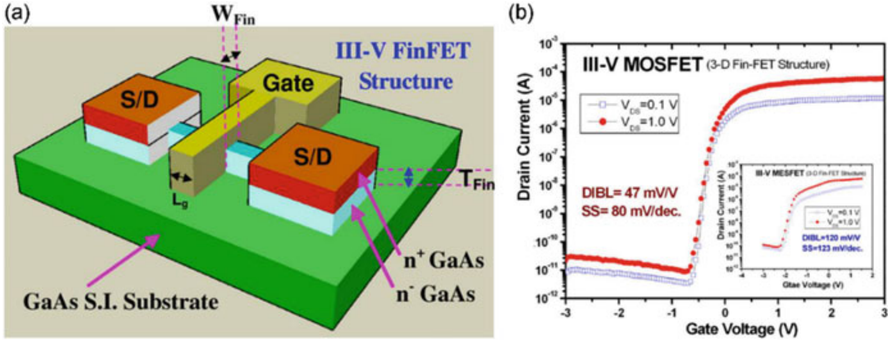


Fig. 1.36 (**a**) Schematic diagram and (**b**) I–V characteristic of GaAs FinFET with Al_2O_3 as gate dielectric [144]

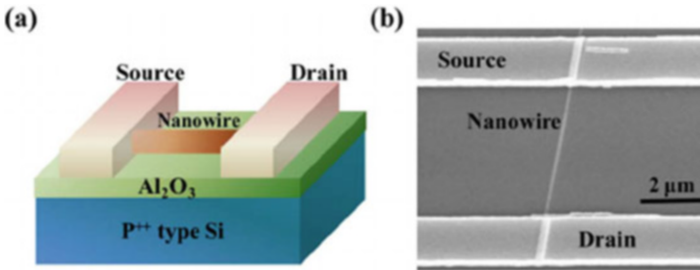
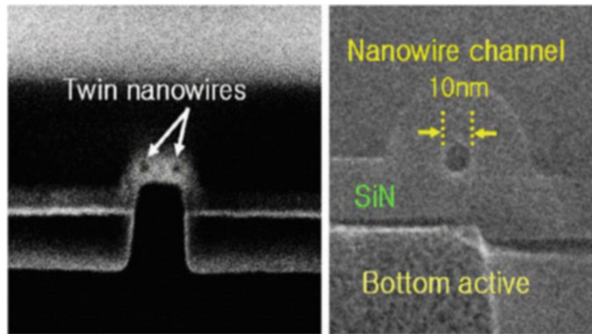


Fig. 1.37 (**a**) Schematic diagram and (**b**) SEM image of ZnO nanowire FET [147]

Fig. 1.38 Cross sectional SEM images of the twin nanowire FET [149]



In addition, impressive electrical properties have been achieved from the idea of gate-all-around twin silicon nanowire MOSFET with the gate length of 30 nm [149]. According to the experimental results, an on/off ratio of 10^6 has been achieved, SS and DIBL are 71 mV/dec and 13 mV/V, implying the good immunity of nanowire to short channel effect. Besides, the testing on hot carrier lifetime and

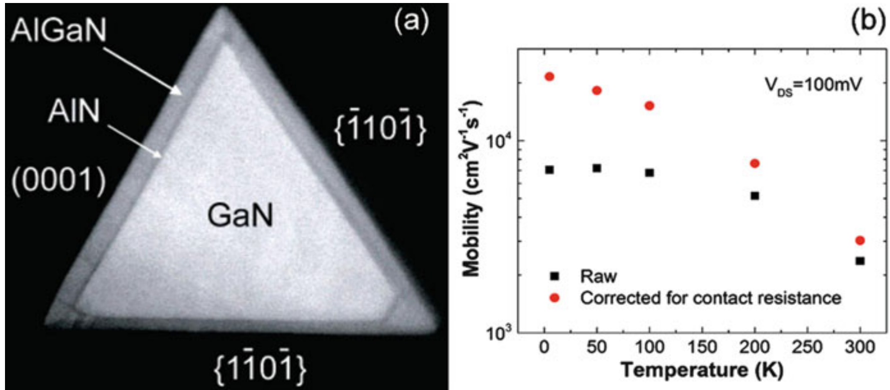


Fig. 1.39 (**a**) TEM image and (**b**) carrier mobility at different temperature of GaN/AlN/AlGaN nanowire [151]

the gate induced drain leakage current indicates its better reliability than that of planar MOSFET. Therefore the twin nanowire is a promising structure and might be improved by applying materials with higher k value. Similarly, III-V compounds can also be considered as the alternative of Si substrate in nanowire based MOSFET, for example, the vertical wrap-gated InAs/high-k nanowire gate stack exhibits low D_{it} near the semiconductor conduction band [150], which is necessary for achieving high carrier mobility.

Furthermore, III-V compound nanowires are suitable for high electron mobility transistors (HEMT). Y. Li, et al. has achieved extremely high mobility using GaN/AlN/AlGaN radial nanowire [151]. MOCVD is used as the method of the formation of the radial structure and ZrO_2 plays the role of gate dielectric. In this work, the carrier mobility, on/off ratio and SS are 21000 $cm^2\ V^{-1}\ s^{-1}$, 10^7, and 68 mV/dec, respectively. These excellent results opens up new opportunities for nanoelectronics and provide new thoughts of the development of MOS devices.

1.6 Summary

In order to keep the trend of device scaling down, high-k is proposed as the alternative of SiO_2 due to the approaching of the physical limit of SiO_2. Since a reversely proportional relationship exists between k value and band gap of materials, apart from k value, many factors including band gap, band offset with the substrate, thermal and kinetic stability, etc. have to be considered when choosing the suitable one. Hf- and La-based high k oxides have attracted most attention recently, especially HfO_2 has already been put in to commercial applications. However, similar to other high k materials, high density of defects and traps in

the bulk and at/near the high-k/substrate interface and low crystallizing temperature are still the main challenges of HfO_2 and La_2O_3. Therefore, post deposition treatments such as thermal annealing and fluorine incorporation are necessary to reduce the defects and traps. Besides, the idea of applying multicomponent high-k materials is an effective way to improve the quality of high-k bulk and the interface, and thus optimize the device performance. Ge and III-V compound semiconductors like GaAs, InGaAs, etc. are expected to replace Si in the future for further mobility increasing. However, their easily formed unstable native oxide and high density of interface states when contact with high-k oxides leading to Fermi-level pinning and mobility degradation still needs more future works.

References

1. S.M. Sze, K.K. Ng, *Physics of Semiconductor Devices* (Wiley, Hoboken, NJ, 1981)
2. R.H. Dennard, F.H. Gaesslen, H. Yu, V.L. Rideout, E. Bassons, A.R. LeBlanc, IEEE J. Solid State Circuits **SC-9**, 256 (1974)
3. D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, H.P. Wong, Proc. IEEE **89**, 259 (2001)
4. H. Wong, H. Iwai, Microelectron. Eng. **83**, 1867 (2006)
5. M. Depas, B. Vermeire, P.W. Mertens, R.L. Van Meirhaeghe, M.M. Heyns, Solid State Electron. **38**, 1465 (1995)
6. G. Chindalore, S.A. Hareland, S. Jallepalli, A.F. Tasch, C.M. Maziar, V.K.F. Chia, S. Smith, IEEE Electron Device Lett. **18**, 206 (1997)
7. H.S. Monose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Saito, H. Iwai, IEEE Trans. Electron Devices **43**, 1233 (1996)
8. M. Cao, P.V. Voorde, M. Cox, W. Greene, IEEE Electron. Device Lett. **19**, 291 (1998)
9. M.L. Green, E.P. Gusev, R. Degraeve, E.L. Garfunkel, J. Appl. Phys. **90**, 2057 (2001)
10. K.S. Kirsch, C.G. Sodini, J. Appl. Phys. **76**, 2284 (1994)
11. D.A. Buchanan, A.D. Marwick, D.J. DiMaria, L. Dori, J. Appl. Phys. **76**, 3595 (1994)
12. J. Robertson, High dielectric constant oxides. Eur. Phys. J. Appl. Phys. **28**, 265 (2004)
13. R.L. Puurumen, J. Appl. Phys. **97**, 121301 (2005)
14. G.D. Wilk, R.M. Wallace, J.M. Anthony, J. Appl. Phys. **89**, 5243 (2001)
15. K.J. Hubbard, D.G. Schlom, J. Mater. Res. **11**, 2757 (1996)
16. D.G. Schlom, J.H. haeni, Mater. Res. Soc **27**, 198 (2002)
17. S. Stemmer, Z.Q. Chen, P.S. Lysagt, J.A. Gisby, J.R. Taylor, Proc. Electrochem. Soc. 2003-2 (Silicon Nitride and silicon Dioxide Thin Insulating films) 119, (2003)
18. M. Houssa, L. Pantisano, L. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S.D. Gendt, G. Groeseneken, Mater. Sci. Eng. Rep. **51**, 37 (2006)
19. R.M.C. Almeida, I.J.R. Baumvol, Surf. Sci. Rep **49**, 1 (2003)
20. J. Robertson, Solid-States Electron. **49**, 283 (2005)
21. G.M. Rignanese, X. Gonze, A. Pasuarello, Phys. Rev. B **63**, 104305 (2001)
22. A.S. Foster, F.L. Gejo, A.L. Shluger, R.M. Nieminen, Phys. Rev. B **65**, 174117 (2002)
23. A.S. Foster, V.B. Sulimov, F.L. Gejo, A.L. Shluger, R.M. Nieminen, Phys. Rev. B **64**, 224108 (2001)
24. P.W. Peacock, J. Robertson, Appl. Phys. Lett. **83**, 2025 (2003)
25. A. Yokozawa, J. Robertson, Phys. Rev. B **55**, 13783 (1997)
26. E.P. Gusev, D.A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P.C. Jamiso, D.A. Neumayer, M. Copel, M.A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L.A. Ragnarsson, P. Ronsheim, K. Rim, R.

J. Fleming, A. Mocuta, and A. Ajmera, IEEE international electron devices meeting 20.1.1, (2001)
27. O. Engstrom, B. Raeissi, J. Piscator, I.Z. Mitrovic, S. Hall, H.D.B. Gottlob, M. Schmidt, P.K. Hurley, K. Cherkaoui, J. Telecommun. Inf. Technol. **1**, 10 (2010)
28. T. Yasuda, Y. Ma, S. Habermehl, G. Lucovsky, Appl. Phys. Lett. **60**, 434 (1992)
29. M. Gutowski, J.E. Jaffe, C.L. Liu, M. Stoker, R.I. Hegde, R.S. Rai, P.J. Tobin, Appl. Phys. Lett. **80**, 1897 (2002)
30. T. Nabatame, M. Kadoshima, K. Iwamoto, N. Mise, S. Migita, M. Ohno, H. Ota, N. Yasuda, A. Ogawa, K. Tominaga, H. Satake, A. Toriumi, IEEE Trans. Electron Devices Meet. **83** (2004)
31. T.L. Li, C.H. Hum, W.L. Ho, H.C.H. Wag, C.Y. Chang, IEEE Trans. Electron Devices **52**, 1172 (2005)
32. H. Wakabayashi, Y. Saito, K. Takeuchi, T. Mogami, T. Kunio, IEEE Trans. Electron Devices Meet. **253** (1999)
33. T.H. Cha, D.G. Park, T.K. Kim, S.A. Jang, I.S. Yeo, J.S. Roh, J.W. Park, Appl. Phys. Lett. **82**, 4192 (2002)
34. J. Lu, Y. Kuo, S. Chatterjee, J.Y. Yewg, J. Vac. Sci. Technol. B **24**, 349 (2006)
35. M.V. Fischetti, D.A. Neumayer, E.A. Cartier, J. Appl. Phys. **90**, 4587 (2001)
36. M.H. Chowdhury, M.A. Mannan, S.A. Mahmood, Int. J. Emerg Technol. Sci. Eng. **2**, 1 (2010)
37. A. Oshiyama, Jpn. J. Appl. Phys. **2**, 37 (1998)
38. W. Monch, Phys. Rev. Lett. **58**, 1260 (1987)
39. J. Robertson, J. Vac. Sci. Technol. B. **18**, 1785 (2000)
40. H. Wong, B. Sen, B.L. Yang, A.P. Huang, P.K. Chu, J. Vac. Sci. Technol. B **25**, 1853 (1858)
41. G. He, Z. Sun, *High-k gate dielectrics for CMOS technology* (Wiley-VCH, Germany, 2012)
42. H. Yamada, T. Shinizu, T. Suzuki, Jpn. J. Appl. Phys. **41**, L368 (2002)
43. Y. Ohshita, A. Ogura, M. Isikawa, T. Kada, H. Mahida, Jpn. J. Phys. **42**, L578 (2003)
44. T. Suntola, J. Antson, U. S. Patent 4058430, (1977)
45. S.M. George, Chem. Rev. **110**, 111 (2010)
46. F. Werner, W. Stals, R. Gortzen, B. Veith, R. Brendel, J. Schnidt, Energy Procedia **8**, 1301 (2011)
47. H. Kim, J. Vac. Sci. Technol. B **21**, 2231 (2003)
48. P. Darmawan, P.S. Lee, Y. Setiawan, J.C. Lai, P. Yang, J. Vac. Sci. Technol. B **25**, 1203 (2007)
49. N. Zhan, M.C. Poon, C.W. kok, K. La, Ng, H. Wong, J. Electrochem. Soc **150**, F200 (2003)
50. H. Wong, K.L. Ng, N. Zhan, M.C. Poon, C.W. Kok, J. Vac. Sci. Technol. B **22**, 1094 (2004)
51. C.S. Kang, H.J. Cho, K. Onishi, R. Nieh, R. Choi, S.K. Gopalan, J.H. Han, J.C. Lee, Appl. Phys. Lett. **81**, 2539 (2002)
52. K.J. Choi, J.H. Kim, S.G. Yoon, W.C. Shin, J. Vac. Sci. Technol. B **22**, 1755 (2004)
53. P. Kroll, Phys. Rev. Lett. **90**, 125501 (2003)
54. Y. Yonamoto, Y. Inaba, N. Akamatsu, Appl. Phys. Lett. **98**, 232906 (2011)
55. C. Yang, L. Hang, J. Xu, Mater. Sci. Semicond. Process **29**, 321 (2015)
56. H.Y. Yu, N. Wu, M.F. Li, C. Zhu, B.J. Cho, D.L. Kwong, W.D. Wang, D.Z. Chi, C.H. Ang, J. Z. Zheng, S. Ramanathan, Appl. Phys. Lett. **81**, 3618 (2002)
57. M.S. Joo, B.J. Co, C.C. Yeo, S.H. Cha, S.J. Whoang, S. Mathew, B.L. Kanta, N. Balasubramanian, D.L. Kwong, IEEE Trans. Electron Devices **50**, 2088 (2003)
58. T.J. Park, J.H. Kim, J.H. Jang, C.K. Lee, K.D. Na, S.Y. Lee, H.S. Jung, M. Kim, S. Han, C.S. Hwang, Chem. Mater. **22**, 4175 (2010)
59. S.H. Bae, C.H. Lee, R. Clark, D.L. Kwong, IEEE Electron Device Lett. **24**, 556 (2003)
60. X. Yu, C. Zhu, M.F. Li, A. Chin, A.Y. Du, W.D. Wang, D.L. Kwong, Appl. Phys. Lett. **85**, 2893 (2004)
61. Y. Yamamoto, K. Kita, K. Kyuno, A. Toriumi, Appl. Phys. Lett. **89**, 032903 (2006)
62. C.H. An, M.S. Lee, J.Y. Choi, H. Kim, Appl. Phys. Lett. **94**, 262901 (2009)

63. M.F. Li, C.X. Zhu, C.Y. Shen, F.F. Xiong, P. Yuan, Y.C. Ywo, A. Chin, D.L. Kwong, S.H. Wang, A.Y. Du, G. Samudra, ECS Trans. **1**, 717 (2006)
64. M. Leskela, K. Kukli, M. Ritala, J. Alloys Compd. **418**, 27 (2006)
65. Y.C. Yeo, T.J. King, C. Hu, Appl. Phys. Lett. **81**, 2091 (2002)
66. G. Lippert, J. Dabrovski, V. Melnik, R. Sorge, C. Wenger, P. Zaumseil, H.J. Mussig, Appl. Phys. Lett. **86**, 042902 (2005)
67. K. Kukli, M. Ritala, T. Pilvi, T. Sajavaara, M. Leskela, A.C. Jones, H.C. Aspinall, D.C. Gilmer, P.J. Tobin, Chem. Mater. **16**, 5162 (2004)
68. Y. Zhao, Material **5**, 1413 (2012)
69. S. Guha, E. Cartier, M.A. Gribelyuk, N.A. Bojarczuk, M.C. Copel, Appl. Phys. Lett. **77**, 2710 (2000)
70. T. Gougousi, D. Niu, R.W. Ashcraft, G.N. Parsons, Appl. Phys. Lett. **83**, 3543 (2003)
71. R.D. Shannon, J. Appl. Phys. **73**, 348 (1993)
72. W.C. Koehler, E.O. Wollan, Acta. Crystallog. **6**, 741 (1953)
73. A.F. Kapustinskii, Q. Rev, Chem. Soc. **10**, 283 (1956)
74. Y. Yokogawa, M. Yosimura, S. Somiya, J. Mater. Sci. Lett. **10**, 509 (1991)
75. N.C. Su, S.J. Wang, A. Chin, IEEE Electron Device Lett. **30**, 1317 (2009)
76. C.Y. Han, W.M. Tang, C.H. Leung, C.M. Che, P.T. Lai, Org. Electron. **15**, 2499 (2014)
77. J.Q. Song, C.Y. Han, P.T. Lai, Comparative study of Nb2O5, NbLaO, and La_2O_3 as ate dielectric of InGaZnO thin film transistor. IEEE Trans. Electron Devices **63**, 1928 (2016)
78. W.J. Song, S.K. So, D.Y. Wang, Y. Qiu, L.L. Cao, Appl. Surf. Sci. **177**, 158 (2001)
79. S. Jeon, F.J. Walker, C.A. Billman, R.A. McKee, H. Hwang, IEEE Electron Device Lett. **24**, 218 (2003)
80. G.J. Norga, C. Marchiori, C. Rossel, A. Guiller, J.P. Locquet, H. Siegwart, D. Caimi, J. Fompeyrine, J.W. Seo, C. Dieker, J. Appl. Phys. **99**, 084102 (2006)
81. J.H. Hao, J. Gao, Z. Wang, D.P. Yu, Appl. Phys. Lett. **87**, 131908 (2005)
82. S.A. Chambers, Y. Liang, Z. Yu, R. Droopad, J. Ramdani, K. Eisenbeiser, Appl. Phys. Lett. **77**, 1662 (2000)
83. R. Droopad, Z. Yu, L. Hilt, J. Curless, C. Overgaard, J.L. Edwards, J. Finder, K. Eisenbeise, W. Ooms, Mater. Sci. Eng. B **87**, 292 (2001)
84. A.B. Posadas, C.W. Lin, A.A. Demkov, S. Zollner, Appl. Phys. Lett. **103**, 142906 (2013)
85. X.B. Lu, Z.G. Liu, X. Zhang, R. Huang, H.W. Zhou, X.P. Wang, B.Y. Nguyen, J. Phys. D. Appl. Phys. **36**, 3047 (2003)
86. X.B. Lu, Z.G. Liu, G.H. Shi, H.Q. Ling, H.W. Zhou, X.P. Wang, B.Y. Nguyen, Appl. Phys. A Mater. Sci. Process **78**, 921 (2003)
87. W.F. Xiang, H.B. Lu, B.H. Chen, M. He, X.B. Lu, L.F. Liu, H.Z. Guo, Z.Y. Liang, Chin. Phys. Lett. **22**, 182 (2005)
88. I.Y. Chang, S. You, M. Chen, P. Juan, C. Chen, J.Y. Lee, J. Appl. Phys. **105**, 104512 (2009)
89. S. Takagi, A. Toriumi, M. Iwase, H. Tango, IEEE Trans. Electron Devices **41**, 2357 (1994)
90. Y.K. Kim, S.H. Lee, S.J. Choi, H.B. Park, Y.D. Seo, K.H. Chin, D. Kim, J.S. Lim, W.D. Kim, K.J. Nam, M.H. Cho, K.H. Hwang, Y.S. Kim, S.S. Kim, Y.W. Park, J.T. Moon, S.L. Lee, M. Y. Lee, IEEE International Electron Devices Meeting, Technical Digest, (2000)
91. J. Lutzen, A. Bimer, M. Goldbach, M. Gutsche, T. Hecht, S. Jakschik, A. Orth, A. Sanger, U. Schroder, H. Seidl, B. Sell, D. Schumann, Symposium on VLSI Technology, Digest of Technical Papers, (2002)
92. E. Atanassova, A. Paskaleva, Microelectron. Reliab. **47**, 913 (2007)
93. N. Pawlak, M. Popovici, J. Swerts, K. tomida, M.S. Kim, B. Kaczer, K. Posomer, M. Schaekers, P. Favia, H. Bender, IEEE International Electron Devices Meeting, 929, (2010)
94. D. Zhou, U. Schroeder, J. Xu, J. Heitmann, G. Jegert, W. Weinreich, M. Kerber, S. Knebel, E. Erben, T. Mikolajick, J. Appl. Phys. **108**, 124104 (2010)
95. S.K. Kim, G.J. Choi, S.Y. Lee, H. Seo, S.W. Lee, J.H. Han, H.S. Ahn, S. Han, C.S. Hwang, Adv. Mater. **20**, 1429 (2008)

96. S. Mori, Y. Araki, M. Sato, H. Meguro, H. Tsunoda, E. Kamiya, K. Yoshikawa, N. Arai, E. Sakagami, IEEE Trans. Electron Devices **43**, 47 (1996)
97. A. Sheikholeslami, P.G. Gulak, Proc. IEEE **88**, 677 (2000)
98. J. Pu, S.J. Kim, B.J. Cho, IEEE Trans. Electron Devices **56**, 2739 (2009)
99. W. He, J. Pu, S.H. Chan, B.J. Cho, IEEE Trans. Electron Devices **56**, 2746 (2009)
100. X.D. Huang, L. Liu, J.P. Xu, P.T. Lai, IEEE Trans. Device Mater. Reliab. **13**, 490 (2011)
101. H. Park, G. Bersuker, D. Gilmer, K.Y. Lim, M. Jo, H. Hwang, A. Padovani, L. Larcher, P. Pavan, W. Taylor, P.D. Kirsch, Proc. IMW **175** (2010)
102. J.K. Hyo, S.Y. Cha, D.J. Choi, Mater. Sci. Semcond. Process **13**, 9 (2010)
103. Y.M. Pan, W.W. Yeh, IEEE Trans. Electron Devices **55**, 2354 (2008)
104. Y.H. Wu, L.L. Chen, M.L. Wu, C.C. Lin, C.H. Chang, IEEE Electron Device Lett. **31**, 1008 (2010)
105. X.G. Wang, J. Liu, W.P. Bai, D.L. Kwong, IEEE Trans. Electron Devices **51**, 597 (2004)
106. X.D. Huang, P.T. Lai, J.K.O. Sin, Appl. Phys. A Mater. Sci. Process **108**, 229 (2012)
107. R.P. Shi, X.D. Huang, C.H. Leung, J.K.O. Sin, P.T. Lai, IEEE Trans. Device Mater. Rev. **15**, 123 (2015)
108. X.D. Huang, J.K.O. Sin, P.T. Lai, IEEE Tran. Electron Devices **58**, 4235 (2011)
109. X.D. Huang, P.T. Lai, J.K.O. Sin, Solid State Electron. **79**, 285 (2013)
110. Z. Liu, C. Lee, V. Narayanan, G. Pei, E.C. Kan, IEEE Trans. Electron Devices **49**, 1606 (2002)
111. J.C. Wang, C.T. Lin, C.S. Lai, J.L. Hsu, Appl. Phys. Lett. **97**, 023513 (2010)
112. X.D. Huang, P.T. Lai, J.K.O. Sin, ECS Solid State Lett. **1**, Q45 (2012)
113. J.H. Chen, W.J. Yoo, D.S.H. Chan, L.J. Tang, Appl. Phys. Lett. **86**, 073114 (2005)
114. Y. Zhou, J. Yin, H. XU, Y. Xia, Z. Liu, A. Li, Y. Gong, L. Pu, F. Yan, Y. Shi, Appl. Phys. Lett. **97**, 143504 (2010)
115. H.T. Lue, S.Y. Wang, E.K. Lai, Y.H. Shih, S.C. Lai, L.W. Yang, K.C. Chen, J. Ku, K.Y. Hsieh, R. Liu, C.Y. Lu, in IEEE International Electron Devices Meeting, 547, (2005)
116. Y.Q. Wang, W.S. Hwang, G. Zhang, G. Samudra, Y.C. Yeo, W.J. Yoo, IEEE Trans. Electron Devices **54**, 2699 (2007)
117. B. Chakrabarti, H. Kang, B. Brennan, T.J. Park, K.D. Cantley, A. Pirkle, S. Mcdonell, J. Kim, R.M. Wallace, E.M. Vogel, IEEE Trans. Electron Devices **58**, 4189 (2011)
118. M. Zhao, R. Liang, J. Wang, J. Xu, Appl. Phys. Lett. **102**, 142906 (2013)
119. C.X. Li, X. Zou, P.T. Lai, J.P. Xu, C.L. Chan, Microelectron. Reliab. **48**, 526 (2008)
120. H.X. Xu, J.P. Xu, C.X. Li, C.L. Chan, P.T. Lai, Appl. Phys. A Mater. Sci. Process **99**, 903 (2010)
121. C.X. Li, C.D. Wang, C.H. Leung, P.T. Lai, J.P. Xu, Microelectron. Eng. **86**, 1596 (2009)
122. W.B. Chen, B.S. Shie, C.H. Cheng, K.C. Hsu, A. Chin, IEEE International Electron Devices meeting, 420, (2010)
123. C.X. Li, H.X. Xu, P.T. Lai, J.P. Xu, Appl. Phys. Lett. **93**, 022910 (2009)
124. F. Ji, J.P. Xu, J.G. Liu, C.X. Li, P.T. Lai, Appl. Phys. Lett. **98**, 182901 (2011)
125. F. Ji, J.P. Xu, Y. Huang, L. Liu, P.T. Lai, IEEE Trans. Electron Devices **61**, 3608 (2014)
126. F.S. Aguirre-Tostado, M. Milojevic, K.J. Choi, H.C. Kim, C.L. Vogel, J. Kim, T. Yang, Y. Xuan, P.D. Ye, R.M. Wallace, Appl. Phys. Lett. **93**, 061907 (2008)
127. M.K. Lee, C.F. Yen, Appl. Phys. A Mater. Sci. Process **116**, 2051 (2014)
128. L.N. Liu, H.W. Choi, P.T. Lai, J.P. Xu, J. Vac. Sci. Technol. B **33**, 050601 (2015)
129. L.S. Wang, J.P. Xu, L. Liu, W.M. Tang, P.T. Lai, Appl. Phys. Express **7**, 061201 (2014)
130. L.N. Liu, H.W. Choi, J.P. Xu, P.T. Lai, Appl. Phys. Lett. **107**, 213501 (2015)
131. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirao, H. Hosono, Nature **432**, 488 (2004)
132. J.S. Park, W.J. Maeng, H.S. Kim, J.S. Park, Thin Solid Films **520**, 1679 (2012)
133. L.F. Lan, J.B. Peng, IEEE Trans. Electron Devices **58**, 1452 (2011)
134. Y.H. Lin, J.C. Chou, J. Nanomater. **2014**, 347858 (2014)
135. H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, H. Hosono, Appl. Phys. Lett. **89**, 112123 (2006)

136. J. Kim, C. Fuentes-Hernandez, B. Kippelen, Appl. Phys. Lett. **93**, 242111 (2008)
137. L.X. Qian, P.T. Lai, IEEE Trans. Device Mater. Reliab. **14**, 177 (2014)
138. L.X. Qian, P.T. Lai, Microelectron. Reliab. **54**, 2396 (2014)
139. P. Barquinha, L. Pereira, G. Goncalves, R. Martins, D. Kuscer, M. Kosec, E. Fortunato, J. Electrochem. Soc. **156**, H824 (2009)
140. L.X. Qian, P.T. Lai, W.M. Tang, Appl. Phys. Lett. **104**, 123505 (2014)
141. L.X. Qian, P.T. Lai, IEEE Electron Device Lett. **35**, 363 (2014)
142. D Ghattacharya, N.K. Jha, 2014, 365689, (2014).
143. D. Ha, H. Takeuchi, Y.K. Choi, T.J. King, W.P. Bai, D. L. Kwong, A. Agarwal, M. Ameen, IEEE International Electron Devices meeting, 643, (2004)
144. S.H. Chen, W.S. Liao, H.C. Yang, S.J. Wang, Y.G. Liaw, H. Wang, S. Gu, M.C. Wang, Nanoscale Res. Lett. **7**, 431 (2012)
145. F. Schwierz, Nat. Nanotechnol. **5**, 487 (2010)
146. P.A. Alvi, K.M. Lal, M.J. Siddiqui, S.A.H. Naqvi, Indian J. Pure Appl. Phys. **43**, 899 (2005)
147. M. Choe, G. Jo, J. Maeng, W.K. Hong, M. Jo, G. Wang, W. Park, B.H. Lee, H. Hwang, T. Lee, J. Appl. Phys. **107**, 034504 (2010)
148. D. Yeom, K. Keem, J. Kang, D.Y. Jeong, C. Yoon, D. Kim, S. Kim, Nanotechnology **19**, 265202 (2008)
149. S.D. Suk, S.Y. Lee, S.M. Kim, E.J. Yoon, M.S. Kim, M. Li, C.W. Oh, K.H. Yeo, S.H. Kim, D. S. Shin, K.H. Lee, H.S. Park, J.N. Han, C.J. Park, J.B. Park, D.W. Kim, D. Park, B.I. Ryu, IEEE International Electron Devices meeting, 717, (2005)
150. J. Wu, K. Jansson, A.S. Badadi, M. Berg, E. Lind, L.E. Wernersson, IEEE Trans. Electron Devices **63**, 584 (2016)
151. Y. Li, J. Xiang, F. Qian, S. Gradecak, Y. Wu, H. Yan, D.A. Blom, C.M. Lieber, Nano Lett. **6**, 1468 (2006)