On the Electronic Realizations of Fractional-Order Phase-Lead-Lag Compensators with OpAmps and FPAAs

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Abstract It is well known that the fractional-order phase-lead-lag compensators can achieve control objectives that are not always possible by using their integer-order counterparts. However, up to now one can find only a few of publications discussing the strategies for parameters' tuning of these compensators, with only simulation results reported. This is due in part to the implicit difficulties on the implementation of circuit elements with frequency responses of the form $s^{\pm\lambda}$ that are named "fractances". In this regard, there exist approximations with rational functions, but the drawback is the difficulty to approximate the required values with the ones of the commercially-available resistances and capacitors. Consequently, fractional compensators have not been appreciated by the industry as it is in the academia. Therefore, motivated by the lack of reported implementations, this chapter is structured as a tutorial that deals with the key factors to perform, with the frequency-domain approach, the design, simulation and implementation of integer-order and fractional-order phase-lead-lag compensators. The circuit implementations are performed with

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Operational Amplifiers (OpAmps) and with Field Programmable Analog Arrays (FPAA). Emphasis is focused in the obtaining of commercially-available values of resistances and capacitors. Therefore, the design procedure starts with the use of equations that provide the exact and unique solution for each parameter of the compensator, avoiding conventional trial-and-error procedures. Then, five OpAmp-based configurations for integer-order and fractional-order realizations are described in terms of basic analog building blocks, such as integrators or differential amplifiers, among others. The corresponding design equations are also provided. Then, six examples are presented for both, OpAmp-based and FPAA-based implementations with the simulation and experimental results discussed regarding other results reported in the literature.

Keywords Fractional calculus · Fractional-order lead/lag compensators · Field programmable analog array

1 Introduction

Proportional-Integral-Derivative (*PID*) controllers [4–6], and lead/lag compensators are the control strategies most used in today's industry. The phase-lag compensator reduces the static error by increasing the low-frequency gain without any resulting instability, and increases the phase margin of the system to yield the desired overshoot [30]. Meanwhile, the phase-lead compensator change the phase diagram to reduce the percent overshoot and to reduce the peak time [30]. The design of lead/lag compensators may require four-step and twelve-step trial-and-error approaches, respectively [30]. Typically, during the design stage the plant is modeled by its transfer function with integer orders q on the Laplace frequency s^q. However, experimental evidences show that physical systems can be modeled with higher accuracy using fractional-order transfer functions [16, 20, 46]. On this direction, it is known that the fractional-order PID controllers and phase-lead-lag compensators have better performance than their integer counterparts [16, 22, 27, 28, 35]. That is due to the addition of degrees of freedom, which can be used to incorporate additional control objectives. For instance, in the case of lead/lag compensators it can be established a constrain in the initial value of the error signal (actuator's constraint) [35].

Although fractional calculus has been studied from Leibniz in 1965, its practical use has been restricted. It was not until the development of new computing environments and numerical calculus (e.g. MATLAB) when researchers introduced this theory to the modeling and control of systems [16, 24, 36, 38]. In fact, those computing environments allowed other complex control strategies such as the reported in [7–10, 12, 13, 47]. That way, in 1999 Podlubny proposed the first fractional PID controller [32]. Up to now one can find several realizations for this kind of controller [22, 24, 27, 28, 32, 38, 41, 46]. In addition, researchers have developed the corresponding rules for parameters' tuning, some of them considering Ziegler-Nichols rules [17, 25, 40], optimization methods [29, 36], techniques in the frequency

domain [18, 25, 39], which offer robustness to the controller facing parametric uncertainties of the process and presence of external perturbations [2]; or also in techniques for intelligent computing, such as: neural networks [31], genetic algorithms [14], or fuzzy logic [43, 45]. In general, these techniques can be classified as analytical, numeric or rules-based ones. A summary of them is given in [29, 41, 42]. Unfortunately, the fractional-order lead/lag compensators have not been reported as abundantly as the fractional PID controllers. In [29, 34] there have been studied the following fractional-order lead/lag compensator (and rational-order approximations for such a compensator)

$$C(s) = K\left(\frac{1+\alpha\tau s}{1+\tau s}\right)^{\lambda}, \qquad \lambda \in (0,\infty) \tag{1}$$

In [35] it was reported a method for the unique solution of the parameters α, τ and q of the compensator

$$C(s) = K\left(\frac{1+\alpha\tau s^{q}}{1+\tau s^{q}}\right), \qquad q \in (0,2) \tag{2}$$

Unfortunately, to the best of the authors' knowledge, analog implementations of this compensator have not been reported. As in the case of PID controllers, it is due to the difficulties to accomplish the design of circuit elements with frequency responses of the form $s^{-\lambda}$ or s^{μ} that are named "fractances". The fractances are circuit elements with constant phase response at all frequencies [23]. For instance, very few physical realizations have been reported related to "fractal capacitances" [11, 21]. Unfortunately, those elements are bulky, require chemical compounds with difficult manipulation and the order λ cannot be modified easily. As alternatives, there exist approximations with rational functions in s for the operators $s^{-\lambda}$ or s^{μ}, that are obtained from Carlson methods, Oustaloup, continuous fractions expansion (CFE) [16, 33], among others. The resulting functions are implemented with arrays of resistances, capacitors and inductors in ladder networks [33]. The drawback of these realizations is the difficulty to approximate the required values with the ones of the commercially-available resistances and capacitors [19], in addition they can require negative impedance converters [3, 33], or inductors [15].

From the difficulties on the implementations mentioned above and motivated by the lack of reported implementations of (2), this chapter is structured as a tutorial that deals with the key factors to perform the design, simulation and implementation of integer and fractional-order phase-lead-lag compensators. It is proposed the use of first-order analog approximations for fractional derivatives and integrals, with the main advantage of using integrators of integer order, differential amplifiers, two-inputs adder amplifiers, and conventional lead-lag networks, all of them realized with OpAmps. Most important is that the resulting circuits can be implemented with commercially-available resistances and capacitors, avoiding the use of negative impedance converters or inductors. Each design is realized obtaining the parameters of (2) with the procedure reported in [35]. Five configurations for integer

and fractional-order compensators are verified experimentally from realizations using OpAmps uA741 and using an Application Specific Integrated Circuit (ASIC) that is known as Field-programmable Analog Array (FPAA) AN231E04 from Anadigm [1]. Six design examples of both integer and fractional-order phase-lead-lag compensators are presented.

2 Theoretical Background

This section describes the calculus of derivatives and integrals of fractional order, the corresponding Laplace transforms, and the fractional order transfer function. From these concepts fractional order phase-lead-lag compensators are described in Sect. 2.3.

2.1 Derivative and Integral of Fractional Order

The Riemann-Lieuville definition for calculation of fractional derivatives and integrals establishes [20]

$$\mathscr{D}_t^{\alpha} f(t) = \frac{1}{\Gamma(m-\alpha)} \left(\frac{d}{dt}\right)^m \int_0^t \frac{f(\tau)}{(t-\tau)^{\alpha-m+1}} d\tau \tag{3}$$

where $\alpha \in \mathbb{R}, m-1 < \alpha < m, m \in \mathbb{N}$ and $\Gamma(\cdot)$ is Gamma function. For $\alpha > 0$, $\alpha < 0$ and $\alpha = 0$ one gets the fractional derivative, integral and identity function.

2.2 Laplace Fractional Operator and Fractional-Order Transfer Function

Laplace Transform with initial conditions equal to zero of (3) is given by [20]

$$\mathscr{L}\left\{\mathscr{D}_t^{\alpha} f(t)\right\} = s^{\alpha} F(s) \tag{4}$$

where $F(s)$ denotes Laplace transform of $f(t)$, and s^{α} is the Laplace operator of fractional order expressed as

$$s^{\alpha} = (j\omega)^{\alpha} = \omega^{\alpha}\left[\cos\left(\frac{\alpha\pi}{2}\right) + j\sin\left(\frac{\alpha\pi}{2}\right)\right] \tag{5}$$

Since Laplace transform is a lineal operator, (4) can be applied to a differential equation of fractional order with coefficients $a_k, b_k \in \mathbb{R}$ and input and output signals $u(t)$ and $e(t)$ to obtain the transfer function [2]

$$H(s) = \frac{U(s)}{E(s)} = \frac{b_m s^{\beta_m} + b_{m-1} s^{\beta_{m-1}} + \cdots + \beta_0 s^{\beta_0}}{a_n s^{\alpha_n} + a_{n-1} s^{\alpha_{n-1}} + \cdots + \alpha_0 s^{\alpha_0}} \tag{6}$$

where $U(s) = \mathscr{L}\{u(t)\}$ and $E(s) = \mathscr{L}\{e(t)\}$.

2.3 *Integer and Fractional-Order Phase-Lead-Lag Compensators*

The phase-lag compensator reduces the static error by increasing the low-frequency gain without any resulting instability. This compensator also increases the phase margin of the system to yield the desired overshoot in the transient response [30]. In most cases reported in the literature, that design process is a four-step trial-and-error approach based on graphic approximation (Bode plots) [30]. On the other hand, the phase-lead compensator is designed, via Bode plots, to change the phase diagram in order to increase the phase margin, reduce the percent overshoot, and increase the bandwidth (by increasing the gain crossover frequency) to obtain a faster transient response with a reduced peak time [30]. Typically, the design procedure of this compensator requires a twelve-step trial-and-error approach.

In 2003 and 2013 Wang and Tavazoei reported, respectively, exact and unique solutions for integer-order and fractional-order phase-lead-lag compensators when the gain and phase that the compensator must provide are known for a given frequency. The advantage of those methods is that no trial-and-error or other guesswork is needed. Considering this advantage, in this work are employed the procedures described by Wang and Tavazoei. This way, this section summarizes the design equations developed in [35, 44]. Examples of the use of these equations are provided in Sect. 5.

2.3.1 Exact Solution for Integer-Order Phase-Lead-Lag Compensation [44]

Consider M dB and p rad ($-\pi/2 \leq p \leq \pi/2$) as the required magnitude and phase which should be provided by the integer-order phase-lead-lag compensator at a frequency $\omega = \omega_c$ to yield the desired transient response. This goal is obtainable by means of the compensator

$$C(s) = \frac{1 + \alpha\tau s}{1 + \tau s} \tag{7}$$

if and only if

$$c > \sqrt{1 + \delta^2} \quad \textit{and} \quad 0 < p < \pi/2 \qquad (\textit{phase-lead compensation}) \tag{8}$$

$$c < \frac{1}{\sqrt{1 + \delta^2}} \quad \textit{and} \quad -\pi/2 < p < 0 \quad (\textit{phase-lag compensation}) \tag{9}$$

where $c = 10^{M/20}$ and $\delta = \tan(p)$. If (8) or (9) are satisfied, the compensator parameters α and τ can be calculated as

$$\alpha = \frac{c(c\sqrt{1+\delta^2}-1)}{c-\sqrt{1+\delta^2}} \quad and \quad \tau = \frac{c-\sqrt{1+\delta^2}}{c\delta\omega_c} \tag{10}$$

2.3.2 Exact Solution for Fractional-Order Phase-Lead-Lag Compensation [35]

Consider M dB and p rad ($-\pi/2 \leq p \leq \pi/2$) as the required magnitude and phase which should be provided by a fractional-order compensator at the frequency $\omega = \omega_c^q$. This objective is obtainable by means of

$$C_f(s) = K\left(\frac{1+\alpha\tau s^q}{1+\tau s^q}\right), \quad q \in (0,2) \tag{11}$$

if and only if

$$\cot\left(\frac{q\pi}{2}\right) < \frac{c\cos(p)-1}{c\sin(p)}, \quad 0 < p < \frac{\pi}{2} \quad (\textit{phase-lead compensation}) \tag{12}$$

$$\cot\left(\frac{q\pi}{2}\right) < \frac{c-\cos(p)}{\sin(p)}, \quad -\frac{\pi}{2} < p < 0 \quad (\textit{phase-lag compensation}) \tag{13}$$

If (12) or (13) are satisfied, the parameters α and τ can be calculated as

$$\alpha = \frac{uv\tan\left(\frac{q\pi}{2}\right)-1}{v\tan\left(\frac{q\pi}{2}\right)-1}, \qquad \tau = \frac{1}{\omega_c^q}\left[v\sin\left(\frac{q\pi}{2}\right)-\cos\left(\frac{q\pi}{2}\right)\right] \tag{14}$$

where

$$u = c\frac{c-\cos(p)}{c\cos(p)-1}, \qquad v = \frac{c\cos(p)-1}{c\sin(p)} \tag{15}$$

In the case of the fractional-order phase-lead compensator ($0 < p < \pi/2$), the value of q is selectable in the range $(q^*, 2)$, where

$$q^* = \frac{2}{\pi}\tan^{-1}\left(\frac{c\sin(p)}{c\cos(p)-1}\right), \quad for \quad c > \frac{1}{\cos(p)} \tag{16}$$

$$q^* = 2 + \frac{2}{\pi}\tan^{-1}\left(\frac{\sin(p)}{c-\cos(p)}\right), \quad for \quad c < \frac{1}{\cos(p)} \tag{17}$$

Similarly, for the fractional-order phase-lag compensator ($-\pi/2 < p < 0$), the value of q is selectable in the range $(q^*, 2)$, where

$$q^* = \frac{2}{\pi}\tan^{-1}\left(\frac{\sin(p)}{c-\cos(p)}\right), \quad for \quad c < \cos(p) \tag{18}$$

$$q^* = 2 + \frac{2}{\pi}\tan^{-1}\left(\frac{c\sin(p)}{c\cos(p)-1}\right), \quad for \quad c > \cos(p) \tag{19}$$

2.3.3 Exact Solution for Integer-Order Phase-Lead-Lag Compensation with Actuator's Constrains [35]

One advantage of the fractional-order phase-lead and phase-lag compensators regarding their integer-order counterparts is the fact that the order q, selectable in the range $(q^*, 2)$, represents and additional degree of freedom, which can be used to satisfy another control objective. This way, the exact value of q can be chosen based on an acceptable value for the initial peak of the control signal, i.e., establishing an actuator constraint.

Supposing that it is desired that the initial peak of the control signal be equal to u_0 when the input is a unit step reference, for lead compensation ($u_0 \in (K, \infty)$) the exact value of q must be selected as

$$q = \begin{cases} \frac{2}{\pi}\tan^{-1}\left(\frac{u_0-K}{v(u_0-Ku)}\right) & \text{if} \quad v(u_0-Ku) > 0 \\ 1 & \text{if} \quad v(u_0-Ku) = 0 \\ 2+\frac{2}{\pi}\tan^{-1}\left(\frac{u_0-K}{v(u_0-Ku)}\right) & \text{if} \quad v(u_0-Ku) < 0 \end{cases} \tag{20}$$

and in the case of lag compensation ($u_0 \in (0, K)$) the order q must be calculated as

$$q = \begin{cases} 2+\frac{2}{\pi}\tan^{-1}\left(\frac{u_0-K}{v(u_0-Ku)}\right) & \text{if} \quad v(u_0-Ku) > 0 \\ 1 & \text{if} \quad v(u_0-Ku) = 0 \\ \frac{2}{\pi}\tan^{-1}\left(\frac{u_0-K}{v(u_0-Ku)}\right) & \text{if} \quad v(u_0-Ku) < 0 \end{cases} \tag{21}$$

2.4 Realization of Analog Fractances

The challenge in implementing fractional-order transfer functions and, consequently, fractional-order phase-lead-lag compensators is related to the non-existence of circuit elements that reproduce the operator (5). Those elements are called fractances [23], which are characterized by a magnitude response with roll-off $\pm 20\alpha$ deci-

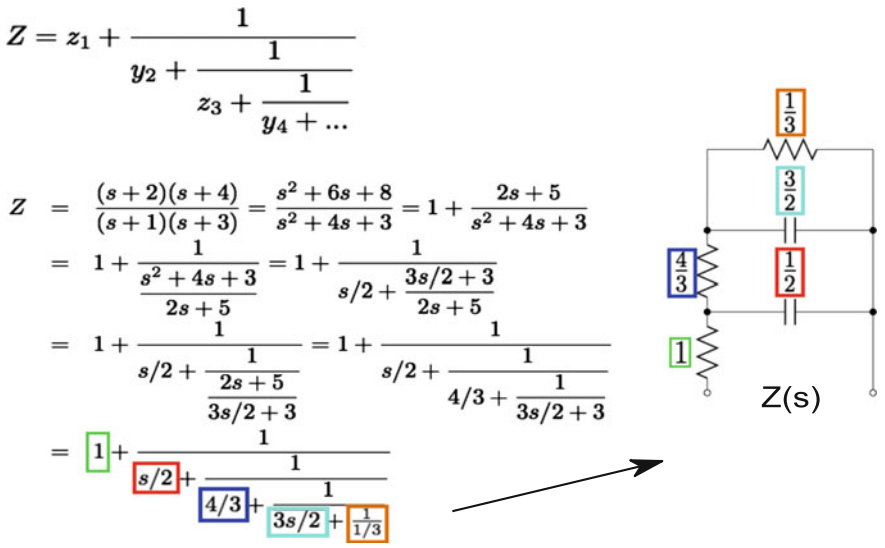


Fig. 1 Method of Cauer for circuit synthesis

bels by decade, and a constant-phase response at all frequencies of $\pm 90\alpha$ degrees. For instance, very few physical realizations have been reported related to "fractal capacitances", capacitors with impedance $Z = 1/(s^{\alpha}C)$ [11, 21]. Unfortunately, those elements are bulky, require chemical compounds with difficult manipulation and the order α cannot be modified easily. Alternatively, the fractances can be approached in a desired bandwidth with rational functions from the methods of Newton, Carlson, Muir, Oustaloup, Matsuda, power series expansion (PSE), continuous fractions expansion (CFE), among others [16, 23, 33]. Once a rational function is obtained it can be synthesized with ladder networks of Cauer, or Foster [33], tree structure, or transmission lines [16, 33]. The circuit components can be resistors, inductors [15], capacitors and sometimes negative impedance converters [3, 33]. One example for synthesis by Cauer method is given in Fig. 1. The drawback of these realizations is the difficulty to approximate the required values with the ones of the commercially-available resistances and capacitors [19].

Once the procedures to design integer-order and fractional-order phase-lead-lag compensators have been described, in the following sections will be focused the problem of circuit implementation.

3 Basic Building Blocks

This section presents the OpAmp-based basic building blocks that will be employed in Sect. 4 to perform the synthesis of integer-order and fractional-order phase-lead-lag compensators.

3.1 Inverting Integrator (IInt)

The OpAmp-based Inverting Integrator of Fig. 2a uses capacitive feedback to integrate the input signal V_{in1}. The transfer function of this circuit is given by

$$\frac{V_{out_1}}{V_{in_1}} = -\frac{1}{R_g C_g s} = -\frac{1}{s} \tag{22}$$

where C_g can be used as degree of freedom and $R_g = 1/C_g$. Then, magnitude (Z_m) and frequency (Ω_f) denormalizations can be used to obtain commercially available values of the passive elements and the desired frequency response.

3.2 Non-inverterting and Inverting Amplifiers (NIA, IA)

The OpAmp-based Non-inverting Amplifier (NIA) and Inverting Amplifier (IA) depicted in Fig. 2b and c use resistive feedback to amplify the input signals V_{in2} and V_{in3}. The corresponding transfer functions are

$$\frac{V_{out_2}}{V_{in_2}} = 1 + \frac{R_{e2}}{R_{e1}}, \qquad \frac{V_{out_3}}{V_{in_3}} = -\frac{R_{f2}}{R_{f1}} \tag{23}$$

3.3 Weighted Differential Amplifier and Differential Amplifier

The Weighted Differential Amplifier (WDA) amplifies the weighted difference between two voltages. A particular case is the Differential Amplifier (DA), which amplifies the difference between the two voltages but does not amplify the particular voltages. Fig. 2d shows an implementation of a WDA with R_{g1} and R_{g2} used to control the gains and with R_g as degree of freedom. By nodal analysis the output voltage V_{out_4} results

$$V_{out_4} = \frac{R_g}{R_{g1}} V_{1A} - \frac{R_g}{R_{g2}} V_{2A} \tag{24}$$

Alternatively, by omitting in Fig. 2d the landed resistors R_{g1} and R_{g2} and by choosing $R_{g1} = R_{g2} = R_{g3}$ is obtained the DA of Fig. 2e with output voltage

$$V_{out_5} = \frac{R_g}{R_{g3}} \left(V_{1B} - V_{2B} \right) \tag{25}$$

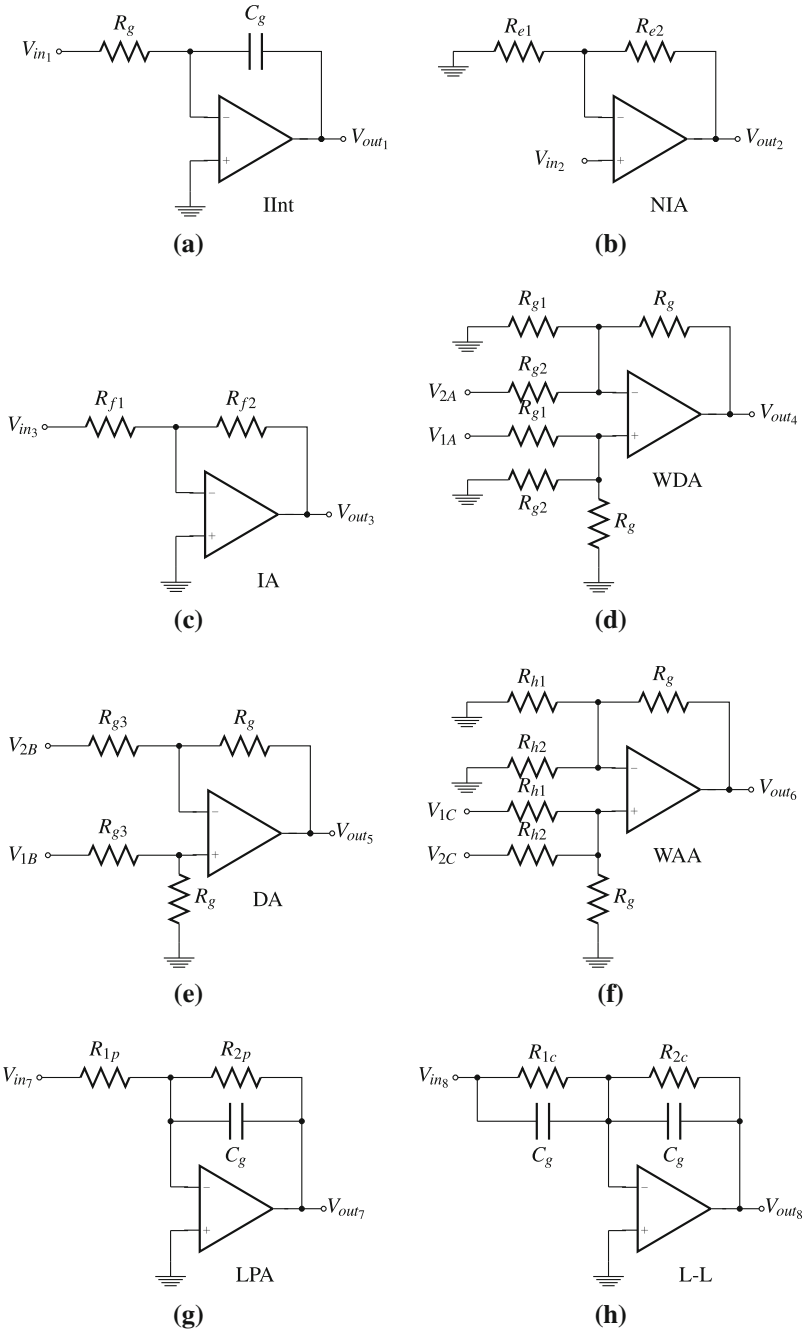


Fig. 2 OpAmp building blocks: **a** Inverting Integrator (IInt). **b** Non-inverting Amplifier (NIA). **c** Inverting Amplifier (IA). **d** Two-input weighted differential amplifier (WDA). **e** Differential Amplifier (DA). **f** Two-input weighted adder amplifier (WAA). **g** Low-Pass Amplifier (LPA). **h** Lead/lag network

3.4 Two-Input Weighted Adder Amplifier (WAA)

It produces an output V_{out_6} equal to the weighted sum of the two inputs V_{1C} and V_{2C}. The realization of Fig. 2f uses R_g as degree of freedom and R_{h1} and R_{h2} to control the weighted factors by means of

$$V_{out_6} = \frac{R_g}{R_{h1}} V_{1C} + \frac{R_g}{R_{h2}} V_{2C} \tag{26}$$

3.5 Lowpass Amplifier (LPA)

Figure 2g shows a first-order inverting Low Pass Filter Amplifier (LPA) ("bilinear filter"). The DC gain and corner frequency of this circuit are $|H|_{s=0} = R_{2p}/R_{1p}$ and $\omega_c = 1/(R_{2p}C_g)$ (C_g can be used as degree of freedom), R_{2p} determines the corner frequency and R_{1p} the DC gain. The transfer function V_{out_7}/V_{in_7} results

$$\frac{V_{out_7}}{V_{in_7}} = -\frac{\dfrac{1}{R_{1p}C_g}}{s + \dfrac{1}{R_{2p}C_g}} \tag{27}$$

3.6 Lead/Lag Network (L-L)

The transfer function of the circuit of Fig. 2h, its pole, its zero and its DC gain can be calculated as

$$\frac{V_{out_8}}{V_{in_8}} = -\frac{R_{2c}}{R_{1c}} \left(\frac{1 + sR_{1c}C_g}{1 + sR_{2c}C_g} \right) \tag{28}$$

$$\omega_z = \frac{1}{R_{1c}C_g}, \quad \omega_p = \frac{1}{R_{2c}C_g}, \quad |H|_{(s=0)} = \frac{R_{2c}}{R_{1c}} \tag{29}$$

Clearly, this network provides positive (leading) phase shift if the zero of the transfer function is closer to the origin of the s-plane than the pole, which occurs if $R_{1c} > R_{2c}$. Conversely, with $R_{1c} < R_{2c}$ the pole is closer than the zero to the origin of the s-plane, and the network provides negative (lagging) phase shift of the output signal relative to the input signal at all frequencies.

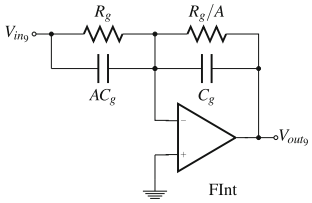


Fig. 3 First-order approximation of a Fractional-order Integrator (FInt)

3.7 Fractional Integrator (FInt)

As mentioned before, the operator s^{-q} cannot be implemented directly, it is required to perform an approximation. Consider the transfer function $V_{out_9}/V_{in_9} = -s^{-q}$. Then, an approximation of order one of a Fractional-order Integrator given by

$$\frac{V_{out_9}}{V_{in_9}} = -\frac{1}{s^q} \approx -\frac{(1-q)s+(1+q)}{(1+q)s+(1-q)} = -\frac{As+1}{s+A} = -\frac{1}{A}\left(\frac{1+As}{1+\frac{s}{A}}\right), \quad A = \frac{1-q}{1+q} \tag{30}$$

can be implemented with an adequate selection of the capacitors and resistances of the Lead-Lag network in Fig. 2h, resulting the circuit of Fig. 3.

4 OPAMP-Based Realization of Integer-Order and Fractional-Order Phase-Lead-Lag Compensators

This section presents OPAMP-based realization of integer-order and fractional-order phase-lead-lag compensators performed with the basic building blocks of Figs. 2 and 3.

4.1 Integer-Order Phase-Lead-Lag Compensator

A phase-lead-lag compensator with DC unity-gain can be realized by means of the OpAmp-based network shown in Fig. 4, which consists of a L-L network connected in series with an IA block (with $R_{f1} = R_{1c}$ and $R_{f2} = R_{2c}$). The transfer function of this network is expressed by

$$\frac{V_{oc}}{V_{ic}} = \frac{1+sR_{1c}C_g}{1+sR_{2c}C_g} = \frac{1+\alpha\tau s}{1+\tau s} \tag{31}$$

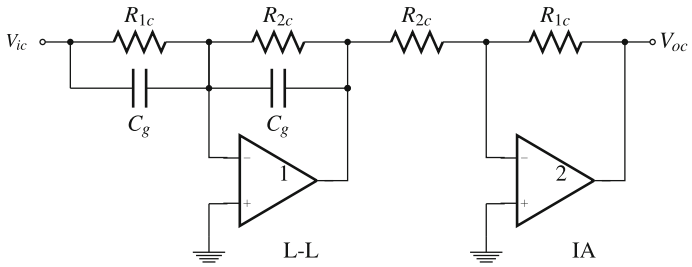


Fig. 4 Integer-order phase-lead-lag compensator

where

$$\tau = R_{2c}C_g, \quad \alpha = \frac{R_{1c}}{R_{2c}} \tag{32}$$

Therefore, for $\alpha > 1$ (i.e. with $R_{1c} > R_{2c}$) and $\alpha < 1$ (i.e. with $R_{2c} > R_{1c}$) are obtained, respectively, phase-lead and phase-lag responses.

4.2 Fractional-Order Phase-Lead-Lag Compensator (1 < q < 2)

Consider the fractional-order phase-lead-lag transfer function given by

$$\frac{V_{oc}(s)}{V_{ic}(s)} = \frac{1 + \alpha\tau s^q}{1 + \tau s^q} \tag{33}$$

where $1< q <2$ is assumed. Algebraic manipulation on (33) leads to

$$V_{oc}(s) + V_{oc}(s)\tau s^q = V_{ic}(s) + V_{ic}(s)\alpha\tau s s^{q-1} \tag{34}$$

and after dividing both sides of (34) by τs^q and regrouping similar terms, it results in

$$V_{oc}(s) = \frac{V_{ic}(s) - V_{oc}(s)}{\tau s s^{q-1}} + \alpha V_{ic}(s) \tag{35}$$

This way, the fractional-order phase-lead-lag compensator with $1< q <2$ can be realized starting from the block diagram shown in Fig. 5a. The corresponding implementation using OpAmps is shown in Fig. 5b. Here, the algebraic operation $(V_{ic}(s) - V_{oc}(s))/\tau$ is performed by the block DA of Fig. 2e, with $R_{g3} = \tau R_g$. The operation $1/s^q = (1/s)(1/s^{q-1})$ is realized by means of the series array of an integer-order Inverter Integrator IInt (with $R_g = 1/C_g$) and a Fractional-order Integrator FInt whit $\tilde{A}$ calculated from (30) as

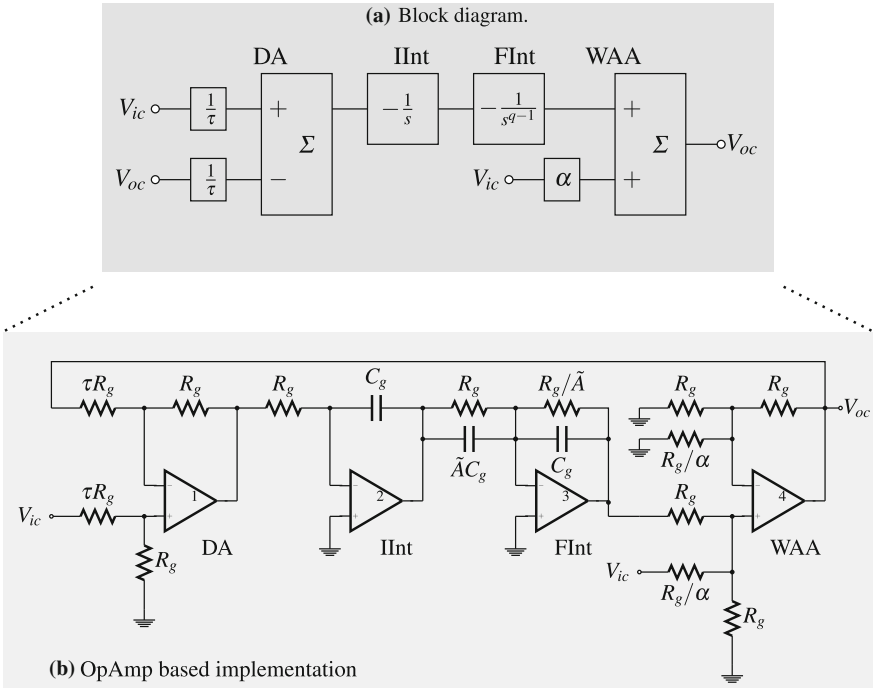


Fig. 5 Fractional-order phase-lead-lag compensator (case $1 < q < 2$)

$$\tilde{A} = \frac{1-(q-1)}{1+(q-1)} = \frac{2}{q} - 1 \tag{36}$$

Finally, to complete (35), the output of FInt is added to αV_{ic} by means of the block WAA, using $R_g/R_{h1} = 1$ and $R_g/R_{h2} = \alpha$.

4.3 Fractional-Order Phase-Lead-Lag Compensator **(0 < *q* < 1)**

For the case of fractional-order phase-lead-lag compensators with $0 < q < 1$, the block IInt of Fig. 5 must be omitted. Consequently, the block WAA must be changed by a block WDA to avoid a positive feedback, with the output of the block FInt connected to the inverting input of the block WDA, resulting the implementation depicted at Fig. 6. In this circuit, the block DA is designed with $R_{g3} = \tau R_g$, the block WDA is realized with $R_{g1} = R_g/\alpha$ and $R_{g2} = R_g$, and A is calculated with (30).

Two alternative implementations for fractional-order phase-lead-lag networks with $0 < q < 1$ and with fewer active but more passive elements are presented below.

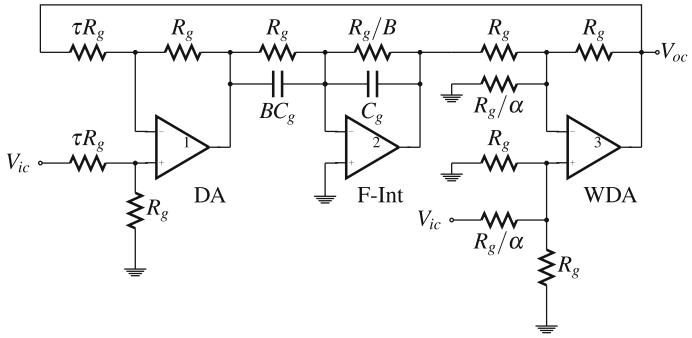


Fig. 6 Fractional-order phase-lead-lag compensator (case $0 < q < 1$)

4.4 Fractional-Order Phase-Lead-Lag Compensators $\mathbf{0 < q < 1}$ *(Cauer's Approximation)*

The circuit of Fig. 7a is a well known phase-lead configuration, but with a capacitor C substituted by a fractal capacitor with fractance $1/(s^q C)$. It can be easily demonstrated with nodal analysis that the transfer function of this circuit becomes

$$\frac{V_{oc}(s)}{V_{ic}(s)} = \frac{1 + R_{1ca} C s^q}{1 + \left(R_{1ca} || R_{2ca}\right) C s^q} = \frac{1 + \alpha \tau s^q}{1 + \tau s^q} \tag{37}$$

$$\tau = \left(R_{1ca} || R_{2ca}\right) C, \quad \alpha = 1 + \frac{R_{1ca}}{R_{2ca}} \tag{38}$$

and the fractal capacitor can be approximated with any of the methods mentioned in Sect. 2.4 (for a given n-th order of approximation) and, subsequently, implemented by Cauer networks by means of Continuous Fraction Expansion method.

Analogously, the circuit of Fig. 7b is a well known phase-lag configuration with the capacitor C substituted by a fractal capacitor with fractance $1/(s^q C)$. In this case the transfer function takes the form

$$\frac{V_{oc}(s)}{V_{ic}(s)} = \frac{1 + R_{2ca} C s^q}{1 + \left(R_{1ca} + R_{2ca}\right) C s^q} = \frac{1 + \alpha \tau s^q}{1 + \tau s^q} \tag{39}$$

$$\tau = \left(R_{1ca} + R_{2ca}\right) C, \quad \alpha = \frac{R_{2ca}}{R_{1ca} + R_{2ca}} \tag{40}$$

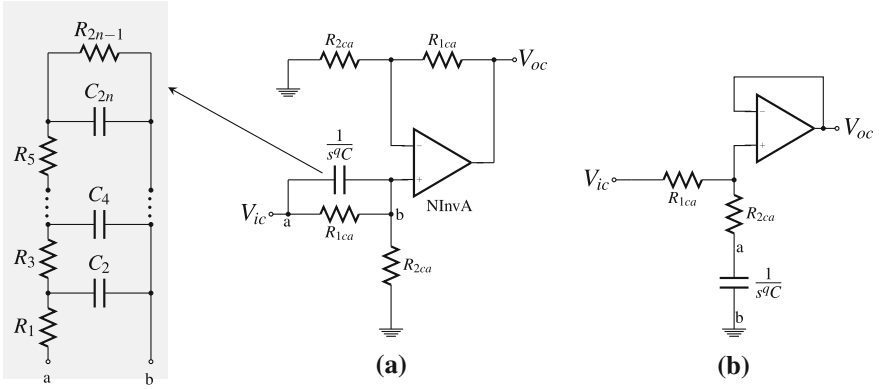


Fig. 7 Fractional-order compensators with $0 < q < 1$ and Cauer networks. **a** Phase-lead compensator. **b** Phase-lag compensator

5 Examples of Phase-Lead-Lag Compensated Systems Implemented with OpAmps

To validate the proposals of implementation of Sect. 4, this Section presents simulation or experimental results of systems that use the circuits in Figs. 4, 5, and 7 as compensators connected in series with an integer-order plant in unity-gain negative feedback configuration. Additionally, to explain the procedures described in Sect. 2.3 to design integer-order and fractional-order phase-lead-lag compensators, will be employed the system modeled by the following transfer function

$$G(s) = \frac{100K}{s(s+36)(s+100)} \tag{41}$$

This system has been considered as an academic example in [30, 44] for integer-order compensation, and in [35] for fractional-order compensation. Gains $K = 5839$ and $K = 1440$ have been employed in the lag and lead compensators, respectively, to satisfy steady-state error specifications. Figure 8 shows an OpAmp-based implementation of $G(s)$ by means of blocks IInv, LPA and IA. By equating the transfer function of this circuit with (41), results

$$\frac{\left(\frac{1}{R_{1p}C_g}\right)\left(\frac{1}{R_{1p}C_g}\right)}{s\left(s+\frac{1}{R_{2p}C_g}\right)\left(s+\frac{1}{R_{3p}C_g}\right)} = \frac{100K}{s(s+36)(s+100)} \tag{42}$$

and by choosing $1/(R_{2p}C_g) = 36, 1/(R_{3p}C_g) = 100, 1/(R_{1p}C_g) = 10\sqrt{K}, C_g = 1$ F and $R_g = 1\,\Omega$ are obtained: $R_{1p} = 1/\sqrt{100K}\,\Omega$, $R_{2p} = 0.0277\,\Omega$ and $R_{3p} = 0.01\,\Omega$.

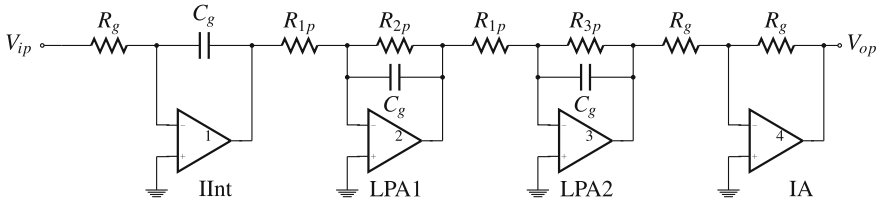


Fig. 8 Implementation of the plant $G(s)$ with OpAmps

Table 1 Design details of the plant $G(s)$

Block	Element	Theoretical value	Employed value (commercially available)
IInt	R_g	100 KΩ	100 KΩ
	C_g	10 nF	10 nF
LPA1	R_{1p}	130 Ω for $K = 5839$	120 Ω
		260 Ω for $K = 1440$	270 Ω
	R_{2p}	2.77 KΩ	2.7 KΩ
	C_g	10 nF	10 nF
LPA2	R_{1p}	130 Ω for $K = 5839$	120 Ω
		260 Ω for $K = 1440$	270 Ω
	R_{3p}	1 KΩ	1 KΩ
	C_g	10 nF	10 nF
IA	R_g	100 KΩ	100 KΩ

Then, impedance ($Z_m = 1E5$) and frequency ($\Omega_f = 1000$) denormalizations are carried out over this elements to obtain the values detailed in Table 1.

5.1 Example 1: Integer Order Phase-Lag Compensator ($K = 5839$)

Figure 9a shows the Bode diagram of $G(s)$ with $K = 5839$. As can be observed, the system presents a phase margin of 67° and a gain of 22.9 dB at the desired crossover frequency $\omega_c = 11$ rad/s. Assuming a required phase margin $PM = 62°$ to yield the desired transient response, a phase $p = -5°$ and a magnitude $M = -22.9$ dB must be provided by the phase-lag compensator to obtain a composite Bode diagram that goes through 0 dB at $\omega_c = 11$ rad/s. Therefore, using the procedure presented in Sect. 2.3 for integer-order compensators are calculated $c = 10^M/20 = 0.0711$ and $\delta = \tan(p) = -0.087$. Substituting these values of c and δ in (10) are obtained $\alpha = 0.0711$ and $\tau = 14.3472$, resulting the integer order phase-lag compensator

$$C(s) = \frac{1 + \alpha\tau s}{1 + \tau s} = \frac{1 + (0.0711)(14.3472)s}{1 + 14.3472s} \tag{43}$$

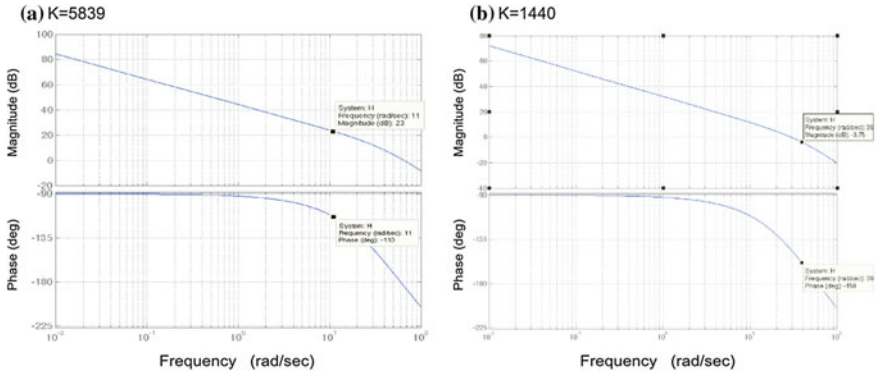


Fig. 9 Bode magnitude and phase plots of $G(s) = 100K/s(s + 36)(s + 100)$ with **a** $K = 5839$; **b** $K = 1440$

Table 2 Design details of the integer-order phase-lag compensator of Fig. 4 and Example 1 with $K = 5839$

Block	Element	Theoretical value	Employed value (commercially available)
L-L	R_{1c}	100 KΩ	100 KΩ
	R_{2c}	1.43 MΩ	1.5 MΩ
	C_g	10 nF	10 nF
InvA	R_{1c}	100 KΩ	100 KΩ
	R_{2c}	1.43 MΩ	1.5 MΩ

Additionally, it can be verified that with $\delta = -0.087$ and $c = 0.0711$ the condition (9) is satisfied, guarantying the existence of the compensator, which is implemented with the circuit of Fig. 4. Therefore, by choosing $C_g = 1$ and $\alpha = 0.0711$ in (32) are obtained $R_{2c} = 14.34\,\Omega$ and $R_{1c} = 1.02\,\Omega$. Then, impedance ($Z_m = 1E5$) and frequency ($\Omega_f = 1000$) denormalizations are carried out to obtain the values of elements detailed in Table 2.

The system in Fig. 8 in the unity negative feedback structure with the lag-phase compensator of Fig. 4 was simulated using HSPICE and the model of the OpAmp uA741. The details of design are listed in Tables 1 and 2. Figure 10 shows the results for an step-input of 1 V and frequency 166.6 Hz. The resulted overshoot was 9.7% with a peak time 258.4 μs. This overshoot corresponds to a second order system with phase margin $PM = 58.93°$ and damping factor $\zeta = 0.596$. These results show a good agreement with the results given in [44] (PM = 62°, $\zeta = 0.591$, overshoot = 10%) and [30] (overshoot = 9.8%, denormalized peak time = 260 μs), validating the proposal of implementation.

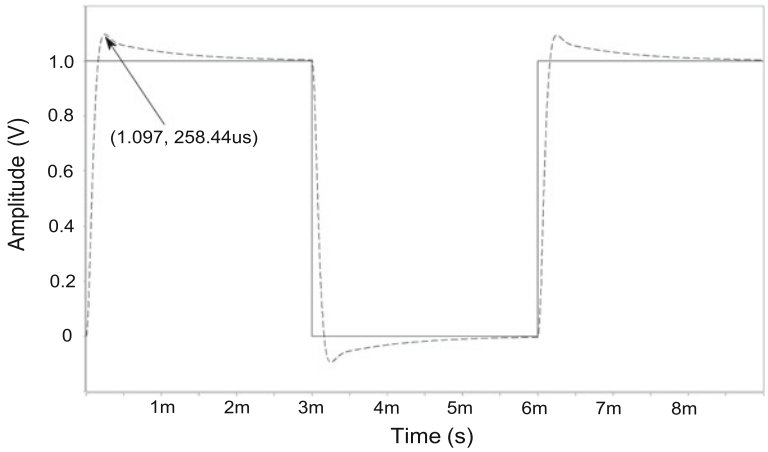


Fig. 10 Time-domain simulation results of the integer-order phase-lag compensator $C(s) = [1 + (0.0711)(14.3472)s]/[1 + 14.3472s]$ realized with the circuit of Fig. 4 with design details of Table 2, in unity negative feedback configuration, in which the plant $G(s) = 583900/[s(s + 36)(s + 100)]$ is implemented with the circuit of Fig. 8 with the design details of Table 1. Denormalizations in impedance and frequency $Z_m = 1E5$ and $\Omega_f = 1000$ were also performed

5.2 *Example 2: Integer Order Phase-Lead Compensator (K = 1440)*

Figure 9b shows the Bode diagram of $G(s)$ with $K = 1440$. The phase margin and gain of the system at the expected crossover frequency $\omega_c = 39$ rad/s are $PM = 180°–159° = 21°$ and $M = -3.7668$ dB, respectively. Consider a required phase margin $PM = 45.5°$ to yield the desired transient response. Consequently, the phase-lead compensator must provide a phase of $p = 24.5°$ and a gain of $M = 3.7668$ dB to yield the desired transient response with a Bode diagram that goes through 0 dB at $\omega_c = 39$ rad/s. By means of the procedure presented in Sect. 2.3, for integer-order compensators, are calculated: $c = 10^M/20 = 1.5429$ and $\delta = \tan(p) = 0.4473$. Substituting these values of c and δ in (10) results $\alpha = 2.3799$ and $\tau = 0.0166$. The corresponding integer-order phase-lead compensator becomes

$$C(s) = \frac{1 + \alpha\tau s}{1 + \tau s} = \frac{1 + (2.3799)(0.0166)s}{1 + 0.0166s} = 2.3795\left(\frac{s + 25.31}{s + 60.24}\right) \tag{44}$$

and the existence of this phase-lead compensator is guaranteed because of with $\delta = 0.4473$ and $c = 1.54$ the condition (8) is satisfied. To proceed with the implementation it is employed the circuit of Fig. 4. By selecting $C_g = 1$ F and $\alpha = 2.3799$ in (32) are obtained $R_{2c} = 0.0166\,\Omega$ and $R_{1c} = 0.0395\,\Omega$. Then, impedance ($Z_m = 1E5$) and frequency ($\Omega_f = 1000$) denormalizations are carried out to obtain the details of design summarized in Table 3.

The system in Fig. 8 in the unity negative feedback structure with the integer-order phase-lead compensator of Fig. 4 was simulated using HSPICE and the model of the OpAmp uA741. The details of design are listed in Tables 1 and 3. Figure 11 shows the results for an step-input of 1 V and frequency 166.6 Hz. The resulted overshoot was 18.2% with a peak time 77.5 μs. This overshoot corresponds to a second order system with phase margin 49.9° (compared with the theoretical value of 45.5°) and damping factor $\zeta = 0.476$. These results show a good agreement with the results given in [44] (PM = 45.5°, $\zeta = 0.427$, overshoot = 22.6%) and [30] (overshoot = 22.6%, denormalized peak time = 72 μs), validating the implementation.

Table 3 Design details of the integer-order phase-lead compensator of Fig. 4 and Example 2 with $K = 1440$

Block	Element	Theoretical value	Employed value (commercially available)
L-L	R_{1c}	3.95 KΩ	3.9 KΩ
	R_{2c}	1.66 KΩ	1.2 KΩ + 470 Ω
	C_g	10 nF	10 nF
InvA	R_{1c}	3.95 KΩ	3.9 KΩ
	R_{2c}	1.66 KΩ	1.2 KΩ + 470 Ω

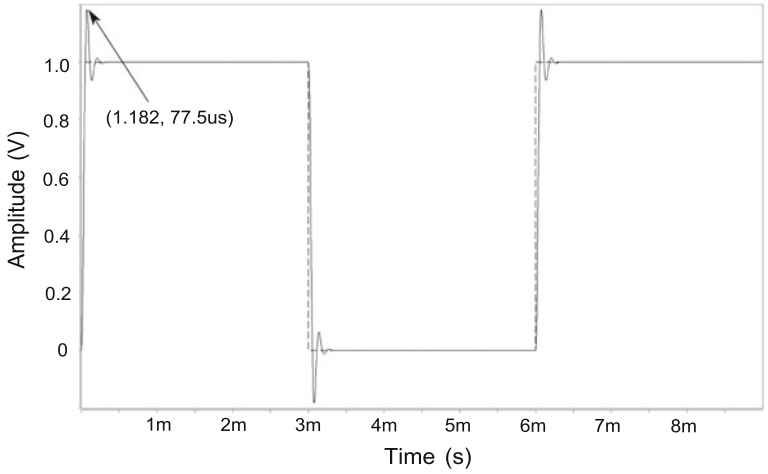


Fig. 11 Time-domain simulation results of the phase-lead compensator $C(s) = [1 + (2.3799)(0.0166)s]/[1 + 0.0166s]$ realized with the circuit of Fig. 4 with design details of Table 3, in unity negative feedback configuration, in which the plant $G(s) = 144000/[s(s + 36)(s + 100)]$ is implemented with the circuit of Fig. 8 with the design details of Table 1. Denormalizations in impedance and frequency $Z_m = 1E5$ and $\Omega_f = 1000$ were also performed

5.3 Example 3: Fractional-Order Phase-Lead Compensator ($1 < q < 2$)

Consider the system $G(s)$ given by (41) with $K = 1440$. As was explained in Example 2, a desired phase margin 45.5° with a gain cross-frequency of 39 rad/s correspond to $M = 3.76$ dB, $c = 1.5429, p = 24.1$ and $\delta = 0.4473$. Using the procedure described in Sect. 2.3 for fractional-order compensators and according to (16), this goal is achievable by means of a fractional-order phase-lead compensator with $q \in (q^*, 2) = (0.6338, 2)$. By taking advantage of the additional grade of liberty it can be obtained the exact value of q by establishing a desired value of the initial peak of the control signal, i.e., by using an actuator constraint. For instance, assuming a desired initial peak of the control signal of $u_0 = 2500$ and according to (20) and (15) it is obtained $q = 1.33$. Substituting this value in (14) and (15) the resulting fractional-order phase-lead compensator is expressed by

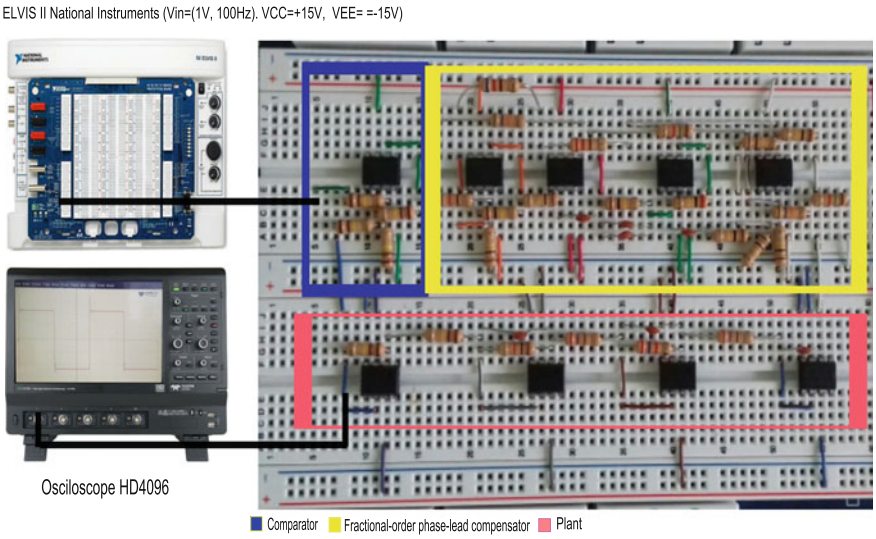
$$C(s) = \frac{1 + \alpha\tau s^q}{1 + \tau s^q} = \frac{1 + (1.736)\left(8.1395 \times 10^{-3}\right) s^{1.33}}{1 + 8.1395 \times 10^{-3} s^{1.33}} \tag{45}$$

This fractional-order phase-lead compensator satisfies the condition (12) with $\delta = 0.4557$ and $c = 1.5429$. The implementation is performed with the circuit of Fig. 5 selecting $R_g = 1\,\Omega, \alpha = 1.736, \tau = 8.1395 \times 10^{-3}$ and $\tilde{q} = q - 1 = 0.33$. This way, the following results are obtained: $\tilde{A} = (1 - \tilde{q})/(1 + \tilde{q}) = 0.5037, \tau R_g = 8.1395 \times 10^{-3}\,\Omega, R_g/\tilde{A} = 1.9853\,\Omega, \tilde{A}/R_g = 0.5037$ F and $R_g/\alpha = 0.576\,\Omega$. Then, impedance ($Z_m = 1$E5) and frequency ($\Omega_f = 1000$) denormalizations are carried out to obtain the details of design summarized in Table 4.

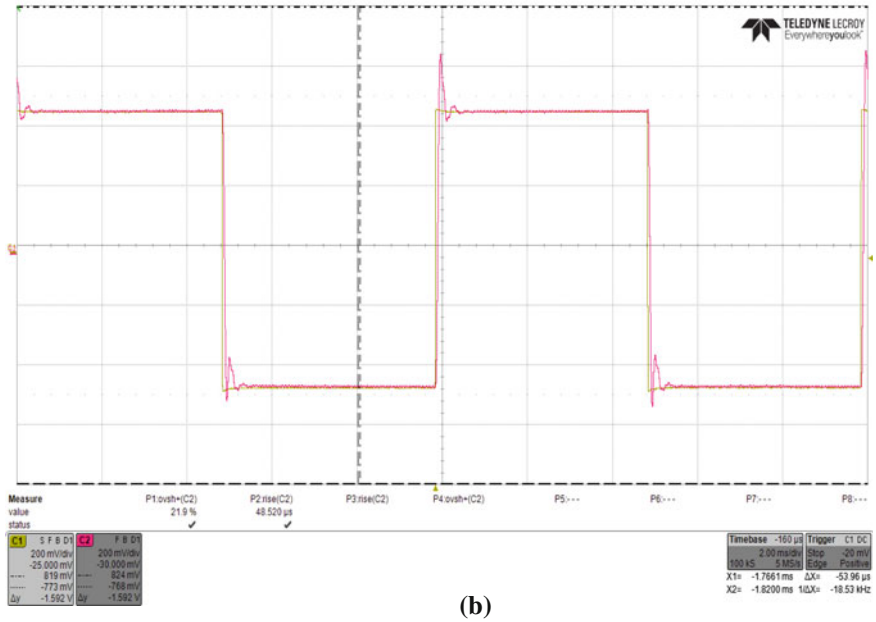
The system in Fig. 8 in the unity negative feedback structure with the fractional-order lead-phase compensator of Fig. 5 was implemented on protoboard with OpAmps uA741 and the details of design listed in Tables 1 and 4. The experimental

Table 4 Design details of the fractional-order phase-lead compensator of Fig. 4 and Example 3 with $K = 1440$

Block	Element	Theoretical value	Employed value (commercially available)
DA	R_g	100 KΩ	100 KΩ
	τR_g	813.9 Ω	820 Ω
IInt	R_g	100 KΩ	100 KΩ
	C_g	10 nF	10 nF
L-L	R_g	100 KΩ	100 KΩ
	$R_g/\tilde{A}$	200 KΩ	200 KΩ
	$\tilde{A}C_g$	5 nF	5 nF
	C_g	10 nF	10 nF
WAA	R_g	100 KΩ	100 KΩ
	R_g/α	57.6 KΩ	47 KΩ + 10 KΩ



(a)



(b)

Fig. 12 **a** Experimental setup of the fractional-order phase-lead compensator $C(s) = [1 + (1.736)(8.1395 \times 10^{-3})s^{1.33}]/[1 + 8.1395 \times 10^{-3}s^{1.33}]$ realized with the circuit of Fig. 5 in unity negative feedback configuration with plant $G(s) = 144000/[s(s + 36)(s + 100)]$ implemented with the circuit of Fig. 8. **b** Time-domain experimental results

setup is shown in Fig. 12a. It consists of an input square signal of 1 V in amplitude, offset = 0.5 V, and frequency of 100 Hz, supplied from the experimental platform ELVIS II from National Instruments. This device also provides bias voltages of ±15 V to the OpAmps. Figure 12b shows the measured time response. The output was measured with an Oscilloscope HD4096 Teledyne Lecroy. The resulted overshoot was 21.9%. This overshoot corresponds to a second order system with phase margin 46.32° and damping factor $\zeta = 0.435$. It can be noted that the theoretical (overshoot = 22.7%, $\zeta = 0.426$, PM = 45.5°), the simulation (overshoot = 21.13%, $\zeta = 0.4434$, PM = 47.05°), the experimental results (overshoot = 21.9%, $\zeta = 0.435$, PM = 46.32°) and the results reported in Fig. 7 of [35] are in good agreement, thus validating the proposal of implementation.

5.4 *Example 4: Fractional-Order Phase-Lead Compensator with* $0 < q < 1$ *and Cauer Approximation*

With an unconstrained initial peak of the control signal, the value of q in Example 3 may be any in the range $(q^*, 2) = (0.6338, 2)$. Consider $q = 0.7$. Substituting this value in (14) and (15) the fractional-order phase-lead compensator becomes

$$C(s) = \frac{1 + \alpha\tau s^q}{1 + \tau s^q} = \frac{1 + (7.442)\left(9.5243 \times 10^{-3}\right) s^{0.7}}{1 + 9.5243 \times 10^{-3} s^{0.7}} \tag{46}$$

and this compensator satisfies the condition (12) with $\delta = 0.4557$ and $c = 1.5429$. In this case, the circuit implementation can be performed with the circuit of Fig. 6. However, this implementation is similar to the presented in Example 3. Instead, in this example will be explored the realization with network approximation by means of the Cauer method. Then, consider the circuit implementation of Fig. 7. With $q = 0.7, C = 1$ and a fourth-order approximation of the impedance $1/s^q$ is obtained [23]

$$\begin{aligned} \frac{1}{s^q} &= \frac{Q_0 s^4 + Q_1 s^3 + Q_2 s^2 + Q_3 s + Q_4}{Q_4 s^4 + Q_3 s^3 + Q_2 s^2 + Q_1 s + Q_0} \\ &= \frac{0.037 s^4 + 2.324 * s^3 + 9.921 s^2 + 7.8 s + 1}{s^4 + 7.8 s^3 + 9.92 s^2 + 2.324 s + 0.037} \end{aligned} \tag{47}$$

where

$$\begin{aligned} Q_0 &= q^4 - 10q^3 + 35q^2 - 50q + 24 \\ Q_1 &= -4q^4 + 20q^3 + 40q^2 - 320q + 384 \\ Q_2 &= 6q^4 - 150q^2 + 864 \\ Q_3 &= 4q^4 - 10q^3 + 40q^2 + 320q + 384 \\ Q_4 &= q^4 + 10q^3 + 35q^2 + 50q + 24 \end{aligned} \tag{48}$$

Alternatively, the approximation of $1/s^q$ can be obtained by other methods of approximation, such as Crone, Carlson or Matsuda, employing the Ninteger tool box of MATLAB [26]. Moreover, the synthesis of the fractance (47) can be obtained with the repeated division process of terms described in Sect. 2.4 (Continued Fraction Expansion) by means of the tool box FOMCON of MATLAB and the following code [26, 37]

$$\gg a1 = [1 \;\; 7.807 \;\; 9.921 \;\; 2.323 \;\; 0.037];$$
$$\gg b1 = [0.037 \;\; 2.3239 \;\; 9.921 \;\; 7.807 \;\; 1];$$
$$\gg [q, expr] = polycfe(b1, a1)$$

resulting

$$\frac{1}{s^{0.7}} = R_1 + \cfrac{1}{sC_2 + \cfrac{1}{R_3 + \cfrac{1}{sC_4 + \cfrac{1}{R_5 + \cfrac{1}{sC_6 + \cfrac{1}{R_7 + \cfrac{1}{sC_8 + \cfrac{1}{R_9}}}}}}}} \tag{49}$$

The values of $R_1, C_2, R_3, C_4, R_5, C_6, R_7, C_8$ and R_9 are shown in Table 5. Impedance ($Z = 1\text{E}5$) and frequency ($\Omega = 1000$) denormalizations were carried out. Finally, using $\alpha = 7.442, C = 1$ and $\tau = 9.5243 \times 10^{-3}$ are solved simultaneously both equations in (38) to obtain $R_{1ca} = 0.07088\,\Omega$ and $R_{2ca} = 0.011\,\Omega$. Again by using the impedance denormalization $Z = 1\text{E}5$ over these elements are obtained the values indicated in Table 5.

The system in Fig. 8 in the unity negative feedback structure with the fractional-order lead-phase compensator with Cauer network approximation of Fig. 7 was simulated using HSPICE and the model of the OpAmp uA741. The details of design

Table 5 Design details of the fractional-order phase-lead compensator of Fig. 7 and Example 4 with $q < 1$ and $K = 1440$

Element	Value	Element	Value
R_1	3.7 KΩ	R_7	534 KΩ
C_2	4.9 nF	C_8	9.8 nF
R_3	65.38 KΩ	R_9	1.87 MΩ
C_4	5.6 nF	R_{1ca}	7 KΩ
R_5	224.8 KΩ	R_{2ca}	1.12 KΩ
C_6	6.8 nF		

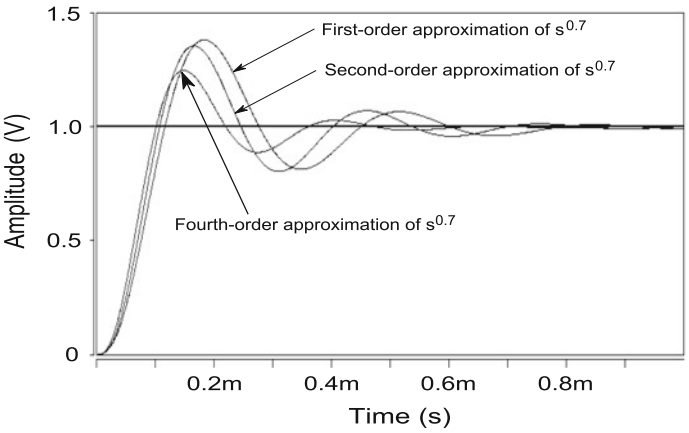


Fig. 13 Time-domain simulation results of the fractional-order phase-lead compensator $C(s) = [1 + (7.442)(9.5243 \times 10^{-3})s^{0.7}]/[1 + 9.5243 \times 10^{-3}s^{0.7}]$ realized with the circuit of Fig. 7 with design details of Table 5, in unity negative feedback configuration, in which the plant $G(s) = 144000/[s(s + 36)(s + 100)]$ is implemented with the circuit of Fig. 8 with the design details of Table 1. Denormalizations in impedance and frequency $Z = 1E5$ and $\Omega = 1000$ were also performed

are listed in Tables 1 and 5. Figure 13 shows the results for an step-input of 1 V, offset 0.5 V and frequency 100 Hz. The resulted overshoot was 25% with a peak time 75.3 μs. This overshoot corresponds to a second order system with phase margin 43.46° and damping factor $\zeta = 0.4037$. These results show a good agreement with the results given in Example 3 and in Fig. 6 of [35], validating the implementation. However, in Fig. 13 it can also be observed that the network approximation is not appropriate in this case when the order of the approximation is less than 4. It is due to the limited bandwidth where the approximation is valid.

6 Phase-Lead Compensated Systems Implemented with FPAA

In this section is illustrated, starting from the designs of Examples 2 and 3, the implementation and experimental validation of integer-order and fractional-order phase-lead compensators by means of FPAAs, which are processors for analog signals, equivalents to the digital processors FPGAs (Field Programmable Gate Arrays). FPAAs are devices of specific purpose with the characteristics of being reconfigurable electrically. They are used to implement a variety of analog functions, such as: integration, derivation, weighted sum/subtraction, filtering, rectification, comparator, multiplication, division, analog-digital conversion, voltage references, signal conditioning, amplification, nonlinear functions, generation of arbitrary signals, among others. Since FPAAs are reconfigurable, one can implement complex

prototypes in a short time. In this work the FPAA AN231E04 from Anadigm [1], is used. It uses technology of switched capacitors and it is organized into four configurable analog blocks (CABs). Those CABs are distributed in a matrix of size 2×2, supported by resources of programmable interconnections, seven configurable analog cells of input-output with active elements for amplification and dynamic reduction of offset and noise, an on-chip generator of multiple non-overlapped clock-signals and internal voltage references to eliminate temperature effects. It also includes a look-up table (LTU) of 8×256 bits for function synthesis and nonlinear signals, and for analog-digital conversion. The configuration data is saved into an internal SRAM, which allows reprogramming the device without interrupting its operation. The circuits are designed using the software Anadigmdesigner2, in which the user has access to a library of functional circuits CAMs (Configurable Analog Modules). Those CAMs are mapped in a portion for each CAB. The CABs have matrices of switches and capacitors, two OpAmps, a comparator, and digital logic for programming.

6.1 Example 5: FPAA Implementation of the Integer-Order Phase-Lead Compensator of Example 2

Figure 14a shows an implementation, using the FPAA AN231E04, equivalent to the closed-loop system designed in Example 2. The corresponding experimental setup is illustrated in the same figure. Details of the design and the corresponding transfer functions of every employed building block are listed in Table 6. The comparator producing the signal error $e(t) = V_{in}(t) - V_{out}(t)$ is realized using a CAM "SumDiff" (adder-subtractor) with gains 1 and -1 at each input. The integer order lead controller (44) is implemented by CAM "FilterBilinear 1" (Bilinear filter), designed to produce a transfer function with DC gain 2.3795, and one pole ($\omega_p = 60.24$ rad/s) and one zero ($\omega_z = 25.31$ rad/s), both denormalized by a factor $\Omega_f = 1000$ ($f_p = 9.57$ kHz, $f_z = 4.02$ kHz).

On the other hand, the plant (41) with $K = 1440$ is modeled by two low-pass filters $H_2(s) = -36/(s + 36)$ and $H_3(s) = -100/(s + 100)$ (CAM "Bilinear Filter 2" and CAM "Bilinear Filter 3", respectively), and by an "integrator" CAM, $H_1(s) = -40/s$, in series with a block of gain -1 (CAM "GainInv1"). The frequency denormalization $\Omega_f = 1000$ was realized by substituting in each block s by s/Ω_f.

The experimental configuration of Fig. 14a has a differential input of 0.5 V in amplitude and frequency 500 Hz, and a common-mode component of 1.5 V. It is provided by the array of three OpAmps and the target ELVIS II from National Instruments. This device also provides bias voltages of ± 15 V to the OpAmps. The output is converted from differential mode to simple mode with a differential amplifier. The output is measured with an Oscilloscope HD4096 Teledyne Lecroy (see Fig. 14b). The resulted overshoot was 21.1%. This overshoot corre-

Table 6 Details of the design in FPAA of the closed-loop system conformed by the plant (41) and the integer-order phase-lead controller (44) with $\Omega_f = 1000$

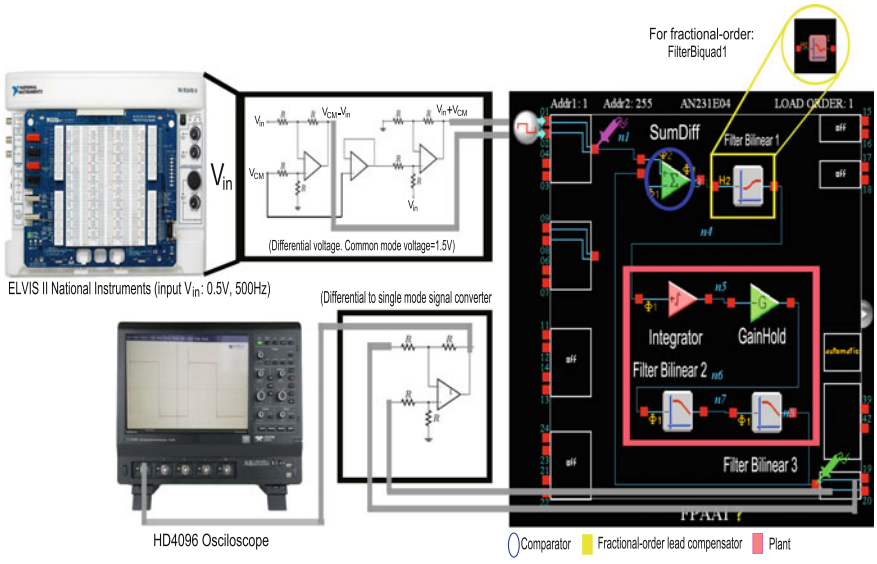
Operation	CAM	Transfer function	Characteristics
Comparator	SumDiff (Sum/difference)	$V_o = V_{in} - V_{out}$	$G_1 = 1$ $G_2 = -1$
Lead controller	Filter bilinear 1 (pole-zero filter)	$-G\left(\frac{1+s/\omega_z}{1+s/\omega_p}\right)$	$G = 1$ $f_p = \frac{\omega_p \Omega_f}{2\pi} = \frac{(60.24)(1000)}{2\pi} =$ 9.57 kHz $f_z = \frac{\omega_z \Omega_f}{2\pi} = \frac{(25.31)(1000)}{2\pi} =$ 4.02 kHz
Plant	Filter bilinear 2 (lowpass filter)	$-G\left(\frac{\omega_p}{s+\omega_p}\right)$	$G = 1$ $f_p = \frac{\omega_p \Omega_f}{2\pi} = \frac{(36)(1000)}{2\pi} =$ 5.74 kHz
	Filter bilinear 3 (lowpass filter)	$-G\left(\frac{\omega_p}{s+\omega_p}\right)$	$G = 1$ $f_p = \frac{\omega_p \Omega_f}{2\pi} = \frac{(100)(1000)}{2\pi} =$ 15.9 kHz
	Integrator	$\frac{K_{int}}{s}$	$K_{int} * \Omega_f = 40 * 1000 =$ $40000 = 0.04/\mu s$
	GainHold (Inverter amplifier)	$-G$	$G = 1$

G_i: gain of the CAM. f: corner frequency of the CAM. K_{int}: integration constant of the CAM

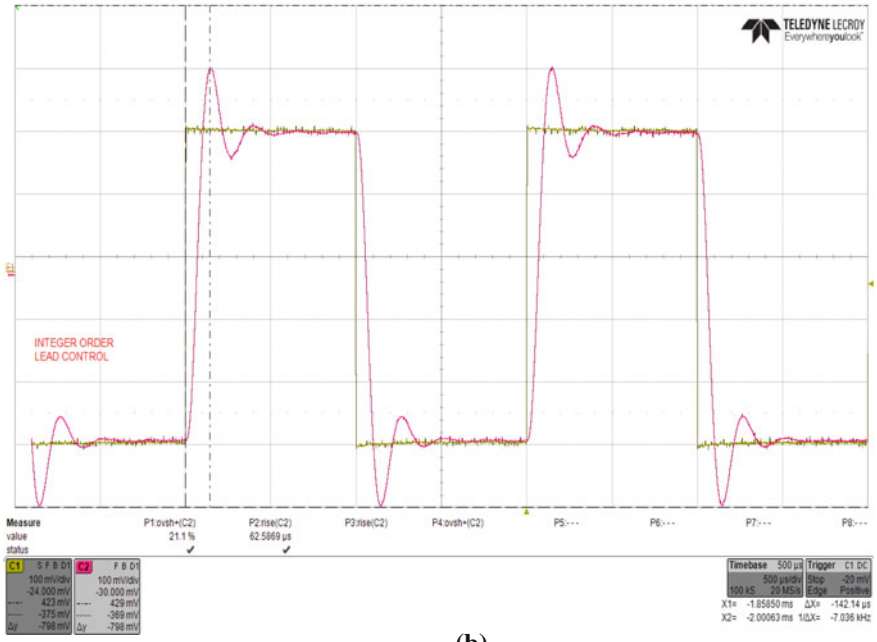
sponds to a second order system with phase margin 47° (compared with the theoretical value of 45.5°) and damping factor $\zeta = 0.443$. The simulation results of Example 2 and the experimental results of the system of Fig. 14a are in good agreement, thus validating this proposal of implementation.

6.2 *Example 6: FPAA Implementation of the Fractional-Order Phase-Lead Compensator of Example 3*

Consider the fractional-order phase-lead compensator with $q = 1.33$ presented in Example 3 (see (45)). This controller can be reformulated by using a first-order approximation of the fractional derivator $s^{\tilde{q}} = (Bs + 1)/(s + B)$, with $0 < \tilde{q} < 1$, resulting



(a)



(b)

Fig. 14 **a** Experimental setup of the integer-order phase-lead compensator $C(s) = [1 + (2.3799)(0.0166)s]/[1 + 0.0166s]$ realized with an FPAA, in unity negative feedback configuration, with plant $G(s) = 144000/[s(s + 36)(s + 100)]$ also implemented in the FPAA. A denormalization in frequency $\Omega_f = 1000$ was performed. **b** Time-domain experimental results

$$C(s) = \frac{1+\alpha\tau s^{q}}{1+\tau s^{q}} = \frac{1+\alpha\tau s^{1+\tilde{q}}}{1+\tau s^{1+\tilde{q}}} = \frac{1+\alpha\tau s\left(\dfrac{Bs+1}{s+B}\right)}{1+\tau s\left(\dfrac{Bs+1}{s+B}\right)}$$
$$= \alpha\left(\frac{s^2+\dfrac{\omega_z}{Q_z}s+\omega_z^2}{s^2+\dfrac{\omega_p}{Q_p}s+\omega_p^2}\right) \tag{50}$$

where

$$\tilde{q} = q-1, \qquad s^{\tilde{q}} \approx \frac{Bs+1}{s+B}, \qquad B = \frac{1+\tilde{q}}{1-\tilde{q}} \tag{51}$$

and

Table 7 Details of the design in FPAA of the closed-loop system conformed by the plant (41) and the fractional-order lead controller (50) with $\alpha = 1.736$, $\tau = 8.1395 \times 10^{-3}$, $q = 1.33$ and $\Omega_f = 3000$

Operation	CAM	Transfer function	Characteristics
Comparator	SumDiff (Sum/Difference)	$V_o = V_{in} - V_{out}$	$G_1 = 1$ $G_2 = -1$
Lead controller	Filter biquad (pole-zero filter)	$G\left(\dfrac{s^2+\dfrac{\omega_z}{Q_z}s+\omega_z^2}{s^2+\dfrac{\omega_p}{Q_p}s+\omega_p^2}\right)$	$G = 1.736$ $f_p = \dfrac{\omega_p\Omega_f}{2\pi} = \dfrac{(11.084)(3000)}{2\pi} =$ 5.29 kHz $Q_p = 0.1776$ $f_z = \dfrac{\omega_z\Omega_f}{2\pi} = \dfrac{(8.4122)(3000)}{2\pi} =$ 4.016 kHz $Q_z = 0.2326$
Plant	Filter bilinear 2 (lowpass filter)	$-G\left(\dfrac{\omega_p}{s+\omega_p}\right)$	$G = 1$ $f_p = \dfrac{\omega_p\Omega_f}{2\pi} = \dfrac{(36)(3000)}{2\pi} =$ 17.22 kHz
	Filter bilinear 3 (lowpass filter)	$-G\left(\dfrac{\omega_p}{s+\omega_p}\right)$	$G = 1$ $f_p = \dfrac{\omega_p\Omega_f}{2\pi} = \dfrac{(100)(3000)}{2\pi} =$ 47.7 kHz
	Integrator	$\dfrac{K_{int}}{s}$	$K_{int} * \Omega_f = 40 * 3000 =$ $120000 = 0.12/\mu s$
	GainHold (Inverter amplifier)	$-G$	$G = 1$

G_i: gain of the CAM. f: corner frequency of the CAM. K_{int}: integration constant of the CAM

$$\omega_p = \frac{1}{\sqrt{\tau}}, \quad Q_p = \frac{\sqrt{\tau}B}{\tau+1}, \quad \omega_z = \frac{1}{\sqrt{\alpha\tau}}, \quad Q_z = \frac{\sqrt{\alpha\tau}B}{\alpha\tau+1} \tag{52}$$

This way, the fractional-order phase-lead compensator with $1 < q < 2$ can be realized by means of a biquad filter. Based on this idea, Fig. 14a shows the implementation in FPAA AN231E04 of the closed-loop controlled system designed in Example 3. Details of the design and the transfer functions of every building block are listed in Table 7. The comparator producing the signal error $e(t) = V_{in}(t) - V_{out}(t)$ is realized using a CAM "SumDiff" (adder-subtractor). The fractional-order lead controller (50) is implemented by CAM "FilterBiquad1" (Biquad filter, see Fig. 14a). The parameters of this block are calculated using (51) and (52) with $\alpha = 1.736$, $\alpha\tau = 1.4131 \times 10^{-2}$, $\tau = 8.1395 \times 10^{-3}$ and $\tilde{q} = 0.33$, been obtained: $\omega_p = 11.084$ rad/s, $\omega_z = 8.412$ rad/s, $Q_p = 0.1776$ and $Q_z = 0.2326$. Then, a frequency denormalization $\Omega_f = 3000$ is realized, resulting $f_p = 5.29$ kHz and $f_z = 4.02$ kHz. The same denormalization is performed in the plant, which is designed as in the Example 5 (see Fig. 14a). The design details are summarized in Table 7.

The experimental configuration is equal to the reported in Fig. 14a, but with the CAM "FilterBiquad1" instead of the CAM "FilterBilinear1". It has a differential input of 0.5 V in amplitude, offset 0.25 V and frequency 500 Hz, and a common-mode component of 1.5 V from the array of three OpAmps and target ELVIS II from National Instruments. This device also provides bias voltages of ±15V to the OpAmps. The output is converted from differential mode to simple mode with a

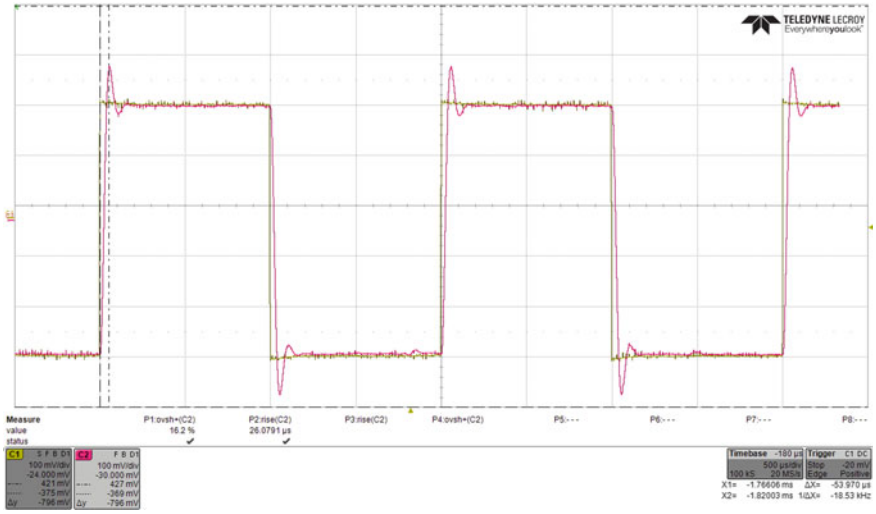


Fig. 15 Time-domain experimental result of the fractional-order phase-lead compensator $C(s) = [1 + (1.736)(8.1395 \times 10^{-3})s^{1.33}]/[1 + (8.1395 \times 10^{-3})s^{1.33}]$ realized with an FPAA, in unity negative feedback configuration, with plant $G(s) = 144000/[s(s + 36)(s + 100)]$ also implemented in the FPAA. A denormalization in frequency $\Omega_f = 3000$ was performed

differential amplifier. The output is measured with an Oscilloscope HD4096 Teledyne Lecroy (see Fig. 15). The resulted overshoot was 16.2%, compared with the 21.9% obtained with the implementation of Example 3. This overshoot corresponds to a second order system with phase margin 51.9° and damping factor $\zeta = 0.5$. The simulation results of Example 3 and the experimental results of Example 6 are similar, but with a difference of 5% regarding the overshoot. This difference is attributed to the different amplitudes and frequencies of the input signals (the FPAA has swing limits), the resolution of the programmable gains that can be implemented with the FPAA and the different denormalization frequencies.

7 Conclusion

The OPAMP-based and FPAA-based design of integer-order and fractional-order phase-lead-lag compensators for the case of $q \in (0, 1)$ and $q \in (1, 2)$, have been introduced. Each design was realized considering: (i) the parameters obtained with the procedures reported in [44] (integer-order) and [35] (fractional-order) when the gain and the phase required at a particular frequency are known for a desired time-domain response; (ii) Five configurations of compensators realized with basic OPAMP building blocks and (iii) Two more configurations (fractional and integer orders) with FPAAs. The OPAMP building blocks employed include inverter integrators, inverter and non-inverter amplifiers, differential amplifiers, weighted adders, first order low-pass filters, fractional-order phase-lead-lag ladders and fractional integrators. With all those blocks, the design equations were established taking care that some resistor and all capacitor values were chosen like degrees of freedom. Six design examples of both integer and fractional-order phase-lead-lag compensators were presented. In order to compare the performance of the different compensators, an integer-order plant was used. The compensation was made in series with the plant in a unity feedback loop. Simulation and experimental results agree with theory. An interesting result is the fact that the proposed solutions are good enough for the case of $q \in (1, 2)$ when the order of the approximation of s^q is one; however, those are not adequate when $q \in (0, 1)$. In those cases is necessary employ an approximation of higher order. It was evident with the third example that when the Cauer ladders are not employed, it is possible to synthesize realizations with commercial values of capacitors and resistors based on frequency and impedance transformations. Nevertheless, according with the fourth example, when $q \in (0, 1)$, the number of active elements can rise significantly since the approximation of the operator $s^{\pm\alpha}$ is required to be of high-order. In this case, the Cauer ladder solution might be an option despite of its inherent complexity for the computation of the commercial element values. To the author's knowledge, there very few (two) fractional-order phase lead-lag compensators reported in the literature. Therefore, the circuit solutions presented in this chapter offer useful alternatives that can be occupied for diverse controllers. Furthermore, some other applications such as memristors, filters and chaotic systems might benefit from the proposed strategies of implementation.

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References

1. AN231E04 Datasheet Rev 1.2. (2012). http://www.anadigm.com/an231e04.asp
2. Angel, L., & Viola, J. (2015). Design and statistical robustness analysis of FOPID, IOPID and SIMC PID controllers applied to a motor-generator system. *IEEE Latin America Transactions*, *13*(12), 3724–3734. doi:10.1109/TLA.2015.7404900.
3. Antoniou, A. (1972). Floating negative-impedance converters. *IEEE Transactions on Circuit Theory*, *19*(2), 209–212.
4. Azar, A. T., & Serrano, F. E. (2014). Robust IMC-PID tuning for cascade control systems with gain and phase margin specifications. *Neural Computing and Applications*, *25*(5), 983–995. doi:10.1007/s00521-014-1560-x.
5. Azar, A. T., & Serrano, F. E. (2015). Design and modeling of anti wind up PID controllers. In Q. Zhu, A. T. Azar (Eds.), *Complex system modelling and control through intelligent soft computations*. Germany: Springer. doi:10.1007/978-3-319-12883-21.
6. Azar, A. T., & Serrano, F. E. (2016). Stabilization of mechanical systems with backlash by PI loop shaping. *International Journal of System Dynamics Applications*, *5*(3), 20–47.
7. Azar, A. T., & Vaidyanathan, S. (2015). *Chaos modeling and control systems design* (Vol. 581). Studies in computational intelligence. Germany: Springer.
8. Azar, A. T., & Vaidyanathan, S. (2015). *Computational intelligence applications in modeling and control* (Vol. 575). Studies in computational intelligence. Germany: Springer. ISBN 978-3-319-11016-5.
9. Azar, A. T., & Vaidyanathan, S. (2015c). *Handbook of research on advanced intelligent control engineering and automation*. Advances in computational intelligence and robotics (ACIR) book series. USA: IGI Global. ISBN 978-1-466-67248-2.
10. Azar, A. T., & Vaidyanathan, S. (2016). *Advances in chaos theory and intelligent control*. Studies in fuzziness and soft computing. Germany: Springer.
11. Biswas, K., Sen, S., & Dutta, P. K. (2006). Realization of a constant phase element and its performance study in a differentiator circuit. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *53*(9), 802–806. doi:10.1109/TCSII.2006.879102.
12. Boulkroune, A., Bouzeriba, A., Bouden, T., & Azar, A. T. (2016). Fuzzy adaptive synchronization of uncertain fractional-order chaotic systems. *Advances in chaos theory and intelligent control* (Vol. 337). Studies in fuzziness and soft computing. Germany: Springer.
13. Boulkroune, A., Hamel, S., & Azar, A. T. (2016). Fuzzy control-based function synchronization of unknown chaotic systems with dead-zone input. In *Advances in chaos theory and intelligent control* (Vol. 337). Studies in fuzziness and soft computing. Germany: Springer.
14. Cao, J., Liang, J., & Cao, B. (2005). Optimization of fractional order PID controllers based on genetic algorithms. In *2005 International Conference on Machine Learning and Cybernetics* (Vol. 9, pp. 5686–5689). doi:10.1109/ICMLC.2005.1527950.
15. Charef, A. (2006). Analogue realization of fractional-order integrator, differentiator and fractional $PI^{\lambda}D^{\mu}$ controller. *IEE Proceedings—Control Theory and Applications*, *153*(6), 714–720.
16. Chen, Y., Petras, I., & Xue, D. (2009). Fractional order control—a tutorial. In *2009 American Control Conference* (pp. 1397–1411). doi:10.1109/ACC.2009.5160719.
17. Deepak, V. D., & Kumari, U. S. (2014). Modified method of tuning for fractional PID controllers. In *2014 International Conference on Power Signals Control and Computations, EPSCICON 2014* (pp. 8–10). doi:10.1109/EPSCICON.2014.6887481.

18. Dobra, P., Trusca, M., & Duma, R. (2012). Embedded application of fractional order control. *Electronics Letters*, *48*(24), 1526–1528. doi:10.1049/el.2012.1829.
19. Dorcák, L., Terpák, J., Petrá, I., Valsa, J., & González, E. (2012). Comparison of the electronic realization of the fractional-order system and its model. In *Carpathian Control Conference (ICCC), 2012 13th International* (pp. 119–124). doi:10.1109/CarpathianCC.2012.6228627.
20. Herrmann, R. (2011). *Fractional calculus* (1st ed.). World Scientific publishing Co.
21. Jesus, I. S., & Tenreiro, J. A. (2009). Development of fractional order capacitors based on electrolyte processes. *Nonlinear Dynamics*, *56*(1–2), 45–55. doi:10.1007/s11071-008-9377-8.
22. Khubalkar, S., Chopade, A., Junghare, A., Aware, M., & Das, S. (2016). Design and realization of stand-alone digital fractional order PID controller for buck converter fed DC motor. *Circuits, Systems, and Signal Processing*, *35*(6), 2189–2211. doi:10.1007/s00034-016-0262-2.
23. Krishna, B. T. (2011). Studies on fractional order differentiators and integrators: A survey. *Signal Processing*, *91*(3), 386–426. doi:10.1016/j.sigpro.2010.06.022.
24. Lachhab, N., Svaricek, F., Wobbe, F., & Rabba, H. (2013). Fractional order PID controller (FOPID)-toolbox. In *Control Conference (ECC), 2013 European* (pp. 3694–3699).
25. Ltifi, A., Ghariani, M., & Neji, R. (2013). Performance comparison on three parameter determination method of fractional PID controllers. In *2013 14th International Conference on Sciences and Techniques of Automatic Control and Computer Engineering (STA)* (pp. 453–460). doi:10.1109/STA.2013.6783171.
26. Mahmood, A. K., & Saleh, S. A. R. (2015). Realization of fractional order differentiator by analogue electronic circuit. *International Journal of Advances in Engineering and Technology*, *1*, 1939–1951.
27. Marzaki, M. H., Rahiman, M. H. F., Adnan, R., & Tajjudin, M. (2015). Real time performance comparison between PID and fractional order PID controller in SMISD plant. In *2015 IEEE 6th Control and System Graduate Research Colloquium (ICSGRC)* (pp. 141–145). doi:10.1109/ICSGRC.2015.7412481.
28. Mehta, S., & Jain, M. (2015). Comparative analysis of different fractional PID tuning methods for the first order system. In *2015 International Conference on Futuristic Trends on Computational Analysis and Knowledge Management (ABLAZE)* (pp. 640–646). doi:10.1109/ABLAZE.2015.7154942.
29. Monje, C. A., Chen, Y., Vinagre, B. M., Xue, D., & Feliu-Batlle, V. (2010). *Fractional-order systems and controls, fundamentals and applications* (1st ed.). Advances in industrial control. Springer.
30. Nise, N. S. (2011). *Control systems engineering* (6th ed.). Wiley. ISBN 978-0-470-91373-4.
31. Ou, B., Song, L., & Chang, C. (2010). Tuning of fractional PID controllers by using radial basis function neural networks. In *2010 8th IEEE International Conference on Control and Automation (ICCA)* (pp. 1239–1244). doi:10.1109/ICCA.2010.5524367.
32. Podlubny, I. (1999). Fractional-order systems and $PI^{\lambda}D^{\mu}$-controllers. *IEEE Transactions on Automatic Control*, *44*(1), 208–214. doi:10.1109/9.739144.
33. Podlubny, I., Petras, I., Vinagre, B. M., O'Leary, P., & Dorcak, L. (2002). Analogue realizations of fractional-order controllers. *Nonlinear Dynamics*, *29*(1), 281–296.
34. Raynaud, H. F., & Zergainoh, A. (2000). Brief state-space representation for fractional order controllers. *Automatica*, *36*(7), 1017–1021. doi:10.1016/S0005-1098(00)00011-X.
35. Tavazoei, M. S., & Tavakoli-Kakhki, M. (2014). Compensation by fractional-order phase-lead/lag compensators. *IET Control Theory and Applications*, *8*(5), 319–329. doi:10.1049/iet-cta.2013.0138.
36. Tepljakov, A., Petlenkov, E., & Belikov, J. (2011). FOMCON: Fractional-order modeling and control toolbox for MATLAB. In *Mixed Design of Integrated Circuits and Systems (MIXDES), 2011 Proceedings of the 18th International Conference* (pp. 684–689).
37. Tepljakov, A., Petlenkov, E., & Belikov, J. (2011). FOMCON: Fractional-order modeling and control toolbox for MATLAB. In *Proceedings of the 18th International Conference Mixed Design of Integrated Circuits and Systems—MIXDES 2011* (Vol. 4, pp. 684–689).

38. Tepljakov, A., Petlenkov, E., & Belikov, J. (2012). A flexible MATLAB tool for optimal fractional-order PID controller design subject to specifications. In *Control Conference (CCC), 2012 31st Chinese* (pp. 4698–4703).
39. Truong, V., & Moonyong, L. (2013). Analytical design of fractional-order proportional-integral controllers for time-delay processes. *ISA Transactions*, *52*(5), 583–591. doi:10.1016/j.isatra.2013.06.003.
40. Valerio, D., & da Costa, J. (2006). Tuning of fractional PID controllers with Ziegler Nichols-type rules. *Signal Processing*, *86*(10), 2771–2784. doi:10.1016/j.sigpro.2006.02.020.
41. Valerio, D., & Da Costa, J. S. (2006). Tuning-rules for fractional PID controllers. In *Proceedings of the 2nd IFAC Workshop on Fractional Differentiation and its Applications FDA06, Porto, Portugal*.
42. Valerio, D., & Da Costa, J. S. (2010). A review of tuning methods for fractional PIDs. In *Preprints, IFAC Workshop on Fractional Differentiation and its Applications, Badajoz, Spain*.
43. Varshney, P., & Gupta, S. K. (2014). Implementation of fractional Fuzzy PID controllers for control of fractional-order systems. In *Proceedings of the 2014 International Conference on Advances in Computing, Communications and Informatics, ICACCI 2014* (pp. 1322–1328). doi:10.1109/ICACCI.2014.6968376.
44. Wang, F. Y. (2003). The exact and unique solution for phase-lead and phase-lag compensation. *IEEE Transactions on Education*, *46*(2), 258–262. doi:10.1109/TE.2002.808279.
45. Xue, D., Liu, L., & Pan, F. (2015). Variable-order fuzzy fractional PID controllers for networked control systems. In *2015 IEEE 10th Conference on Industrial Electronics and Applications (ICIEA)* (pp. 1438–1442). doi:10.1109/ICIEA.2015.7334333.
46. Zhong, J., & Li, L. (2015). Tuning fractional-order $PI^{\lambda}D^{\mu}$ controllers for a solid-core magnetic bearing system. *IEEE Transactions on Control Systems Technology*, *23*(4), 1648–1656.
47. Zhu, Q., & Azar, A. T. (2015). Complex system modelling and control through intelligent soft computations. In *Studies in fuzziness and soft computing* (Vol. 319). Germany: Springer. ISBN 978-3-319-12882-5.