20. Electrical Characterization of Semiconductor Materials and Devices

M. Jamal Deen, Fabien Pascal

Semiconductor materials and devices continue to occupy a preeminent technological position due to their importance when building integrated electronic systems used in a wide range of applications from computers, cell-phones, personal digital assistants, digital cameras and electronic entertainment systems, to electronic instrumentation for medical diagnositics and environmental monitoring. Key ingredients of this technological dominance have been the rapid advances made in the quality and processing of materials – semiconductors, conductors and dielectrics – which have given metal oxide semiconductor device technology its important characteristics of negligible standby power dissipation, good input–output isolation, surface potential control and reliable operation. However, when assessing material quality and device reliability, it is important to have fast, nondestructive, accurate and easy-to-use electrical characterization techniques available, so that important parameters such as carrier doping density, type and mobility of carriers, interface quality, oxide trap density, semiconductor bulk defect density, contact and other parasitic resistances and oxide electrical integrity can be determined. This chapter describes some of the more widely employed and popular techniques that are used to determine these important parameters. The techniques presented in this chapter range in both complexity and test structure requirements from simple current–voltage measurements to more sophisticated low-frequency noise, charge pumping and deep-level transient spectroscopy techniques.

20.1 **Resistivity** ... 454
20.1.1 Bulk Resistivity ... 454
20.1.2 Contact Resistivity ... 459

20.2 **Hall Effect** ... 462
20.2.1 Physical Principles ... 462
20.2.2 Hall Scattering Factor ... 463

20.3 **Capacitance–Voltage Measurements** ... 464
20.3.1 Average Doping Density by Maximum–Minimum High-Frequency Capacitance Method ... 464
20.3.2 Doping Profile by High-Frequency and High–Low Frequency Capacitance Methods ... 466
20.3.3 Density of Interface States ... 467

20.4 **Current–Voltage Measurements** ... 470
20.4.1 *I–V* Measurements on a Simple Diode ... 470
20.4.2 *I–V* Measurements on a Simple MOSFET ... 470
20.4.3 Floating Gate Measurements ... 471

20.5 **Charge Pumping** ... 472

20.6 **Low-Frequency Noise** ... 473
20.6.1 Introduction ... 473
20.6.2 Noise from the Interfacial Oxide Layer ... 474
20.6.3 Impedance Considerations During Noise Measurement ... 475

20.7 **Deep-Level Transient Spectroscopy** ... 477

References ... 479

The continued evolution of semiconductor devices to smaller dimensions in order to improve performance – speed, functionality, integration density and reduced cost – requires layers or films of semiconductors, insulators and metals with increasingly high quality that are well-characterized and that can be deposited and patterned to very high precision. However, it is not always the case that improvements in the quality of materials have kept pace with the evolution of integrated circuit down-scaling. An important aspect of assessing the material quality and device reliability is the development and use of fast, nondestructive and accurate electrical characterization techniques to determine important parameters such as carrier doping density, type and mo-

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bility of carriers, interface quality, oxide trap density, semiconductor bulk defect density, contact and other parasitic resistances and oxide electrical integrity. This chapter will discuss several techniques that are used to determine these important parameters. However, it is not an extensive compilation of the electrical techniques currently used by the research and development community; rather, it presents a discussion of some of the more widely used and popular ones [20.1–4].

An important aspect of electrical characterization is the availability of appropriate test components [20.1–4]. In this chapter, we concentrate on discussing techniques that use standard test devices and structures. In addition, we will use the metal–oxide–semiconductor field-effect transistor (MOSFET) whenever possible because they are widely available on test chips. This is also motivated by the fact that MOSFETs continue to dominate the semiconductor industry for a wide range of applications from memories and microprocessors to signal and imaging processing systems [20.5]. A key reason for this dominance is the excellent quality of the silicon wafers and the silicon–silicon dioxide interface, both of which play critical roles in the performance and reliability of the device. For example, if the interface has many defects or interface states, or it is rough, then the device's carrier mobility decreases, low-frequency noise increases and its performance and reliability degrades. In particular, it is not only the interface that is important, but also the quality of the oxide; good-quality oxide prevents currents from flowing between the gate and substrate electrodes through the gate oxide. Both interface and oxide quality allows for excellent isolation between the input and output terminals of the MOSFETs, causing it to behave as an almost ideal switch. Therefore, it is important to have good experimental tools to study the interface properties and the quality of the gate dielectric.

Electrical characterization of semiconductors and the semiconductor–dielectric interface is important for a variety of reasons. For example, the defects at and in the interfacial oxide layer in silicon–silicon dioxide ($Si–SiO_2$) systems and in the bulk semiconductor play critical roles in their low-frequency noise, independent of whether the device is surface-controlled such as a MOSFET, or a bulk transport device such as a polysilicon emitter bipolar junction transistor (PE BJT). These defects can affect the charge transfer efficiency in charge coupled devices (CCDs), p–n photodiodes or complementary metal-oxide-semiconductor (CMOS) imagers, and can be the initiation point of catastrophic failure of oxides. Interface and bulk states can act as scattering centers to reduce the mobility in MOSFETs, thus affecting their performance parameters such as switching speed, transconductance and noise. This chapter is devoted to the electrical characterization of semiconductors, insulators and interfaces. In the first part (Sects. 20.1 and 20.2), the basic electrical properties of materials (such as resistivity, concentration and mobility of carriers) are studied. The main measurement techniques used to determine these electrical parameters are presented. Due to its increasing importance in modern ultrasmall geometry devices, electrical contacts are also studied. All of the characterization techniques presented in this first part are associated with specially designed test structures. In the second part (Sects. 20.4–20.7), we use active components such as capacitors, diodes and transistors (mainly MOSFETs) in order to determine more specific electrical parameters such as traps, oxide quality and noise level that are associated with material or devices. Of course this involves specific measurement techniques that are often more sophisticated than those discussed in the previous two sections.

20.1 Resistivity

Resistivity is one of the most important electrical parameters of semiconductors [20.1–4]. First, we present the basic physical relations concerning the bulk resistivity. The main electrical measurement techniques are then described: the two oldest ones that are still relevant today – the *four-point-probe* technique and the *van der Pauw* technique – and then the *spreading resistance* technique. Second, because it is closely linked with bulk resistivity measurement techniques and it is increasingly important in modern ultrasmall geometry devices, contact resistivity will be presented. Special attention will be given to *Kelvin contact resistance* (*KCR*) *measurement* and the *transmission line measurement* (*TLM*) techniques.

20.1.1 Bulk Resistivity

Physical Approach, Background and Basics

The bulk resistivity ρ is an intrinsic electrical property related to carrier drift in materials such as metals and semiconductors [20.6]. From a macroscopic point of view, the resistivity ρ can be viewed as the normalization of the bulk resistance (R) by its geometrical dimensions – the cross-sectional area ($A = Wt$) through

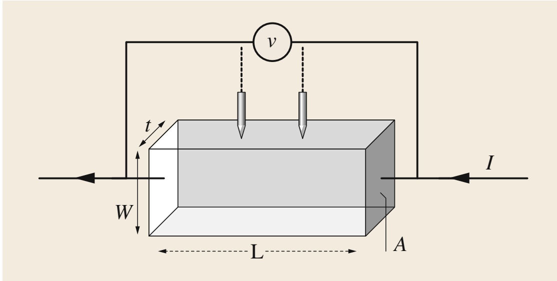

Fig. 20.1 Bulk resistance and its geometrical dimensions

which the current flows, and the distance between the two ideal contacts L, as shown in Fig. 20.1. The resistivity is given by

$$\rho = \frac{RA}{L} \quad \text{in } \Omega\,\text{m or commonly } \Omega\,\text{cm.} \tag{20.1}$$

For thin semiconductor layers, the sheet resistivity ρ_s is often used instead of the bulk resistivity ρ. The sheet resistivity ρ_s is the bulk resistivity divided by the sample's thickness t. This normalized parameter is related to the resistance of a square of side L. For this particular geometry in Fig. 20.1, since $A = Wt$, then $\rho_s = R_\square$, the sheet resistance. The unit of sheet resistance is Ω/square or $\Omega/\square$. The parameter $R_\square$ is convenient for integrated circuit designers because it allows them to quickly design the geometry for a specific value of resistance using very thin implanted or diffused semiconductor regions or polycrystalline layers. Resistivity (or its inverse, the conductivity σ in $\Omega^{-1}\,\text{cm}^{-1}$ or S/cm) and its variation with temperature is often used to classify material into metals, semiconductors and insulators.

Since different semiconductors can have the same resistivity, and also different values of resistivity can be found for a given semiconductor, depending on how it is processed for example, then resistivity is not a fundamental material parameter. From solid state theory, in the case of homogeneous semiconductor materials, the resistivity expresses the proportionality between the applied electric field E and the drift current density J; that is, $J = (1/\rho)\,E$. It can be defined by the microscopic relation

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)} , \tag{20.2}$$

where q is the electronic charge, n and p are the free electron and hole concentrations, and μ_n and μ_p are the electron and hole drift mobilities, respectively. In this way, the resistivity is related to fundamental semiconductor parameters: the number of free carriers, and their ability to move in the lattice when an electric field is applied.

In n-type or donor (N_D)-doped, or p-type or acceptor (N_A)-doped semiconductors, the free carrier densities are determined by the ionized impurities (N_D or $N_A \gg$ the intrinsic carrier concentration n_i), then (20.2) can be simplified to

$$\rho \approx \frac{1}{qn\mu_n} , \quad \text{for an n-type semiconductor} , \tag{20.3}$$

$$\text{and } \rho \approx \frac{1}{qp\mu_p} , \quad \text{for a p-type semiconductor} . \tag{20.4}$$

In the following sections, only single-type semiconductors will be studied. This corresponds to most semiconductor materials used in electronic and optoelectronic devices because either $N_D \gg N_A$ or $N_A \gg N_D$ in a typical semiconductor layer.

Measurement Techniques

The simplest way to determine bulk resistivity is to measure the voltage drop along a uniform semiconductor bar through which a direct current (DC) I flows, as shown in Fig. 20.1. Thus, the measured resistance and knowledge of the geometrical dimensions can lead to an estimate for the bulk resistivity according to (20.1). Unfortunately the measured resistance (R_{mea}) includes the unexpected contact resistance ($2R_c$), which can be significant for small-geometry samples because R_c is strongly dependent on the metal-semiconductor structure. Therefore, special processing technologies are used to minimize the influence of R_c (Sect. 20.1.2). Now, the measured resistance is expressed as

$$R_{mea} = R + 2R_c . \tag{20.5}$$

If probes are used instead of large metal-semiconductor contacts, then the spreading resistance (R_{sp}) under the two probes must also be added, as shown in Fig. 20.2. In this case, (20.5) becomes

$$R_{mea} = R + 2R_{sp} + 2R_c , \tag{20.6}$$

where R_{sp} for a cylindrical contact of radius r, and for a semi-infinite sample, it can be expressed by

$$R_{sp} = \frac{\rho}{4r} . \tag{20.7}$$

For a hemispherical contact of radius r, R_{sp} is given by

$$R_{sp} = \frac{\rho}{2\pi r} . \tag{20.8}$$

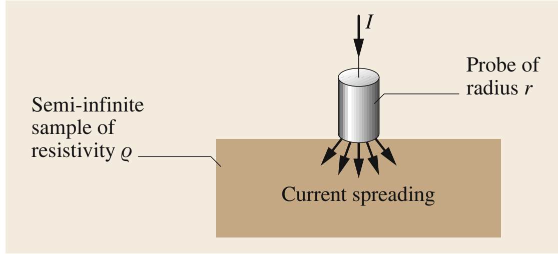

Fig. 20.2 Spreading resistance associated with a probe contact

In both cases, it is very difficult to provide a direct measurement or an accurate model of the contact resistance. So determining the bulk resistivity by this approach is not recommended, except when the spreading resistance is the dominant term in (20.6) and when (20.7) or (20.8) can be applied. In this case, the resistivity is determined by the *spreading resistance* technique measurement. Nevertheless, despite the lack of accuracy of the two contact techniques, it can be sufficient for monitoring some process steps and it is often used in the semiconductor industry as a process monitor.

Four-Point Probe Technique. In order to eliminate or at least minimize the contact contribution to the measured resistance value, techniques based on separate current injection and voltage drop measurements have been developed. First, the two-probe technique can be used, as reported in Fig. 20.1. This measurement is very simple, but it is affected by several parameters: lateral contact geometry, probe spacing, and minority carrier injection near the lateral contacts. The main disadvantage of this technique is the need for lateral contacts. This requirement is overcome with the four-point probe technique, where two probes are used for current injection and the other two probes are used to measure the voltage drop. The more usual probe geometry configuration is when the four probes are placed in a line, as shown in Fig. 20.3.

The voltage at probe 2, V_2, induced by the current flowing from probe 1 to probe 4 is given by:

$$V_2 = \frac{\rho I}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2 + s_3}\right) . \tag{20.9a}$$

The voltage at probe 3 is

$$V_3 = \frac{\rho I}{2\pi}\left(\frac{1}{s_1 + s_2} - \frac{1}{s_3}\right) . \tag{20.9b}$$

Then, by measuring $V = V_2 - V_3$, the voltage drop between probes 2 and 3, and the current I through probes 1 and 4, the resistivity can be determined using (20.9a)

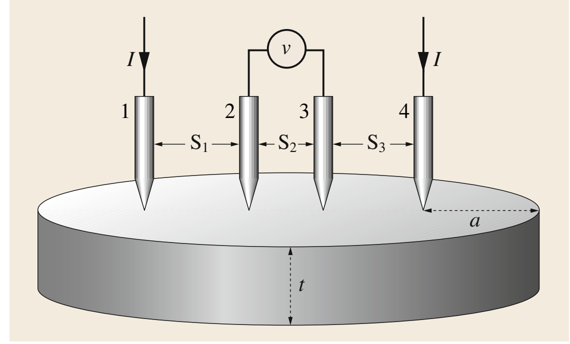

Fig. 20.3 Linear four-point probe configuration. The sample thickness is t and a is the distance from the edge or boundary of the sample

and (20.9b) as

$$\rho = \frac{2\pi V/I}{\left(\frac{1}{s_1} + \frac{1}{s_2} - \frac{1}{s_2+s_3} - \frac{1}{s_1+s_2}\right)} \tag{20.10}$$

Thus, a direct measurement of the resistivity can be made using a high-impedance voltmeter and a current source. When the probe spacings are equal ($s_1 = s_2 = s_3 = s$), which is the most practical case, then (20.10) becomes

$$\rho = 2\pi s \frac{V}{I} . \tag{20.11}$$

Equations (20.10) and (20.11) are valid only for semi-infinite samples; that is, when both t and the sample surface are very large ($\rightarrow \infty$), and the probes' locations must be far from any boundary. Because these relations can be applied only to large ingots, then in many cases a correction factor f must be introduced in order to take into account the finite thickness and surface of the sample and its boundary effects. Further, for epitaxial layers, f must also consider the nature of the substrate – whether it is a conductor or an insulator. Thus, (20.11) becomes

$$\rho = 2\pi s \frac{V}{I} f . \tag{20.12}$$

For a thin semiconductor wafer or thin semiconducting layer deposited on an insulating substrate, and for the condition $t < s/2$, which represents most practical cases because the probe spacing s is usually on the order of a millimeter, then the correction factor due to the thickness is

$$f = \frac{(t/s)}{2\ln 2} \quad \text{so that} \quad \rho = 4.532 t \frac{V}{I} . \tag{20.13}$$

The noninfinite sample surface must be corrected if the ratio of the wafer diameter to the probe spacing is not

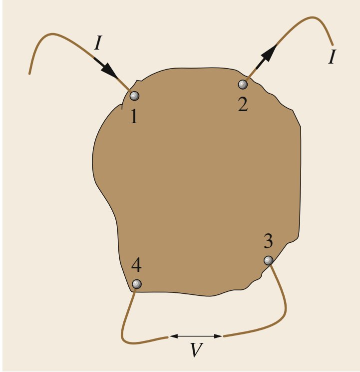

Fig. 20.4 van der Pauw method for an arbitrarily shaped sample

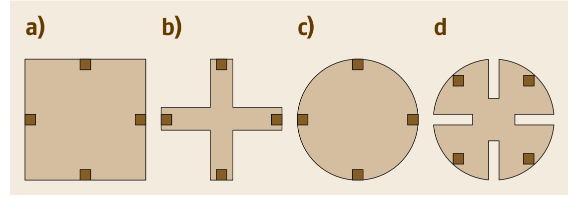

Fig. 20.5a–d Symmetrical van der Pauw structures: **(a)** square, **(b)** Greek cross, **(c)** circle and **(d)** cloverleaf

greater than 40, otherwise a correction factor of less than unity has to be introduced [20.3].

If the probe header is too close to any boundary, then (20.13) is no longer valid and another correction factor must be introduced. This correction factor is close to 1 until the ratio a/s is greater than 2, where a is the distance from the edge of the sample that is shown in Fig. 20.3. A study of various 8 inch n- and p-type silicon wafers have demonstrated that the edge exclusion limit is 5 mm [20.7].

In the case of a different arrangement of probes, for instance a square array or when a different measurement configuration of the four-point collinear probes is used, such as current injection between probes 1 and 3, other specific correction factors are required. Here, rather than detail all the different correction factors, complementary information can be found in [20.4, Chap. 4] and [20.3, Chap. 1].

Taking into account the appropriate correction factors as well as some specific material parameters such as hardness or surface oxidation, it is possible to map the resistivities of different types of semiconductor wafers or deposited semiconductor layers with an accuracy better than 1% over a large range of resistivity values using commercial equipment and appropriate computational techniques.

Van der Pauw Technique. Based on the same basic principle of separating the current injection and voltage measurement, the *van der Pauw* [20.8] measurement technique allows for the determination of resistivity on a sample of arbitrary shape using four small contacts placed on the periphery, as shown in Fig. 20.4. Then, the resistivity of a uniform sample of thickness t is given by

$$\rho = \frac{\pi t}{\ln 2} \frac{(R_\mathrm{A} + R_\mathrm{B})}{2} f \,. \tag{20.14}$$

Here, R_A and R_B are resistances measured by injecting current on two adjacent contacts and by measuring the voltage drop on the two remaining ones. With the notation in Fig. 20.4, one can define

$$R_\mathrm{A} = \frac{V_3 - V_4}{I_{1,2}} \,, \quad R_\mathrm{B} = \frac{V_4 - V_1}{I_{2,3}} \,,$$

f is a correction factor that is

a function of the ratio $R_f = \dfrac{R_\mathrm{A}}{R_\mathrm{B}}$. (20.15)

with R_f obtained from

$$\frac{(R_f - 1)}{(R_f + 1)} = \frac{f}{\ln 2} \operatorname{arccosh}\left(\frac{\exp(\ln 2/f)}{2}\right) . \tag{20.16}$$

In the case of samples with symmetrical geometries, and when the contacts are also symmetrical, as shown in Fig. 20.5, then $R_\mathrm{A} = R_\mathrm{B}$, $R_f = 1$ and $f = 1$, and (20.14) becomes

$$\rho = \frac{\pi t}{\ln 2} R_\mathrm{A} = 4.532 t R_\mathrm{A} \,. \tag{20.17}$$

In order to minimize errors caused by the finite dimensions of the contacts (since ideally the contact area should be zero) and the finite thickness of the sample, then the distance between the contacts must be larger than both the diameter and the thickness of the contact. Also, the cloverleaf configuration in Fig. 20.5d is recommended to prevent contact misalignment, but this configuration requires a more complicated patterning technology.

The main advantage of the van der Pauw technique compared to the four-point probe technique is its use of a smaller area for the test structure. Therefore, this measurement technique is often used in integrated circuit technology. Also, because of its simple structure, the Greek cross configuration in Fig. 20.5b is widely used (experimental results obtained on SiGeC epitaxial layers are reported in Fig. 20.6 as an example). However, when narrows arms are used, current crowding at the corners may have a significant influence, and in this case a different Greek cross layout can be considered to reduce this current crowding effect [20.9].

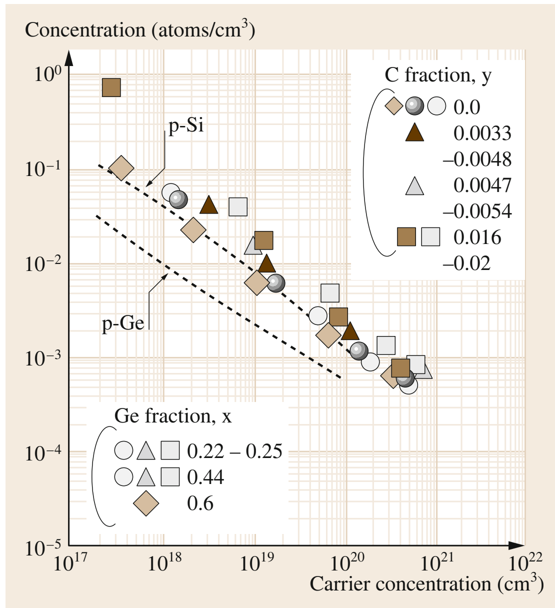

Fig. 20.6 Resistivity versus carrier concentration in $Si_{1-x-y}Ge_xC_y$ films obtained using a cloverleaf van der Pauw structure. (After [20.10])

Spreading Resistance Technique. The spreading resistance technique is based on the modeling of current spreading from a probe tip or a small metallic contact and flowing into a bulk semiconductor, as shown previously in Fig. 20.2. Equations (20.7) and (20.8) presented above are for cylindrical probes and hemispherical probes, respectively. Basically, the principle of this method is opposite to the previous four-contact techniques where the separation of the current injection from the measured voltage drop was used to avoid the spreading resistance. Here, the spreading resistance is expected to be the dominant term in (20.6). Only two contacts are needed: two closely aligned probes, a small top contact probe or a metallic contact and a large bottom contact. In the first case, surface mapping can be performed, but the main use of this compact probe configuration is for resistivity profiling using a bevelled sample [20.3]. The second configuration has been used to measure the substrate resistivity of silicon integrated circuits where simple test structures – for example the square top contact of 25 μm × 25 μm and 50 μm × 50 μm shown in [20.12] – have been included on a test chip.

More recently, semiconductor resistivity has been nanocharacterized using scanning spreading resistance microscopy (SSRM) with a standard atomic force microscope (AFM) of lateral resolution of 10 to 20 nm. A SSRM image of a 0.5 μm nMOSFET is given in Fig. 20.7a [20.11]. The resistance is low in the highly doped regions (dark) and high in the lower doped regions (bright): source, drain, gate and well regions are clearly observed in Fig. 20.7a or the resistance profile in Fig. 20.7b. With such a high resolution, scanning the lateral and vertical diffusion of dopants in active regions of submicron transistors is possible. An example is shown in Fig. 20.7c where the extra implantations (halo and lightly doped drain (LDD)) in a 0.35 μm nMOSFET process are clearly visible and result in a change of L_{eff} from 295 nm without extra implantations to 229 nm with the extra implantations.

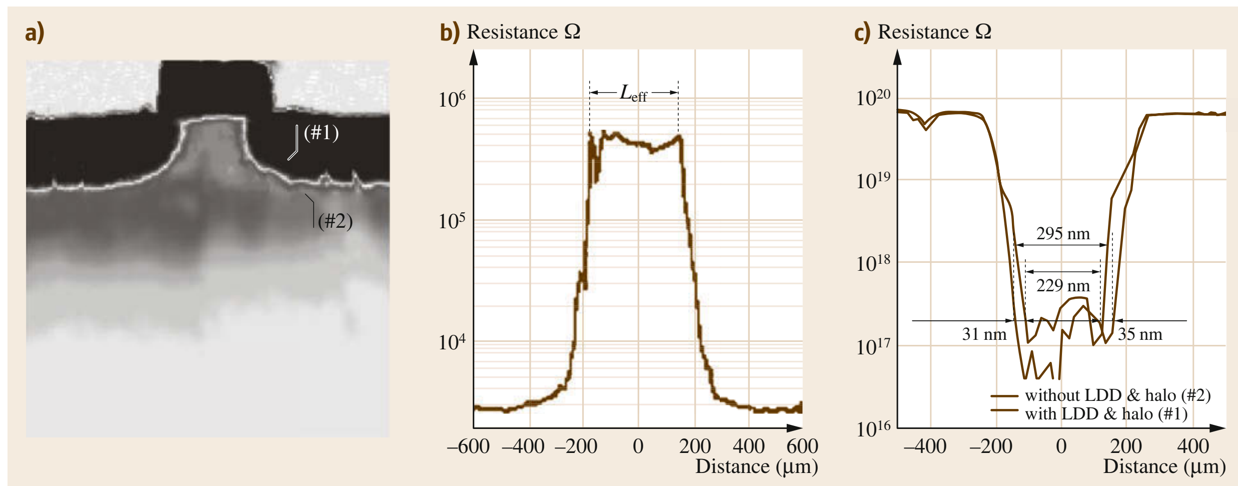

Fig. 20.7 (a) SSRM resistance image (scan size: 1.5 μm × 1.5 μm) of a 0.5 μm nMOSFET; **(b)** lateral section taken 10 nm under the gate oxide of the same transistor; **(c)** lateral carrier concentration profiles measured with SSRM 10 nm under the gate oxide for two 0.35 μm nMOSFETs (with and without halo and LDD process). (After [20.11])

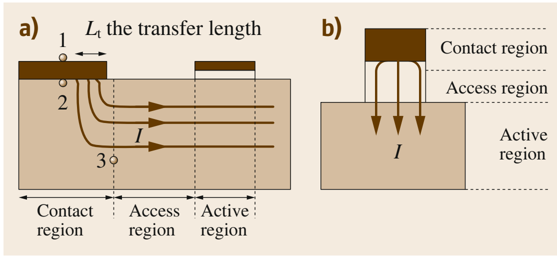

Fig. 20.8 (**a**) Horizontal contact and (**b**) vertical contact. *Black* indicates the metallic conductor, *white* the semiconductor material or an insulator

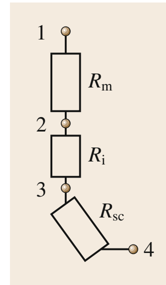

Fig. 20.9 Different components of the contact resistance

20.1.2 Contact Resistivity

The contact resistance of an active device and interconnection becomes larger as the dimensions are scaled down. As a consequence, the performance of single transistors as well as integrated circuits can be seriously limited by increasing *RC* time constants and power consumption. This is of major interest for the semiconductor industry, as reported by the International Technology Roadmap for Semiconductors, ITRS 2001 [20.5], and in [20.13].

Contact Resistance Elements

Basically, the contact resistance R_c is the resistance localized from a contact pad, a probe or from the metallization process to an active region. However, it does not include all of the access resistances between these two regions, as shown in Fig. 20.8a for a horizontal contact and Fig. 20.8b for a vertical contact.

Starting from the contact pad (Figs. 20.8a and 20.9), the contact resistance includes the resistance of the metal R_m, the interfacial metal-semiconductor resistance R_i, and the resistance associated with the semiconductor just below the contact in the contact region R_{sc}. Thus, the contact resistance can be expressed as

$$R_c = R_m + R_i + R_{sc} . \quad (20.18)$$

The last component R_{sc} cannot be accurately defined because the boundary between the contact and access regions is very difficult to determine due to (for example) interdiffusion of metal and semiconductor atoms, and because the current flow into this region is not homogeneous due to current spreading and lateral or vertical current crowding at the periphery of the contact. The relative importance of each component of R_c is strongly dependent on different parameters of the process itself – annealing temperature, doping density and the geometry used (lateral or vertical).

When comparing different contact technologies and different contact areas, the most convenient parameter to use is the contact resistivity ρ_c, which is referred to as the specific contact resistance in $\Omega\,cm^2$, and ρ_c is given by

$$\rho_c = R_c A_{ceff} , \quad (20.19)$$

where A_{ceff} is the effective contact area; that is, the current injection area. The concept of an effective contact area can be approximated by the contact geometry in the case of a vertical contact in Fig. 20.8b. However, A_{ceff} is more difficult to specify for a lateral contact, where a transfer length L_T, representing the length where the current flow transfers from the contact into the semiconductor just underneath, must be introduced, as shown in Fig. 20.8a. L_T is defined as the length over which the voltage drops to e^{-1} of its value at the beginning of the contact [20.3], and is given by

$$L_T = \sqrt{\frac{\rho_c}{\rho_{sc}}} , \quad (20.20)$$

where ρ_{sc} is the sheet resistivity of the semiconductor below the contact.

Because of its various components, it is difficult to accurately model the contact resistivity. Nevertheless, a theoretical approach to the interfacial resistivity (see R_i in (20.18)), ρ_i, can be determined from the well-known Schottky theory of metal–semiconductor contacts. The interfacial resistivity ρ_i is defined by

$$\rho_i = \left.\frac{\partial V}{\partial J}\right|_{V=0} . \quad (20.21)$$

This metal–semiconductor structure is equivalent to an abrupt p-n junction. According to the Schottky theory (for more details see [20.14, Chap. 5]), the J–V characteristic of a metal–semiconductor contact in the case of a low-doped semiconductor is given by

$$J = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] , \quad (20.22)$$

where A^* is Richardson's constant, and T the absolute temperature. ϕ_B is the barrier height formed at

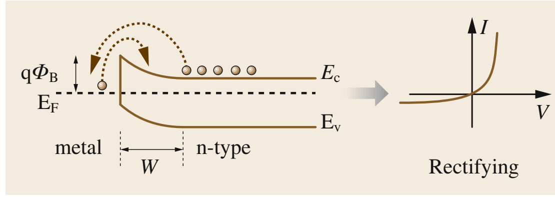

Fig. 20.10 Energy-band diagram of an n-type semiconductor–metal contact and related rectifying contact. W is the width of the depletion layer

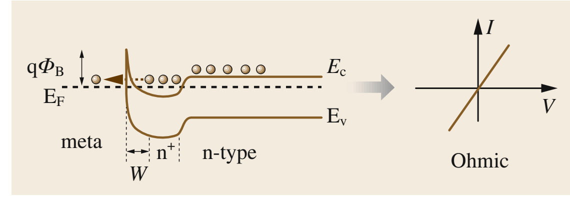

Fig. 20.11 Energy-band diagram of an n^+-n semiconductor–metal structure and related ohmic contact

the metal–semiconductor interface – the difference between the vacuum level and the Fermi level of the metal and of the semiconductor materials respectively, and ϕ_B is given by

$$\phi_B = \phi_M - \chi \tag{20.23}$$

where ϕ_M is the metal work function and χ the semiconductor electron affinity.

The energy band diagram for a low-doped n-type semiconductor–metal contact is shown in Fig. 20.10. In this case, the current transport is dominated by the thermionic emission current, resulting in a rectifying contact.

Thus, when the conduction mechanism is controlled by the thermionic emission (TE), the interfacial resistivity in (20.21) is simply obtained from the derivative of (20.22), and $\rho_{i,TE}$ is

$$\rho_{i,TE} = \frac{k}{qA^*T} \exp\left(\frac{q\phi_B}{kT}\right) \tag{20.24}$$

Due to the presence of surface states, the barrier height ϕ_B is positive and weakly dependent on the metal–semiconductor material. ϕ_B is $\approx 2E_g/3$ for an n-type semiconductor and $\approx E_g/3$ for a p-type semiconductor. Therefore, high values of interfacial resistivity $\rho_{i,TE}$ are usually obtained except when narrow bandgap semiconductors are used.

The way to fabricate ohmic contacts with low contact resistivity values is to process the metal on a heavily doped semiconductor layer. In this case, the depletion width decreases ($W \approx N_D^{-1/2}$) and the probability of carrier tunneling through the barrier increases. Thus, the conduction mechanism is dominated by tunneling, as shown in Fig. 20.11.

The electron tunneling current is expressed as

$$J_{tun} \approx \exp\left(\frac{q\phi_B}{E_{00}}\right), \tag{20.25}$$

where

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon_s m_n^*}}, \tag{20.26}$$

ε_s is the permittivity of the semiconductor and m_n^* is the effective mass of the electron.

From (20.21), (20.25) and (20.26), the interfacial resistivity $\rho_{i,T}$ is found to be

$$\rho_{i,T} \propto \frac{2\sqrt{\varepsilon_s m_n^*}}{\hbar}\frac{\phi_B}{\sqrt{N_D}}. \tag{20.27}$$

Comparing $\rho_{i,TE}$ from (20.24) to $\rho_{i,T}$ from (20.27), we see that a highly doped layer can significantly reduce the interfacial resistivity. For $N_D \geq 10^{19}\,cm^{-3}$, the tunneling process dominates the interfacial resistivity, while for $N_D \leq 10^{17}\,cm^{-3}$, the thermionic emission current is dominant.

As most semiconductors such as Si, SiGe, GaAs, InP are of relatively wide bandgap, the deposition of a heavily doped layer before the metallization is commonly used in order to form a tunneling contact. For compound semiconductor manufacturing processes, the contact layer is generally formed from the same semiconductor material, or at least from the same material as the substrate. For silicon and related materials such as SiGe alloys or polysilicon, silicidation techniques are commonly used to make the contact layer with very thin silicide layers such as $CoSi_2$ or $TiSi_2$ layers.

Measurement Techniques

As mentioned above, it is difficult to accurately model the contact resistance, so direct measurements of the contact resistance or of the contact resistivity are of great importance. The two main test structures used to determine contact characteristics will now be discussed: the *cross Kelvin resistor* (*CKR*) *test structure* and the *transmission line model* (*TLM*) structure.

Kelvin Test Structure. The Kelvin test structure, also referred to as the cross Kelvin resistor (CKR) test structure, is shown in Fig. 20.12. The contact resistance R_c is determined from the potential drop in the contact window (V_{34}) when a current I is forced through the contact window from contact pad 1 to pad 2, and R_c is

$$R_c = \frac{V_{34}}{I}. \tag{20.28}$$

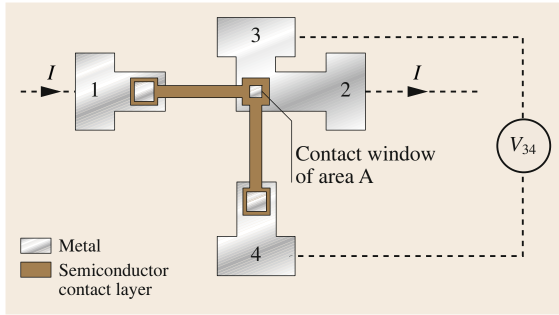

Fig. 20.12 Cross Kelvin resistor test structure

Therefore, a measure of R_c and knowledge of the contact area A allows for direct extraction of the contact resistivity ρ_c, given by

$$\rho_c = R_c A\,. \tag{20.29}$$

This basic approach is not valid when parasitic effects are present. One of the main problems is current crowding around the contact. In order to extract accurate values for the contact resistivity using Kelvin test structures, it is necessary to take into account the two-dimensional current-crowding effect. This is achieved using the results from numerical simulations [20.15]. Nevertheless, the development of ohmic contacts with very low values of contact resistivities require complex technology with different materials and usually with several interfaces. In this case, a large discrepancy between the extracted and the measured contact parameters can be found [20.15, 16]. To improve the accuracy, three-dimensional models are now used to take into account the different interfacial and vertical parasitic effects [20.17].

Transmission Line Model Test Structures. The transmission line model test structure (TLM) consists of depositing a metal grid pattern of unequal spacing L_i between the contacts. This leads to a scaled planar resistor structure. Each resistor changes only by its distance L_i between two adjacent contacts, as shown in Fig. 20.13, and it can be expressed by

$$R_i = \frac{\rho_s L_i}{W} + 2R_c \tag{20.30}$$

Then, by plotting the measured resistances as a function of the contact spacing L_i, and according to (20.30), the layer sheet resistivity ρ_s and the contact resistance R_c can be deduced from the slope and from the intercept at $L_i = 0$ respectively, as shown in Fig. 20.14

$$\text{Slope} = \frac{\rho_s}{W}\,;\; R_i(\text{intercept}) = 2R_c\,;$$
$$\text{and}\; |L_i(\text{intercept})| = 2L_T \tag{20.31}$$

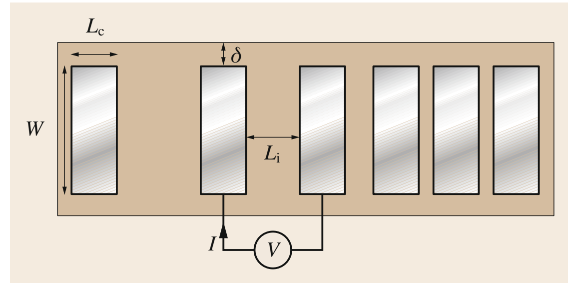

Fig. 20.13 Transmission line model (TLM) test structure

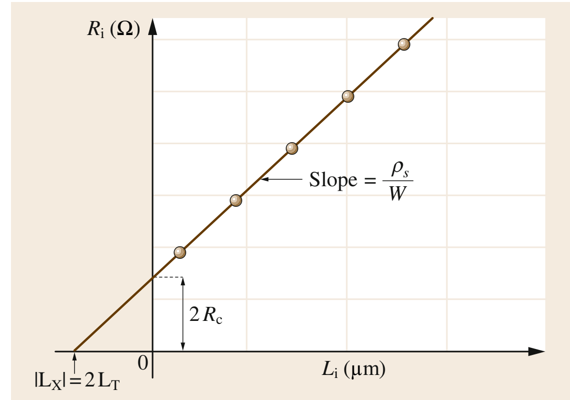

Fig. 20.14 Determination of the sheet resistivity and characterization of the contact using a TLM test structure

As discussed in Sect. 20.1.2, the most suitable parameter for characterizing a contact is its contact resistivity (ρ_c) or the specific contact resistance ($R_c A_{ceff}$), given by

$$\rho_c = R_c A_{ceff} = R_c W L_T \tag{20.32}$$

As shown in Fig. 20.8a, for a planar resistor, the effective contact area requires the notion of the transfer length L_T. According to (20.20), and assuming that the sheet resistance under the contact ρ_{sc} is equal to the sheet resistance between the contacts ρ_s, then L_T can be expressed by (20.20).

Therefore, the substitution of R_c into (20.32) in (20.30) leads to

$$R_i = \frac{\rho_s}{W} L_i + \frac{\rho_s}{W} 2L_T \tag{20.33}$$

Now, extrapolation to $R_i = 0$ allows us to determine the value of L_T. The main advantage of the *TLM* method is its ability to give two main electrical parameters, the resistivity of the semiconductor contact layer ρ_s and the contact resistance R_c. However, this is done at the expense of a questionable assumption that the sheet resistance under the contact must be equal to the sheet resistance between the contacts. More on this technique can be found in [20.3].

20.2 Hall Effect

As mentioned before, the resistivity of a semiconductor is not a fundamental material parameter. One can consider the carrier density (n or p) or the carrier mobility (μ_n or μ_p) to be fundamental or microscopic parameters. For a semiconductor material, the resistivity is related to these two parameters (density and mobility) by (20.2). The strength of the Hall effect is to directly determine the sheet carrier density by measuring the voltage generated transversely to the current flow direction in a semiconductor sample when a magnetic field is applied perpendicularly, as shown in Fig. 20.15a. Together with a resistivity measurement technique such as the four-point probe or the van der Pauw technique, Hall measurements can be used to determine the mobility of a semiconductor sample.

In modern semiconductor components and circuits, knowledge of these two fundamental parameters n/p and μ_n/μ_p is critical. Currently, Hall effect measurements are one of the most commonly used characterization tools in the semiconductor industry and research laboratories. This is not just because of the parameters that can be extracted for use in device modeling or materials characterization, but also because of the quantum Hall effect (QHE) in condensed matter physics [20.18]. Moreover, in the applied electronics domain, one should note the development of different sensors based on the physical principle of the Hall effect, such as commercial CMOS Hall sensors.

As is very often the case, the development of a characterization technique is related to its cost, simplicity of implementation and ease of use. Since these practical characteristics are satisfied even when specially shaped samples are required, then the Hall effect measurement technique has become a very popular method of characterizing materials.

In this section, we will first present the physical principle of the Hall effect. Then we will show how it can be used to determine the carrier density and mobility. Finally, the influence of the Hall scattering factor will be presented, followed by some practical issues about the implementation of the Hall effect method.

20.2.1 Physical Principles

The Hall effect was discovered by *Hall* in 1879 [20.19] during an experiment on current transport in a thin metal strip. A small voltage was generated transversely when a magnetic field was applied perpendicularly to the conductor.

The basic principle of this Hall phenomenon is the deviation of some carriers from the current line due to the Lorentz force induced by the presence of a transverse magnetic field. As a consequence, a voltage drop V_H is induced transversely to the current flow. This is shown in Fig. 20.15a for a p-type bar-shaped semiconductor, where a constant current flow I_x in the x-direction and a magnetic field in the z-direction results in a Lorentz force on the holes. If both holes and electrons are present, they deviate towards the same direction. Thus, the directions of electrical and magnetic fields must be accurately specified.

The Lorentz force is given by the vector relation

$$F_L = q(\boldsymbol{v} \times \boldsymbol{B}) = -qv_x B_z \,, \tag{20.34}$$

where v_x is the carrier velocity in the x-direction. Assuming a homogeneous p-type semiconductor

$$v_x = \frac{I}{qtWp} \,. \tag{20.35}$$

As a consequence, an excess surface electrical charge appears on one side of the sample, and this gives rise to an electric field in the y-direction E_y. When the magnetic force F_L is balanced by the electric force F_{EL}, then the Hall voltage V_H is established, and from a balance between F_L and F_{EL}, we get

$$F = F_L + F_{EL} = -qv_x B_z + qE_y = 0 \,, \tag{20.36}$$

$$\text{so } E_y = \frac{BI}{qtWp} \,. \tag{20.37}$$

Also, the Hall voltage V_H is given by

$$V_H = V_y = E_y W = \frac{BI}{qtp} \,. \tag{20.38}$$

So if the magnetic field B and the current I are known, then the measurement of the Hall voltage gives the hole sheet concentration p_s from

$$p_s = pt = \frac{BI}{qV_H} \,. \tag{20.39}$$

If the conducting layer thickness t is known, then the bulk hole concentration can be determined (see (20.41)) and expressed as a function of the Hall coefficient R_H, defined as

$$R_H = \frac{tV_H}{BI} \tag{20.40}$$

$$\text{and } p = \frac{1}{qR_H} \tag{20.41}$$

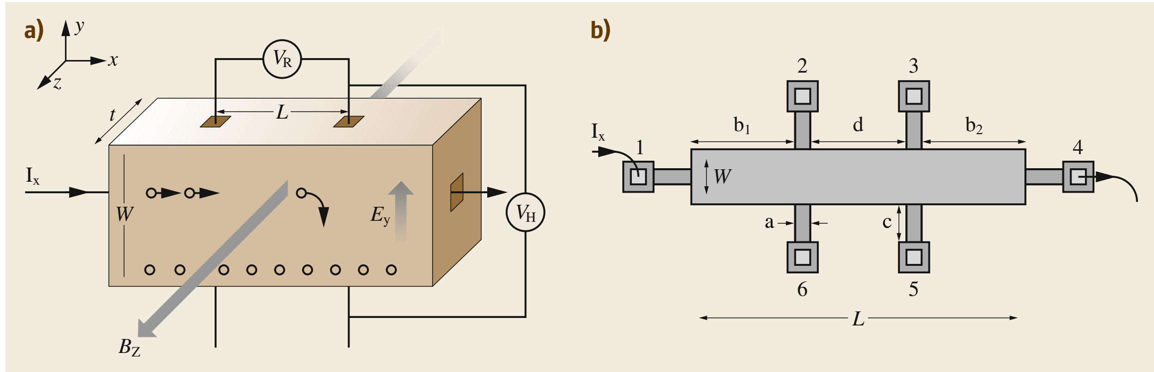

Fig. 20.15 **(a)** Representation of the Hall effect in an p-type bar-shaped semiconductor. **(b)** Practical sample geometry: a six-terminal Hall-bar geometry

Using the same approach for an n-type homogeneous semiconductor material leads to

$$R_H = -\frac{tV_H}{BI} , \tag{20.42}$$

$$\text{and } n = -\frac{1}{qR_H} \tag{20.43}$$

Now, if the bulk resistivity ρ is known or can be measured at the same time using a known sample such as a Hall bar or van der Pauw structure geometry in zero magnetic field, then the carrier drift mobility can be obtained from

$$\mu = \frac{|R_H|}{\rho} \tag{20.44}$$

There are two main sample geometries commonly used in Hall effect measurements in order to determine either the carrier sheet density or the carrier concentration if the sample thickness is known, and the mobility. The first one is the van der Pauw structure presented in Sect. 20.1.1. The second one is the Hall bar structure shown in Fig. 20.15b, where the Hall voltage is measured between contacts 2 and 5, and the resistivity is measured using the four-point probes technique presented in Sect. 20.1.1 (contacts 1, 2, 3 and 4). Additional information about the shapes and sizes of Hall structures can be found in [20.3, 4, 20].

Whatever the geometry used for Hall measurements, one of the most important issues is related to the offset voltage induced by the nonsymmetric positions of the contact. This problem, and also those due to spurious voltages, can be controlled by two sets of measurements, one for a magnetic field in on direction and another for a magnetic field in the opposite direction.

The Hall effect has also been investigated on specific structures, and an interesting example can be found in reference [20.21], where a Hall bar structure was combined with a double-gate n-silicon-on-insulator (SOI) MOSFET. This was done in order to understand the mobility behavior in ultra-thin devices and to validate the classical drift mobility extraction method based on current–voltage measurements.

In the Hall effect experiment, the measurement of the Hall coefficient R_H leads to the direct determination of the carrier concentration and mobility. Moreover, the sign of R_H can be used to determine the type of conductivity of the semiconductor sample. If various types of carriers are present, then the expression for R_H becomes more complex and approximations in the limit of low and high magnetic field are necessary [20.3, Chap. 8].

We have so far discussed the Hall effect on a uniformly doped substrate or single semiconductor layer deposited on an insulating or semi-insulating substrate. In the case of a semiconductor layer deposited on a semiconducting substrate of opposite doping type, Hall effect measurements can be performed if the space charge region can act as an insulator. In the case of multilayers, the problem is more difficult, but an approximation for transport experiments has been developed for two-layer structures [20.22] and applied to different metal–semiconductor field-effect-transistor (MESFET) structures, for instance [20.23].

20.2.2 Hall Scattering Factor

The relations presented above are based on an energy-independent scattering mechanism. With this assumption made, the Hall carrier concentration and the Hall mobility are equal to the carrier concentration and the carrier drift mobility. When this assumption is no longer valid, these electrical parameters are different and the Hall scattering factor r_H must be taken into account. In this case (20.41), (20.43) and (20.44) must be modified

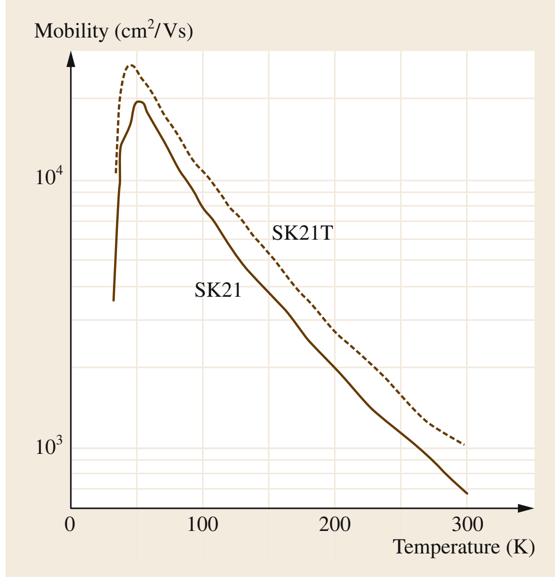

Fig. 20.16 Hall mobility as a function of temperature on two SOI films. (After [20.24])

as follows

$$p_H = \frac{r_H}{qR_H} = r_H p \,, \tag{20.45}$$

$$n_H = -\frac{r_H}{qR_H} = r_H n \,, \tag{20.46}$$

and

$$\mu_H = r_H \frac{|R_H|}{\rho} = r_H \mu \,. \tag{20.47}$$

The Hall scattering factor [20.25] is related to the energy dependence of the mean free time between carrier collisions $\tau(E)$, and r_H is given by

$$r_H = \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \,. \tag{20.48}$$

According to theory [20.3], the Hall scattering factor tends to unity in the limit of high magnetic field. Therefore, r_H at low magnetic fields can be determined by measuring the Hall coefficient in the limit of both high and low magnetic fields [20.25] using

$$r_H = \frac{R_H(B)}{R_H(\infty)} \tag{20.49}$$

Depending on the scattering mechanism involved (lattice, ionized or neutral impurity, electron, or phonon scattering), r_H is found to vary between 0.6 and 2 [20.26]. However, due to valence band distortion effects, values as low as 0.26 have been found in strained p-type SiGe epilayers [20.27]. Therefore, the Hall carrier concentration and especially the Hall mobility must be distinguished from carrier concentration and carrier drift mobility.

As the different scattering mechanisms have different temperature (T) dependences, then the Hall mobility as function of temperature is often used to separate the different scattering processes. An example is given in Fig. 20.16 for silicon-on-insulator (SOI) films [20.24]. The increase in the mobility between 4 and 45 K, which is given by $\mu \propto T^{2.95}$, is related to the ionized donor scattering mechanism. The decrease in mobility between 46 and 120 K given by $\mu \propto T^{-1.55}$ is associated with lattice scattering. However, after 150 K, the rapid decrease in mobility observed, where $\mu \propto T^{-2.37}$, suggests that other scattering mechanisms as well as the lattice scattering mechanism, such as electron or phonon scattering, must be taken into account.

20.3 Capacitance–Voltage Measurements

Capacitance–voltage (C–V) measurements are normally made on metal-oxide semiconductor (MOS) or metal-semiconductor (MS) structures in order to determine important physical and defect information about the insulator and semiconductor materials. For example, high-frequency (HF) and low-frequency (LF) or quasi-static C–V measurements in these structures are used to determine process and material parameters – insulator thickness, doping concentration and profile, density of interface states, oxide charge density, and work function or barrier height. In this section, we describe various C–V measurements and how they can be used to provide process parameters as well as valuable information about the quality of the materials. A typical C–V curve for a MOS capacitor with an n-type semiconductor is shown in Fig. 20.17. For a MOS capacitor with a p-type substrate, the C–V curve be similar to that in Fig. 20.17, but reflected about the y-axis.

20.3.1 Average Doping Density by Maximum–Minimum High-Frequency Capacitance Method

The maximum–minimum high-frequency (HF) capacitance method uses the HF capacitance under strong accumulation (C_{OX}) and strong inversion ($C_{HF,min}$) to

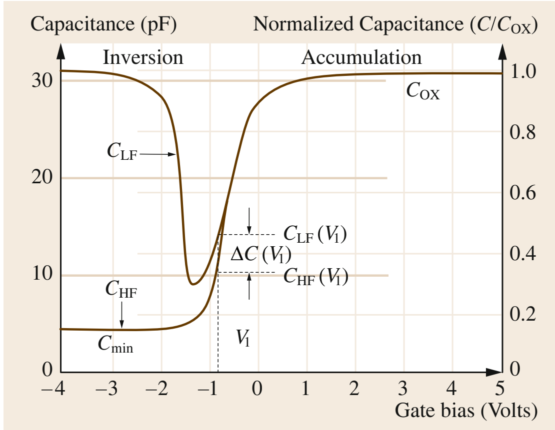

Fig. 20.17 Typical C–V curve for a MOS capacitor on an n-type substrate. (After [20.28])

determine the average doping density [20.29, pp. 406–408]. Note that under strong inversion and at high frequencies, the interface trap capacitance is negligible ($C_{\text{it}} \approx 0$). Under strong inversion, the depletion width ($w_{\max}$) is a maximum and so the high frequency capacitance per unit area $C_{\text{HF,min}}$ is a minimum, since the minority carriers cannot respond to the high-frequency signal. Since the inversion layer is very thin compared to the depletion layer, then

$$w_{\max} = \varepsilon_{\text{Si}} \left(\frac{1}{C_{\text{HF,min}}} - \frac{1}{C_{\text{OX}}} \right) , \tag{20.50}$$

where ε_{Si} is the permittivity of silicon and C_{OX} is the gate oxide capacitance per unit area.

At the conditions for $w_{\max}$, the band bending $\psi_{\max}$ is a maximum, and it is

$$\begin{aligned}\psi_{\max} &= 2\phi_{\text{B}} + \frac{kT}{q} \ln\left(2\frac{q}{kT}\phi_{\text{B}} - 1\right) \\ &= 2\frac{kT}{q}\left\{\ln\left(\frac{n}{n_i}\right) + \frac{1}{2}\ln\left[2\ln\left(\frac{n}{n_i}\right) - 1\right]\right\} ,\end{aligned} \tag{20.51}$$

where $\phi_{\text{B}} = (k_{\text{B}}T/q)\ln(n/n_i)$ is the shift of the Fermi level from the intrinsic Fermi level $\phi_i = (E_{\text{c}} - E_v)/2q$ in the bulk of the silicon in the MOS structure due to the doping concentration n, and n_i is the thermally generated carrier concentration in silicon. For a uniformly doped sample,

$$w_{\max}^2 = \frac{2\varepsilon_{\text{Si}}\psi_{\max}}{qn} \tag{20.52}$$

and from (20.50) and (20.52), a relation between the doping concentration n and the measured capacitance

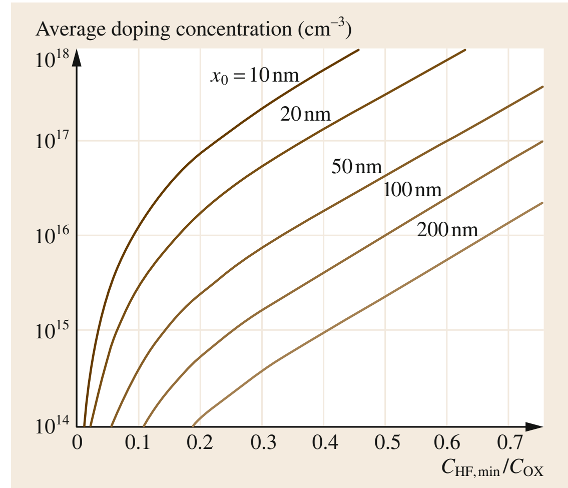

Fig. 20.18 Doping concentration n as function of $C_{\text{HF,min}}/C_{\text{OX}}$ with oxide thickness, based on (20.53). (After [20.29])

can be established [20.29, p. 407] as

$$\frac{n}{\ln\left(\frac{n}{n_i}\right) + \frac{1}{2}\ln\left[2\ln\left(\frac{n}{n_i}\right) - 1\right]} = \frac{4kT}{q^2\varepsilon_{\text{Si}}} \frac{C_{\text{OX}}^2}{\left(\frac{C_{\text{OX}}}{C_{\text{HF,min}}} - 1\right)^2} . \tag{20.53}$$

Equation (20.53) is a transcendental equation in average doping concentration n that can be solved numerically by iteration. Figure 20.18 shows the solutions as function of $C_{\text{HF,min}}/C_{\text{OX}}$ with oxide thickness, and this can be used to obtain the average doping n graphically. Equation (20.53) can be further simplified by neglecting the term $0.5\ln[2\ln(n/n_i) - 1]$, and assuming $C_{\text{OX}} = C_{\text{HF,max}}$ [20.30]. Also, an approximation of (20.53) for the average doping concentration n in unit cm^{-3} is obtained in [20.4] and [20.31] for silicon MOS structures at room temperature, and this is given by

$$\begin{aligned}\log_{10}(n) = 30.38759 &+ 1.68278 \\ &\times \log_{10}(C_{\text{DM}} - 0.03177) \\ &\times [\log_{10}(C_{\text{DM}})]^2 ,\end{aligned} \tag{20.54}$$

where the depletion capacitance (per cm^2 of area) C_{DM} is defined as

$$C_{\text{DM}} = \frac{C_{\text{HF,min}}C_{\text{OX}}}{C_{\text{OX}} - C_{\text{HF,min}}} , \tag{20.55}$$

where all capacitances are in units of F/cm^2.

20.3.2 Doping Profile by High-Frequency and High–Low Frequency Capacitance Methods

The doping profile in the depletion layer can be obtained [20.29, Sect. 9.4] by assuming that the depletion capacitance per unit area C_D and the oxide capacitance per unit area C_{OX} are connected in series; that is, that the measured high frequency capacitance C_{HF} is given by

$$\frac{1}{C_{HF}} = \frac{1}{C_D} + \frac{1}{C_{OX}} \Rightarrow \frac{1}{C_D} = \frac{1}{C_{HF}} - \frac{1}{C_{OX}} . \quad (20.56)$$

For a particular gate biasing V_G of the MOS structure, the depletion thickness $w(V_G)$ is obtained from C_D as

$$w(V_G) = \varepsilon_{Si}\left(\frac{1}{C_{HF}} - \frac{1}{C_{OX}}\right) . \quad (20.57)$$

The doping concentration $n(V_G)$ is given by the slope of the $(1/C_{HF})^2$ versus V_G characteristic, given by

$$n(w) = \frac{-2}{q\varepsilon_{Si}\frac{\partial}{\partial V_G}\left(\frac{1}{C_{HF}^2}\right)} . \quad (20.58)$$

Note that a plot of $1/C_{HF}^2$ versus V_G (Fig. 20.19) can yield important information about the doping profile. The average n is related to the reciprocal of the slope in the linear part of the $1/C_{HF}^2$ versus V_G curve, and the intercept with V_G at a value of $1/C_{OX}^2$ is equal to the flat-band voltage V_{FB} caused by the fixed surface charge Q_{SS} and the gate–semiconductor work function ψ_{MS} [20.3, 30].

Equation (20.58) does not take into account the impact of interface traps, which cause the C–V curve to stretch. The traps are slow and do not respond to the high frequency of the test signal, but they do follow the changes in the gate bias. Therefore, ∂V_G must be replaced with ∂V_{G0} in (20.58), with ∂V_{G0} representing the case when no interface traps are present.

The value of ∂V_{G0} can be obtained by comparing high- and low-frequency (quasi-static) C–V curves for a MOS structure at the same gate biases V_G. Therefore, the ratio $\partial V_{G0}/\partial V_G$ can be found at any gate bias V_G, since the band-bending is the same for both HF and LF capacitances. In [20.29, Sect. 9.4], it is shown that

$$\frac{\partial V_{G0}}{\partial V_G} = \frac{C_{OX} + C_D}{C_{OX} + C_D + C_{IT}} = \frac{1 - C_{LF}/C_{OX}}{1 - C_{HF}/C_{OX}} . \quad (20.59)$$

In this case (20.58) is modified to

$$n(w) = \frac{-2}{q\varepsilon_{Si}\frac{\partial}{\partial V_G}\left(\frac{1}{C_{HF}^2}\right)} \frac{1 - C_{LF}/C_{OX}}{1 - C_{HF}/C_{OX}} \quad (20.60)$$

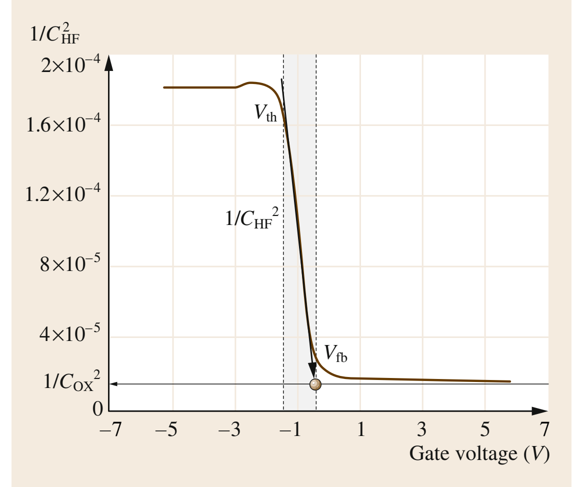

Fig. 20.19 A $1/C_{HF}^2$ versus V_G plot [20.30]. The slope of the *fitted arrow line* is proportional to the average doping, and the *arrow* points to the flat-band voltage V_{FB}, obtained at the V intercept with $1/C_{OX}^2$, shown with the *second horizontal arrow*

as originally proposed in [20.32] and illustrated in Fig. 20.20. As seen from Fig. 20.20, the stretching of the C–V curves due to the interface states induced by stress in Fig. 20.20a causes a disparity in the doping profile in Fig. 20.20b if only the high frequency capacitance is used. The disparity is well-suppressed in Fig. 20.20c by the high–low frequency capacitance measurement, taking into account the stretching of the C–V characteristics. Provided that the depletion layer capacitance is measured at a high frequency, the depletion layer width w is still obtained by (20.57).

Note that the maximum depth w_{max} (20.52) and the resolution Δ_w of the doping profile by means of C–V measurements is limited by the maximum band-bending ψ_{max} and the extrinsic Debye length λ_{Debye}, given by (20.51) and (20.61), respectively, and λ_{Debye} is

$$\lambda_{Debye} = \sqrt{\frac{\varepsilon_{Si}kT}{q^2 n}} . \quad (20.61)$$

The doping profile obtained in this way is reliable for depths w of between $3\lambda_{Debye}$ and $w_{max}/2$, when the MOS structure is in depletion and weak inversion, but not in accumulation. That is, $C_{LF} < 0.7C_{OX}$ as a simple rule. As illustrated in Fig. 20.21, the range of w values between $3\lambda_{Debye}$ and equilibrium, obtained via quasi-static C–V measurements, cover about half-a-decade. With proper corrections, the lower distance decreases

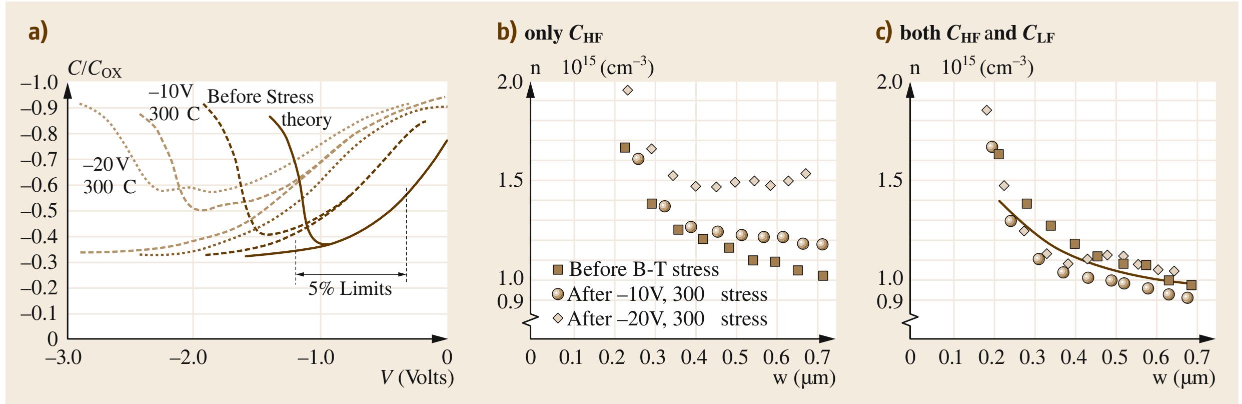

Fig. 20.20a–c C–V curves and doping profiles of a MOS structure with 145 nm oxide and uniform doping of $10^{15}\,\mathrm{cm}^{-3}$ before and after bias temperature stress [20.32]. **(a)** Theoretical and (stretched) measured C–V curves. **(b)** Doping profile deduced from only C_{HF} (see (20.58)); **(c)** Doping profile deduced from both C_{HF} and C_{LF} (see (20.60)). (After [20.32])

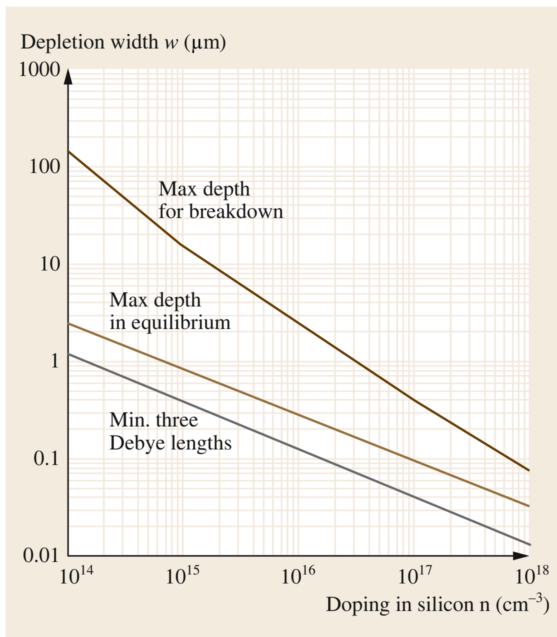

Fig. 20.21 Limitations on the depth achievable when profiling the doping of silicon MOS structures via C–V measurements at room temperature. (After [20.4, p. 86])

to one Debye length [20.30]. Using nonequilibrium (transient) C–V measurements in deep depletion, the profiling can be extended to higher distances by about an order of magnitude, but further limitations can appear due to the high-frequency response of the interface charge, measurement errors, avalanche breakdown in deep depletion, or charge tunneling in highly doped substrates and thin oxides. More details are presented in [20.29].

20.3.3 Density of Interface States

Interface traps change their charge state depending on whether they are filled or empty. Because interface trap occupancy varies with the slow gate bias, stretching of the C–V curves occurs, as illustrated in Fig. 20.20. A quantitative treatment of this *stretch-out* can be obtained from Gauss' law as

$$C_{\mathrm{OX}}(V_{\mathrm{G}} - \psi_{\mathrm{S}}) = -Q_{\mathrm{S}} - Q_{\mathrm{IT}} = -Q_{\mathrm{T}}\,, \tag{20.62}$$

where Q_{S} and Q_{IT} are the surface and interface trap charges (per unit area), which are both dependent on the surface band-bending ψ_{S}, $Q_{\mathrm{T}} = Q_{\mathrm{S}} + Q_{\mathrm{IT}}$ is the total charge in the MOS structure, C_{OX} is the gate capacitance (per unit area), and V_{G} is the bias applied at the gate of the MOS structure. For simplicity, the (gate metal)-to-(semiconductor bulk) potential ψ_{MS} is omitted in (20.62), but in a real structure the constant ψ_{MS} must be subtracted from V_{G}. As follows from (20.62), small changes ∂V_{G} in gate bias cause changes $\partial \psi_{\mathrm{S}}$ in the surface potential bending, and the surface C_{S} and interface trap C_{IT} capacitances (both per unit area) can represent Q_{S} and Q_{IT}, given by

$$C_{\mathrm{OX}}\partial V_{\mathrm{G}} = (C_{\mathrm{OX}} + C_{\mathrm{S}} + C_{\mathrm{IT}})\partial \psi_{\mathrm{S}}\,. \tag{20.63}$$

C_{S} and C_{IT} are in parallel and in series with the C_{OX}, respectively. Therefore, the measured low-frequency capacitance C_{LF} (per unit area) of the MOS structure becomes

$$\begin{aligned} C_{\mathrm{LF}} &= \frac{\partial Q_{\mathrm{T}}}{\partial V_{\mathrm{G}}} = \frac{\partial Q_{\mathrm{T}}}{\partial \psi_{\mathrm{S}}}\frac{\partial \psi_{\mathrm{S}}}{\partial V_{\mathrm{G}}} \\ &= \frac{C_{\mathrm{OX}}\,(C_{\mathrm{S}} + C_{\mathrm{IT}})}{C_{\mathrm{OX}} + C_{\mathrm{S}} + C_{\mathrm{IT}}}\,. \end{aligned} \tag{20.64}$$

Equation (20.64) shows that stretch-out in the C–V curve can arise due to a non-zero value of C_{IT}, which deviates from the ideal case of $C_{IT} = 0$.

According to [20.29, p. 142], D_{IT} is the density of interface states per unit area (cm^2) and per unit energy (1 eV) in units of cm^{-2} eV^{-1}. Since the occupancy of the interface states has a Fermi–Dirac distribution, then upon integrating over the silicon band-gap, the relation between C_{IT} and D_{IT} is

$$C_{IT}(\psi_S) = qD_{IT}(\phi_B + \psi_S) \,, \tag{20.65}$$

where $\phi_B = (k_B T/q)\ln(n/n_i)$ is the shift of the Fermi level from the intrinsic level $\phi_i = (E_c - E_v)/2q$ in the silicon bulk of the MOS structure due to the doping concentration n, and n_i is the thermally generated carrier concentration in silicon. Since the derivative of the Fermi–Dirac distribution is a sharply peaking function, then $C_{IT}(\psi_S)$ at particular ψ_S probes $D_{IT}(\phi_B + \psi_S)$ over a narrow energy range of $k_B T/q$, in which D_{IT} can be assumed to be constant and zero outside this interval. Thus, varying the gate bias V_G, and therefore ψ_S, (20.65) can be used to obtain the density of states D_{IT} at a particular energy shift $q(\phi_B + \psi_S)$ from the silicon intrinsic (mid-gap) energy E_i.

It is evident from (20.64) and (20.65) that the experimental values for D_{IT} can be obtained only when C_{IT}, and ψ_S are determined from C–V measurements. The simplest way to determine ϕ_B is to get the average doping density n using the maximum–minimum high-frequency capacitance method (see (20.53) and Fig. 20.18), or to use the values of n from doping profiles at 0.9 w_{max} – see (20.59) [20.30]. Either the high-frequency or the low-frequency $C-V$ measurement can be used to obtain C_{IT}, but it is necessary to calculate C_S as function of ψ_S, which makes it difficult to process the experimental data.

The most suitable technique for experimentally determining D_{IT} is the combined high–low frequency capacitance method [20.29, Sect. 8.2.4, p. 332]. The interface traps respond to the measurement of low–frequency capacitance C_{LF}, whereas they do not respond to the measurement of the high-frequency measurement C_{HF}. Therefore, C_{IT} can be obtained from measurements by *subtracting* C_{HF} from C_{LF}, given by

$$C_{IT} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{OX}}\right)^{-1} - \left(\frac{1}{C_{HF}} + \frac{1}{C_{OX}}\right)^{-1} . \tag{20.66}$$

Denoting $\Delta C = C_{LF} - C_{HF}$, the substitution of (20.66) into (20.65) provides a direct estimate of D_{IT} from C–V measurements (see also [20.3, p. 371]) as

$$D_{IT} = \frac{\Delta C}{q}\left(1 - \frac{C_{LF}}{C_{OX}}\right)^{-1}\left(1 - \frac{C_{HF}}{C_{OX}}\right)^{-1} \tag{20.67}$$

Note that the combined high–low frequency capacitance method provides C_{IT} and D_{IT} as function of gate bias V_G. However, if D_{IT} needs to be plotted as a function of the position in the energy band-gap, the surface band-bending ψ_S must also be determined as function of gate bias V_G, as follows from (20.65).

There are several ways to obtain the relation between ψ_S and V_G. One way is to create a theoretical plot of C_{HF} versus ψ_S and then, for any choice of C_{HF}, a pair of values for ψ_S and V_G is found [20.29, p. 327]. This method is relatively simple if the doping concentration n in the silicon is uniform and known, because the high-frequency silicon surface capacitance C_S under depletion and accumulation is a simple function of the band-bending ψ_S, and the flat-band capacitance C_{FB} [20.29, pp. 84, 97, 164] is given by

$$C_{FB} = \frac{\varepsilon_{Si}}{\lambda_{Debye}} = \sqrt{\frac{\varepsilon_{Si} q^2 n}{k_B T}} \tag{20.68}$$

$$C_S(\psi_S) \approx \begin{cases} \frac{C_{FB}}{\sqrt{2}} \frac{\exp\left(\frac{q\psi_S}{k_B T}\right) - 1}{\sqrt{\exp\left(\frac{q\psi_S}{k_B T}\right) - \frac{q\psi_S}{k_B T} - 1}} \,, \\ \quad \psi_S > 0 \text{ in accumulation} \\ C_{FB},\ \psi_S = 0 \text{ at flat band,} \\ \frac{C_{FB}}{\sqrt{2}} \frac{1 - \exp\left(\frac{q\psi_S}{k_B T}\right)}{\sqrt{\exp\left(\frac{q\psi_S}{k_B T}\right) - \frac{q\psi_S}{k_B T} - 1}} \,, \\ \quad \psi_S < 0 \text{ in depletion} \,. \end{cases} \tag{20.69}$$

Since C_S is in series with C_{OX}, then the theoretical C_{HF} is obtained as a function of the band-bending ψ_S by

$$\frac{1}{C_{HF}(\psi_S)} = \frac{1}{C_{OX}} + \frac{1}{C_S(\psi_S)} \tag{20.70}$$

For a uniformly doped silicon with SiO_2 as the insulator, the ratio $C_{HF}(V_{FB})/C_{OX}$ at gate bias for flat-band conditions is given [20.3, p. 349] by

$$\frac{C_{HF}(V_{FB} \text{ or } \psi_S = 0)}{C_{OX}} = \frac{1}{1 + \frac{136\sqrt{T/300}}{t_{ox}\sqrt{n}}} \,, \tag{20.71}$$

where t_{ox} is the oxide thickness (cm), n is the doping (cm^{-3}), and the T is the temperature (K).

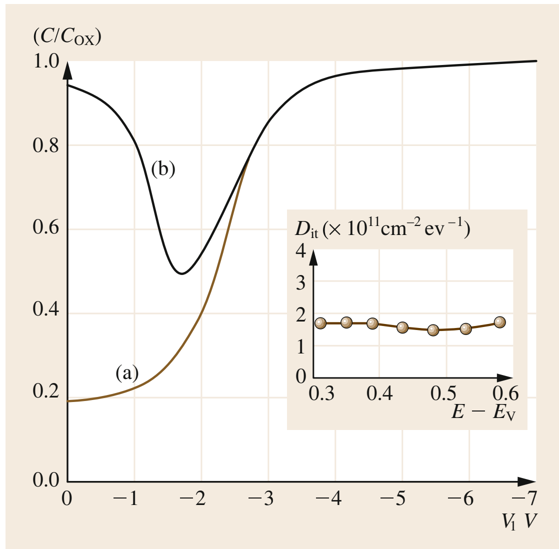

Fig. 20.22 Results from the combined high–low frequency capacitance method [20.33]. *(a)* High-frequency *C–V* curve; *(b)* low-frequency *C–V* curve. The energy profile for the density of interface states D_{IT} is shown in the *inset*, as calculated by (20.65), (20.67) and (20.72)

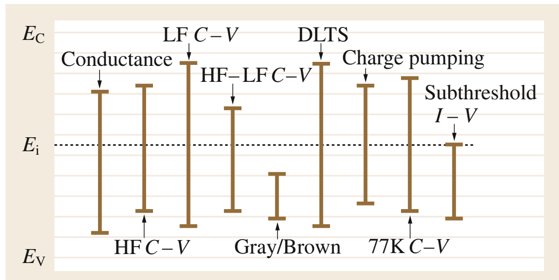

Fig. 20.23 Energy ranges in the silicon band-gap of a p-type substrate over which the density of interface traps can be determined using various measurement methods and characterization techniques. (After [20.3, p. 104])

It was demonstrated in [20.29] that the method of using a theoretical plot to obtain the relation between ψ_S and V_G works well in the case of uniformly doped silicon even if only high-frequency *C–V* measurements are used to obtain the density of states; that is, the $1/C_{HF}^2$ versus V_G plot is almost a straight line. However, with substrates that are not uniformly doped, the method is inconvenient because the corrections in (20.68) and (20.69) are difficult to implement. Therefore, in practice, a method based on low-frequency *C–V* measurement is preferred [20.30].

Low-frequency *C–V* measurement was first used to obtain the relation between ψ_S and V_G [20.34]. This method is based on the integration of (20.66) from an initial gate bias V_{G0}, arbitrarily chosen either under strong accumulation or strong inversion, to the desired V_G at which the band-bending $\psi_S(V_G)$ is to be obtained. Since C_{IT} is part of (20.66), then the low-frequency *C–V* curve [20.29, p. 93] is integrated as

$$\psi_S(V_G) = \psi_{S0} + \int_{V_{G0}}^{V_G} \left(1 + \frac{C_{LF}(V_G)}{C_{OX}}\right) dV_G \,. \qquad (20.72)$$

The value of ψ_{S0} is selected such that $\psi_S(V_{FB}) = 0$ when integrating from V_{G0} to the flat-band gate voltage V_{FB}. In this case, V_{FB} is usually obtained beforehand from the point of V-intercept with $1/C_{OX}^2$ when extrapolating the linear part of the $1/C_{HF}^2$ versus V_G curve toward the V_G axis (Fig. 20.19). After determining ψ_{S0}, (20.72) provides the relation between ψ_S and V_G. Thus, the density of states D_{IT} obtained from (20.67) as function of V_G using the combined high–low frequency capacitance method can be plotted against the position of D_{IT} in the silicon band gap, as given by (20.65). High and low frequency *C–V* measurements can therefore be used to plot the data, as illustrated in the insert of Fig. 20.22.

Overall, many different techniques are used to determine the density of states D_{IT} (Fig. 20.23). For some of these techniques, the ability to sense the energy position of D_{IT} in the band-gap of silicon is summarized in [20.3]. Most of them use *C–V* measurements, but others are based on *I–V* measurements taken during the subthreshold operation of MOS transistors, deep-level transient spectroscopy (DLTS), charge pumping (CP) in a three-terminal MOS structure, cryogenic temperature measurements, and so on. Each technique has its strengths and weaknesses, which are discussed in [20.3, 35].

In the methods discussed above, it has been assumed that the gate bias V_G varies slowly with time, 20–50 mV/s, and that the MOS structure is in equilibrium; that is, the minority carriers are generated and the inversion layer is readily formed in the MOS structure when V_G is above the threshold. However, the time constant for minority carrier generation is high in silicon (≈ 0.1 s or more), and it is possible to use nonequilibrium high-frequency *C–V* measurements to further analyze the properties of the MOS structure. Some applications of these methods are presented later.

20.4 Current–Voltage Measurements

20.4.1 *I–V* Measurements on a Simple Diode

Current–voltage measurements of mainstream semiconductor devices are perhaps the simplest and most routine measurements performed, and they can provide valuable information about the quality of materials used. For example, if we consider the *I–V* characteristics of a p-n diode structure, the source–substrate or drain–substrate junctions can provide useful information on the quality of the junction, such as whether defects are present (they give rise to generation–recombination currents or large parasitic resistances for the contacts at the source, drain or substrate terminals).

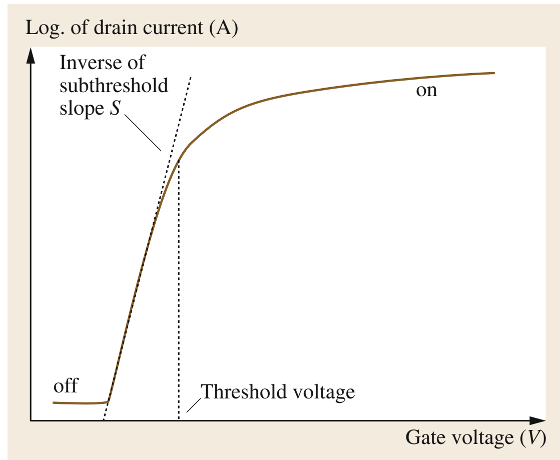

Fig. 20.24 Typical subthreshold characteristics of a MOSFET. The interface state density can be extracted from S

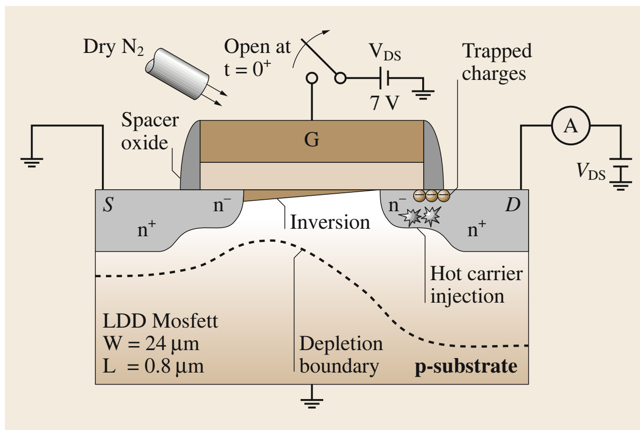

Fig. 20.25 Schematic diagram showing the set-up used for floating gate measurements. The area where charge is trapped after hot electrons are applied is shown

This is easily seen from the current–voltage relation given by the sum of the diffusion (I_{DIFF}) and recombination (I_{GR}) currents

$$I_D = I_{DIFF} + I_{GR} = I_{D0}\left[\exp\left(\frac{eV_D}{nk_BT}\right) - 1\right] + I_{GR0}\exp\left(\frac{eV_D}{2k_BT}\right) \tag{20.73}$$

where I_{D0} and I_{GRO} are the zero-bias diffusion and recombination currents respectively, n is an ideality factor (typically 1), and V_D is the voltage across the intrinsic diode, which is given by

$$V_D = V_{applied} - I_D R_{parasitic} . \tag{20.74}$$

For (20.73), a plot of $\ln(I_D)$ versus V_D allows us to separate out the diffusion and the recombination current components. From (20.73) and (20.74), we can also use the diode's *I–V* characteristics to determine the parasitic resistance in series with the intrinsic diode, as described in detail in [20.36]. In most cases, this $R_{parasitic}$ is dominated by the contact resistance.

20.4.2 *I–V* Measurements on a Simple MOSFET

Simple current–voltage measurements – drain current versus gate voltage (I_{DS}–V_{GS}), and I_{DS} versus drain voltage (V_{DS}) – are routinely taken on MOSFETs in order to study their electrical characteristics; however, these can also be used to obtain useful information on the quality of the semiconductor, contacts, oxide and semiconductor–oxide interface. For example, the $I_{DS} - V_{GS}$ characteristics at very small V_{DS} biases (linear region of operation) for a set of test transistors of fixed channel width and different channel lengths is often used to extract parameters such as the threshold voltage (V_T), the transconductance (g_m), the intrinsic mobility (μ_o) and the mobility degradation coefficients θ_0 and η, the parasitic source (R_S) and the drain resistances (R_D) in series with the intrinsic channel, the channel length reduction ΔL, the output conductance (g_{DS}) and the subthreshold slope (S) [20.37].

These parameters are required for modeling and they directly impact the device's performance. However, some of these parameters can also be used to assess the quality of the silicon–silicon dioxide (Si–SiO_2) interface [20.38, 40]. For example, interface states at the Si–SiO_2 interface can change the threshold voltage,

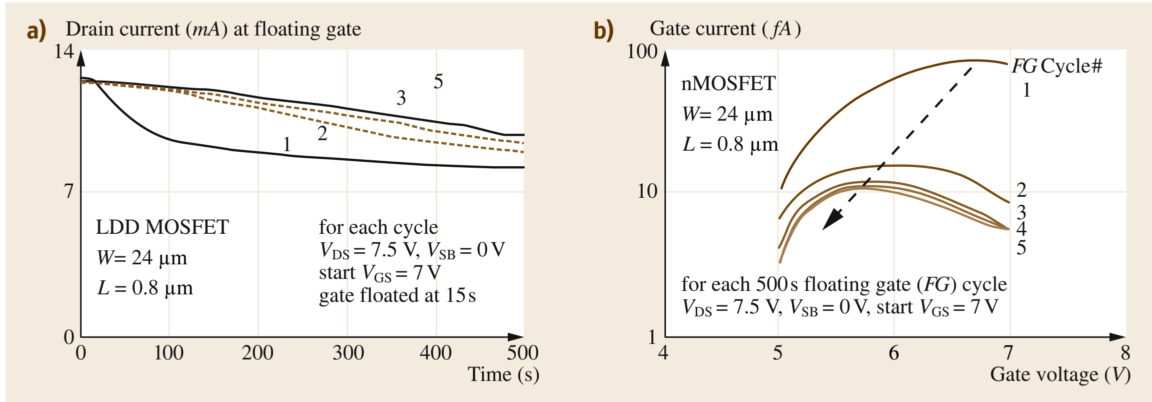

Fig. 20.26 **(a)** Evolution of the drain current over five floating gate cycles. Biasing conditions were chosen to maximize hot-electron gate currents. Note that the maximum drop in drain current occurs after the first floating gate cycle. **(b)** Extracted gate currents using (20.78) and the measurements in **(a)**. As with the drain current, the maximum change in gate current occurs between floating gate cycles 1 and 2. The shift in the peak of the gate current is explained in [20.38, 39]

the subthreshold slope and the mobility, all of which will impact on the drain–source (I_{DS}) current flowing through the device. Here, we look at one parameter in more detail – the subthreshold slope S in mV (of V_{GS})/decade (of I_{DS}).

First, the interface trap density (D_{IT}) can be determined from a semi-log plot of $I_{DS} - V_{GS}$ characteristics at very low drain biases, as shown in Fig. 20.24. We start with the expression for the subthreshold slope

$$S = \frac{k_B T}{q} \ln(10) \left(1 + \frac{C_D + C_{IT}}{C_{OX}}\right) \tag{20.75}$$

in which

$$C_D = \frac{q\varepsilon_{Si} N_A}{\sqrt{2\psi + |V_B| - \frac{k_B T}{q}}} \tag{20.76}$$

D_{IT} can then be calculated from

$$C_{IT} = qD_{IT} \tag{20.77}$$

once C_{IT} is determined from (20.75). In fact, a recent comparison in [20.41] of the interface trap densities extracted from capacitance, subthreshold and charge pumping measurements produced similar results, demonstrating that simple and fast I–V measurements based on the subthreshold technique can provide useful information on the Si–SiO_2 quality.

20.4.3 Floating Gate Measurements

The floating gate technique is another simple I–V measurement in which the evolution of the drain current I_{DS} is monitored after the gate bias has been removed. It has been shown to be particularly useful when monitoring early-mode hot-carrier activity in MOS transistors [20.39, 41]. In this measurement, we first check the oxide quality by biasing the transistor in the strong linear region (very low V_{DS} and a V_{GS} well above V_T), and then lift the gate voltage probe so that $V_{GS} = 0\,V$ and measure the evolution of I_{DS} with time. For a high-quality gate and spacer oxide, I_{DS} remains constant for a long time, indicating that there is negligible carrier injection across the gate oxide through Fowler–Nordheim tunneling or other leakage mechanisms.

A second precaution is to have a dry or inert gas such as nitrogen flowing over the chip to reduce the possibility of other leakage mechanisms such as that from water vapor. The measurement set-up for this experiment is shown in Fig. 20.25. The evolution of the floating gate current over several cycles with the gate voltage applied and then removed is shown in Fig. 20.26. The biasing voltages and time at which the gate is floated are also given in Fig. 20.26a. For this experiment, a biasing condition of $V_{GS} \approx V_{DS}$ was chosen for a high-impact ionization-induced gate current, but a lower-than-maximum electron injection situation was used for the initial biasing condition.

From the evolution of I_{DS} and the $I_{DS} - V_{GS}$ characteristics of a virgin (not intentionally stressed) transistor at the same V_{DS} as the floating gate measurements, and from measurements of the total capacitance associated with the gate (C_G), the gate current (I_G) evolution after each floating gate cycle can be determined using

$$I(V_{GS}) = C_G \frac{dV_{GS}}{dt} \,. \tag{20.78}$$

This $I_G - V_{GS}$ evolution is shown in Fig. 20.26b. An ancillary benefit of the floating gate technique

is that very small gate currents (in the fA range or even smaller) can be easily determined by measuring much larger drain currents using, for example, a semiconductor parameter analyzer. The reason for this is that the gate current is not directly measured in this technique – it is determined from $I_{DS} - V_{GS}$ and (20.78). Also, the change in the floating gate current after the first few cycles can be used to monitor for early mode failure after statistical evaluation.

20.5 Charge Pumping

Charge pumping (CP) is another electrical technique that is well suited to studying semiconductor–insulator interfaces in MOSFETs [20.42–47]. There are several versions of the CP technique: spatial profiling CP [20.43–47], energy profiling CP [20.48], and, more recently, new CP techniques [20.49] that permit the determination of both interface states (N_{IT}) and oxide traps (N_{OT}) away from the interface and inside the oxide. The charge pumping technique is more complicated than either of the I–V or floating gate methods. However, it is a very powerful technique for assessing interface quality and it works well even with very small transistor geometries and very thin gate oxides, where tunneling can be a problem.

The charge pumping technique was first used in 1969 [20.50] to measure the interface traps at $Si-SiO_2$ interface. Since then, there have been numerous publications with enhancements, refinements and applications of the technique to a variety of semiconductor–insulator interfacial studies. In the basic charge pumping experiment, the gate of an NMOST (for example) is pulsed from a low value (V_L) when the device is in accumulation to a high value (V_H) when the device is in inversion. This results in the filling of traps between $E_{F,ACC}$ (corresponding to V_L) and $E_{F,INV}$ (corresponding to V_H) with holes and electrons, respectively. When pulsing the gate between accumulation at V_L and inversion at V_H, a current flows due to the repetitive recombination at the interface traps of minority carriers from the source and drain junctions with majority carriers from the substrate. This current is termed the charge pumping current, and it was found to be proportional to the frequency of the gate pulse, the gate area and the interface state density. Its sensitivity is better than $10^9\,cm^{-2}\,eV^{-1}$. In the traditional CP experiment shown in Fig. 20.27, but with $\Delta V_S = |V_D - V_S| = 0\,V$, the gate G is connected to a pulse generator, a reverse bias V_R or no bias is applied to both sources S and drain D terminals, and the charge pumping current flowing in the substrate terminal, I_{CP}, is measured. To generate a typical charge pumping curve (as shown in the top part of Fig. 20.28), the base level of the pulse is varied, taking the transistor from below flat-band to above surface inversion conditions, as shown in the bottom part of Fig. 20.28.

In the traditional CP experiment, the charge pumping current I_{CP} is given by

$$I_{CP} = qA_{GATE}\overline{D_{IT}}\Delta E\,, \quad (20.79)$$

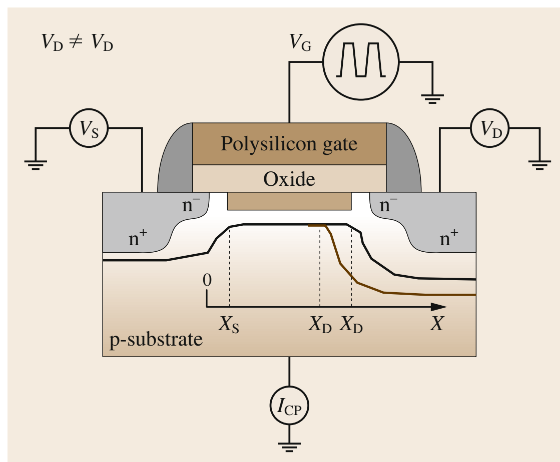

Fig. 20.27 Example of spatial profiling charge-pumping set-up used when the source and drain biases are slightly different

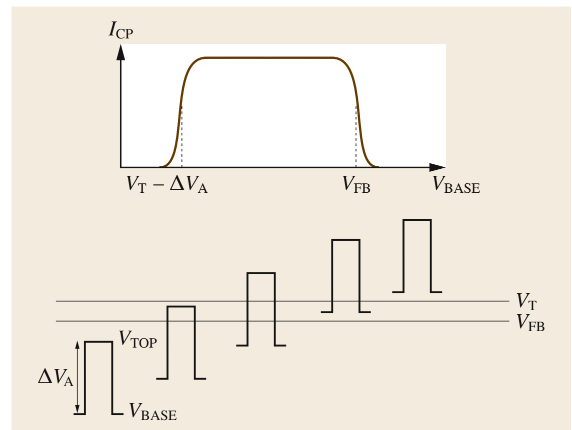

Fig. 20.28 Demonstration of how the CP curve is generated by varying the base level of the pulse so that the entire pulse is between V_{FB} and V_T

where

$$\Delta E = (E_{F,INV} - E_{F,ACC}) . \quad (20.80)$$

This expression assumes that the electrical and physical channel lengths are the same. However, for short channel devices, this assumption results in an error. Therefore, a more accurate expression is

$$I_{CP} = qfW \int_{x_s}^{x_d} N_{IT}(x)(q\Delta\psi_{SO}) \quad (20.81)$$

$$x_d = L - \sqrt{\frac{2\varepsilon_{Si}}{qN}} \left(\sqrt{V_D + \psi_S} - \sqrt{\psi_S}\right) . \quad (20.82)$$

The interface state density at the edge of the drain depletion region ($N_{IT}(x_d)$) is given by

$$N_{IT}(x_d) = \frac{1}{qfWq\Delta\psi_{S0}} \left(\frac{dx_s}{dV_S}\right)^{-1} \left(\frac{dI_{CP}}{dV_S}\right)_{V_D=\text{constant}} \quad (20.83)$$

When performing spatial profiling CP experiments, some precautions are required. The first is that a voltage difference ΔV_S between V_D and V_S that is too small results in a difference in I_{CP} that is too small as well, and hence a large error in $N_{IT}(x)$, as indicated from (20.83). On the other hand, values of ΔV_S that are too large result in a I_D that is too high and hence more substrate current I_B. This current I_B can interfere with I_{CP} if ΔV_S is large or if L is very short, resulting in a large error in $N_{IT}(x)$. The range 50–100 mV for ΔV_S seems to be a good compromise for the devices investigated in [20.43, 44]. Experimental results for spatial profiling CP measurements indicate that $N_{IT}(x)$ peaks near S/D edges. However, after normal mode stress, $N_{IT}(x)$ only increases near D. This is shown in Fig. 20.29. More details about charge pumping can be found in a recent review [20.51].

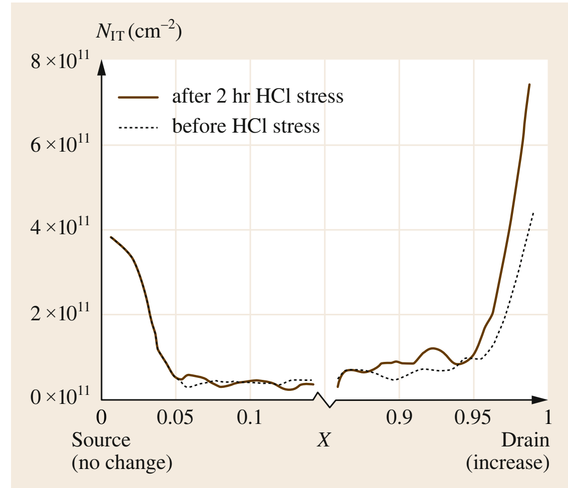

Fig. 20.29 Spatial interface state distribution over the channel in a 1 µm-long device. The stress was applied for 2 h at $V_{DS} = 5$ V and $V_{GS} = 2.4$ V

20.6 Low-Frequency Noise

20.6.1 Introduction

Low-frequency noise (LFN) spectroscopy requires very good experimental skills in the use of low-noise instrumentation as well as grounding and shielding techniques. Other special considerations are also required, which are discussed later. Although it is time-consuming to perform, it has been widely used to probe microscopic electrical transport in semiconductors and metals. LFN is very sensitive to defects in materials and devices, and large differences in LFN characteristics can be observed in devices with identical electrical current–voltage characteristics. This is mainly because electrical I–V measurements only probe the average or macroscopic transport in devices and so are not as sensitive to defects as LFN. Due to its sensitivity to defects, traps or generation–recombination centers, LFN has been proposed as a good tool for predicting device reliability. For example, LFN has been used to predict the reliabilities of metal films [20.52], and has been used in processing steps that produce photodetectors with better performance [20.53, 54]. LFN noise is sensitive to both bulk and surface defects or contaminants of a material.

Using low-frequency noise spectroscopy and biasing the transistor in saturation, we can spatially profile the defect density near the drain and source terminals for devices in normal and reverse modes of operation [20.55]. Low-frequency noise in the linear region also allows us to extract the average defect density over the entire channel region at the silicon–silicon dioxide interface [20.56, 57]. Noise experiments were performed on small-geometry polysilicon emitter bipolar transistors to investigate the number of interface states in the thin interfacial oxide layer between the monocrystalline and polycrystalline silicon [20.58–

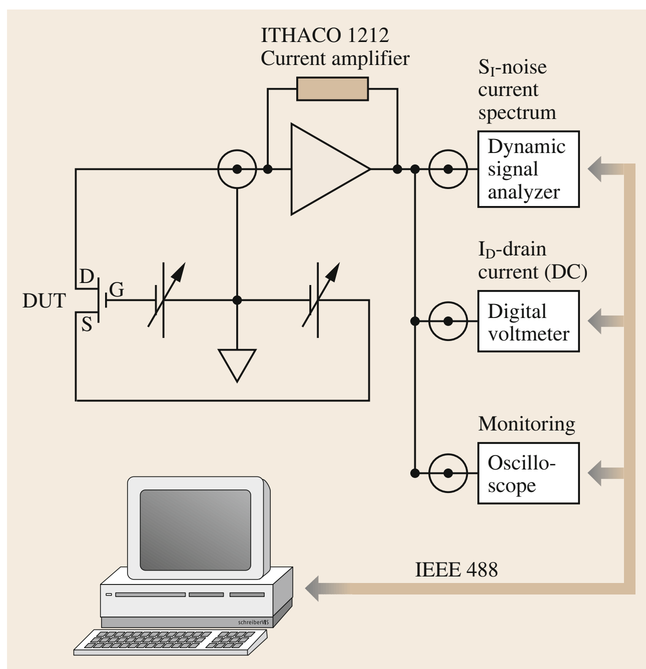

Fig. 20.30 System for measuring low-frequency noise. In this diagram, the device under test is any field-effect or thin-film transistor

68]. Recent experiments using body or substrate bias (V_B) in a MOS transistor allowed us to look at the contribution of bulk defects (defects away from the silicon–silicon dioxide interface) and their contribution to device noise [20.69–71]. This is important since substrate biasing has been proposed as a means to cleverly manage power dissipation and speed in emerging circuits and systems [20.72].

We will discuss how low-frequency noise (LFN) spectroscopy can be applied to the interfacial oxide layer between the mono-silicon and polysilicon emitter in bipolar junction transistors (BJTs) here. The experimental system shown in Fig. 20.30 is used for LFN measurements of field-effect transistors (FETs); the same system can also be used for BJTs.

As mentioned before, special attention must be paid to grounding and shielding in LFN measurements, as this is crucial to minimizing the effects of experimental and environmental noise sources on the device under test (DUT). Because electric power supplies are noisy, especially at 60 Hz (in North America) and its harmonics, and this noise can dominate the noise of the DUT, batteries are often used to supply the voltage. Metal film resistors are the preferred means of changing the biasing conditions, because of their better low-noise characteristics compared to carbon resistors, for example.

With these experimental precautions taken, the noise signal from the transistor might still be too low to be directly measured using a spectrum or signal analyzer. Therefore, a low-noise voltage or current amplifier, whose input noise sources are lower than that of the noise signal, is used to boost the noise signal. In addition, other instruments might be used to measure currents or voltages, or to display the waveforms (as shown in Fig. 20.30). An example of a low-frequency noise characterization system that we have used to study the noise in thin film polymer transistors is shown in Fig. 20.30. Note that LFN measurements are time intensive because a large number of averages are required for smooth spectra. Also, in noise measurements, the power spectrum densities S_V and S_I for the noise voltages and currents are measured, in units V^2/Hz and A^2/Hz, respectively.

20.6.2 Noise from the Interfacial Oxide Layer

Here we present some sample results and show how low-frequency noise spectra in ultrasmall devices can

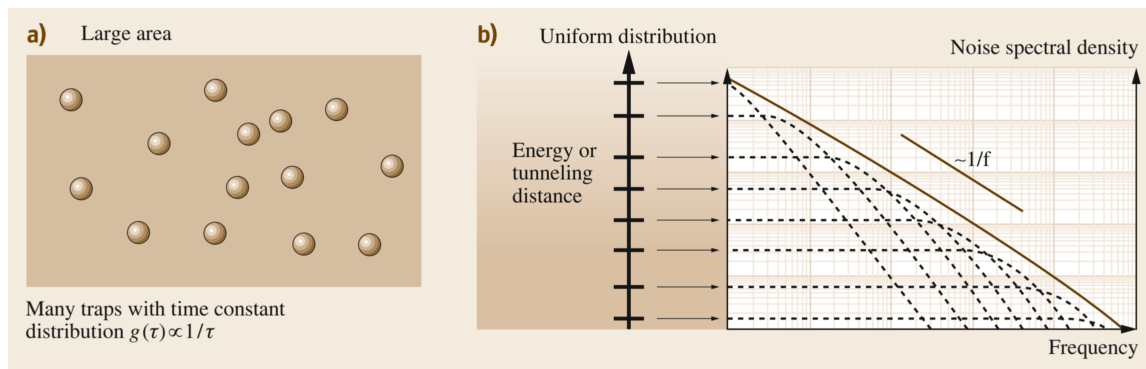

Fig. 20.31 Schematic representation of a *large*-area PE-BJT with many traps distributed uniformly across the band gap and the emitter area, and with a $g(\tau) = 1/\tau$ distribution for the time constant. The resulting spectrum is $1/f$ noise

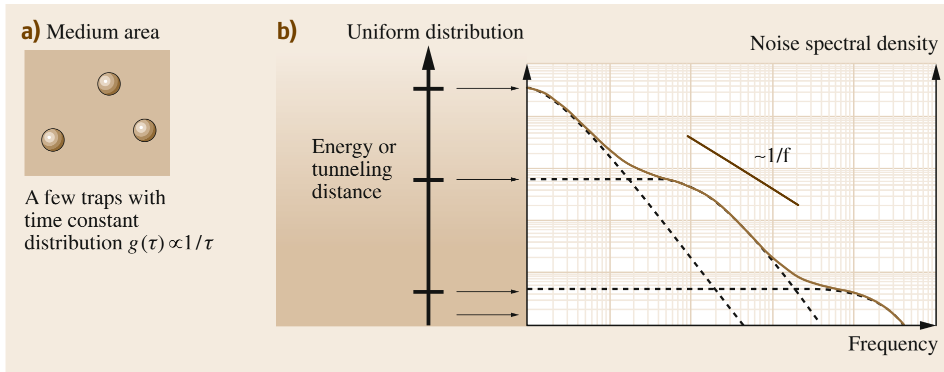

Fig. 20.32 Schematic representation of a *medium*-area PE-BJT ($\approx 0.5\,\mu m^2$) with a few traps. Note that g–r bumps appear for each trap since there are only a few traps

be used to estimate the oxide trap density. Generally, the low-frequency noise spectra of polysilicon emitter (PE) BJTs are made up of $1/f$ noise, generation–recombination (g–r) noise and shot noise sources. In the case of the base current, the noise spectra can be modeled as

$$S_{I_B} = \frac{K_F I_B^{A_F}}{f} + \sum_{i=1}^{n} \frac{B_i \tau_i}{1 + (2\pi f \tau_i)^2} + 2qI_B \,, \qquad (20.84)$$

where the symbols have their usual meanings, see [20.68] for example.

As described in [20.63–68], the LFN in PE BJTs originates from the thin layer of oxide between the monocrystalline and polycrystalline silicon emitter. The defects at this interface may be dangling oxygen bonds, oxygen vacancies, interface states or oxide traps [20.63]. Devices with large emitter areas have many traps, and these produce generation–recombination noise which produce $1/f$ noise when added. This is schematically shown in Fig. 20.31.

As the device area is reduced, and assuming a constant trap density (which is normally true for devices on the same wafer), then there are fewer traps in the interfacial oxide layer for smaller area devices. In this case, the spectral density of the noise changes and it gains characteristic *bumps* associated with resolvable g–r noise components. This is schematically shown in Fig. 20.32.

In very small devices with only a single trap, for example, the noise spectrum changes dramatically; only g–r noise is observed in the frequency domain along with a random telegraph signal (RTS) in the time domain. This is schematically shown in Fig. 20.33. Real experimental results are shown for three sizes of transistors (2.4, 0.64 and $0.16\,\mu m^2$) in Fig. 20.34. Here, one can see how $1/f$ noise is made up of g–r spectra as the emitter geometries are scaled to smaller and smaller values. For the PE BJT with an emitter area of $0.16\,\mu m^2$, a lower bound of $\approx 10^9\,cm^2$ can be approximated for the oxide trap density. Similar results have been obtained for MOSFETs [20.73].

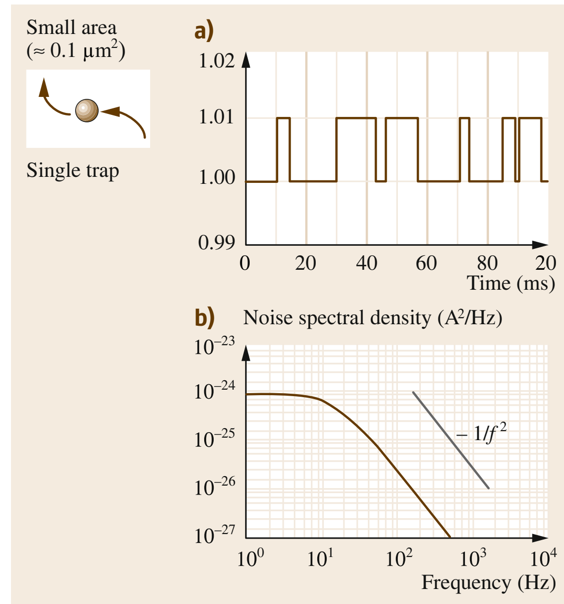

Fig. 20.33 Schematic representation of a *small*-area PE-BJT ($\approx 0.1\,\mu m^2$) with one trap. Note that **(a)** a single RTS and **(b)** g–r spectrum appear because there is only one trap

20.6.3 Impedance Considerations During Noise Measurement

Two basic circuits can be employed when measuring the low-frequency noise (LFN) in a device. These configurations are sketched in Fig. 20.35. In voltage noise measurement (Fig. 20.35a), a low-noise preamplifier senses the voltage across the device, and this signal is sent to a spectrum analyzer or a fast Fourier transform (FFT) analyzer. In current noise measurements (Fig. 20.35b), the low-noise preamplifier senses the current through the device, converts it into a voltage,

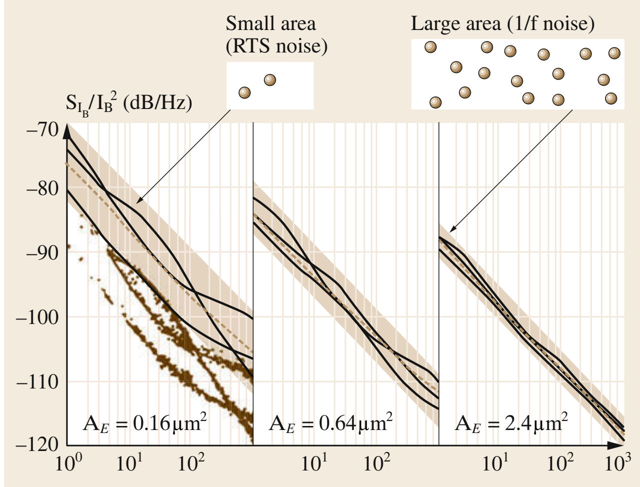

Fig. 20.34 Experimental results for low-frequency noise spectra from sets of large-, medium- and small-area PE-BJTs. In all cases, the average spectrum is $1/f$ noise and the relative magnitude of the $1/f$ noise is the same; that is, the area of $K_F\times$ is the same for the three sets of transistors. (After [20.59–62])

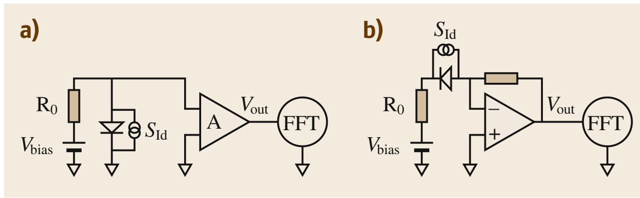

Fig. 20.35a,b Basic circuits used to measure the low-frequency noise (LFN) in a device (DUT). **(a)** Voltage noise measurement; **(b)** current noise measurement

and forwards the voltage to a FFT or spectrum analyzer.

In principle, both configurations can be used for LFN measurement, but the impact of the nonideality of the amplifier (such as the input impedance, noise voltage and current) changes when the device impedance changes. Also, the noise from the bias source varies with each measurement set-up.

The noise equivalent circuit used for voltage measurement is shown in Fig. 20.36. The noise from the amplifier is represented by the input-referred noise voltage ($S_{V\mathrm{n}}$) and noise current ($S_{I\mathrm{n}}$) sources. The noise voltage from the bias is represented by S_{V0}. The impedance of the bias source is R_0, whereas the input impedance of the amplifier is neglected, since it is usually very high compared to R_0. The impedance of DUT is r_d. The noise current $S_{I\mathrm{d}}$ of the device that can be measured, assuming that the noise voltage at the input of the amplifier $S_{V\mathrm{m}} = S_{I\mathrm{d}} r_\mathrm{d}^2$. However, the amplifier sees

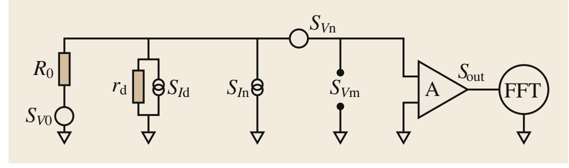

Fig. 20.36 Noise equivalent circuit for voltage noise measurements

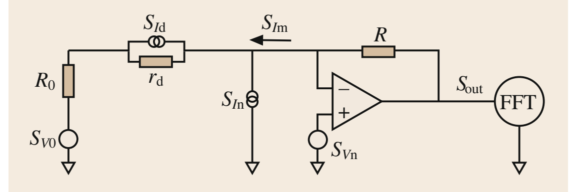

Fig. 20.37 Noise equivalent circuit of the current noise measurement

a different level of $S_{V\mathrm{m}}$, given by

$$S_{V\mathrm{m}} = \frac{S_{\mathrm{OUT}}}{A^2} = S_{V0}\left(\frac{r_\mathrm{d}}{r_\mathrm{d}+R_0}\right)^2 + S_{V\mathrm{n}} + (S_{I\mathrm{I}} + S_{I\mathrm{I}})Z^2 \quad (20.85)$$

where

$$Z = (r_\mathrm{d}//R_0) = \frac{r_\mathrm{d} R_0}{r_\mathrm{d}+R_0} \quad (20.86)$$

and A is the voltage gain of the amplifier. Therefore, the estimated value for $S_{I\mathrm{d}}$ is

$$S_{I\mathrm{d}} = \frac{S_{V\mathrm{m}} - S_{V\mathrm{n}}}{Z^2} - \frac{S_{V0}}{R_0^2} - S_{I\mathrm{n}} \,. \quad (20.87)$$

The uncertainty in (20.87) is

$$\frac{\Delta S_{I\mathrm{d}}}{S_{I\mathrm{d}}} = \frac{\Delta S_{V\mathrm{n}}}{S_{V\mathrm{m}}} + \frac{\Delta S_{V0}}{S_{V\mathrm{m}}}\left(\frac{Z}{R_0}\right)^2 + \frac{\Delta S_{I\mathrm{n}}}{S_{V\mathrm{m}}} Z^2 \quad (20.88)$$

where $\Delta S \leq S$ denotes the uncertainty in each noise source. As seen from (20.88), the impact of the bias source noise ΔS_{V0} and the input current noise $\Delta S_{I\mathrm{n}}$ can be reduced if the impedance of the measurement circuit Z is low and the ratio r_d/R_0 is kept much less than 1; in other words, the *voltage noise measurement is more appropriate for low-impedance devices, such as diodes at forward biasing*, and the noise floor of the measurement is limited by the input-referred voltage noise S_{V_n} of the amplifier.

For the other (dual) case, current noise measurement, the noise equivalent circuit is shown in Fig. 20.37. The corresponding equations for the measured noise

current $S_{I\text{m}}$, Z, the device noise $S_{I\text{d}}$, and the uncertainty, respectively, are given by (20.89–20.92) below

$$S_{I\text{m}} = \frac{S_{\text{OUT}}}{R^2} = \frac{S_{V0}}{(r_\text{d}+R_0)^2} S_{I\text{n}} + \frac{S_{V\text{n}}}{Z^2} + S_{I\text{d}} \left(\frac{r_\text{d}}{r_\text{d}+R_0}\right)^2 \tag{20.89}$$

$$Z = (r_\text{d}+R_0)//R = \left(\frac{1}{R} + \frac{1}{r_\text{d}+R_0}\right)^{-1} \tag{20.90}$$

$$S_{I\text{d}} = (S_{I\text{m}} - S_{I\text{n}}) \left(1+\frac{R_0}{r_\text{d}}\right)^2 - \frac{S_{V0}}{r_\text{d}^2} - \frac{S_{V\text{n}}}{Z^2}\left(1+\frac{R_0}{r_\text{d}}\right)^2 \tag{20.91}$$

$$\frac{\Delta S_{I\text{d}}}{S_{I\text{d}}} = \frac{\Delta S_{I\text{n}}}{S_{I\text{m}}} + \frac{\Delta S_{V0}}{S_{I\text{m}}} \frac{1}{(r_\text{d}+R_0)^2} + \frac{\Delta S_{V\text{n}}}{Z^2 S_{I\text{m}}} \tag{20.92}$$

As expected from duality, it is apparent from (20.92) that the impact of the bias source noise ΔS_{V0} and the input voltage noise $\Delta S_{I\text{n}}$ can be reduced if the impedance of the measurement circuit Z and $(r_\text{d}+R_0)$ are both high; in other words, the *current noise measurement is more appropriate for high-impedance devices, such as diodes at reverse biasing*, and the noise floor of the measurement is limited by the input-referred current noise S_{I_n} of the amplifier.

This analysis above demonstrates that the choice of the measurement configuration follows our expectation that voltage should be measured in low-impedance devices and current in high-impedance devices. Also, the noise floor limiting parameter of the preamplifier is of the same type as the type of measurement; that is, input-referred noise voltage for voltage noise measurement and input-referred noise current for current noise measurement. Note that there is a trade-off between the voltage and current noise in amplifiers, which implies that the measurement configuration – either voltage or current measurement – should also be carefully selected with respect to the impedance of the device under test. In addition, four-point connection can be used to measure the noise in very low impedance devices ($r_\text{d} <$ 100). These and other considerations for low-frequency noise instrumentation are discussed in many papers, for example [20.74–76].

20.7 Deep-Level Transient Spectroscopy

Deep-level transient spectroscopy (DLTS) is a fairly complicated electrical characterization technique where the temperature is varied in large range from cryogenic temperatures ($< 80\,\text{K}$) to well above room temperature ($> 400\,\text{K}$). However, it is a powerful and versatile technique for investigating deep-level defects and it also gives accurate values for the capture cross-sections of defects. There are several DLTS techniques and [20.77, 78] provide recent reviews of the subject. In DLTS, the semiconductor device or junction is pulsed with an appropriate signal, and the resulting transient (such as capacitance, voltage or current) is monitored at different temperatures. Using these recorded transients at different temperatures, it is possible to generate a spectrum with peaks, each of which is associated with a deep level. The heights of the peaks are proportional to the defect density.

Here, we will focus on a new version of DLTS: the constant resistance (CR) DLTS technique [20.79–81]. We were able to accurately investigate bulk defects in a variety of test structures with CR-DLTS. Using body bias in a MOS transistor, we were able to distinguish interfacial and bulk defects that are important for different applications. For example, interfacial defects are important for electronic applications, and bulk defects are important for imaging or radiation detection applications. Examples of results from DLTS studies with and without body bias will be discussed.

CR-DLTS is well-suited to investigations of electrically active point defects that are responsible for the creation of deep levels in the semiconductor band-gap. CR-DLTS can also be used to distinguish bulk traps and interface traps in MOSFETs.

A conventional DLTS system is shown schematically in Fig. 20.38. In DLTS, an excitation pulse is applied to the sample to fill all of the traps and then the pulsing is stopped. The next step is to detect the transient signal from the sample due to charge emission from the traps. The right side of Fig. 20.38 shows capacitance transients at eight different temperatures. By selecting a time window from t_1 to t_2, and then plotting $[C(t_1) - C(t_2)]$ as a function of temperature, a DLTS spectrum with a characteristic peak is obtained as shown in the bottom of Fig. 20.38.

This peak is a signature from a specific defect level. To determine the properties of the defect (its energy level and capture cross-section), the time window ($\tau = t_2 - t_1$) is changed. In this case, different DLTS spectra are obtained at different temperatures. Using the time difference τ and the temperatures at which the peaks occur,

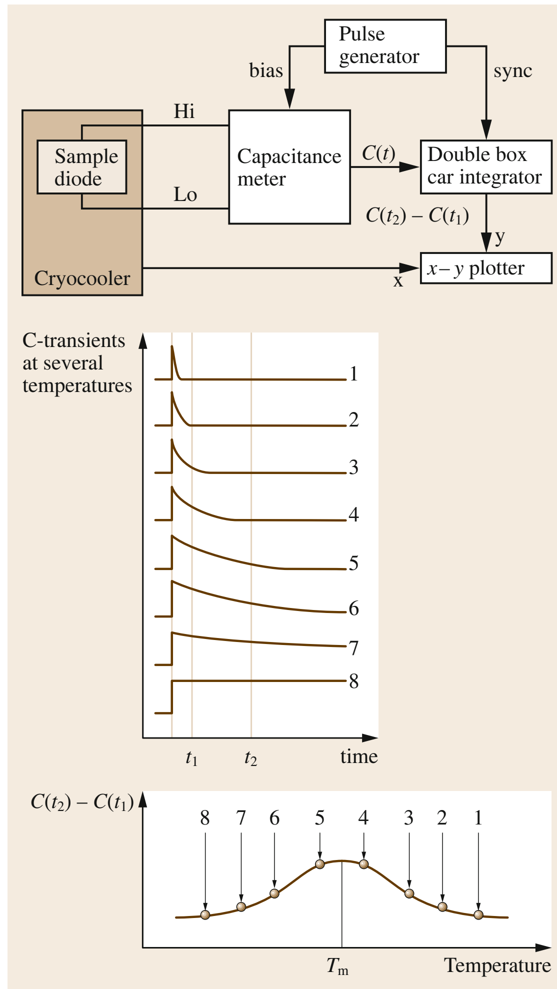

Fig. 20.38 Schematic representation of a conventional DLTS system. The time scans from which the DLTS temperature spectrum is obtained are shown on the *right*

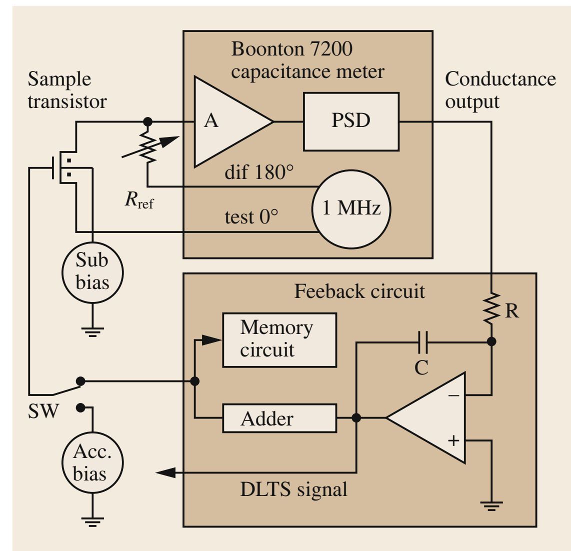

Fig. 20.39 Block diagram representation of the CR-DLTS system

Arrhenius plots are constructed in order to determine the defect energy level and its capture cross-section. Examples of DLTS spectra and Arrhenius plots associateed with CR-DLTS are presented later (in Fig. 20.40).

A block representation of the CR-DLTS system is shown in Fig. 20.39. More details can be found in [20.79–83]. A discussion of the signal processing and averaging techniques used with this DLTS technique can be found in [20.82]. Here, the gate bias voltage of the field-effect transistor is adjusted using a feedback circuit so that the resistance corresponding to the source–drain conductance matches that of a reference resistor R_{ref}, which is typically around 1 MΩ. The voltage transient due to the change in occupancy of the traps appears as a compensation voltage on the gate. This voltage change can be regarded as a threshold voltage change because the flat-band voltage of the device changes when the occupancy of the traps change. More details on how this change in the threshold is related to the traps can be found in [20.77, 79, 81].

Some important advantages of the CR DLTS technique are that the surface mobility of the MOS transistors does not need to be high, and that it is theoretically independent of the gate area of the transistor. This is expected, since the small amount of charge trapped beneath the gate must be balanced by a correction voltage applied across a relatively small gate–substrate capacitance.

Figure 20.40a shows six DLTS spectra for a junction field-effect transistor (JFET) damaged with 2.7×10^9 protons/cm^2 [20.79, 81] with six selected rate windows. Using the temperatures at which the peaks occur and the rate windows, Arrhenius plots can be constructed as shown in Fig. 20.40b, where the energies of five electron trap levels below the conduction band are also indicated. For the five traps, the extracted capture cross sections were 4.6×10^{-15} cm^2 (E1), 6.3×10^{-15} cm^2 (E2), 1.2×10^{-16} cm^2 (E3), 8.5×10^{-16} cm^2 (E4) and 3.4×10^{-15} cm^2 (E5).

Figure 20.41 shows CR-DLTS spectra as the source–body bias voltage is varied. The scans with a body bias of −1 V are lower in magnitude than those without substrate bias, except for the peak associated with the hole trap at 0.13 eV above the valence band [20.81]. When the reverse substrate bias is increased, the gate control of the space charge region near the channel decreases, meaning that fewer interface traps participate in the capture and emission of

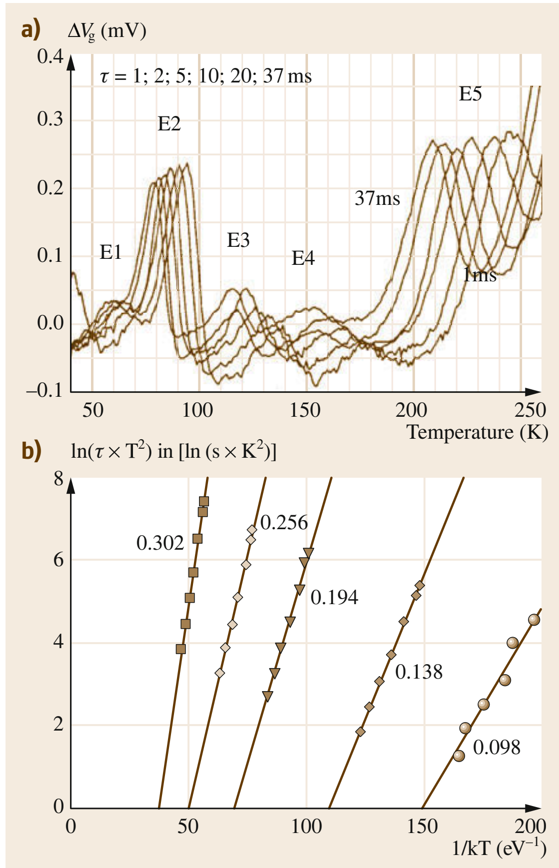

Fig. 20.40 **(a)** CR-DLTS spectra of a $50\,\mu m \times 20\,\mu m$ MOSFET damaged with 2.7×10^9 proton/cm^2. **(b)** Arrhenius plot derived from the CR-DLTS spectra, showing the energies of the five traps E1–E5. (After [20.80, 83])

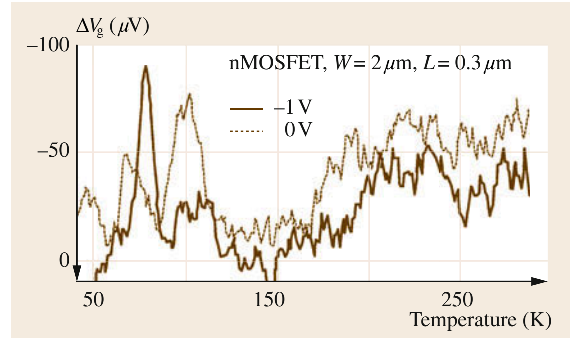

Fig. 20.41 Effect of body bias on CR-DLTS spectra. The body bias affects the surface and bulk traps in different ways

charges. However, the increased reverse substrate bias results in an increased space charge region in the silicon beneath the gate, so more bulk deep levels can participate in the capture and emission processes. This explains the increased deep-level peak (below 75 K) when −1 V is applied to the body. These differences between the CR-DLTS spectra demonstrate the ability to distinguish bulk traps from surface traps when the substrate bias of the MOSFET is varied.

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