Emerging Memories in Radiation-Hard Design

Roberto Gastaldi

1 Introduction

In many applications, electronic equipment must operate in an environment exposed to heavy radiation. These environments include those of: satellites in a terrestrial orbit used for telecommunication or military tasks and spacecraft on scientific missions outside our solar system in deep space; civilian and military aircraft; and equipment for measurement and control during experiments in high-energy physics and near nuclear power plants, industrial accelerators, and sources and in medical applications like radiology and radiotherapy. However, even electronic equipment used for common consumer applications can be affected by low-dose radiation, e.g., due to natural radioactivity in materials, high energy cosmic rays (especially in avionic applications), natural contaminants, and X-Rays coming from scanners in airports and controlled zones. In particular, commercial integrated circuits (ICs) that are the components of electronic systems can have a high sensitivity to radiation, so that their reliability is greatly compromised. IC technological evolution, which tends to yet denser integration, has generated two opposite phenomena: on one hand, devices became more tolerant to cumulative effects of radiation, while, on the other, they are more sensitive to soft errors generated by single events, because the dimensions of critical nodes have been reduced.

For many years, the design community has tried to answer the question about how to protect integrated circuits against radiation effects; in this regard, we can distinguish different approaches. The easiest conceptually is to shield the electronic systems with materials that stop radiation; this concept can be scaled down at component level using packages particularly designed to shield the internal die. Although this method is not invasive to the system and its components (ICs), it has

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a big limitation due to the weight of the shielding. If high protection is needed, thick metal shields must be used, whose weight cannot be tolerated in avionics and space applications, plus it is not easy to shield all harmful radiation this way. The second method is to operate at component level, making modifications to the silicon technology and/or to design to achieve immunity to radiation. If special technological steps are introduced to increase robustness, we speak about RHBP: radiation hardening by process. Otherwise, in cases where we rely on special design methodology to meet the target, we talk about RHBD (radiation hardening by design).

2 Radiation Environments

High-energy particles from galactic cosmic rays interact with the outer terrestrial atmosphere, losing energy and giving rise to a shower of secondary particles that strike the Earth's surface, in particular, neutrons and muons. Neutrons are the most important concern at sea level. Another source of radiation on the Earth's surface are the natural contaminants present in materials used for ICs' packages.

In the interplanetary space, instead, radiation is composed of electrons and protons trapped in the magnetic field of planets, high-energy particles coming from the Sun (protons and heavy ions), and cosmic rays (protons and heavy ions).

The interaction between external radiation (photons like X-rays and γ-rays, charged particles like protons, electrons, and heavy ions, or neutral particles) and a semiconductor cause two main phenomena: ionization and displacement. The first phenomenon creates an electron-hole pair (HEP), the second effect is an energy transfer from the incoming radiation and the reticule, causing modification to the reticule itself.

3 Effects of Radiation on Semiconductors

When radiation interacts with the semiconductor material, energy transferred to the reticle leads to the generation of an electron-hole pair by ionization: an electron acquires enough energy to move to conduction band as a free electron, leaving a hole in the valence band. If this event takes place in a region where an electric field is present, pair is separated and carriers move under the action of the electric field giving a transient current, before eventually recombine, or remain trapped, usually into an insulator, or they are collected from an electrode. In Fig. 1, the ionization process and resulting charge kinetics are illustrated.

Energy lost by an incident particle during its impact on material is measured by Linear Energy Transfer (LET). The LET depends on atomic number and energy of the striking particles and on the target material, and it is defined as

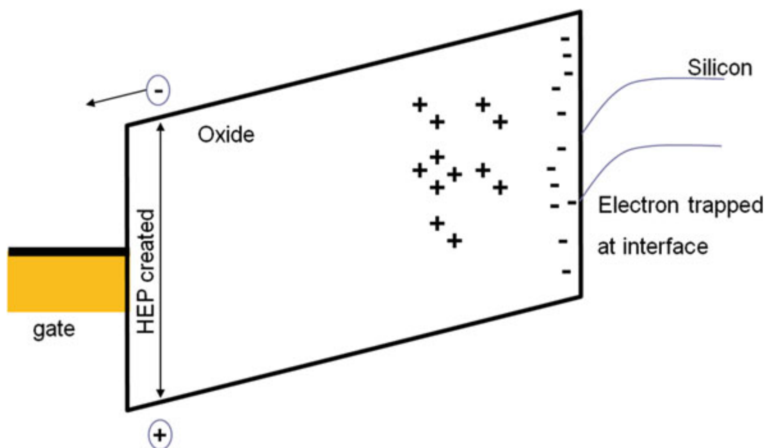

Fig. 1 Charge generated by radiation is trapped inside the oxide

$$\mathrm{LET} = (\mathrm{dE}/\mathrm{dx})1/\rho \quad (\mathrm{Me\ cm^2/mg}) \tag{1}$$

where ρ is the density of the target material and dE/dx indicates the average energy transferred into the target material per length unit along the particle trajectory. Another possibility is that a particle striking the silicon can displace an atom from its original position, leaving a defect in the reticle that can be seen as the creation of localized energy levels in the band-gap altering electrical properties of semiconductor. Part of the charge generated during ionization phenomena described above remains trapped in insulator layers [1–3] of a silicon device or at the interface between insulator and semiconductor where free carriers have a very low mobility and are easily captured by traps or interface states. In particular holes which have mobility many orders of magnitude lower than electrons can easily be trapped and act as a fixed positive charge both in gate oxides and in field oxides. Damaging effects caused by this trapped charge are cumulative and become important after a long exposure to radiation, they are measured with the Total Ionizing Dose (TID) which is the total amount of energy imparted by ionizing radiation to a unit mass of absorbing material and it is measured in Rads (1 rad = 0.01 J/kg).

In CMOS integrated circuits, the region most sensitive to cumulative effects is the gate oxide. The trapped holes (positive charge) introduce a negative shift in threshold voltage ΔV_{th}, given by:

$$\Delta V_{th} = -q/C_{ox}\Delta N_t = -(q/\varepsilon_{ox})t_{ox}\Delta N_t \tag{2}$$

where q is the elementary charge, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area, N_t is the density of trapped holes into the oxide, ε_{ox} is the dielectric constant of the oxide, and t_{ox} is the oxide thickness. Effects of negative threshold shift [4] cause an increase of sub-threshold current of N-MOS transistors and decrease their

controllability through the gate. However, at the first degree of approximation, trapped charge is proportional to t_{ox}, and consequently ΔV_{th} is proportional to t_{ox}^2, and for thin or very thin oxides (e.g., for thicknesses thinner than approximately 3 nm), threshold shift becomes negligible. This means that threshold shift due to charge trapped into the gate oxide is more important for older technologies using thicker gate oxides.

A second problem is coming from positive charge trapped in the Shallow Trench Isolation (STI) regions at the transition between a field-thick oxide and a gate-thin oxide (see Fig. 2). The region on the side of an STI can be modeled as a parasitic transistor in parallel with the MOS transistor channel. They are normally turned off because, due to the thick oxide their threshold voltage is higher, however due to positive charge trapped causing a negative shift of threshold voltage, parasitic transistors could turn on thus creating a parasitic path between drain and source, in parallel with the MOS-transistor channel once again increasing leakage current. Unfortunately this second effect is not improving too much with technology scale-down because field oxide is thick enough to cause non-negligible threshold voltage shift.

Also Displacement Damage Dose (DDD) has an effect of MOS electrical characteristics: lattice defects created at the Si-SiO_2 interface by the displacement introduce energy states in the band-gap [5, 6], which may trap channel carriers. The voltage threshold shift due to the charge trapped into interface states is

$$\Delta V_{IT} = -Q_{IT}/C_{ox} \tag{3}$$

where Q_{IT} is the trapped charge at the interface, which depends on device biasing. Moreover, trap states due to lattice defects facilitate decrease carriers mobility:

$$\mu = \mu_0/(1 + \alpha\Delta N_{IT}) \tag{4}$$

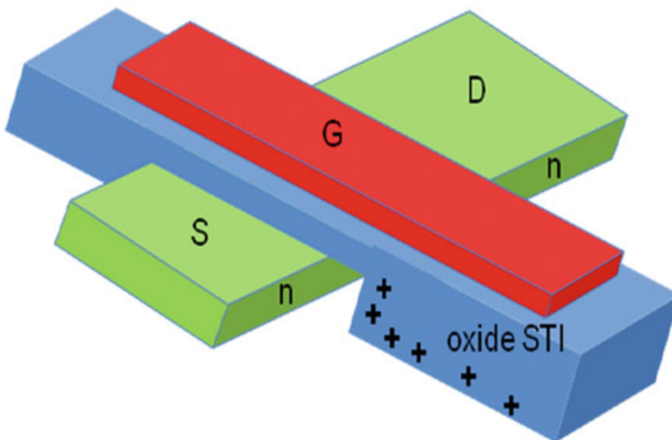

Fig. 2 Positive charge trapped in STI oxide

where μ_0 is the pre-irradiated mobility; α is a parameter dependent on the chosen technology; and ΔN_{IT} is the number of charges trapped at interface.

As a conclusion in an NMOS transistor, TID causes a leakage current when the transistor is turned-off and an alteration of transconductance characteristic with a decrease of gain β defined as:

$$\beta = \mu C_{ox} \tag{5}$$

A comparison of I_d/V_g characteristic before and after radiation exposure is shown in Fig. 3 where it can be seen the big increase of sub-threshold current after irradiation.

Ultimately these effects cause a failure of the whole system, but, even before this point, higher leakage current can cause power consumption get out of specification, particularly in stand-by mode.

In a PMOS transistor, TID causes an increase of the threshold voltage, but usually this effect is less dangerous for device functionality.

So far we have seen the effects due to a cumulative absorption of radiation that are more and more severe increasing the exposition time. There is another class of effects [7, 8] called single event effects (SEE) that are generated by a single strike of a high-energy particle at a point of a semiconductor, this class of effects can cause transient failures called SEU (single-event upset) to electronic devices or result in a permanent failure or damage, then we speak of SEL (single-event latch-up) or SEGR (single-event gate rupture).

Single-event effects are due to charge generation in a reverse-biased p-n junction in a CMOS IC. The junction may be part of a MOS transistor (drain-body or source-body), or may be a well-substrate junction. This mechanism is illustrated in

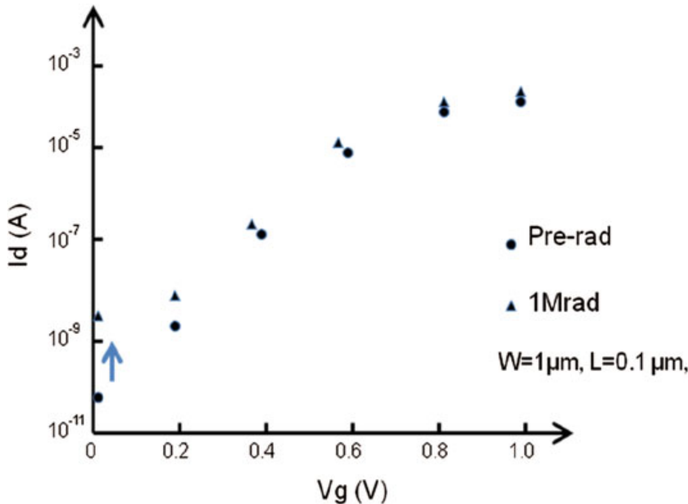

Fig. 3 Id/Vg shift of a NMOS transistor after irradiation

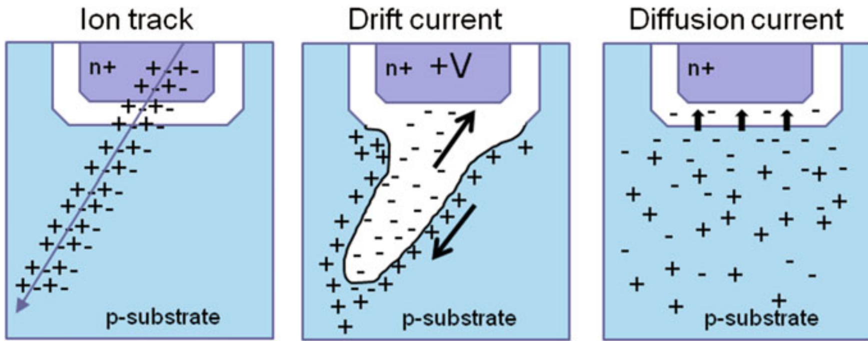

Fig. 4 Hole-Electron pairs generation in the substrate as a result of the impact with a high-energy particle. Part of the charge can be collected by biased junctions causing errors and malfunctions

Fig. 4 where a high-energy ion strikes a p-n junction generating a cloud of hole-electron pairs. The electric field in the reverse-biased p-n junction separates electrons and holes. The generated carriers are collected by neighboring electrodes, thus imparting a parasitic current with a peak due to carrier drift, followed by a tail due to carrier diffusion. N-junctions at a positive voltage collect the generated electrons, and, if the collected charge is higher than a critical charge, generates a glitch, temporarily changing the logic state of the collecting node: this is called a single-event transient (SET). Most of the logic nodes allow the transient to be recovered in a few nanoseconds as shown in Fig. 5, and, in pure combinatorial logic, the impact of a SET can be limited; however, they may propagate to adjacent

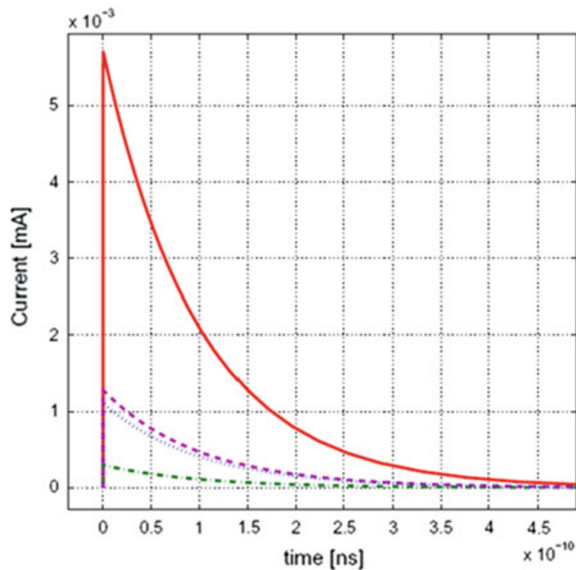

Fig. 5 Transient current generated by radiation can be recovered in few nanoseconds

nodes where the effect of other SETs can be added; if parts of the circuitry containing sequential logic are affected (latches, registers, or memories) [9], a permanent change of logic state in some nodes or data toggling in the memory can occur (see Fig. 6) and a single-event upset (SEU) takes place.

In this case, recovery is not possible because the transient has triggered a permanent logic change in some nodes. At some point, this logical error can occur after a number of logic operations involving different circuits, and it may be difficult to identify the point at which the original malfunction took place.

If a SEU affects two or more memory cells, a multiple bit upset (MBU) occurs. A SEU in the control logic may lead to a single-event functional interruption (SEFI).

Unfortunately, sometimes the sum of SET's can trigger physical damage in semiconductors, and this happens more frequently in power circuits where high currents or voltages are involved. In a structure as the one schematized in Fig. 7, the charge collected in the substrate after a SEE can trigger a positive gain loop made of parasitic bipolar transistors, resulting in a single-event latch-up (SEL), and high current flowing in the circuit during latch-up may lead to complete destruction of the IC [10].

Other destructive SEEs are the single-event burnout (SEB), which occurs in high-voltage devices when an avalanche multiplication mechanism is triggered by a parasitic charge in a p-n junction reverse biased and a single-event gate rupture (SEGR), where the displacement effect can result in an oxide-gate rupture. SEB and

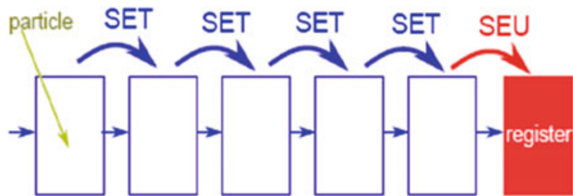

Fig. 6 A SET can propagate and generate a SEU in another circuit

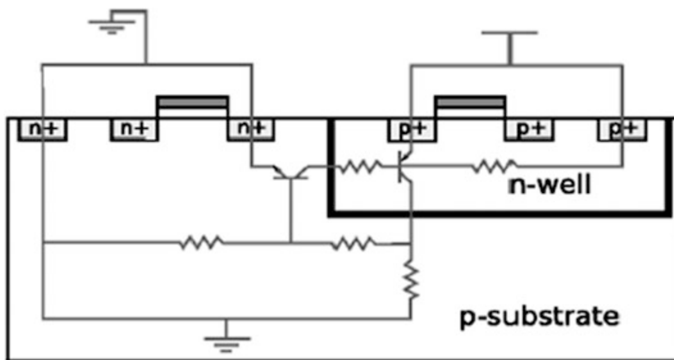

Fig. 7 Parasitic bipolar components in CMOS technology

Table 1 Summary of damaging events in semiconductor circuits

SEU	Single-Event Upset	Change of bit in memory element	Memory, latch
SET	Single-Event Transient	Temporary variation of a bit or of a voltage value	Analog and digital
MBU	Multiple-Bit Upset	Change of several bits coming from a SET/SEU	Memory, latch
SEFI	Single-Event Failure Interrupt	Corruption of data path in state machines	Flash memory, microprocessor, FPGA
SED	Single-Event Disturb	Temporary corruption of a bit coming from a SET	Combinational logic
SEL	Single-Event Latchup	High-current conditions leading to hard error	CMOS, BiCMOS
SEGR	Single-Event Gate Rupture	Rupture of the gate coming from high-electric field	Power MOSFET, NV memory, Deep VLSI
SEB	Single-Event Burnout	Burnout coming from high-current conditions	BJT, n-channel Power MOSFET
SHE	Single-Event Hard Error	Unalterable change of a bit	Memory (NV)
SESB	Single-Event Snapback	High-current conditions	Power MOSFET, SOI

SEGR occur in power MOS transistors [11,12] and are minor problems for memories, except perhaps in some non-volatile memory in which the high voltage required for writing is generated on-chip using charge pumps. Sensitivity versus SEE is measured with the cross section (in square centimeters), which constitutes the sensitive area of device. Finally Table 1 summarizes the possible effects of radiation on semiconductors that we have so far briefly discussed.

4 Radiation Effects in Memories

SEE effects in memories have been studied for a long time [13, 19], because of their big impact on stored data. In SRAM, a particle striking one of the feedback nodes of the latch leads to toggling of the cell's data due to the high-positive feedback of the latch itself (see Fig. 8).

Also DRAMs are very sensitive because a small amount of charge is enough to destroy the data stored in the cell capacitor. Even if SEE are much more critical in SRAM and DRAM, they can also be affected by cumulative effects due to total dosage (TID): NMOS threshold shift in 6T-RAM can degrade the stability factor and increase leakage current [14, 16], while in DRAM degrading performance of the cell's selector can reduce retention time. The periphery can be even more affected because larger transistors are present.

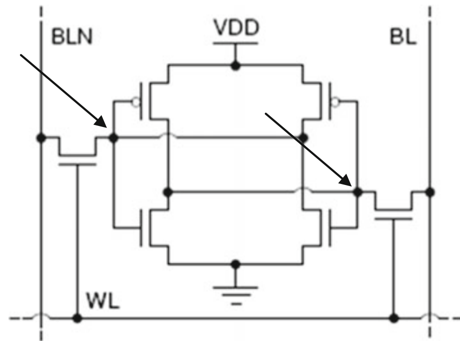

Fig. 8 Electrical circuit of a typical SRAM cell. Radiation particles striking critical nodes, as those indicted by the *arrows*, can cause flipping of memory-cell state inducing a bit failure in the memory array

For FLASH memories TID represents an important issue due to the fact that the storage mechanism relies on a charge accumulated in a floating gate surrounded by insulator. The technology's scaling-down roadmap reduces the charge stored in the cell to hundreds or tens of electrons, thus increasing the sensitivity to radiation effects.

In Fig. 9, a summary of these effects is presented, for a cell that is supposed to store a charge Q_{st} in the floating gate. The first effect is the creation of electron-hole pairs in the floating gate and control- gate oxide. Electrons in conduction band are swept out from the electric field created by the negative charge stored in the floating gate, while holes are collected in the floating gate, compensating the negative charge. The second one is an energy transfer from the high-energy particles striking the floating gate directly to stored electrons that are emitted over the oxide barrier (photoemission). Both these phenomena add up to cause charge loss in the cell.

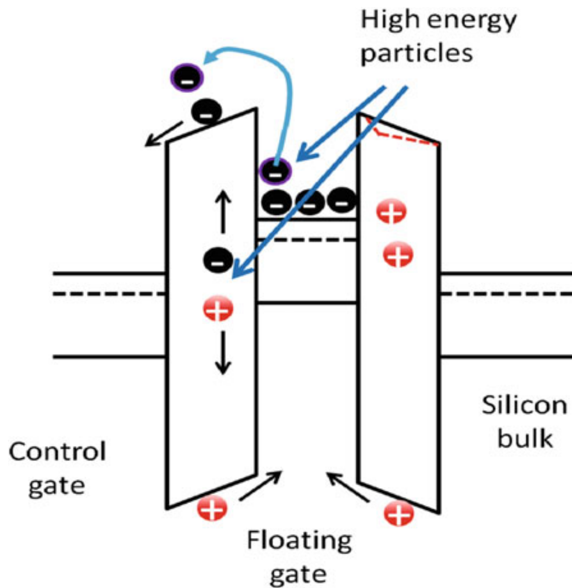

Fig. 9 Effects of radiation on a flash-memory cell

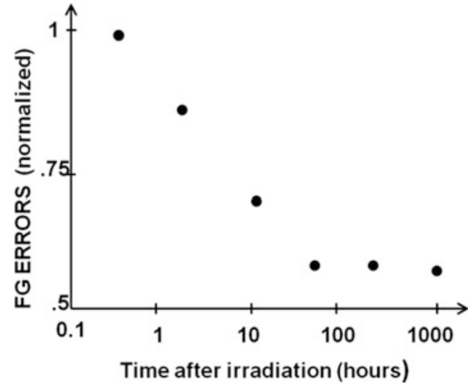

Fig. 10 Threshold shift induced by exposure to high-energy radiation can be partially recovered after a period of time

A third mechanism involves the positive charge created by ionization that can be trapped in the oxide and cause a local band bending that, on one hand, helps the charge emission by tunneling from the floating gate, and, on the other hand, increases the local electric field in the oxide, degrading reliability.

Experiments have been reported for NAND flash that confirm the impact of total dose on retention. Retention failures have been reported at dose < 50 Krad, quite independently from operating conditions.

The action of total dose on the threshold distribution in flash cells is to shift the whole threshold distribution toward the intrinsic distribution that is the one in which no charge is present in the floating gate.

Charge loss and errors consequently generated can be recovered at least for the portion due to trapped charge in the oxide, and that can be removed by annealing bake or de-trap spontaneously after a period of time (see, for example, Fig. 10).

On the contrary, in other cases the damage is permanent, probably because a defect in the oxide has been created during the strike: in this case the cell will have retention problems, experiencing early charge loss after a reprogramming.

5 Radiation Immunity of Emerging Memories

As we have seen, a big concern for flash memories is the charge stored in the floating gate that can be removed during interaction with high-energy radiation, leading to loss of stored data. When emerging memories don't rely on electrical-charge storage to retain logic data, but more on changes of bulk-material physical properties, then they could be more robust under radiation stress. Although there are no extensive data for all emerging memories under development, TID measurement performed with gamma and X-rays are reported on 90 nm PCM devices showing TID immunity up to 0.7 and >2MRad [15], while no errors after unbiased irradiation have been found until LET(Si) = 58 $\mathrm{MeVmg^{-1}cm^{2}}$. Upsets are not expected to occur along the scaling path at least before 32-nm node. [25].

A possible degradation mechanism that has been proposed is that penetration of heavy ions inside the GST, can lead to a heating of a small cylinder of the material around the particle path due to electron-phonon coupling until melting temperature is locally reached. This can cause a local phase change and a consequent modification of overall resistance of the memory element. This failure mechanism changes SET cells to RESET [25] and should become more important reducing cell's feature size. On the other hand, an incidence of single-event latch-up (SEL) and single-event functional interrupt (SEFI) in PCM irradiated with heavy ions has been reported [15, 23] but these failures seem to be connected to layout or external circuitry rather than to the memory material.

Measurement made on oxide ReRAM shows that the switching window exhibits a degradation under protons irradiation at high fluence, but at least some of the damage can be recovered after tens of writing cycles [20, 24]. Degradation is due to displacements damage in the oxide, which randomly create vacancy defects, so then a parallel filament can be created in parallel with the pre-existing one (see Fig. 11).

The layout configuration of a ReRAM cell, including a selector NMOS transistor and similar in this aspect to MRAM and PCM (at least for one of the possible configurations), can show SEE weakness. In fact, considering a generic cell cross-section with the non-selected cell, we have the situation of Fig. 12. In this figure the gate of selector transistor is at ground, and drain n^+ region is at 1.8 V, because no current flows in the system. If a particle strikes the drain region of selector, a glitch to GND can be produced and enough bias voltage would appear across the cell to cause a spurious write.

Another criticality linked to the selector is the possibility of a threshold shift and degradation of the transconductance that would impact the leakage current through the unselected cells and could eventually lead to bit failure. The same kind of degradation affects NMOS in peripheral circuits, and we have seen that the reason for device failure can originate more from a malfunction in periphery circuitry than from intrinsic weakness of the memory cell, so in the following we will cover, in a little more detail, the ways to protect circuitry from radiation effects.

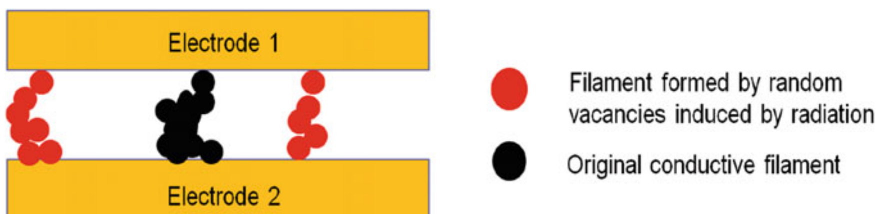

Fig. 11 Mechanism of degradation caused by interaction with high-energy protons in a ReRAM cell

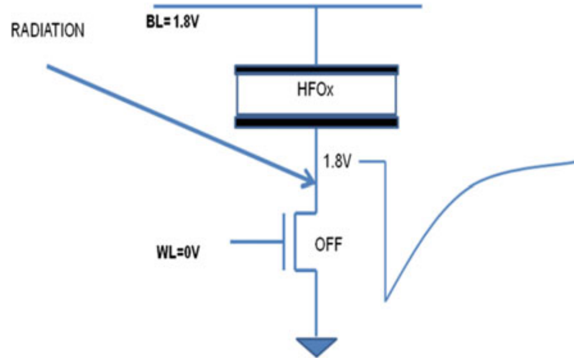

Fig. 12 Problem of disturb in a ReRAM cell

6 Design of Radiation-Hardened Memories

In the previous discussion about memory robustness to radiation stress, it is clear that, beyond the specific weaknesses related to the memory cell itself, coming from storing mechanism and materials used, an important cause of failure is represented by the periphery circuitry that is subject to the same problems of all MOS devices when operating in a radiation environment. In many cases, in particular in emerging memories, these problems can cancel the advantages that come brought by an intrinsically robust memory cell and lead to poor performance of the device.

Using a shield to protect electronic systems is very expensive due to the weight associated with the shielding, and the inevitable trade-off with performances can be not completely satisfactory. Another possibility comes from process modifications, for example, the use of SOI can improve robustness to induced latch-up (SEL). In general, in any case, adoption of special process for rad-hard devices is not sustainable by foundries, due to the relatively low volume of devices requiring high rad-hard performance. In addition, transporting a design from one foundry to the other is more difficult than using a full standard process. Also, technology scaling–down, which reduces area of critical nodes and distances, makes it more and more difficult to adequately protect devices. For this reason, an increasing interest has been put on inventing special design techniques and layout rules to improve device tolerance to radiation.

The first step for an effective protection begins at the layout level [17]: we have already seen that charge injected into a silicon substrate from a high-energy particle striking a semiconductor device can trigger a potentially destructive latch-up. We have also seen that the prevalent part of failures in experiments under radiation is due to SEL. So the natural countermeasure is to apply latch-up protection guidelines whenever possible, making guard-rings and reinforcing contacts to Vdd and gnd to avoid that some junctions be biased in such a way to make latch-up easier.

An example of this kind of treatment is shown in Fig. 13.

Here two n^+ and p^+ guard-rings around a p-well and an n-well are interposed between a p-channel and an n- channel of an MOS to prevent latch-up triggering.

Fig. 13 Layout of guard-rings between p-channel and n-channel transistors to prevent latch-up

Guard-rings must be connected to Vdd and gnd respectively through a metal line above them and the contacts chain to guarantee that all the ring is at the same potential. In addition, whenever possible, n-channel and p-channel MOSs should be grouped and positioned as far from each other as much as possible. Moreover, it is possible to use guard-rings around transistors of the same type but biased at different voltages to reduce the leakage induced by positive charge trapped in the STI oxide.

We have also seen in the previous discussion that a big problem is the charge accumulated at the edge of STI, which creates a leakage path bypassing the transistor channel. This is a long-term effect depending on the total dose absorbed (TID) and produces a degradation of the transistor characteristics that eventually makes it impossible to switch off the device, leading to component functional failure. To counteract efficiently this issue, it is possible to adopt the so-called edge-less transistor (ELT) that is a way to layout the transistor without an edge on the field oxide. In this transistor the drain region is completely surrounded by a source region and the anular gat defines the channel region, so that no field edge crosses the gate and a parallel leakage path is no longer possible.

Generally, it is convenient in ELT transistor to minimize the drain area that is the most sensitive node to SEE, which means to put the drain terminal on the internal side.

Although ELT is an effective way to increase TID robustness of MOS ICs, the price to pay in terms of area is very high. It should be noted that ELT is mandatory only for NMOS because trapped charge is positive, PMOS are not affected, and this contributes to mitigate the area drawback. But still it remains a problem for more dense and performance demanding ICs, not only for the mentioned area occupation, but also due to the increase of parasitic capacitances and gate capacitance that prevent very high-speed operation.

Looking at memory ICs that are built around the array of cells, the use of ELT in decoding circuitry puts a limit on the reduction of row and column pitch, in particular for flash memories where the last stage of decoding must sustain the high voltage required for programming. Emerging technologies are in a better situation because they require much less voltage than flash during write. On the other hand, if ELT is used, the memory cell itself obviously cannot be made very small. SRAM cells using extensive ELT proved to be immune up to TID = 15Mrad and SEU LET immune up to 5MeVmg/cm^2 while avoiding ELT in all the transistors TID immunity has been reduced to <200Krad.

At circuit level, a designer can use dedicated circuit configurations to lower sensitivity to SEE. Low capacitive nodes are more sensitive to the transients caused by particles strike (SET), so full C-MOS logic should be used as much as possible, and the number of transistors not directly connected to supplies should be minimized. Also, very sensitive nodes may be designed to have a higher parasitic capacitance in such a way to increase critical charge.

An important aid for designers comes from dedicated software that can simulate the effect of charge injection in a node of the network. It becomes possible to evaluate the critical charge for nodes that are judged particularly critical and understand how the generated disturbance propagates throughout the whole network and its effect on the global operation [18].

Mitigation of SEFI requires that feedback loops are avoided as much as possible, but this cannot be done easily when sequential logic is involved, so a possibility is to try to delay the loop to give the transient the time to finish [19]: unfortunately, the time constants involved may be a serious problem for high speed logic.

A sort of hardware redundancy is represented from voter circuits as depicted in Fig. 14.

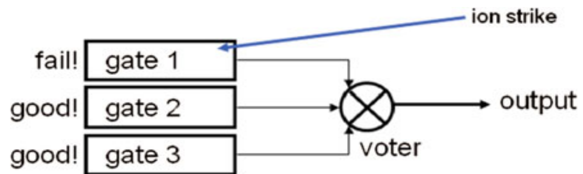

Fig. 14 Concept schematic of voter circuitry

The concept is to replicate the same gate or logic circuit an odd number of times (three in the figure) and take as correct the output indicated by the majority of the gates, considering that the probability that a particle strikes the majority of the gates at the same time is low enough.

As a matter of fact, all these techniques pay a high price in silicon area and operation speed, so a trade-off is always needed to target of robustness and electrical performance.

Concerning memories, there are additional considerations to be made for chip architecture: it has been found that the charge pump used to generate the on-board high voltage required for flash-cell programming is particularly weak under radiation stress, even at relatively low doses of irradiation, causing the memory device to fail program. This is an issue favoring emerging memories that don't require high voltage for programming.

We have already seen that the cells inside the array can fail due to a SEE effect. This failure can be seen from the outside as a single bit failure or a pair failure if the neighbor bit is affected.

An efficient way to survive with this kind of error is to provide an error detection and correction (EDAC) engine on board; this is quite common not only for rad-hard memories, but also in consumer products, such as large-capacity NANDs, and it is mandatory in almost all emerging technologies to achieve an acceptable low-bit error rate.

The overhead of EDAC-blocks for circuit complexity and access- time delay depends on the number of fail bits that can be corrected in a word, and, unfortunately, memories in a radiation environment are sensitive to failures that affect many bits or even the whole word. For example, an SEU occurring in the array row or column decoding will lead to an incorrect reading or programming of the whole row or column, if they are selected during the upset. In case of hard damage, the failure of the selected element will be permanent. It is then reasonable to prefer array architectures that mitigate the risk of failure of a whole word or column [22].

Significant improvement can be obtained with an array partitioning, by providing each memory array storing a single bit of the word with separate bit-line and word-line decoders, to avoid MBUs. An example of such an array organization in a 512K SRAM is shown in Fig. 15. Even if many cells are affected by a particle strike, the resulting error will be only on a single bit of the word, and this is true also if one of decoders is hit.

On the other side an issue of this solution is the large area occupation that limits the maximum memory size practically achievable.

In addition it requires a careful design to balance different signal paths at byte level and to avoid cross-coupling noise among the tiles. Non-volatile memories, as we have seen, if they are affected by a single event or by cumulative effect, can degrade the information stored. For example, flash can experience charge loss, and

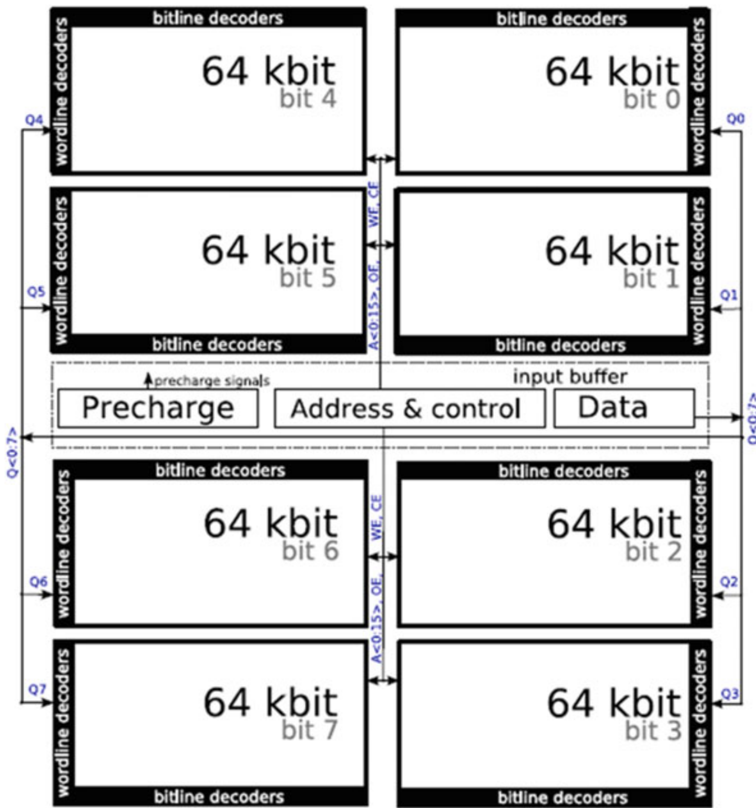

Fig. 15 Array architecture of Redcat Devices 512Kb SRAM (RC7C512RH)

PCM and other emerging memories can change their resistance or can go through a write disturb as described above for ReRAM. In this case, the signal available for reading the memory is reduced and the result can be a reading failure or an unstable reading that can give a correct result or a failure depending on the temperature, operating conditions, and the process parameters. This kind of malfunction can be very difficult to detect in the system before it eventually evolves into a permanent fail. The concept that may be employed to mitigate read-window narrowing, is to use two cells for a single bit and compare each to the other after programming them with a complementary data, as conceptually shown in Fig. 16. Although it doubles the available reading window, this self-referencing architecture is highly area consuming and can be used for low-medium memory size.

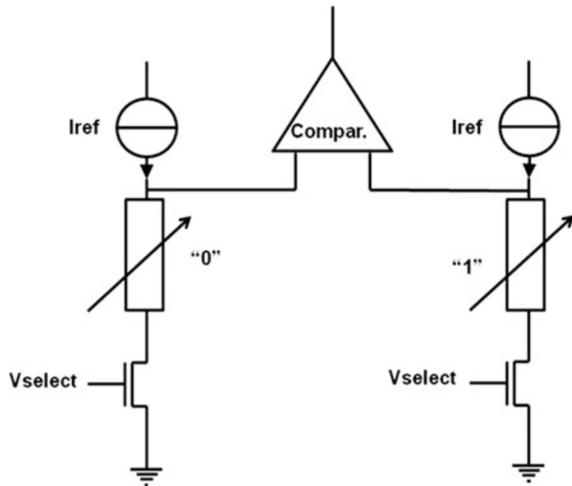

Fig. 16 Conceptual drawing of self-reference reading scheme

7 Conclusions

Unlike mainstream flash technology, which is affected by interactions with high-energy particles due to their mechanism being based on charge stored in a floating gate, emerging memories prove to be more robust against TID degradation. In addition, low-voltage operation required for most of emerging technologies allows the elimination of some circuits, like charge pumps that were found to be a critical point during irradiation experiments.

Nevertheless, peripheral circuitry and the cell selector device become the weak point of the system, and process and design techniques to mitigate this weakness must be adopted. In particular, radiation hardening by design has the advantage to operate on a standard process and thus to optimizing reliability and cost, but by paying a price in terms of silicon area and performance.

For these reasons, radiation hardening by design always requires a compromise between the degree of protection and the electrical performance required by the system.

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