Chapter 8
Flip-Chip Underfill: Materials, Process, and Reliability

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Abstract In order to enhance the reliability of a flip-chip on organic board package, underfill is usually used to redistribute the thermo-mechanical stress created by the Coefficient of Thermal Expansion (CTE) mismatch between the silicon chip and organic substrate. However, the conventional underfill relies on the capillary flow of the underfill material and has many disadvantages. In order to overcome these disadvantages, many variations have been invented to improve the flip-chip underfill process. This chapter reviews the recent advances in the material design, process development, and reliability issues of flip-chip underfill, especially in no-flow underfill, molded underfill, and wafer-level underfill. The relationship between the materials, process, and reliability in these packages is discussed.

8.1 Introduction

The brain of the modern electronics is the integrated circuit (IC) on semiconductor chip. In order for the brain to control the system, interconnects need to be established between the IC chip and other electronic parts, power and ground, and inputs and outputs. The first-level interconnect usually connects the chip to a package made of either plastics or ceramics, which in turn is assembled onto a printed circuit board (PCB). Three main interconnect techniques are used: wire-bonding, tape automated bonding (TAB), and flip-chip. In a wire-bonded package, the chip is adhered to a carrier substrate using a die-attach adhesive with the active IC facing up. A gold or aluminum wire is then bonded between each pad on the chip and the corresponding bonding pad on the carrier as shown in Fig. 8.1. The chip and the wire interconnections are usually protected by encapsulation. TAB, on the other hand, uses a prefabricated lead frame carrier with copper leads adapted to the IC

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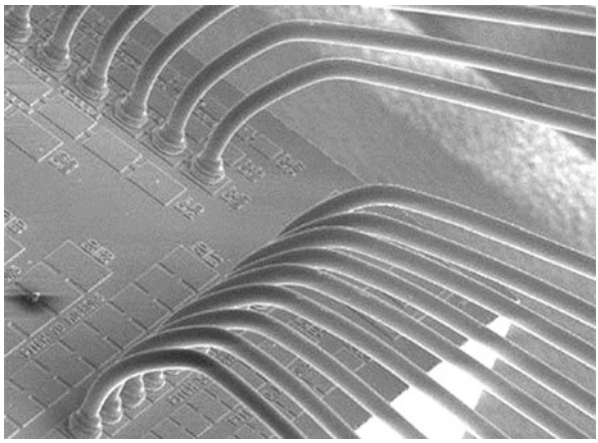

Fig. 8.1 First-level interconnect using wire-bonding

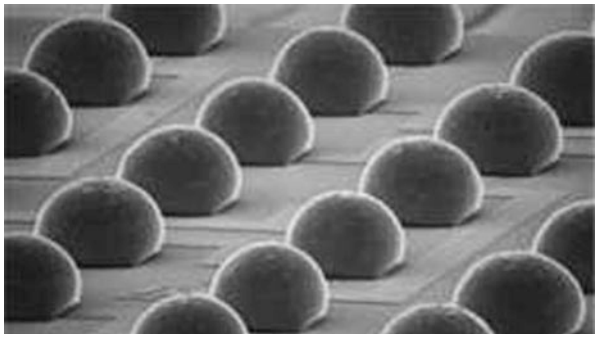

Fig. 8.2 Area array solder bumps for flip-chip interconnect

pads. The copper is usually gold-plated to provide a finish for bonding to the IC chip pads. The chip is attached onto the carrier and either thermosonic/thermocompression bonding or Au/Sn bonding is used to establish interconnection. Both wire-bonding and TAB interconnects are limited to peripheral arrangement and therefore low input/output (I/O) counts. Flip-chip, however, can utilize the entire semiconductor area for interconnects. In a flip-chip package, the active side of an IC chip is faced down toward and mounted onto a substrate [1]. Interconnects, in the form of solder bumps, stud bumps, or adhesive bumps, are built on the active surface of the chip, and are joined to the substrate pads, in a melting operation, adhesive joining, thermosonic, or thermocompression process. Figure 8.2 shows an example of solder bumped chip surface for flip-chip interconnect. The first flip-chip was a beam-leaded device which was developed in 1957 in the Bell Labs. Since then, many variations of the flip-chip design have been developed, among which, the Controlled Collapse Chip Connection (also known as C4) invented by IBM in 1960s is the most important form of flip-chip [2]. Compared with conventional packaging using wire-bonding technology, flip-chip offers many advantages such as high I/O density, short interconnects, self-alignment, better heat dissipation

Table 8.1 CTE of several major materials in flip-chip packaging

Materials	CTE (ppm/°C)	Application in flip-chip
Silicon	2.5	Chip or substrate
FR-4 board	16	Organic substrate
Alumina	6.9	Ceramic substrate
Solder	18–22	Interconnects
Polyimide	45	Flexible organic substrate
Epoxy	55–75	Polymeric resin of the underfill
Silicon dioxide (SiO_2)	0.5	Filler of the underfill

through the back of the die, smaller footprint, lower profile, and high throughput. The outstanding merits of flip-chip have made it one of the most attracting techniques in modern electronic packaging, including MCM modules, high-frequency communications, high-performance computers, portable electronics, and fiber optical assemblies.

The early flip-chip devices usually had small dies and the substrates were limited to the high-cost ceramic or silicon materials, and the coefficient of thermal expansion (CTE) mismatch between the die and substrate was not large enough to cause a reliability problem. Since the late 1980s, the dies have been increasing in size and low cost and light organic substrates, such as FR-4 board or polyimide began to be used in the flip-chip, therefore "fatigue life" of the solder joints became an issue. This thermal-mechanical issue mainly arises from the CTE mismatch between the semiconductor chip (typically Si, 2.5 ppm/°C), solder (CTE 18–22 ppm/°C) and the substrate (4–10 ppm/°C for ceramics and 18–24 ppm/°C for organic FR4 substrate). Table 8.1 shows the CTE of major materials used in the flip-chip packaging. As the distance from the neutral point (DNP) increases, the shear stress at the solder joints increases accordingly. So with the increase in the chip size, the thermal-mechanical reliability becomes a critical issue. Organic substrates have advantages over ceramic substrates because of their low cost and low dielectric constant. But the high CTE differences between the organic substrates and the silicon chip exert great thermal stress on the solder joint during temperature cycling.

In 1987, Hitachi first demonstrated the improvement of solder fatigue life with the use of filled resin to match solder CTE [3]. This filled resin, later called "underfill", was one of the most innovative developments to enable the use of low-cost organic substrate in flip-chip packages. Underfill is a liquid encapsulant, usually epoxy resins heavily filled with fused silica (SiO_2) particles, that is applied between the chip and the substrate after flip-chip interconnection. Upon curing, the hardened underfill exhibits high modulus, low CTE matching that of the solder joint, low moisture absorption, and good adhesion toward the chip and the substrate. Thermal stresses on the solder joints are redistributed among the chip, underfill, substrate and all the solder joints, instead of concentrating on the peripheral solder joints. It has been demonstrated that the application of underfill can reduce the all-important solder strain level to 0.10–0.25 of the strain in joints which are not encapsulated [4, 5]. Therefore, underfill can increase the solder joint fatigue life by

10–100 times. In addition, it provides an environmental protection to the IC chip and solder joints. Underfill becomes the practical solution to extending the application of flip-chip technology from ceramics to organic substrates, and from high-end to cost-sensitive products. Today, flip-chip is being extensively studied and used by almost all major electronic companies around world including Intel, AMD, Hitachi, IBM, Delphi, Motorola, Casio, etc.

8.2 Conventional Underfill Materials and Process

The generic schematic of a flip-chip package is shown in Fig. 8.3. Conventional underfill is applied after the flip-chip interconnects are formed. The resin flows into the gap between the chip and the substrate by a capillary force. Therefore, it is also called "capillary underfill" (CUF). A typical capillary underfill is a mixture of liquid organic resin binder and inorganic fillers. The organic binders are often epoxy resin mix, although cyanate ester or other resin has been used for underfill application as well. Figure 8.4 shows the chemical structure of some commonly used epoxy resins. In additional to epoxy resin, a hardener is often used to form cross-linking structure upon curing. Sometimes a latent catalyst is incorporated to achieve long pot life and fast curing. Inorganic fillers typically used in underfill formulation are micron-sized silica. The silica fillers are incorporated into the resin binder to enhance the material properties of cured underfill such as low CTE, high modulus, and low moisture uptake. Other agents that can be found in an underfill formulation include adhesion promoters, toughening agents, and dispersing agents. These chemicals are incorporated to help the resin mixing and enhance the cured underfill properties.

Figure 8.5 shows the process steps of flip-chip with conventional underfill. Separate flux dispensing and cleaning steps are required before and after the assembling of the chip, respectively. After the chip is assembled onto the substrate, the underfill is usually needle-dispensed and is dragged into the gap between the

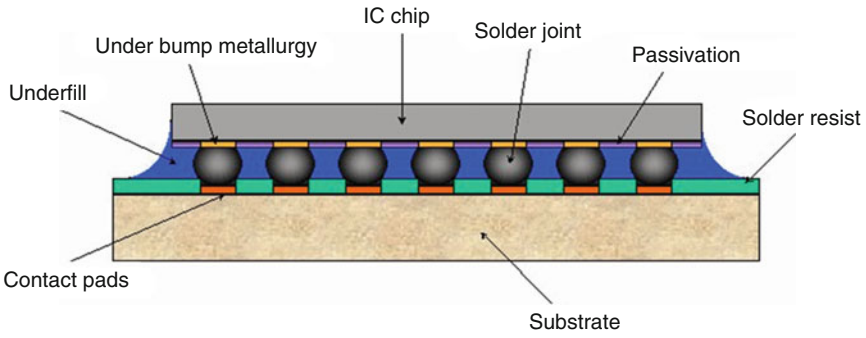

Fig. 8.3 Generic configuration of a flip-chip package with underfill

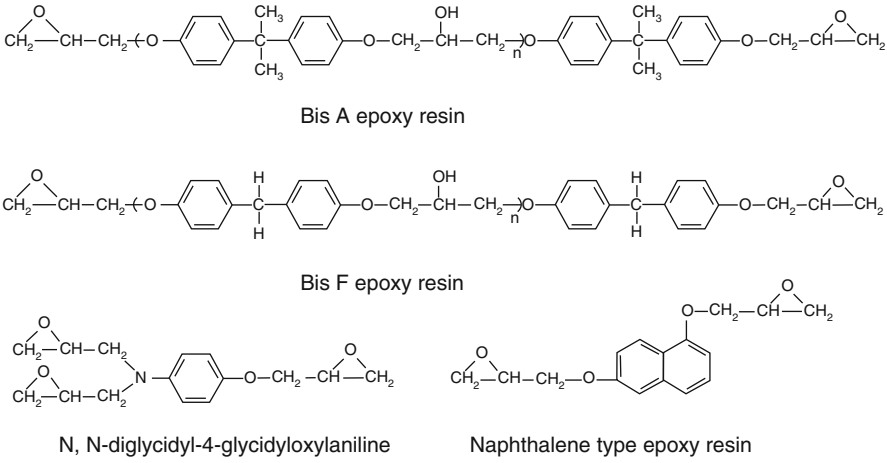

Fig. 8.4 Typical epoxy resin structures used in underfill formulations

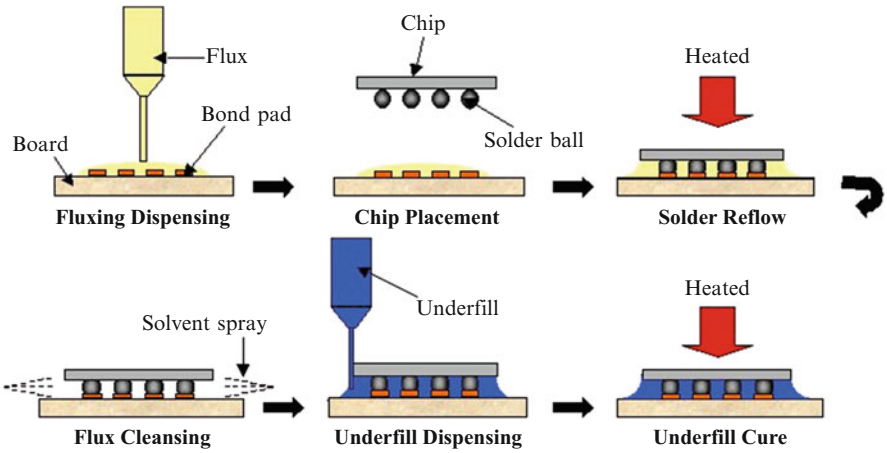

Fig. 8.5 Flip-chip process using conventional underfill

chip and the substrate by a capillary force. Then a heating step is needed to cure the underfill resin to form a permanent composite.

The flow of the capillary underfill has been extensively studied since it is considered to be one of the bottlenecks for the flip-chip process. The capillary flow is usually slow and can be incomplete, resulting in voids in the packages and also non-homogeneity in the resin/filler system. The filling problem becomes even more serious as the chip size increases. The flow modeling of flip-chip underfill is often approximated as viscous flow of the underfill adhesive between two parallel plates. One can use the Hele-Shaw model to simulate the underfill flow with the above approximation. The time required to fill a chip of length L can be calculated as [6]:

$$t_{\text{fill}} = \frac{3\eta L^2}{\sigma h \cos\theta} \tag{8.1}$$

where η is the underfill viscosity; σ is the coefficient of the surface tension; θ is the contact angle; and h is the gap distance. It is easily seen that a larger chip with a smaller gap distance would require longer time to fill.

The above approximation does not take the existence of solder bumps into account. It is shown that the approximation breaks down when the spacing between bumps is comparable to the gap height [7]. Therefore, this model cannot apply to high-density area array flip-chip applications. Using transparent quartz dies assembled onto different substrates, Nguyen et al. observed the flow of commercial underfills and used a 3D PLICE-CAD to model the underfill flow front [8]. A comparison between the peripheral and area array chips showed that the bumps enhanced the flatness of the flow front by providing periodic wetting sites. A racing effect along the edges was observed. Voids can be formed at the merging of flow fronts. The merging of the fronts also produced streaks, which are zones of no- or slow-moving fluids, leading to higher potential for filler settling.

Recent development in underfill flow models has also considered the effect of the contact angle on solder and bump geometry. A study by Young and Yang used a modified Hele-Shaw model considering the flow resistance in both the thickness direction between the chip and substrate, and the plane direction between solder bumps [9]. It was found that the capillary force parameter would approach a constant value at very large pitch for the same gap height. As the bump pitch reduces, the capillary force will increase to a maximum as a result of underfill wetting on the solder given the contact angle on the solder is small, and then quickly drops to zero as the pitch approaches the bump diameter. Their study also showed that a hexagonal bump arrangement is more efficient to enhance the capillary force at critical bump pitch.

Before the underfill dispensing, the underfill volume and mass required for a flip-chip should be calculated accurately. The underfill volume can be estimated by accounting for the underfill volume filling the gap under the chip, less the volume of the solder bumps interconnections, and plus the volume of the underfill in the fillets around the chip edges (Fig. 8.6). The underfill volume can be approximated by the following Eqs. (8.2)–(8.6) [10]. There are three commonly used types of dispensing patterns: single side, L-shaped, and modified U-pattern. To get reliable parts from

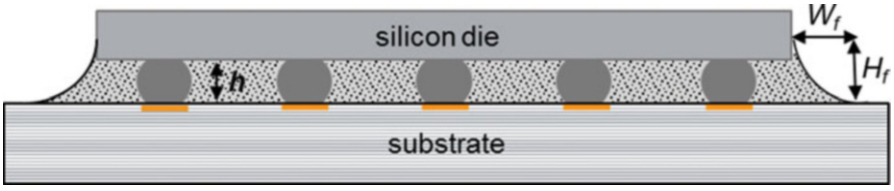

Fig. 8.6 Schematic of an underfilled flip-chip device [10]

the underfill process, the right amount of underfill material must be dispensed in the right pattern in a well-timed sequence.

$$V_{\text{underfill}} = V_{\text{standoff gap}} - V_{\text{bumps}} + V_{\text{fillet}} \tag{8.2}$$

$$V_{\text{standoff gap}} = L_{\text{chip}} * W_{\text{chip}} * h \tag{8.3}$$

$$V_{\text{bumps}} = N_{\text{bumps}} * V \tag{8.4}$$

$$V_{\text{fillet}} = \left[2\left(L_{\text{chip}} + W_{\text{chip}}\right) * \left(H_f * W_f\right) + \pi/3 * \left(W_f^2 * H_f\right)\right] * \text{SF} \tag{8.5}$$

$$W_{\text{underfill}} = V_{\text{underfill}} * \rho_{\text{underfill}} \tag{8.6}$$

Note: SF = shape factor which is determined by the contact angle, V = volume, L_{chip} = length, W_{chip} = width, $W_{\text{underfill}}$ = weight of the underfill, $\rho_{\text{underfill}}$ = density of the underfill, h = die-substrate gap, W_f = width of the fillet, and H_f = height of the fillet.

8.3 Reliability of Flip-Chip Underfill Packages

The reliability of a flip-chip package can be evaluated in a number of different methods, including thermal cycling, thermal shock, pressure-cook test, etc. The lifetime of a solder joint interconnect during temperature cycling can often be described by statistical models such as Weibull distribution. The probability density function (PDF) of the Weibull distribution is given by:

$$f(x) = \left(\frac{\beta}{x}\right)\left(\frac{x}{\theta}\right)^{\beta} \quad \exp\left(-\left(\frac{x}{\theta}\right)^{\beta}\right) \tag{8.7}$$

where x is the thermal cycling life as a random variable; θ is the characteristic life; β is the shape parameter. The mean time to failure (MTTF), which is the expectation of the time to failure, for the Weibull distribution is:

$$\text{MTTF} = \theta \cdot \Gamma\left(1 + \frac{1}{\beta}\right) \tag{8.8}$$

where Γ is the gamma function. It is generally believed that fatigue of the solder joints is a major reason for structure and electrical failures. The solder fatigue life can be described as a function of inelastic shear strain in Coffin–Manson equation:

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f'}\right)^{1/c} \tag{8.9}$$

where N_f is the number of cycles to fatigue failure, $\Delta\gamma$ is the inelastic shear strain, $\varepsilon_f^{'}$ is the fatigue ductility coefficient, and c is the fatigue ductility exponent. Other strain-based fatigue equations have been proposed, among which Solomon's model is often used:

$$N_f = \left(\frac{\theta}{\Delta\gamma_p}\right)^{1/\alpha} \tag{8.10}$$

where $\Delta\gamma_p$ is the percentage inelastic shear strain, θ and α are constants.

It has been shown that the use of the underfill can increase the lifetime of the solder joints by at least an order of magnitude during thermal cycling [11]. It was found that in an underfilled flip-chip package, the fatigue life is highly dependent on the material properties of the underfill. The analytic model by Nysaether et al. [12] showed that while an underfill without filler increased the lifetime by a factor of 5–10, a filled underfill with a lower CTE gave a 20–24-fold increase in lifetime. For both filled and non-filled sample, the lifetime is nearly constant regardless of distance to the neutral point (DNP), indicating that the underfill effectively couples the stress among all the solder joints.

Many numerical models have been developed to study the solder fatigue life of a flip-chip package with or without underfill. The polymeric nature of the underfill material requires careful characterization for correct material property input to the numerical models. The modulus of a polymeric material is not only a function of temperature, but also a function of time, i.e., it is a viscoelastic material. Thermal mechanical analyzer (TMA) and dynamical mechanical analyzer (DMA) are typically used to characterize the viscoelastic properties of the underfill material. Dudek et al. characterized four commercial electronic polymers and used finite element (FE) analyses to study the effect of die size and underfill material properties on the thermo-mechanical reliability of the flip-chip on board (FCOB) package [13]. They found that although the use of underfill can effectively reduce the shear strain, it can also cause bump creep strain in the transverse board direction due to stretching and compressing of the bump during thermal cycling. This load is due to the CTE mismatch between the solder and underfill/solder-mask layer. Underfill with CTE that matched the solder material (22–26 ppm/°C) gives the best thermal cycling life based on the creep strain criterion.

The function of the underfill in a flip-chip package is stress redistribution, not stress reduction. A rigid underfill material mechanically couples the device and the substrate, changing partially the shear stress experienced by the solder joints into bending stress on the whole structure. Shrinkage of the underfill during cure and the CTE mismatch during cooling after cure can generate large stress on the Si chip, resulting in die crack in some cases. Palaniappan et al. performed in-situ stress measurements in the flip-chip assemblies using a test chip with piezoresistive stress sensing devices [14]. The study concluded that the underfill cure process generates large compressive stress on the active die surface, indicating a complex convex bending state in the flip-chip. The level of stress measured can lead to Si fracture.

The residual die stress was found to be strongly dependent on underfill CTE, modulus, and T_g. A finite element analysis by Mercado et al. on the die edge cracking in flip-chip PBGA packages also concluded that the energy release rate for horizontal Si facture increases with underfill modulus and CTE [15].

In addition to temperature-related thermomechanical failure, moisture-induced failures such as delamination and corrosion are common for a flip-chip underfill package. HAST (highly accelerated stress test) is often used to determine the temperature and moisture sensitivity of the package. The test uses harsh environment conditions such as high temperature, high humidity, and high pressure. A typical test condition can be 121 °C, 100 % RH (relative humidity), and 2 atm pressure. It has also been known as the autoclave or pressure cooker test (PCT). The moisture absorbed by the polymeric materials can hydrolyze the interfacial bonds between underfill and the die, resulting in delamination starting from the corner of the die, which further promotes the moisture diffusion along the interface. The moisture at the interface can cause corrosion of the solder joints and metal traces on the substrate. Delamination decouples underfill with the Si die and cause stress concentration on the surrounding solder joints, leading to early fatigue failure of those joints. The absorbed moisture also causes hygroscopic swelling. Lahoti et al. studied the combined effect of moisture and temperature on the reliability of flip-chip ball grid array (FCBGA) packages using FE analysis. The simulation results revealed the significance of hygroscopic-induced tensile stress on the under bump metallurgy (UBM) and inter dielectric layer (ILD) [16].

Interfacial delamination of underfill to various materials such as die passivation, solder material, and solder mask on the substrate is a leading cause for failure in flip-chip underfill packages. One way to improve the reliability under temperature and humid aging is to incorporate adhesion promoters, or coupling agents, into underfill to increase adhesion of underfill to the surrounding materials. Luo et al. studied six different coupling agents and their effect on underfill. The authors found that the incorporation of the coupling agents clearly affected the curing profile and bulk property of the underfill, such as T_g and modulus. The effect of coupling agents on adhesion and adhesion retention after temperature moisture aging was highly dependent on coupling agent type and interacting surfaces. The addition of titanate and zirconate coupling agents can improve adhesion of epoxy underfill with BCB-passivated silicon. However, with the addition of same coupling agents, the adhesion strength of underfill with polyimide passivation decreased after aging at 85 °C/85 % RH [17].

In summary, many studies have concluded that underfill material property is one of the key factors determining the reliability of the package. The general guideline on the material properties of underfill for flip-chip package can be summarized in Table 8.2. However, one has to keep in mind that different failure modes coexist in a reliability test, which sometimes present conflicting requirements on underfill. For instance, to effectively couple the stress on the solder joints, high modulus underfill is desired. On the other hand, high underfill modulus can lead to high residual stress and therefore die crack. Another example is the filler loading. Low CTE requirement on underfill indicates high filler loading. However, an underfill with higher

Table 8.2 Desirable underfill properties for flip-chip packages

Curing temperature	<150 °C
Curing time	<30 min
T_g	>125 °C
Working life (viscosity double at 25 °C)	>16 h
Viscosity (at 25 °C)	<25kcps
CTE (α_1)	22–27 ppm/°C
Modulus	5–10 GPa
Fracture toughness	>1.3 MPa $m^{1/2}$
Moisture absorption (8 h in boiling water)	<0.25 %
Filler contents	50–70 wt%
Alpha particle emission	<0.005 counts/cm^2/h
Hardness (shore D)	>85
Volume resistivity (at 25 °C)	> 10^{13} Ω-cm
Dielectric constant (at 25 °C and at 1 kHz)	<4.0
Dielectric loss (at 25 °C and at 1 kHz)	<0.005
Extractable ions (e.g., Cl, Na, K, Fe, etc.)	<20 ppm total

filler loading typically has a higher viscosity, causing difficulty in underfill dispensing. The result might be underfill voids and non-uniformity, which would cause reliability issues. Therefore, the choice of underfill highly depends on the application, e.g., die size, passivation material, substrate material, type of solder, and environment conditions the package will be subjected to during application.

8.4 New Challenges to Underfill

As silicon technology moves to 45 nm, 28 nm, 16 nm, and even below 10 nm feature size, the demands for packaging also evolves as the bump pitch gets tighter, bump size smaller, die size larger for future flip-chip packages. As a result, the capillary underfill process faces tremendous challenges. As it was discussed previously, underfill flow problem aggravates as the size of the chip becomes larger and the gap between the chip and substrate gets smaller. Among the emerging development of flip-chip, lead-free solder and low-K (dielectric constant) ILD (interlayer dielectric)/Cu present new challenges to underfill [18].

High-lead and lead-tin eutectic solders have been widely used for chip-package interconnections. Recent environmental legislations toward toxic materials and consumers' demand for green electronics have pushed the drive toward lead-free solders. Alternatives have been proposed using multiple combinations of elements like tin, silver, copper, bismuth, indium and zinc, most of which require increased reflow temperature profiles during the soldering process relative to the well-known tin-lead alloys. Table 8.3 shows some of the common lead-free solders.

Table 8.3 Possible lead-free alloys

Alloy	Melting point
Sn96.5/Ag3.5	221 °C
Sn99.3/Cu0.7	227 °C
Sn/Ag/Cu	217 °C (ternary eutectic)
Sn/Ag/Cu/X(Sb, In)	Ranging according to compositions, usually above 210 °C
Sn/Ag/Bi	Ranging according to compositions, usually above 200 °C
Sn95/Sb5	232–240 °C
Sn91/Zn9	199 °C
Bi58/Sn42	138 °C

Among the several Pb-free candidate solders, the near ternary eutectic Sn–Ag–Cu (SAC) alloy compositions, with melting temperatures around 217 °C, are becoming consensus candidates. The optimal composition 95.4 Sn/3.1Ag/1.5Cu has provided a combination of good strength, fatigue resistance, and plasticity [19]. In addition, the alloy has sufficient supply and adequate wetting characteristics.

The use of Sn/Ag/Cu solder presents two major challenges on the flip-chip assembly process. First, since the melting point of the alloy is more than 30 °C higher than that of the eutectic Sn/Pb alloy, the process temperature is raised by 30–40 °C. The high process temperature has a great impact on the substrate since the conventional FR-4 material has a T_g at around 125 °C and also subjects the attached components to a higher thermal stress. Higher warpage is introduced when the board is subjected to higher temperature reflow. There have been considerable researches in high T_g substrate for lead-free process. The second challenge comes from the flux chemistry. Since the current fluxes in use are usually designed for eutectic Sn/Pb solder, they either do not have high enough activity or do not possess sufficient thermal stability at high temperature. So generally, the wetting behavior of the lead-free solders is not as good as that of the eutectic Sn/Pb solder [20, 21].

With the trends of lead-free solder interconnect, the underfill for flip-chip in package application faces new challenges of compatibility with higher reflow temperature. High temperature reflow causes component damage due to increased level of materials degradation, moisture ingress, and mechanical expansion. Therefore, the thermal stability, adhesion to various interfaces, strength, and fracture toughness of the underfill need to be improved. The SAC alloy does not plastically deform as much as the eutectic PbSn solder. The creep deformation is less at lower stress level and more at higher stress level compared to the PbSn solder, which indicates that the choice of the underfill would depend on the application needs. A temperature cycle with a large temperature difference and lower dwelling times could induce more creep and therefore requires more protection from the underfill [22]. An evaluation of underfill materials for lead-free application conducted by

Intel Corporation [23] showed that majority of the failure occurred during the moisture-sensitive level (MSL) 3 followed by 260 °C reflow. Delamination seemed to be the common failure mechanism after the high temperature reflow. This failure was also correlated to the materials with low filler content and low coupling agent content. In general, materials with high filler content (and therefore low CTE, high modulus, and low moisture uptake) and good adhesion were compatible with the lead-free process.

As the IC fabrication moves toward small feature and high density, the interconnect delay becomes dominant. This calls out for new interconnect and interlayer dielectric (ILD) materials. The Cu metallurgy and low-K ILD has been successfully implemented to increase device speed and reduce power consumption. These low-K materials tend to be porous and brittle, having high CTE and low mechanical strength, compared to the traditional ILD materials such as SiO_2. The CTE mismatch between the low-K ILD and the silicon die creates a high thermomechanical stress at the interface. Therefore, the choice of underfill becomes critical since it not only protects the solder joints by stress redistribution, but also need to protect the low-K ILD and its interface with the silicon. Critical material properties of underfill to achieve reliability requirement for the low-K ILD package include the T_g, CTE, and the modulus. However, the optimal combination of these properties is still controversial.

Five underfills were evaluated for the low-K flip-chip package by Tsao et al. [24]. Both modeling and experimental evaluation indicated that the low T_g and low stress-coupling-index underfills yielded better reliability in the low-K flip-chip package. Two moderately low T_g underfills (T_g between 70 °C and 120 °C) showed good potential in protecting both the solder joints and low-K interface. An underfill with a very low T_g (lower than 70 °C), on the other hand, failed to protect the solder joints during the thermal cycling test. A study conducted by LSI Logic Corp and Henkel Loctite (now called Henkel) Corp [25], on the other hand, indicated that underfills with high T_g and low modulus is advantageous for the low-K flip-chip. The low modulus of the underfill exerts lower stress on the package and therefore reducing the stress on the low-K layer, preventing underfill delamination and die cracking. The high T_g prevents solder bump fatigue by maintaining a low CTE over the temperature cycling. The high T_g, low modulus underfill developed by Henkel exhibited good manufacturability and reliability in the package qualification testing including JEDEC preconditioning, thermal cycling, biased humidity testing, and high temperature storage.

With all the new challenges to the flip-chip and underfill, capillary underfill is still the main packaging technology for flip-chip devices. However, the continuing shrinking of pitch distance and gap height will eventually post limitation on the capillary flow. The industry has started to look for alternatives to capillary underfill. The following sections describe several recent developments in underfill material and process.

8.5 No-Flow Underfill (NUF)

The idea of integrated flux and underfill was patented by Pennisi et al. in Motorola back in 1992 [26]. It triggered the research and development of no-flow underfill process. The first no-flow underfill process was published by Wong et al. in 1996 [27]. The schematic process steps are illustrated in Fig. 8.7. Instead of underfill dispensing after the chip assembly in the conventional process, in a no-flow underfill process, the underfill is dispensed onto the substrate before the placement of the chip. Then the chip is aligned and placed onto the substrate and the whole assembly goes through solder reflow where the chip to substrate interconnection through solder bumps is established while the underfill is cured. This novel no-flow process eliminates the separate flux dispensing and flux cleaning steps, avoids the capillary flow of underfill, and finally combines the solder bump reflow and underfill curing into a single step, hence, improving the production efficiency of underfill process. It is a step forward for the flip-chip to be compatible with surface mount technology (SMT).

The key to the success of a no-flow underfill process lies in the underfill material. The first patent on the no-flow underfill material was filed by Wong and Shi in Georgia Institute of Technology [28]. Two of the most critical properties of the no-flow underfill to enable this new process are the latent curing ability and the build-in fluxing capability. A high-performance no-flow underfill material needs not only all the generic material properties required for the conventional capillary underfill, but also several more specific properties:

1. A NUF must provide sufficient fluxing capability to effectively remove oxides on the solder bumps and metal pads to facilitate the formation of solder interconnects;
2. A NUF should have excellent curing latency that ensures the solder joint formation prior to the underfill curing. Gelled underfill would prevent the molten solder bumps from collapsing onto the contact pads, resulting in low yield of solder joint;
3. A NUF has the ability to be fully cured either in-line during the solder reflowing step or off-line at the temperature below 175 °C;

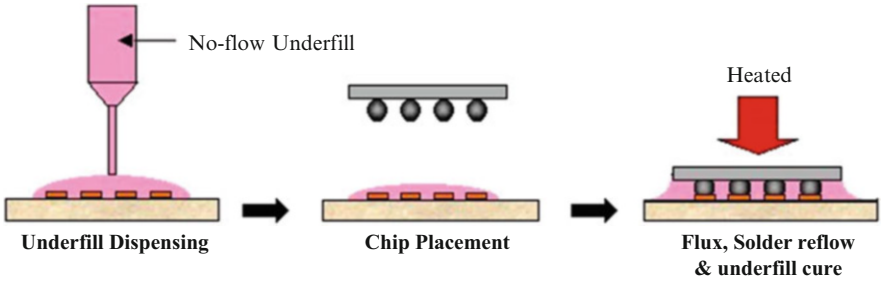

Fig. 8.7 Flip-chip process using no-flow underfill (NUF)

4. A NUF must have low (ideally zero) filler entrapment by formed flip-chip joints. Filler selection is essential and more details will be discussed in a later section.

Many latent catalysts for epoxy resins have been explored for the application of no-flow underfill. In the material system that Wong and Shi designed, Co (II) acetylacetonate was used as the latent catalyst [29, 30], which gave enough curing latency for no-flow underfill. The advantage of metal chelates lies not only in its latent acceleration, but also in the wide curing range they offer. By exploring different metal ions and chelates, the curing behavior of different epoxy resins could be tailored to the application of no-flow underfill for lead-free solder bumped flip-chip [31]. Since lead-free solders usually have a higher melting point than eutectic SnPb solder, no-flow underfill for lead-free bumped flip-chip requires higher curing latency to ensure the wetting of the lead-free solder on the contact pad. Zhang et al. explored 43 different metal chelates and developed no-flow underfill compatible with lead-free solder reflow [31]. Successful lead-free bumped flip-chip on board package using no-flow underfill process has been demonstrated [32].

Despite the importance of the curing process of no-flow underfill, there is little study on the curing kinetics and its relation to the reflow profile. In an attempt to develop systematic methodology to characterize the curing process of no-flow underfill, Zhang et al. used an autocatalytic curing kinetic model with temperature-dependent parameters to predict the evolution of degree of cure (DOC) during the solder reflow process [33]. Figure 8.8 shows the result of DOC calculation of a no-flow underfill in eutectic SnPb and lead-free solder reflow process. If the DOC of the underfill at the solder melting temperature is lower than the gel point, the molten solder would be allowed to wet the substrate and make the interconnection. Another approach is the in-situ measurement of viscosity of no-flow underfill using microdielectrometry by Morganelli et al. [34]. Since the viscosity is related to the ionic conductivity, the dielectric properties of the underfill can be used for the in-situ analysis of the no-flow underfill in the reflow process, which can be used to predict the solder wetting behavior.

The other key property for no-flow underfill is the fluxing capability. In a conventional flip-chip process, flux is used to reduce and eliminate the metal oxide on the solder and metal contact pads, and to prevent them from being reoxidized under high temperature. Instead of applying flux, no-flow underfill is dispensed before the chip placement. Hence, the self-fluxing capability is required to facilitate solder wetting. To achieve this goal, research has been done to develop reflow-curable polymer fluxes [35]. A comprehensive study on the fluxing agent of no-flow underfill material was carried out by Shi et al. [36–38], which included the relationship between the surface composite on Cu pad and the fluxing capability of no-flow underfill, and also the effect of the addition of the fluxing agent on the curing and material properties of no-flow underfill.

The process of no-flow underfill has always attracted much attention in the assembly industry. Voids formation is often observed in many flip-chip no-flow underfill packages. The origin of the voids could be the out-gassing of the underfill,

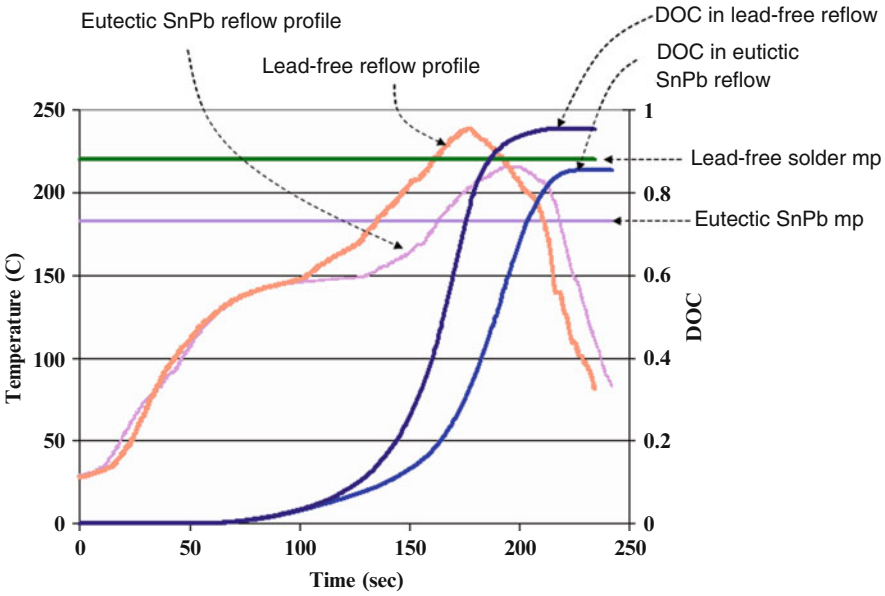

Fig. 8.8 Degree of cure (DOC) evolution of a no-flow underfill in eutectic SnPb and lead-free reflow process

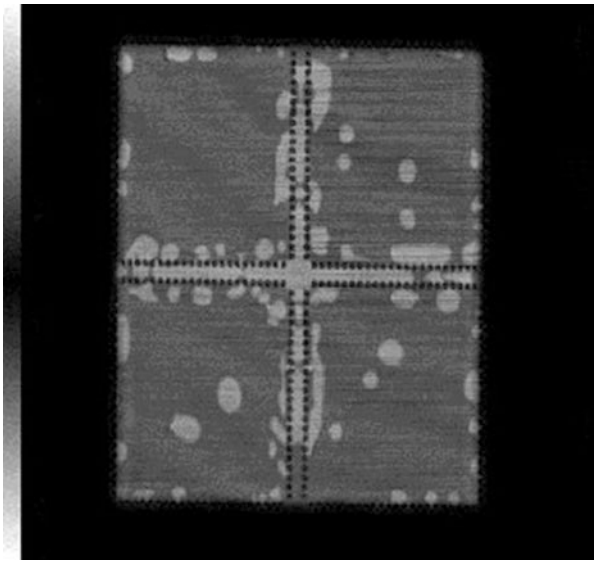

Fig. 8.9 A scanning acoustic microscopy image of a no-flow underfill package (lighter dots are underfill voids)

moisture in the board, and trapped voids during assembly. They are usually tacked to a solder bump or in between two bumps [39, 40]. Figure 8.9 shows an example of underfill voids in a no-flow underfill package observed with scanning acoustic microscope. Voids in the underfill, especially voids near the solder bumps lead to

early failure through a number of ways including stress concentration, underfill delaminate, and solder extrusion. Study has showed that solder bridging might result from the solder bump extrusion through the micro voids trapped between adjacent bumps [41]. The material and process factors influencing the voiding behavior are complicated and interacting. It has been shown that the outgassing of anhydride could cause severe voiding, if the curing latency is high and also the reflow temperature is high; hence, the voiding becomes more prominent in a lead-free reflow process [42]. The important process parameters that affects underfill voiding in a no-flow process include the underfill dispensing pattern, the solder mask design, the placement force and speed, and the reflow profile. [43, 44]. Before assembly, the substrate needs to be baked to dry out any moisture to prevent voiding from the board [40]. It has been shown that in some cases a fast gelation of underfill is desired to minimize the voiding while in other cases, extending duration at high temperature can "push" out the voids [40, 45]. In short, with the right material and process parameters, voiding in no-flow underfill can be minimized. However, the process window is usually very narrow. An important point was raised by Zhao et al. [44] that for a small circuit board where the temperature distribution is more homogenous, it is relatively easy to develop a "good" reflow profile while for complex SMT assemblies involving multiple components and significant thermal mass difference across the board, the optimization of the reflow process presents great challenge.

The reliability of flip-chip no-flow underfill package has been evaluated in many occasions. Discrepancies exist among these reports because the process and reliability of the no-flow underfill package depend largely on the package designs including the size of the chip, the pitch, the surface finish of the pad, etc. Among the earliest reporters on no-flow underfill, Gamota and Melton compared the reliability and typical failure mode of conventional underfill package and no-flow underfill packages [46]. They found that in a conventional underfill assembly, the failure of the assembly mainly resulted from the interfacial delamination between the underfill and the chip passivation. However, with unfilled no-flow underfill, good interfacial integrity was observed, and the assembly failed mainly due to the fracture through the solder interconnects near PCB. Since the no flow underfill was unfilled, the CTE was high. They argued that the relative localized CTE mismatch between the chip, the underfill, and the PCB resulted in a high local stress field which initiated fracture in the solder interconnects. No-flow underfill without silica fillers or very low filler loadings is not only high in CTE, but also low in fracture toughness [47]. Combined with high CTE mismatch, the low fracture toughness leads to early underfill cracking both inside the bulk and in underfill fillet. Fillet cracking causes delamination between the underfill and the die passivation and/or between the underfill and the board, while bulk cracking can initiate solder joint cracking and solder bridging [48]. These all become the common failure modes for flip-chip no-flow underfill package. Efforts have been made to enhance the toughness of the no-flow underfill materials through the incorporation of the toughening agents [49]. The effect of the glass transition temperature (T_g) of the no-flow underfill on the reliability of the package has been controversial. It is

usually believed that the T_g of the underfill should exceed the upper limit of the temperature cycling (125 °C, or 150 °C) to ensure consistent material behavior during the reliability test. However, some tests have shown that low T_g (~70 °C) underfill material performed better in liquid-to-liquid thermal shock (LLTS) [50]. The research by Zhang et al. on the development of non-anhydride-based no-flow underfill [51] also showed that high T_g is not critical to reliability. Although the CTE of the underfill above T_g is much higher than that below T_g, the modulus of the underfill decreases dramatically; so the overall stress in the underfill does not necessarily increase when the environment temperature exceeds its T_g. But high T_g might result in a higher residue stress inside the underfill after the material cools down after curing, which leads to early crack in the underfill.

8.5.1 *Approaches of Incorporating Silica Fillers into No-Flow Underfill*

The previous research has shown that the correlation between the material properties and package reliability in the case of flip-chip underfill is very complicated. It is difficult to separate the effect of each factor since the material properties are often correlated with each other. However, it is generally agreed that low CTE and high modulus are favorable for high interconnect reliability [52]. Hence, the inclusion of silica fillers into the underfill is critical to enhance the reliability. However, since the underfill is pre-deposited on the substrate before the chip assembly in a no-flow process, the fillers are easily trapped in between the solder bump and contact pad, and thus hinder the solder joint formation [53]. Thermo-compression reflow (TCR) has been used to exclude the silica filler from solder joint [54]. The process step is illustrated in Fig. 8.10. In a TCR process, the underfill is dispensed on to a pre-heated substrate. The chip is then picked, bonded to the substrate, and held at an elevated temperature under force for a certain period of time for solder joint formation. The assembly is post-cured afterward. It was found that the bonding force and temperature were important factors influencing yield. A detailed study was carried out by Kawamoto et al. at NAMICS Corporation to determine the effect of filler on the solder joint connection in a TCR-like no-flow underfill process [55]. The study used two different sizes of silica fillers at different loading levels. It

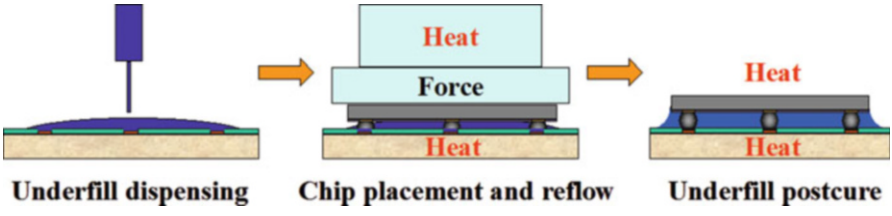

Fig. 8.10 Thermo-compression reflow for flip-chip

was found that good solder connection can be made with underfill with up to 60 wt % filler loading without filler surface treatment. Smaller filler tended to increase the viscosity of the underfill and more fillers were trapped in the solder joints due to larger number of fillers at the same weight percentage loading. The study also found that proper surface treatment of the fillers can lower the underfill viscosity and increase yield at high filler loading.

Other approaches have been explored to incorporate silica fillers into no-flow underfill. In a novel patented process, Zhang et al. used a double-layer no-flow underfill [56], in which two layers of no-flow underfill are applied. The bottom layer underfill has relatively higher viscosity and is not filled with silica fillers. It is applied onto the substrate first, and then the upper layer underfill which is filled with silica fillers is dispensed. The chip is then placed onto the substrate and reflowed, during which the solder joints are formed and the underfill is cured or partially cured. The process flow chart is illustrated in Fig. 8.11. It was demonstrated that high yield was achieved using the upper layer underfill with 65 wt% silica [57]. Further investigation on the process indicated that factors affecting the interconnection yield of the double-layer no-flow underfill are complicated and interacting with each other [58]. The process window is narrow, and the thickness and the viscosity of the bottom layer underfill are essential to the wetting of the solder bumps. And of course, it adds on another step in the flip-chip process and has a higher process cost.

The recent advances in nano-science and nano-technology have enabled innovative research in materials for electronic packaging. It was found that nano-sized silica fillers with surface modification can be mixed with thermosetting resins to provide a uniform dispersion of non-agglomerated particles. Used as no-flow underfill, the nano-composite materials allowed 50 wt% filler loading with good

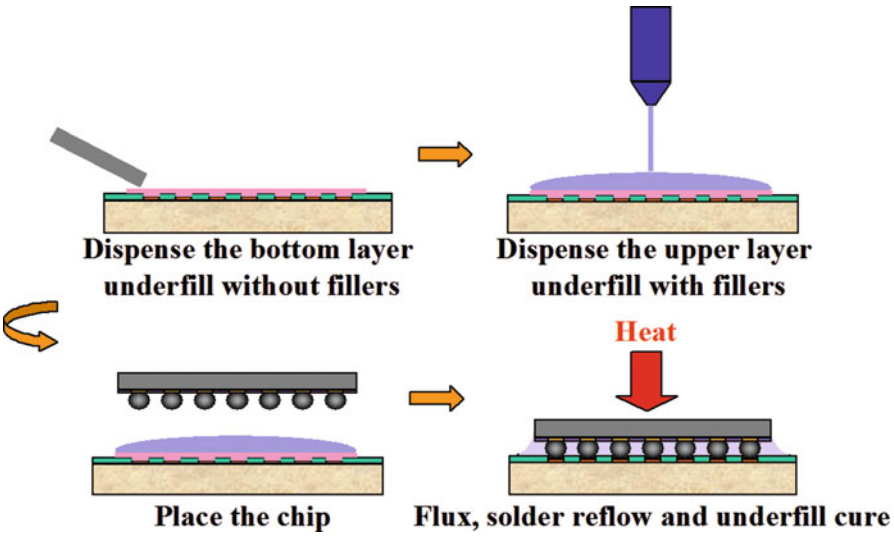

Fig. 8.11 Double-layer no-flow underfill process

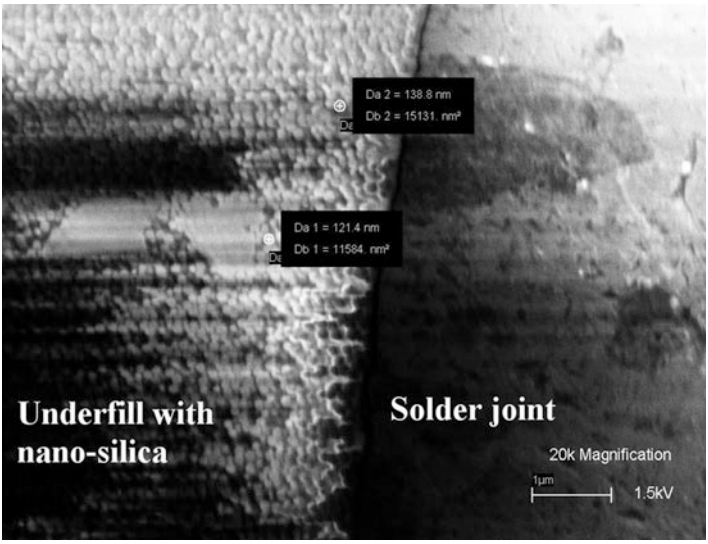

Fig. 8.12 SEM picture of a solder joint with nano-silica incorporated no-flow underfill

interconnect yield [59]. This high-performance no-flow underfill developed by 3M used 123 nm silica filler. With filler loading of 50 wt%, the CTE of the material was 42 ppm/°C and the good interconnect yield was achieved using PB10 die (5 mm × 5 mm, 64 peripheral bumps). A joint research study was conducted by 3M and Georgia Tech on the process and reliability evaluation of the nano-silica incorporated no-flow underfill [60]. Figure 8.12 shows a SEM picture of the solder joint in presence of no-flow underfill with nano-silica fillers. A 1.5 times of increase of characteristics life was observed in the air-to-air thermal cycling (AATC) reliability test with the nano-silica fillers. Although the nano-composite no-flow underfill material shows good potential for a highly reliable flip-chip package using a SMT-friendly no-flow underfill process, the fundamental mechanism of the nano-silica interaction with the solder joints and the underfill is still not well understood. Since nano-size particles have a large surface area and tend to form irregular agglomerations which increase the difficult to be incorporated into a binder, surface treatment of nano-silica is of great importance in formulating an underfill. A fundamental study on the surface modification of nano-size silica for underfill application was carried out by Sun et al. [61]. They found that the type of the surface treatment was the primary factor affecting the property of the formulation. Using an epoxy silane, the authors showed that the viscosity of the composite underfill was greatly reduced.

In summary, the invention of no-flow underfill greatly simplifies the flip-chip underfill process and draws flip-chip toward SMT. A successful no-flow underfill process requires careful investigation on the materials and process parameters. A lot of research efforts have been devoted to the materials, process, and reliability of flip-chip no-flow underfill assembly. Since the underfill does not contain silica filler

and hence behaves differently from the conventional underfill, the failure modes and reliability concerns are sometimes also different from the conventional flip-chip underfill assembly. There are several ways to enhance the reliability of a flip-chip no-flow underfill package. One way is to enhance the fracture toughness of the underfill without degrading other material properties to prevent underfill cracking in the thermal cycling. Or, low T_g and low modulus materials have been used to decrease the stress in the underfill. However, this approach diminishes the role of the underfill as a stress redistribution layer, and although it does decrease the stress in underfill, it cannot prevent solder joint fatigue failure from the thermo-mechanical stress, especially in the case of the large chip, high I/O counts and small pitch size applications. The other way is to add silica fillers into the underfill and match the properties of a conventional underfill. In order to overcome the difficulty of filler entrapment, different approaches have been explored. However, these approaches are less SMT transparent and diminish the low cost purpose of a no-flow underfill process. Nano-silica incorporated no-flow underfill showed potential of a highly reliable flip-chip package with a SMT-friendly no-flow underfill process. However, fundamental understanding of the nano-silica and its interaction with underfill and solder is still lacking, and thus further development is needed to optimize the materials and processes.

8.6 Molded Underfill

With the increasing functionality requirements and the progressively decreasing package size, it usually needs the integration of flip-chip packages into various baseband. In such product lines, the flip-chip is assembled using the traditional capillary underfill process on a strip-based package and subsequently over-molded. The growing pricing pressures and drastically competitive landscape in the electric packaging has made it imperative to reduce the flip-chip assembly cost for assembly subcontractors [62, 63]. Despite continued progress in both the material properties as well as dispensing systems and mechanism, underfill process still remains as one of the slowest processes in the flip-chip assembly flow due to the fact that it needs to be done in a unit-by-unit manner and the inherent capillary flow characteristic of the CUF. To relieve this stress and without compromising product reliability requires, molded underfill (MUF), which combine the over-molding and underfill process together [64, 65], was explored and found to be viable due to the merit of lower material cost and faster throughput due to batch process operation in strip format. Molded underfill is applied to a flip-chip in package via a transfer molding process, during which, the molding compound not only fills the gap between the chip and the substrate but also encapsulates the whole chip [66]. It offers the advantages of combining the underfilling and transfer molding into one step for reduced process time and improved mechanical stability [67]. It also utilizes EMCs which have long been proven to provide superior package reliability. Compared with the conventional underfill which is usually filled with silica at around 50–70 wt%, molded

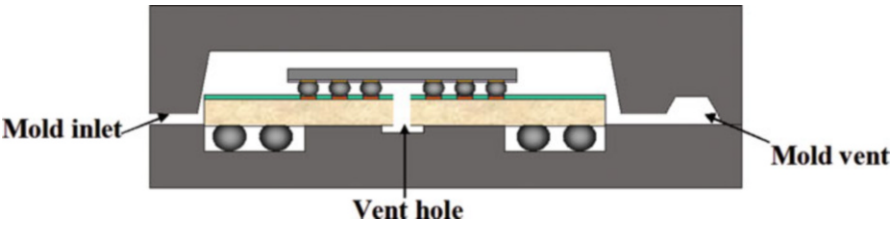

Fig. 8.13 Design of flip-chip BGA with molded underfill (MUF)

underfill can afford a much higher filler content up to 80 wt%, which offers a low CTE closely match with the solder joint and the substrate. Also, compared with the conventional molding compound, molded underfill requires fillers in smaller size, which also can contribute to lower the CTE of the material [68]. Molded underfill is especially suitable for flip-chip package to improve the production efficiency. It was reported that a fourfold production rate increase can be expected using molded underfill versus a conventional underfill process [69].

Molded underfill resembles the pressurized underfill encapsulation [70] in the mold design and process except that the materials in use are not liquid encapsulants that only fill up the gap between the chip and the substrate, but rather molding compounds that over-mold the entire components. Figure 8.13 shows a design of the mold for flip-chip ball grid array (FCBGA) components using molded underfill.

The design of the mold faces the challenge that the flip-chip geometry has a higher resistance to the mold flow, such as the decreasing stand-off height and bump pitch, so that air might be trapped under the chip. In fact, voids have been observed in the molded underfill packages using acoustic microscope [71]. Several molding processes can be used to minimize this geometry effect [72]. One way is to use mold vents as shown in Fig. 8.13 and to use also geometrical optimization to create similar flow resistance over and under the chip. One can also use vacuum-assisted molding to prevent air entrapment. Another approach is to design a cavity in the substrate as shown in Fig. 8.13. Though it requires a special design on the substrate, this method has proved to be a robust process and is commonly adopted. By choosing the suitable MUF filled with fine filler size and optimizing vacuum mold process, very small gaps of the order of 50 μm can be filled without trapping any mold voids [62].

Important process parameters in a molded underfill process include the molding temperature, clamp force, and injection pressure [54]. High temperature molding is favored for lower viscosity of the molding compound and hence better flow properties and less stress on the solder joint. However, the upper limit of the molding temperature is the melting point (Tm) of the solder material. Temperature near Tm combined with high injection pressure might cause the solder to melt and even the die to be "swept" away from the site. Also low T_g substrate is likely to be damaged at high molding temperature and high clamp force. The overflow of the molding compound might contaminate other contact pads or testing pads on the substrate. Bump cracking and die cracking are likely to occur as a result of high

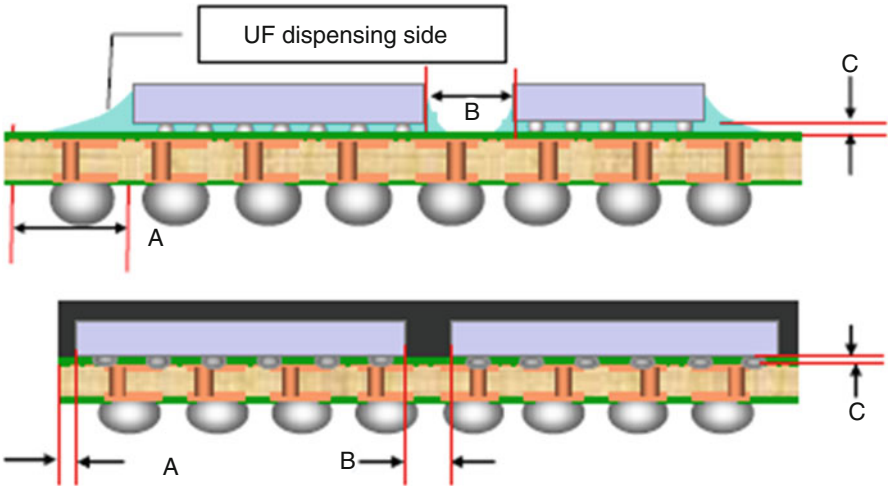

Fig. 8.14 Package design rules for the flip-chip with CUF and MUF [62]

Table 8.4 Package design rules for the flip-chip with CUF and MUF [62]

Design rules		CUF	MUF
A	Package edge to die edge	0.4–1.3 mm	0.1–0.2 mm
B	Clearance between dies	0.8–1.0 mm	0.3–0.4 mm
C	Bump standoff height	30–50 μm	40–60 μm

injection pressure. In short, a successful molded underfill process requires a combined effort in material selection, mold design, and process optimization. But the potential cost reduction and reliability enhancement of molded underfill is attracting great efforts in the industry.

For designing a flip-chip package, the MUF poses some key advantages over CUF. In the CUF approach, fillets around the die along all four sides should be formed using the capillary dispense. This underfill fillet has the largest width at the dispense side. So, minimum clearances between the die edge to package edge as well as between two dies or a die and a neighboring passive component are needed for the package designer. While for the MUF approach, fillets are not necessary, which will keep the die and/or the component much closer to each other and enable a smaller package size and lower the package or substrate cost. Also, electronic performance will be improved with lower inductance path between the capacitor and power bumps on the die. Figure 8.14 and Table 8.4 illustrate the comparison of production package design rules for flip-chip using MUF and CUF. From the package design considerations, MUF needs a smaller keep out zone between dies, die-and passives, and die-package clearance as compared with the traditional CUF. The reduced package size indirectly helps in saving package cost by about 20–25 %, and much higher cost saving can be realized in the multiple die stacks [62, 63]. Overall, the evolving requirements in the IC products demanding smaller,

faster, multifunction, and cheaper packages have put the package manufacturing under scrutiny and the design benefits provided by MUF have caught the eyes of product designers and package assemblers alike. Especially for the ongoing 3D stacks technology, the molded underfill could be efficiently used to optimized the structure and process of package which will be give detail descriptions in the following 3D stacks session 8.8.

8.7 Wafer Level Underfill

The invention of no-flow underfill eliminates the capillary flow and combines fluxing, solder reflow, and underfill curing into one step, which greatly simplifies the underfill process. However, as pointed out in the previous text, no-flow underfill has some inherent disadvantages including the unavailability of a heavily filled material, which is a big concern for high reliability packages. Also, no-flow process still needs individual underfill dispensing step and therefore is not totally transparent to standard SMT facilities. An improved concept, wafer level underfill, was proposed as a SMT-compatible flip-chip process to achieve low cost and high reliability [73–76]. The schematic process steps are illustrated in Fig. 8.15. In this process, the underfill is pre-applied either onto a bumped wafer or a wafer without solder bumps, using a proper method, such as printing or coating. Then the underfill is B-staged and wafer is diced into single chips. In the case of unbumped wafer, the wafer is bumped before dicing when the underfill can be used as a mask. The individual chips are then placed onto the substrate by standard SMT assembly equipment.

It is noted that in some types of WLCSP, a polymeric layer is also used on the wafer scale to redistribute the I/O and/or to enhance the reliability. However, this polymeric layer usually does not glue with the substrate and cannot be considered as underfill. The wafer level underfill discussed here is an adhesive to glue chip and

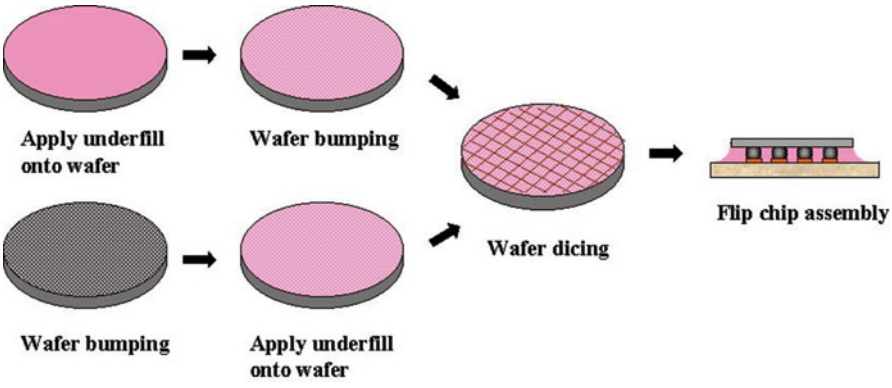

Fig. 8.15 Process steps of wafer level underfill

substrate together and functions as a stress-redistribution layer rather than a stress-buffering layer. The attraction of the wafer level underfill lies in its low cost potential (since it does not require a significant change in the wafer back-end process) and high reliability of the assembly enhanced with the underfill. However, the wafer level underfill faces critical material and process challenges including uniform underfill film deposition on the wafer, B-stage process for the underfill, dicing and storage of B-staged underfill, fluxing capability, shelf-life, solder wetting in presence of underfill, desire for no post-cure, and reworkability. Since the wafer level underfill process suggests a convergence of front-end and back-end of the line in package manufacturing, close cooperation between chip manufacturers, package companies, and material suppliers are required. Several cooperated research programs in this area have been carried out [77–79]. Innovative ways of addressing the above issues and examples of wafer level processes are presented in this chapter.

In most wafer level underfill process, the applied underfill must be B-staged before the singulation of the wafer. The B-stage process usually involves partial curing, solvent evaporation, or both, of the underfill. In order to facilitate dicing, storage, and handling, the B-staged underfill must appear solid-like and possess enough mechanical integrity and stability after B-stage. However, in the final assembly, the underfill is required to possess "reflowability", i.e., the ability to melt and flow to allow the solder bumps to wet the contacting pads and form solder joints. Therefore, the control of the curing process and the B-stage properties of the underfill is essential for a successful wafer level underfill process. A study conducted in Georgia Tech utilized the curing kinetics model to calculate the degree of cure (DOC) evolution of different underfills during solder reflow process [80]. Combined with the gelation behavior of the underfills, the solder wetting capability during reflow was predicted and confirmed experimentally. Based on the B-stage process window and the material properties of the B-staged underfill, a successful wafer level underfill material and process was developed. Full area array at 200 μm pitch flip-chip assembly with the developed wafer level underfill was also demonstrated [81] as shown in Fig. 8.16.

The above study shows that the control of B-stage process of the wafer level underfill is critical to achieve good dicing and storage properties and the solder interconnect on board-level assembly. One way to avoid dicing in presence of non-fully cured underfill is presented in Fig. 8.17, a wafer scale applied reworkable fluxing underfill process developed by Motorola, Loctite and Auburn University [77]. Since uncured underfill materials are likely to absorb moisture that leads to potential voiding in the assembly, in this process, wafer is diced prior to underfill coating. Two dissimilar materials are applied: the flux layer coating by screen or stencil printing and the bulk underfill coating by a modified screen printing to keep the saw street clean. The separation of the flux from the bulk underfill material preserves the shelf-life of the bulk underfill as well as prevents the deposition of fillers on top of the solder bump so as to ensure the solder joint interconnection in the flip-chip assembly. In this process, no additional flux dispensing on board is

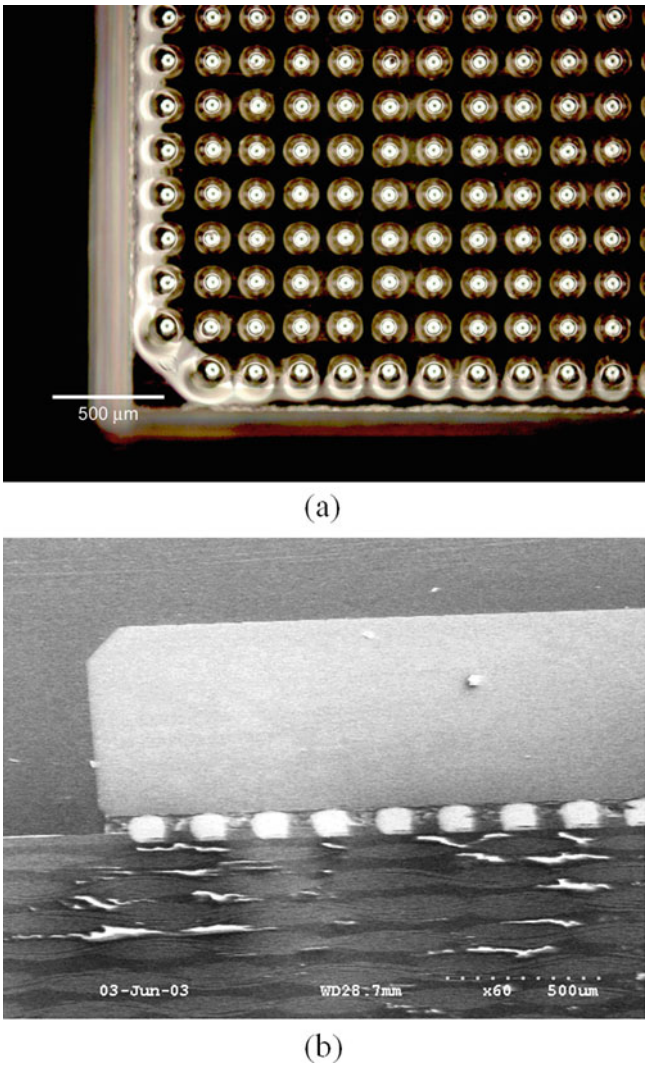

Fig. 8.16 (**a**) An optical image of wafer level underfill coated wafer with a 200 µm bump and (**b**) a cross-sectional image of solder joints after the die assembled on the substrate

needed and hence the underfill needs to be tacky in the flip-chip bonding process to ensure the attachment of the chip to the board, as discussed in the previous text.

Underfill deposition on a wafer using liquid material via coating or printing requires subsequent B-staging, which is often tricky and problematic. The process developed by 3M and Delphi-Delco circumvents the B-stage step using film lamination [82]. The process steps are shown in Fig. 8.18, in which the solid film comprised of thermoset/ thermoplastic composite is laminated onto the bumped wafer in vacuum. Heat is applied under vacuum to ensure the complete wetting of

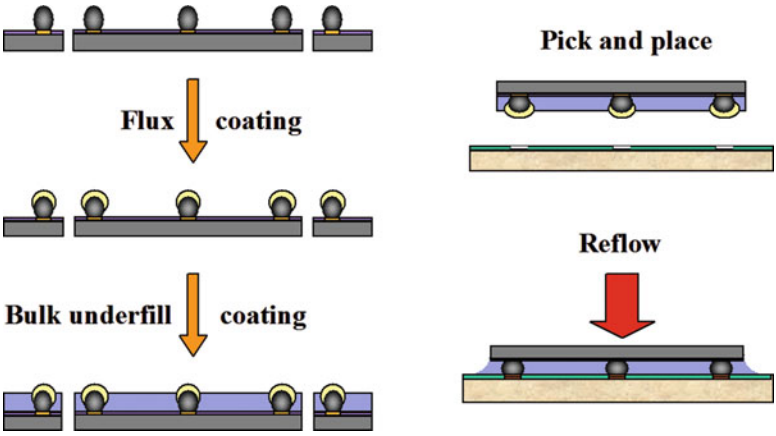

Fig. 8.17 A wafer scale applied reworkable fluxing underfill process

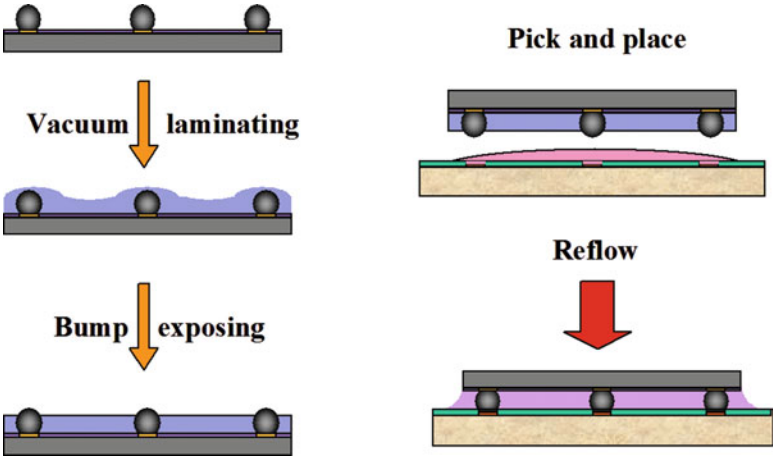

Fig. 8.18 A wafer-applied underfill film laminating process

the film over the whole wafer and to exclude any voids. Then a proprietary process is carried out to expose the solder bump without altering the original solder shape. The subsequent flip-chip assembly is carried out in a no-flow underfill-like process in which a curable flux adhesive is applied on the board and then the assembly is reflowed.

Wafer level underfill can also be applied before the bumping process. Figure 8.19 shows a multi-layer wafer-scale underfill process developed by Aguila Technologies, Inc. [83]. The highly filled wafer level underfill is screen printed onto an unbumped wafer and then cured. Then this material is laser-ablated to form microvias that expose the bond pads. The vias are filled with solder paste. After reflowing, solder bumps are formed on top of the filled vias. The flip-chip assembly

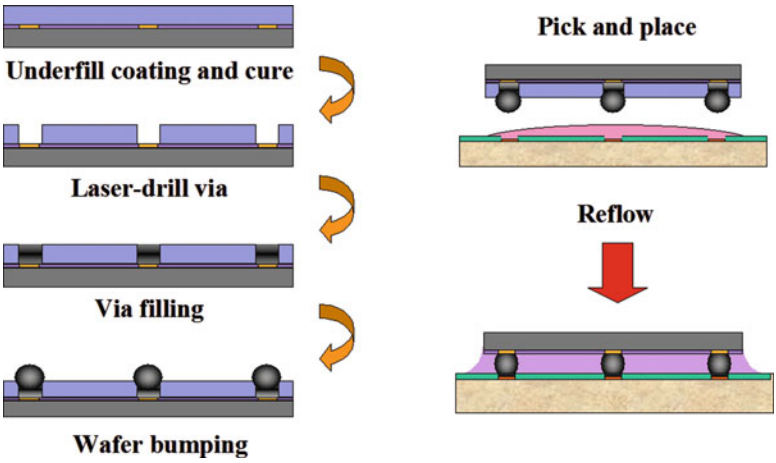

Fig. 8.19 A multi-layer wafer-scale underfill process

is similar to no-flow underfill process again with a polymer flux dispensed onto the board before chip placement.

One similarity among all these three processes is the separation of flux material from the bulk underfill. Wafer level underfill process provides the convenience of separating different functionalities by using dissimilar materials so that "the one magic material that solves everything" is not required. However, it is likely to create inhomogeneity inside the underfill layer, the impact of which on the reliability is not fully understood.

A novel photo-definable material which acts both as a photoresist and an underfill layer applied on the wafer level was reported by Georgia Tech [84]. In the proposed process as shown in Fig. 8.20, the wafer level underfill is applied on the un-bumped wafer, and then is exposed to the UV light with a mask for crosslinking. After development, the un-exposed material is removed and the bump pads on the wafer are exposed for solder bumping. The fully cured film is left on the wafer and acts as the underfill during the subsequent SMT assembly after device singulation. A polymeric flux is needed during the assembly for holding the device in place on the substrate and providing fluxing capability, a process similar to the dry film laminated wafer level underfill. In order to enhance the material property, the addition of silica fillers is necessary. In this case, nano-sized silica fillers were used to avoid UV light scattering which hinders the photo-crosslinking process. The nano-sized fillers also resulted in an optical transparent film on the wafer to facilitate the vision recognition during dicing and assembly process. The photo-definable nano-composite wafer level underfill presents a cost-effective way of applying wafer level underfill and has potentially fine-pitch capability.

The WL-NCF (wafer level non-conductive film) has become one of the promising interconnection adhesives for flip-chip assembly [85]. The underfill film is manufactured in a separate process yielding a B-staged and highly-filled underfill

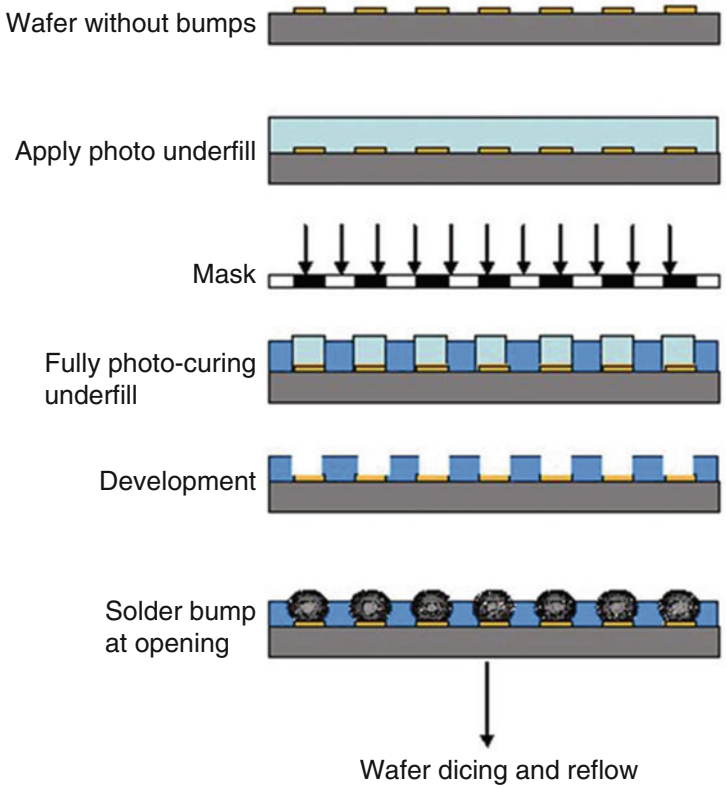

Fig. 8.20 A photo-definable wafer level underfill process

film with a uniform thickness. Because NCFs have many advantages such as low cost, easy handling, and fine pitch application, they can be laminated on the active side of bumped wafers by a hot roll laminator without voids. A WL-NCF can be supplied as a roll by being sandwiched with plastic film like PET (polyethylene terephthalate) or so [86]. The process flow of using WL-NCF is given in Fig. 8.21. The WL-NCF needs to possess the following properties:

- Adequate flow and wetting to allow the NCF to flow over the features on the wafer front side.
- Good adhesion to the wafer front side and good mechanical properties to prevent the NCF from being damaged during the dicing process.
- Rapid softening, flow, and wetting of the substrate during thermocompression bonding.

Since wafer level underfill is a relatively new concept and most researches are still in the process and material development stage, there are few reports on the reliability of a flip-chip package using wafer level underfill. Although there is no

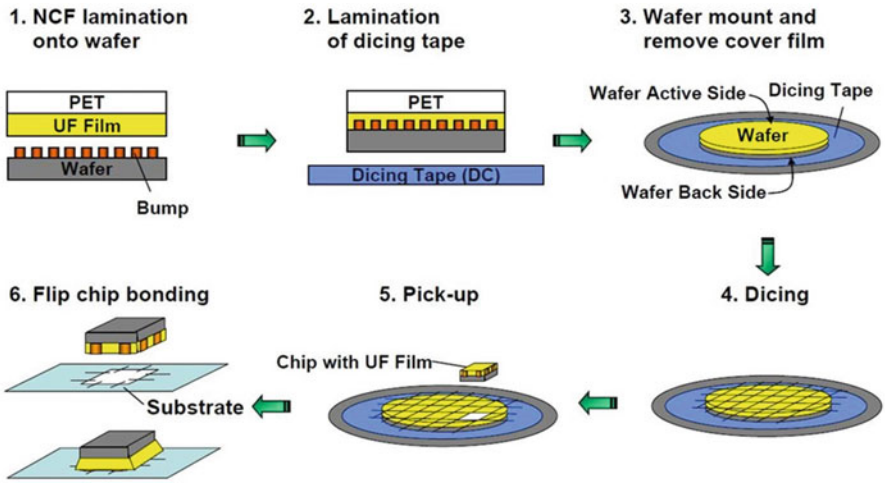

Fig. 8.21 A non-conductive film underfill process

standard process for wafer level underfill yet, the final decision might depend on the wafer and chip size, bump pitch, package type, etc. Like wafer level CSP, multiple solutions may co-exist for wafer level underfill process.

8.8 Underfill for 3D Stacks

Under the guidance of Moore's law, over the past few years, the IC chip has been significantly reduced in size and electronic devices have undergone various packaging improvements. The target of packages is further to raise silicon packaging efficiency [87]. A solution closely followed at the moment is the development of three dimension (3D) ICs and 3D packaging, which is miniaturization, faster interconnections, power saving, and limitation to node transition in the front-end process. Typical 3D IC package structure designs are built around the through silicon via (TSV), micro-bumps interconnections, and thinned wafer/dies face-to-face interconnections with micro-bumps [87–89]. These are silicon "die"-based structure. In developing the 3D IC technologies, there are quite a lot of challenges involved, the development and scaling of TSVs and micro-bumps, the handling of ultra thinned wafers, the stacking options needed, and the selection of the right type of underfill materials. Especially, a key element for improving 3D stacking and packaging reliability and cost-effectiveness is the choice of the right underfill materials, as the size of bumps and pitches have been reduced which indicate the lower height of the underfill filling gaps. Then, it could be difficult to make traditional capillary type underfills and underfilling process to work due to the very narrow gaps and fine bump pitches. So, new kind of underfill materials and underfilling concepts become inevitable. The use of pre-applied underfills, such as

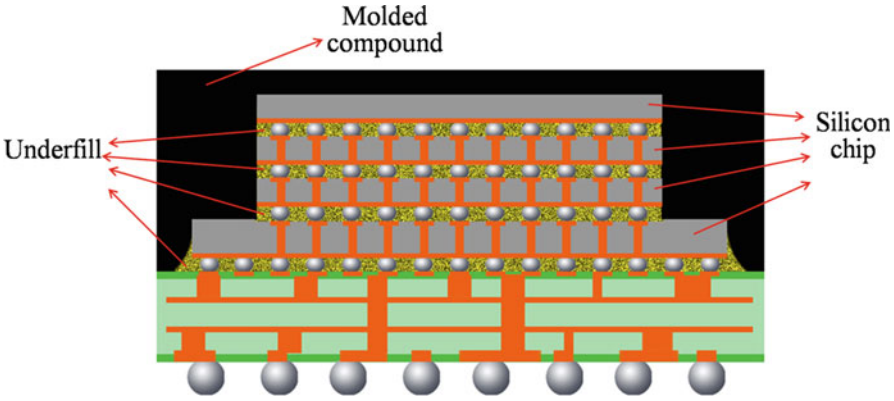

Fig. 8.22 Typical stack-up package with multi-die stack and underfills

the wafer level underfill and no flow underfills in combination with the thermocompression bonding process, has shown to be a viable solution for 3D stacking (Fig. 8.22) [87].

When using the NUF type underfill in the 3D stacking process, it would be better to consider the amount of time needed to dispense the material on both the wafer and locally (on the backside) of each die to be stacked, and also the consider whether to do local thermal-compression bonding or collective bonding [87]. When doing the local thermal compression bonding, the NUF was first dispensed on the wafer, followed by die-to-wafer population, then collective thermo-compression bonding and finally dicing, the whole process flow is shown in Fig. 8.23 [87]. Also, the die-to-wafer and collective thermo-compression bonding process will have to be repeated several times according to the number of chips to be stacked. The drawback of this process is that amount of handling is needed to transfer the wafer back and forth between the dispenser, the pick and place, and the collective bonder. This frequent transfer process might lead to the misalignment on individual dies and get lower assembly efficiency.

According to section 8.7, the wafer level underfills are underfill materials that are directly applied at wafer level by either a spin coating (liquid form) or lamination (film type) process. Using the wafer level underfill significantly reduces the processing time as compared to the other dispensable underfillm, such as CUF and NUF, and has become the main underfill choice for the 3D stacks. It has been reported that the wafer level underfill could be able to fill very narrow underfill gaps ($<$15 μm) and devices with very fine micro-bumps pitches ($<$40 μm) [87, 89].

The other prevailing underfill approach is the molding technique using the fine filler filled molded underfill helped by the vacuum [90]. As shown in Fig. 8.24, the stacked chips were first placed into the vacuum chamber of a dispensing machine at atmospheric pressure and the stage temperature of the vacuum underfill tool was controlled and set to suitable temperature depending on the properties of the used underfill material. After putting the sample on the stage in the vacuum chamber, the

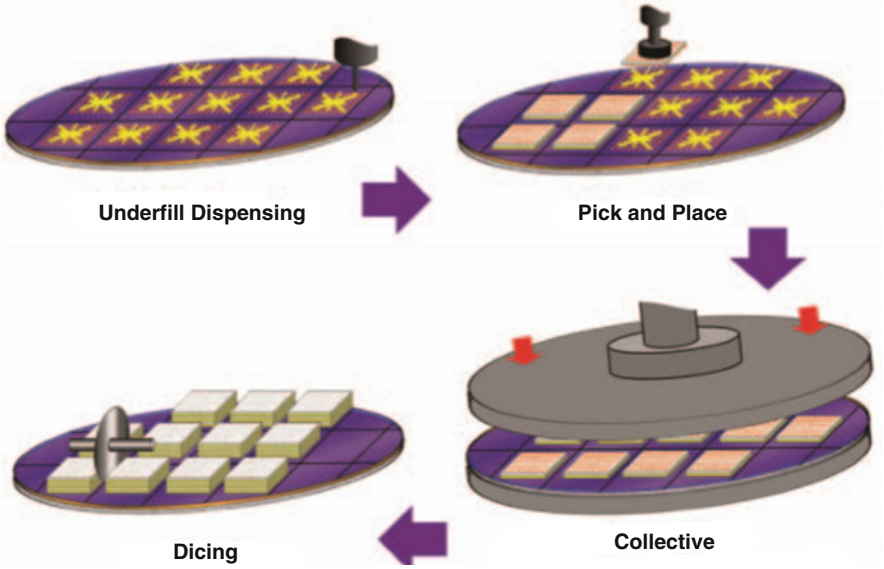

Fig. 8.23 Concept flow for die-to-wafer and collective thermo-compression bonding using NUF [87]

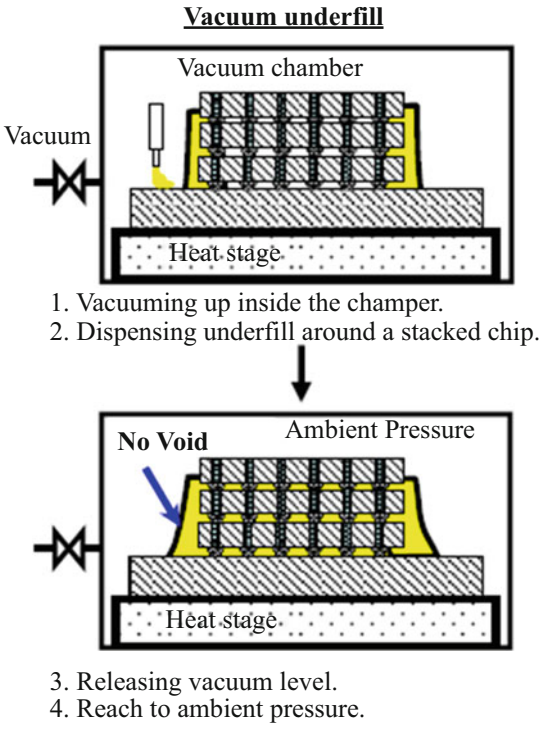

Fig. 8.24 Comparison of standard capillary underfill deposition with the vacuum underfill process for the 3D chip stack [90]

chamber is evacuated to a target vacuum pressure and a valve dispenses the underfill material around the each stacked chip on the substrate, and the vacuum is released. When the vacuum is filled with air at normal atmospheric pressure, the pressure beneath the stacked chip is lower than the external pressure, and the pressure difference push the underfill dispensed all around each stacked chip. By using this method, the underfill was uniformly injected into the 6 μm gaps between three-layer stacks of 70 μm chips and no voids were observed in any of the gaps [90].

Other new underfill dispensing process has been developed in recent years. Li et al. developed the thorough silicon underfill dispensing process for the 3D die/interposer stacking [91]. In this process, the TSV functions as entrances for fluid dispensing or paths for fluid flow. TSV dispensing is applied after the flip-chip interconnects are formed as shown in Fig. 8.25.

8.9 Nanocomposites Underfill

Among the various materials in the underfill formulation, filler plays an important role in reducing overall CTE of the underfill material, minimizing moisture uptake, and eventually improving device reliability. As a general rule of thumb, the maximum filler particle size should be less than one-third of the gap height between chip and substrate [92]. Otherwise, the particles will be trapped in the gap. The shrinking gap in the flip-chip package continues to demand the underfill material filled with smaller and smaller particle size. Different from the conventional underfill in which the size of silica particles is in the micrometer range, the filler size has been quickly decreased to below single digital micron in diameter in most advanced underfill formulation. The nanosilica ranging in diameter from 20 nm to 550 nm has been investigated as the filler for underfill application [93–98]. When using the nanosized silica as filler, the uniformly dispersed nanosized filler particles would provide an exclusively high interfacial surface area between the filler and epoxy matrix, this extensive interfacial surface area will greatly improve thermal-mechanical properties of the underfill.

The reduction of filler size is important for underfill processes to address the concerns about the shrinking of pitch size and gap height, and filler settling problems. Moreover, the fine size filler is also the most critical factor to ensure the solder wetting and interconnect formation during a no-flow process. Since the no-flow underfill is applied to the substrate prior to the placement of the IC chip, conventional micron size fillers have a great probability of being entrapped between the solder bumps on the chip and the contact pads on the substrate [99]. The trapped fillers prevent solder wetting on contact pads and thus significantly reduce the solder joint yield and the electrical continuity [100]. Thus, the micron size fillers have to be replaced by the nano size fillers in the no-flow process. It was found that silica in the size region of 100–150 nm were less likely to be trapped in the flip-chip assembly and a nanocomposite no-flow underfill with 50 wt% silica filler of 120 nm

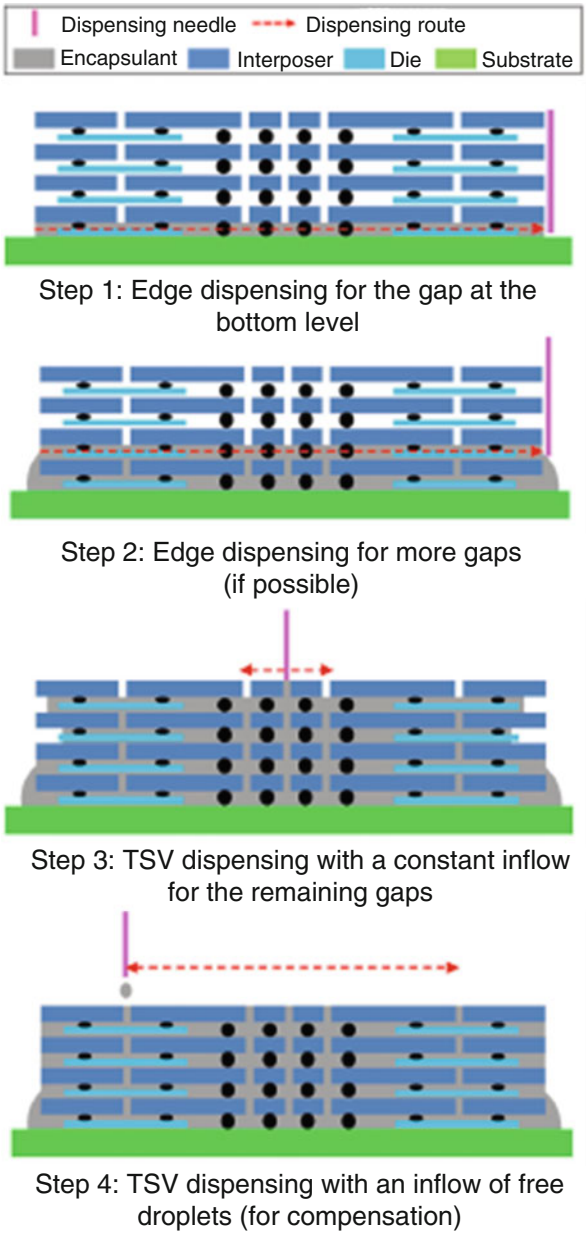

Fig. 8.25 Underfill dispensing on multiple layers [91]

size has been demonstrated to offer both high solder joint yield and package reliability in air-to-air thermal cycling test [101].

The wafer level underfill also faces to many challenges regarding the filler addition. Besides the similar problems related with the solder wetting as no-flow underfill, the vision recognition in the wafer level underfill process becomes a new

issue because the wafer is covered with underfill [102]. During the pick-and-place vision process of wafer level packaging, the solder bumps are used as locating features in place of fiducials. In the presence of underfill, the apparent size and shape of the bumps may be altered. Especially, the highly filled underfill with large filler particles makes the bumps almost invisible due to the light scattering. In addition, the three-dimensional topography of an uncoated bumped die aids vision recognition with the formation of shadows around the bumps. These shadows enhance the camera's ability to sense the bright bump against the darkness of the shadows. With a coated die, the topography is flattened, further complicating the recognition step. The superior optical transparency of nanocomposite underfill will be helpful to solve this problem. It was found that the underfills with nanosilica were almost as transparent as pure epoxy in visible region (400–700 nm) because the filler has a particle size smaller than the wavelength of the visible light. The nano size fillers show superior properties in the underfill applications and have the potential to solve the problems associated with the large size filler, such as clogging flow in the fine pitch package, filler settling, hindering the solder wetting, and disturbing the vision recognition during assembly. Nanocomposite underfills will provide significant reliability improvement for the large-area flip-chip packages. However, challenges remain and some fundamental problems need to be addressed before the successful implementation of the nanocomposite underfill to meet the requirements of low cost, high yield, and high reliability for flip-chip assembly. The filler particle dispersion becomes a dominant factor for the nanocomposite underfill application. The degree of dispersion, the interaction between the dispersed phase and the dispersion medium, and the interaction between the particles can influence the materials' properties.

Other important issue for the new direction of underfill is to develop underfill with high thermal conductivity. Along with the die size of device become smaller, fine pith, narrow gap and multi-chip stacking are the market mainstream for the high-performance 3D IC technology. Therefore, heat dissipation is the most important issue for this kind of electronic device to avoid internal heating from device during operation. Generally speaking, the major heat-dissipation bottle neck is the solder ball array interface between die and substrates or individual dies. Several works were proposed to develop new kinds of underfill with high thermal conductivity, these fillers contains alumina, aluminum nitride, silicon carbide, alumina, diamond, and boron nitride [103–107]. Using this underfill, the heat will be dissipated through PCB or chip, passing through the underfill which will significantly enhance the reliability of electronic devices (Fig. 8.26).

8.10 Summary

Flip-chip offers many advantages over other interconnection technologies and has been practiced in many applications. Underfill is necessary for a reliable flip-chip on organic package but is process-unfriendly and becomes the bottle-neck of a high

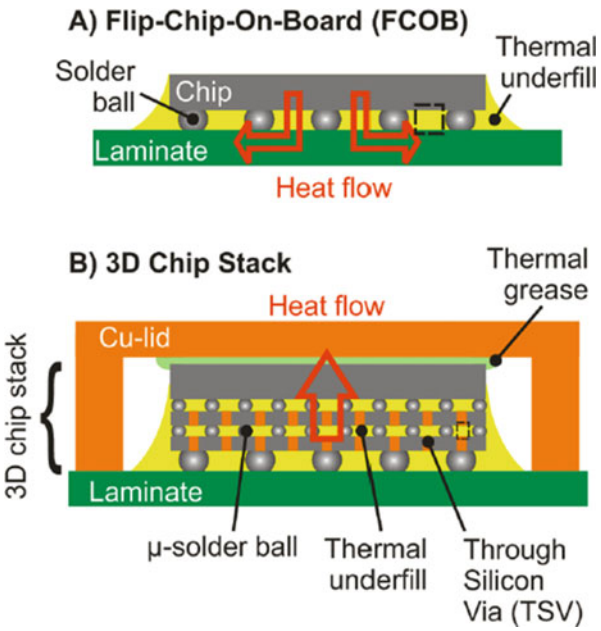

Fig. 8.26 Heat dissipation in a FCOB without backside heat sink (**a**) and a high-performance 3D chip stack package (**b**) [105]

production flip-chip assembly. As silicon technology moves to nanometer nodes with feature size even less than 28 nm, shrinking pitch and gap distance, as well as the introduction of lead-free solder and low-K ILD/Cu interconnect present new challenges to underfill materials and process. Many variation of the conventional underfill have been invented to address the problem, among which, the newly developed no-flow underfill, molded underfill, and wafer level underfill have attracted much attentions. The no-flow underfill process simplifies the conventional flip-chip underfill process by integrating flux into the underfill, eliminating capillary flow, and combining solder reflow and underfill cure into one step. However, the pre-deposited underfill cannot contain high level of silica filler due to the interference of filler with solder joint formation. The resulting high CTE of the underfill limits the reliability of the package. Various ways have been explored to enhance the reliability through improved fracture toughness of the underfill material, low T_g and low modulus underfill, and the incorporation of fillers using other process approaches. Molded underfill combines underfill and over-mold together and is especially suitable for flip-chip in package to improve the capillary underfill flow and the production efficiency. Careful material selection, mold design, and process optimization are required to achieve a robust molded underfill process. Wafer level underfill presents a convergence of front-end and back-end in packaging manufacturing and may provide a solution for low cost and high reliable flip-chip process. Various material and process issues, including underfill deposition, wafer dicing with underfill, shelf-life, vision recognition, chip placement, and solder wetting with underfill, have been addressed through novel material development and different process approaches. Although the research is still in the early

stage and there is no standard in the process yet, there have been considerable successes in demonstrating the process, which looks promising for the future packaging manufacturing. All of these three approaches require close cooperation between the material suppliers, package designers, assembly companies, and maybe chip manufacturers. A good understanding in both the materials and the processes and their inter-relationship is essential to achieve successful packages.

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