Chapter 14
Interconnect Quality and Reliability of 3D Packaging

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14.1 Introduction

The challenges to quality and reliability for 3D IC packaging technology include but not limited to the followings. (1) New manufacturing processes that heavily involve through silicon via (TSV), microbumping, die stacking, multiple high temperature reflows; (2) New materials including new under bump metallurgies (UBM) with new Pb-free solder materials mainly based on intermetallic compounds, new underfill materials that flow into thin gap for microbumps; (3) Miniaturization in size, where solder joint is 5–10× smaller than C4 solder joints, which translates to a volume shrinkage by three orders of magnitude; (4) Thermal mechanical environment changes: Joule heating has to find new ways to dissipate and thermal gradient and thermal stress concentration are built up across layers; (5) Any new electromigration and thermomigration concerns should be studied, including failure in redistribution layers; (6) Reliability requirement changes due to new failure modes transition from desktop, laptop to mobile devices [1].

In this chapter, we discuss quality and reliability of interconnects in 2.5D IC and 3D IC packaging technology—microbump, TSV, UBM and copper interconnects, and we compare them to the quality and reliability concerns observed in the existing interconnects. We shall cover microstructure changes and failures driven by mechanical stressing, electromigration (EM), and thermomigration (TM). This way we can see how the transition, for example, from C-4 joints to microbumps

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may affect the failure modes. On mechanical stressing, we emphasize the brittle nature as well as microvoid formation, especially Kirkendall void formation in microbumps. A string of voids in a brittle material can easily lead to fracture damage [2]. The interest in mechanical failures is because for mobile and wearable devices, the frequency of impact and dropping to the ground is high. On EM and TM in microbumps, we emphasize the enhanced failure mode due to Joule heating.

14.2 Quality Challenges for 3D Packaging

3D IC devices involve more complicated stacking processes where interconnect size becomes much smaller. Materials properties used in 3D IC influence the quality and reliability of electronic assemblies. For example, PCB substrate, silicon, microbump, copper layer and underfill have very different materials properties. Taking thermomechanical properties as example, Table 14.1 summarized the elastic modulus, coefficient of thermal expansion (CTE), and Poisson's ratio in room temperature. With more layers of stacking together in *z*-dimension, this becomes more challenging for 3D packaging processes to ensure both quality and reliability sound. One of the most obvious change in the continuous miniaturization of solder joint is the increase of volume fraction of intermetallic compounds (IMC) so that a microbump in 3D IC technology could be completely transformed into IMC. In other words, it is IMC instead of solder itself that plays a dominant role in determining microbump properties and reliabilities [3]. While IMC is electrically conducting, it is widely known to be mechanically brittle, see Table 14.2. Hence, the first concern is mechanical reliability. Besides its own brittle nature, its influence on low-*k* dielectrics on chip is also worth noticing. It is known that low-*k* dielectrics are susceptible to damage from chip-packaging interaction during thermal cycling. The presence of Cu-Sn IMC-based microbump has caused crack formation in the low-*k* dielectric layer [4]. This is one of the critical reasons that electronic industry depends on 2.5D IC for the reduction of chip-packaging

Table 14.1 Material properties used in 3D packaging

Materials	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/°C)
PCB (FR4)	*xy*: 12.2–22, *z*:1.6–10	0.19–0.39	*xy*: 13–18, *z*:60
TSV/Pad (copper)	120–130	0.3–0.36	16.5–17
Solder (63Sn37Pb)	24.8–31.7	0.32–0.4	23.9–25
Solder (Sn3.8Ag0.7Cu)	44.4–58.0	0.35–0.4	23.5–26
Substrate (BT resin)	19–26	0.18–0.39	13–14
Solder mask	2.5–4.9	0.3–0.48	30–95
Silicon	106.9–169	0.22–0.35	2.3–2.7
Mold compound	12.5–16	0.25–0.35	20–25
Underfill	4.4–6	0.35–0.4	22–45
Die adhesive	3.45–7.4	0.27–0.35	45–100

Table 14.2 Properties of materials constituents of microbumps used in 3D IC technology [7]

Materials / Parameters	Cu_6Sn_5	Cu_3Sn	Ni_3Sn_4	Sn	Cu	Ni
Young's modulus (GPa)	116.89 ± 2.04 [8]	133.49 ± 4.44 [8]	141.12 ± 3.85 [8]	50	120	186 [9]
Indentation hardness (GPa)	6.35 ± 0.20 [8]	6.32 ± 0.15 [8]	6.31 ± 0.16 [8]	0.11 ± 0.05 [10]	1.7 ± 0.2 [10]	2.8 [11]
Yield strength (MPa)	2009 ± 63 [12]	1787 ± 108 [12]		35 ± 0.4	180 ± 9	950 [11]
Indentation fracture toughness (MPa $\sqrt{m}$)	2.73 ± 0.63 [13]	5.72 ± 0.86 [13]	3.88 ± 0.53 [13]	35–55 [14]	100–107 [14]	122 [15]
Poison's ratio	0.31	0.30	0.33	0.36	0.33	0.31
Coefficient of thermal expansion (ppm/K)	16.3 [16]	19.0 [16]	13.7 [16]	22.5 [9]	16.4 [16]	12.5 [9]
Electrical resistivity (μΩ cm)	17.5	8.8	28.5	11.5	1.71	6.99
Thermal conductivity (W/cm-K)	0.341	0.704	0.196	0.668	4	0.91
Melting point (°C)	415	676	795	232	1085	1455
Volume shrinkage (%)	5.0 % $6Cu + 5Sn = Cu_6Sn_5$ [17]	4.3 % $Cu_6Sn_5 + 9Cu = 5Cu_3Sn$ [17]	11.3 % $3Ni + 4Sn = Ni_3Sn_4$ [17]			
Crystal structure	Hexagonal (η) above 186 °C Monoclinic (η') below 186 °C	Orthorhombic (ε)	Monoclinic	Body-centered tetragonal	Face-centered cubic	Face-centered cubic

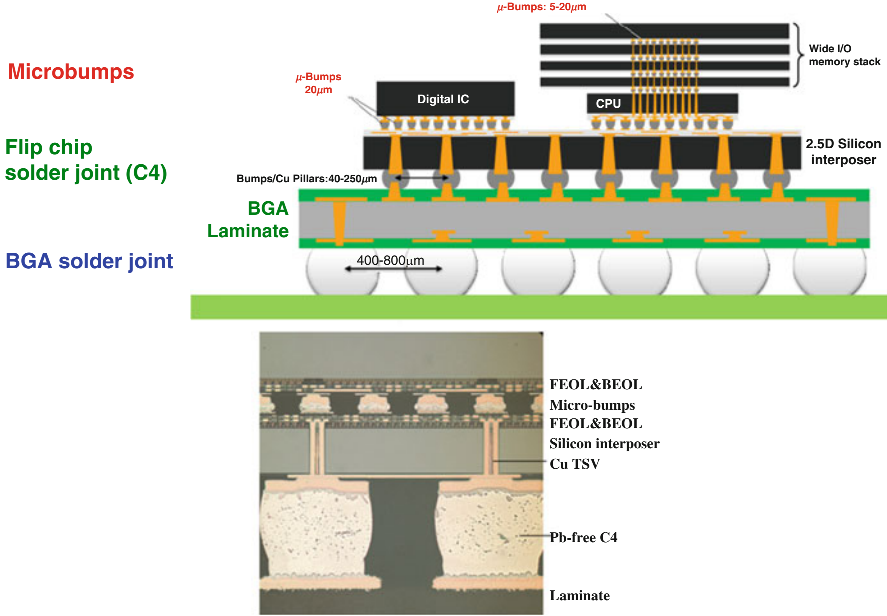
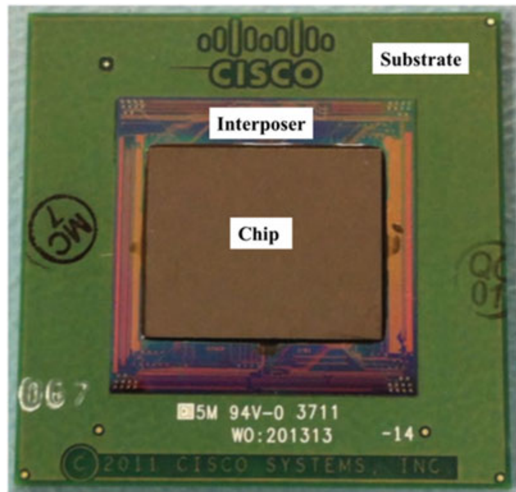


Fig. 14.1 Schematic diagram and optical image of a typical Chip-on-Wafer-on-Substrate (CoWoS) architecture using three-dimensional chip stacking with 2.5D silicon interposer ([5])

Fig. 14.2 A top view of 3D IC assembly [6]



interaction by using a thin layer of Si interposer, as shown in Fig. 14.1. The interposer is between the vertically stacked Si chips and the packaging substrate to greatly relieve thermomechanical stress in the Si chips. One of the prototypes of vertically stacked chips with Si interposer is shown in Fig. 14.2.

In a conventional flip chip solder joint, or Controlled-Collapse-Chip-Connection (C4) joint, the IC chips with pre-deposited solders are flipped over so that top surface of chip faces down and bonds with landing metal pads with a complex under bump metallurgy (UBM). One of the major constituents of UBM is a thin layer of Cu pad. In order to prevent the rapid Cu consumption by solder which may result in pancake-type electromigration (EM) void formation, typically a thin layer of Ni is deposited on top of Cu to change the metallurgy of UBM and reduce the Cu consumption rate. Hence only a small volume fraction of solder joint was converted to IMCs.

For the microbumps used in 3D IC technology, Thermal Compression Bonding (TCB) is used to meet the requirement for fine-pitch interconnect and high bonding yield, especially in wafer-level packaging [4]. Copper pillar, instead of Cu thin-film UBM, is used to control the fine gap between chip-to-chip stacking. This results in the utilization of low-volume and fine-cap Pb-free solder which is electroplated on Cu pillar before TCB process to form microbumps. For a small size microbump, its thickness is below 10 μm. Considering the large difference in terms of thickness and Young's modulus between Cu pillar (120 GPa) and Sn cap (50 GPa) of a microbump, see Table 14.2, Cu pillar may induce large thermomechanical stress at joint interfaces compared to the conventional flip chip solder joints. Hence, microbump is expected to have brittle fracture. In addition, the trend toward the miniaturization of electronic consumer products leads to the shrinkage of solder joint size, resulting in not only a high volume fraction but also a limited number of IMC grains within the microbump. Under a similar C-4 joint processing condition, i.e., about 240 °C and 1 min reflow time, a Sn-based microbump can be completely transformed into Cu-Sn or Ni-Sn IMC. Hence, microbump is no longer a solder joint. Instead, it is based on intermetallic compounds. For an IMC-based microbump, its mechanical reliabilities are far from understood because of the lack of field data.

For a chip about the size of our finger nail, ~1 cm^2, there are about a million of microbumps per chip, or 10^6 joints/cm^2, if we consider microbump diameter to be 5–10 μm. Therefore, how to study an individual microbump is quite challenging. In addition, for microbump diameter smaller than 5 μm, there is a strong likelihood that microbump properties are controlled by a few grains or even a single grain. For tens of thousands of IMC-based microbump interconnect, the microstructural anisotropy and texture effect may become even more important [1]. This in turn can influence microbump mechanical reliabilities such as early failure. Microstructure, in terms of grain size, morphology, texture, phase transformation, and phase stability, determines ultimately the properties, especially mechanical reliabilities of microbump. Therefore, an in-depth understanding of the properties and scalability of microbump for mass production requires a focused review.

14.3 Quality and Reliability of Microbumps

We present four types of microbumps that are widely used in the industry for 3D IC technology, in which the under-bump metallization (UBM) is in different metallurgical combinations. For each type of microbump, there are case studies and discussion of quality and reliability concerns. The aim is to understand the impact of different UBM or surface finishes on the mechanical reliability of microbump.

Microbump materials are typically Sn-based Pb-free solder, e.g., SnAgCu, SnAg, SnCu or SnAgCu-*X* where *X* represents the fourth elements. We simplified the discussion here by using "Sn" to represent solder and focus on the impact of UBM. No doubt the solder composition also plays a critical role to quality and reliability. With a fixed UBM layer, modulating solder composition and bonding temperature profile can significantly impact performance.

14.3.1 Type 1: Cu/Sn/Cu

14.3.1.1 Microstructure of Cu-Sn IMCs-Based Microbump

Cu/Sn/Cu is one of most widely used microbumps for chip-to-chip connection. When the joint height is less than 10 μm, under typical assembly condition at 240 °C for 1 min bonding time, all the microbumps can be converted completely into Cu-Sn IMCs. The kinetically favorable Cu_6Sn_5 is preferentially nucleated at the Cu/solder interface and continues to grow at assembly condition. Under further reflow or thermal annealing, Cu_6Sn_5 can be gradually transformed into the thermodynamically stable phase of Cu_3Sn. A typical microstructural evolution of Cu-Sn microbump in both as-received and reflowed condition is shown in Fig. 14.3.

14.3.1.2 Microstructural Characteristics of Cu_6Sn_5 in Microbump

Li et al. prepared Cu/Sn/Cu microbump samples by controlled compression of two polished copper surfaces sandwiching a tin foil in the middle with thickness 25 μm under different reflow temperature [19]. They monitored Cu_6Sn_5 microstructural evolution during continuous liquid state reaction where Sn is in the molten state. Shown in Fig. 14.4, Cu_6Sn_5 was formed at the Cu/Sn interface in scallop-type morphology. Growth and ripening of Cu_6Sn_5 on two opposing interfaces happened concurrently. Once the two opposing Cu_6Sn_5 grains came into contact with each other, the parallel grain boundaries surprisingly disappeared. No grain boundaries in lateral direction could be identified and only vertical columnar grain boundaries could be observed, Fig. 14.4c. The similar findings were also reported by Chuang [17] and Wang [20], Figs. 14.5 and 14.6. The columnar Cu_6Sn_5 was further consumed by Cu into more stable phase of Cu_3Sn in much finer columnar grain

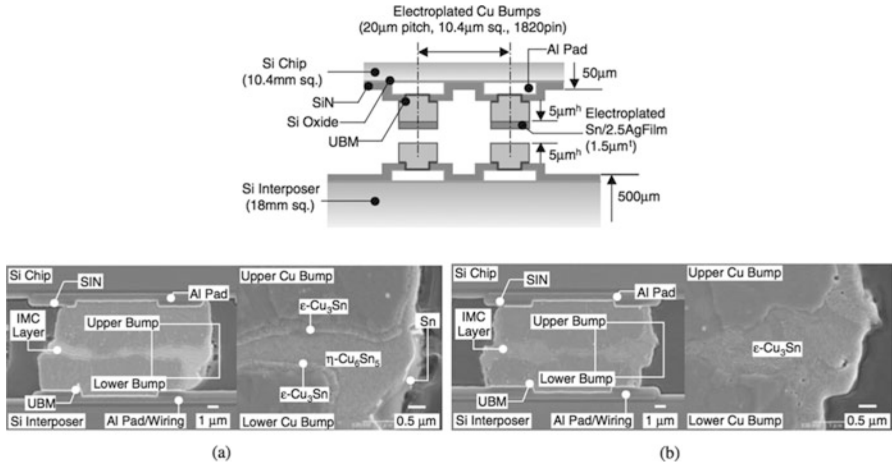


Fig. 14.3 Schematic diagram of Cu/Sn/Cu microbump-enabled chip-to-chip interconnection; SEM images of microstructural evolution of Cu-Sn microbump cross section (**a**) 240 °C, (**b**) 350 °C for 1-min bonding time [18]

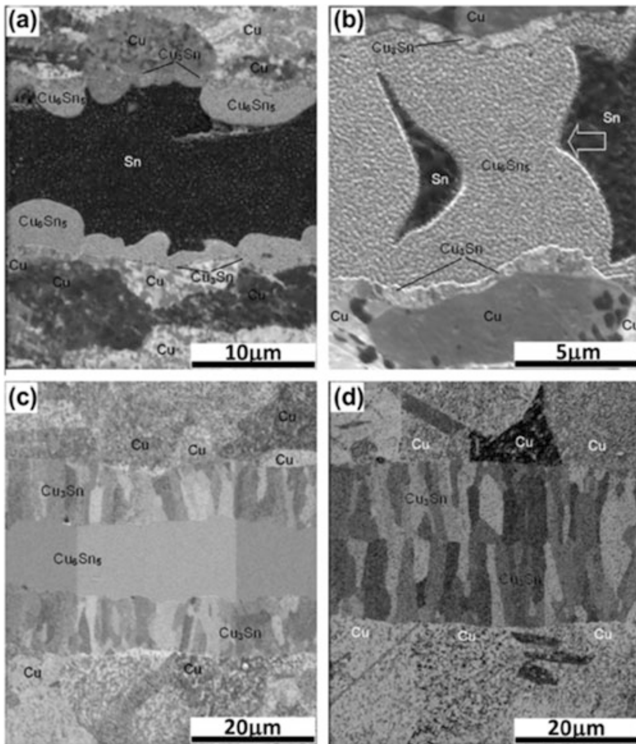


Fig. 14.4 FIB ion beam image of Cu/Sn/Cu micro-joint reflowed at: (**a**) 260 °C for 5 min; (**b**) 300 °C for 10 min; (**c**) 300 °C for 480 min; (**d**) 340 °C for 480 min [19]

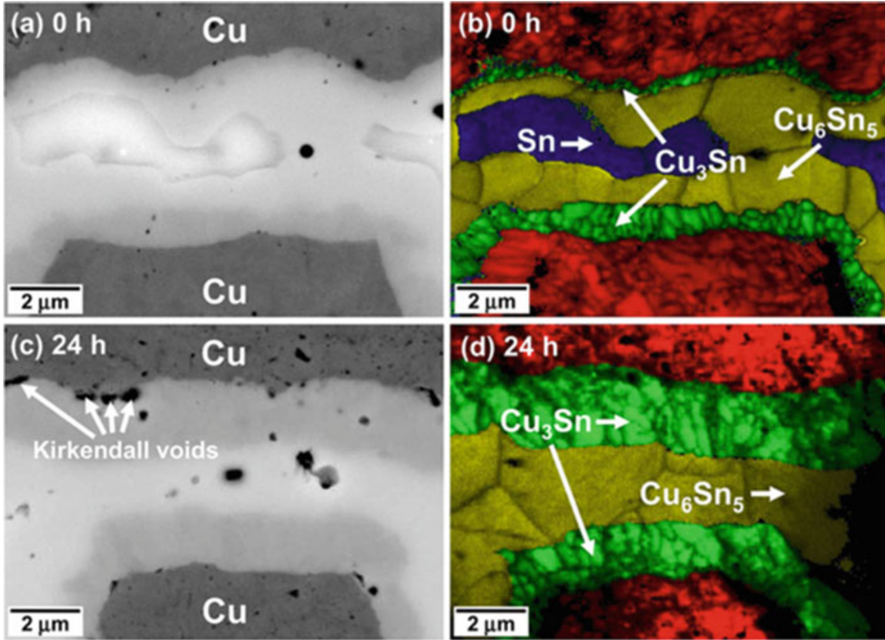


Fig. 14.5 BSE and EBSD phase mappings of Cu/Sn-Ag/Cu microbump in which IMCs microstructural evolution during isothermal annealing at 180 °C were characterized: (**a**, **b**) as-received, (**c**, **d**) 24-h annealing [20]

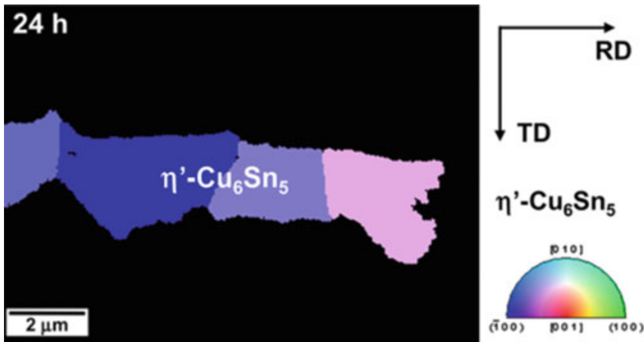


Fig. 14.6 Cu_6Sn_5-based microbump was indexed by low temperature η'-Cu_6Sn_5 phase and no lateral grain boundaries was identified in columnar-type Cu_6Sn_5-based microbumps [20]

structure. When the residual Cu_6Sn_5 was completely consumed, unlike Cu_6Sn_5 grains, two layers of impinging Cu_3Sn grains were left with both lateral and vertical grain boundaries. The underlying reasons that why opposing Cu_6Sn_5 grains tends to coarsen into a single grain with the disappearance of the lateral grain boundaries were not clearly understood. This remains a very puzzling question on columnar

Cu_6Sn_5 formation. However, the absence of lateral grain boundaries is certainly a benefit for microbump mechanical reliabilities because the horizontal grain boundaries across a microbump can degrade the microbump fracture strength by inducing crack formation and propagation.

14.3.1.3 Kirkendall Void and Porous Void Formation in Cu_3Sn

Cu_3Sn is known as the phase containing microvoid, i.e., Kirkendall void [21]. Kirkendall void is typically observed in Cu/Sn solder joints during a high temperature storage test or current stressing where Cu overconsumption leads to microvoid formation in the Cu_3Sn layer [21, 22]. Kirkendall void formation is due to unbalancing interdiffusion of Cu and Sn atomic flux where Cu diffuses much faster than Sn in the reverse direction [21, 23]. However, Kirkendall void can be effectively reduced by adding Co or Ni into Pb-free solder [24]. Besides, by controlling electroplating bath, or to have nanotwinned Cu as UBM can significantly reduce microvoid nucleation [25–28]. Kirkendall void can be a serious reliability issue. If it is not under control, Kirkendall voids tend to coarsen along the Cu_3Sn/Cu interface and induce micro-crack formation, as shown in Fig. 14.7

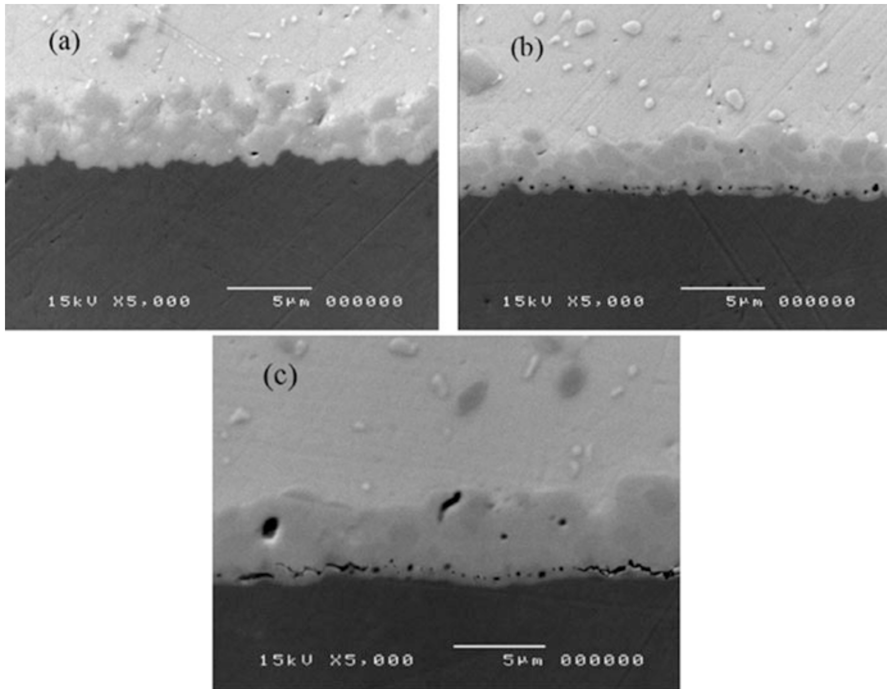


Fig. 14.7 SAC solder/copper pad cross-sectional interface after Ar^+ sputtering etch (**a**) as reflowed; (**b**) 500 cycles of thermal cycling that Kirkendall void formed and occupied about 10 % of interface; (**c**) 1000 cycles of thermal cycling at which Kirkendall void growth induced microcrack formation could be observed at the interface [28]

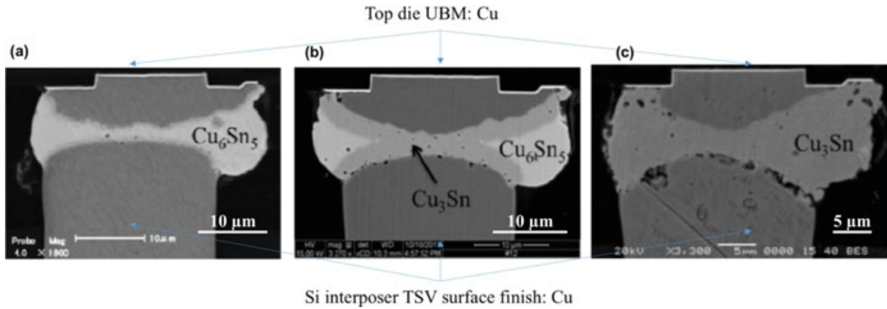


Fig. 14.8 Backscattered cross-sectional SEM images of Cu (top-die)-SnCu-Cu (TSV) microbump at different stages of thermal aging at 170 °C (**a**) as-received; (**b**) 83 h; (**c**) 1000 h [29]

[28]. No doubt, Kirkendall void is undesirable and deleterious to both mechanical and electrical performance of microbumps.

Wang et al. performed thermal annealing experiments on Cu-TSV/SnCu solder/Cu microbump at 170 °C. They found that Kirkendall void formation can induce crack formation at the interface between SnCu solder and Cu-TSV in the Si interposer after 1000-h annealing [29]. The Kirkendall void preferentially nucleated and grew on the TSV side of interface between Cu-TSV/microbump. This is attributed to different electrochemistry used in forming Cu UBM on the chip side and Cu-TSV in the interposer. In the latter, the Cu was filled in the via by electroplating where organic impurities such as S might be trapped inside and segregated to the end of Cu-TSV so that Kirkendall voids were preferentially nucleated at the Cu/Cu_3Sn interface because of heterogeneous nucleation. This was suggested to be the reason why Kirkendall void formation was only observed on the Cu-TSV interface instead of on the chip side (Fig. 14.8) [29].

Besides Kirkendall void formation, Chen et al. recently reported that there is another type of porous void formation which can happen inside $Cu/Cu_3Sn/Cu$ microbump under aggressive thermal annealing or current stressing [30–32]. In porous microbump, Cu_3Sn can exist in two types of morphology: nonporous Cu_3Sn layer with Kirkendall void formation at the Cu/Cu_3Sn interface, and porous Cu_3Sn as middle layer sandwiched between its nonporous counterparts, Fig. 14.9. Wang et al. found that by conducting aggressive high temperature storage test at 210 °C for samples of Cu-wire/Sn/Cu-wire micro-joint in which Cu is of infinite amount. The mechanical strength of Cu wire degraded dramatically from 162 MPa from as-received state to 60 MPa after annealed for 1 week, Fig. 14.10.

14.3.1.4 Anisotropic Effect in Microbump

Suh et al. found that a very strong orientation relationship exists between Cu_6Sn_5 and Cu from the reaction between a pure (100) oriented single crystal Cu and eutectic SnPb. There are six types of preferred crystallographic orientation

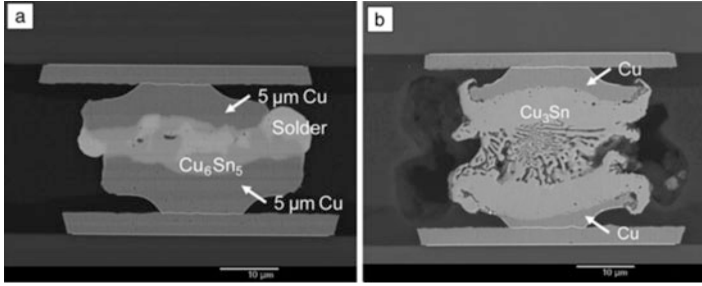


Fig. 14.9 (**a**) As-fabricated Cu/solder/Cu microbump with 8-μm-thick SnAg solder. (**b**) Porous Cu_3Sn is formed in the middle of microbump between two of nonporous Cu_3Sn layers after reflow at 260 °C for 12 h [32]

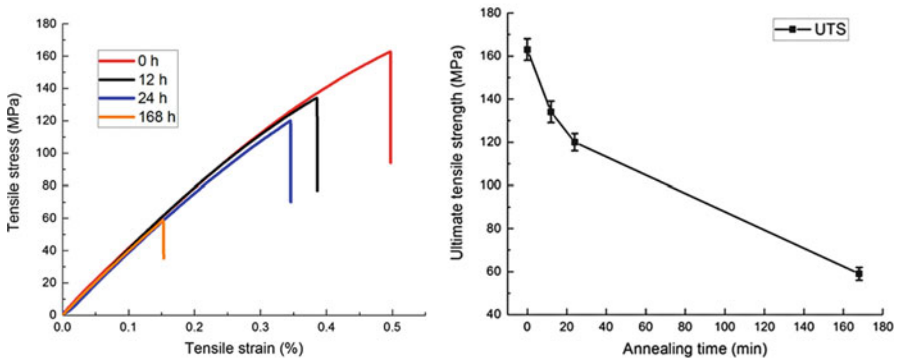


Fig. 14.10 (**a**) Tensile test curve of Cu/Sn(10-μm)/Cu micro-joint under aggressive high temperature storage at 210 °C up to 168 h. The adhesion strength degraded dramatically from 162 to 60 MPa [33]

relationship identified by Synchrotron X-ray microdiffraction [34, 35]. Figure 14.11a is an orientation mapping representing the angle between [101] direction of Cu and $[\bar{1}01]$ direction of Cu_6Sn_5. Figure 14.11b is a histogram orientation distribution corresponding to Fig. 14.11a. It indicates that most of the IMC grains have very strong orientation relationship between the [101] direction of Cu and $[\bar{1}01]$ direction of Cu_6Sn_5. A similar crystallographic orientation relationship also exists in the same kind of pure Cu and pure Sn diffusion couple, see Fig. 14.11c, d. The reason of preferred orientation relationship between [101] direction of Cu and $[\bar{1}01]$ of Cu_6Sn_5 is attributed to low misfit energy. The misfit between Cu and Cu_6Sn_5 is 0.24 %. The misfit direction lies on (001) plane of Cu.

$$(010)_{Cu_6Sn_5}//(001)_{Cu} \cdot \cdot [\bar{1}01]_{Cu_6Sn_5}//[101]_{Cu}$$

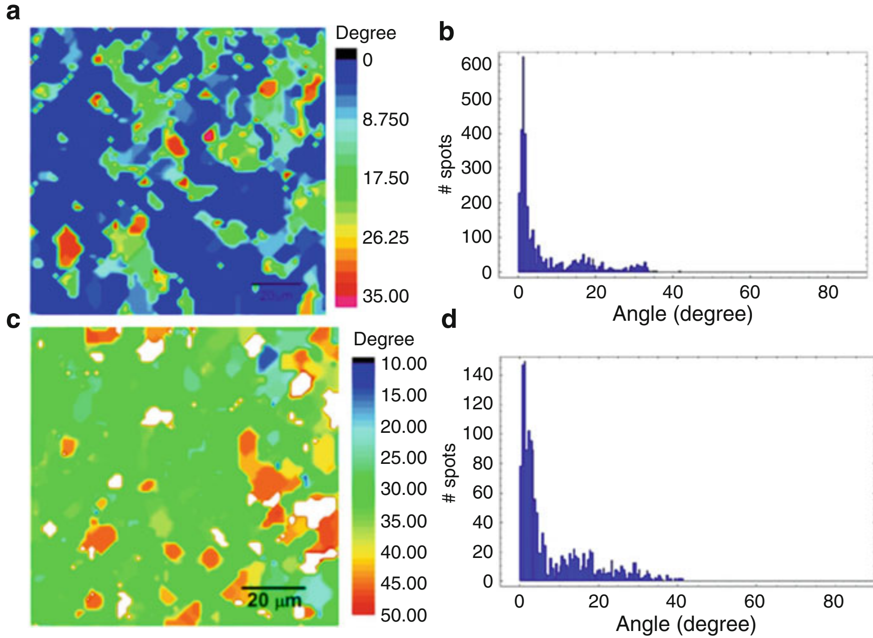


Fig. 14.11 Orientation mapping and histogram of (**a**), (**b**) Cu/SnPb and (**c**), (**d**) Cu/Sn sample with 4-min reflow time at 250 °C [35]

$$(343)_{Cu_6Sn_5}//(001)_{Cu} \cdot\cdot [\overline{1}01]_{Cu_6Sn_5}//[101]_{Cu}$$

$$(\overline{3}4\overline{3})_{Cu_6Sn_5}//(001)_{Cu} \cdot\cdot [\overline{1}01]_{Cu_6Sn_5}//[101]_{Cu}$$

$$(101)_{Cu_6Sn_5}//(001)_{Cu} \cdot\cdot [\overline{1}01]_{Cu_6Sn_5}//[101]_{Cu}$$

$$(141)_{Cu_6Sn_5}//(001)_{Cu} \cdot\cdot [\overline{1}01]_{Cu_6Sn_5}//[101]_{Cu}$$

$$(\overline{1}4\overline{1})_{Cu_6Sn_5}//(001)_{Cu} \cdot\cdot [\overline{1}01]_{Cu_6Sn_5}//[101]_{Cu}$$

An EBSD study indicates that the rooftop or prism-type Cu_6Sn_5 is elongated along two perpendicular $\langle 110 \rangle$ directions on the (001) plane of Cu, which also corresponds to low misfit directions of the Cu_6Sn_5. This study implies that if we can control the orientation of the UBM, i.e., (001) oriented Cu, the crystal orientation of Cu_6Sn_5 can also be controlled with preferred texture, resulting in unique grain morphology, i.e., rooftop, compared to randomly oriented scallop-type Cu_6Sn_5 grains. This orientation relationship might be potentially useful in controlling the texture of columnar grains-based microbumps, which is essentially dependent on the texture of Cu_6Sn_5 grains (Fig. 14.12).

This unique rooftop morphology was further studied by several groups [36, 37]. It was reported by Tian et al. that rooftop Cu_6Sn_5 morphology can be formed at elevated temperature, i.e., 300 °C while scallop-type Cu_6Sn_5 exists

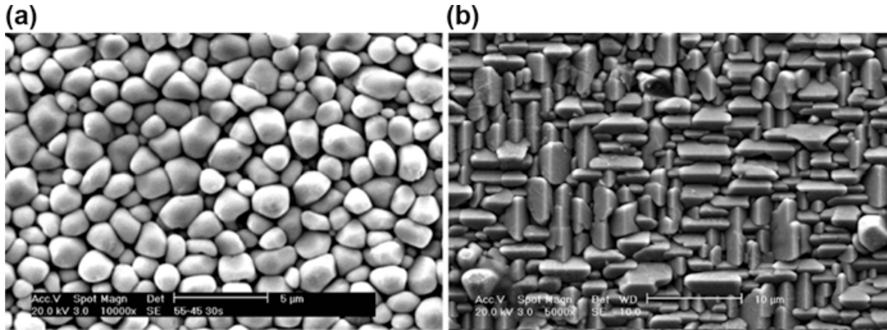


Fig. 14.12 Top view of exposed Cu_6Sn_5 grains after deep etching of eutectic SnPb solder joint reflowed at 200 °C for 30 s: (**a**) scallop-type Cu_6Sn_5 grains on polycrystalline Cu substrate; (**b**) rooftop-type Cu_6Sn_5 grains on (001) Cu [34]

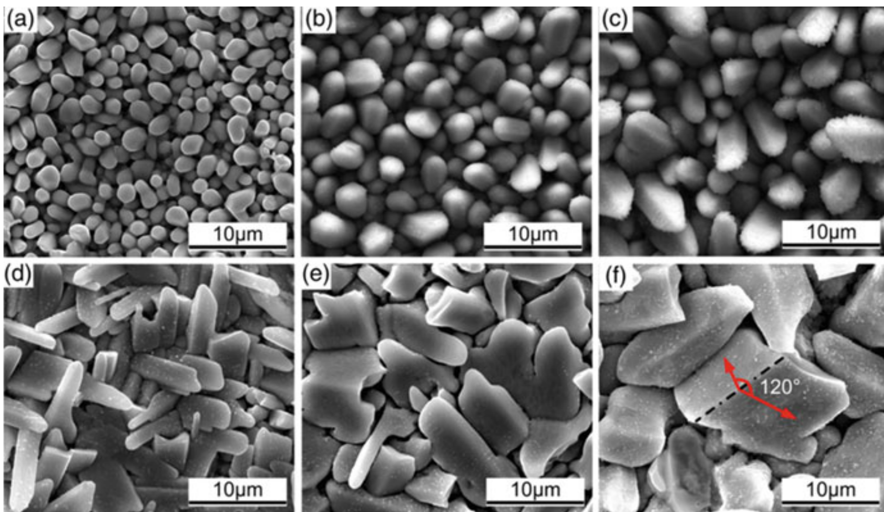


Fig. 14.13 Different interfacial morphology of Cu_6Sn_5 grains on polycrystalline Cu under different conditions: interfacial scallop-type morphology at 250 °C for (**a**) 10 s; (**b**) 60 s; (**c**) 300 s; and rooftop morphology at 300 °C for (**d**) 10 s; (**e**) 60 s; (**f**) 300 s [36]

during reflow at 250 °C. Both scallop-type and rooftop-type Cu_6Sn_5 have preferred [0001] direction parallel to the Cu surface normal (Fig. 14.13) [36].

In addition, the Cu_6Sn_5 grains of strong texture can also be obtained at typical reflow temperature, i.e., 240 °C for extended reflow time. Instead of using single crystal Cu, highly textured Cu_6Sn_5 grains can also form on polycrystalline Cu by reflowing at 240 °C at which η - Cu_6Sn_5 forms in [0001] direction which is aligned to the normal of polycrystalline Cu substrate. In order to induce strong preferred texture, a long-time reflow was conducted. As shown in Fig. 14.14, a clear texture

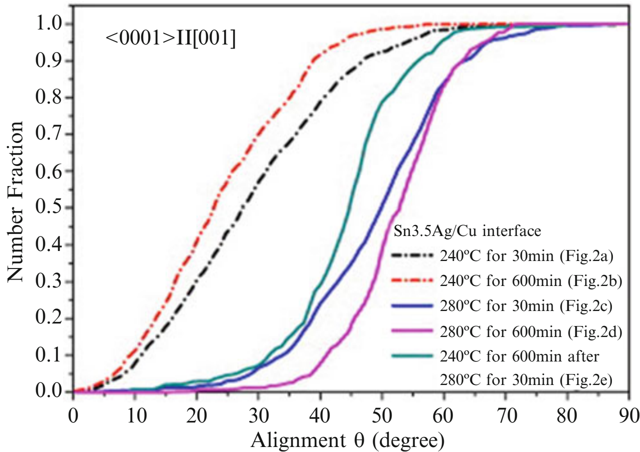


Fig. 14.14 Misorientation chart of alignment angle statistics of ⟨0001⟩-oriented Cu_6Sn_5 with polycrystalline Cu substrate toward [001] direction [38]

can be observed at 240 °C at which strongest orientation dependence of growth of Cu_6Sn_5 along the normal of the Cu substrate can be obtained, when it was reflowed at 240 °C for 600 min. At this condition, about 70 % of Cu_6Sn_5 grains have misorientation angle smaller than 30 °. Unlike the Cu_6Sn_5 texture formed on single crystal (100) Cu, the texture from polycrystalline Cu is a result of interfacial grain ripening.

The textured Cu_6Sn_5 was further evaluated from mechanical properties perspective. As shown in Fig. 14.15, Sn3.5Ag was used for reflow soldering for two conditions: 240 °C, 1 min, and 280 °C, 1 min for common polycrystalline Cu substrates. For comparison, a textured Cu_6Sn_5 substrate was used for reflow soldering at 280 °C for 1 min. Ball shear tests were conducted to evaluate IMC strength with preferred orientation and the average value was taken by 30 measurements and results were plotted in Fig. 14.15d. It indicates that the [0001]-oriented Cu_6Sn_5 formed at 280 °C for 1 min has highest joint shear strength [38]. This unique oriented growth of Cu_6Sn_5 is worth to be further studied and applied in a controlled growth of IMC-based microbump.

14.3.2 Type 2: Ni/Sn/Ni

For typical Ni/Sn/Ni microbump, Ni is used as diffusion barrier to retard IMC formation especially under reflow or thermal compression bonding. Hence, it could leave behind a sufficient amount of unreacted solder as mechanical buffer layer to retain the ductility of microbump. As shown in Fig. 14.16, for as-received Ni/Sn/Ni microbump, after bonding, Ni-Sn microbump was more or less transformed into Ni_3Sn_4 IMC at the center but with the remaining solder squeezed out on the

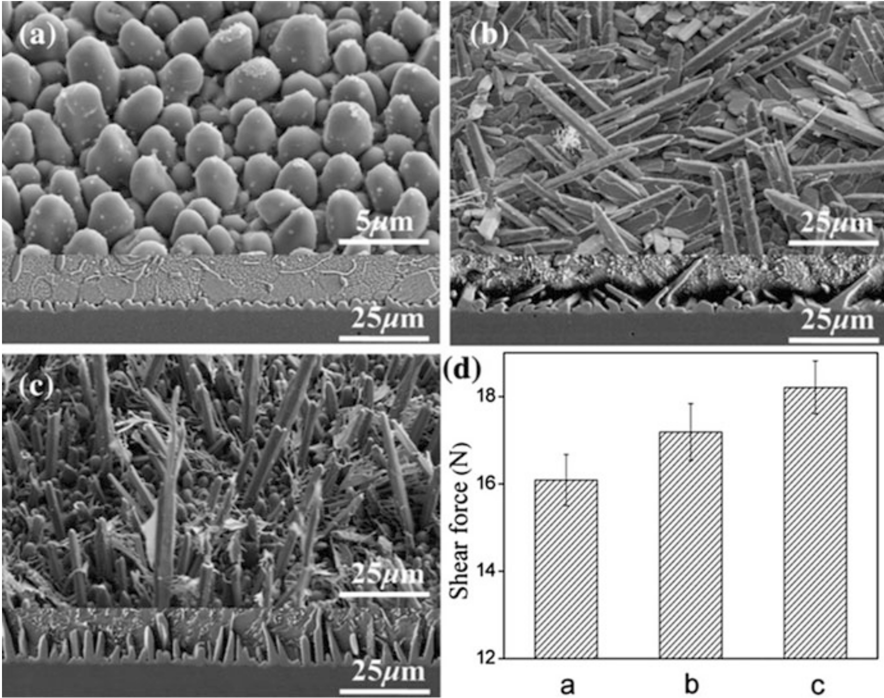


Fig. 14.15 Morphologies of Cu_6Sn_5 formed on Cu substrate at (**a**) 240 °C and (**b**) randomly-oriented Cu_6Sn_5 at 280 °C for 1 min, and (**c**) [0001]-oriented Cu_6Sn_5 at 280 °C for 1 min. The joints were cooled in air. (**d**) Shear strength of solder joint of (**a**), (**b**), and (**c**) condition [38]

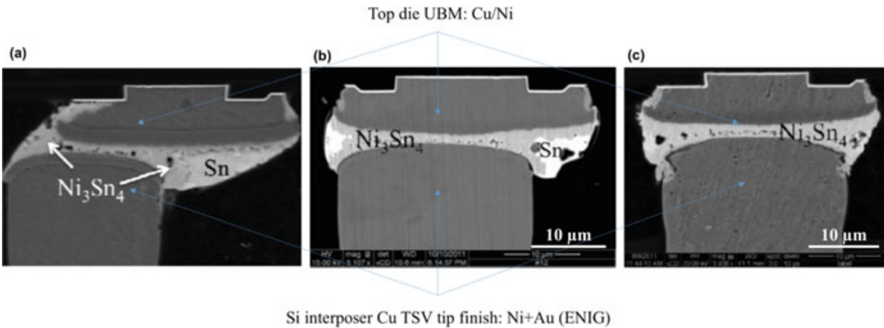


Fig. 14.16 BS-SEM images of cross sections of the Ni-Sn-Ni microbump under isothermal annealing at 170 °C (**a**) as-received; (**b**) 83 h; (**c**) 1000 h [29]

periphery of the microbump. The top and bottom layers of Ni_3Sn_4 were almost impinged into each other. Upon further thermal annealing, eventually the Ni/Sn/Ni microbump was fully converted into Ni_3Sn_4 IMC, in which an array of microvoids were trapped along the impinged Ni_3Sn_4 grain boundaries, which is susceptible to

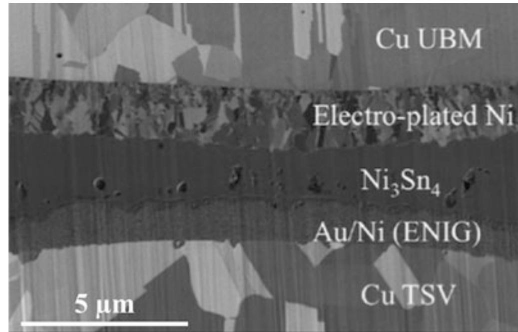


Fig. 14.17 FIB cross-sectional image of Ni-Sn-Ni microbump/TSV joint with microvoids trapped inside Ni_3Sn_4 IMC [29]

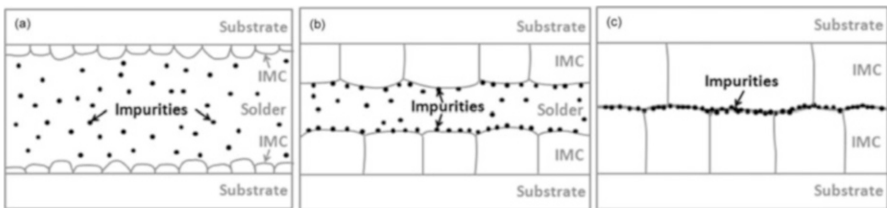
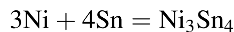


Fig. 14.18 Schematic diagrams showing the impurities concentration increases while residual solder is gradually transformed into IMC (**a**) As-reflowed condition; (**b**) two-third of solder consumed; (**c**) all of the solder completely converted into IMC [17]

grain boundaries embrittlement due to trapped impurities [29]. From the point of view of mechanical reliability, inter-grain fracture is expected to occur along this grain boundary which contains a large amount of microvoids and impurities. The detailed impurities migration to Ni_3Sn_4 grain boundaries was also given by Chuang et al. [39] (Figs. 14.17 and 14.18).

Besides impurities trapping, another type of mechanically weak link can be attributed to Ni/Sn chemical reaction in Ni-Sn-Ni microbump. The interfacial reaction of Ni and Sn is given by the following chemical reaction:



$$3Ni + 4Sn = Ni_3Sn_4$$

The theoretical net volume shrinkage based on atomic volume calculation is 11.3 %, see Table 14.2. After all of the remaining solder is completely transformed into Ni_3Sn_4, due to its brittle nature, the volume shrinkage can no longer be accommodated by solder thickness reduction. Instead, it results in void formation to dissipate the volume shrinkage. As shown in Fig. 14.19, void formation in Ni_3Sn_4-based microbump annealed at 180 °C for 240 h was identified. The cross section was polished by ion beam milling to avoid possible mechanical polishing induced micro-crack formation or polishing powder smearing effect. Figure 14.19 clearly demonstrates that the void was originated from Sn pockets during Ni/Sn IMC formation. As also indicated by Chen's Ph.D. thesis [40], for Ni-Sn-Ni

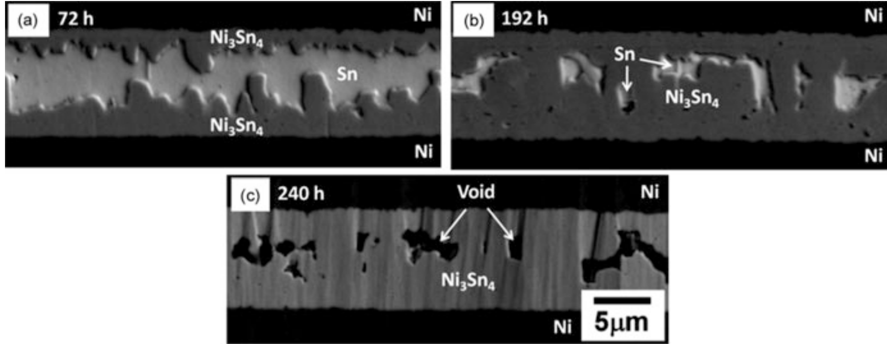


Fig. 14.19 Cross-sectional SEM images of Ni_3Sn_4 microstructural evolution in Ni/Sn (10 μm)/Ni micro-joint under isothermal annealing at 180 °C for (**a**) 72 h, (**b**) 192 h, and (**c**) 240 h [17]

microbump, Sn is faster diffusion species compared to Ni. The IMC growth during thermal annealing is also a flux-driven ripening process, which means larger grains will grow at the expense of smaller grains. The ripening effect tends to result in uneven interface due to opposing IMC impingement and hence result in forming Sn pockets in thermal annealing. Since Sn is faster diffusion species, the asymmetrical atomic flux results in vacancy accumulate inside Sn pocket. When the remaining Sn is completely consumed, the supersaturation of vacancy leads to void formation and therefore trapped inside the original position of Sn pocket. No doubt, the void trapped inside Ni_3Sn_4 microbump can adversely degrade IMC mechanical reliability. In terms of UBM used for Ni_3Sn_4 microbump, Ni ($E = 186$ GPa) itself is less mechanically compliant than Cu ($E = 120$ GPa), Table 14.1. It seems that Ni_3Sn_4 microbump, based on the above discussion, would have a more serious mechanical reliability concerns than Cu-based microbumps: the trapped impurities induced grain boundaries embrittlement and volume shrinkage resulted void or micro-crack formation. Traditionally, Ni was introduced to reduce IMC formation in order to address mechanical reliability concerns. Nevertheless, for the application of fine-pitch interconnects in 3D IC technology which requires joint thickness down to 5 μm, joint with full IMC formation is inevitable so that the utilization of Ni as UBM would not necessarily mitigate the full IMC formation and might actually result in serious mechanical reliability issues.

14.3.3 Type 3: Cu/Sn/Ni

The third type of metallurgical configuration of microbump is Cu/Sn/Ni. As shown in Fig. 14.20, Cu/Sn/Ni type of microbump was prepared to study IMC microstructural evolution and reliability [29]. The UBM on the top Si chip was composed of Cu stud while the TSV in the interposer was made of Cu coated with electroless-plated Ni as surface finish. Cross-sectional EDX analysis indicated that initial

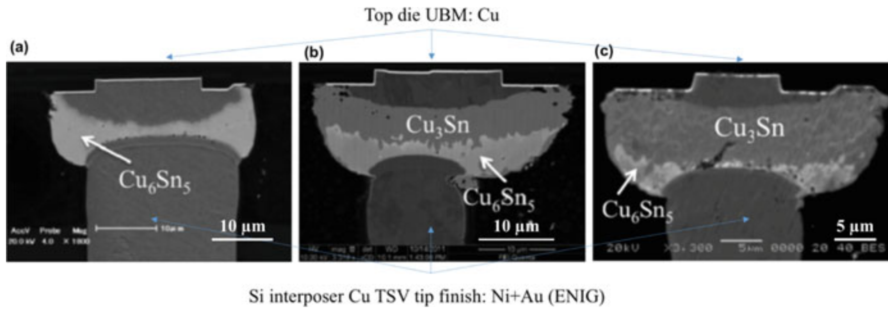


Fig. 14.20 Backscattered-SEM image of cross section of the Cu (top-die)/microbump/Ni (surface finish of Cu-TSV) isothermally annealed at 170 °C, (**a**) as-received; (**b**) 267 h; (**c**) 1000 h [29]

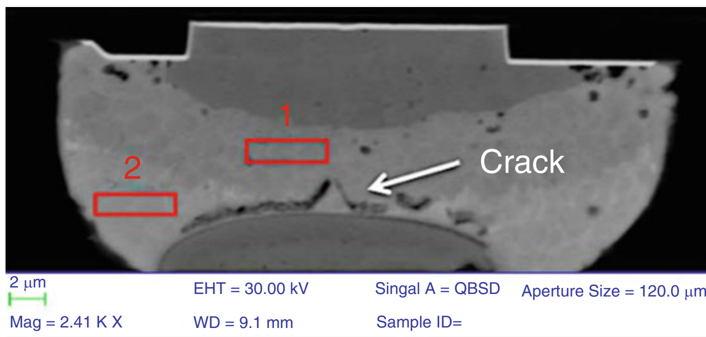


Fig. 14.21 A crack was identified near the interface between Cu_3Sn and Ni_3Sn_4 for Cu/Sn/Ni-type microbump [29]

thermal compression bonding has consumed all of the solder into IMC in the stoichiometric form of $(Cu,Ni)_6Sn_5$ with a limited amount of Ni dissolution. No $(Ni,Cu)_3Sn_4$ IMC was identified. The reason of preferential formation of Cu_6Sn_5 instead of Ni_3Sn_4 is due to the large volume difference between a limited amount of solder compared to the unlimited supply of Cu stud, which resulted in preferential formation of Cu_6Sn_5 instead of Ni_3Sn_4. Upon continuous thermal annealing, $(Cu, Ni)_3Sn_4$ layer grew thicker at the expense of Cu_6Sn_5. Since Ni was used as surface finish for diffusion barrier at the Cu-TSV side, the growth of Cu_3Sn was significantly restarted. This asymmetrical design of Cu-Sn-Ni microbump ultimately resulted in an asymmetrical IMC formation and excessive Cu UBM consumption at the top side of the stacked chips.

Crack formation was observed in Cu/Sn/Ni-type microbump, as shown in Fig. 14.21. The reason was attributed to thermomechanical stress, resulting from CTE mismatch of dissimilar IMC formation, for which CTE of Cu_3Sn and Cu_6Sn5, are respectively, 19.0 and 13.7 ppm/K, see Table 14.1. Besides, there might be another two reasons for the crack formation for Cu/Sn/Ni-type microbump. Once IMCs are formed inside the Cu/Sn/Ni microbump, Cu_6Sn_5 on the top die side was

further transformed into Cu_3Sn, whereas on the bottom TSV side Sn diffusion is much faster than Ni diffusion. The unbalancing Sn and Ni diffusion flux results in vacancy supersaturation and void formation along the Ni surface finish/microbump interface, which ultimately leads to crack formation. The other possible reason is due to volume shrinkage difference between Cu-Sn and Ni-Sn IMC. As indicated in Table 14.1, volume shrinkage of Cu_6Sn_5, Cu_3Sn, and Ni_3Sn_4 are, respectively, 5 %, 4.3 %, and 11.3 %. The volume shrinkage could not be accommodated by IMCs deformation due its brittle nature. Hence, the mismatch of volume shrinkage might also result in crack formation.

14.3.4 Type 4: Cu/Ni/Sn/Ni/Cu

14.3.4.1 Typical Composition Parameters of Cu/Ni/Sn/Ni/Cu Microbumps

The fourth type of microbump is Cu/Ni/Sn/Ni/Cu. Two symmetrical Ni layers are used as diffusion barriers for two opposing Cu pillars joined by Sn cap during thermal compression bonding. For a typical symmetrical Cu/Ni/Sn/Ni/Cu microbump, its dimensional parameter is shown in Fig. 14.22. Sn2.5Ag was used as Pb-free solder. The microbump pitch is 30 μm. For each side of UBM, the thickness of Cu and Ni is, respectively, 5 and 3.5 μm. The passivation opening for Cu pillar is 12 μm. After assembly at 250 °C, IMC thickness from both sides is about 1 μm and the remaining solder thickness is 2.5 μm.

Under thermal cycling test between −55 and 125 °C, the failure rate of Cu/Ni/Sn2.5Ag/Ni/Cu microbump is 9.5 % for the standard 1000 cycle test. The failure rate only increased dramatically to 47.3 % at the same testing condition when the number of thermal cycles is beyond 1000, which exceeds generally accepted accelerated testing conditions. It indicates that Cu/Ni/Sn/Ni/Cu-type microbumps actually meet the mechanical reliability requirement (Fig. 14.23).

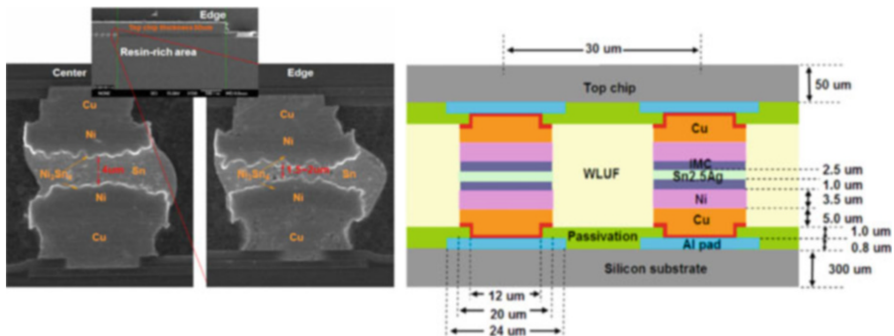


Fig. 14.22 Cross-sectional SEM images and schematic diagram of Cu/Ni/Sn/Ni/Cu microbump [41]

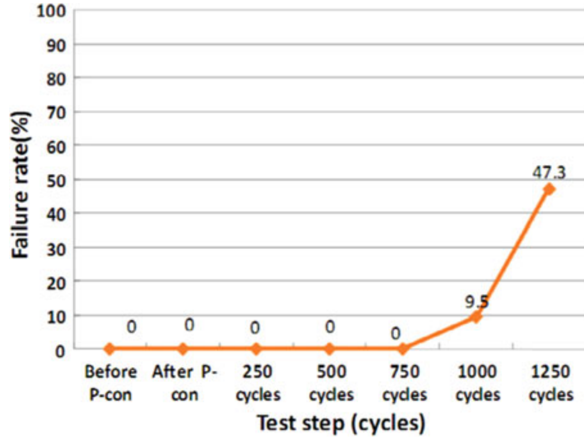


Fig. 14.23 Accumulative failure rate of Cu/Ni/Sn2.5Ag/Ni/Cu microbump during temperature cycling test between −55 and 125 °C [41]

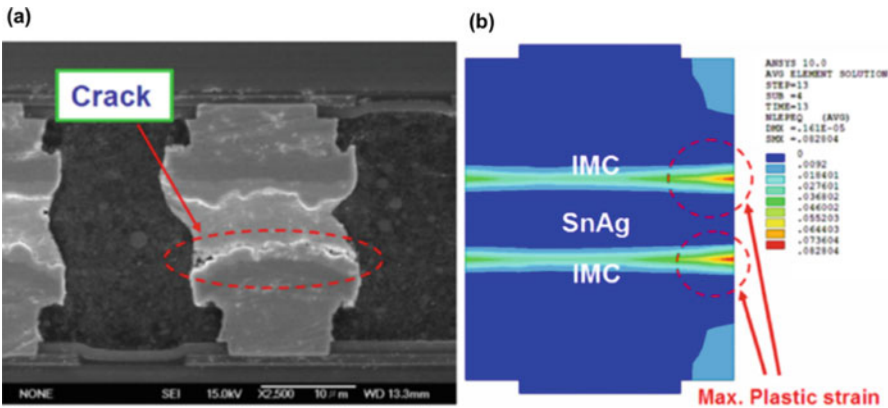


Fig. 14.24 Cross-sectional image of interfacial fracture of Cu/Ni/Sn2.5Ag/Ni/Cu microbump: (**a**) SEM image indicates that a crack propagates along IMC/solder interface; (**b**) finite element simulation result [41]

14.3.4.2 IMC/Solder Interfacial Crack Formation

Finite element simulation was performed on the Cu/Ni/Sn/Ni/Cu-type microbump with the geometry shown in Fig. 14.24b. The simulated result reveals that the maximum plastic strain exists at the corner of the interface between the IMC and remaining solder, which indicates that the micro-crack formation and rapid crack penetration through IMC layer are highly possible [41]. This postulation is indeed in accord with the experimental finding that crack formation was found to propagate along the IMC/solder interface, shown in Fig. 14.24a.

A similar finding of IMC/solder interfacial crack formation for the Cu/Ni/Sn/Ni/Cu-type microbump was also reported by Hsu et al., where crack formation and propagation was identified along the interface between the Ni_3Sn_4 and residual Sn2.5Ag-solder, as shown in Fig. 14.25 [42].

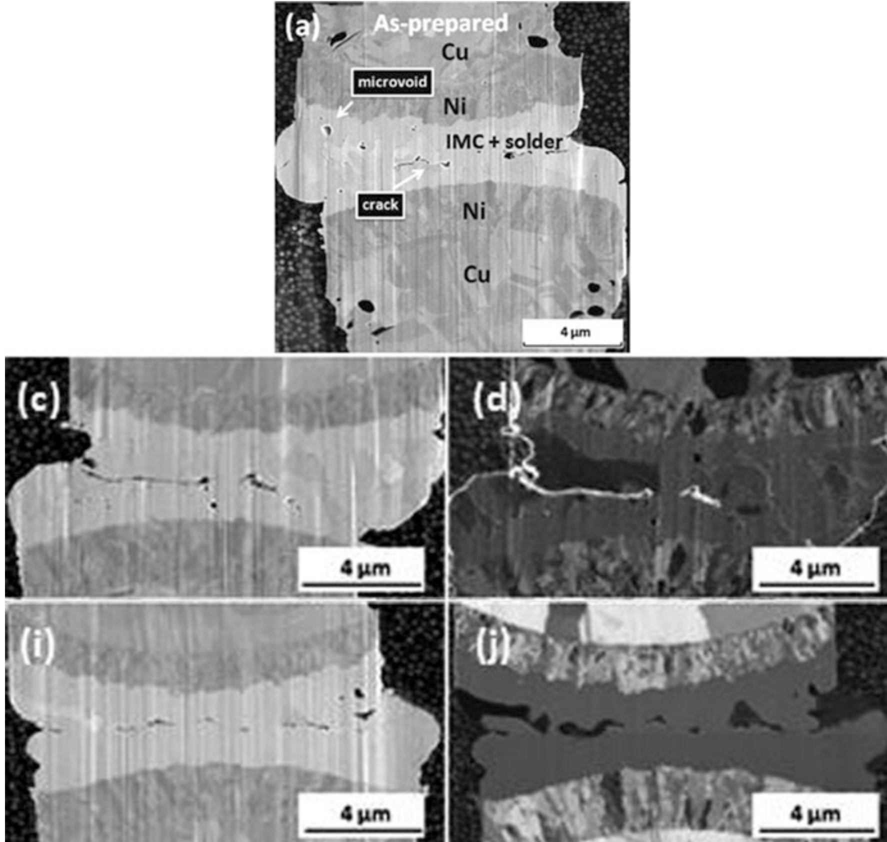


Fig. 14.25 Cu/Ni/Sn-2.5Ag/Ni/Cu microbump samples under solid state annealing at 150 °C for (**a**) as-received; (**c**) e-beam image of sample annealed for 25 h; (**d**) ion beam image of sample annealed for 25 h; (**i**) e-beam image of sample annealed for 250 h; (**j**) ion beam image of sample annealed for 250 h [42]

14.3.4.3 Ni as Effective Diffusion Barrier to Suppress Kirkendall Void Formation

For Cu/Ni/Sn/Ni/Cu microbump in which Ni is used as diffusion barrier, it has limited Kirkendall void formation. Shown in Fig. 14.26, three types of samples with one side of UBM fixed as Ni pad and the other side with different surface finishes of Cu pillar [25]. Sample A is 10-μm Cu with 10-μm SnAg. Sample B is 14-μm Cu with 8-μm SnAg. Sample C is 10-μm Cu with 2-μm Ni as diffusion barrier covered by 0.5-μm Cu with 10-μm SnAg. All of the three types of microbump samples were subjected to high temperature storage test at 150 °C for 500 and 1000 h. It clearly indicates that by depositing a diffusion barrier layer of Ni between Cu pillar and low volume of Sn-based solder, Kirkendall void formation is effectively eliminated. In

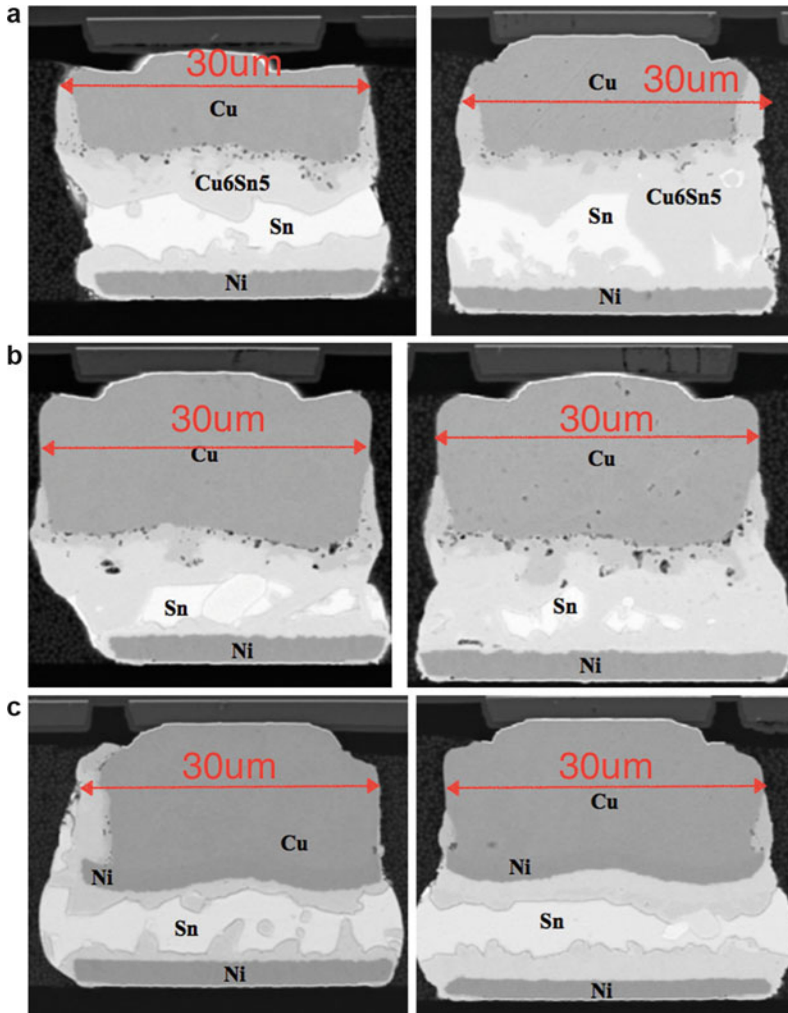


Fig. 14.26 (**a**) Sample A. 10-μm Cu/10-μm SnAg under thermal annealing. (1) 150 °C, 500 h; (2) 150 °C, 1000 h [25]. (**b**) Sample B. 14-μm Cu/8-μm SnAg under thermal annealing. (1) 150 °C, 500 h; (2) 150 °C, 1000 h [25]. (**c**) Sample C. 10-μm Cu/2-μm Ni/0.5-μm Cu/10-μm SnAg (1) 150 °C, 500 h; (2) 150 °C, 1000 h [25]

addition, under the same time of annealing, for microbump with Ni diffusion barrier, there is still about 50 % of microbump volume where the remaining solder was not converted to IMC yet. We expect that such joint has better mechanical properties. Therefore, in order to control Kirkendall void formation, besides adding Ni or Co into solder [24]; electroplating with nanotwin copper [26]; controlling electroplating bath chemistry [27], the addition of Ni between Cu and solder as diffusion barrier seems to be a promising approach. This is because the other three

methods are more difficult in finding a practical and cost-effective route during operation and especially in control of electroplating bath chemistry for mass production.

14.3.5 Concluding Remarks

Among the four types of microbump discussed above, symmetrical Cu/Ni/Sn/Ni/Cu is one of the ideal and widely accepted metallurgical configurations of microbump in the industry for 2.5D/3D IC technology. It has superior mechanical reliability compared to other three metallurgical configurations: Cu/Sn/Cu; Ni/Sn/Ni; and Cu/Sn/Ni, in terms of Kirkendall void, porous void formation in Cu_3Sn, IMC volume contraction induced crack propagation, and asymmetrical impinging IMC interfacial cracking.

14.4 Field Performance Prediction of 3D Packaging

As compared to traditional desktop and laptop, the mobile devices tend to adopt more 3D technologies in order to reduce device size and weight. In the mean time, these devices are exposed to more stringent and dynamic environments due to handheld. However, the fundamentals to predict field performance are the same. One needs to understand (1) type of environmental/inherent stress that the devices experience and duration across its usage life (2) the failure modes that such stress can cause, (3) accelerated stress (run in lab) to duplicate such failure, and (4) acceleration model to interpret lab tests results to field performance.

Taking microbump open failure as an example, the cause of the failure is typically thermal cycling due to device power on/off and environmental temperature variation. Cyclic stress-strain will deform the solder material due to CTE mismatch in different electronic materials, thus inducing thermal fatigue failure. Thermal cycling (TC) or thermal shock (TS) tests can be used for accelerated testing of 3D packaging. JEDEC standard of temperature cycling provides different test conditions, where condition *G* (−40 to 125 °C), *J* (0–100 °C), *K* (0–125° C), *L* (−55 to 110 °C), and *M* (−40 to 150 °C) as shown in Fig. 14.27 can be used with frequency of 1 cycle/h and soak time of 15 min.

Two different approaches can be used to develop a life prediction model for microbump. One approach is to develop fatigue model by conducting displacement-controlled isothermal mechanical fatigue test using bulk solder material. The other is to develop fatigue model by combining actual reliability test data and FEA simulation results.

For the first method, Coffin-Manson strain-based model and Morrow's energy-based model have been reported:

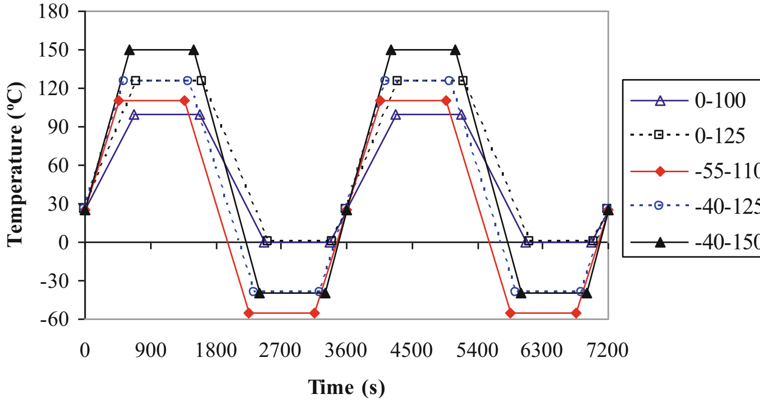


Fig. 14.27 Different thermal cycling profiles

$$N_f^m \Delta\varepsilon_{in} = C$$
$$N_f^n W_p = A$$

The fatigue ductility coefficient, *C* and *A*, and the fatigue exponent, *m* and *n,* for SAC bump can be obtained from strain-life and energy-life curves at different test conditions such as at 25, 75, and 125 °C with 0.1, 0.01, or 0.001 Hz, Temperature changes from –40 to 125 °C with 1 h per cycle during thermal cycling test. The highest temperatures of 125 °C and strain rate (low frequency at 0.001 Hz) in thermal cycling test have significant effect on solder joint fatigue failure. Hence, the isothermal test condition at temperature 125 °C with 0.001 Hz frequency was selected for further fatigue analysis. The *m*, *n*, *C*, and *A* are 0.853, 0.897, 9.2, 311.7 MPa (at 125 °C with 0.001 Hz), respectively reported by Pang et al. [24] (Fig. 14.28).

For the second method, the coefficient and exponent in fatigue model can be determined by combining numerical result and actual test data based on a damage mechanism. Schubert et al. proposed fatigue model for SAC bump solder determined by creep strain criteria and creep strain energy-based method based on FEA results and actual reliability test data (300 Ω as a failure criterion) from different assemblies such as FCOB with or without underfill and PBGA with Ni/Au board finish under different thermal cycling conditions:

$$N_f = 4.5{\varepsilon_{cr}}^{(-1.295)}$$
$$N_f = 345{\mathrm{W}_{cr}}^{(-1.02)}$$

When elastic-plastic-creep constitutive model for solder was used in FEA simulation, the inelastic strain includes two part, plastic strain and creep strain. When creep part is dominant, fatigue life can be predicted by substituting creep

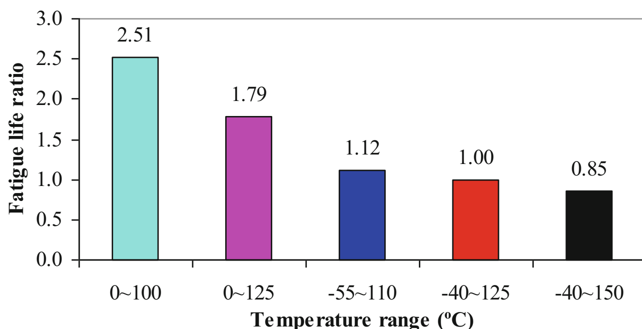


Fig. 14.28 Fatigue life ratio for different temperature ranges

strain or creep strain energy into above equations. When plastic part is dominant, fatigue life can be predicted by using plastic strain or plastic strain energy as fatigue damage parameter. Otherwise, fatigue life prediction also can be done using total inelastic parameter including creep and plastic parts as fatigue damage parameter. In addition, a combined creep-fatigue life prediction model for solder was proposed by Pang et al. [13, 29] as given below:

$$\frac{1}{N_\mathrm{f}} = \frac{1}{N_\mathrm{p}} + \frac{1}{N_\mathrm{c}}$$

14.5 Electromigration Reliability for 3D IC Packaging

To connect the hundreds of millions or even billions transistors on a Si chip in VLSI circuit technology, multilayers of thin-film interconnect wires made of Al or Cu were used. Electromigration (EM) in interconnects has been one of the most crucial and persistent reliability issues in Si-based microelectronic technology. Al or Cu interconnects usually have a small cross-sectional area. Thus, a very high current density will be carried, typically 10^5–10^6 A/cm^2. Under such high current density, atomic diffusion and rearrangement are enhanced, leading to void formation at the cathode and extrusion in the anode. The cathode and anode are sites of atomic flux divergence, which has been recognized. The analysis of back stress accompanying EM has also attracted much attention. When flip chip technology introduced the C-4 solder joint, the effect of current crowding on EM was found to occur near the contact area of solder joints with a current density about 10^4 A/cm^2 [1–9]. As consumer electronic products are ubiquitous in the big data era, its dense packaging in using very small size microbumps in 2.5D/3D IC requires a careful thermal management. While EM damage is still affected by flux divergence, back-stress, and current crowding, Joule heating is now the new focus.

After introducing the basic concepts in electromigration very briefly below, we will show experimental findings of EM damages in interconnects and flip chip solder joints. Then we will discuss EM failures of 3D IC in using the vertical stacking of Si chips containing the new interconnect structure of microbumps and TSVs. Based on these new structures, we will present their EM behaviors. Especially, we show that system level EM study is becoming important. In the system, a surprise was the failure of the redistribution layer (RDL) between the C-4 solder joints and the microbumps. In the system level EM test, heat dissipation becomes a critical problem. Synergistic effect of Joule heating and EM will be discussed.

14.5.1 Introduction on Electromigration

Electromigration is the interaction between electron flow and atomic diffusion. The electrical force acting on a diffusion atom is expressed by Huntington as below [43]:

$$F_{\mathrm{em}} = Z^{*} eE = \left(Z_{\mathrm{el}}^{*} + Z_{\mathrm{wd}}^{*}\right) eE$$

where e is the charge of an electron and E is the electric field, and Z^{*} is the effective charge number of EM and it consists of Z_{el}^{*} and Z_{wd}^{*}. Z_{el}^{*} can be regarded as the nominal valence of the diffusing ion in the metal when the dynamic screening effect is ignored. $Z_{\mathrm{el}}^{*}eE$ is called the direct force (or static force) and it is acting in the direction opposing electron flow. Z_{wd}^{*} is an assumed charge number representing the effect of momentum exchange between electrons and the diffusing ions. $Z_{\mathrm{wd}}^{*}eE$ is called the electron wind force (or dynamic force), which is acting in the same direction as electron flow. In EM-enhanced atomic diffusion, atoms are found to move in the same direction as the applied electron flow direction. Thus, electron wind force is much bigger than the direct force.

14.5.1.1 Back Stress

Among all the experimental studies of EM in Al interconnects, a couple of them deserve mentioning. One is the addition of Cu to Al lines to retard EM, and the other is the use Al short stripes designed by I. A. Blech for a direct observation of EM and the finding of the effect of back stress. In the latter, short stripes of Al were deposited onto a titanium nitride (TiN) film and stressed at a high current density. As Al resistivity was much lower than that of the TiN layer, the short stripes would carry most of the current, which result in the transportation of Al atoms from the cathode to the anode. It leads to the formation of void at cathode and hillock at the anode, which become observable and in turn measurable for quantitative analysis of the driving force of EM. Furthermore, it was found that the longer the stripe, the

more the depletion at the cathode side in EM. This was explained by the back stress below [43, 44].

The transport of Al atoms from the cathode to the anode will lead to compression in the latter and tension in the former. According to Nabarro-Herring model of creep where the equilibrium vacancy concentration is affected by the stress potential ($\sigma\Omega$), the tensile region has more vacancies and the compressive region has lesser vacancies than the unstressed region, so there is a vacancy gradient crossing the cathode to the anode. This gradient will induce an atomic flux of Al going from anode to cathode, which is opposite to the EM flux of Al. The vacancy concentration gradient depends on the length of Al stripe, and the shorter the stripe, the greater the gradient. At a certain short length defined as the critical length, the gradient is large enough to balance EM, so that no depletion at the cathode and no extrusion at the anode occur. At the steady state, the expression for the critical length is obtained as:

$$\Delta x = \frac{\Delta\sigma\Omega}{Z^{*}eE}$$

where Δx is the critical length, $\Delta\sigma\Omega$ is the stress potential difference, Z^* is effective charge number, e is electron charge, and E is electric field.

14.5.1.2 Statistical Analysis by Weibull Distribution Function in Reliability Study

In industrial manufacturing, it uses a statistical analysis for a large number of test samples in order to separate an early failure from the regular failure. The latter is acceptable because it follows the distribution and is expected, but the former is not because it is outside the distribution and is unexpected. Product assurance requires reliability tests of mean-time-to-failure (MTTF) besides the physical analysis of failure mode and failure mechanism. Knowing MTTF enables device engineers to predict the lifetime of devices. Here we will briefly introduce Weibull distribution and Black's MTTF equation. The Weibull distribution function is given below:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \tag{14.1}$$

where $F(t)$ is percentage or fraction of the failed sample as a function of time, η is the characteristic lifetime, and β is the shape factor or the slope of the Weibull plot. In Black's MTTF equation, there are three parameters: pre-factor A, current density power factor n, and activation energy E_a:

$$\mathrm{MTTF} = A(j^{-n})\exp\left(\frac{E_\mathrm{a}}{kT}\right) \quad (14.2)$$

With Black's equation, we can determine those parameters experimentally and obtain the statistical analysis. We need to conduct at the least the EM tests at two temperatures and two current densities. To find the activation energy and to determine n, we will not repeat them here, and the reader can use Google search or textbooks.

14.5.2 Experimental Studies of Electromigration in Al and Cu Interconnects

In the Al(Cu) interconnect, *W* via plugs are used to make vertical connections between different layers of Al lines, for example, the M2 or M1 metallization layers as shown in Fig. 14.29a. Since the atomic diffusion of *W* is much slower than Al, there will be flux divergence of Al atoms as well as vacancies located over the top of *W* via, and the divergence leads to hillock and void formation [45–48].

In comparison, the Cu dual-damascene structure is differently constructed [49, 50]. In Cu dual-damascene interconnects, the lower-level M2 trench and V1 that connects to the M1 level are simultaneously prepared before Cu electroplating,

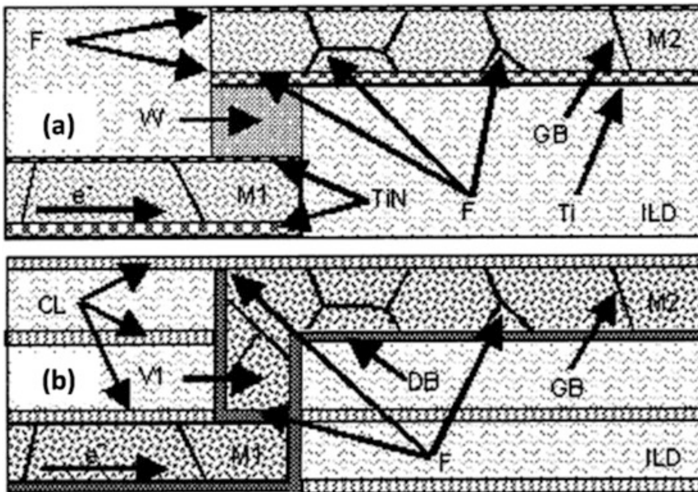


Fig. 14.29 (**a**) Idealized schematic of a two-level Al(Cu) or PVD Cu interconnect; (**b**) Idealized schematic of a two-level Cu interconnect. Where CL stands for capping layer, *DB* Ta barrier, e^{-} electron charge, *F* flux divergence region, *Ti* titanium layer, *TiN* titanium nitride layer, *V1* dual damascene via, *W* Tungsten plug, *GB* grain boundary, *ILD* interlevel dielectric, *M1* metal level 1, *M2* metal level 2

as shown in Fig. 14.29b. The M1 level is also separated from the V1 via by an electrically conducting diffusion barrier (DB) that also coats the inner walls of V1 and the side and bottom walls of the M2 trench. Consequently, the dual-damascene process places the flux divergence, not at the V1/M2 interface, which is the top of V1 as in Al(Cu), but at the M1/V1 interface at the bottom of V1. This via-bottom flux divergence is potentially problematic from a reliability standpoint because only a small amount of material depletion by EM will be sufficient for voiding damage to occur.

The dual-damascene interconnect is distinctly different from the previous Al (Cu) architecture in the other respect. It has been shown that EM in Cu interconnect occurs by surface diffusion at the device operation temperature of 100 °C. In processing the dual-damascene architecture, the top surface after electroplating must be chemical-mechanically polished and capped by a nitride layer before building of the next layer [51]. Because of the weak chemical bonding between the nitride and Cu, the interface can be regarded as a free surface of Cu diffusion and allows rapid surface diffusion of Cu resulting in EM reliability concern. As indicated in Fig. 14.29, a flux divergence exists at the cathode end of the M2 interconnect where Ta barrier and capping nitride layer intersect. And void would naturally form at this location.

14.5.3 Electromigration in Flip Chip Solder Joints

In C-4 flip chip solder joints, the current crowding usually occurs at the entrance and departure point of electron flow. This is because the cross-sectional area of thin Al line is much smaller compared to flip chip solder joints. Current crowding occurs at the entrance of the flip chip solder joint and tends to drive in Sn atoms in downward direction and hence vacancy comes back in reverse direction resulting in voids formation. After voids formation, current will move ahead of existing void, pushing Sn atoms down again and hence leading to the pancake type of void formation continuously along solder/UBM interface. As shown in Fig. 14.30, pancake type of void can be observed in bump No. 5, 3, and 1, which electron flow enters left corner of the solder joints [52–54].

14.5.4 System Level Electromigration Studies in 3D IC Packaging

Packaging technology is currently in transition from 2D ICs technology to 3D ICs to meet the requirements of consumer electronic products. Compared to flip chip technology in 2D IC, TSV and microbump are new. Besides, the dimension of microbumps in 3D ICs is shrunk by a factor of 10 and the manufacturing and

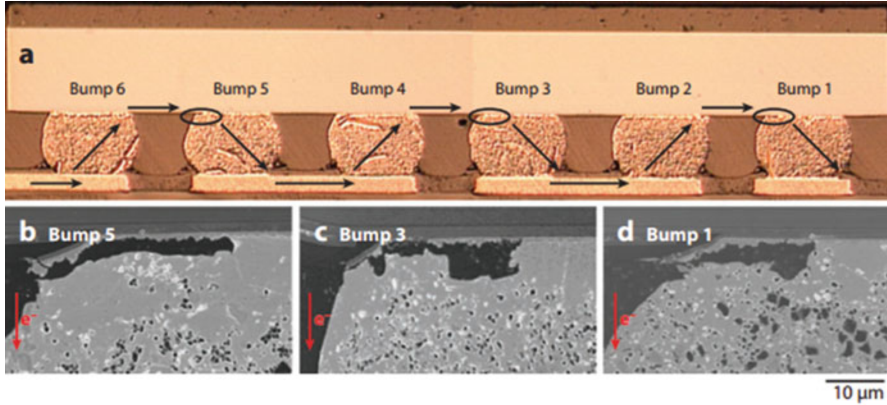


Fig. 14.30 (**a**) Optical microscope image to show current flow in daisy chain of solder joints. (**b**) SEM image to show package voids formation after electromigration [52]

structure of Cu-filled TSVs are also new. Based on these two reasons, the studies of electromigration failure in microbumps and TSVs have received much attention lately. In addition, system level electromigration study is new in 3D IC because heat dissipation becomes a problem. Synergistic effect of Joule heating and electromigration will be the trend of reliability failure in the near future.

14.5.4.1 Electromigration in Microbumps

Microbumps have a size reduction of ten times from that of a C-4 joint. Yet, the total volume shall shrink 1000 times and it affects EM behavior [29, 55–61]. It has been found that microbumps show a much better resistance to EM than traditional flip chip solder joints and no pancake type of void has been observed in microbumps. Figure 14.31 shows one of the EM testing results [20]. In the sample, microbumps adopted Ni as UBM. The testing condition of (a) and (b) was 4950 h at $8.8 \times 10^4\ \mathrm{A/cm^2}$ and 150 °C, and (c) and (d) was 2850 h at $1 \times 10^5\ \mathrm{A/cm^2}$ and 150 °C. There is no observable EM failure in microbumps.

The reason that microbump has robust EM resistance is partially because the percentage of intermetallic compound (IMC) in the microbump was very high. Furthermore, during EM, microbumps with remaining solder can be converted to total IMC microbumps at the early stage of electromigration, as we can see in Fig. 14.31, the entire bump has been changed into IMC after the EM test. Since IMC has a better resistance to EM, microbumps can survive at a higher temperature and higher current density during EM testing compared to C-4 solder joints.

Another possible explanation of superior EM resistance of microbump can be related to back stress [43]. As discussed in Sect. 14.5.1.1, at constant current density, when the length of Al stripe is smaller than the critical length, there is no EM damage. Due to the scaling trend, the height of the solder layer in microbumps

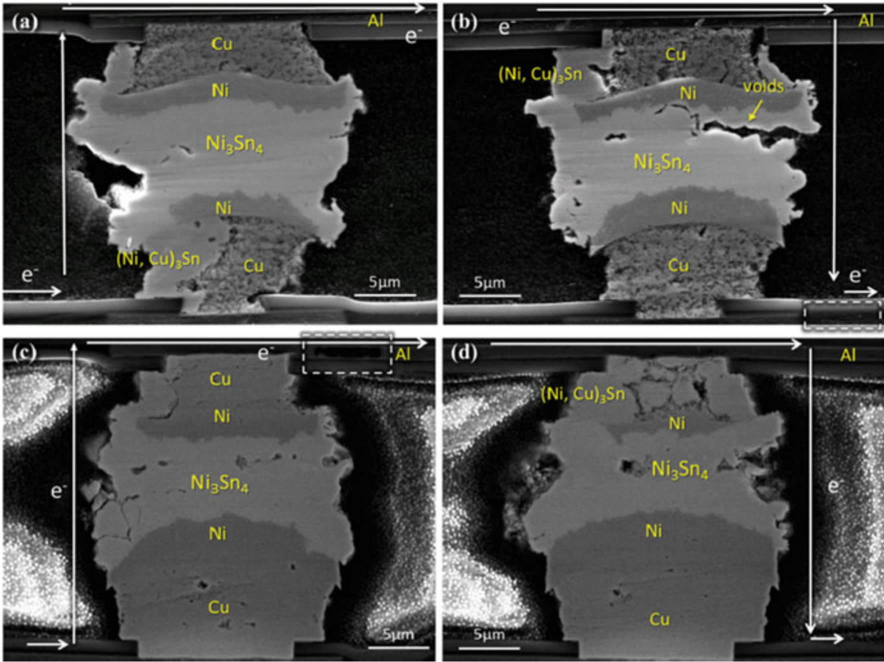


Fig. 14.31 Cross-sectional SEM images of microbump after current stressing of (**a**) and (**b**) 4950 h at 8 × 10^4 A/cm^2 and 150 °C, and (**c**) and (**d**) 2850 h at 1 × 10^5 A/cm^2 and 150 °C [55]

will shrink to less than 5 μm. This height is probably smaller than the critical length at the tested current density condition. However, typically it is a system that is under EM test. Usually when current density increased, Al lines, Cu redistribution layer or under ball metallization (UBM) tends to fail first. Actually, some studies even report that no failure of microbumps was observed before it was failed by Joule heating when the current density increased. Right now although many studies have been reported on electromigration failure related to microbumps, there is no direct observation of EM induced voids formation failure in microbumps.

14.5.4.2 Electromigration in TSVs

Early reliability studies of TSV started during the last decade with thermomechanical simulations, since the thermal expansion mismatch between Cu TSV and Si die is very large. Several studies evaluated, through finite element simulations, fatigue of Cu TSV, delamination at TSV interfaces, and Si cracking due to thermomechanical stress. These studies point out that the existence of the Cu TSV affects the stress distributions and the interconnection reliability [62–64]. For EM, most studies focus on matter flux diffusion modeling at TSV interfaces, but there is no sufficient emphasis on experimental results [65–67].

Frank, Moreau [68–70] and their group did EM experimental analysis of a high density Cu TSV-last technology of 2–4 μm diameters, and 15 μm of length. EM-induced voids were found in the adjacent metal level, right at TSV interface. Moreover, the expected lifetime benefit by increasing line thickness did not occur due to increasing dispersion of voiding mechanism. They also reported EM experimental reliability of Cu TSV-middle technology of 10 μm diameter and 80 μm thickness. EM revealed similar degradation mechanism and kinetics as those in TSV-last approach. Figure 14.32 shows the FIB cross-sectional image of the failure in both the thin and thick process on TSV-last approach.

For thin metal process, current density exponent n and activation energy E_A of Black's equation are extracted through MTTF data. Very close values are obtained for both configurations. $E_A = 0.9 \pm 0.1$ eV is the expected activation energy for surface diffusion of Cu on Cu damascene surfaces, ensuring by SiN capping. $n = 2 \pm 0.2$ is acceptable regarding the theoretical value of 2 to be expected. Yet it might be affected by local Joule heating in the TiN barrier as void becomes larger than the TSV section. As failure is revealed to be driven by void growth, any aging extrapolations should be made with a consistent but conservative value $n = 1$.

For thick metal process, activation energy and current exponent for downstream configuration are, respectively, of 0.8 ± 0.2 eV and $n = 2.4 \pm 0.3$, which are close to values of the thin metal level process, but it is less accurate due to the difference in lognormal standard deviation between MTTF distributions.

With the same $E_A = 0.9$ eV, and a conservative $n = 1$, the MTTF distributions of both thin and thick metallization processes are extrapolated at same operation conditions of current and temperature. At 50 % cumulative failure, the benefit of thick metallization process is about six times higher than thin metallization process. However, since lifetime is always extrapolated at 0.1 % cumulative failure, thicker process has at this cumulative failure no significant benefit (only 1.1 times thin process).

Another group from Samsung [71] also found the similar EM results. Electromigration-induced voids were found at Cu/SiN interface between TSV bottom and backside metal, but not at TSV itself due to the unexpectedly strong reliability of TSV.

14.5.5 System Level Weak-Link Failure in 2.5D Integrated Circuits

In system level EM test of 2.5D integrated circuits, a new failure mode due to synergistic effect of Joule heating and EM has been found [38]. In the test circuit, there are three levels of solder joints, two Si dies (one of them serves as interposer and has TSVs) and one polymer substrate. In addition, there are two redistribution layers, one between every two levels of the solder joints. It has been found that the redistribution layer (RDL) between the flip chip solder joints and microbumps is the

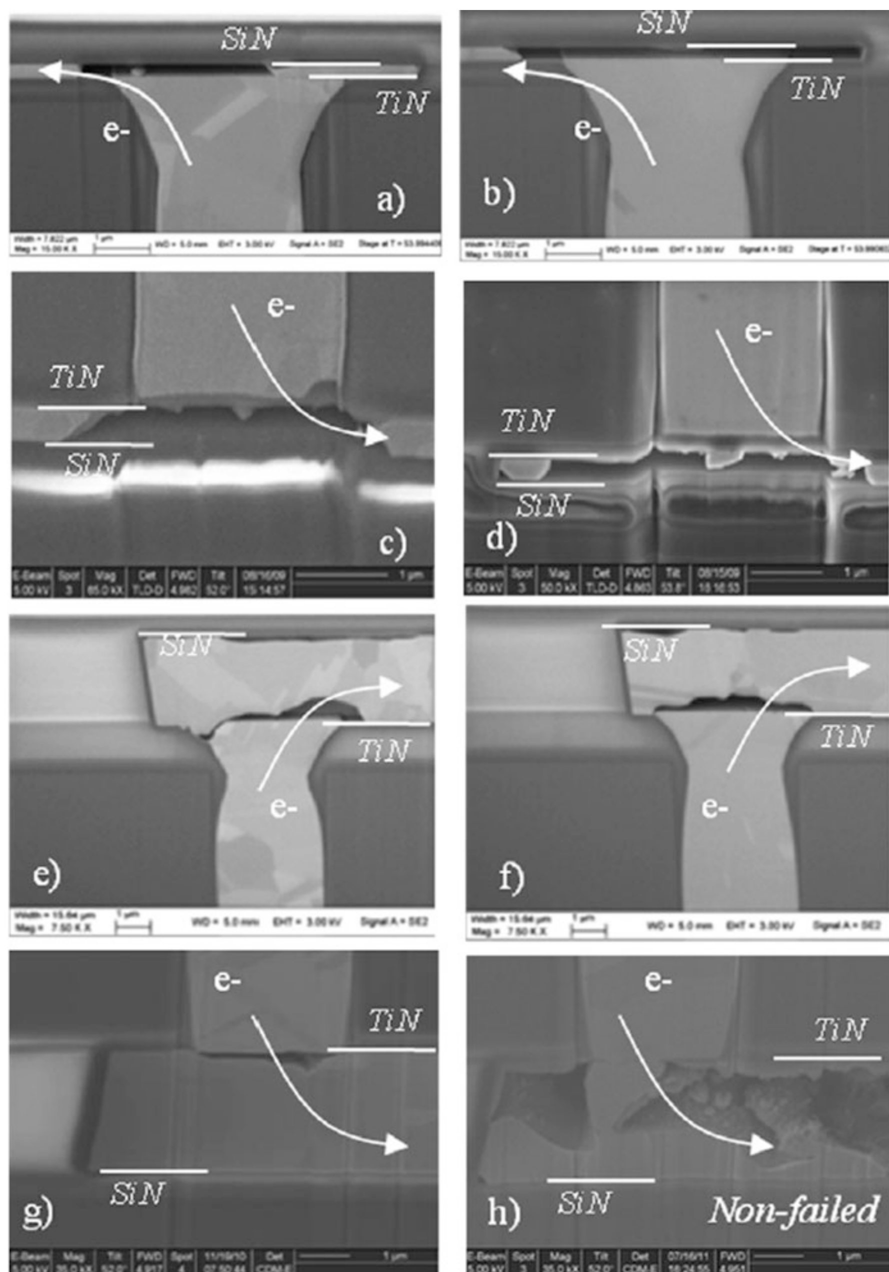


Fig. 14.32 Failure analyses of two samples for: (**a** and **b**) thin process upstream; (**c** and **d**) thin process downstream; (**e** and **f**) thick process upstream and (**g** and **h**) thick process downstream [68]

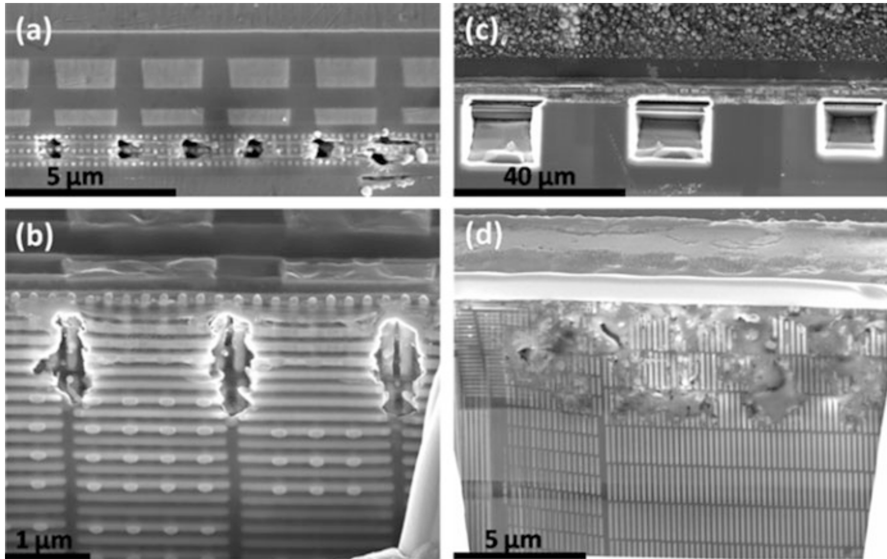


Fig. 14.33 Failure site images (**a** and **c**) and their corresponding FIB cut images (**b** and **d**). In (**c**), the failure site is really big, about 80 μm long. FIB was used to cut three holes at the beginning, the middle, and the end of the failure site [72]

weaklink and failed easily by burnout in EM test, as shown in Fig. 14.33. There are six periodic burnout holes in Fig. 14.33a. In Fig. 14.33d, the burnout area is quite big, about 80 μm. The failure is time-dependent with a sudden resistance increase.

The reason of this new failure mode to occur is due to the difficulty of thermal dissipation in the structure. The design of the network structure of Cu line in RDL is very compact when compared to previous Cu or Al structures studied in the literature. Besides the compact structure, the reduced Si interposer layer thickness also leads to the poor heat dissipation. What's more, the thickness of Si chip has a tendency of decreasing with the trend of smaller packaging size. Right now, in 3D IC, the stacked chip is about 50 μm, which is much less than the typical thickness of Si wafer at 200 μm. The heat conduction of Si interposer is much reduced and it becomes one of the reasons why heat dissipation is poor. These situations are very different from the previous EM studies carried out in Cu and Al lines reported in the literature. Joule heating generation and dissipation is a critical issue, leading to the time-dependent heat accumulation and temperature increase. These special situations result in the new failure mode, the time-dependent failure of burnout in EM test. The simulation results show that Joule heating has a positive feedback to EM in the redistribution layer and caused the thermal runaway failure [72].

This synergistic effect of Joule heating and EM on burnout is a new failure mode of reliability. Joule heating will be the critical issue as the density of transistor becomes increasingly higher while the form factor is reduced in mobile devices. This synergistic effect can couple with mechanical and other failure in the future. Clearly, it needs our attention and requires more in-depth understanding.

14.5.6 Concluding Remarks

Electromigration and Joule heating are of concern for 3D IC packaging. In microbumps, 100 % IMC can help increase MTTF at higher current density. TSV also has a higher resistance to EM failure. Nevertheless, EM failure can be transferred to RDL layer when it is poorly designed. In a complicated 3D IC system, Joule heating must be considered during the design stage to avoid current crowding not only in solder joints but also in redistribution metal layers. And EM failure always occurs in the weakest link of the system. By including EM design rules upfront in manufacturing may help predict or even prevent the weakest link failure in the system level happen.

14.6 Thermomigration in 3D IC Packaging

14.6.1 Introduction

For the thermal management in 3D IC, heat generation and dissipation among the stack of chips is the most critical reliability issue. When the Si chips are stacked vertically with the dielectric underfill in between, the heat generation from Joule heating of transistors in silicon chips is very large whereas the heat dissipation is very bad due to the poor thermal conductivity of the underfill materials. Meanwhile, heat dissipation depends on the temperature gradient according to Fourier's law. While a large thermal gradient is better for heat dissipation, it might lead to thermomigration (TM), which is another reliability concern in this review [73].

In flip chip solder joints, a temperature gradient of 1000 °C/cm is sufficient to induce TM according to many studies reported [74–76]. TM is a reliability concern because it will lead to phase redistribution and void formation, which will cause failure. For the eutectic Pb-Sn solder joint, Pb is found to be the dominant diffusing species in TM, and it will diffuse from the hot end to cold end [77]. TM for Pb-free solder joint is also well studied, and Sn is determined to move from the cold end to hot end with a positive heat of transport [78]. If we assume for microbumps, TM will also occur at the same temperature difference, i.e., 1 °C, across a microbump having a diameter of 10 μm, it will induce a serious thermomigration failure. It is hard to guarantee that we can control a temperature difference of 1 °C. Hence, the reliability problem associated with TM must be studied for microbumps. First, we shall discuss the fundamentals of TM. Then, we will discuss the observation of TM in flip chip solder joints. Finally, we will present the new challenges in TM for microbumps used in 3D IC packaging.

14.6.2 Fundamentals of Thermomigration

TM is the phenomenon of atomic diffusion driven by a temperature gradient. Classically, it is called the Soret effect. Mathematically, the driving force of TM can be expressed as

$$F = -\frac{Q^*}{T}\left(\frac{\partial T}{\partial x}\right)$$

where Q^* is the heat of transport, which is defined by the difference between heat carried by a moving atoms per mole and the heat of atoms per mole at the initial state (the hot end or the cold end), T is the working temperature, and $\frac{\partial T}{\partial x}$ is temperature gradient. The atomic flux due to the presence of TM has been expressed as

$$J = C\frac{D}{kT}\frac{Q^*}{T}\left(-\frac{\partial T}{\partial x}\right)$$

where C is the atomic concentration and D is the diffusivity of the diffusing atom at the working temperature [79].

14.6.2.1 Traditional TM Studies

To measure the Q^* and determine the dominant diffusing species in solder joints, insitu observation of TM has been conducted in traditional C-4 flip chip solder joints. TM in eutectic 63Sn37Pb flip-chip solder joints has been reported. Typically, TM is accompanied by EM when electric current is applied to the solder joints [80]. In order to decouple the electromigration effect, the neighboring unpowered solder joints, which are only subjected TM, are used to study TM effects. Figure 14.34 shows a typical arrangement of TM test. In this sample, there are 11 solder joints, but only a pair of them (number 6/7) are powered, and the rest of them are unpowered. The last bump (number 12) is at the as-received state for reference. The UBM thin films on the chip side were Al (~0.3 μm)/Ni(V) (~0.3 μm)/ Cu (~0.7 μm) deposited by sputtering. The bondpad metal layers on the substrate side were Ni (5 μm)/Au (0.05 μm) prepared by electroplating. The bump height between the UBM and the bond pad is 90 μm, and the solder bump material is eutectic SnPb [79].

Since the on-chip Al interconnects are the source of Joule heating and Si is a good thermal conductor, a temperature gradient was produced across all the solder bumps and caused TM in all of them. In this case, the Si chip side is the hot side while the FR4 substrate side is the cold side.

Figure 14.34 shows the SEM cross-section image after a DC current stressing of 0.95 A at 100 °C for 27 h. The average current density at the contact opening was

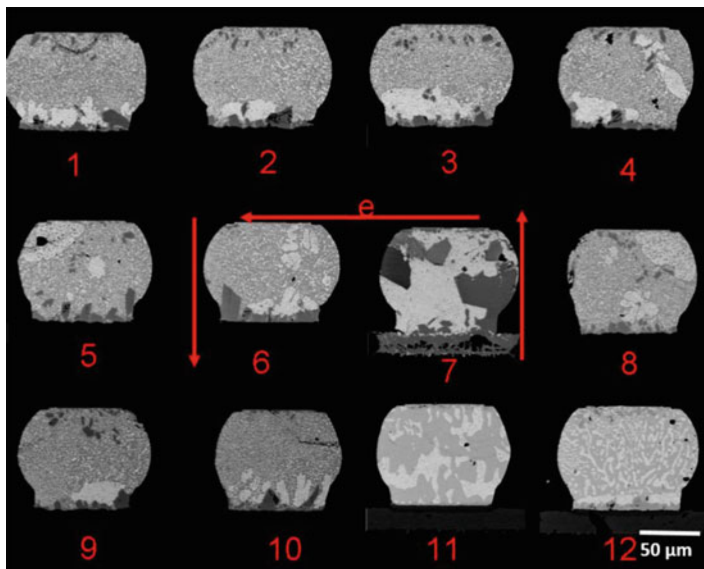


Fig. 14.34 SEM cross-section image after only one pair of them subjected to current stressing (Courtesy of Professor Ouyang Fanyi, National Tsing Hua University)

$1.5 \times 10^4\ \mathrm{A/cm^2}$ [78]. The current flow direction is marked on the image. The lighter color in the SEM image represents Pb-rich phase and the darker color represents Sn-rich phase. Compared with the as-received sample, we can see that the Pb-rich phase has moved from chip side (hot side) to substrate side (cold side) in the unpowered bumps.

Due to environmental concerns, Pb-free solders are introduced to replace the eutectic SnPb solder. The TM effect in Pb-free SAC305 has also been studied for reliability concern [81–84]. For in-situ sample preparation, the sample was usually first polished down to the half of solder bumps, and then an array of markers was indented on one of the cross-sectioned solder joint surface to determine the direction and magnitude of atomic flux in TM [78]. Figure 14.34 shows the SEM cross-section of Pb-free solder bumps before and after TM at an AC current density of $1 \times 10^4\ \mathrm{A/cm^2}$ and at 100 °C for 800 h [81]. It is assumed that no EM occurs in AC, yet Joule heating remains. The temperature gradient across the solder bump was found to be around 2800 °C/cm. We can see that hillock formation occurs at the hot side. Also the Ag in solder was found to migrate to the cold side. The marker was found to move toward the substrate side (cold end), indicating that the dominant species in the TM has moved to the hot side. Based on the atomic flux measured through marker motion, the Sn transport heat is measured to be 1.36 kJ/mol in this study. The test structure similar to Fig. 14.34 is also designed for Pb-free solder bump to study TM, of which two bumps are under current stressing in order to generate Joule heating, while others are under TM [78]. Figure 14.35 shows the SEM cross-section of Pb-free unpowered solder bumps after TM at 150 °C. The

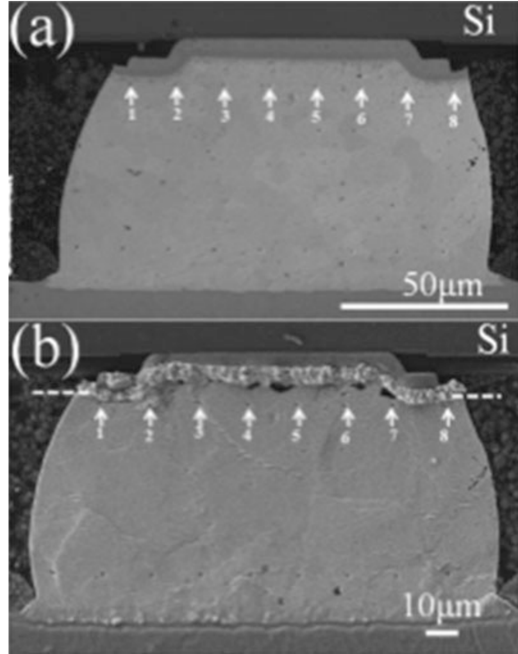


Fig. 14.35 Cross-section SEM images of the sample (**a**) before and (**b**) after thermomigration respectively at an AC current density of 1×10^4 A/cm^2 at 100 °C for 800 h [81]

temperature gradient is simulated to be around 250 °C/cm. We can see that the cold end has depletion while the hot end has protrusion. EDX data shows that Sn diffused to the hot end while Ag diffused to the cold end, which agrees with the TM study under AC stressing (Fig. 14.36).

14.6.3 Thermomigration Studies in 3D IC Packaging

In 3D IC packaging, chip-to-chip interconnections are enabled by through silicon via (TSV) and microbumps. The diameter of microbumps is usually below 20 μm, and is being scaled towards 5 μm. The solder joint is dominated by IMC due to rapid reaction with under-bump metallization (UBM) during reflow. In this section, we will discuss the TM issue in microbumps.

14.6.3.1 Thermomigration in Microbumps

The TM effect on microbumps reliability was first reported on the effect of asymmetrical IMC formation during reflow or solid state annealing with a temperature gradient [85]. Figure 14.37a, b displays the evolution of the microstructure of microbumps before and after subject to a temperature gradient of 7308 °C/cm at 145 °C, respectively [86]. Compared to the as-received samples shown in

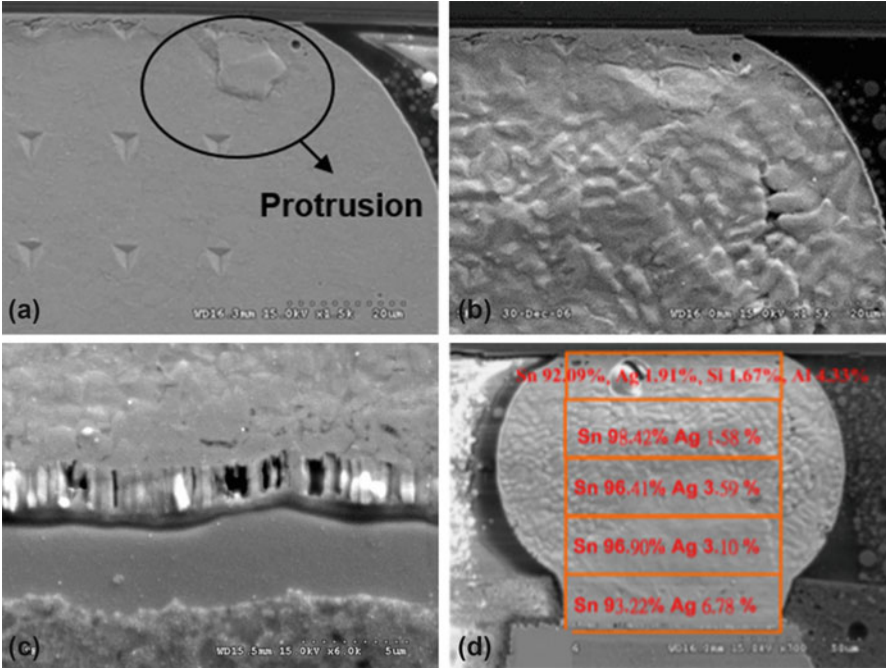


Fig. 14.36 SEM cross-section image of thermomigration bump at (**a**) 26 h; (**b**) chip side for 62 h; (**c**) substrate side for 62 h; (**d**) EDX data for the thermomigration bump after 62 h [78]

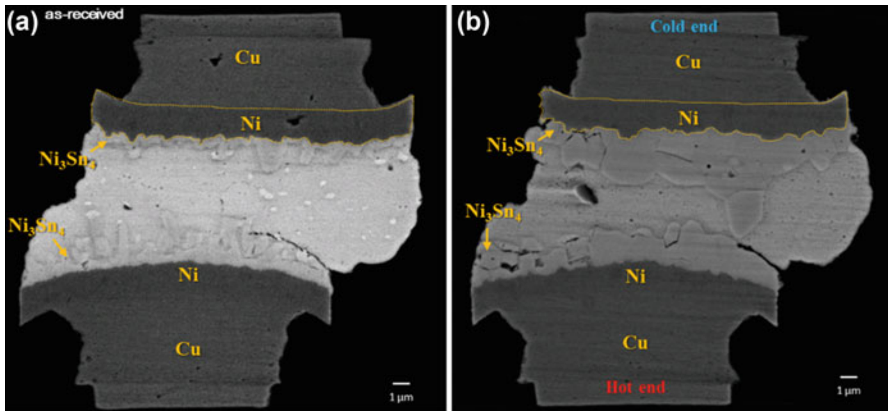


Fig. 14.37 Cross-sectional SEM images of a microbump (**a**) before and (**b**) after thermomigration of 7308 °C/cm at 145 °C

Fig. 14.34a, we see that Fig. 14.34b reveals a thicker IMC appeared in the cold end, which indicates that temperature gradient enhances the Ni diffusion interstitially inside Sn going from the hot end to cold end, and has caused more IMC formation at the cold end. What is interesting is that the TM effect on Sn is less significant for

microbumps than that for flip chip solder joint [87], especially when the bump height is below 5 μm. One of possible reasons is that the back stress induced vacancy flux is in the opposite direction of TM-induced flux. In principle, when a solder joint is under a temperature gradient, TM induces mass transport of Sn from the cold to the hot end. The latter will be in compression and the former in tension. Based on the Nabarro-Herring model of equilibrium vacancy concentration in a stressed solid, the tensile region possesses more vacancies than the unstressed solid, whereas the compressive regions possess fewer vacancies, resulting in a stress-induced vacancy flux from hot to cold end. The driving force of TM is counteracted by this chemical-mechanical force, which is called back stress. Thus, the driving force of TM could be expressed as

$$F = -\frac{Q^*}{T}\left(\frac{\partial T}{\partial x}\right) - F_{\mathrm{BS}}$$

where

$$F_{\mathrm{BS}} = \frac{d\sigma\Omega}{dx} = \frac{(\sigma_1 - \sigma_2)\Omega}{d}$$

where F_{BS} is the back stress, σ_1 and σ_2 are the maximum hydrostatic stresses at each end of bump, Ω is atomic volume, and x or d is the height of solder. For flip chip solder joint, x is typically around 100 μm, while for microbumps, x is typically around 5 μm. The shrinkage of bump height will dramatically affect the back stress, and then affect the net effect of TM. In EM study, we note that there is also a back stress which goes against the electron wind force, and it will balance out EM effect when the metal stripe is under the critical length (Fig. 14.37).

14.6.3.2 Thermomigration in TSV

Through Silicon Via (TSV) is typically made of Cu, the TM of Cu is different from solder, because the latter is typically a binary alloy except pure Sn. So far, there is no literature reported regarding to the TM issue of TSV. However, TM will happen in pure metal. In [88], both the net diffusion of Cu and Au are studied under thermal gradient. It is found that Cu can diffuse from hot end to cold end when the temperature gradient is in the order of 1000 °C/cm [88] with a positive heat of transport. This means that for a TSV with 50 μm in height, 5 °C difference across TSV will trigger TM. However, TM reliability issue of pure metal interconnect, such as Cu interconnects, is not well reported. The reason is possibly related to back stress. Because device is usually working at 100 °C, this temperature is too low for creep to take place in Cu. When TM drives more Cu atoms from the hot side into the cold side (or the reverse direction depending on the heat of transport), the stress will build up at the end where atomic accumulation occurs, and then the stress gradient will produce an atomic flux of Cu against the TM.

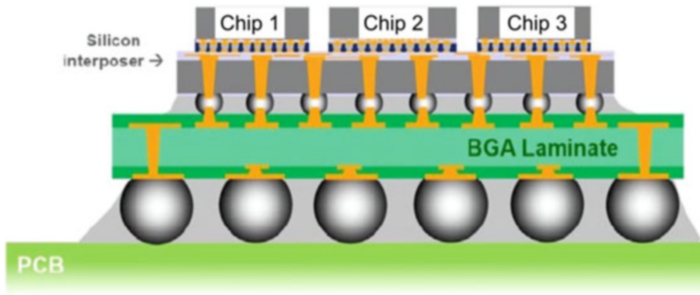


Fig. 14.38 2.5D multi-chip horizontal arrangement (adapted from Yole Développement)

Since TSV is connected to the redistribution layer at both ends, and the current crowding will occur at the interfaces, it is possible that the local Joule heating due to current crowding will create a temperature gradient that is high enough for TM to occur. Meanwhile, due to the high power density and poor heat dissipation in 3D IC, the working temperature around TSV might be high enough for creep to take place in Cu, in which case the back stress may not play a role.

14.6.3.3 Thermomigration Induced by Thermal Crosstalk

In 2.5D IC packaging design, a layer of Si interposer is used in between dies and substrate to mitigate the chip-packaging interaction. Nevertheless, this new design can also cause new reliability issue such as thermal crosstalk-induced thermomigration. Figure 14.38 shows that two Si chips are horizontally placed on one Si interposer. Since Si is a good heat conductor, if chip 1 is powered, the Joule heating can be transported to the bottom of chip 2. However, the top of chip 2 is not heated because the gap between chip 1 and chip 2 is filled with underfill materials, which is a poor thermal conductor. Therefore, chip 2 will undergo TM with the interposer side to be the hot side while chip 1 is powered. This phenomenon is called thermal crosstalk. The thermal cross-talk will be a reliability issue if we use Si interposer as the new substrate, and it deserves more research efforts.

14.6.4 Concluding Remarks

The TM effect of traditional interconnects has been summarized, including eutectic Pb-Sn solder joint and Pb-free flip chip solder joint. From the previous studies of flip chip solder joints, we can conclude that a temperature gradient of 1000 °C/cm will cause Pb to diffuse from hot end to cold end with Q^* to be -25.3 kJ/mol, and it causes Sn to diffuse from cold end to hot end with Q^* to be $+1.36$ kJ/mol. The materials driven away by thermal gradient will form void and cause reliability

issue. The study of TM of new interconnect structures in 3D IC, such as microbumps and TSVs, is still ongoing. At present, microbump is found to be more resistant to TM because of its lower bump height (higher back stress), and stronger bonding in IMC. However, the asymmetrical IMC growth will occur inside microbumps under a temperature gradient. The study of TM in TSV is few. We can only conclude from precious study of pure Cu that 5 °C difference for a 10-μm-long TSV will induce TM. Finally, the use of Si interposer will cause new TM issue due to thermal crosstalk between the horizontal dies. It is a new reliability issue due to heterogeneous integration of various chips on a common interposer of good thermal conduction.

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