Chapter 12
Fluorine-Implanted Enhancement-Mode Transistors

Kevin J. Chen

12.1 Introduction: Fluorine in III-Nitride Heterostructures: Robust V_{th} Control

The fluorine plasma ion implantation approach was discovered when large positive shift in V_{th} was observed in AlGaN/GaN HEMTs as F ions were incorporated into the barrier layer by carbon tetrafluoride (CF_4) plasma treatment, whose major role is identified as providing F ions with enough energy to penetrate into the subsurface layer of III-nitride epitaxial layers grown along the [0001] direction [1, 2]. The effectiveness of fluorine implantation technique in GaN and related compounds stems from the strong electronegativity of F element and the intrinsic III-nitride wurtzite crystal structure. In AlGaN/GaN heterostructures, because of the very tight lattice structure (with an in-plane lattice constant of a ~3.2 Å), the implanted F ions tend to be stabilized at the interstitial sites by the repulsive forces from the neighboring atoms (Al, Ga, or N). Since group-VII F has the strongest electronegativity among all the chemical elements, a single F ion at the interstitial site tends to capture a free electron and becomes a negative fixed charge. These negative fixed charges subsequently modulate the local potential and deplete the 2DEG in the channel, as shown in Fig. 12.1b. The amount of the V_{th} shift can be robustly controlled by the implantation time, as shown in Fig. 12.2. The fluorine plasma implantation technique also leads to the first demonstration of E-mode GaN-on-Si HEMTs [3].

The RF plasma power is another parameter that needs to be adjusted during process optimization. While this power needs to exceed a lower bound (in the range of ~100–250 W depending on the specific plasma systems used) to introduce

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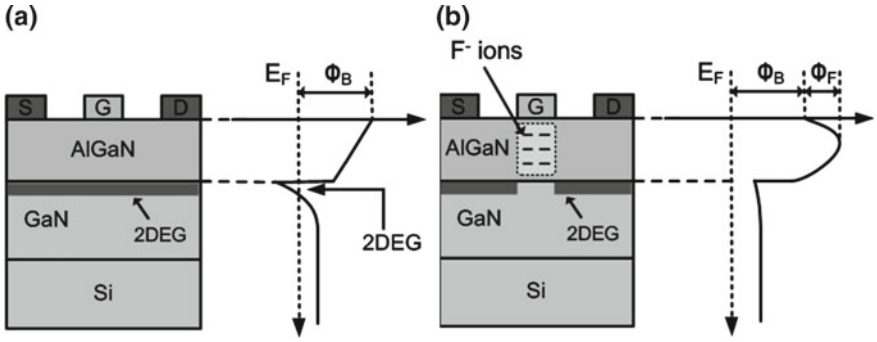

Fig. 12.1 Cross section and the conduction band profiles of standard **a** normally on and **b** normally off AlGaN/GaN HEMTs. The normally off HEMT features F^- ions incorporated in the AlGaN barrier by plasma ion implantation

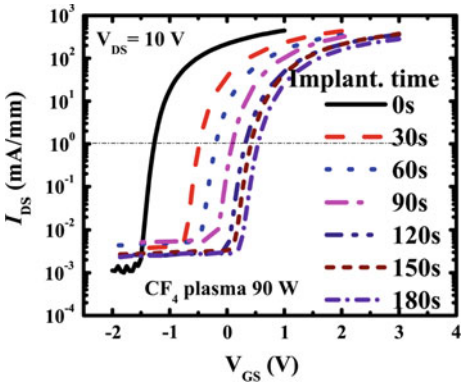

Fig. 12.2 Transfer characteristics of AlGaN/GaN HEMTs with different fluorine plasma ion implantation times

significant V_{th} shift, it is preferred to keep this power as low as possible in order to minimize the plasma-induced lattice damages and the amount of F ions that can penetrate to the channel region. Annealing at 400 °C has been proven to be effective in removing majority of the plasma-induced damages. The nature of the ion implantation process, however, indicates that there is a small amount of F ions in the 2DEG channel, presenting themselves as impurities that could lead to slight mobility degradation. With process optimization, the 2DEG mobility degradation can be reduced to 10–20 %.

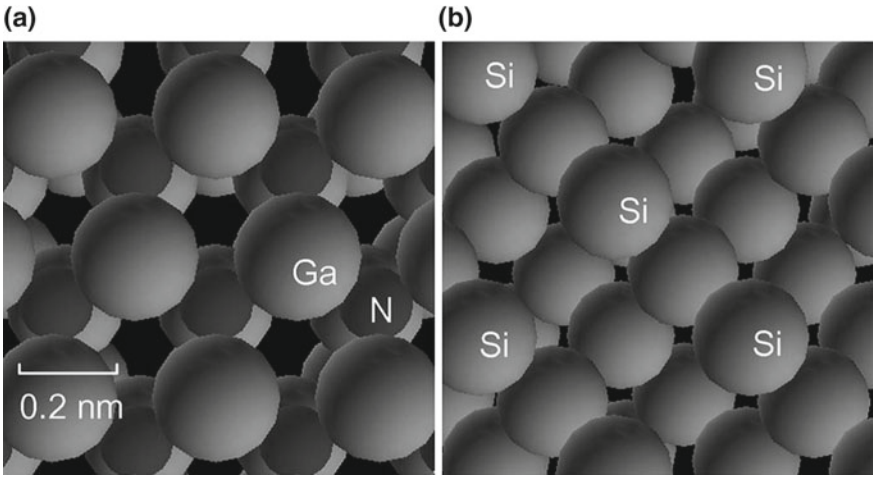

Fig. 12.3 Top view of **a** Ga-faced (0001) GaN wurtzite crystal, and **b** (100) Si crystal. The same physical scale is used in (**a**) and (**b**). Even Si features larger lattice constant (5.43 Å), there is little opening along the incident direction

12.2 Physics Mechanism of Fluorine Implantation

12.2.1 Atomistic Modeling of F Plasma Ion Implantation

To provide a theoretical framework for understanding the physical mechanisms and developing a modeling tool for process design and optimization, it is necessary to develop an approach capable of predicting the ion or dopant distribution profiles and the effects of the ion–solid interactions.

Despite the high atomic densities of GaN and related compound, low-energy (0.1–1.0 keV) F ions are able to penetrate to a shallow depth in AlGaN/GaN heterostructures, partially as a result of the narrow opening channels along the [0001] GaN, as shown in Fig. 12.3. A molecular dynamics (MD) simulation framework [4] was established to study the F plasma implantation into III-nitride material system, because the MD simulation takes into account the ion–lattice interactions on an atomistic scale and includes lattice structure information that is absent in other more traditional implantation simulation tools such as Stopping and Range of Ions in Matter (SRIM) which are based on Monte Carlo method. The MD simulation also provides time and space evolution of atomic coordinates, resembling a real-time observation of the F ion implantation process.

The substrate structure under study is a standard C-plane AlGaN/GaN HEMT structure with a 20-nm AlGaN barrier layer. F^- ions are implanted by CF_4 plasma into the region under the gate. The regular wurtzite lattice structure is applied to model both AlGaN and GaN layers in the MD simulation. Because of its small thickness (20 nm), the AlGaN barrier is assumed to be strained without any lattice

relaxation. Thus, the piezoelectric charge polarization and the slight variation in the vertical lattice constant, as a result of the strained AlGaN layer, are both considered in MD simulations. It was found that the charge polarization has negligible effect on the fluorine dopant profiles.

According to published results [5], F^- and CF_3^+ ions are the main ions existing in CF_4 plasma. However, after CF_4 plasma implantation, no obvious change has been observed in the carbon concentration according to SIMS (second ion mass spectroscopy) measurement and the detected carbons are already in presence in the as-grown sample. There are two possible causes for this phenomenon, (1) F^- is much lighter than CF_3^+, with a mass ratio of 9:33. With the same acceleration time determined by the RF signal applied across the two electrodes driving the plasma, majority of F^- ions travel enough distance to reach the sample, which is located at the bottom electrode. On the contrary, only small fraction of CF_3^+ can reach the sample surface before the electric field reverses its direction and pulls the ions away from the sample; (2) In the plasma system, the bottom electrode is grounded, and the top electrode is capacitively coupled to the RF source. Thus, a negative self-bias in the order of several hundreds of volts is induced at the top electrode, which attracts CF_3^+ and pulls them away from the sample. It should be noticed that the absence of additional C atoms in the sample is preferred because C impurities present adverse effects to AlGaN/GaN HEMT [6].

With MD simulation, the 1-D profile of F ion in AlGaN/GaN heterostructure is calculated and plotted in Fig. 12.4, along with the experimental results measured by SIMS. The simulation results with a (100) Si substrate are also calculated as reference. Excellent agreement between simulation and measurement is obtained in the case of F ion in AlGaN/GaN heterostructure. It can be seen that F ion implantation in AlGaN/GaN could get a smaller full width at half maximum (FWHM) compared to Si. This can be explained by the higher density of $Al_{0.3}Ga_{0.7}N$ (5.19 g/cm^3) compared to Si (2.33 g/cm^3).

In the region near the substrate surface, i.e., in the AlGaN layer, the F concentration exhibits a Gaussian-like profile. F ions can penetrate deeper into AlGaN/GaN heterojunction than (100) Si, despite higher atomic density in AlGaN/GaN, indicating a strong channeling effect for the F ions in III-nitride wurtzite lattice structure.

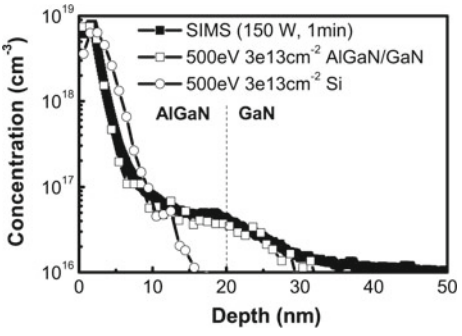

Fig. 12.4 Simulated F profiles in AlGaN/GaN and Si by MD simulation. The implantation energy of F ion is 500 eV and the dose of F is 3×10^{13} cm^{-2}. The F profile in an implanted AlGaN/GaN sample was measured by SIMS and plotted for comparison

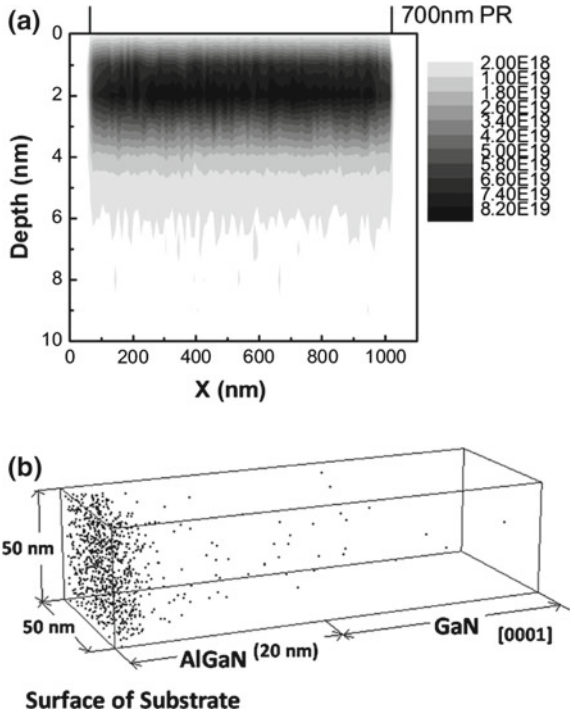

Fig. 12.5 **a** 2-D and **b** 3-D F ion distribution profiles by molecular dynamics simulations. In (**a**), the gate length is 1 μm and the height of the protection mask (photoresist) is 700 nm. In (**b**), a $50 \times 50 \times 40$ nm volume was considered

From the top views of both III-nitride wurtzite lattice and (100) Si crystal structure, it can be seen that there are many channels available in GaN for incident fluorine ions to go through, while the cubic lattice of silicon does not provide these open channels in the direction of implantation.

2-D and 3-D F distribution profiles have been simulated, as shown in Fig. 12.5. The simulation tool considers F ions with all possible incident angles. It should be noted that the F ions penetrating into the AlGaN/GaN structure are capable of inducing vacancies along the implantation path. The long-term high-temperature (400 °C) annealing indicates no shift in V_{th} [7], suggesting weak correlation between these vacancies and the threshold voltage.

12.2.2 Stability of F Ions in AlGaN/GaN Heterostructures

Unlike in Si or other compound semiconductors in which the F ions have shown rather poor thermal stability due to F's small atomic size and large space in the interstitial regions of these materials [8, 9], much better thermal and electrical stabilities have been reported for F ions in AlGaN/GaN heterostructures [7, 10]. The F ions' stability is revealed by the potential energy profiles of F ions in AlGaN/GaN,

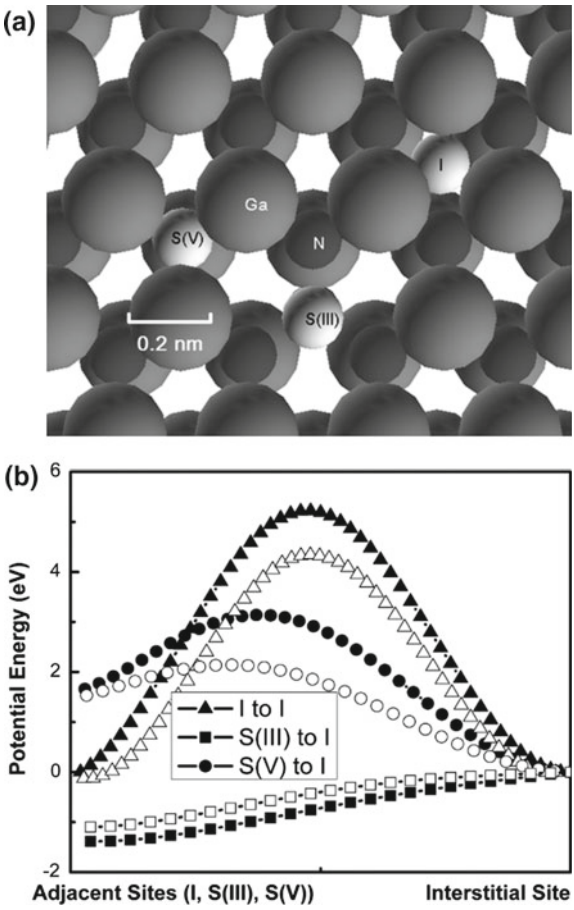

Fig. 12.6 **a** Top view of (0001) GaN with three possible sites that can accommodate fluorine ions. **b** The potential energy profiles from I, S(III) and S(V) sites to their nearest I site of fluorine ion in $Al_{0.25}Ga_{0.75}N$ (*open symbols*) and GaN (*solid symbols*). The $Al_{0.25}Ga_{0.75}N$ is strained and lattice matched to GaN

also calculated by MD simulation [11]. The three locally stable sites that can physically accommodate fluorine ions are (Fig. 12.6a): interstitial site I, substitutional group-III cation site S(III), and substitutional group-V anion site S(V). Since majority (>90 %) of the implanted F ions are initially located at the I sites after implantation, the potential energy profiles between an I site and these three possible nearby sites along the minimum energy path are calculated and shown in Fig. 12.6b.

Several conclusions can be drawn from Fig. 12.6 as follows:

- Interstitial F ions will be stabilized at the I site unless there is an S(III) site nearby.
- An F ion exhibits higher potential energy at the S(V) site compared to an I site since the Ga atoms around an N vacancy provide strong repulsive force to F ions and also help prevent interstitial F ions from moving into N vacancies.
- Around a Ga vacancy, the N atoms are smaller and the repulsive force to an F ion is significantly weaker. Thus, it is easier for an interstitial fluorine ion to move into a nearby Ga vacancy when available.

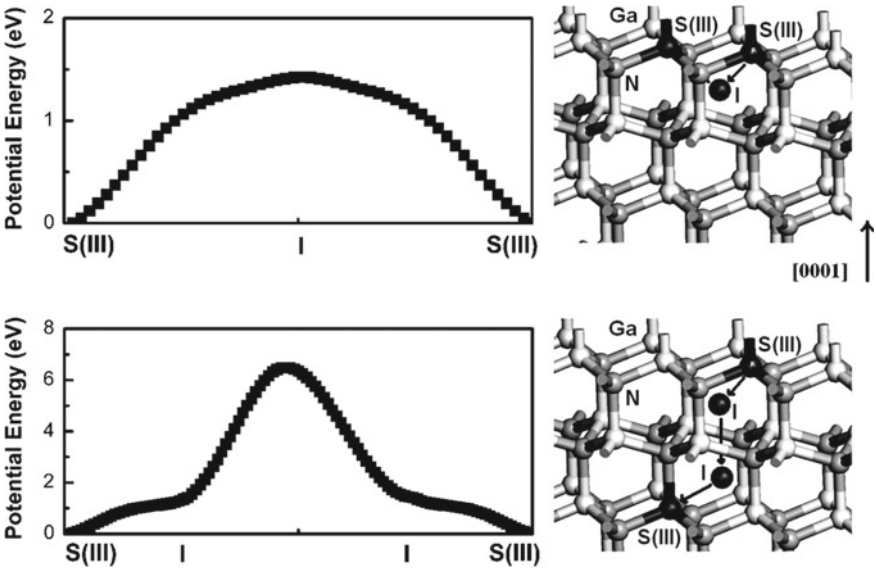

Fig. 12.7 Potential energy profiles through S(III)-I-S(III) and S(III)-I-I-S(III) paths. The movement paths are shown on the *right*. The *black*, *dark gray*, and *light gray balls* are F sites, N atoms, and Ga atoms, respectively

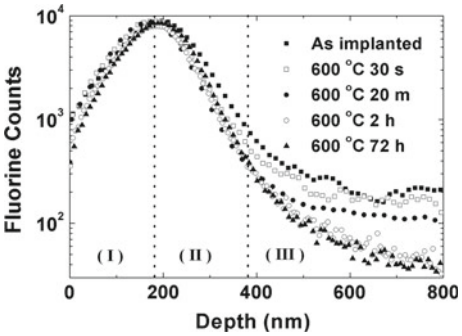

Fig. 12.8 Depth profiles of fluorine after post-implantation annealing at 600 °C. This experiment was conducted on a sample implanted by 180 keV F ions with a dose of $1 \times 10^{15}/cm^2$, so that the peak F concentration is deep inside the bulk

When there are no continuous S(III) vacancy chains, the F ions will be trapped at the S(III) sits, as depicted in Fig. 12.7. The thermal stability of F ions in GaN is highlighted in Fig. 12.8 and the F–Ga vacancy interactions are revealed by positron annihilation spectroscopy experiment, as shown in Fig. 12.9 [12].

Excellent thermal stability has been reported in F-implanted normally off GaN HEMTs as long as the ambient temperature does not exceed the limit of the gate

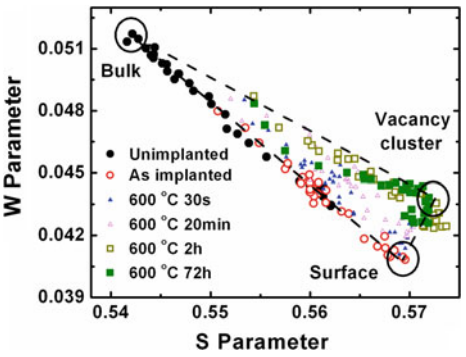

Fig. 12.9 S-E curve of the fluorine-implanted samples after annealing in N_2 atmosphere at 600 °C from 30 s to 72 h

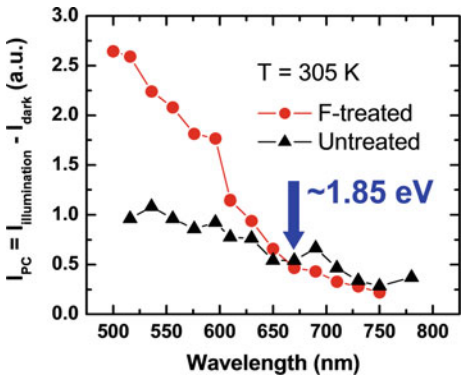

Fig. 12.10 Photoconductive current between two ohmic contacts made to 2DEG, measured in two samples with and without F-implant

metal (e.g., 500 °C for Ni) [7] or gate dielectric (>800 °C for SiN_x). The stability of the gate metal or gate dielectric is critical since it provides the cover that prevents F ions from escaping through the surface under high-temperature thermal excitation. It is observed that F ions can be stable under high electric field stress as long as large number of defects and dislocations are not introduced, e.g., by the inverse piezoelectric effect.

12.2.3 Electron Binding Energy Around F Ions

To study the binding energy of electrons associated with F ions, photoconductivity measurements were conducted using a Xe lamp together with a monochromator. The photocurrents as a function of the excitation wavelength are plotted in Fig. 12.10. The photocurrent increases slowly as the wavelength decreases (photon energy increases) from 750 nm in both the F-implanted and unimplanted samples. As the wavelength falls below 670 nm (corresponding to a 1.85 eV photon energy), the F-implanted sample starts to exhibit a much higher increasing rate compared to the

unimplanted sample, indicating activation of electrons from certain deep levels. Thus, the electron binding energy associated with the F ions in AlGaN/GaN is ~1.85 eV [13].

12.3 Fluorine-Implanted Enhancement-Mode GaN MIS-HEMTs

12.3.1 GaN MIS-HEMTs

Many of the early normally off GaN FETs are HEMT devices with Schottky gate, which has relatively small threshold voltage (<1 V) and small gate swing that is limited by the Schottky-gate forward turn-on voltage (e.g., <3 V). In power-switching applications, large positive threshold voltage (e.g., >3 V) and large gate swing (e.g., >10 V) are required to prevent the power switches from faulty turn-on by electromagnetic interference and to become compatible with the gate drive designs currently used for Si-based power transistors. MIS-HEMT (metal–insulator–semiconductor HEMT) with a gate dielectric inserted between the gate metal and group-III-nitride surface provides the capability of scaling up the threshold voltage and gate swing. Various dielectric materials (e.g., Al_2O_3, SiO_2, and SiN_x) have been employed to convert Schottky gate to MIS gate [14, 15]. A few reports have shown GaN E-mode devices with large gate swings [16]. Meanwhile, low current collapse, or low dynamic on-resistance (R_{on}), is another indispensable requirement for achieving high-efficiency power conversion under high-voltage switching conditions, whereas effective device passivation still demands more effort [17].

Device Structure and Fabrication

The studied sample features a 21-nm barrier layer (with 2-nm GaN cap, 18 nm $Al_{0.25}Ga_{0.75}N$, and 1 nm AlN) and a 4-μm GaN buffer/transition layer, grown on a 4-inch p-type (111) Si substrate. The schematic cross section of a fabricated E-mode MIS-HEMT is shown in Fig. 12.11. An AlN/SiN_x passivation stack structure was deposited with plasma-enhanced atomic layer deposition (PE-ALD) of 4 nm AlN and plasma-enhanced chemical vapor deposition (PECVD) of 50 nm SiN_x in sequence [18]. Planar device electrical isolation was realized by standard fluorine ion implantation. The gate window was opened with low-power dry etching of the passivation stack. The gate region was then subjected to CF_4 plasma at an RF power of 200 W for 250 s with photoresist as the plasma implantation mask. After removing photoresist and carrying out an *ex situ* surface cleaning process with remote NH_3/Ar/N_2 plasma at 300 °C in the PE-ALD system to effectively remove the detrimental Ga–O bonds at the surface [19], the second SiN_x thin film of 17 nm thickness was immediately grown by PECVD and deployed as the gate insulator to reduce gate leakage. Gate electrode with 1-μm footprint and 0.5-μm overhang was formed with Ni/Au deposited upon the second SiN_x.

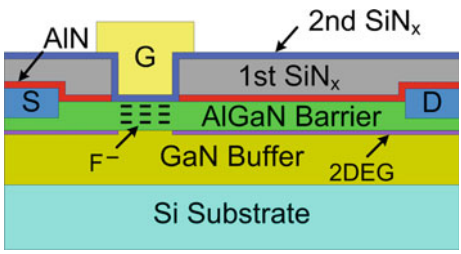

Fig. 12.11 Schematic cross section of a fabricated E-mode MIS-HEMT

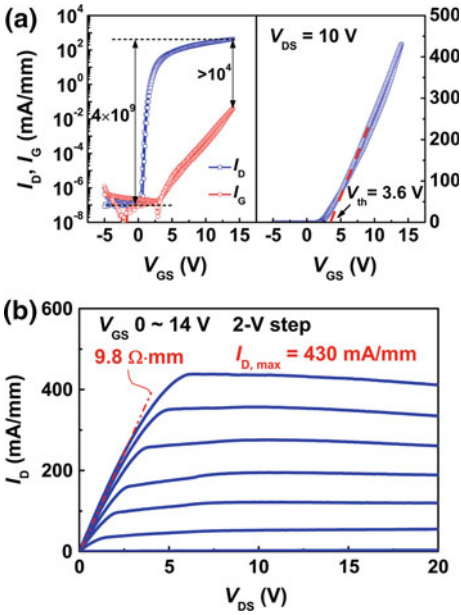

Fig. 12.12 **a** DC I_D–V_{GS} and I_G–V_{GS} characteristics measured with gate bias positive/negative sweeping at a drain bias of 10 V. **b** DC I_D–V_{DS}

Measurement Results and Analysis

Device characterization was carried out on devices with $L_{GS} = 1$ μm, $(W/L)_G = 10$ μm/1 μm, and $L_{GD} = 15$ μm (unless otherwise specified). Figure 12.12 shows typical DC transfer and output characteristics of an MIS-HEMT. The threshold voltage Vth, determined by the linear extrapolation method (i.e., the gate bias intercept of the linear extrapolation of drain current at the point of peak transconductance), is extracted to be +3.6 and +1.2 V for the MIS-HEMTs and the Schottky-gate control HEMTs fabricated on the same wafer, respectively. The positive shift of V_{th} in the MIS-HEMT is primarily a result of the reduced gate-to-channel capacitance by the insertion of the SiN_x gate dielectric.

The trap density at SiN_x/barrier interface is estimated to be ~3×10^{12} cm^{-2} using a pulsed I_D–V_{GS} measurement [20]. The device exhibits an ON/OFF current ratio of 4×10^9 and a drive current of 430 mA/mm. The gate leakage is effectively suppressed

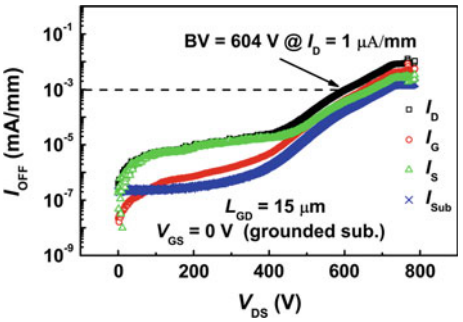

Fig. 12.13 Off-state breakdown/leakage characteristics with $V_{GS} = 0$ V and the substrate connected to the ground. A breakdown voltage of 604 V is achieved at a drain leakage current of 1 μA/mm

by the SiN_x at positive gate bias, enabling a large gate swing of 14 V and a low R_{on} of 9.8 Ω mm. The DC-specific R_{on} is calculated to be 2.1 mΩ cm^2, taking into account a 1.5 μm transfer length for each ohmic contact (i.e., source and drain) in active area calculation.

The off-state breakdown/leakage characteristics of an MIS-HEMT are shown in Fig. 12.13. Gate and source electrodes are biased at 0 V and the substrate is grounded. It can be observed that the leakage current is mainly originated from the source injection current at a drain bias V_{DS} up to 450 V, when the off-state gate leakage has been substantially suppressed by the gate insulator SiN_x. When V_{DS} continues to increase, the gate leakage and vertical substrate leakage will both increase to be comparable to the source injection current as V_{DS} approaches 600 V. The breakdown voltage (BV), defined as the drain bias at a drain leakage current of 1 μA/mm, is measured to be 604 V.

Current collapse evaluation is performed using AMCAD-pulsed *I–V* measurement system. Figure 12.14a shows the pulsed I_D–V_{DS} characteristics of a normally off device with $L_{GS} = 1$ μm, $(W/L)_G = 2 \times 50$ μm/1 μm, and $L_{GD} = 10$ μm. The quiescent bias point is set at $(V_{GSQ}, V_{DSQ}) = (0\text{ V}, 60\text{ V})$. The pulse width and pulse period are 500 ns and 1 ms, respectively. The DC output curves are plotted for reference. Effective suppression of current collapse by AlN/SiN_x passivation is demonstrated with little difference between the DC and pulsed drain current in the linear region. The elimination of self-heating effect is believed to be the reason for the higher drain current obtained in the pulsed *I–V* measurement. For high-voltage switching measurement, a slow-switching on-wafer testing was conducted using Agilent B1505A power device analyzer/curve tracer. After a high drain bias stress in the off-state with $V_{GS} = 0$ V, the device is turned on when the dynamic R_{on} is measured at $V_{GS} = 12$ V and $V_{DS} = 1.5$ V with a transient on-state current of ~ 100 mA/mm, as shown in Fig. 12.14b. The off-to-on switching time is 0.1 s when the drain stress voltage V_{DS} is lower than 200 V and 2.7 s when V_{DS} is higher than 200 V. The device has slight dynamic R_{on} degradation of only 76 % for an off-state drain bias stress of 650 V.

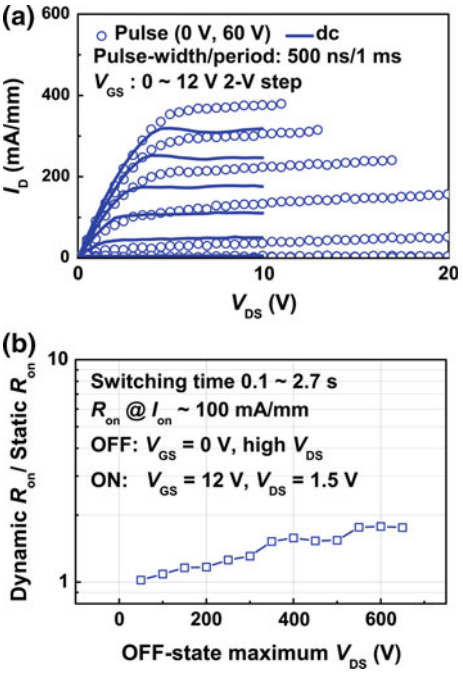

Fig. 12.14 **a** Pulsed I_D–V_{DS} characteristics of an E-mode MIS-HEMT with $L_{GS} = 1$ μm, $(W/L)_G = 2 \times 50$ μm/1 μm, and $L_{GD} = 10$ μm. **b** Ratio of dynamic R_{on} and DC static R_{on} obtained by low-speed high-voltage switching measurement. The device is with $L_{GD} = 15$ μm, $(W/L)_G = 10$ μm/1 μm, and $L_{GD} = 15$ μm

12.3.2 GaN MIS-HEMTs with Partially Recessed Fluorine-Implanted Barrier

For the GaN transistors with metal–insulator–semiconductor (MIS) structure, their high-temperature stability can be hindered by the challenges of V_{th} instability originating from the thermal electron emission of trap states at the dielectric/III-N interface [21, 22]. To address this issue, a thinned barrier layer is proposed to bring the deep interface traps below the Fermi level at pinch-off so that they become inactive [22]. In this work, the normally off MIS-HEMTs featuring a partially recessed (Al)GaN barrier were realized by a fluorine plasma implantation/etch technique. The partially recessed barrier leads to improved thermal stability, while the fluorine implantation can convert the device from D-mode to E-mode without completely removing the barrier and sacrificing the high mobility heterojunction channel [1].

Device Fabrication

The schematic cross section of the normally off MIS-HEMT is shown in Fig. 12.15. Both the fluorine ion implantation and gate recess were carried out using CF_4 plasma [23]. By properly adjusting the power level of the RF source driving the fluorine plasma, we are able to obtain two desirable results: (1) a well-controlled slow dry etching for gate recess; and (2) effective shallow implantation of fluorine ions into the AlGaN barrier. Fluorine plasma implantation at a higher RF power level of 200 W

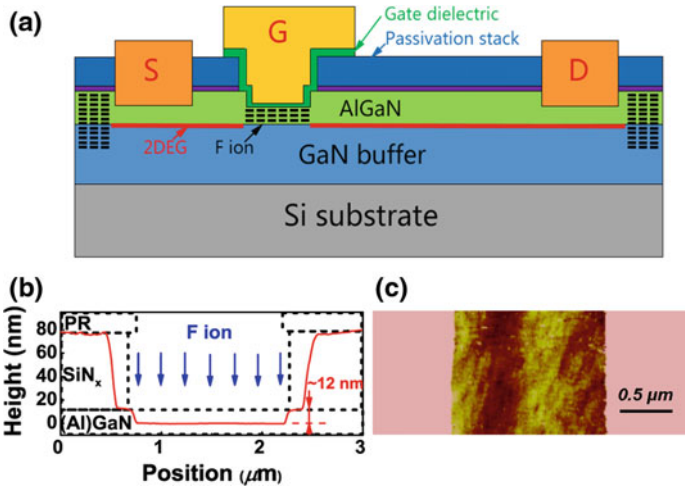

Fig. 12.15 **a** Cross section of a fabricated E-mode MIS-HEMT. **b** Side wall profile of the gate region after F-implantation (*solid line in red*) and the outline of gate region before F-implantation. **c** Surface morphology of the recessed gate region

resulted in a well-controlled slow-etching process with an etching rate of 2 nm/min. Meanwhile, a lower RF power of 150 W only induced insignificant etching of the barrier layer [1]. After 6 min of F-implantation/etch, a recess depth of ~12 nm and a smooth etched surface were obtained. After removing another 2 nm AlGaN by a digital etching [24], 20 nm Al_2O_3 was deposited by ALD with an *in situ* nitridation process [19].

Results and Discussion

The partially recessed F-implanted E-mode MIS-HEMT exhibits a threshold voltage (V_{th}) of +0.6 V at a drain current of 10 μA/mm, a maximum drive current of 730 mA/mm, an on-resistance of 7.07 Ω mm (Fig. 12.16), and a hysteresis of ~ 0.3 V between the up- and down-V_{GS}-sweep with a relatively fast sweeping rate (0.7 V/s).

The temperature (T)-dependent transfer and output characteristics of an MIS-HEMT were characterized (Fig. 12.17). When temperature increases from 25 to 200 °C, an increase in 3 orders of magnitude is observed in the OFF-state drain leakage due to increased buffer leakage, while the drain current exhibits an decrease (e.g., from 240 mA/mm to 200 mA/mm at $V_{GS} = 4$ V). By using a current criteria of I_{DS} of 10 μA/mm, V_{th} shifted by 0.5 V toward negative direction when T increased from 25 to 200 °C.

According to a recent report [22], the thermally stable V_{th} of MIS-HEMTs with recessed gate is mainly attributed to the thin barrier thickness (Fig. 12.18a). As shown in figure inset, the V_{th} shift with temperature increasing from 25 to 200 °C depends on the barrier layer thickness (t_{BR}). As t_{BR} is reduced, the thermally induced V_{th} shift can be significantly suppressed. The recessed barrier buries the deep interface traps

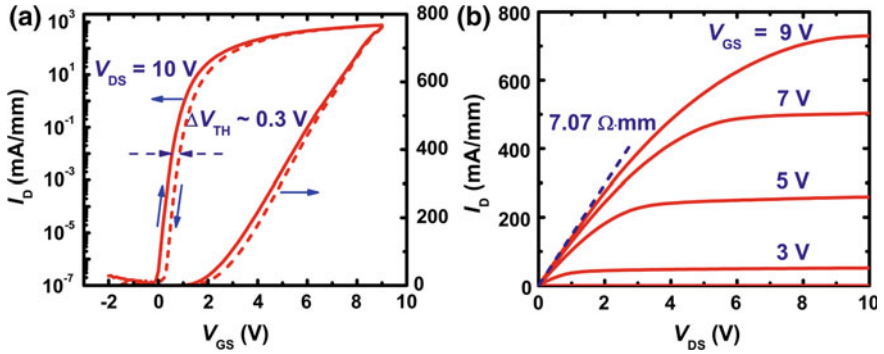

Fig. 12.16 (a) Transfer and (b) output characteristics of a MIS-HEMT with L_G = 1.5 μm and L_{GD} = 10 μm

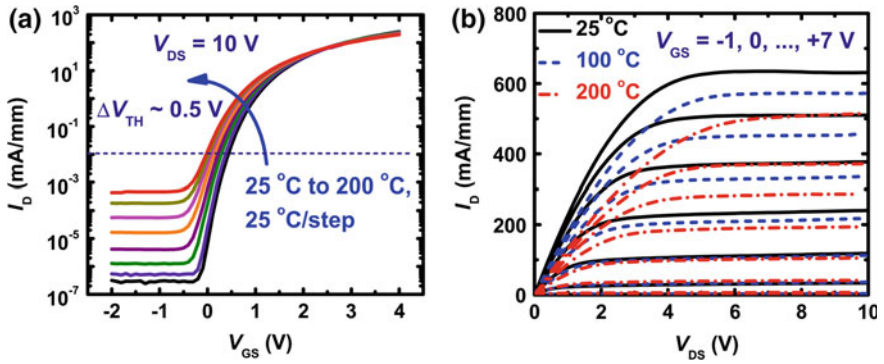

Fig. 12.17 Temperature (*T*)-dependent **a** transfer and **b** output characteristics of a MIS-HEMT with L_G = 1 μm and L_{GD} = 2 μm at *T* increasing from 25 to 200 °C

below the Fermi level at pinch-off (i.e., $\Delta E_3 < \Delta E_2 < \Delta E_1$) so that they become inactive and do not participate in the thermally sensitive emission (Fig. 12.18b). Stable charge states of the interface traps would lead to more stable V_{th}.

12.3.3 GaN Smart Power ICs

Although the current focus of GaN power device technologies is on discrete power devices, higher level integration of GaN power electronics could lead to many application-relevant benefits including reduced cost and improved reliability. In a more complete power converter module, besides the core power components (i.e., switches and rectifiers), intelligent control units are also needed to achieve precise

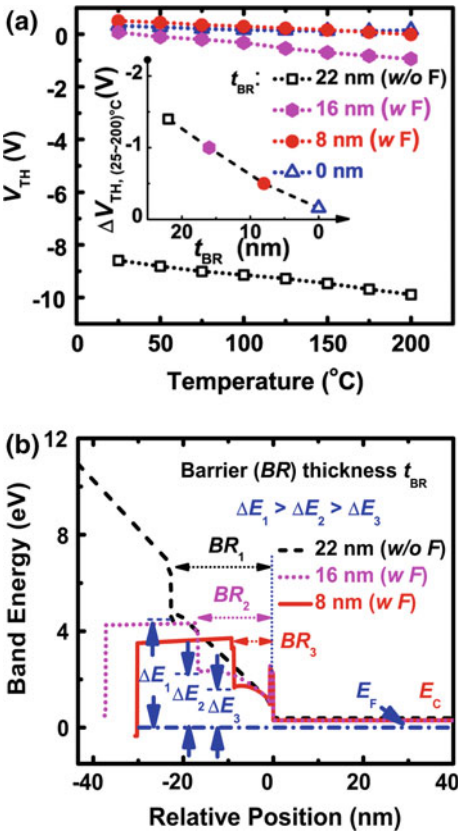

Fig. 12.18 **a** *T*-dependence of threshold voltage of GaN MIS-HEMTs with various barrier thicknesses and with/without fluorine (F) implantation. **b** Simulated band diagram of MIS-HEMT structure in this work (*red*) at pinch-off situation, compared with MIS-HEMTs with thicker barrier layer. The band diagrams are simulated using a 1D Poisson/Schrödinger equation solver. A uniform fluorine concentration (yielding a sheet density of $1 \times 10^{13}/cm^2$) in the AlGaN barrier was used in the simulation for the purpose of simple illustration

adjustment of the output signal under different loading conditions, as shown in Fig. 12.19. Ultimately, robust sensing and protection units should be integrated to realize full-range protections against extreme operating conditions such as over-temperature, over-current, and over-voltage. It is thus desirable to develop highly integrated GaN power electronics technology with which we can implement on-chip power conditioning/protection circuits that promise to provide optimized performance, increased functionality, and enhanced reliability.

Platforms for Heterogeneous Integration

A smart power IC technology requires a platform on which both high-voltage components and low-voltage periphery devices can be integrated (Fig. 12.20) [25, 26]. The high-voltage switches prefer normally off transistors for their inherent fail-safe operation. For digital IC development, the mainstream CMOS-like architecture may have intrinsic difficulties in GaN materials due to the inferior hole mobility. The analog IC development using AlGaN/GaN has started recently.

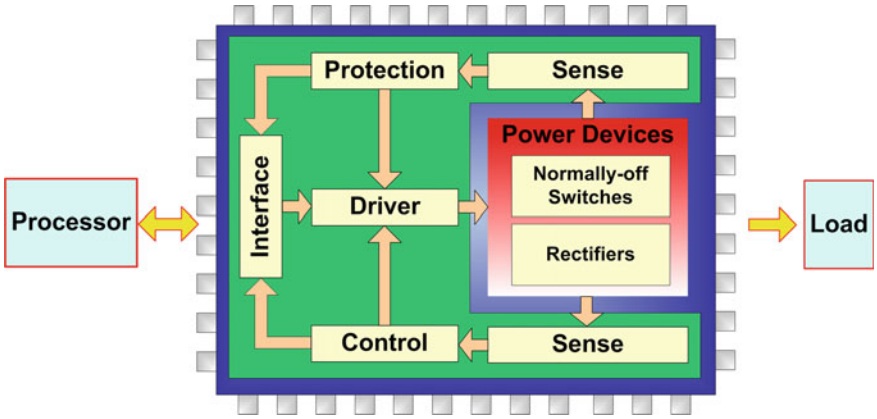

Fig. 12.19 Functional block diagram of a power converter module

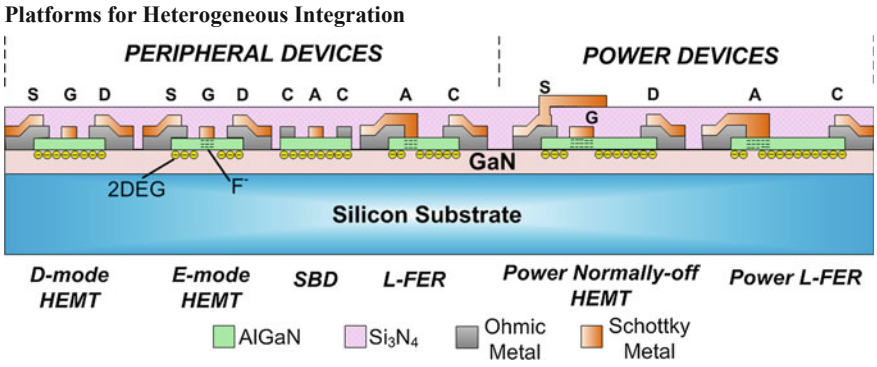

Fig. 12.20 Schematic platform of GaN smart power technology: integration of low-voltage peripheral and high-voltage power devices

Based on the robust fluorine plasma ion implantation technique, several key smart power components including high-voltage normally off transistors and lateral field-effect rectifiers [27, 28] have been developed. A smart power chip technology also requires low-voltage peripheral devices for the implementation of digital and analog blocks. Due to the lack of high-performance p-channel GaN devices, the simplest circuit configuration for GaN digital circuits is the direct-coupled FET logic (DCFL) that requires both the E-mode and D-mode n-channel HEMTs [29]. The Schottky diodes and L-FERs all exhibits graceful temperature dependences that can be explored for temperature sensing and compensation.

Lateral Field-Effect Rectifier (L-FER)

Analog circuits typically require diodes in additional to transistors. With the III-N heterostructures, diodes can be realized with three approaches including the lateral

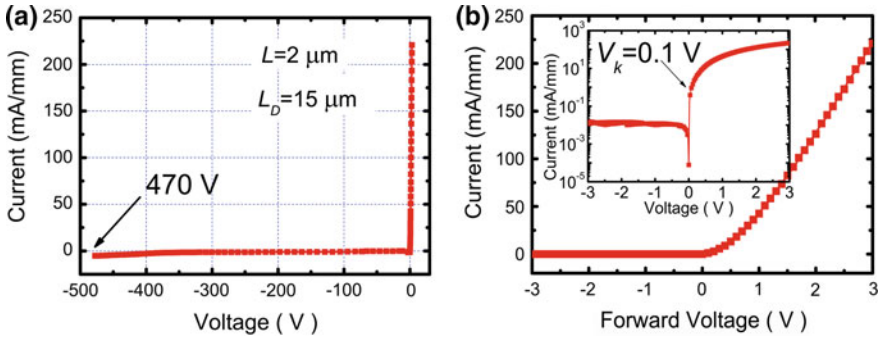

Fig. 12.21 Measured DC performances of L-FERs: **a** reverse bias, **b** forward bias

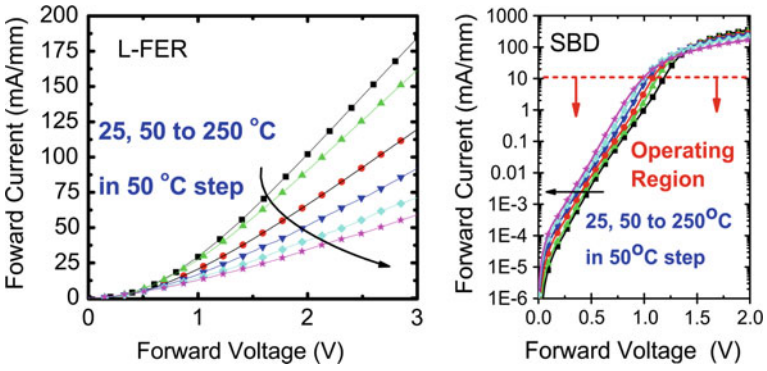

Fig. 12.22 Forward *I–V* characteristic of L-FER and SBD at varied operating temperatures

field-effect rectifier (L-FER) [27], the simple Schottky barrier diode (SBD) on heterostructures, or the lateral SBD with the Schottky junction to the 2DEG channel made from the sideway [30]. The forward and reverse characteristics of an L-FER with the anode–cathode drift region length L_D of 10 μm are plotted in Fig. 12.21. The knee voltage V_k, defined as the anode bias at a forward current of 1 mA/mm, is 0.1 V in the proposed L-FER. Figure 12.22 shows the forward *I–V* curves of L-FER and SBD at varied operating temperature. It is seen that the current of L-FER exhibits a negative temperature coefficient because its conduction current is dominated by phonon scattering. For the SBD directly fabricated on the heterostructure, the thermionic emission dominates the forward current at forward bias smaller than 1 V, and thus, its forward current has a positive temperature coefficient.

GaN Mixed-Signal ICs Based on Monolithic Integration of E/D-Mode HEMTs
Based on the fluorine implantation technique, monolithic integration of E/D-mode HEMTs has been demonstrated [29]. A 17-stage ring oscillator has been shown to operate properly, even at 375 °C [31]. Various mixed-signal GaN ICs have been

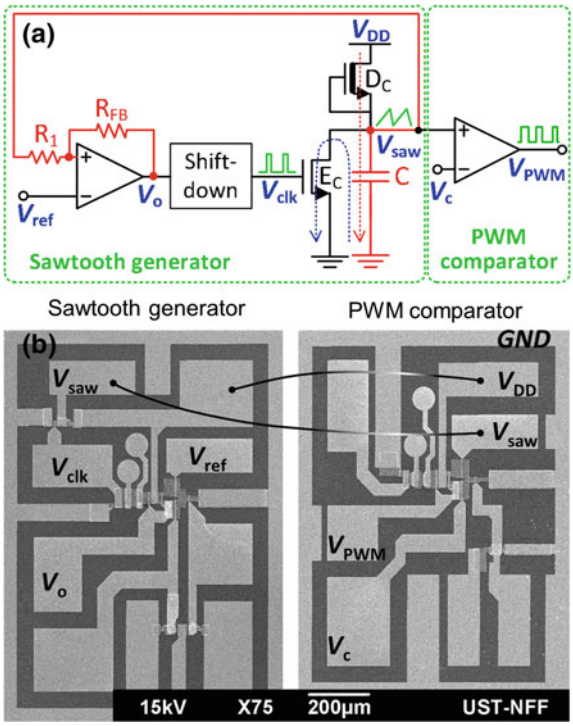

Fig. 12.23 **a** Block diagram of the GaN-based PWM IC. Three off-chip passive components are used (*marked in red line*) for the sawtooth generator. V_c is the reference voltage sampled from the converter output. **b** Scanning electron microscope (SEM) picture of the adjacent dies (*left* sawtooth generator; *right* PWM comparator). The GaN-on-Si chip is wire-bonded and mounted onto a PCB which also houses three off-chip passive components

demonstrated including a voltage reference [32], a bootstrapped comparator [33], a 2-bit quantizer and flip-flop [34], a temperature sensor [35], and a self-startup circuit [36].

The first GaN-based PWM circuit using monolithically integrated E/D-mode HEMTs and L-FERs [37] is illustrated in Fig. 12.23. The circuit is able to generate 1 MHz PWM signal with its duty cycle modulated linearly over a wide range.

The GaN-based pulse width modulator incorporates two functional blocks, i.e., a sawtooth generator and a comparator. The sawtooth generator produces a sawtooth signal (V_{saw}) and the comparator (referred to as the PWM comparator) produces the PWM signal (V_{PWM}) by comparing the reference voltage (V_c) sampled from the converter output against the sawtooth signal (V_{saw}). The pulse width of V_{PWM} is modulated by V_c, and its frequency is determined by that of V_{saw}. Circuit performances up to 1 MHz are investigated with a 5 V supply voltage. The generated sawtooth signal (V_{saw}) is injected into the PWM comparator and compared against V_c, yielding a PWM signal with its duty cycle modulated by V_c. Figure 12.24 shows the PWM waveforms when the circuit is operated at ~1.08 MHz. The pulse width of the PWM signal can be modulated over a wide range (by varying V_c from 1.3 to 2.0 V with V_{saw} oscillating between 0.89 and 2.18 V).

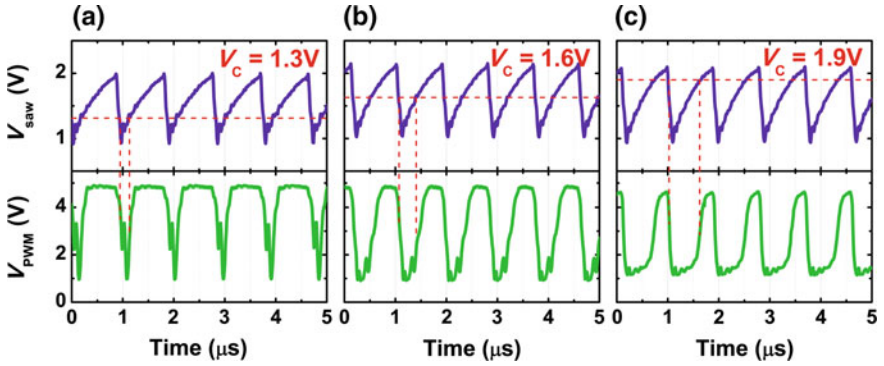

Fig. 12.24 Waveforms of GaN PWM circuit, V_{DD} = 5 V, I_{DD} = 5 mA. V_c (*red dash*) cuts V_{saw} (f = 1.08 MHz, V_{saw} = 0.89–2.18 V) and determines the duty cycle of V_{PWM}. **a** V_c = 1.3 V, **b** V_c = 1.6 V, **c** V_c = 1.9 V

12.4 Conclusions

Fluorine implantation, in particular the low-energy implantation using plasma tools, is shown to be able to locally incorporate negatively charged F ions into AlGaN/GaN heterojunctions. These negative fixed charges provide robust and flexible means of adjusting the threshold voltage in the 2DEG channel, enabling the realization of E-mode GaN HEMT and MIS-HEMTs on D-mode HEMT platform. Atomistic modeling based on molecular dynamics simulation reveals that F ions can be reasonably implanted into AlGaN/GaN heterojunctions assisted by the channeling effect of the (0001) C-plane AlGaN/GaN, but can be stably confined within the crystal because of the tight lattice structure of GaN and related compounds. The fluorine implantation technique offers robustness and flexibility in delivering GaN power components (transistors and rectifiers) and peripheral mixed-signal functional blocks on the same technology platform for the ultimate GaN system-on-a-chip solutions for various applications smart power amplifiers and smart power converters.

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