

# A Method of Reducing Output Waveform Distortion in Photovoltaic Converter System

Huixiang Xu and Nianqiang Li<sup>(✉)</sup>

School of Information Science and Engineering,  
University of Jinan, Jinan 250022, China  
jd\_chuying1990@163.com

**Abstract.** For the problem of leak inductance energy and voltage spike, given in the fly-back photovoltaic converter system (hereinafter abbreviated as PV), a new physical circuit of RCD (resistor-capacitor-diode) is proposed which based on the Boost circuit topology to recovering leak inductance energy and depressing main switch voltage spike during the commutation of power MOSFET. The circuit can recycle the leak inductance energy effectively [1–2], and suppress output capacitance (hereinafter abbreviated as Coss) electric discharge which caused the voltage spike during MOSFET switch-on. In addition, after detailed analysis, the new physical circuit can solve the problem of the energy loss generate from the Coss electric discharge which is not pay more attention by the other papers. The new design can clamp the drain-source voltage and implement the control policy of soft-switch. In this paper, we give the theoretical derivation of the circuit parameter and the implemented physically experimental curve of the physical circuit by analyzing the causes of voltage spike generated. Compared with the traditional method, improved the converter efficiency from 94.2 % to 96.2 %, and the MPPT efficiency to 99.4 %.

**Keywords:** Leak inductance energy recovery · Voltage spike depress · Coss capacity discharge · Soft-switch · RCD · Boost topology · Converter

## 1 Introduction

The PV converter is a controller that input DC and output AC, which include two ways to implement it, converter-booster (firstly, inverse the DC to AC, then boost the voltage up to 230 V) and booster-converter (firstly, boost the DC voltage up to 230 V, then inverse the DC to AC). The former need using large transformer, so it's more used in high power inverter design. Traditional design prefer to use converter-booster to conversion the voltage, because of its directness. However, in order to protect the electronic component from being damaged, the cost of this method is very high. For the distributed converter with high frequency and miniature, its more prefer to used the method of booster-converter [3], which is cheaper than traditional method. The fly-back is the main transformer in the secondary side which include the half-wave diode rectifier to output the half-wave with the 100 Hz frequency and 330 V peak value, then conversion 50 Hz sine wave through the H-bridge converter circuit.

Experiments show that, during an DC-AC conversion, producing a good or bad half wave is the key to affect the wave shape and the conversion efficiency. In addition the quality of half wave affected by the leak inductance energy and the power MOSFET parasitic capacitor discharge more seriously. if its magnitude is excessive, the problem will cause the voltage spike, energy loss and the converter efficiency greatly reduced [4]. For this problem, designer usual use the circuit of leak inductance energy recovery based on the Buck topology to absorb the leak inductance energy, just like mentioned in the Ref. [2]. But if the leak inductance energy is too much or unstable, the output voltage of buck circuit will be influenced seriously. Moreover, in the circuit, the traditional method do not consideration the effect of capacitor electric discharge, and no theory analysis about the circuit parameter selection. In this paper, the control policy of MOSFET used the sinusoidal pulse width modulation (hereinafter abbreviated as SPWM) to achieve zero voltage switching (ZVS) [5]. The new design has improved the ability of physical circuit energy absorption, and clamped the drain-source voltage. In addition, inversion curve and converter efficiency curve are measured by circuit parameter selection with theory analysis.

## 2 The Cause of the Fly-Back Leak Inductance and Voltage Spike

Compare to the traditional one converter power system for multiple PV modules, the fly-back converter suitable for medium and small power transformation, can be used to one converter and one PV modules connected. It is more easily to work in the Maximum Power Point Tracking (MPPT) [2, 6, 7]. The working principle of the fly-back transformer is that the secondary coil do not output power to the load, until the primary coil incentive cut off. Because of the fly-back have an air gap when its designed, so the original boundary energy can not be 100 % transformation to the secondary side, thus cause the leak inductance. The existence of leak inductance will necessarily produces energy loss, and may cause counter assault if its magnitude is excessive [8–10]. The output power can not meet the requirements if too much leak inductance energy retention during input. Reflected in the waveform has been shown in Fig. 1. The energy loss are generated during each half wave connect. Besides, the leak inductance not only affect the power conversion efficiency, also can cause the voltage spikes of the power switches in turn off instant [11].

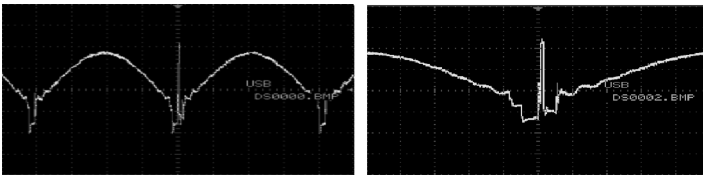


Fig. 1. Leak inductance energy loss

When the grid-source electrode of the power MOSFET be shorted, the capacitance value during the drain-source electrode is called  $C_{oss}$  output capacitance. The principle diagram of the MOSFET has been shown in Fig. 2.

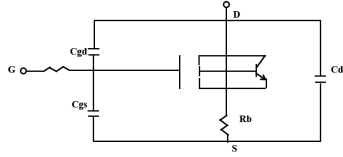


Fig. 2. Principle diagram of MOSFET with the parasitic capacitance

Let  $C_{gd}$  means the terminal capacity between Gate (G) and Drain (D), and  $C_{ds}$  means the terminal capacity between Drain and Source (S).  $C_{gd}$  added  $C_{ds}$  is equal to  $C_{oss}$ . The  $C_{oss}$  capacitor charged when the power tube turn off, during this time, most of the electricity flowing through the MOSFET, and relative small current through the  $C_{oss}$  capacitor. Therefore, the voltage between drain and source maintain in a low voltage value. Before the gate-source voltage value (VGS) from zero to gate threshold voltage value ( $V_{TH}$ ), the MOSFET do not load inductance current. The  $C_{oss}$  capacitor will discharge after the VGS value reaching the power MOSFET switch-on voltage value [12–14]. If the system is not set reasonable discharged circuit, the voltage of  $C_{oss}$  capacitor will be added to D-S side. That cause the high voltage spike, especially in the converter design. The fly-back rectifying half wave waveform with approximately 70 V voltage spike has been show in Fig. 3. From the theoretical analysis, the voltage spike are generated by the leak inductance retention and the parasitic capacitor discharged. If these condition are not suppressed effectively, it will produce a high current stress during the commutation of the power, even breakdown the MOSFET. In addition, because of its instability, PWM controller and zero synchronous detection measurement will be disturbed, which can lead to reducing the converter efficiency.

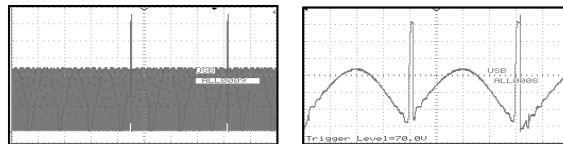


Fig. 3. Half wave with voltage spike(10 V/lattice)

### 3 Analysis for the Improved Circuit

#### 3.1 The Working Principle of the Circuit

According to the principle of fly-back transformer and the generate cause of voltage spike, the energy stored in the transformer primary side during the power turn on, and output to the secondary side when the power turn off. For the issue, the circuit needs to

increase the discharge absorbing loop. For the problem of output voltage instability in buck circuit, utilize the parasitic capacitance of MOSFET and the parasitic inductance of fly-back transformer, we design the circuit of RCD which based on Boost circuit topology to recovering leak inductance energy and depressing main switch voltage spike during switch-on (the dotted line part of the Fig. 4). The new design removes the high frequency transformer and the MOSFET, which mentioned in ref. 2 to reduce the energy consumption. The main topology of half wave converter has been shown in Fig. 4.

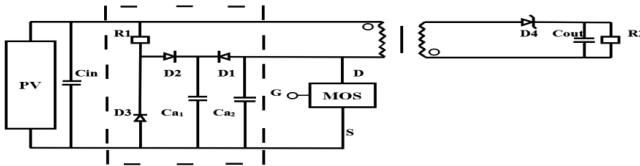


Fig. 4. Topology of half wave converter

When the MOSFET turns off, the leak inductance energy back to the clamp capacitance  $C_{a1}$  by rapid conduction diode  $D1$ , absorbing the excess energy. The clamp capacitance  $C_{a1}$  will suppress the  $C_{oss}$  capacitance discharge voltage, and depress the voltage spike when the MOSFET switch-on. After the MOSFET turn on, the  $D1$  cutoff and the absorbed energy recycle to the DC input side through resistance  $R1$ . The drain-source voltage of the main switch is clamped with  $D1$  and  $D2$  to prevent the voltage spike caused by  $C_{oss}$  capacitance. The  $C_{a2}$  protect the MOSFET, and participates in the implementation of soft-switch control policy.

### 3.2 The Circuit Parameter Design

For the RC parameters designed, if the resistance value is too small, before the power conduction, the capacitance value may drop to zero, then the reflect voltage energy will be consumed. If capacitance get a large value, the voltage of capacitance rise slowly and the absorbed energy can not pass to the secondary side quickly. If the capacitance value is excessive, the peak voltage will be less than the reflect value, which lead clamp resistance  $R1$  become a dead load to consumption magnetic core energy [15]. The ideal clamp circuit voltage waveform has been shown in Fig. 5.

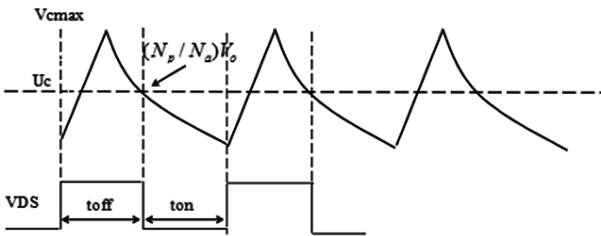


Fig. 5. The ideal clamp circuit voltage waveform

According to the geometrical relationship of clamp voltage wave and drain-source voltage of power MOSFET in Fig. 5, the following formula can be obtained.

$$\frac{\frac{N_p}{N_s} V_o}{V_{cmax}} = \frac{ton}{T} = D_{max} \quad (1)$$

$$V_{cmax} = \frac{N_p \bullet V_o}{N_s \bullet D_{max}} \quad (2)$$

To meet the capacitance value to  $\frac{N_p}{N_s} V_o$ , when the power conduction, need to

$$V_{cmax} \bullet e^{\frac{-(1-D_{max})T}{Rc}} = \frac{N_p}{N_s} \bullet V_o \quad (3)$$

Substitute Eqs. (2) to (3),

$$RC = (D_{max} - 1)T / \ln D_{max} \quad (4)$$

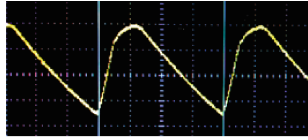
$$D_{max} = D = \frac{U_g}{N \bullet U_{pv} + U_g} \quad (5)$$

In the formula, the D means the duty cycle, the  $U_{pv}$  means the value of network voltage, the N means the ratio of turns and the T means the working frequency. According to calculation, when the working frequency is 10 KHZ, then  $R1 = 100 \text{ K}$ ,  $Ca = 3.3 \text{ nf}$ .

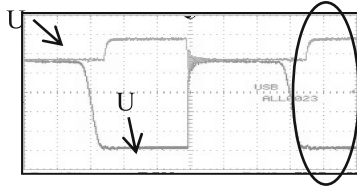
## 4 The Experimental Result of the Improved Circuit

In this paper, the converter rated capacity is 230 VA, with the input 30 V DC and output 220 V AC. The main power MOSFET was used IRF4321, in which the parasitic capacitance  $C_{oss} = 390\text{PF}$ , the primary induction  $5.4 \mu\text{H}$ , the leak inductance  $0.2 \eta\text{H}$ , and the ratio of turns is 1:6. The clamp capacitance  $Ca$  is 3.3 nF. The leak inductance recovery resistance  $R1$  is 100 K. The clamp diode used ES1D. The switch tube in secondary side was used 17N80, which include the commutation diode C2D05120.

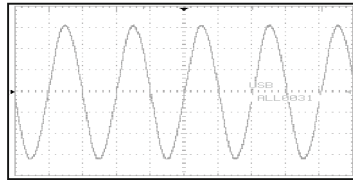
The experiments waveform have been shown in Fig. 6. The voltage waveform of clamp capacitance, which based on the theoretical derivation as shown in Fig. 6(a). The waveform close to the ideal curve. The voltage curve of the  $U_{gs}$  (the voltage between gate and source of MOSFET) and the  $U_{ds}$  (the voltage between drain and source of MOSFET) has been shown in Fig. 6(b). From the waveform we can see that the main switch achieve zero voltage switching (ZVS). As the Fig. 6(c) shown that the grid voltage waveform with the peak value is about 330 V, and very smooth. The experimental results show that, in this paper, the correctness of the theoretical analysis and the efficiency of the improved physical circuit.



(a) Voltage waveform of clamp capacitance( $t=5\text{ms}/\text{lattice}$ )



(b) The voltage of the drive of main switch and the drain-source



( $t=10\text{ms}/\text{lattice}$ , peak value= $100\text{V}/\text{lattice}$ )

(c) The converter AC output voltage

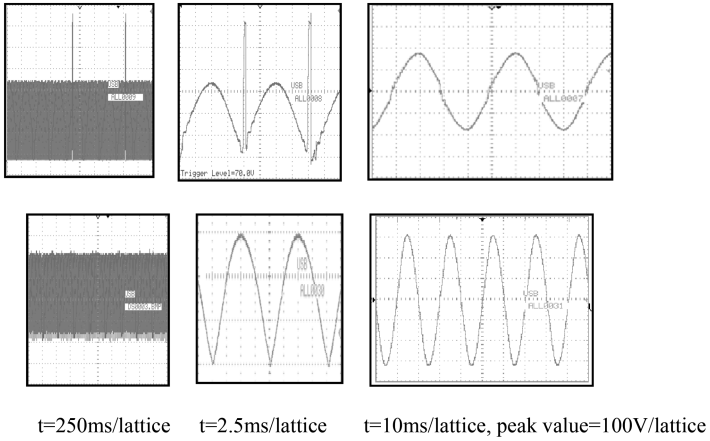
**Fig. 6.** Experiment waveform

## 5 Conclusions

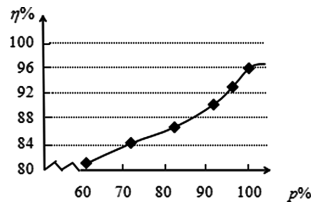
The comparison of the waveform before and after modification has been shown in Fig. 7. From the experiment waveform, we can find that the shake in half wave connection and the voltage spike which is generated by the  $C_{oss}$  electric discharge during the commutation of power MOSFET are absorbed and suppressed.

In this paper, the test curve of converter efficiency ( $\eta$ ) has been shown in Fig. 8, which the output converter efficiency can reach 96.2 %  $p$  is output power. The converter can achieve higher output efficiency in the whole load range. The efficiency of MPPT has been shown in Fig. 9, which can reach 99.4 % when full load. The results show that the new circuit which mentioned in this paper, can absorb and recycle the leak inductance energy, and suppress the voltage spike caused by the  $C_{oss}$ , and improve the converter efficiency.

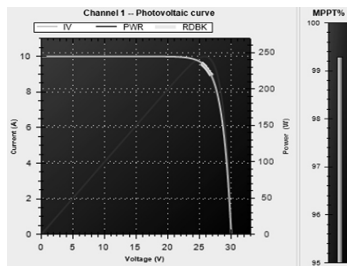
The Theoretical analysis and experimental results show that, the physical circuit which is proposed in this paper has the efficient, stable and reliable advantages to deal with the problem of leak inductance and the voltage spike. The new method solves the issues of leak inductance energy recovery and voltage spike phenomenon which caused by the leak inductance and the parasitic capacitance discharged during MOSFET switch-on. The design can protect the power switch by clamping the voltage spike



**Fig. 7.** The comparison of the waveform



**Fig. 8.** The efficiency test curve



**Fig. 9.** The MPPT test curve

value. In this paper, compare with the *ref.* 2, we improved the domestic converter efficiency from 94.2 % to 96.2 %, while the world’s highest converter efficiency up to 98 % [16].

**Acknowledgement.** The authors would like to express thanks for the helpful discussions with Dr Li, and the AMETEK Programmable Power company for providing relevant photovoltaic equipment. The author also thank Mr. Sun for providing some opinions about the photovoltaic converter system design. Authors would like to thank Han Yu of University of Jinan Computational Intelligence Lab for providing relevant information about this meeting announced.

## References

1. Cai, C., Qin, H.: A design of the snubber circuit for flyback converter. *Chin. J. Electron Devices* **04**, 469–472 (2013)
2. Gu, J., Wu, H., Chen, G., Xing, Y.: Soft-switching grid-connected PV inverter with interleaved flyback topology. *Proc. CSEE* **12**, 40–45 (2011)
3. Tseng, K.C., Liang, T.J.: Novel high-efficiency step-up converter. *Electr. Power Appl.* **2004** (03), 182–190 (2004)
4. da Rocha, J.F., dos Santos, M.B., Costa, J.M.D.: Voltage spikes in integrated CMOS buck DC-DC converters: analysis for resonant and hard switching topologies. *Procedia Technol.* **17**, 327–334 (2014)
5. Sicheng, W., Shijie, Y., Delin, W., et al.: Development of 3KW dispatchable grid connected inverter. *Acta Energiæ Solaris Sinica* **01**, 17–20 (2001)
6. Loukriz, A., Haddadi, M., Messalti, S.: Simulation and experimental design of a new advanced variable step size Incremental Conductance MPPT algorithm for PV systems. *ISA Trans.* **08**, 6–14 (2015)
7. Ma, Y., Guo, Q., Zhou, X.: A modified variable step size MPPT algorithm. *Microcomput. Appl.* **34**(17), 78–80,84 (2015)
8. Zhang, H., Zhao, Y.: Design of multifunctional flyback switching power supply. *Electr. Power Autom. Equipment* **01**, 113–117 (2011)
9. Lv, L., Xiao, J., Zhong, Z., Shi, Yu.: Design of single-ended flyback transformer in high-frequency switching power supply. *J. Magn. Mater. Devices* **01**, 36–38 (2006)
10. Zhu, S.: The research and design of grid-connected microinverter based on an interleaved flyback structure. School of Electrical Engineering Shenyang University of Technology (2013)
11. Liu, G., Dong, J.: Study of RCD clamp circuit in flyback converter. *Jiangsu Electr. Apparatus* **01**, 20–24 (2011)
12. Liu, J., Li, J., Cui, Y., Han, M.: Power MOSFET gate driver of the high frequency resonant inverter. *Trans. China Electrotechnical Soc.* **05**, 113–118 (2011)
13. Bo, W., Au, H., Ming, C., Yong, T.: Influence and suppression of voltage spike in turn-off transient of IGBT. *Mater. Device* **2011**(07), 501–504 (2011)
14. Dai, Y., Wang, G., Guan, Y., Wu, L., Li, X.: Degradation analysis of power MOSFET parasitic capacitance intransient response of switching. *Chin. J. Power Sources* **04**, 661–664 (2014)
15. Chen, X., Li, G., Liu, F.: Charging Efficiency Analysis for RC Circuit. *J. EEE* **02**, 32–35 (2012)
16. Jian, F., Li, Z.: Technology status and future development of PV inverter. *High Power Converter Technol.* **03**, 5–9 (2014)