Chapter 12
Damage Characterization for Electronic Components Under Impact Loading

Sangwook Sihn, Christie L.H. Devlin, Steven R. Dooley, Ajit K. Roy, and Eric R. Heller

Abstract A new experimental method has been develop to characterize critical interfacial damage parameters of solder interconnects subjected to high strain-rate mechanical loading, simulating shock or impact loading. A test apparatus and a test specimen were devised to experimentally characterize such critical damage parameters, particularly interfacial shear strength and fracture toughness. The test fixture was designed to easily mount and unmount test specimens, and accommodate various sizes of electronic components and solder layer thicknesses. Test specimens were fabricated with both metallic and polymeric solder materials, and tests were conducted under various shear load rates. It was found that both strength and fracture toughness exhibit significant rate-dependency.

12.1 Background and Introduction

Damage tolerance of electronic components subject to severe impact loading is of a great concern for reliable electronic operations. Under severe impact loading, the device can fail mechanically and electrically due to loss of adequate contact and bonding between the device package and the printed circuit board (PCB). One of standard methodologies for understanding structural responses and damage mechanisms of the electronic packages under the impact loading is the board-level drop test method proposed by Joint Electron Device Engineering Council (JEDEC) [1–3]. Numerous studies have conducted the board-level drop tests with various kinds of electronic components [4–6]. Among them, Kaplan et al. conducted experimental and computational investigation of dynamic response of PCB strain under the high-g shock impact loading [7]. In this study, a strain gauge was mounted on the PCB to monitor the dynamic strain response under ~15,700 g vertical acceleration, resulting in a maximum strain amplitude peak of near 6,300 μm. It was noted that the strain response of the PCB was sinusoidal with decaying amplitudes over time, which indicated that the major mode of the PCB deformation was longitudinal bending perpendicular to the plane of circuit board. Such strain responses were also reported by other experimental investigations [5, 8]. Due to the bending stiffness difference between the PCB and the electronic packages on it, tensile and shear stresses are built up at their interfaces during the PCB bending, causing interfacial cracks to open and slide, resulting in component failure. Therefore, solder joint reliability is closely related to the dynamic responses of PCB, and further the interfacial damage resistance between the PCB and the electronic components. Numerous experimental and computational studies regarding the impact damage indicate that interfacial normal and shear fractures near the PCB-package interfaces are the dominant damage mechanisms [6, 9–15]. Therefore, it is essential to characterize the interfacial damage resistance parameters to assess and predict the overall performance of such electronic components under impact loading.

S. Sihn (✉)
Materials and Manufacturing Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, Dayton, OH 45433, USA

Nonstructural Materials Division, University of Dayton Research Institute, 300 College Park, Dayton, OH 45469-0050, USA
e-mail: sangwook@alumni.stanford.edu

C.L.H. Devlin
Sensors Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, Dayton, OH 45433, USA

Wyle Laboratories, Dayton, OH, USA

S.R. Dooley
Sensors Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, Dayton, OH 45433, USA

A.K. Roy • E.R. Heller
Materials and Manufacturing Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, Dayton, OH 45433, USA

In the present study, we devised a new test apparatus and a test specimen to experimentally characterize the critical interfacial damage parameters of solder interconnects. The test apparatus was devised to experimentally characterize such critical damage parameters, particularly interfacial shear strength and fracture toughness. A measure of fracture toughness in terms of strain energy release rate was evaluated by means of a simplified shear test apparatus. The test apparatus was designed to easily mount and unmount test specimens, and accommodate various sizes of components and solder layer thicknesses. Test specimens were fabricated with both metallic and polymeric solder materials, and tests were conducted under various shear load rates. Rate dependency of the fracture toughness, strength and modes of the failed solder joints were also examined. Once measured, these parameters can be used for the computational simulations to predict the damage phenomena under high-g impact loading. We also developed FE models based on the cohesive zone model (CZM) to assess the feasibility of the present method.

12.2 Experimental Setup

The test specimen was fabricated with the PCB and an electronic component (die/chip) bonded to the top surface of the PCB with solder materials. The PCB is fabricated with FR-4 (woven glass-fiber epoxy composites). For feasibility study of the proposed test method and apparatus, a dummy chip was made of the same material as the PCB. Fig. 12.1 shows schematic top and side views of the test specimen and its dimensions. The PCB has two holes to be screwed to the back support grip of the test apparatus, as Fig. 12.2c shows. Length (L_B) and width (W_B) of the PCB are 25.4 mm (1.0 in.) by 12.7 mm (0.5 in.). Length (L_C) and width (W_C) of the dummy chip are 3.81 mm (0.15 in.) by 3.81 mm (0.15 in.). The thicknesses of the PCB (T_B) and the dummy chip (T_C) are approximately 1.6 mm (63 mil). Thin Cu pads, whose size dimensions are 2.54 mm (0.1 in.) by 2.54 mm (0.1 in.), and thickness is approximately 25 μm, are adhered to the PCB and the chip surfaces for better solder bonding. Exact dimensions of L_B, W_B, T_B, L_C, W_C, of each specimen were measured using a caliper before the tests. Furthermore, a total thickness (T_T) was measured from the top surface of the chip to the bottom surface of the PCB, as Fig. 12.1b shows. The thickness of the solder layer (T_S) was then calculated as $T_S \cong T_T - 2T_B$, where $T_C \cong T_B$.

The shear test apparatus was fabricated based on a design modeled with several iterations of numerical simulations using a commercial finite element (FE) software program ABAQUS. Fig. 12.2 shows schematic views of the shear test apparatus, which consists of a back-support grip (aluminum), a shear-tool grip (aluminum), and a pin plug (stainless steel). Holes in cylindrical portion of the back-support grip and the shear-tool grip are pinned to test load frame (MTS) grips, as shown in Fig. 12.3. While the back-support grip is fixed, the shear tool is horizontally displaced to apply the shear load to the die/PCB interface, and thus to induce pure interfacial shear failure. To prevent undesirable bending of PCB during the shear loading, the PCB is mounted and screwed to a flat surface of the back-support grip with two screws, as shown in Fig. 12.2c. The edge of tested die/chip soldered on the PCB surface is in contact with the pin plug, as shown in Fig. 12.2c. The pin plug is inserted through a hole in the shear-tool grip, as shown in Fig. 12.2a, b. With this design, we can easily reutilize the back-support and shear-tool grips for multiple tests, and furthermore can have flexibility of testing various sizes of dies/chips as well as solder layers.

The shear test apparatus and specimen were modeled with ABAQUS to conduct the shear loading simulations and to study the correlation between the load-displacement behaviors and the interfacial fracture toughness. The actual material properties and dimensions of the apparatus and specimens were used in the model. The cohesive zone model (CZM) based
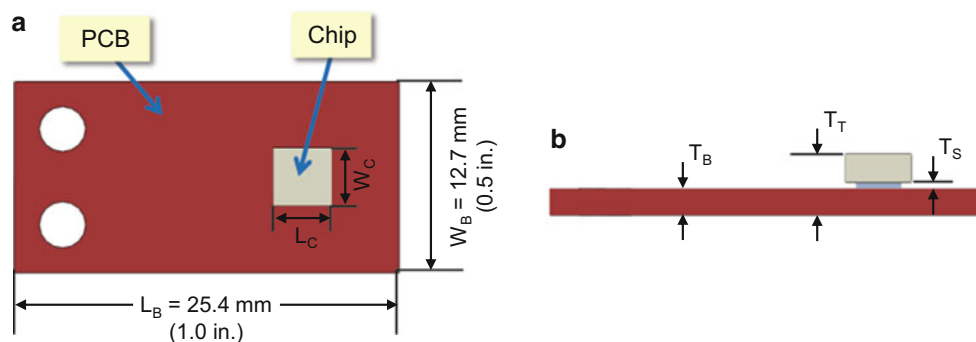
Fig. 12.1 Schematic (**a**) *top* and (**b**) *side* views of a shear test specimen and its dimensions with a dummy chip soldered to a PCB with Cu pads in-between
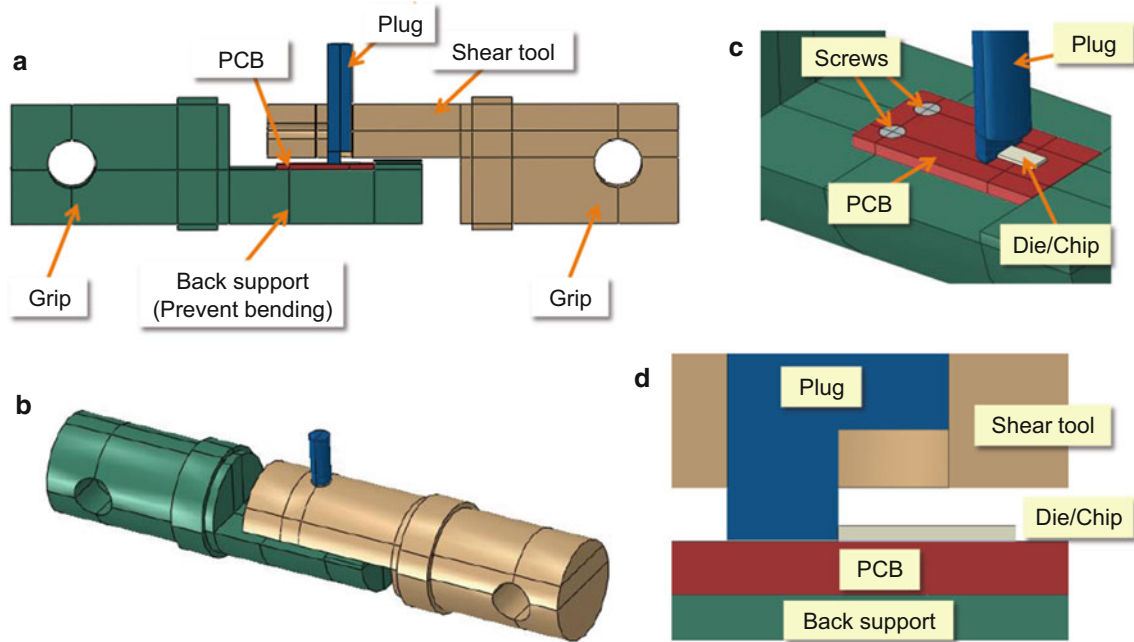
**Fig. 12.2** Schematic views of shear test apparatus and test specimen

Fig. 12.3 Shear test apparatus and specimen mounted and tested in an MTS load frame

on the traction-separation law was implemented to predict the initiation and progression of damage at the interfaces near the solder layer. Several model parameters required by the CZM simulation are not readily available or difficult to measure, so reasonably assumed values were used for these parameters, and parametric studies were conducted to determine the sensitivity of these parameters on the final results. The assumed CZM parameters and their reference values are as follows:

- Normal and shear stiffnesses: $k_n = k_s = 160$ MPa
- Peak nominal stress (normal): $t_n = 20$ MPa
- Peak nominal stress (shear): $t_s = 30$ MPa
- Normal mode fracture energy: $G_n = 2000$ N/m
- Shear mode fracture energy: $G_s = 6000$ N/m
- Friction coefficient (tangential): $f = 0.3$
- Solder layer thickness: t = 0.368 mm (Obtained from caliper measurements)
- Damage evolution: Exponential softening law.
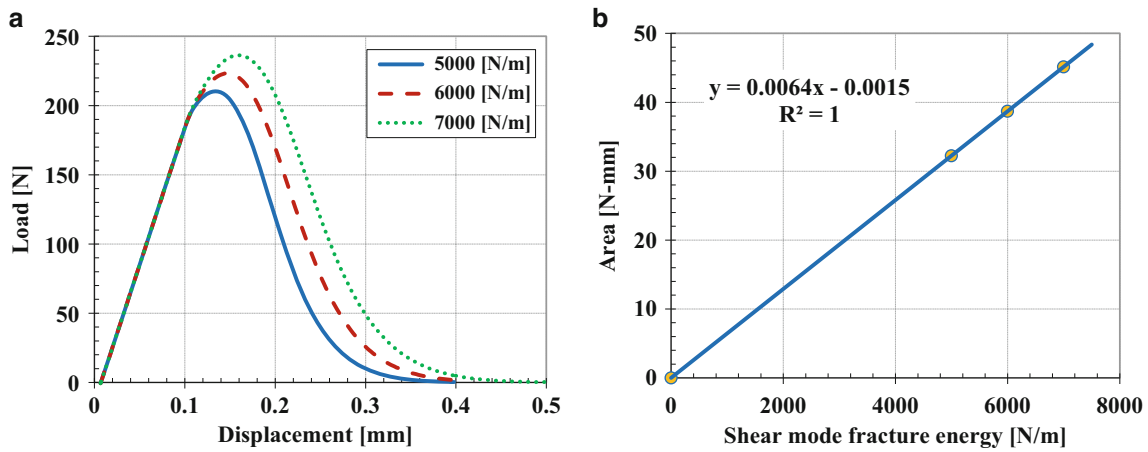
Fig. 12.4 (a) Load-displacement curves simulated with three shear mode fracture energy ($G_s = 5000, 6000, 7000$ N/m); (b) Area underneath the load-displacement curves against G_s
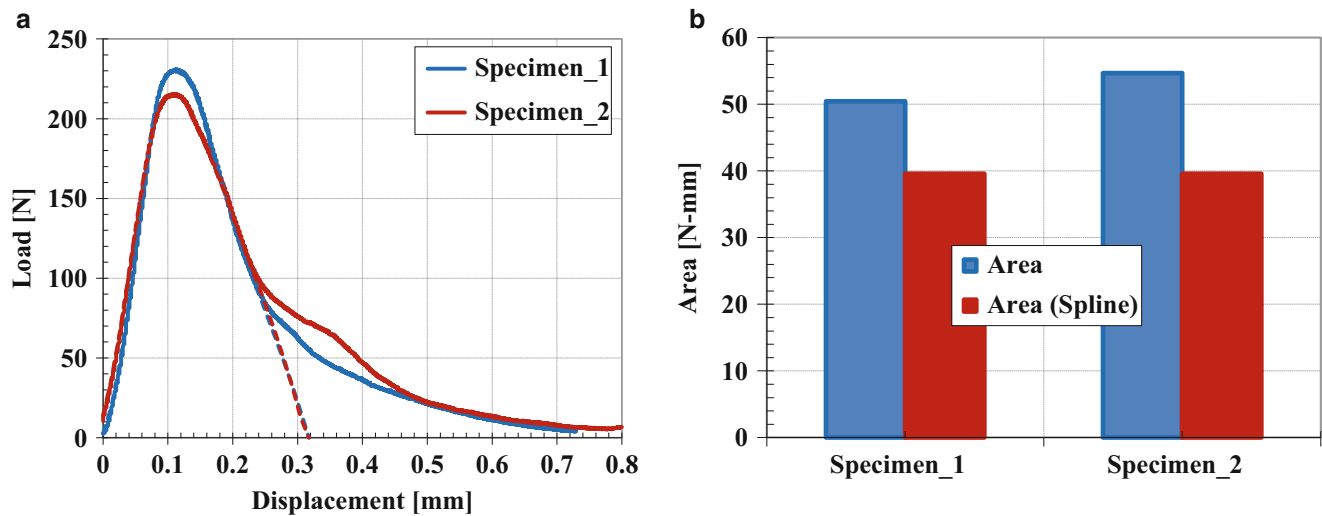
Fig. 12.5 (a) Load-displacement curves; (b) Area underneath the curves of two shear test specimens

It was found from several parametric studies that the simulation results are not sensitive to the CZM model parameters except the shear mode fracture energy (G_s). Therefore, we can conclude that the present test apparatus and specimens are suitable to characterize the interfacial shear mode fracture toughness.

Three values (5000, 6000 and 7000 N/m) of the interfacial shear mode fracture parameter, G_s, were chosen for the parametric study, and the resulting load-displacement curves are plotted in Fig. 12.4a, b shows the calculated area underneath the load-displacement curves against the three G_s. The three points as well as the origin (0, 0) are fit with a linear interpolation, whose fitting equations and the reliability of the fit are shown in the figures. All three cases indicate that the area underneath the load-displacement curves are linearly correlated with G_s. Therefore, once the area is obtained from experimentally measured load-displacement curves using the proposed shear test apparatus and specimens, G_s value can immediately be extracted from the fit equation.

12.3 Results and Discussion

Tests were conducted in the MTS machine at various displacement rates. During the tests, load and displacement were recorded. Fig. 12.5a shows an example of the load-displacement curves (solid lines) of the two shear specimens tested at 4.23 μm/s (0.01 in/min). The specimens were fabricated with metallic tin-lead (Sn63/Pb37 from Chip Quik) solder. Both
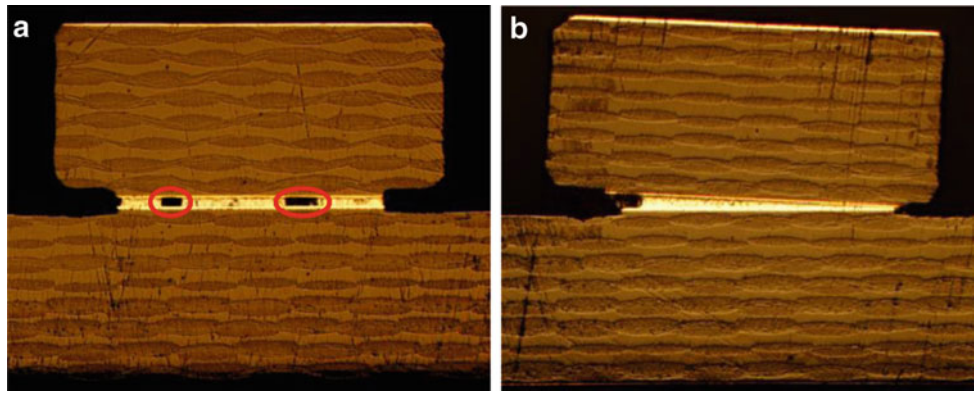
Fig. 12.6 Optical microscopic cross section images of sectioned shear test specimens showing (**a**) voids in the solder layer (highlighted with *red circles*); (**b**) significantly tilted chip
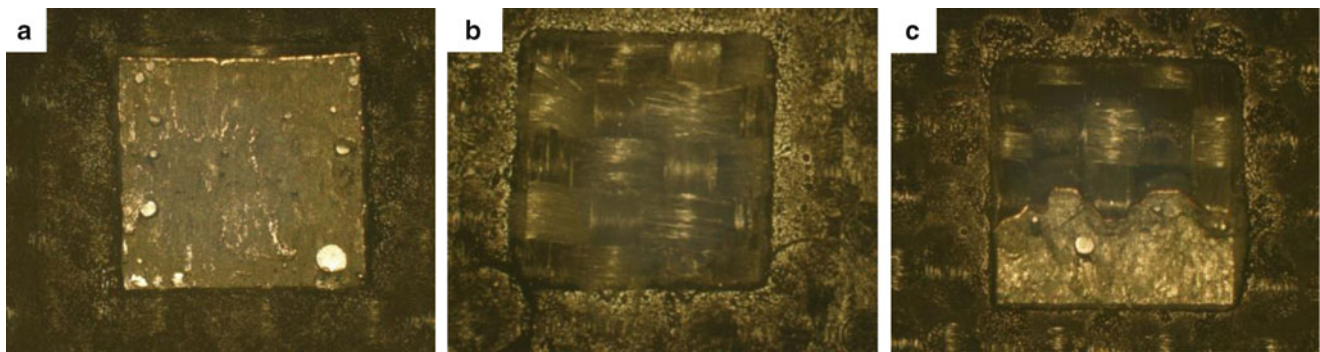

Fig. 12.7 Microscopic images of failed sections of (**a**) cohesive failure at the solder layer; (**b**) interfacial failure between PCB and Cu pad on PCB surface; (**c**) mixed cohesive and interfacial failure

curves show that the load increases with the increment of the shear deformation until a maximum load, where the interfacial damage likely initiates at the solder layer. The load decreases monotonically with the further increase of the displacement. Note that both curves are nearly identical in the incremental portion up to approximately 200 N and 0.07 mm with a slight difference in the maximum load. The curves also show the similar decremental behavior up to approximately 100 N at 0.24 mm. However, with the further increase of the displacement (>0.24 mm), the curves become significantly different. The curve of Specimen_1 continues to decreases monotonically, while the curve of Specimen_2 has a kink at the displacement between 0.24 and 0.46 mm. Both curves finally decrease nearly identically for larger displacements than 0.46 mm.

The difference in the load-displacement behavior, especially in the load-decremental portion, might be attributed from material and fabrication variability, such as void defect in the solder layer, misalignment/tilt of the chip, etc. To study such variability, the specimens were sectioned and polished to inspect their cross sections near the solder layer using an optical microscope. Optical microscopy images of two sectioned specimens in Fig. 12.6 clearly show the void defect in the solder layer and misalignment/tilt of the chip, which attribute to the variation in the load-displacement curves and damage behavior. To isolate the consequences of the material and fabrication variability from the overall trends, the decremental portion of the curve was simplified by ignoring the portion beyond any major kinks or inflections, and fitting the rest of the curves with a spline function. Dotted lines in Fig. 12.5a indicate the simplified (trimmed) fit curves. The area underneath the original load-displacement curves were calculated and plotted in blue color bars in Fig. 12.5b. The areas underneath the spline-fit curves are also plotted in red color and compared with the original curve areas. While the original curve areas of two specimens are approximately 10 % different because of the kink, the spline-fit curve areas are nearly identical.

By carefully inspecting the failed specimens, it was observed that the specimens failed in one of three failure modes depending on the displacement rates: cohesive failure mode (denoted as "C") at relatively slow rates, interfacial failure mode (denoted as "I") at relatively higher rates, and their mixed mode (denoted as "M") at intermediate rates. Fig. 12.7a shows the microscopic image of the PCB surface of the cohesively ("C") failed specimen, which was tested at a displacement rate of 0.0021 mm/s (0.005 in/min). The solder paste remains on the failed section uniformly. Fig. 12.7b shows the microscopic image
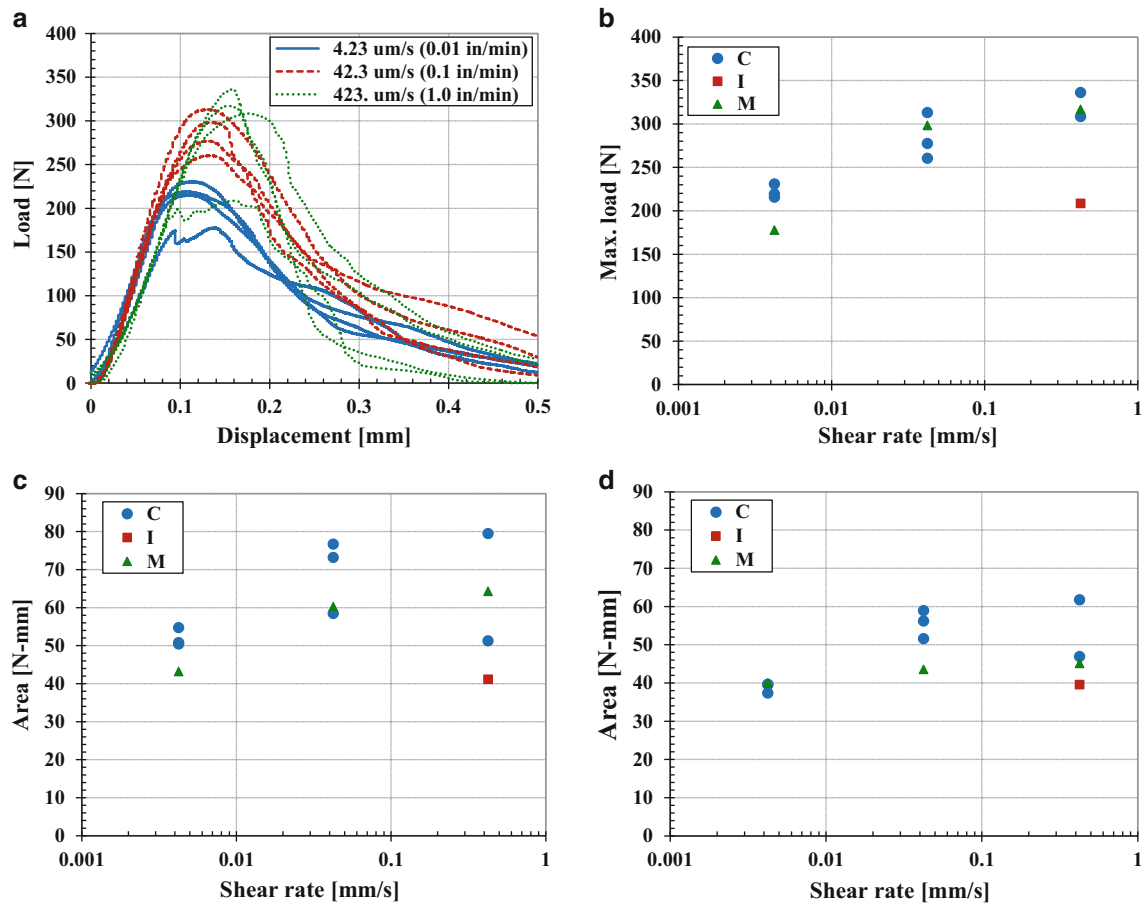
Fig. 12.8 (**a**) Comparison of load-displacement curves under shear loading at three displacement rates for metallic Sn/Pb solder; (**b**) Maximum load of load-displacement curves against applied shear displacement rates; Area underneath (**c**) original and (**d**) trimmed load-displacement curves against applied shear displacement rates. "C", "I", and "M" represent cohesive solder failure, interfacial pad failure, and mixed cohesive and interfacial failure modes, respectively

of the PCB surface of the interfacially ("I") failed specimen, which was tested at a displacement rate of 2.12 mm/s (5.0 in/min). The failed section of tested specimen clearly indicates that failure occurred at the interface between the woven-fabric PCB and the Cu pad on the PCB surface. Fig. 12.7c shows the microscopic image of the PCB surface of the mixed ("M") failed specimen, which was tested at a displacement rate of 0.42 mm/s (1.0 in/min). The image shows a mixture of the cohesive and interfacial failure mode. Some portion of pad surface area is covered by the solder paste, while the rest of the area shows the interfacial peeling between the PCB and the Cu pad.

Twelve more specimens were fabricated with the Sn63/Pb37 solder. Among the 12 specimens, four specimens were tested at each of displacement rates: 4.23 μm/s (0.01 in/min), 42.3 μm/s (0.1 in/min), and 423 μm/s (1.0 in/min). The load-displacement curves obtained from the shear tests at the three displacement rates are plotted and compared in Fig. 12.8a. Blue, red and green curves are for the displacement rates of 4.23 μm/s (0.01 in/min), 42.3 μm/s (0.1 in/min), and 423 μm/s (1.0 in/min), respectively. The maximum loads are plotted against the three displacement rates in Fig. 12.8b. The calculated areas underneath the load-displacement curves, which are related to the interfacial shear-mode fracture toughness, are plotted against the applied shear displacement rates in Fig. 12.8c (area under original curve) and Fig. 12.8d (trimmed area by spline-fit curve). Marker labels, "C", "I" and "M", indicate the cohesive failure mode at the solder layer; the interfacial failure mode between PCB and Cu pad; and the mixed cohesive and interfacial failure mode, respectively. The general trend is that the solder failure is a dominant failure mode at low shear rates, while the interfacial and mixed failure modes become more frequent as the shear rate increases. Such strain-rate dependency damage responses coincide with the results from numerous previous studies that have shown that, with increased strain rate, the tendency for brittle (interfacial) fracture of solders increases [16–20]. Note that the "C" and "M" failure modes yield similar maximum load levels, and much higher than the "I" failure mode, as shown in Fig. 12.8b. However, "C" failure mode yields higher fracture toughness than the "I" and "M" failure modes, as shown in Fig. 12.8c, d. The "I" failure mode yields significantly smaller area than "C" and "M" failure modes. The areas calculated with
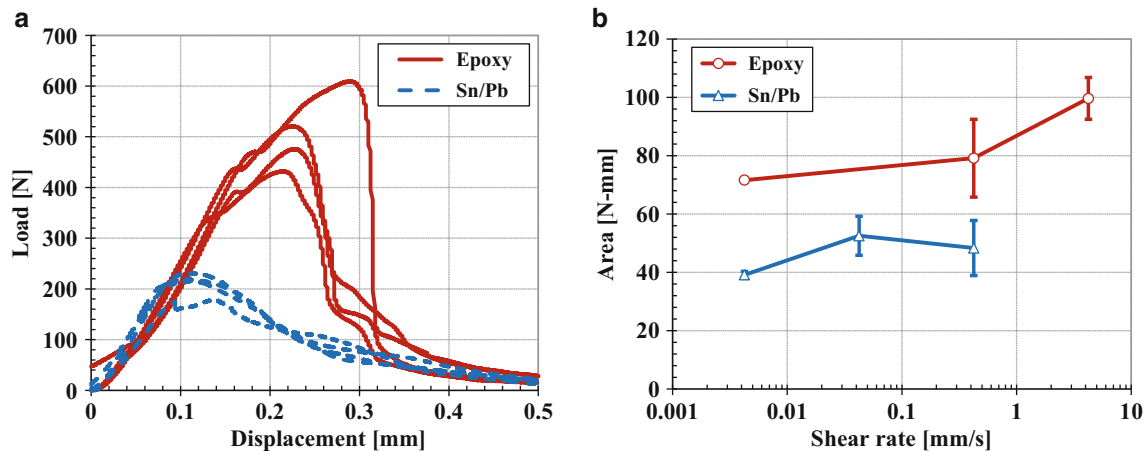
Fig. 12.9 (**a**) Comparison of load-displacement curves of metallic (Sn/Pb) and polymeric (Epoxy) solders under shear loading at a displacement rate of 0.254 mm/min (0.01 in/min); (**b**) Area underneath load-displacement curves against various shear displacement rates

the spline-fit curves yields less scattered data than those from the original curves. The overall trend is that both maximum load and fracture toughness increase significantly with the increase of the displacement rates.

Polymeric solder materials have been developed to enhance the damage resistance under the impact loading. Because of their dielectric nature, polymeric materials need to be mixed with fillers having high electrical conductivity and percolation threshold. Possible filler materials with high conductivity are carbon nanotubes, carbon black, etc. Several shear test specimens were fabricated with epoxy material as solder. In this study, we used neat Epon 828 epoxy resin without any fillers. The epoxy was cured with the curing agent Jeffamine D400. Fig. 12.9a shows the load-displacement curves of the epoxy solder specimens, and compares them with those of the metallic Sn/Pb solder specimens. The displacement rate of these tests is 0.254 mm/min (0.01 in/min). Although initial slope of the curves are similar for both types of solder specimens, the maximum load and area underneath the curves of the epoxy solder specimens are significantly larger than the Sn/Pb solder specimens. Fig. 12.9b compares the areas underneath the curves of the epoxy and the Sn/Pb solder specimens obtained from various displacement rate tests, and clearly shows that the areas of epoxy solder specimens are significantly larger than those of the metallic solder for wide ranges of load rates. Therefore, the epoxy solder can be a stronger and tougher material, and thus enhance the survivability under the shear fracture dominant load. Note that this conclusion is only valid for the relatively low loading rate. Tests at higher rates will be conducted in the future study.

12.4 Summary and Conclusions

A new experimental method was developed to characterize critical interfacial damage parameters of solder interconnects subjected to various strain-rate mechanical loading, ultimately simulating shock or impact loading. The test apparatus and specimen were devised to experimentally characterize such critical damage parameters, particularly interfacial shear strength and fracture toughness at various strain rates. The test apparatus was designed to easily mount and unmount test specimens, and accommodate various sizes of components and solder layer thicknesses. Test specimens were fabricated with both metallic and polymeric solder materials, and tests were conducted under various shear displacement rates. Maximum load and area as the measure of fracture toughness were characterized from measured load-displacement curves. Three failure modes depending on the load rates were identified from optical microscopy. It was found that both strength and fracture toughness exhibit significant rate-dependency. Computational simulations were also conducted to correlate the measured area of the curves with the interfacial fracture energy, which will further be used for the damage prediction of the electronic components under the high-g impact loading.

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