# Chapter 9
# High-Voltage Fast-Switching Gate Drivers

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## 9.1 Introduction

Gate drivers are key circuit blocks with growing importance for various automotive applications like fast switching DC-DC conversion and motor bridge drivers. New challenges arise from the introduction of the 48 V automotive board net and growing e-mobility with battery voltages in the range from 12 to 400 V. Increasing voltage requirements have influence on circuit design for power train control, power conversion between high- and low-voltage batteries, safety electronics and more. At the same time, the growing amount of electronics in cars demands for compact and cost efficient solutions with a high integration level.

More than hundred switched-mode converters with an output power of typically less than 10 W are installed in a car, for example. Converters have to be small in size and low in cost. This is achieved by increasing the switching frequency to the multi-MHz range, as the passive filter components of switching converters scale down. This results in very small on-times of the power switch [1].

Compact high-voltage converters demand for highly integrated gate drivers with galvanic isolation at even faster transition slopes. With wide bandgap semiconductors, such as GaN or SiC, converters with switching frequencies in the MHz-range and voltage slopes of >100V/ns are already achieved. This raises challenges also for the gate driver design, including compact layout with low parasitic inductances as well as robust transmission of gate driver control signals over a galvanic isolation barrier with small and matched propagation times [2].

With increasing switching frequency and steeper switching edges, electromagnetic compatibility (EMC) is a major concern in automotive. Gate drivers with slope control optimize EMC while maintaining good switching efficiency.

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After a brief overview of gate driver fundamentals in Sect. 9.2, Sect. 9.3 covers fast-switching drivers for 12 V and 48 V board net applications. Highly integrated gate drivers, suitable for high-voltage applications up to 400 V and above, are addressed in Sect. 9.4. The emphasis of Sect. 9.5 is on EMC and EMC optimized gate drivers.

## 9.2 Gate Driver Fundamentals

**Driver Configurations and Building Blocks** Figure 9.1 shows the fundamental power switch and driver configurations. Due to the lower on-resistance, the majority of power switches are n-type devices. This is in particular true in automotive applications. Depending on the location of the power switch, a low-side switch (Fig. 9.1a) and a high-side switch (Fig. 9.1b) can be distinguished. Both switches together form a half-bridge (Fig. 9.1c) and two half-bridges a full-bridge, also called H-bridge. Figure 9.1c indicates possible typical applications, an inductive DCDC converter and a DC motor driver, respectively.

A complete driver design includes several circuit blocks, some are highlighted in Fig. 9.1a, b. The control logic delivers the turn-on or turn-off signal for the power stage, usually in a pulse width modulated fashion. A level shifter converts the driver control signal from the low-voltage domain into the driver voltage domain. In a high-side driver, the control signal is shifted up with reference to the input supply voltage $V_{IN}$ of the power stage. The high-side driver may include a galvanic isolation for safety reasons (in case of high-voltage) and as part of the signal transfer. The gate supply provides the gate overdrive voltage $V_{drv}$. Many gate drivers utilize a linear regulator or a shunt regulator from $V_{IN}$ to generate $V_{drv}$. For an n-type high-side power transistor, a high-side gate supply of $(V_{IN} + V_{drv})$ needs to be available in order to keep the power transistor turned on. This can be accomplished with a bootstrap supply or a charge pump. If the power stage is configured as a half-bridge, a dead-time control is mandatory to avoid damage at the power stage due to cross conduction.

**Gate Driver Operation and Key Characteristics** The gate driver has to turn on a power transistor with sufficient gate overdrive voltage $V_{drv}$. Figure 9.2a shows

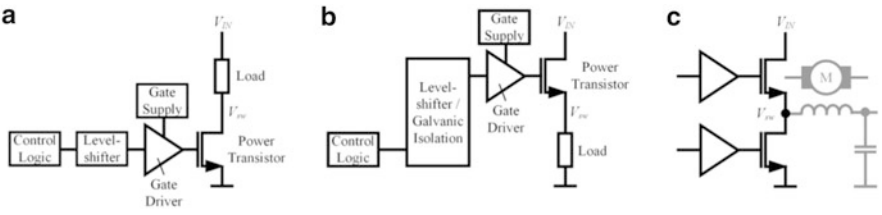


**Fig. 9.1** Power stage and driver configurations: (**a**) low-side driver; (**b**) high-side driver; (**c**) half-bridge

the circuit principle of a low-side gate driver. To turn-on the power transistor, its gate gets connected to $V_{drv}$, while its gate is pulled to ground (or more precisely to the source potential of the power transistor) to turn it off, each with a finite on-resistance $R_{drv}$ (which may be different in each path). Many applications use a CMOS inverter as a gate driver, especially for on-chip power stages with drive voltages $V_{drv} \leq 5\,\text{V}$. However most discrete power transistors require $V_{drv} > 5\,\text{V}$. PMOS devices in this voltage class, suitable for a driver design, are usually not area-efficient [3]. In some high-voltage technologies the PMOS transistor has up to 30 times larger resistance compared to the NMOS transistor. Therefore, an output stage with two NMOS transistors can be used [3–5]. A bootstrap circuit is required to provide the gate overdrive voltage for the NMOS transistor in the pull-up path. This will be covered in more detail in Sect. 9.4. While such configurations can be classified as hard switching drivers, few applications use current mode drivers, which essentially represent a current source output. Such stages are useful for EMC optimized drivers as discussed in Sect. 9.5.

The power transistor represents a capacitive load equal to the equivalent gate capacitance $C_{gate}$ (see Fig. 9.2a). The larger the gate current $I_{gate}$, the faster the rate of change of the gate voltage $V_{gate}$. The dc characteristics in Fig. 9.2b relates the gate voltage $V_{gate}$ to the current $I_{gate}$. While hard switching drivers are limited by

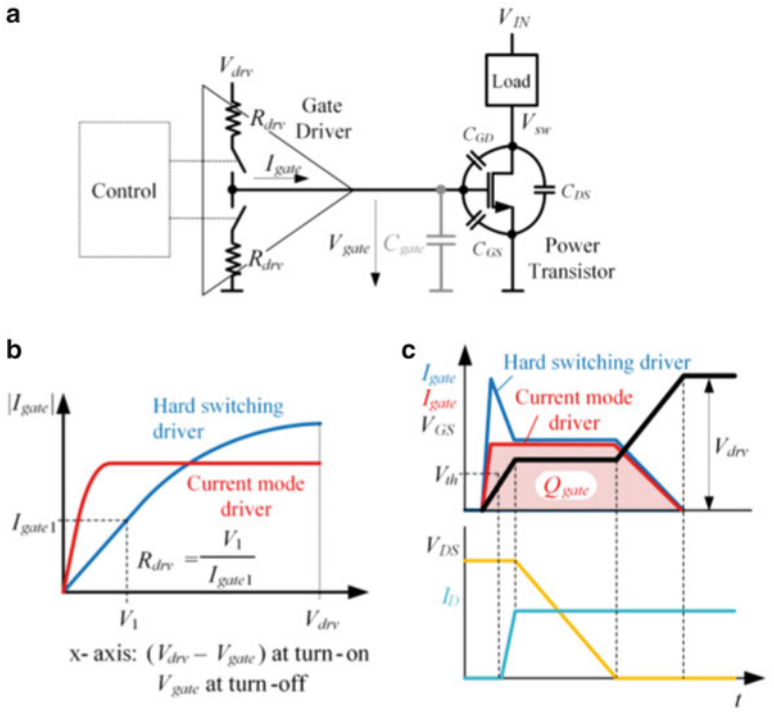


**Fig. 9.2** Low-side gate driver: (**a**) equivalent circuit; (**b**) dc and (**c**) transient characteristics

their finite on-resistance $R_{drv}$, current source drivers provide a nearly constant gate current over a wide range of $V_{gate}$. If the x-axis is chosen as indicated in the graph, the curve is valid for both the turn-on and turn-off case.

The transition starts at $I_{gate} = 0$, reaches a maximum current after some delay and goes back to $I_{gate} = 0$ after the transition has finished. This is illustrated in Fig. 9.2c for the two driver types. The absence of the current over-shoot represents a major advantage of the current mode driver with respect to EMC. This will be further explored in Sect. 9.5.

**Optimization for Speed, Power, Area** Fast switching with low propagation delay can be achieved by cascaded drivers. This approach has been used originally for CMOS digital drivers to drive large off-chip (capacitive) loads, e.g. for I/O buffers. The driver is designed such that the $W/L$-ratio of the transistors increases from stage to stage. The most common approach is based on a fixed scaling factor $\alpha$ [6, 7]. A minimum delay can be achieved by optimizing the scaling factor $\alpha$ and the number of stages $n$ with the general relationship expressed by

$$\alpha = \sqrt[n]{\frac{C_{gate}}{C_{inv}}}, \quad n = \frac{\ln \frac{C_{gate}}{C_{inv}}}{\ln \alpha} \quad . \tag{9.1}$$

While the model in [7] proposes an ideal scaling factor of $\alpha = \mathrm{e} \approx 2.71$, practical designs achieve a minimum delay for typical values of $\alpha = 3 \ldots 6$.

The optimization for minimum delay does not necessarily correspond to minimum power loss in the driver. The shoot-through current and dynamic gate charge losses in each inverter stage contribute to the overall power losses. Loss optimization typically results in less number of stages (larger scaling factor) compared to speed optimization. Usually power optimization comes along with reduced layout area, hence losses and area can be minimized concurrently.

**dv/dt Robustness** Once the driver is optimized for speed and/or power, there is one more design goal to be fulfilled. The driver needs to be strong enough to be robust against dv/dt transients. Referring to Fig. 9.2a, if the power transistor is turned off, the switching node transient causes a capacitive charging of $C_{GD}$. The pull-down path of the driver needs to be strong enough, so that the gate-source voltage of the power transistor does not reach the threshold voltage, i.e. $R_{drv} \leq V_{th} / \left( C_{GD} \frac{\partial V_{DS}}{\partial t} \right)$. If this condition requires to increase the driving strength of the final stage (i.e. $w_{n-1}$), the scaling factor $\alpha$ recalculates to $\alpha = \sqrt[n-1]{\frac{W_{n-1}}{W_1}}$ with the width $W_1$ of the first stage inverter.

## 9.3 Fast Switching Drivers

High-speed requirements for gate drivers are often derived from low-power switching converters in automotive systems. One battery supplies a large amount of applications like electrical motor control, safety, infotainment, lighting. Supply

wires are often long and converters are implemented in the applications at the point of load to supply micro-controllers, control circuits, interfaces and sensors. Converters have to be small in size and low in cost. This is achieved by increasing the switching frequency to the multi-MHz range, as the passive filter components of switching converters scale down.

### 9.3.1 Fast Switching Gate Driver Stage

A conversion from 50 to 5 V at a switching frequency of 10 MHz requires an on-time of the switch of less than 10 ns with rise/fall times in the range of 1 ns. This also minimizes frequency dependent transition losses. The on-time pulse has to be transferred properly to the power switches by the level shifter and gate driver. The whole driver and in particular the level shifter have to be robust against coupling currents caused by fast switching transients. A cascaded gate driver as described in Sect. 9.2 is suitable to achieve these high-speed requirements. An implementation of a high-speed gate driver is shown in Fig. 9.3.

For $C_{inv} = 7\,\text{pF}$ and $C_{gate} = 145\,\text{pF}$ the driver in Fig. 9.3 provides a good trade-off between die size and propagation delay for $n = 6$ inverter stages with a scaling factor of $\alpha = 5.24$ per stage [8]. To improve dynamic losses, which become dominant towards higher switching frequencies, cross currents have to be avoided, in particular in the last driver stage. This is accomplished by splitting up the driver stage into two branches, as shown in Fig. 9.3. This allows to control the PMOS and NMOS transistor of the last driver stage separately. There is no area penalty, since each branch has to drive approximately half of the capacitive load. Cross currents in the last stage are eliminated by asymmetric sizing within each

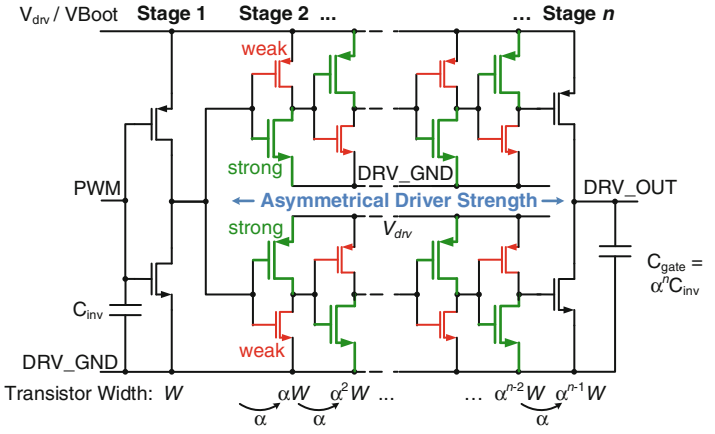


**Fig. 9.3** Cascaded gate driver with asymmetrically sized inverter stages, optimized for propagation delay and current consumption

inverter stage [1, 9]. This assures that the PMOS in the last driver stage is always turned off before the NMOS turns on and vice versa. An asymmetry factor of 20 % is used in this design, i.e., the width of the strong transistors is increased and the width of the weak transistors is decreased by 20 % with respect to the nominal value (based on Eq. (9.1)). This way, the losses in gate drivers can be reduced by up to 25 %, confirmed by simulations.

### 9.3.2 Comparison of NMOS and PMOS Power Switch

Figure 9.1 has shown the use of an NMOS transistor as a high-side switch, which results in lower on-resistance and lower area consumption compared to a PMOS switch. On the other hand, its gate supply based on a charge pump or bootstrap circuit requires a higher effort and adds more complexity. The PMOS power switch generates also less switching noise, because its gate voltage receives a swing in between two constant voltages, *VIN* and $HSGND = VIN - 5\,\text{V}$, which is typically generated by an on-chip linear regulator. The main requirement for the PMOS level shifter is a fast switching speed and to propagate short on-time pulses of a few ns. This can be achieved with current mirror based [1, 10] or capacitive level shifters [11].

For an NMOS high-side transistor as shown in Fig. 9.1b, the source of the transistor is at the switching node *VSW*, which becomes also the ground reference of the gate driver and the high-side portion of the level shifter. The gate supply *VBoot* is above *VSW* by $V_{drv}$ (typically 5 V) to safely turn on the NMOS transistor if $VSW \rightarrow VIN$. *VBoot* is generated by a bootstrap circuit [12] or by a charge pump. Figure 9.4 shows how *VBoot* follows the switching transition at *VSW*. Slopes larger than 20 V/ns charge/discharge the parasitic capacitances of the high-side isolation, resulting in large peak currents. Coupling currents in the mA range get superimposed to the level shifter signal currents, which are in the lower µA range. Existing level shifter concepts for PMOS transistors cannot directly be utilized for NMOS transistors, as they are sensitive to in-coupling and would cause faulty switching during fast high-side transitions. They would also not be fast enough for multi-MHz operation, as will be discussed in the next section.

### 9.3.3 Conventional Level Shifters

Several fast switching level shifters for NMOS power transistors have been published [13, 14], which achieve a very fast propagation delay, but a transfer of short PWM on-time pulses in the low nanoseconds range is not supported. In conventional level shifter concepts, the signal is typically transferred by a high-voltage switch on the low-side, which creates a voltage drop on the high-side across a resistor or a current source, as shown in Fig. 9.5. This voltage drop is detected on the high-side

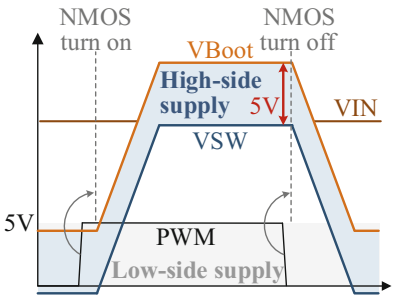


**Fig. 9.4** High-side voltage domain for controlling NMOS power transistors with a floating high-side

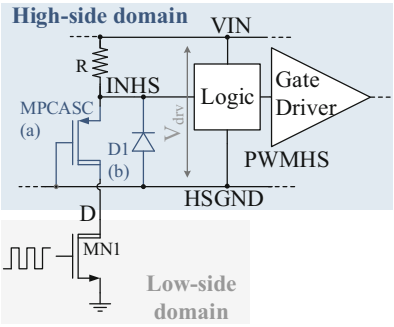


**Fig. 9.5** Conventional level shifter with PMOS cascode (**a**) and diode clamping (**b**)

by a digital circuit, e.g. a latch. As the high-side circuits use low-voltage transistors, the voltage drop across the resistor or current source has to be clamped to not violate the maximum ratings. Figure 9.5 shows two ways of commonly used clamps, based on a cascode (a) and diode (b), respectively. Both clamping components need to be low resistive and, hence, add significant parasitic capacitance to the *INHS* node. The charging time is in the range of 20 ns to >100 ns in a 180 nm BiCMOS technology, for instance. Pulses within this time are completely filtered. Capacitive level shifters [15] provide an alternative option for fast signal transfer. However, they also need some kind of clamping and suffer from large parasitic coupling currents during high-side transitions. In conclusion, the speed of conventional level shifters is too low for multi-MHz switching.

### *9.3.4 High-Speed Level Shifters*

For the control of a PMOS power transistor, the level shifter depicted in Fig. 9.6a is suitable and provides several advantages [1, 8, 16]. A symmetrical single-stage amplifier with its output stage referred to *HSGND* generates a rail-to-rail control signal *PWMHS* on the high-side. To achieve the required delay, a small 1 ţA pre-bias current keeps the bias voltages of the current mirrors above the threshold, reducing the voltage swing during switching significantly. This way, a total propagation delay in the level shifter in the range of 3 ns is achieved.

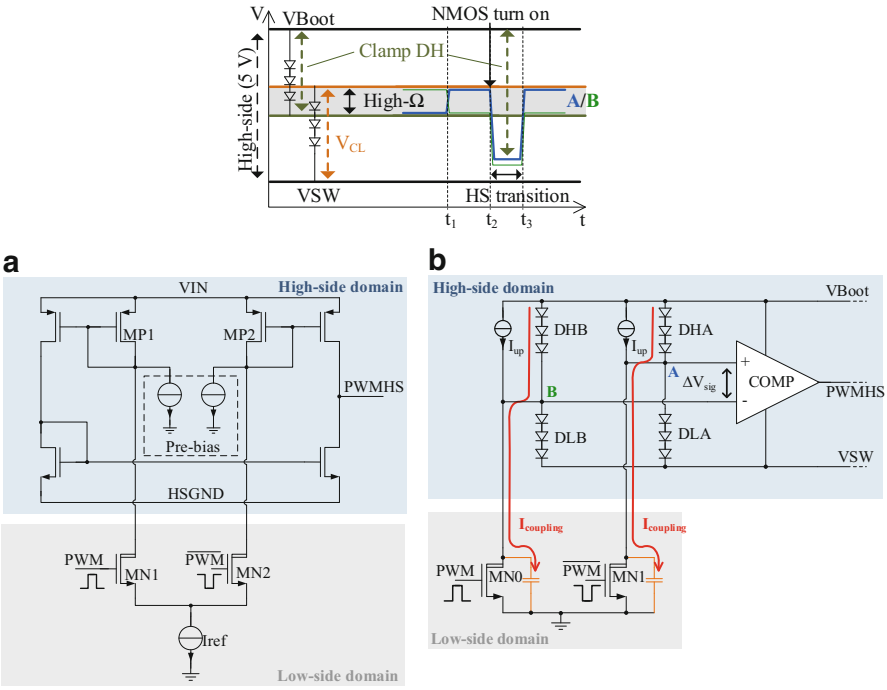


**Fig. 9.6** High-speed level shifters (**a**) for control of a PMOS power transistor, and (**b**) control of an NMOS power transistor at floating high-side

Figure 9.6b shows the level shifter implementation [17], which provides a fast and robust control of a power stage with NMOS high-side transistor. High-voltage switches MN0 and MN1 create a differential voltage $\Delta V_{sig}$ between nodes *A* and *B*, which is detected by a high-speed comparator. The differential voltage range at the nodes *A* and *B* is limited by clamping diodes as shown in Fig. 9.6b. If the low-side switch MN0 or MN1 is turned on, the according node *A* or *B* is held at the lower boundary by the clamps DHA or DHB, respectively (see signals in Fig. 9.6b). Accordingly, when the low-side switch is turned off, the clamps DLA or DLB hold the voltage at *A* or *B* at the upper voltage boundary, while the clamp conducts the active load current $I_{up}$. The clamping voltages are designed such that none of the diode stacks is conducting in between the upper and lower voltage boundary. A high-impedance region is obtained, in which the differential signal between *A* and *B* can change its state at very high speed.

After the state change of *PWM*, the NMOS power transistor is turned on or off by the gate driver. A high-side transition of the switching node follows, in which the voltage rails *VBoot* and *VSW* experience a voltage step up to *VIN* with a slope of 20 V/ns and faster. The parasitic capacitances at the drain of MN0 and MN1 are charged. Even for small parasitic capacitances, coupling currents $I_{coupling}$ in the range of 2 mA are generated, which are superimposed to the signal currents

in the range of 50 µA. At rising high-side transitions, the forward voltages across the clamps DHA and DHB cause the voltages at nodes *A* and *B* to fall significantly below the lower boundary of the high-impedance region. The overlapping diode clamps are designed such that the high-impedance region typically has a range of a few hundred millivolts and occurs in the center between *VBoot* and *VSW*. This allows the nodes *A* and *B* to drop by nearly two volts below the high-impedance region. With a large common mode input range of the comparator, a very large forward voltage across the clamps can be tolerated. Thus, the clamps can be designed small (low capacitance) to handle the full coupling currents. This is a major advantage, compared to clamps of Fig. 9.5, which occupy large area (hence, large capacitance). At falling high-side transitions, the coupling currents are clamped by DLA and DLB to *HSGND*, accordingly.

This concept allows to transfer PWM signals with on-time pulses smaller than 3 ns to the high-side with high robustness against the fast high-side transitions. Thus, the level shifter is suitable to operate at frequencies >10 MHz at large input voltage and high conversion ratios *VIN*/*VOUT*.

Besides the coupling into the signal path, large disturbances in sub-circuits on the entire IC can occur by coupling currents into the substrate, caused by parasitic capacitances of the high-side isolation well during fast switching transients. The high-side isolation (typically implemented as n-well on a p-substrate) is required to isolate the level shifter and gate driver from the low-voltage circuits on the substrate. To effectively dissipate the coupling currents, which can be in the range of hundreds of milliamperes even at switching transients below 10 V/ns, dedicated diverting structures have to be placed on the substrate. Back-side metalization, conducting trenches or p-guardrings are suitable [18].

## 9.4 High-Voltage Drivers

Gate drivers are essential for automotive applications in electric vehicles, running from voltages above 300 V. Figure 9.7 shows a typical setup of a high-voltage gate driver and power transistor. The area-efficient implementation of fully integrated gate drivers is discussed in Sect. 9.4.1. Section 9.4.2 covers galvanic isolation between the low-side driver control circuit and the high-side driver.

### 9.4.1 Driver Output Stage

Typical gate drive voltages of high-voltage power transistors are above 10V. In fully integrated gate drivers, a large portion of die area is occupied by the driver output stage, consisting of two or more transistors with voltage ratings for 15 V and above. NMOS transistors are preferred because of their lower RDSon per area, but they require a bootstrap supply for the gate overdrive. Placing a PMOS transistor in parallel to the NMOS pull-up transistor in the driver output avoids the need for a bootstrap supply. However, a parallel PMOS transistor still occupies significant area, as in most technologies only high-voltage NMOS devices (LDMOS) are optimized for high current density. Dependent on technology, an output stage with two NMOS transistors provides an area-efficient solution, utilizing the effect of high-voltage charge storing as part of an on-chip bootstrap circuit [19, 20]. The operation of a conventional bootstrap circuit is shown in Fig. 9.8a1. For simplified explanations, the diode forward voltages are assumed to be 0 V. If $IN = 0$ V and the level shifter output signal *LvlSh_OUT* is 'low' the driver is turned off and the node *OUT* is shorted to ground by *MN*2. *CBoot* is charged to 5 V by the supply voltage *V*1. By setting *IN* to high, *MN*2 turns off, and *MN*1 is switched on by *LvlSh_OUT* and the buffer *B*2. The *OUT* node rises to *Vdrv* while *DBoot* prevents *CBoot* from discharging to *V*1. *VCBoot* serves as floating voltage supply and has to provide the charge $Q_{tot}$ for *B*2, the gate capacitance of *MN*1 and the level shifter. The gate charge for the actual power transistor is provided separately by *Vdrv*. A typical value for *Vdrv* is 15 V. The charge that is available from *CBoot* to achieve a voltage dip $V_{dip}$ at *VCBoot* can be calculated as

$$Q_{tot} = CBoot \cdot V_{dip}. \tag{9.2}$$

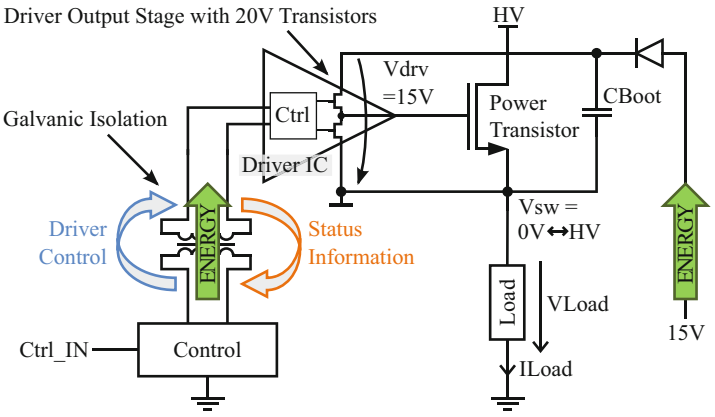


**Fig. 9.7** Gate driver and power transistor

The MOSFET buffers $B1$ and $B2$ in Fig. 9.8 are tapered buffer stages similar to Fig. 9.3 as discussed in Sects. 9.1 and 9.3. They have a typical undervoltage level of 4–4.5 V [21], assuming a nominal gate-source voltage of 5 V for $MN1$, $MN2$. An upper voltage limit is given by its breakdown voltage which is 5.6 V in this case. Hence a bootstrap capacitor charged to 5 V can only be discharged by $Vdip = 0.5-1$ V. It has to be observed that in a real circuit $V1$ must be ∼5.7 V to compensate the forward voltage of *DBoot*. The conventional bootstrap circuit suffers from small charge allocation in respect to the whole stored charge in the bootstrap capacitor. This represents a significant area limitation for an on-chip bootstrap capacitor.

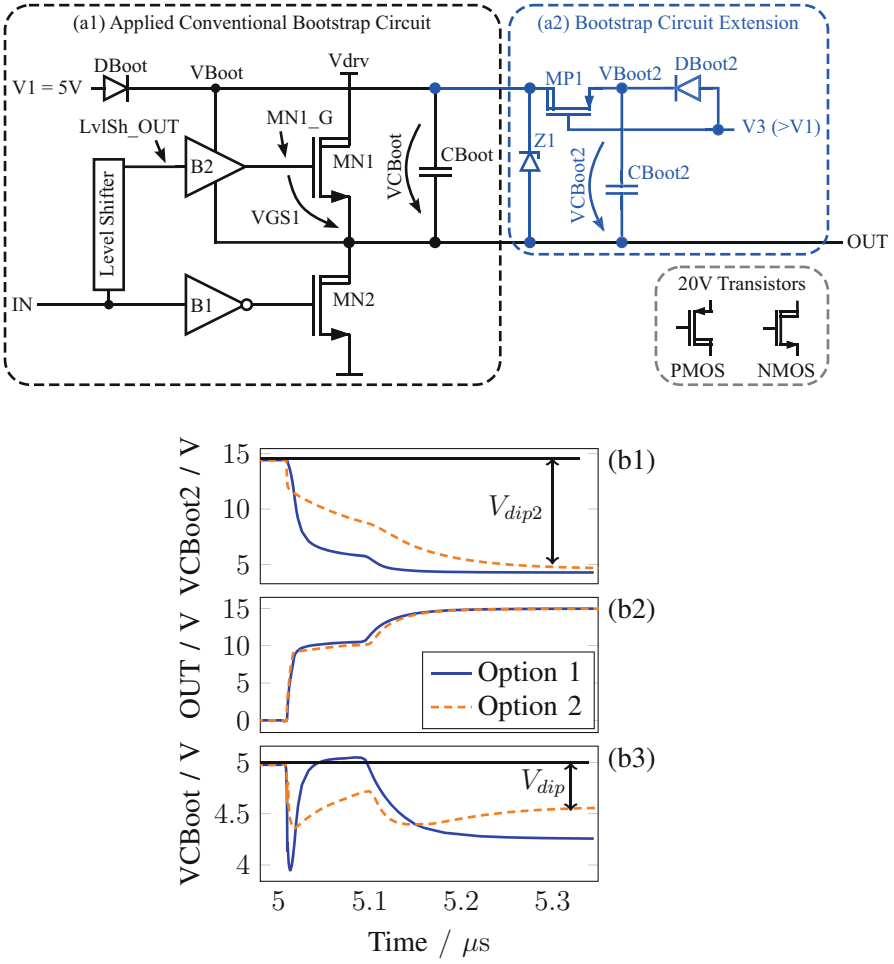


**Fig. 9.8** Two NMOS transistor output stage buffer with (**a1**) conventional bootstrap circuit and extended by (**a2**) bootstrap circuit option 1. (**b**) Transient voltage signals according to the bootstrap circuit option 1 and option 2

The bootstrap concept in Fig. 9.8a2 [19, 20], is an extension of the conventional bootstrap circuit. Figure 9.8b (option 1) shows the corresponding simulated transient voltage signals. A second bootstrap capacitor *CBoot*2 is charged by *V*3, a higher voltage than *V*1, e.g., 15 V, Fig. 9.8b1. For *V*3 the same voltage as *Vdrv* could be used. If the output node *OUT* rises, MP1 conducts as *VBoot*2 exceeds *V*3 by more than a threshold voltage of MP1, Fig. 9.8b2. *DBoot*2 blocks the current from *CBoot*2 to *V*3 and *CBoot*2 automatically discharges to *CBoot*, to the gate node of *MN*1 and to the circuits supplied by *VCBoot* (Fig. 9.8b1 and b3) through *MP*1. A charge balance between *CBoot*, *CBoot*2 and any additional load capacitance (mainly the gate capacitance of *MN*1) occurs. In first order, *CBoot*2 discharges from a value of *V*3 to *V*1, e.g., from 15 to 5 V. *Z*1 protects the circuit at *CBoot* against overvoltage in case of failure, like an overcharged capacitor *CBoot*2. Since the large voltage swing $V_{dip2}$ (Fig. 9.8b1) results in a high amount of charge (Eq. (9.2)) a significantly smaller bootstrap capacitor *CBoot* can be used. Area is saved, even with the addition of capacitor *CBoot*2.

A disadvantage of the circuit in Fig. 9.8 is that MP1 turns on after *OUT* rises. Before this, the required charge comes from *CBoot*, leading to a short voltage dip at *VCBoot* until *CBoot* is recharged from *CBoot*2, Fig. 9.8b3. A voltage dip larger than specified can influence circuit blocks supplied from *VCBoot*, such as faulty switching in the level shifter. In addition, the circuit of Fig. 9.8a2 requires a relatively large PMOS transistor *MP*1.

A second option of the driver output stage, shown in Fig. 9.9, solves these disadvantages (circuit option 3 in [19]). The corresponding transient voltage signals are shown in Fig. 9.8b (Option 2). *MN*3 directly connects *CBoot*2 to the gate node of *MN*1 after *MN*4 turns off, both controlled by the signal *Lvlsh_OUT* via the buffers *B*3 and *B*2*b*. Before the driver output voltage *OUT* rises, the charge for the gate node *MN*1*_G* is supplied directly from *V*3 without discharging *CBoot*2 and *CBoot*. This increases the voltage stability of *VCBoot* and reduces the total required charge from *CBoot*2 and *CBoot*, resulting in a smaller voltage dip *Vdip* in the end of the switching phase, Fig. 9.8b3. When *VGS*1 reaches the turn-off level of gate *NAND*1, *MP*4 turns on and *MN*1*_G* is fully charged by *CBoot*. While *VGS*1 rises, the gate-source voltage of *MN*3 decreases and is finally turned-off. *CBoot*2 is still connected to *CBoot* by *MP*1. The high-voltage PMOS transistor *MP*1 is optional, because the low-voltage transistor *MP*4 keeps *MN*1 in its on-state. Nevertheless, *MP*1 is advantageous for recharging *CBoot* after driver turn-on, Fig. 9.8b3.

Sizing guidelines for *CBoot* and *CBoot*2 are given in [19], considering worst case of operation and process corner. For circuit option 2, *CBoot* is calculated with ~76 pF and *CBoot*2 with 19 pF to get a voltage dip < 1 V at *VCBoot*.

A comparison to a conventional bootstrap circuit can be based on Eq. (9.2). With $Q_{tot,max} = 246$ pC and $V_{dip,max} = 1$ V, *CBoot_conv* results in 246 pF. Considering the same worst case parameters as used for the calculations of *CBoot* and *CBoot*2, *CBoot_conv* results in 324 pF. A decrease of the overall capacitor area by about 70 % can be achieved in case that *CBoot*2 can be placed on top of *CBoot*, while *CBoot*2 can be implemented as high-voltage metal-metal capacitor and *CBoot* as a low-voltage poly-nwell capacitor. The metal-metal capacitor is assumed to have

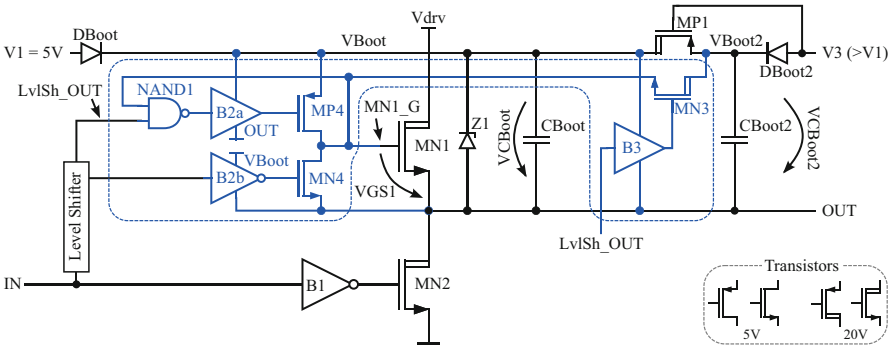


**Fig. 9.9** Option 2 of the bootstrap circuit with an NMOS transistor connecting directly to the gate of MN1

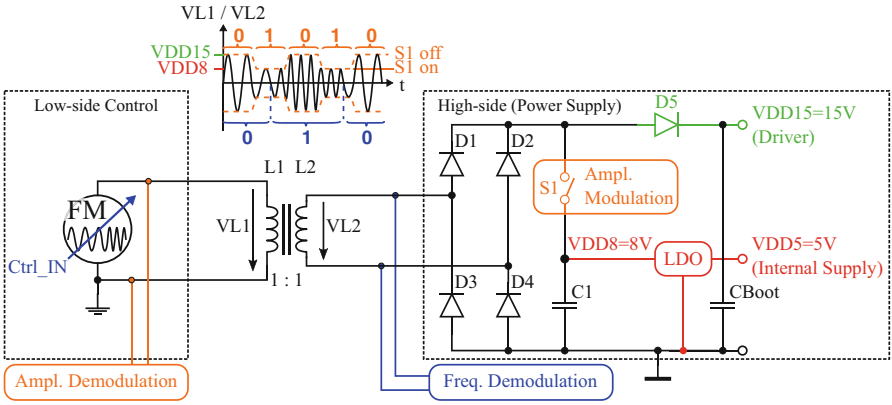


**Fig. 9.10** Implementation of the transmission concept

a capacitance density of 25 % of a poly-nwell capacitor. For area comparison *CBoot_conv* was assumed to be a stacked capacitor, consisting of a metal-metal and poly-nwell capacitor, as well. Even if *CBoot*2 is placed next to *CBoot*, a decrease of >50 % in area is achieved, compared to a non-stacked conventional capacitor *CBoot_conv*.

### 9.4.2 *Galvanic Isolation with Signal and Energy Transfer*

For safety or robustness reasons, galvanic isolated gate drivers are required. There are mainly four physical ways to supply gate drivers with energy and control signals over the isolation barrier: (1) Inductively, with discrete or integrated transformers, (2) optically, with opto couplers or fibre optics, (3) electrically, with capacitors and

(4) mechanically, with piezo elements. For applications in a power range $< 100\,\text{kW}$, transformers and opto couplers are widely used [22]. Opto couplers provide a signal, but no energy transmission, and they have relatively large propagation times [23]. Transformers have the possibility for energy transfer and signal transmission. Separate transformers are typically used for each signal and energy channel [22, 24]. In [25], high performance energy and unidirectional signal transmission is realized by microwave circuits with high complexity and cost. An unidirectional capacitive signal transmission is proposed in [15] with parallel energy transfer via a transformer. With the goal to further reduce the size and component count, the approach in [26] uses the existing signal transformer for energy transfer in addition to a conventional bootstrap gate supply, as indicated in Fig. 9.7. The additional energy transfer eliminates the duty cycle limitation of conventional bootstrapping, as the driver does not need to be switched off periodically for bootstrap recharge. While bootstrapping is the main supply for high current peaks during the driver switching phase (gate charge of the driven power switch), the transfer via the transformer provides the energy to supply the high-side driver electronics and to compensate any leakage currents once the driver is turned on.

Figure 9.10 shows the implementation of energy and bidirectional signal transmission according to [26]. The corresponding voltage signals from a measurement are shown in Fig. 9.11. By alternating switch $S1$, the transferred energy of $VL1$ is distributed to two high-side supply rails, $VDD15 = 15\,\text{V}$ (for the gate overdrive of the external power transistor) and $VDD8 = 8\,\text{V}$ (for high-side circuit blocks), Fig. 9.10. The driver control signal *Ctrl_IN* from low to high-side is transmitted by a frequency modulated (FM) signal ($VL1$, $10/20\,\text{MHz}$), generated by a resonance circuit on the low-side. On the secondary side the signal is demodulated by a frequency demodulation circuit for driver control, switching a high-side power transistor with load (*VLoad*). As a key function, the power distribution switch $S1$ is utilized also for amplitude modulation (*AM_IN*) for a backward signal transmission, Fig. 9.10. If $S1$ is turned-off, $VL1$ oscillates with an amplitude of up to two times of $VDD15$. If $S1$ is turned-on, the amplitude is clamped to an amplitude of nearly two times of $VDD8$. The switching frequency of $S1$ must be chosen significantly lower than the lowest frequency of the FM signal (e.g. $1\,\text{MHz} << 10\,\text{MHz}$). Alternating $S1$ according to the signal *AM_IN* enables a very energy efficient and well detectable modulation (*AM_recovered*) in combination with the energy supply. This is an advantage over conventional load modulation, which demands a trade-off between

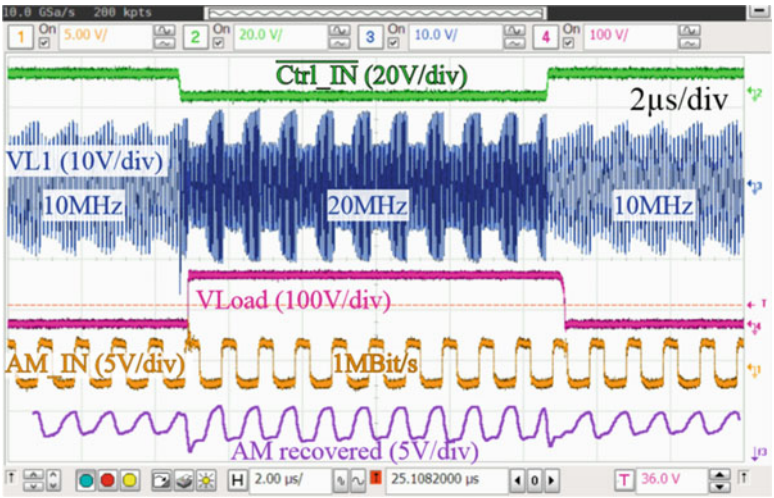


**Fig. 9.11** Measured signal transmission over the transformer with a test setup shown in Fig. 9.7 (*Iload* = 1.2 A, *HV* = 100 V)

power efficiency due to power loss in the load resistor and good detectability of the modulated signals [27, 28].

For very fast switching applications, enabled by new fast switching devices like GaN devices, a short propagation delay and very good delay matching become increasingly important. Both parameters can be significantly improved by pushing the carrier frequency of the FM signal to higher frequencies or by applying pulsed signal transmission concepts.

## 9.5 EMC and Switching Losses

With the increase in switching speed, a reduction in switching losses and in PCB area can be achieved. At the same time, the electromagnetic emissions (EME) are vastly increased because of the fast transition speeds in the power switches. In the following subsections the EMC influencing factors in gate driver design and a trade-off between switching losses and EMC are discussed [29].

### *9.5.1 EMC Influencing Factors*

The EME of a half-bridge circuit can be approximated with the fourier transform of a trapezoidal signal, Fig. 9.12a. This is shown in Eq. (9.3) with the simplification that the risetime $\tau_r$ is equal to the falltime $\tau_f$ [30].

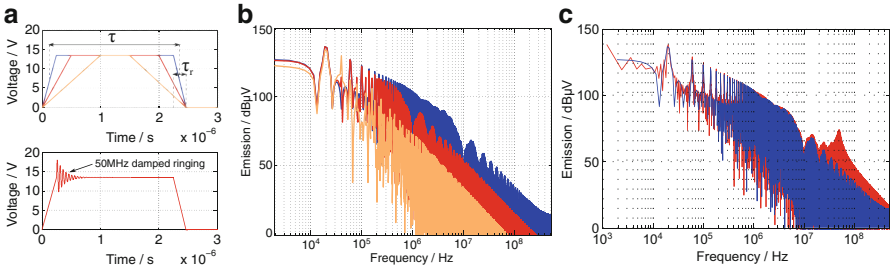


**Fig. 9.12** (**a**) *Top*: Trapezoid signal with different rise times *Bottom*: Trapezoidal signal with 50 MHz ringing. (**b**) Spectral influence of different rise times of the trapezoidal signal. (**c**) Spectral influence of the sinusoidal overshoot

$$E_{dB} = 20\log\left(2A\frac{\tau}{T}\right) + 20\log\left|\frac{\sin(\pi\tau f)}{\pi\tau f}\right| + 20\log\left|\frac{\sin(\pi\tau_r f)}{\pi\tau_r f}\right| \tag{9.3}$$

The first term shows the DC magnitude, which is mainly influenced by the amplitude $A$ of the signal and the on-time $\tau$ of the pulse width modulated (PWM) switching signal. The second term marks the first breakpoint, at which the energy contained in the signal will begin to fall with −20 dB/decade. According to (9.3) the second term is set by the on-time $\tau$ of the trapezoidal signal. As the amplitude $A$, the on-time $\tau$ and the PWM frequency $f$ are given by the application, the first and the second term in (9.3) cannot be influenced by the gate driver. Only the third term remains to reduce the EME of the voltage transition. This term shows the second frequency breakpoint at which the signal begins to decrease with −40 dB/decade. To reduce the EME, the risetime $\tau_r$ of the trapezoidal signal has to be increased by reducing the gate current of the active MOSFET. This is shown by simulation in Fig. 9.12b. The result is a lower emission in the higher frequency range. An often not considered factor is the influence of the current transition on the EME spectrum. In a bridge setup, the commutation current and the parasitic inductances of the printed circuit board traces, interconnects, packaging and especially the bond wires of the semiconductors cause voltage overshoots and ringing, Fig. 9.12a. These effects are superimposed to the trapezoidal shaped voltage signal. This changes the EME at the ringing frequency of the signal as demonstrated in Fig. 9.12c by a Matlab® simulation (at 50 MHz ringing frequency in this example). It can be concluded that there are two main levers to optimize the EMC performance of a half bridge setup with the gate driver. With the voltage transition, the spectrum can be optimized for all frequencies above the second break point of the trapezoidal signal. By reducing the speed of the current transition, it is possible to reduce EME caused by the ringing effects of the commutating load current. Both measures take effect in the higher frequency range. The EME in the lower frequency ranges has to be reduced by effective filter circuits, because it is not possible to reduce them with the gate driver.

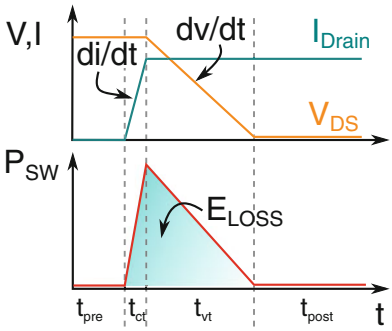


**Fig. 9.13** Switching transitions for inductive switching and losses

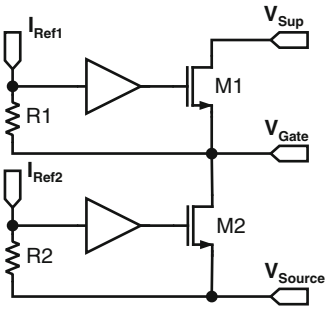


**Fig. 9.14** Output stage of a current mode gate driver

### *9.5.2 Switching Losses vs. EMC*

If di/dt and dv/dt are slowed down, the EME is minimized, but the switching losses in the switch(es) are maximized. The multiplication of $V_{DS}$ and $I_{Drain}$ forms a switching loss triangle as shown in Fig. 9.13. One slope of the triangle is given by the transition of the current and the other slope is defined by the transition of the voltage (see also Fig. 9.2c). Usually the current slope is much steeper than the voltage slope, i.e. the voltage transition is the main contributor to the switching losses. By controlling the di/dt and dv/dt, the gate driver can optimize the switching profile for better EMC performance or for lower switching losses. The profile can also be adjusted for optimized EME in an specific area of the spectrum by adjusting the transition speed with the highest influence in that area.

To be able to influence the transitions of MOSFET bridges separately, a gate driver with a highly variable output current has to be used. A topology with a voltage controlled current source (VCCS) output stage is shown in Fig. 9.14. The output stage can be used as a high-side or low-side driver and is able to switch between freely adjustable current levels with transition times of less than 10 ns.

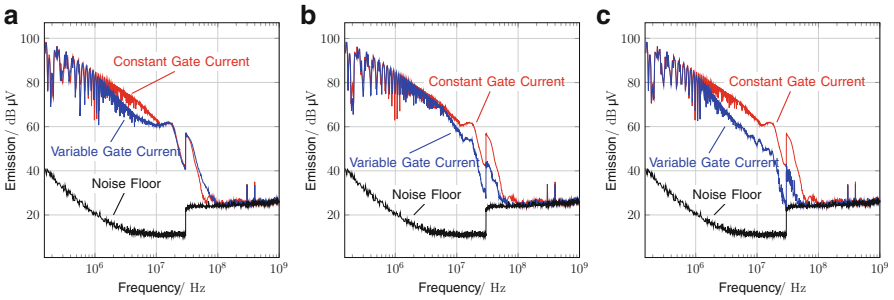


**Fig. 9.15** EMC measurements with reduced gate current in (**a**) the voltage transition $t_{vt}$, (**b**) the current transition $t_{ct}$, (**c**) for both transition phases

### *9.5.3 Experimental Results*

The driver in Fig. 9.14 was tested in a half bridge configuration driving a 300 µH air coil at a switching frequency of 20 kHz. The bridge voltage is $V_{Bat} = 13.5$ V and the load current is $I_{Drain} = 5$ A. EMC measurements were taken at the output node of the half bridge with the 150 Ohm method [31]. In the following measurements, the gate current is always set to 200 mA for the phases $t_{pre}$ and $t_{post}$, Fig. 9.13. With a continuous gate current of 200 mA, the voltage transition takes 100 ns whereas the current transition is 20 ns. A large current spike of 3 A at the end of the current commutation is observed with a ringing frequency of 16 MHz, which corresponds to the peak in the EME spectrum in Fig. 9.15c. When the gate current is reduced to 20 mA for $t_{vt}$ and $t_{ct}$ the resulting voltage slope takes 300 ns and the current ringing is reduced from 3 to 1 A. This results in an improved EME as shown in Fig. 9.15c.

In the second setup, the gate current is switched from the initially constant 200 mA setting to 20 mA for the duration of the voltage transition $t_{vt}$, Fig. 9.16a. As expected, the EME is reduced for frequencies of 1 MHz and above, because of the shift in the second break point in the spectrum, Fig. 9.15a. The average EME reduction in this frequency range amounts to 10 dB. At higher frequencies, the spectrum is equal to the one without gate current reduction in $t_{vt}$, because of the emissions generated by the current transition.

To reduce the EME caused by the current transition, the gate current is now reduced to 20 mA only for $t_{ct}$, Fig. 9.16b. With this setup, the EME is reduced by 15–20 dB in the frequency range from 7 to 60 MHz, Fig. 9.15b. Slowing down the current transition time eliminates most of the ringing, caused by the parasitic inductances of the PCB. The switching losses of the four switching setups were also measured and analyzed, Fig. 9.17. As to be expected, the switching losses are highest with both transitions in low gate current mode and lowest with the constant high gate current setting. The transitions with only voltage or only current transition in low gate current mode both show a tradeoff between EME and switching losses. With a reduced gate current setting in the current transition the switching loss

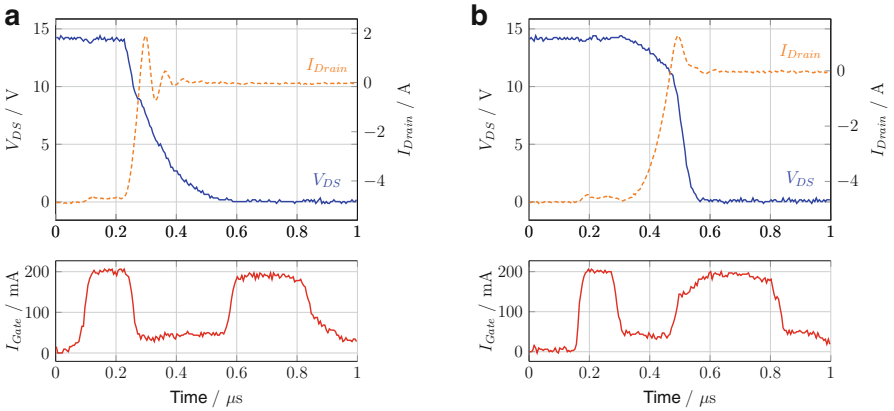


**Fig. 9.16** Turn-on transition with reduced gate current in (**a**) the voltage transition phase $t_{vt}$, (**b**) the current transition phase $t_{ct}$

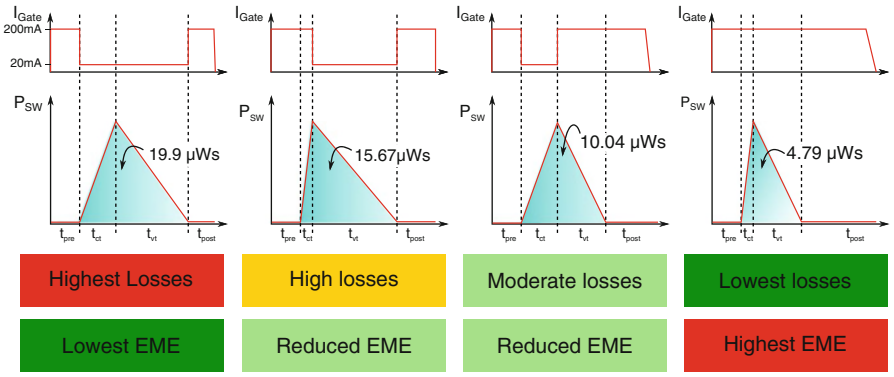


**Fig. 9.17** Switching loss analysis of the four different switching cases

increase is moderate compared to the other options, while still reducing a large part of the EME. In the measurements the broadband EME between 7 and 60 MHz is reduced by up to 20 dB. At the same time the switching losses increased from 4.79 to 10.41 µWs. This results in an increase of 117 % compared to the constant current setting, but is 52 % lower than the switching losses with both transitions slowed down. The trade-off between EME and switching losses can be adjusted by the gate current settings for the individual transitions, if the gate driver can switch between current states fast enough. Reducing the transition speed of the di/dt is often the better trade-off between switching losses and EME, because the current transition is shorter and therefore has less impact on the losses. The decision, which transition to modify, is always highly influenced by the application and board layout. With a variable current gate driver the switching speed can be reduced during the transition, which enables significant EME reduction.

## 9.6 Conclusions

Gate drivers are key circuit blocks with growing importance for various automotive applications. They need to support increasing voltage levels, arising from the introduction of the 48 V board net and HV drive train with >300 V. Compact and cost efficient solutions require fast switching and highly integrated driver solutions. Cascaded drivers achieve high-speed operation and ensure low switching losses in the power stage. The driver itself can be further optimized for low power. In particular, asymmetric sizing eliminates cross-currents in the last driver stage. Fast switching is also enabled by appropriate level shifters. A 50 V level shifter is discussed, which achieves high-speed 3 ns minimum pulses and robust signal transfer for transition slopes of 20 V/ns.

The concept of on-chip high-voltage charge storing enables area-efficient, fully integrated high-voltage gate driver output stages. Combined signal and energy transfer via one single transformer is a way to further reduce size. The growing amount of electronics in cars and faster switching require more effort to meet EMC requirements. By means of a current mode driver, which can change the gate current within 10 ns, the EMC influence of the di/dt and dv/dt transitions have been studied. A trade-off between EMC and switching losses can be achieved.

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