Chapter 5
Blocker and Clock-Jitter Performance in CT ΣΔ ADCs for Consumer Radio Receivers

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5.1 Introduction

WLAN and Cellular communication standards have been the main drivers for low-area, low-power *and* high-performance wideband ADCs. This comes from a requirement for efficient, high-rate wireless data transmissions in a crowded and segmented radio spectrum using large-volume, low-cost, battery-powered handheld devices.

Zero-IF receivers are the most cost-effective radio architecture from a reduced number of high-Q external filter components and a smaller die size. However, a radio transmitting in the vicinity of a zero-IF receiver that is trying to decode a weak, distant signal on the adjacent channel will dominate the receiver's signal budget. ADC performance is a critical factor in a radio's selectivity, as it must convert the in-band received signal with high sensitivity while accommodating a poorly-filtered, large adjacent interferer (blocker) from a lack of high-Q external filters (Fig. 5.1). WLAN and Cellular support a range of channel bandwidths requiring the same sensitivity at similar efficiency across several MIMO antennas and/or aggregated carriers, in order to optimise the use of the spectrum and regulate radio power consumption. This has resulted in an order of magnitude increase in the number of ADCs required to support a radio receiver, and a heavier emphasis towards area-optimised ADC designs for lower-cost consumer radios.

CT ΣΔ ADCs dominated the ADC literature for two decades until SAR ADCs saw an increase in conversion efficiency at the beginning of this decade [1]. However, system-level implications from low-power zero-IF receivers have often been overlooked for either type of ADC in the literature. For instance, unlike CT ΣΔ ADCs, SAR ADCs create challenging anti-aliasing input filtering requirements with

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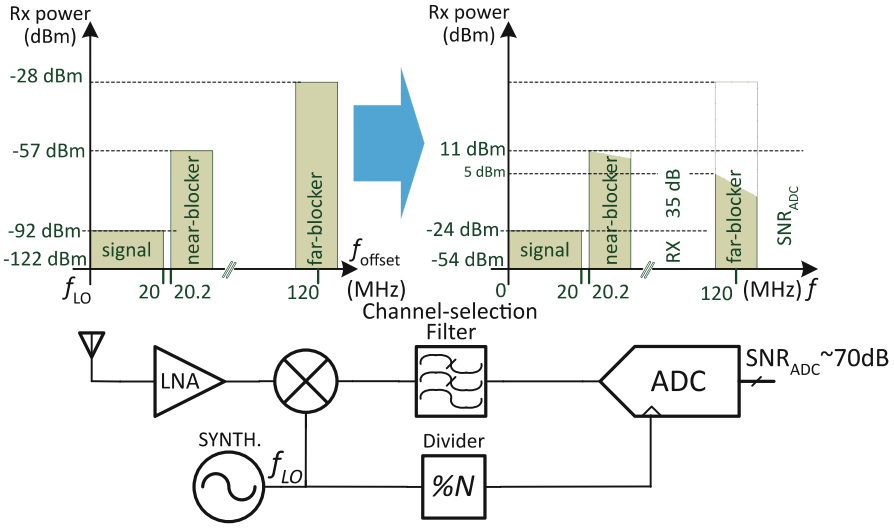

Fig. 5.1 A CT ΣΔ ADC in a zero-IF receiver with radio blockers

power-hungry sampling-input driving loads [2, 3]. Conversely, out-of-band (OOB) gain peaking in the signal transfer function (STF) of CT ΣΔ ADCs impairs zero-IF receiver performance [4]. STF OOB gain is typically seen in CT ΣΔ ADCs with efficient loop-filter architectures. It provides gain to (poorly-filtered) dominant blockers near the edge of band; thereby reducing the available ADC dynamic range for signal in-band.

Another limiting factor for CT ΣΔ ADCs is its higher sensitivity to clock-timing jitter, in the feedback DAC [5]. This is typically managed in CT ΣΔ ADCs by reducing the energy introduced in the feedback DAC from one output sample to the next, i.e. reducing the magnitude of the signal transitions modulating clock jitter. This is typically achieved with either: A larger number of bits in the feedback DAC [5, 6], or by spreading the energy of a single-bit DAC pulse across several time samples, e.g. an FIR DAC [7–10] (or in some cases, both [11]). Single-bit CT ΣΔ ADCs with an FIR DAC result in large area savings when compared to multi-bit DAC implementations with comparable linearity and jitter performance [10], from a simple and compact design. However, this also comes at the cost of (further) OOB STF degradation [12].

Wideband, high conversion-efficiency ADCs that occupy a small area in a zero-IF radio receiver are therefore a balancing act between conflicting requirements. We find that CT ΣΔ ADCs employing feedforward (FF) loop-filter compensation and a single-bit FIR DAC with a flat STF [13] most efficiently accommodate a zero-IF receiver when its requirements on the ADC are carefully reviewed. In this paper, we analyse the practical implications of the choice of ADC architecture in a wide-band, large-volume, low-cost, power-efficient consumer radio receiver to support this conclusion.

5.2 CT ΣΔ ADC STF and Loop Robustness to the FIR Feedback DAC

Loop compensation in high-order ΣΔ ADCs was elegantly resolved through the nesting of 1st order ΣΔ ADCs [14] (coined multiple feedback or FB-compensated), or later on with loop-filter compensating zeroes [15] (coined interpolative, feed-forward or FF-compensated). Lee's interpolative loop-filter results in a more (area and conversion) efficient architecture from a wider first integrator stage unity gain-bandwidth (GBW), fewer (input-referred) noise contributors, a single feedback DAC, and no internal memory. However, accommodating the delay from an FIR DAC in the feedback of a FF-compensated CT ΣΔ ADC to reduce clock jitter noise is challenging from a loop stability perspective. None of the examples of FIR CT ΣΔ ADCs found in the literature prior to [13] are FF-compensated. Instead, they either employ FB-compensation [7–9], or a hybrid FF-FB-compensation [10, 11]. Nesting inner ΣΔ modulators in a FF loop filter eases an FIR DAC CT ΣΔ loop implementation by splitting a noise and delay-sensitive single-feedback DAC FF CT ΣΔ loop (Fig. 5.2a) into a loop-delay sensitive inner CT ΣΔ loop and a noise-sensitive outer CT ΣΔ loop (Fig. 5.2b). A FF-FB-compensated CT ΣΔ ADCs benefits from a low-noise FF front-end and an easier to implement FIR DAC in the loop, but this comes at the area and power cost of a fast inner FB stage.

A FF loop-filter front-end in either FF or FF-FB-compensated CT ΣΔ ADCs, results in OOB STF peaking at near-blocker offset frequencies. The STF of a CT

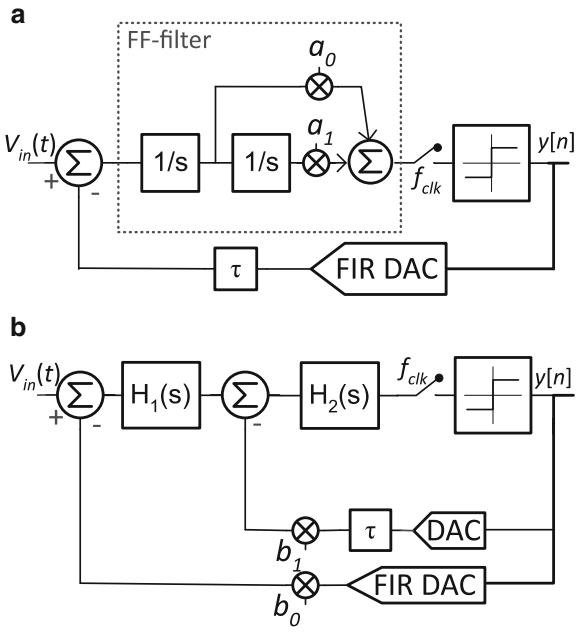

Fig. 5.2 (**a**) **FF CT ΣΔ ADC**; (**b**) **FB CT ΣΔ ADC** when $H_1(s)$ is a single integrator stage and $H_2(s)$ may be one integrator, or one integrator followed by nested FB CT ΣΔ stages; or a hybrid **FF-FB CT ΣΔ ADC** when $H_1(s)$ is a FF-filter and $H_2(s)$ may be one integrator, or one integrator followed by nested FB CT ΣΔ stages

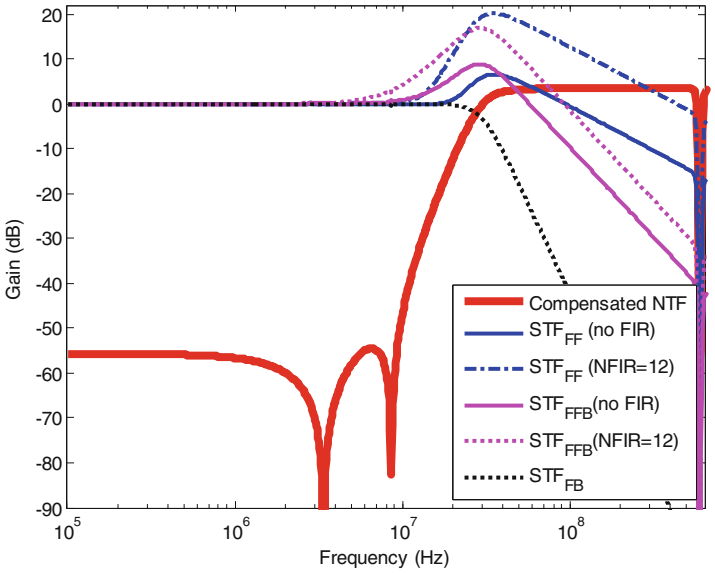

Fig. 5.3 STF in delay-compensated FF, FF-FB and FB CT ΣΔ ADCs with a NRZ DAC and a 12-tap FIR DAC

ΣΔ ADC is defined by [16]:

$$STF\left(\omega\right) = H_a\left(j\omega\right) NTF\left(e^{j\omega}\right), \tag{5.1}$$

where $H_a(s)$ is the transfer function from the input of the CT ΣΔ ADC to the input of its quantiser. The FF-compensation zeroes in $H_a(s)$ resulting from the FF part of the loop filter slow down the gain response roll-off near the 0 dB crossing point for loop stability. This crossing occurs around frequencies where the NTF rises rapidly, resulting in an OOB STF peak near the edge of band from the product of the two, and a degradation in receiver's blocker performance. A FF CT ΣΔ ADC is the most efficient CT ΣΔ to date [17] at 28 fJ/conv.-step but results in a larger OOB STF peak. A FF-FB CT ΣΔ ADC has a more moderate OOB STF peak from fewer stabilising zeroes, at the cost of the power and area impact from one or many additional fast FB loop-filter stages (e.g. 47 fJ/conv.-step in [18]). Finally, FB CT ΣΔ ADCs have a monotonic low-pass filter STF (Fig. 5.3), but are the least efficient.

However, FB CT ΣΔ ADCs may in fact result in an overall more efficient radio, if the OOB STF gain of a FF or FF-FB CT ΣΔ ADC exceeds its conversion efficiency gain over the FB CT ΣΔ ADC, e.g. [19]. This is further emphasised when the STF peak further deteriorates with FIR DAC length and the order of the FF part of the loop-filter (See Fig. 5.3). This effect arises because the low-pass filter response of an FIR DAC in the outer loop causes the FF loop-filter component

Table 5.1 FF CT ΣΔ ADC loop robustness to RC device spread (σ_{RC}) and mismatch (σ_{mis}), measured as a proportion of the deviation from the NTF norm-1(α 1/MSA) with an NRZ & FIR DAC, over 1000 normally distributed samples

	NRZ DAC		2-tap FIR DAC		12-tap FIR DAC	
$(3\sigma_{mis}, 3\sigma_{RC})$	$\mu_{norm\text{-}1}$	$\sigma_{norm\text{-}1}$	$\mu_{norm\text{-}1}$	$\sigma_{norm\text{-}1}$	$\mu_{norm\text{-}1}$	$\sigma_{norm\text{-}1}$
(0.5, 25 %)	1.0126	0.07	1.037	0.13	1.067	0.15
(0.5, 2 %)	1.0004	0.0098	1.0006	0.01015	1.0017	0.01
(0.5, 2 %) + σ_{GBW}	1.001	0.019	1.0019	0.0248	1.0025	0.0247

The ($+\sigma_{GBW}$) term in the last row includes an additional compensated $0.45/f_{clk}$ amplifier GBW-dependent delay, spread ±30 % (3σ) over its nominal value

(and $H_a(s)$) gain to increase at higher frequencies to compensate for the FIR loss, resulting in a higher OOB STF peak. This was reported in [12] for FF-FB CT ΣΔ ADCs and indicates a compromise between FIR DAC length and receiver blocker performance. Figure 5.3 also incorporates FF CT ΣΔ ADCs with an FIR DAC. Note that all CT ΣΔ ADCs inherently provide some amount of filtering above a certain frequency, particularly around Nyquist.

Another important factor of an FIR DAC in CT ΣΔ ADCs is its loop stability and robustness. Reference [12] provides an insight into the robustness of a FIR DAC FF-FB CT ΣΔ loop against RC spread. However, its observations exclude the impact of component mismatch on the NTF, or STF.

Table 5.1 reports the robustness of an FIR DAC FF-compensated CT ΣΔ ADC against RC process spread and component mismatch, measured in terms of the proportional impact on the nominal $norm_1$ of the (loop) noise transfer function (NTF), i.e. the sum of the absolute values of the samples of the impulse response of the NTF or $\sum_{n=0}^{\infty} |ntf\,[n]|$. $norm_1$ is a measure of the signal range quantisation noise occupies in a CT ΣΔ ADC loop, and by extension, the signal range left for the input signal. It is therefore a measure of the (inverse of the) maximum-stable amplitude (or MSA) of a ΣΔ converter. Reference [12] reports that a typical ±25 % (3σ) RC spread does not adversely affect the MSA of a 12-tap FIR DAC FF-FB-compensated CT ΣΔ ADC, any more than a NRZ DAC FF-FB-compensated CT ΣΔ ADC would. This is in line with the observed impact from RC spread on the mean value of the $norm_1$, $\mu_{norm\text{-}1}$, in row (0.5, 25 %) of Table 5.1, for a FF-compensated CT ΣΔ ADC with an FIR and an NRZ DAC. However, the standard deviation, $\sigma_{norm\text{-}1}$, doubles from 7 to 15 % from a NRZ DAC to a 12-tap FIR DAC, when a 25 % (3σ) RC spread and a 2 % (3σ) RC component mismatch are considered. A CT ΣΔ ADC with an un-calibrated ±25 % RC process spread would therefore have to operate within 55 % of its MSA such that it does not overload across a typical 3σ RC mismatch found in large-volume production in a relatively small area on the die.

Table 5.1 indicates that RC calibration (e.g. with a 2 % error) is required to keep ADC performance and yield degradation acceptably low in production. It also demonstrates in row (0.5, 2 %) + σ_{GBW} that an FF CT ΣΔ ADC with an FIR DAC

is robust in terms of loop stability (with RC calibration), even when a 30 % process spread over a power-optimised $0.45/f_{clk}$ amplifier GBW delay-compensation such as [13] is included.

5.3 Filtering CT ΣΔ ADCs

From Sect. 5.2, compromising CT ΣΔ ADC performance or conversion efficiency for a more desirable STF may in fact result in a more efficient radio receiver, albeit at a lower stand-alone ADC conversion efficiency.

Some publications aim to absorb the channel-selection filter in Fig. 5.1 into a (monotonic low-pass STF) FB CT ΣΔ ADC [19, 20]. Reference [21] also tackles FF-FB CT ΣΔ ADC STF OOB peaking with an embedded filter within the loop. Other publications attempt to reduce STF OOB peaking in FF CT ΣΔ ADC architectures by turning the peaky STF into a monotonic low-pass filter STF response through input feedforward coefficients [22]. However, there are a number of problems with the overall premise of filtering in a CT ΣΔ ADC STF.

5.3.1 In-Band Conversion Efficiency Degradation from Filtering in CT ΣΔs

Embedding the channel-selection filter within a FB or a FF-FB CT ΣΔ ADC results in a lower overall power than a channel-selection filter followed by a FB or a FF-FB CT ΣΔ ADC. From [21], we estimate that embedding the filter in a FF-FB CT ΣΔ ADC results in a ∼50 % reduction in filter power, and a ∼20 % reduction in ADC power. This is the result of the first stage of the FF-FB CT ΣΔ ADC loop-filter attenuating the embedded filter noise and linearity contributions, in addition to a lower ADC noise contribution to the overall noise budget from fewer stages in the receiver, e.g. a higher (filter-embedded) FF-FB CT ΣΔ ADC noise achieves the same noise overall than a channel-selection filter followed by an ADC. However, the state-of-the-art filtering (FB or) FB-FF CT ΣΔ ADC [20] is much less efficient *in-band* than a state-of-the-art SAR ADC [23] that includes a channel-selection filter [24], and an input buffer with anti-aliasing [25], e.g. 256 fJ/conv.-step for [20] versus 76 fJ/conv.-step for [23] and [24] with [25]. This may be surprising when SAR ADCs, albeit ∼3× to ∼7× more efficient standalone ADCs than CT ΣΔ ADCs, are known to have very demanding anti-alias and input driving requirements [2, 3, 25], i.e. requiring an additional stage of filtering in the radio for anti-aliasing and a relatively large multiplier of the SAR ADC power to drive it from a buffer at low-distortion and noise.

Signal filtering at the ADC requires heavy processing of input signal at every stage of a CT ΣΔ ADC loop filter; may that be by injecting input signal from the

output of the ADC (e.g. with FB loop-filter stages), or by injecting input signal using feedforward coefficients directly from the ADC input (e.g., [22]). A stand-alone active-filter is more efficient at filtering blockers than a CT ΣΔ ADC when it does not have to spend dynamic range in each Op-Amp processing quantisation noise, while a CT ΣΔ ADC is most efficient *in-band* when it does not have to filter the input signal (monotonically). The power saving from embedding a filter within a FB or FF-FB CT ΣΔ ADC should therefore be weighed against what can be achieved with a state-of-the-art CT ΣΔ ADC and channel-selection filter.

One may compare the embedded-filter FB or FF-FB CT ΣΔ ADCs to the most efficient (FF) CT ΣΔ ADC [17] at 28 fJ/conv.-step with an input filter. However, the STF OOB in a FF CT ΣΔ ADC typically peaks near the edge of band and requires a sharp OOB filter frequency response [26]. The input-filter requirements for a FF CT ΣΔ ADC are comparable to those of a 2.5 times oversampled SAR ADC anti-aliasing filter, but at a much lower stand-alone in-band ADC conversion efficiency (sub-10 fJ/conv.-step [23] vs 28 fJ/conv.-step [17]) and an inability to reuse the existing channel-selection filter that already exists in the radio (Fig. 5.1) [13]. Reference [4] proposes inserting a low-pass filter and its inverse in a FF CT ΣΔ ADC to achieve a low-pass STF in a FF CT ΣΔ ADC and deal with the STF peak with no impact on the loop-filter, but this comes at the cost of an impaired loop stability at high clock frequencies.

Another important factor to consider with filtering ADCs is the sensitivity of the STF to process parameters [27], when an FIR DAC is included. [27, 28] propose the dual-feedback architecture to reduce sensitivity to process mismatch for a NRZ DAC. Figure 5.4 shows the sensitivity of a low-pass STF in a FF CT ΣΔ ADC to RC component mismatch with a short and a long FIR DAC. The STF reaches a large OOB gain peak near the edge of band with a long FIR DAC that will impact in-band DR in the radio when component mismatch is considered.

5.3.2 ADC Out-of-Band Performance

Filtering ADCs tend to provide better OOB linearity-intermodulation performance, e.g. OOB IIP3, when compared to a cascaded filter stage with an ADC stage. This is a result of a blocker filter with gain embedded within the CT ΣΔ ADC loop. However, OOB linearity is not equally critical across the radio receiver chain.

OOB non-linearity in the RF stages of a radio cause a loss in selectivity expressed as cross-modulation and/or desensitisation, from the intermodulation product of blockers falling in the channel of interest. Deterministic signals are not spectrally efficient, so modern radios transmit noise-like signals with a high peak-to-average ratio that is in the order of 12 dB for OFDM in WLAN or 10 dB for WCDMA in cellular. Unlike signals at RF stages of the receiver that are defined as *rms*, ADC performance is defined relative to a hard and deterministic limit: supply or digital full-scale at 0 dBFS. OFDM or WCDMA signals are backed-off by their peak-to-average ratio to accommodate their peak below 0 dBFS at the ADC output

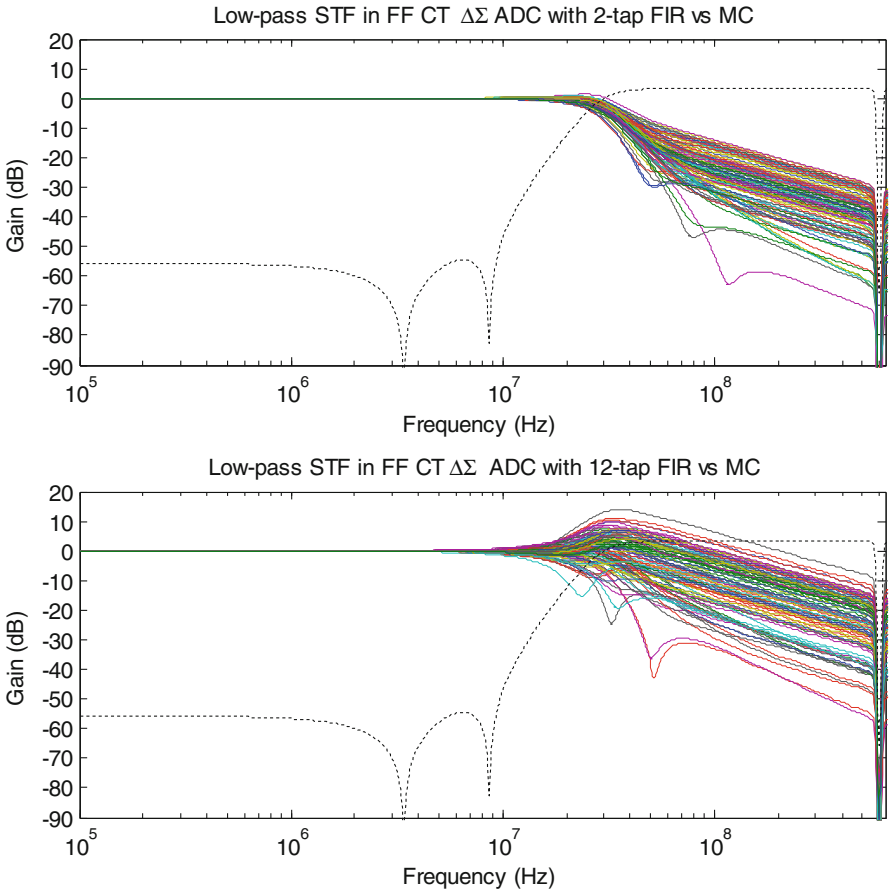

Fig. 5.4 STF robustness in a delay-compensated FF with a low-pass STF with 100 MC samples and RC calibration

and avoid clipping. OOB linearity therefore has a 10–12 dB less weight than in-band dynamic range in the ADC of a modern radio. An OOB-linearity figure-of-merit typically used to characterise filters is often used to compare between filtering ADC performance and a filter followed by an ADC, e.g. $FOM_{filt} = P/\left(N\ BW\ 10^{2/3(IIP3-P_{noise})/10}\right)$ in [19–21]. A more accurate comparison would weigh OOB linearity, e.g. IIP_3, lower than in-band noise, P_{noise}, by the peak-to-average ratio back-off used in the receiver. It's worth noting that FOM_{filt} is infinitely less efficient for a stand-alone non-filtering ADC, i.e. $N = 0$ in FOM_{filt}, than any filtering ADC when in fact OOB ADC linearity and ADC filtering play a secondary role in a radio receiver.

In summary, conversion efficiency and jitter-noise sensitivity (through FIR DAC length) in CT $\Sigma\Delta$ ADCs with a FF loop filter component are directly correlated with

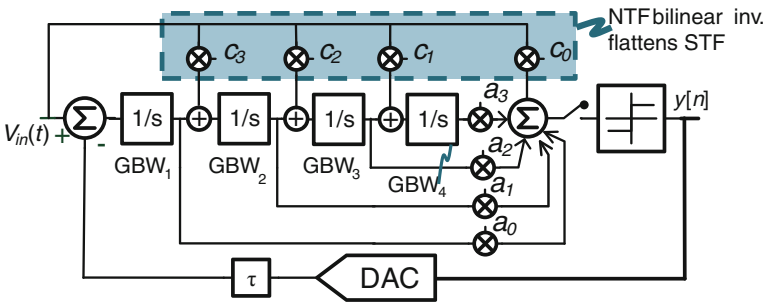

Fig. 5.5 A FF CT ΣΔ ADC with flat STF from input feedforward coefficients, C_x

radio-blocker performance degradation in a radio in terms of dynamic range in-band with an increasing OOB STF peak. However, the OOB IIP3 improvement gained from ADC OOB filtering rates much lower than in-band ADC performance due to the peak-to-average ratio back-off in OFDM or WCDMA signals. Fundamentally, a CT ΣΔ ADC STF should not provide OOB gain, while achieving monotonic filtering at the STF comes at a higher cost for a low benefit. A flat STF in an FF CT ΣΔ ADC has a lower impact on FF loop-filter scaling with a maximised ADC conversion efficiency and the least aggressive insertion possible of signal from the input, with the same blocker performance degradation of in-band noise than any other block driving the ADC.

5.4 Flat STF CT Σ Δ ADCs

A flat STF in a FF CT ΣΔ ADC may be achieved by turning $H_a(s)$ in (5.1) into the bilinear inverse of the NTF [29] using feedforward coefficients from the ADC input (C_x in Fig. 5.5).

Figure 5.6 indicates that a flat STF is more robust to component mismatch with an FIR DAC than a low-pass response in Fig. 5.4. This is due to the fact the feedforward coefficients are two orders of magnitude smaller than, say, a low-pass STF in a FF CT ΣΔ ADC. One valid observation is the reduced anti-aliasing attenuation in the STF of a flat STF, when compared to the inherent STF of CT ΣΔ ADCs or a filtering CT ΣΔ ADCs (see Fig. 5.7).

However, a small RC at the ADC resistive input can provide significant additional signal attenuation around Nyquist at ∼30 times oversampling. The ADC internal noise (from a reference or through coupling) present around half the sampling clock will see as much attenuation as there is with quantisation noise before folding in-band. Finally, the spread in attenuation around Nyquist due to mismatch reduces its practical use for a low-pass STF when compared to a flat STF, with a more modest difference in anti-aliasing when considering the worse-case scenario.

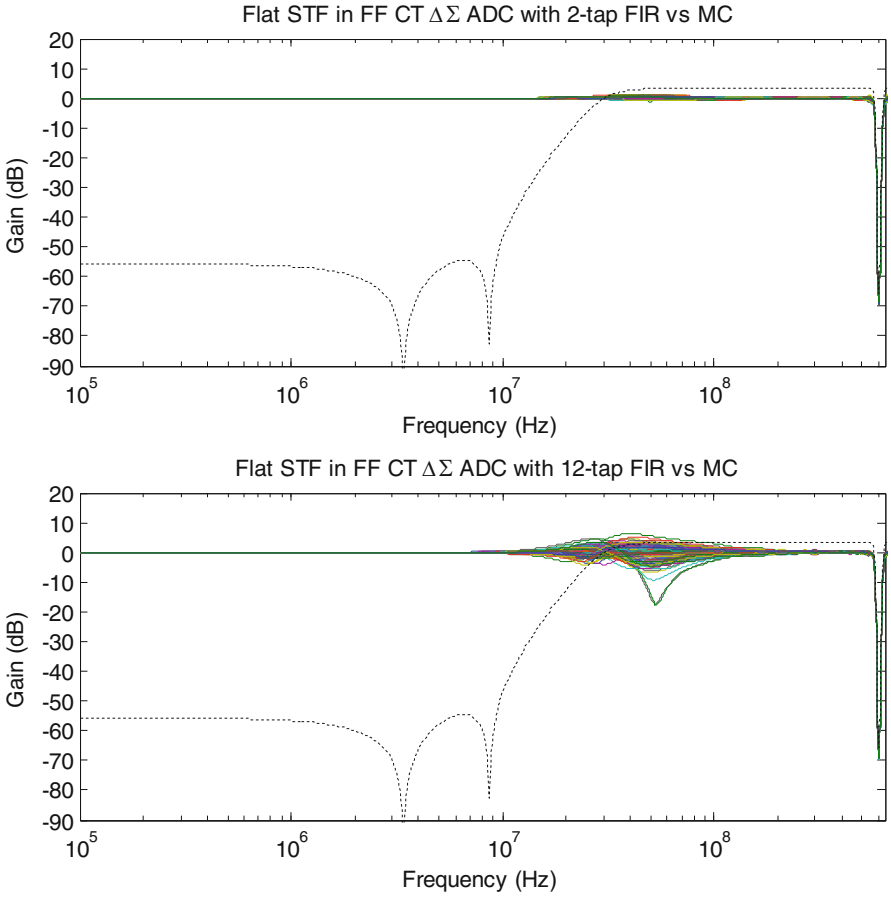

Fig. 5.6 STF robustness in a delay-compensated FF with a flat STF with 100 MC samples and RC calibration. Note that anti-aliasing is no worse than in-band quantisation noise with a low sensitivity

Table 5.2 captures the blocker degradation spread from OOB STF variation in the low-pass STF of Fig. 5.4 alongside the flat STF of Fig. 5.5 shown in Fig. 5.6, against the same MC RC-calibrated conditions than in Table 5.1 but over 100 samples. This quantifies how robust a flat STF is when compared to a low-pass STF in a FF CT $\Sigma\Delta$ ADC. The impact of component mismatch on radio performance is measured as the 3σ OOB STF peak the ADC may to achieve in large-volume production and is denoted as a peak OOB gain blocker margin. This in return defines the margin that should be allocated for in-band dynamic range loss from OOB blocker gain across process and mismatch. Table 5.1 shows that a 12-tap FIR FF CT $\Sigma\Delta$ ADC is robust

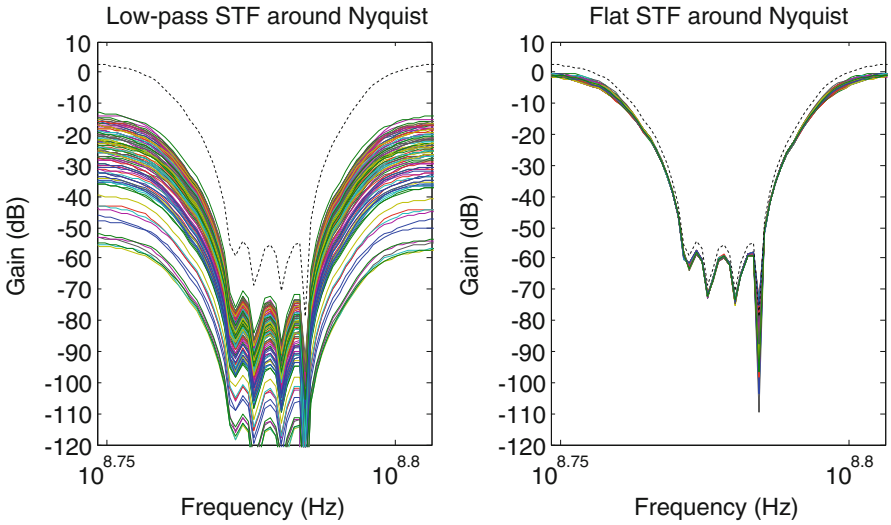

Fig. 5.7 Close-up around Nyquist, for a low-pass and flat STF with a 12 tap FIR

Table 5.2 STF OOB peak robustness MC over 100 normally distributed samples, for a FF CT ΣΔ ADC with a flat STF and a low-pass STF and GBW delay compensation

	2-tap FIR DAC		12-tap FIR DAC	
	μ_{peak} (dB)	σ_{peak} (dB)	μ_{peak} (dB)	σ_{peak} (dB)
Low-pass STF	**0.69 dB**		**12.28 dB**	
Peak OOB gain blocker margin	0.09	0.2	3.06	3.13
Flat STF	**1.17 dB**		**6.3 dB**	
Peak OOB gain blocker margin	0.45	0.24	2.16	1.38

in terms of loop performance and stability. However, a 12-tap FIR DAC results in a peak OOB over mismatch that is equivalent to a 6 dB loss in ADC conversion efficiency in a radio in production. This is a significant degradation.

It's therefore important to quantify how long an FIR has to be with a representative clock jitter spectrum with a flat STF FIR DAC FF CT ΣΔ ADC.

5.5 Clock Jitter in CT ΣΔ ADCs

The clock available in a WLAN receiver must have an integrated phase noise that is at least 0.8° for 64 QAM, i.e. 0.92 ps of rms jitter at 2.4 GHz (in a cellular radio, this is closer to 0.5 ps). If we apply a white 0.92 ps (rms) jitter to a single-bit FF CT ΣΔ ADC with a NRZ DAC, where jitter is subject to $NRZ(z) = \left(1 - z^{-1}\right)$ [5], the ADC noise degrades by 10 dB in Fig. 5.8.

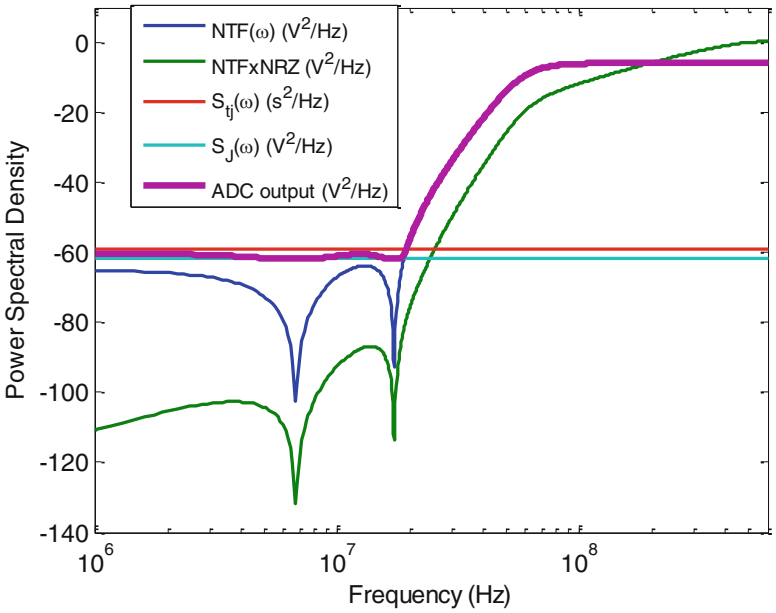

Fig. 5.8 Jitter degradation in a single-bit FF CT ΣΔ ADC with a NRZ DAC and 0.8% integrated phase noise

If we apply the same jitter noise to single-bit FF CT ΣΔ ADC with a 2-tap FIR DAC, jitter should be subject to $FIR(z) = \left(1 + z^{-1}\right)/2$ [8]. However, on should highlight the fact the response of jitter to the FIR is in fact: $FIR(z) = \left(1 - z^{-1}\right)/2$ [13], due to the strong correlation between DAC output noise transitions from a common clock noise source. Figure 5.9 shows a 3 dB degradation in the ADC noise floor from clock jitter when the FIR is included.

This would indicate either a longer FIR or a multi-bit ADC is required, at the cost of blocker performance degradation or area. However, clock jitter is seldom white. It is coloured. In the literature it is assumed a white clock-jitter or a white-noise equivalent of coloured jitter to simplify the analysis [13]. However, this results in a pessimistic noise jitter contribution.

Figure 5.10 shows a jitter response to a 0.92 ps (rms) coloured jitter with a 2-tap FIR DAC. The jitter spectrum is based on a simplified 200 kHz BW PLL mask for a WLAN radio that integrates to 0.92 ps (rms) of jitter.

A 2-tap FIR DAC results in a non-dominant jitter noise in a radio when a more realistic jitter spectrum shape is considered with the same integrated jitter.

Blockers will also modulate jitter. Figure 5.11 shows the effect of a blocker modulating jitter noise. The noise floor increases by 8 dB, but remains 18 dB below the noise floor, resulting in a robust loop with a flat STF response for a modern radio.

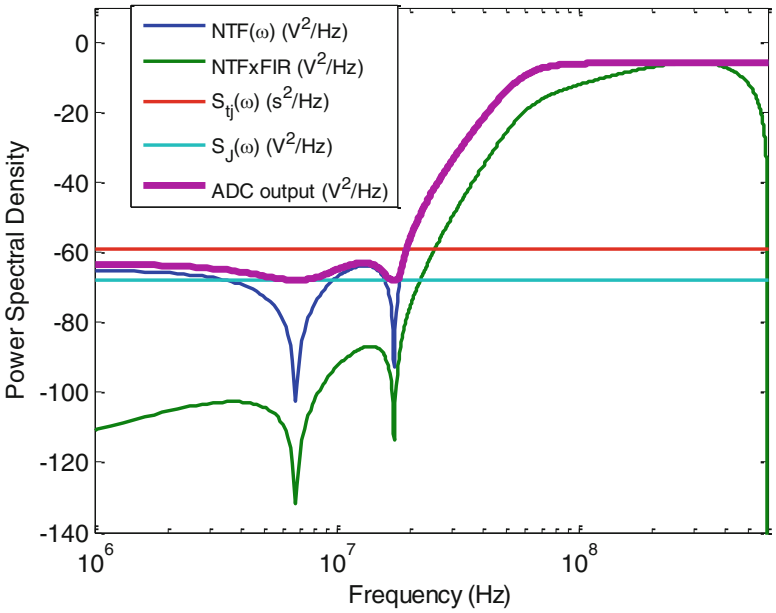

Fig. 5.9 Jitter degradation in a single-bit FF CT ΣΔ ADC with a 2-tap FIR DAC with 0.92 ps (rms) white noise

5.6 Conclusion

FF CT ΣΔ ADCs with an FIR DAC are the most area and conversion efficient CT ΣΔ ADC implementation but are more sensitive to FIR length in terms of STF OOB peaking and stability. It has been shown that a long FIR may be stabilised but that a short FIR is sufficient when the colour of typical radio clock jitter spectrum is considered. A flat STF is the optimal compromise between CT ΣΔ ADC conversion efficiency degradation and receiver blocker performance degradation, when OFDM back-off is taken into account in OOB ADC linearity requirements. On the other hand, filtering at the ADC results in a large area and FOM impact for a low return, especially when compared to a state-of-the-art filter driving a state-of-the-art CT ΣΔ ADC with a flat STF. SAR ADC converter efficiency in a radio suffers from anti-aliasing and sampling input buffer requirements that burn more power than the SAR ADC itself, and result in a poorer overall conversion efficiency in a radio, at 76 fJ/conv.-step vs 67 fJ/conv.-step in [13].

This paper confirms that a single-bit FF CT ΣΔ ADC with a short FIR DAC in the feedback and a flat STF is the most power and area efficient implementation in a modern receiver, when the wider system-level factors of a large-volume consumer radio device are considered.

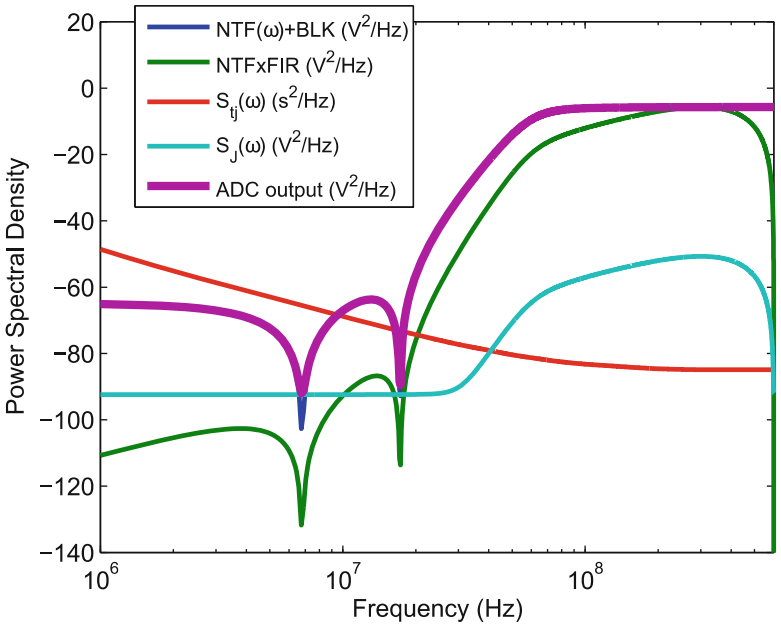

Fig. 5.10 Jitter degradation in a single-bit FF CT ΣΔ ADC with a 2-tap FIR DAC with shaped 0.92 ps (rms) jitter

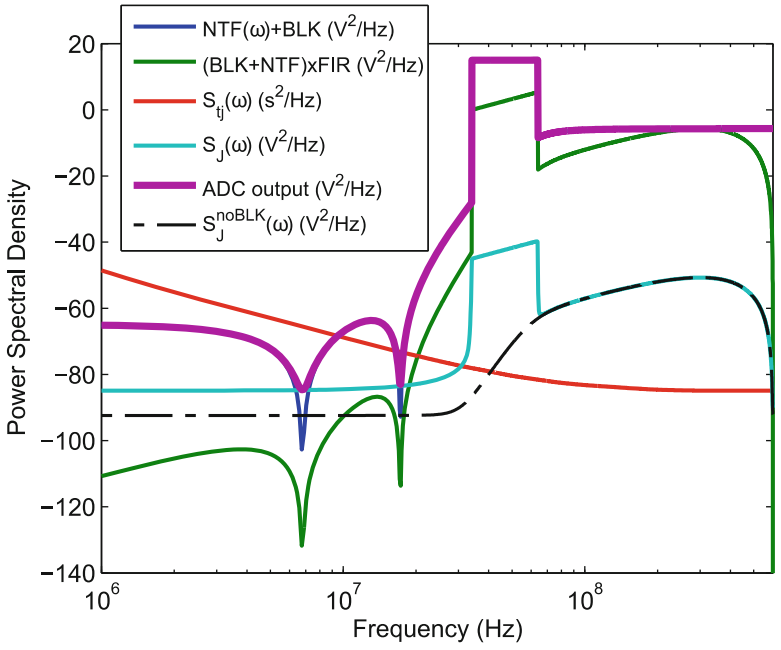

Fig. 5.11 Jitter degradation in a single-bit FF CT ΣΔ ADC with a 2-tap FIR DAC with shaped 0.92 ps (rms) jitter and a blocker

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