Chapter 18
An Ultra-Low-Power Electrostatic Energy Harvester Interface

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18.1 Introduction

Solid-state electronics develop enormously every year, thanks not only to circuit design innovation, but also to the development of better technologies. All this allows to constantly reduce power consumption of electronic systems, while keeping the other performance metrics almost unchanged. In this scenario, energy harvesting is becoming more and more interesting as it allows to reduce the cost of an application by avoiding a periodic replacement of the batteries or by reducing their size, or even allowing the implementation of battery-less systems. There are many environmental energy sources that can be exploited for these purposes (e.g. light, temperature gradient, mechanical vibrations, electromagnetic). The choice of the best source of energy clearly depends on the application. Usually the most abundant form of energy is chosen, even if there are exceptions due to system size and shape.

The focus of this chapter is in the field of industrial machines and vehicle monitoring, in which the sensing electronic systems are positioned usually in inaccessible places (the moving parts), where the cabling can be expensive or almost impossible. The most abundant form of energy in the moving parts of machines is clearly mechanical and so vibrational harvesters are chosen in these systems. There are many types of vibrational harvesters: piezoelectric, electrostatic, magnetic. This chapter will focus on the interfacing of electrostatic harvesters. Basically, these devices are charged capacitors with one plate fixed (or just connected to a bigger

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inertial mass) and the other moving because of the environmental accelerations. In [1], a circuit capable to both bias the variable capacitor and extract power from its movement is proposed. A drawback of this design is that part of the power extracted is used for the polarization of the capacitor. Additionally, this design strategy limits the capacitor polarization voltages to the maximum voltage ratings of the chosen IC manufacturing technology, which most of the times is lower than the polarization voltage for the harvester itself. A solution for scavenging more efficiently energy from the environmental vibrations consists in building a partially isolated structure, in which the variable capacitor is pre-charged with a certain potential and then isolated from the outside world. In this case, the charged electrode is called electret and the harvesters fabricated in this way are denoted as electret-based electrostatic energy harvesters. Recently, this type of harvesters attracted quite some attention, thanks to their capability to generate a large amount of power, even at low accelerations [2]. Unfortunately, these harvesters have extremely large internal impedances, making challenging the design of interfacing circuits for efficient power extraction. In particular, those circuits need to be at the same time ultra-low-power and resistant to several tens of Volts applied on their inputs. In [3] an interfacing circuit working with an input voltage range between 5 and 60 V has been proposed. The main disadvantage of that circuit was mainly the power consumption, as it was not working under 25 μW of available power.

18.2 Open-Loop Inductive Buck Converter at Low Available Powers

Considering the large voltage ranges required by the applications, the best choice is an inductive converter. As shown in Fig. 18.1a, the basic structure of an inductive DC-DC buck converter is consisting of a switch connected to the input and a diode (implemented with passives or, more often, with active circuits). Given the low available power in energy harvesting applications, the converter should be used in Discontinuous Conduction Mode (DCM), meaning that during the period T there will be some time in which the inductor current will be constant and equal to zero.

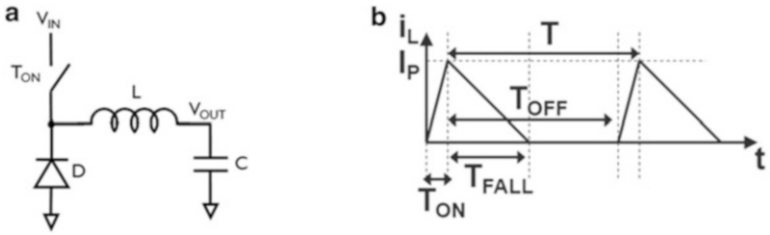

Fig. 18.1 Basic implementation of a DC-DC buck converter (**a**) and inductor current in discontinuous conduction mode (**b**)

This is particularly efficient at low power levels because many control circuits can be turned off when there is no conduction of current to the load. A typical waveform in DCM is shown in Fig. 18.1b. Assuming that the input voltage of the converter is almost constant (the input capacitor has to be large enough), we can easily calculate the input resistance of the converter if operating in open-loop (as charger and not as voltage regulator) by calculating the ratio of the input voltage over the average inductor current flowing during the T_{ON} time (when the switch is ON).

In particular, we get the following expression:

$$R_{IN} = \frac{2LTV_{IN}}{T_{ON}^2 (V_{IN} - V_{OUT})} \tag{18.1}$$

Note that, for energy harvesting purposes, the input resistance needs to match the source resistance of the harvester R_S. This means that a Maximum Power Point Tracking (MPPT) algorithm needs to be implemented in order to achieve power matching. So, in a Pulse Frequency Modulation (PFM) scheme, the period T would have to be modified according to the following law:

$$T = \frac{R_S T_{ON}^2 (V_{IN} - V_{OUT})}{2LV_{IN}} \tag{18.2}$$

As it can be easily recognized, if the input voltage gets close to the output voltage, the period T needs to be decreased by the MPPT algorithm in order to efficiently extract power from the harvester. Assuming that most of the control circuit consumption happens during the conduction time and considering that the conduction time is T_{ON}*V_{IN}/V_{OUT}, the total power consumption is then given by:

$$P_{CTRL} = P_Q + k_1 \frac{T_{ON}}{T} \frac{V_{IN}}{V_{OUT}} + \frac{k_2}{T} \tag{18.3}$$

where P_Q is the quiescent power, k_1 is a constant equal to the power consumed by the blocks turned ON during the conduction phase and k_2 a constant equal to the energy dynamic losses due to the switching operations. By substituting (18.2) in (18.3), we obtain:

$$P_{CTRL} = P_Q + \left(\frac{k_1 T_{ON} V_{IN}}{V_{OUT}} + k_2 \right) \frac{2V_{IN}L}{(V_{IN} - V_{OUT}) T_{ON}^2 R_S} \tag{18.4}$$

Calculating the limit of (18.4) for V_{IN} tending to V_{OUT}, we get that P_{CTRL} tends to infinite. So, when the available power from the harvester decreases, the control power increases, reducing dramatically the converter efficiency. A similar reasoning can be applied to PWM schemes. In this case, the control power results:

$$P_{CTRL} = P_Q + \frac{k_1 V_{IN}}{V_{OUT} T} \sqrt{\frac{2V_{IN}TL}{R_S (V_{IN} - V_{OUT})}} + \frac{k_2}{T} \tag{18.5}$$

It can be appreciated that also in PWM schemes the control power tends to go to infinity when the available power tends to zero. Equations (18.4) and (18.5) represent a problem that needs to be solved in order to lower significantly the power consumption of electrostatic harvester interfaces.

18.3 Hybrid Modulation Scheme

Both PFM and PWM modulation schemes have the characteristic of varying only one parameter: T_{ON} or T. However, from equation (18.1) we can see that the period T is proportional to $T_{ON}{}^2$. This means that, while maintaining resistance matching, the period T could be increased of α^2 if T_{ON} is increased of a factor α. Of course, T_{ON} is not a parameter that we can freely choose, because it defines the peak current in the inductor I_P. Since, for a given power train, an optimal peak current for maximizing energy efficiency exists, T_{ON} cannot be increased ad libitum in order to reduce the operating frequency. A good compromise is easily found and consists in fixing the peak current in the inductor to a value close to its optimal value. This means that T_{ON} is chosen at each period in order to keep the peak current constant and then the period T can be calculated:

$$T = \frac{R_S I_P^2 L}{2V_{IN}\left(V_{IN} - V_{OUT}\right)} \tag{18.6}$$

In this case, the period tends to infinity for input voltages close to the output voltage. To verify that this approach solves the problem, we can calculate the power dissipation of the control circuits:

$$P_{CTRL} = P_Q + \frac{2V_{IN}\left(V_{IN} - V_{OUT}\right)}{I_P^2 L R_S}\left[\frac{k_1 V_{IN} L I_P}{V_{OUT}\left(V_{IN} - V_{OUT}\right)} + k_2\right] \tag{18.7}$$

The limit of P_{CTRL} for V_{IN} tending to V_{OUT} is then equal to:

$$\lim_{V_{IN} \to V_{OUT}} P_{CTRL} = P_Q + \frac{2V_{IN}^2 k_1}{I_P R_S V_{OUT}} \tag{18.8}$$

Notice that now the control power tends to P_Q when the available power ($V_{IN}{}^2/4R_S$) tends to zero.

18.3.1 Proposed Implementation

The design architecture needs then to generate the proper period T at each cycle, following equation (18.6). Given the relative complexity of equation (18.6), it may seem hard to do it in a simple way. In reality, the problem can be solved pretty easily by using the system shown in Fig. 18.2a.

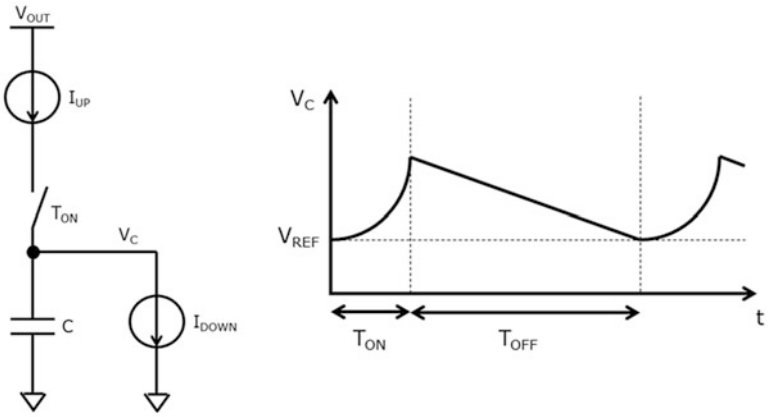

Fig. 18.2 Proposed implementation of the timing control circuit (**a**) and its waveform (**b**)

Assuming now that the conversion period starts when the capacitor voltage V_C becomes lower than a certain reference V_{REF}, we get:

$$T = \frac{\int_0^{T_{ON}} I_{UP}(t)dt}{I_{DOWN}} \tag{18.9}$$

Imposing that (18.9) needs to be equal to (18.2), we get that I_{UP} needs to be a scaled copy of the inductor current and I_{DOWN} a current proportional to the input voltage:

$$\begin{cases} I_{UP} = \frac{i_L}{N} = \frac{(V_{IN}-V_{OUT})}{NL}t \\ I_{DOWN} = k_{MPPT}V_{IN} \end{cases} \tag{18.10}$$

where N is the scaling factor of the inductor current copy and k_{MPPT} is a factor used by the MPPT algorithm in order to change the input resistance of the converter. In particular the input resistance will result equal to $1/(N*k_{MPPT})$. Finally, note that, for fixed values of input and output voltages, I_{UP} increases linearly in time during the interval of time T_{ON} and I_{DOWN} is constant. Therefore, the capacitor voltage V_C will behave like depicted in Fig. 18.2b.

18.3.2 Circuit Implementation

The proposed system architecture is shown in Fig. 18.3, with the integrated blocks highlighted in grey and the die photo on top. Excluding harvester, rectifier and load, there are 4 external components: 2 decoupling capacitors ($C_{IN} = 100$ nF and C_{OUT} larger than 10 μF), 1 inductor ($L = 10$ mH) and 2 resistors ($R_{DC} = 10$ GΩ and $R_{BIAS} = 100$ MΩ).

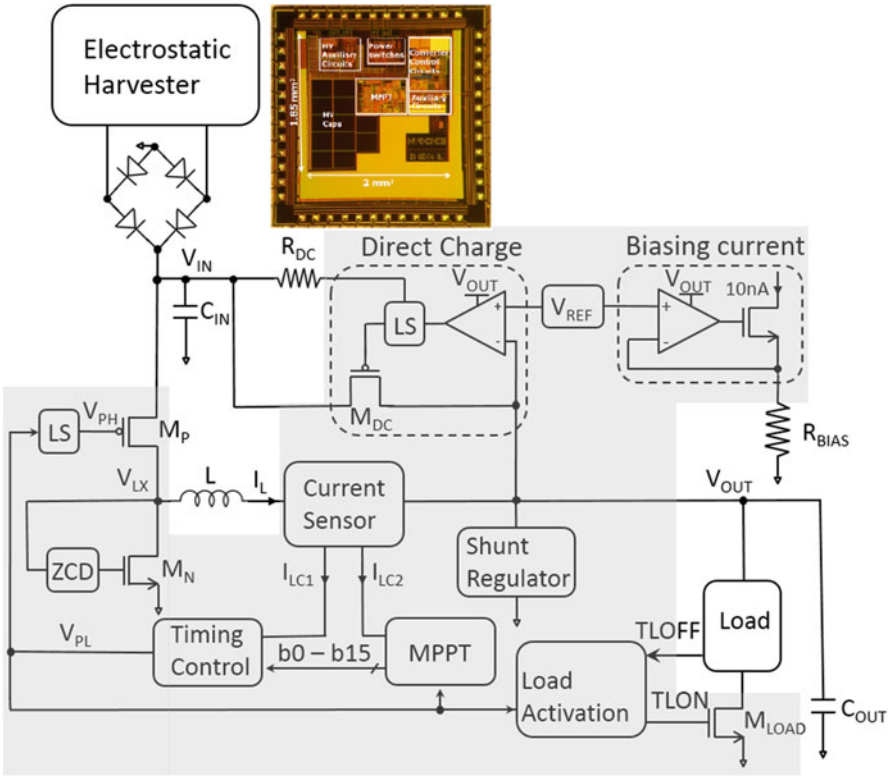

Fig. 18.3 Proposed system architecture and die photo

The resistors R_{BIAS} and R_{DC} are used respectively for defining a bias current of about 10 nA and for providing a basic bias current in start-up conditions. In particular, this start-up bias current is used by a level shifter which shorts the input to the output. All the control mechanisms are based on inductor current sensing. In particular, the sensed copy of the inductor current is used for the timing control, the peak current control and also for the MPPT algorithm, which has to calculate the output power variation. Additionally, in order to allow battery-less operation, the system includes also a shunt regulator and a smart load activation circuit, which connects the load to the output and allows the load to request to be disconnected after it has performed all its operations.

Figure 18.4 shows the circuit implementation of the timing control block. The copy of the inductor current I_{LC1} is mirrored into transistor M_{P2} and integrated by the capacitor C. Simultaneously, the inductor current is also mirrored by M_{P7}, with the aim to perform the peak current control and define the ON-time T_{ON} with the voltage V_{PLN}. As indicated in the previous sub-section, the down current has to be proportional to the input voltage V_{IN}. In order to avoid additional external components, the input voltage is sensed in an indirect way: the inductor current

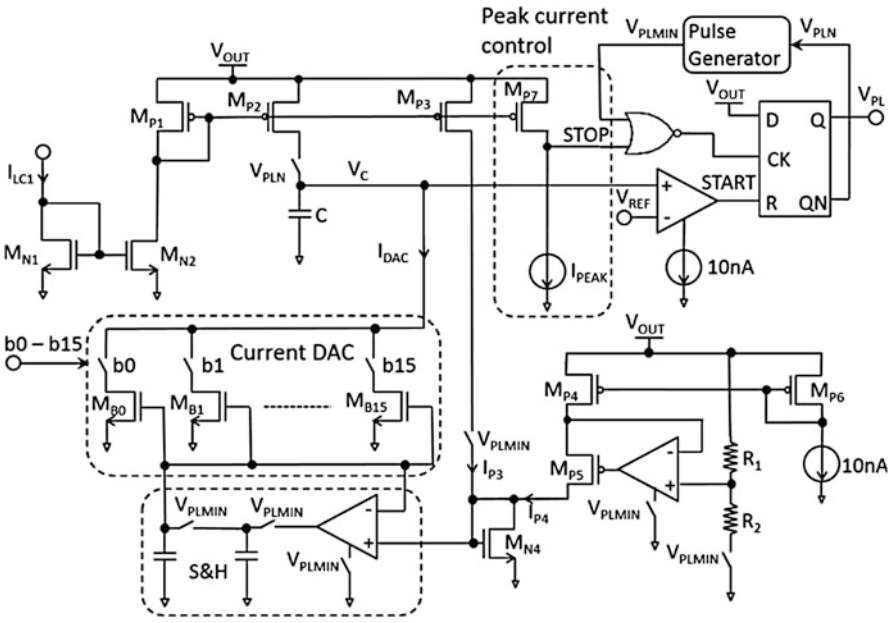

Fig. 18.4 Proposed timing control block

(proportional to V_{IN}-V_{OUT}) is mirrored by M_{P3} and summed to another current I_{P4} proportional just to V_{OUT}. The resulting diode voltage of M_{N4} is then sampled and used to bias a current DAC, which receives as input the MPPT settings b0-b15.

18.3.3 Measurements

The chip has been fabricated in 0.25 μm BCD technology, and in particular using a flavor with 60 V-tolerant MOSFETs. The characterization has been carried out for various values of source resistance, between 500 kΩ and 25 MΩ. The MPPT efficiency (input power over available power) and the end-to-end efficiency (output power over available power) are shown respectively in Figs. 18.5 and 18.6.

Focusing on the left side of the previous figures (around 1 μW available power), the MPPT efficiency is less than 50 %, while the end-to-end efficiency is larger than 10 %. This means that the total power dissipation in this condition is lower than 500 nW, demonstrating the impact of the adopted hybrid modulation scheme. At higher power levels, the MPPT efficiency and end-to-end efficiency reach up to 99 % and 85 %, respectively. As shown in Table 18.1, this work is at state-of-art level even if compared with uncomplete designs (e.g. without MPPT, start-up circuits or load regulation) or not capable to interface high input voltages. In fact, [4] and [5] have no cold-start, only [6] implements an MPPT algorithm but dissipates much more power.

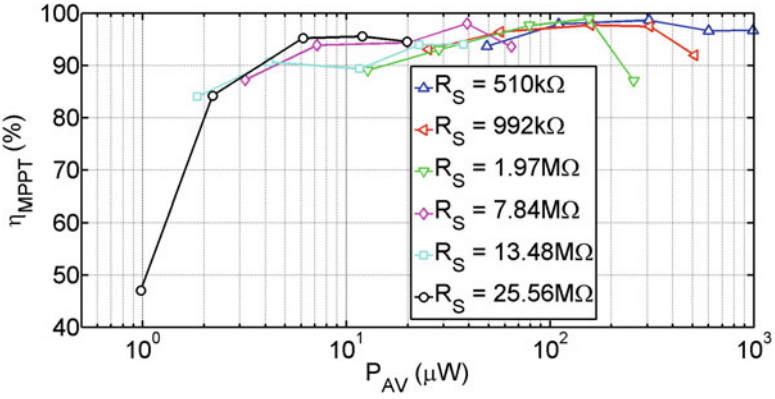

Fig. 18.5 MPPT efficiency as function of available power

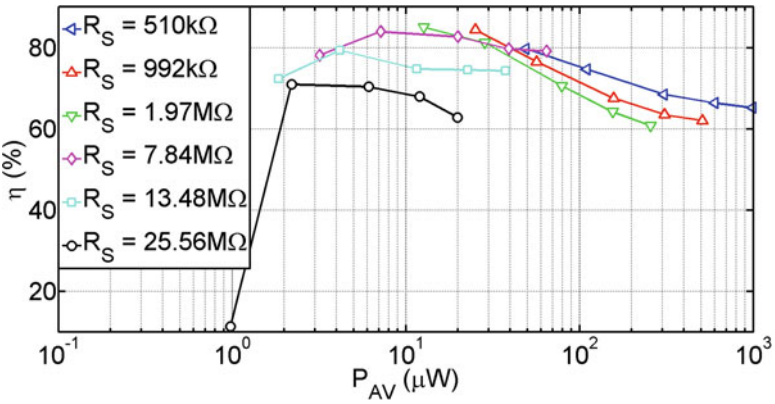

Fig. 18.6 End-to-end efficiency as function of available power

18.4 Conclusions

We have presented an electrostatic harvester interface, based on an ultra-low-power and high-voltage inductive DC-DC converter. Thanks to the proposed modulation scheme, the quiescent current of the converter is lower than 500 nW. The minimum operational available power is 1 μW and the maximum input voltage is 60 V. The chip is fully autonomous and includes start-up, shunt regulation and maximum power point tracking. The converter is capable of tracking source resistance variations between 0.5 MΩ and 25 MΩ.

Table 18.1 Comparison with state-of-art designs

	Hsieh [4]	Huang [5]	Shim [6]	Chen [7]	Danzhu [8]	This work [9]
Process	0.25 μm CMOS	0.25 μm CMOS	0.25 μm BCD	0.18 μm CMOS	0.35 μm	0.25 μm BCD
Max. input voltage (V)	2.5	2.5	7	1	6	60
Output voltage (V)	1	1	1–8	0.35–0.5	2.5	0–5
Input power	1 μW–100 mW	1 μW–50 mW	33 μW–10 mW	50 nW–10 mW	2.5 μW–250 mW	1 μW–1 mW
Function	Output voltage regulation	harvester interface	harvester interface + MPPT	harvester interface	Battery or harvester interface	harvester interface + MPPT
Harvester type	RF	RF	Piezoelectric	Photovoltaic	RF or Vibrational harvester	Electret-based EEH
Architecture	Buck	Buck	Buck-Boost	Buck	Buck	Buck
Control power (nW)	225	217	N.A.	N.A.	100	500
Maximum MPPT efficiency (%)	N.A.	N.A.	99	N.A.	N.A.	99
Maximum end-to-end efficiency (%)	N.A.	N.A.	80	N.A.	N.A.	85
Area (mm2)	0.21	0.39	5.5	1.44	2.88	3

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