Chapter 16
Electrical Compensation of Mechanical Stress Drift in Precision Analog Circuits

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16.1 Introduction: Why Do We Need Stress Compensation Circuits?

It has been known for a long time that (i) mechanical stress alters the parameters of electronic devices [1], and (ii) that integrated circuits are subject to large mechanical stress caused by wafer manufacturing and package assembling processes [2, 3]. In practice, these effects are often negligible, because the principles of circuit design engineering heavily rely on matching of paired devices instead of absolute values of individual devices. For example, the gain of amplifiers is defined by ratios of resistances and the offset depends on the matching of differential input transistor pairs and current mirrors. Although some parameters of single devices are notably altered by package stress (roughly by 10 %), both elements of the pairs vary synchronously, so that their ratio is constant. Of course, this holds only for homogeneous stress and adequate layout techniques like common centroids or interdigitated arrangements [4, 5].

Nonetheless, occasionally circuit designers are bound to rely on absolute values of parameters of single devices, because they define voltages, currents, frequencies, or sensitivities of transducers (temperature, pressure, or magnetic field sensors). In these cases, it is straightforward to trim the circuits after packaging and store the calibration data in on-board memories. Yet, this strategy fails to cope with lifetime drifts of mechanical stress. Sensor designers seem to have been the first ones to note that these drifts are indeed relevant.

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Originally, there were many candidates that might cause these stress drifts [6], but in the course of time, it became apparent that moisture ingress from ambient air into the mold compound of plastic encapsulated packages is the major contributor to mechanical stress drift in the field [7]. In 2002 we conducted an in-house investigation with a stress-sensor testchip after the principles of [8] (Fig. 16.1): MOS-current mirrors with current flow directions in orthogonal directions were used as stress-sensitive elements. The advantage of such a system is that the signal is in the current domain and so it is simple to multiplex an array of elements onto a single terminal in a package like PG-SSO-4-1, which offers only four terminals (two supply terminals, one input and one output current terminal). A moderately "wet" condition of the mold compound was provoked by storing the package in boiling water for 3 h and a moderately "dry" condition was established by storing the package three hours at 180 °C in an oven, which was flushed with dry air. Due to the principle of stress measurement, only the difference of in-plane normal stress components σ_{xx}–σ_{yy} and the in-plane shear stress component σ_{xy} were accessible [9]. Thereby the long edges of the chip are parallel to the x-direction and the short edges are parallel to the y-direction. The patterns of both stress components in dry state agree with [10, 11]. These stress components show an increase in the dry state over wet state by roughly a factor of two. Near the middle of the long edge of the chip, the difference σ_{yy}–σ_{xx} increases by about 20 MPa.

We assembled a Hall plate with biasing circuit and amplifiers for the output signal in the same package [12] and stored it at ambient moisture for several days. Then we measured the magnetic sensitivity while forcing the following sequence of temperatures: start at ambient temperature, then cool down to −40 °C and ramp up to 160 °C, wait there for three hours, then ramp down to −40 °C, and finally ramp up to room temperature. The measurement results in Fig. 16.2 reveal a hysteretic behavior: prior to bake out at 160 °C the mold compound of the package was soaked up with ambient moisture, which causes less compressive stress on the chip and thus more magnetic sensitivity of the Hall plate than after bake out. Between start and stop the magnetic sensitivity exhibits a drift of nearly 2 %. This drift can be reduced to about 0.75 % with optimized mold compounds, but it cannot be avoided altogether for packages, which have to comply with automotive quality standards. Interestingly, when the sample remains in the test fixture over week-end at constant ambient moisture, the magnetic sensitivity drifts back to its original value. So, the package did not disintegrate irreversibly but the stress changes reversible with the water content of the package. This has also been verified by other investigations [7, 13].

These findings led us to the idea to measure the relevant stress components on-chip and feed them into an electronic compensation circuit, which counteracts the systematic effects of the now known mechanical stress on the main circuit (Fig. 16.3). Such a method is versatile: it works for arbitrary packages and silicon technologies. Although the general idea is straightforward, there are challenges: which stress components are relevant, and how can we measure them accurately despite process tolerances and over a wide temperature range.
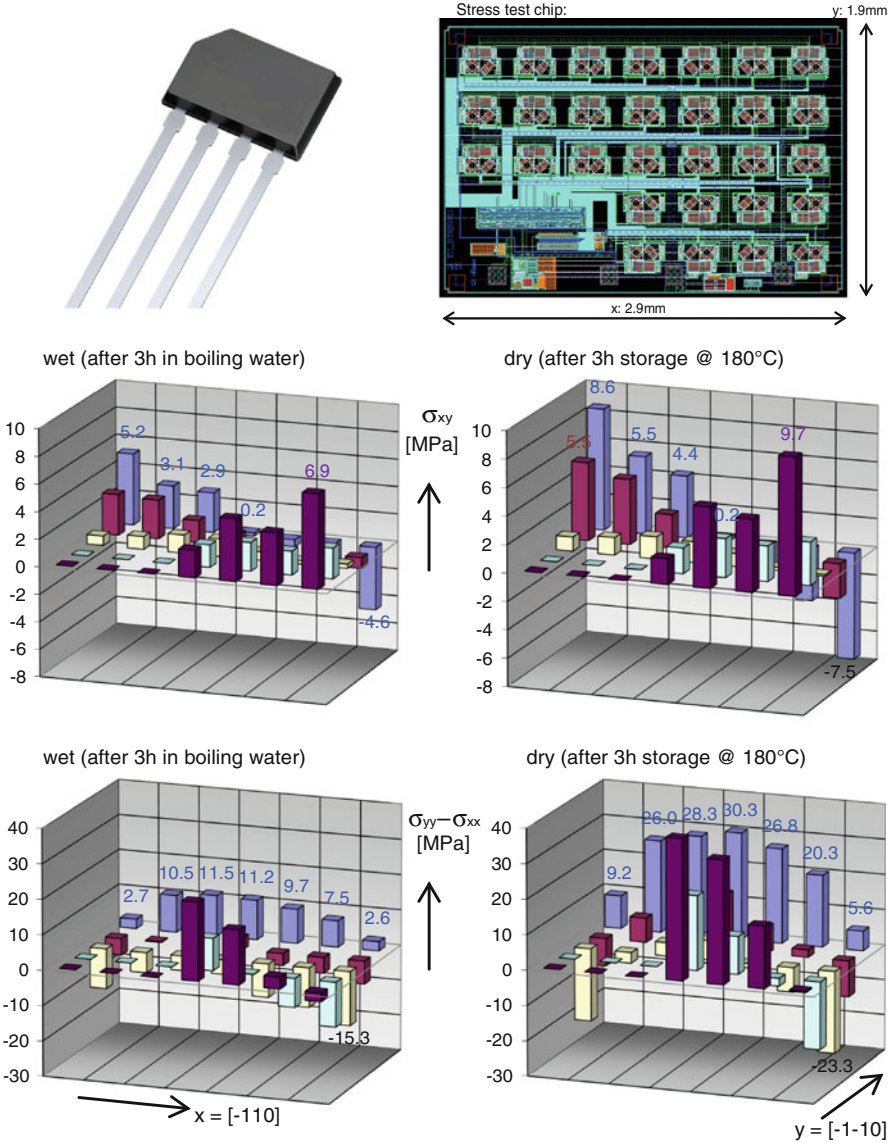
Fig. 16.1 Stress in small plastic encapsulated package (PG-SSO-4-1) as measured with a stress test chip: comparison of wet vs. dry condition at room temperature. The x-axis is parallel to the long edge of the chip and points in [-110] direction of the silicon crystal. The y-axis is parallel to the short edge of the chip and points in [-1-10] direction of the silicon crystal (cf. Fig. 16.7). The silicon chip is 0.22 mm thick, the copper leadframe is 0.2 mm thick, and the overall package is 1 mm thick. Plotted values are averages over 15 devices
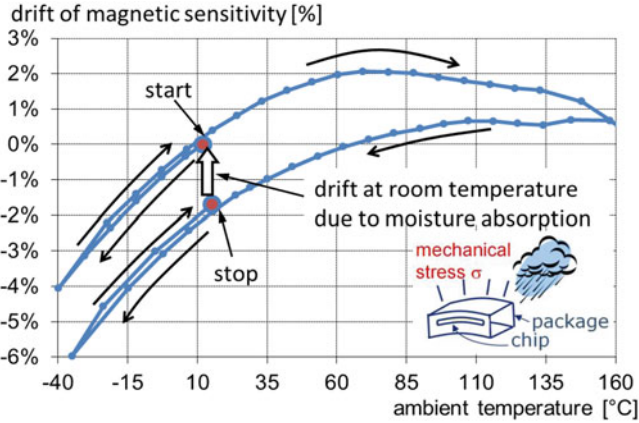
Fig. 16.2 Hysteretic effect of the magnetic sensitivity of a smart Hall sensor due to drift of mechanical stress caused by moisture absorption in plastic encapsulated package PG-SSO-4-1
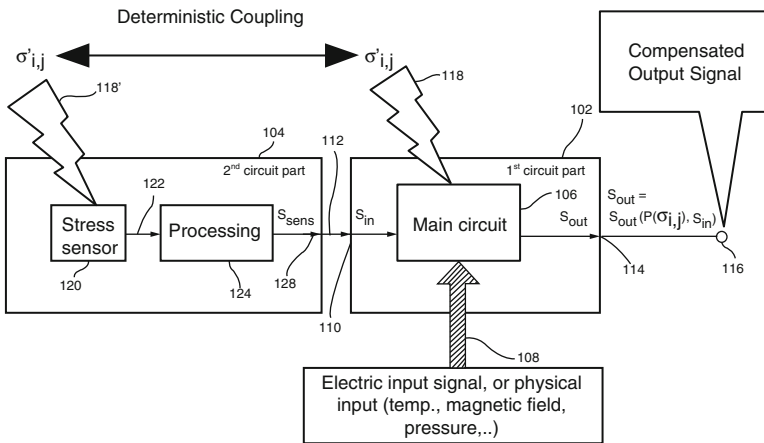

Fig. 16.3 Electronic compensation of drift of main circuit caused by drift of mechanical stress

In the future, more circuits may benefit from electronic compensation of stress related drift: not only do the requirements (accuracy, lifetime stability) increase, but also more inhomogeneous, less predictable, and less stable mechanical stress will be caused by modern package technologies with thinner chips, thinner leadframes, and higher packaging density (Fig. 16.4). Stress compensation circuits also reduce drifts caused by soldering and over-molding.
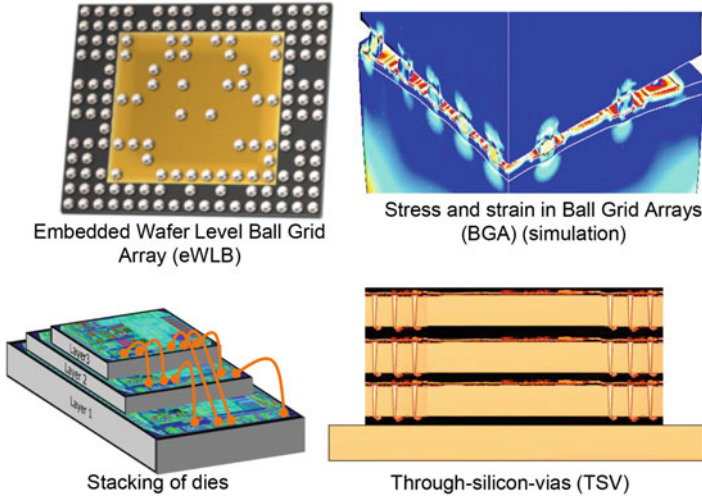
Embedded Wafer Level Ball Grid
Array (eWLB)

Stress and strain in Ball Grid Arrays
(BGA) (simulation)

Stacking of dies

Through-silicon-vias (TSV)

Fig. 16.4 Stress in modern package technologies tends to be higher, less homogeneous, and less predictable with more tensor components

16.2   Some Basics About Mechanical Stress on Micro-Electronic Circuits?

Electronic circuit designers are familiar with temperature drifts and how to compensate them, but usually they are not fluent with mechanical stress and its effects on circuit devices. In spite of some similarities between temperature and stress drift there is one main difference: temperature is a scalar, whereas stress is a tensor quantity. Basically, stress is the force per unit area, which acts inside a rigid body under mechanical load. One can make this force visible, by cutting the rigid body in two parts. Then one has to apply this force on the sectional area of the cuts in order to keep the body under the same load. However, the cut through the body may have various orientations and this also changes the force on the cut area. So the force—which is a vector—depends on the orientation of the cut, too. Thus, this force ($=$ the stress) must have more than three degrees of freedom. Figure 16.5 shows a small block cut out of a rigid body. The block has cut areas perpendicular to x-, y-, z-axes. We can decompose the force on each cut area into components pointing in x-, y-, z- directions. On each cut area we have one component perpendicular to the area: this is the normal stress σ_{xx} with two equal indices specifying the direction of this force. On each cut area we have two mutually perpendicular components parallel to the area. These are the shear stresses σ_{xy}, σ_{xz} with two different indices: the first index specifies the direction of the surface and the second index specifies the direction of the force. In total we have nine components: three cut surfaces, each one with one normal stress and two shear stress components. The forces on the opposite areas (the negative shores with normal vectors in negative x-, y-, z-directions) are equally
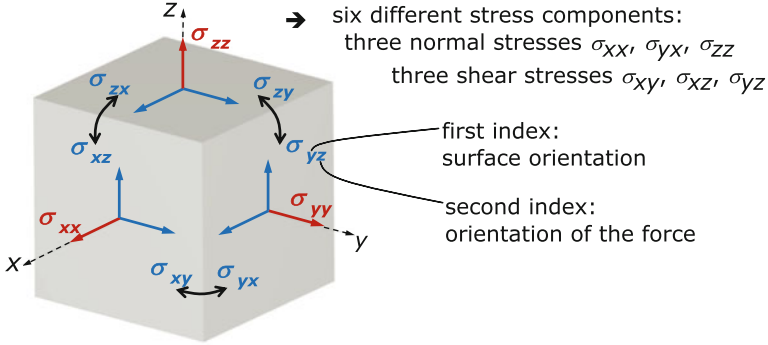
six different stress components:
three normal stresses σ_{xx}, σ_{yx}, σ_{zz}
three shear stresses σ_{xy}, σ_{xz}, σ_{yz}

first index:
surface orientation

second index:
orientation of the force

Fig. 16.5 The stress tensor

Mold body
~ 5 mm x 4 mm x 1 mm

Copper leadframe
~ 0.2 mm thick

chip
2.9 mm x 1.9 mm
x 0.22 mm

chip surface is
under compression
in spite of convex
curvature!

~ -200 MPa

~ -100 MPa

~ -300 MPa

~ 0 MPa

in-plane normal stress
σ_{xx}+ σ_{yy}

~ -400 MPa

in-plane shear
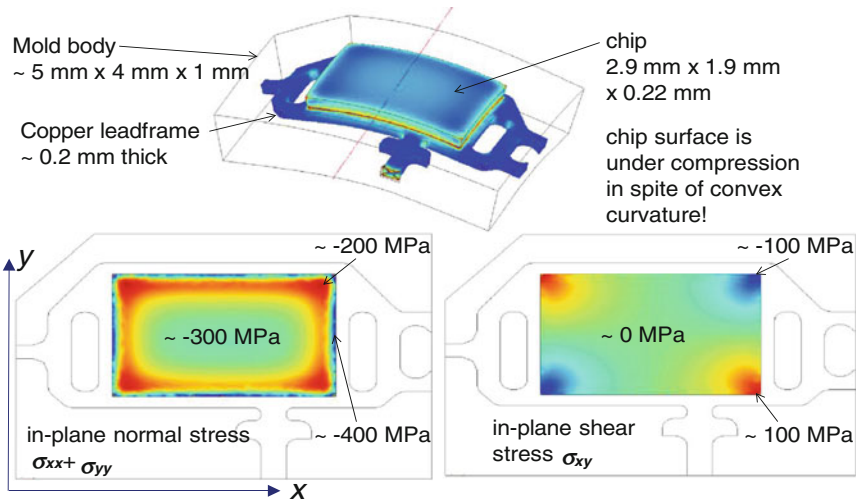stress σ_{xy}

~ 100 MPa

Fig. 16.6 Typical stress pattern in a PG-SSO-4-1 package at 20 °C

large with negative sign. Applying the equilibrium of moments to the block shows
that shear stresses are equal when their indices are swapped: $\sigma_{yz} = \sigma_{zy}$, $\sigma_{xz} = \sigma_{zx}$,
$\sigma_{xy} = \sigma_{yx}$. So eventually, we end up with six independent components of the stress
tensor: three normal stresses σ_{xx}, σ_{yy}, σ_{zz} and three shear stresses σ_{yz}, σ_{xz}, σ_{xy}.

Fortunately, we seldom have to deal with all six stress components, because
micro-electronic packages are usually so-called laminates where the lateral (x,y)-
dimensions are much larger than the thickness (z-dimension). A typical stress
pattern on the chip surface in a package is shown in Fig. 16.6. The PG-SSO-4-1
package serves as an example but other packages of similar technology yet different
size show analogous stress patterns. In particular, the amount of stress near the
center of the chip surface does not depend on the lateral size of the laminate. Over

the main center region of the chip surface (i) the sum of the in-plane normal stress components is homogeneous and negative $\sigma_{xx} + \sigma_{yy} \approx -300$ MPa, and (ii) the in-plane shear stress component vanishes $\sigma_{xy} \approx 0$ MPa. Both values agree with Figs. 5 and 6 in [11]. Negative stress means compressive stress and this is simple to explain, because the mold compound solidifies at elevated temperature and when it cools down, it shrinks more than the silicon chip and the metal leadframe. Interestingly, the curvature of the package is convex: for a homogeneous beam in a bending experiment this shape would mean positive, tensile stress above the neutral fiber, but in the laminate the neutral fiber is shifted (in fact the stress is a zig-zag curve along the thickness [14]). Hence, it is a widespread misconception that the warpage of a package easily defines whether the chip is under compression or tension. Figure 16.6 also shows that near the edges and near the corners all stress components are very inhomogeneous. Thus, we should avoid placing stress sensitive circuitry in an annular region with a width comparable to the chip thickness—this follows from the principle of Saint-Venant [11]. All other stress components (the out-of-plane stress components) vanish on the chip surface, except along the perimeter.

Note that a comparison of stresses in Figs. 16.1 and 16.6 gives $\sigma_{xx} \approx -150$ MPa and $\sigma_{yy} \approx -100$ MPa at positions near the centers of the long edges. In the sequel we will see that some circuit devices respond only to $\sigma_{xx} + \sigma_{yy}$ (which means that they respond equally to σ_{xx} and σ_{yy}) and most other devices can be modified in their layout to have the same stress response. This makes the life for circuit design engineers easy, because one only needs to care about a single combination of tensor components $\sigma_{xx} + \sigma_{yy}$. Fortunately, $\sigma_{xx} + \sigma_{yy}$ is invariant against in-plane rotations so that we can treat this sum of in-plane normal stress components as a scalar just like the temperature in a temperature compensation circuit!

16.3 How Does Mechanical Stress Alter the Parameters of Electronic Devices?

Mechanical stress deforms the crystal lattice, which changes the atomic distances, and this alters the band structure of the semiconductor. The main effect is a change of the curvature of conduction and valence bands, leading to different effective masses of the charge carriers and this affects their mobility.

16.3.1 The Piezo-Resistance Effect

A plain resistor stripe of length *L*, width *W*, and thickness *t* has the resistance

$$R = \rho \; \frac{1}{t} \; \frac{L}{W} \; \text{with} \; \rho = \frac{1}{qn\mu} \tag{16.1}$$

with the specific resistivity ρ, the elemental charge q, the charge density n, and the mobility μ. Mechanical stress alters the resistance according to

$$\delta R = \frac{R - R_0}{R_0} = \frac{\Delta R}{R_0} = \frac{\Delta \rho}{\rho_0} - \frac{\Delta t}{t_0} - \frac{\Delta W}{W_0} + \frac{\Delta L}{L_0} \qquad (16.2)$$

where R is the resistance at stress, and all quantities with lower index "0" denote their values at zero stress. The last three terms on the right hand side are the pure geometrical changes (i.e. the strain). The change of specific resistivity is the piezo-resistance effect. In most cases, it is much larger than the strain terms. Resistivity and stress are second rank tensors, which are more conveniently written as six-component vectors

$$\frac{1}{\rho_0} \begin{pmatrix} \rho_{[100],[100]} - \rho_0 \\ \rho_{[010],[010]} - \rho_0 \\ \rho_{[001],[001]} - \rho_0 \\ \rho_{[010],[001]} \\ \rho_{[100],[001]} \\ \rho_{[100],[010]} \end{pmatrix} = \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix} \cdot \begin{pmatrix} \sigma_{[100],[100]} \\ \sigma_{[010],[010]} \\ \sigma_{[001],[001]} \\ \sigma_{[010],[001]} \\ \sigma_{[100],[001]} \\ \sigma_{[100],[010]} \end{pmatrix} \qquad (16.3)$$

In (16.3) resistivity and stress are measured in the coordinate system of the single crystal. They are related by the piezo-resistive coefficients $\pi_{i,j}$. For low n- and p-doped ($<10^{18}$/cm^3) single crystal silicon at room temperature it holds [15]

$$\pi_{11}^n = -102.2 \ \%/\text{GPa}, \quad \pi_{12}^n = 53.4 \ \%/\text{GPa}, \quad \pi_{44}^n = -13.6 \ \%/\text{GPa} \quad (16.4\text{a})$$

$$\pi_{11}^p = 6.6 \ \%/\text{GPa}, \quad \pi_{12}^p = -1.1 \ \%/\text{GPa}, \quad \pi_{44}^p = 138.1 \ \%/\text{GPa} \quad (16.4\text{b})$$

With larger doping the piezo-resistive coefficients become slightly smaller and with larger temperature they decrease roughly by $-0.3 \ \%/°\text{C}$ [15]. Transforming (16.3) from the crystal- into the chip-reference frame [16] gives for (100)-silicon

$$\delta R_x \cong \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2} \sigma_{xx} + \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \sigma_{yy} + \pi_{12} \sigma_{zz} \qquad (16.5\text{a})$$

$$\delta R_y \cong \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \sigma_{xx} + \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2} \sigma_{yy} + \pi_{12} \sigma_{zz} \qquad (16.5\text{b})$$

$$\delta R_z \cong \pi_{12} \left(\sigma_{xx} + \sigma_{yy} \right) + \pi_{11} \sigma_{zz} \qquad (16.5\text{c})$$

We use the "approximately equal"-sign ($\cong$) because we neglect the strain terms against the piezo-resistive terms. The x-direction is equal to the direction [-110] of the single crystal silicon, the y-direction is equal to [-1-10], and the z-direction is equal to [001] (see Fig. 16.7). R_x and R_y are lateral resistances, where the current
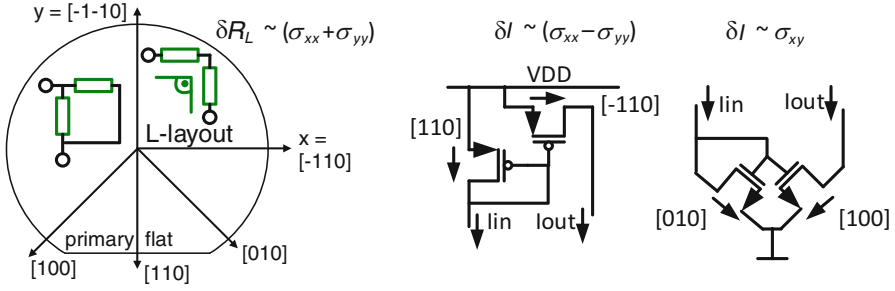
Fig. 16.7 Orthogonal MOS-FET current-mirrors can be used as stress sensors: $\sigma_{xx}-\sigma_{yy}$ (PMOS-FET), σ_{xy} (NMOS-FET). Crystallographic axes in (100)-silicon. Also shown: L-layouts for lateral resistors in parallel and series connection

flows along the *x*- and *y*-axes of the chip, respectively, whereas R_z is a vertical resistance with current perpendicular to the chip surface. The vertical resistance has the nice property that it depends equally on σ_{xx} and σ_{yy} (we may neglect σ_{zz} because it vanishes on the main part of the chip surface). The lateral resistances depend differently on σ_{xx} and σ_{yy}, however, we can add both of them in a so-called L-layout (see Fig. 16.7) to obtain the desired stress dependence [17]

$$\delta R_L \cong \frac{\pi_{11} + \pi_{12}}{2}\left(\sigma_{xx} + \sigma_{yy}\right) + \pi_{12}\sigma_{zz} \tag{16.5d}$$

with $R_L = R_x + R_y$ (series connection) or $R_L = R_x \mathbin{/\mkern-5mu/} R_y$ (parallel connection).

Inserting (16.4a) into (16.5a–d) we get for low *n*-doped resistors

$$\delta R_x^n \cong -17.6\,\%/\text{GPa} \times \sigma_{xx} - 31.2\,\%/\text{GPa} \times \sigma_{yy} + 53.4\,\%/\text{GPa} \times \sigma_{zz} \tag{16.6a}$$

$$\delta R_y^n \cong -31.2\,\%/\text{GPa} \times \sigma_{xx} - 17.6\,\%/\text{GPa} \times \sigma_{yy} + 53.4\,\%/\text{GPa} \times \sigma_{zz} \tag{16.6b}$$

$$\delta R_z^n \cong 53.4\,\%/\text{GPa} \times \left(\sigma_{xx} + \sigma_{yy}\right) - 102.2\,\%/\text{GPa} \times \sigma_{zz} \tag{16.6c}$$

$$\delta R_L^n \cong -24.4\,\%/\text{GPa} \times \left(\sigma_{xx} + \sigma_{yy}\right) + 53.4\,\%/\text{GPa} \times \sigma_{zz} \tag{16.6d}$$

Inserting (16.4b) into (16.5a–d) we get for low *p*-doped resistors

$$\delta R_x^p \cong -66.3\,\%/\text{GPa} \times \sigma_{xx} + 71.8\,\%/\text{GPa} \times \sigma_{yy} - 1.1\,\%/\text{GPa} \times \sigma_{zz} \tag{16.7a}$$

$$\delta R_y^p \cong 71.8\,\%/\text{GPa} \times \sigma_{xx} - 66.3\,\%/\text{GPa} \times \sigma_{yy} - 1.1\,\%/\text{GPa} \times \sigma_{zz} \tag{16.7b}$$

$$\delta R_z^p \cong -1.1\,\%/\text{GPa} \times \left(\sigma_{xx} + \sigma_{yy}\right) + 6.6\,\%/\text{GPa} \times \sigma_{zz} \tag{16.7c}$$

$$\delta R_L^p \cong 2.8\ \%/\text{GPa} \times \left(\sigma_{xx} + \sigma_{yy}\right) - 1.1\ \%/\text{GPa} \times \sigma_{zz} \qquad (16.7d)$$

P-doped vertical resistors and resistor-L have lowest stress dependence [18]. The largest difference in stress dependence between two types of resistors in (100)-Si is for *n*-doped vertical resistors and lateral resistors in L-layout.

Unsilicided poly-silicon resistors consist of crystallites with a small number of orientations [19], yet there seems to be no preference for *x*- and *y*-directions. Therefore, a single poly-silicon resistor has the same isotropic stress-dependence law (16.5d) as single crystal resistors in L-layout. But, the total resistance of poly-silicon is a mixture of inter-grain and intra-grain contributions and this gives piezo-resistive coefficients of equal sign, but smaller magnitude than single crystal resistors in L-layout. For low-ohmic *n*-poly-Si with 100 Ω/square we measured a $(\sigma_{xx} + \sigma_{yy})$-dependence of −4.9 %/GPa, and for high-ohmic *n*-poly-Si with 1 kΩ /square we found −8.8 %/GPa.

16.3.2 The Piezo-MOS Effect

Mechanical stress alters the mobility μ of the charge carriers in the channels of MOS-FETs [8], which leads to a piezo-resistive stress dependence. The mobility enters the current gain β but not the threshold voltage V_{th}. The drain current is

$$I_D = \begin{cases} \beta \left(V_{GS} - V_{th} - V_{DS}/2\right) V_{DS} & \text{for} \quad V_{DS} < V_{GS} - V_{th} \\ (\beta/2) \left(V_{GS} - V_{th}\right)^2 & \text{for} \quad V_{DS} \geq V_{GS} - V_{th} \end{cases} \qquad (16.8)$$

In (16.8) V_{GS} and V_{DS} are gate-source and drain-source voltages, respectively. The current gain is $\beta = \mu \left(\varepsilon_{ox}/t_{ox}\right) (W/L)$ with dielectric constant ε_{ox} and thickness t_{ox} of the gate oxide, and with width W and length L of the channel. Thus, NMOS-FETs are comparable with *n*-doped resistors and PMOS-FETs are similar to *p*-doped resistors if we replace $\delta\beta = \Delta\beta/\beta_0 \cong \delta\mu = -\delta\rho$ (here again we neglect pure strain effects on the channel geometry). As explained in [8] one can use the piezo-MOS effect to make temperature compensated stress sensors for σ_{xx}–σ_{yy} and σ_{xy} (but unfortunately not for $\sigma_{xx} + \sigma_{yy}$, see Fig. 16.7).

16.3.3 The Piezo-Junction Effect

Mechanical stress alters the mobility μ_B of *minority* carriers in the base of a bipolar transistor [20]. This is in contrast to piezo-resistive and piezo-MOS effects, which act on the *majority* carriers. Stress also acts on the intrinsic carrier density $n_{i,B}$ in the base. Both effects change the saturation current I_S.

$$I_C = I_S \exp\left(V_{BE}/V_T\right) \text{ with } V_T = k_b T/q \text{ and } I_S = k_b T \left(A_E/W_B\right) \left(n_{i,B}^2/N_B\right) \mu_B \tag{16.9}$$

I_C is the collector current, V_{BE} is the base-emitter voltage, V_T is the thermal voltage, k_b Boltzmann's constant, T the absolute temperature, A_E the emitter area, W_B the base width, and N_B the doping of the base. The intrinsic carrier density leads to a notable non-linear dependence of saturation current on mechanical stress, so that we need to add second order terms

$$\delta I_{S,ij} = \Delta I_{S,ij}/I_{S0} = -\zeta_{ijkl}\sigma_{kl} - \zeta_{ijklmn}\sigma_{kl}\sigma_{mn} \tag{16.10}$$

ζ_{ijkl} and ζ_{ijklmn} are 1st and 2nd order piezo-junction coefficients. Not all coefficients are known and the reported values of some are also inconsistent (perhaps due to different doping levels or different intrinsic stress). For vertical bipolars in (100)-silicon we use the following rough numbers

$$\begin{aligned}\delta I_S^{VPNP} &\cong -13.8\,\%/\text{GPa} \times \left(\sigma_{xx} + \sigma_{yy}\right) - 30.8\,\%/\text{GPa} \times \sigma_{zz} \\ &\quad + 66\,\%/\text{GPa} \times \left(\sigma_{xx} + \sigma_{yy}\right)^2 + 220\,\%/\text{GPa} \times \sigma_{xy}^2\end{aligned} \tag{16.11a}$$

$$\begin{aligned}\delta I_S^{VNPN} &\cong -43.4\,\%/\text{GPa} \times \left(\sigma_{xx} + \sigma_{yy}\right) + 28.4\,\%/\text{GPa} \times \sigma_{zz} \\ &\quad + 37.5\,\%/\text{GPa} \times \left(\sigma_{xx} + \sigma_{yy}\right)^2 + 366\,\%/\text{GPa} \times \sigma_{xy}^2\end{aligned} \tag{16.11b}$$

Vertical PNPs (VPNPs) are less sensitive to mechanical stress than vertical NPNs (VNPNs) [21]. The situation is more complex for lateral bipolars, because the current flow direction also enters the stress dependence. However, one can again use L-layout to obtain isotropic behavior [21]. Nevertheless, we prefer vertical over lateral bipolars due to practical reasons (less surface effects, size, no L-layout required, availability in standard design packages). For practical use we only need to remember that bipolars should have layouts with 90° symmetry in the (x,y)-plane and they should be placed at regions on the chip where only the in-plane normal stress components are present. Then, their saturation currents have linear and quadratic terms proportional to $\sigma_{xx} + \sigma_{yy}$ and $(\sigma_{xx} + \sigma_{yy})^2$.

16.3.4   The Piezo-Hall Effect

Mechanical stress alters the Hall coefficient, which leads to a change in the current related magnetic sensitivity $S_{i\text{Hall}}$. In (100)-silicon it holds for hall plates [22]

$$\delta S_{i\text{Hall}} = \Delta S_{i\text{Hall}}/S_{i0\text{Hall}} = P_{12}\left(\sigma_{xx} + \sigma_{yy}\right) + P_{11}\sigma_{zz} \tag{16.12}$$

For the piezo-Hall coefficients of low n-doped silicon [22, 23] report $P_{11} = -88\,\%/\text{GPa}$ and $P_{12} = 45\,\%/\text{GPa}$ for a doping level of $1.8 \times 10^{14}/\text{cm}^3$ at 20 °C.

At larger doping concentration or larger temperature, the piezo-Hall coefficients get slightly smaller. In our technologies we measured $P_{12} = 42\,\%/\text{GPa}$. (100)-silicon has the largest piezo-Hall effect, whereas (111)-silicon of old bipolar technologies gives the smallest piezo-Hall effect [24].

To sum up, for all common devices we can use layouts which respond equally to normal stress in both in-plane lateral directions (x and y). Other components of the stress tensor can be neglected. The piezo-coefficients have negative temperature coefficients. Thus, at low temperature the devices are most susceptible to mechanical stress. Moreover, thermo-mechanical stress is largest at low temperature, because the package constituents were joined at elevated temperature and stress builds up due to mismatch of thermal expansion between them. Besides, the stiffness of the mold compound is larger at low temperature. Consequently, low temperature is the worst case for stress drifts of circuits.

16.4 How to Make an On-Chip Stress Sensor for $\sigma_{xx} + \sigma_{yy}$?

It is common practice to place stripes of resistors with different direction on a chip in order to measure various components of the stress tensor on the chip surface. However, these are not self-sufficient on-chip stress sensors, because the changes in resistance values are measured by an off-chip Ohmmeter, which is not subject to the stress, and so it can serve as a stable reference. In order to compensate mechanical stress drifts we need a sensor that outputs a signal with large sensitivity to mechanical stress but only small sensitivity to other effects like temperature. Moreover, since it is not possible to apply stress changes during the production and testing of the circuit, the sensitivity of the stress sensor needs to be stable against process spread.

In principle, one can use any two of the devices discussed in the previous Sect. 16.3, and compare their stress-dependent parameters by some circuit.

(1) n/n^+ stress resistor in L-layout:

We may compare low and high n-doped resistors, both of lateral type and in L-layout. They have stress sensitivities according to (16.5d), yet the resistor with the larger doping has a smaller piezo-resistive coefficient than the low-doped one. The maximum differential sensitivity between both resistors is somewhat less than 20 %/GPa and for p/p^+ stress resistors in L-layout it is about ten times smaller. The process spread between both types of resistors is large, because the two implantation processes do not correlate with each other: They have different sheet resistance, different temperature coefficient of resistance (TCR), and large spread of both parameters. Yet the piezo-coefficients are less affected by spread of doping concentration. So, one can trim off sheet resistances and TCRs in an end-of-line test. However, the residual errors after trimming are likely to be problematic because of the small stress sensitivity.

(2) *n/p* stress resistors in L-layout:

    If we compare low *n*- and *p*-doped lateral resistors in L-layout, the situation is slightly better: *n*- and *p*-resistors still have a large mismatch of sheet resistance, but smaller TCR mismatch and their differential stress sensitivity is 30 % higher: 27.2 %/GPa according to (16.6d, 16.7d) [25]. Instead of comparing just two resistors in L-layout one can also use four resistors in L-layout in a Wheatstone bridge circuit [26].

(3) lateral/vertical *n*-doped stress resistors:

    A significantly higher stress sensitivity is obtained, if we compare a low *n*-doped lateral resistor in L-layout ($R_x + R_y$) with a low *n*-doped vertical resistor (R_z): 77.8 %/GPa according to (16.6c, d). In BiCMOS technologies with *n*-epitaxial layer and *n*-buried layer we make a vertical resistor where the current flows from a contact to the buried layer, then sideways in the low ohmic buried layer and up again into a second contact (R^n_V in Fig. 16.8). Yet the contacts should reach as close as possible to the lateral boundaries of the device to establish straight vertical current flowlines. If there is a spacing between contacts and lateral isolating boundary the current flowlines exhibit some curvature (current crowding into the contact) and this mixes some lateral piezo-resistive portion to the vertical one so that the overall device has less than 77.8 %/GPa stress sensitivity [27].
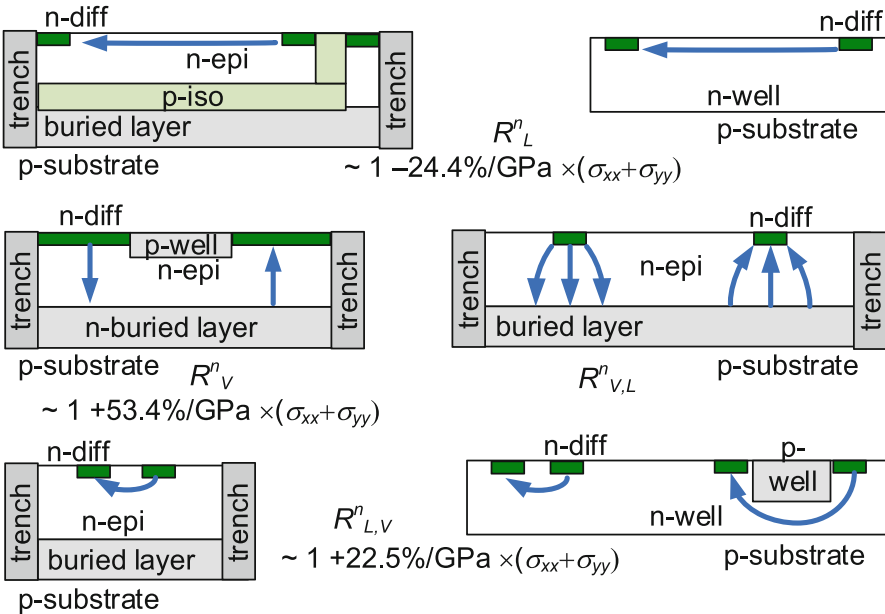

R^n_L

~ 1 −24.4%/GPa ×($\sigma_{xx}+\sigma_{yy}$)

R^n_V

~ 1 +53.4%/GPa ×($\sigma_{xx}+\sigma_{yy}$)

$R^n_{V,L}$

$R^n_{L,V}$

~ 1 +22.5%/GPa ×($\sigma_{xx}+\sigma_{yy}$)

Fig. 16.8 Lateral, vertical and combined stress resistors in technologies with and without buried layer. The *arrows* indicate current streamlines. Only one branch of the L-layouts of resistors is shown

On the other hand, the size of the contact controls the curvature of the current flowlines and so one can achieve nearly all piezo-resistive coefficients between pure lateral and pure vertical current flow ($-24.4 \ldots +53.4$ %/GPa) ($R^n_{V,L} \ldots R^n_V$ in Fig. 16.8).

We can use the same tub for vertical and lateral resistors, if we split up the large contact into two smaller ones with a spacing in-between ($R^n_{L,V}$ in Fig. 16.8). Then the current flow between the two smaller contacts has larger lateral contribution than the vertical current flow. Since the same tub is used, the process spread should have smaller effect on mismatch between the two devices. If the doping profile versus depth is constant, one should be able to realize vertical and lateral resistors with very similar TCR.

In pure CMOS technologies without buried layers one can make lateral resistors having smaller contribution of vertical current flowlines (see R^n_L in Fig. 16.8). However the vertical resistors are worse, because they have larger contributions of lateral current flowlines (see $R^n_{L,V}$ in Fig. 16.8). Moreover, the piezo-resistive coefficients are smaller because the doping of the n-CMOS well is two orders in magnitude larger than in n-epitaxial layers.

16.5   Circuits for Compensation of Mechanical Stress Drift

16.5.1   Stress Compensation with n/p-Resistors in L-Layout

Historically, we applied the electronic compensation of mechanical stress drift for the first time in a smart Hall sensor (Fig. 16.9) [28, 29]. The basic idea was that the stress sensor detects the very same mechanical stress component, which causes a drift in the Hall sensor. According to (16.12) the relevant stress component is $\sigma_{xx} + \sigma_{yy}$ as long as the Hall-plate is near the center of a (100)-silicon chip. So we used lateral resistors in L-layout with low n- and p-doping as stress sensor and placed them close to the Hall plate. The process spread in sheet resistances between n- and p-stress resistors was trimmed at room temperature via a trimmable ratio of current mirrors. Unfortunately, the low n- and p-doped stress resistors have quite different TCR: they can differ by 0.4 %/°C. An on-chip temperature sensor (T) was added near the Hall-plate and the stress-resistors to remove temperature errors between n- and p-stress-resistors. The signals of stress sensor $S_{raw,sum}$ and temperature sensor T need only a small bandwidth so that we can digitize them with the same multiplexed ADC. After packaging, the output $S_{raw,sum}$ of the stress sensor was measured versus temperature and stored as a reference $S_{ref,sum}(T)$ in an on-chip memory. Later on during operation in the field the system only uses the stress drift dS_{sum}.

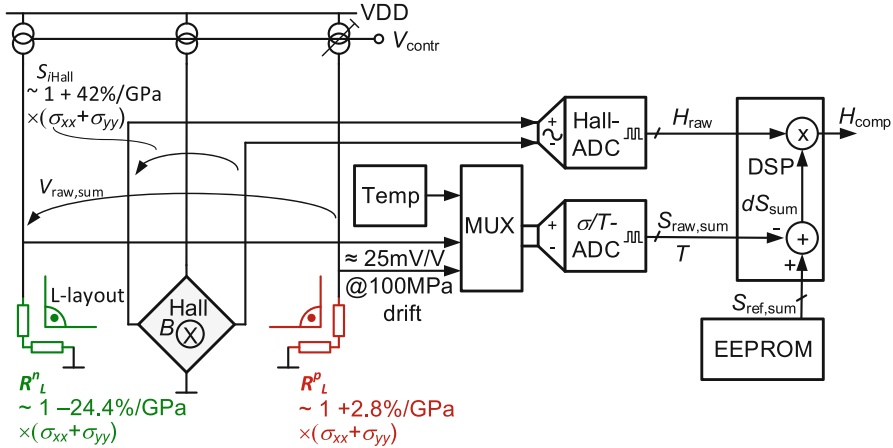$$dS_{sum} = S_{raw,sum} - S_{ref,sum}(T) \qquad (16.13)$$

Fig. 16.9 First stress compensation circuit used for long-term stability of magnetic sensitivity of Hall sensor. The stress sensor signal $V_{raw,sum}$ was A/D-converted and a versatile compensation was implemented with digital signal processing

The main signal of the Hall-plate was also digitized with another ADC. In the digital domain the three signals of Hall-plate H_{raw}, temperature sensor T, and stress-sensor dS_{sum} are conveniently combined to remove temperature- and stress-dependencies of the Hall signal.

$$H_{comp} = H_{raw} \left(1 + TCH_1 \ T + TCH_2 \ T^2 + \cdots\right)$$
$$\left(1 + EPC_1 \ dS_{sum} + EPC_2 \ dS_{sum}^2 + \cdots\right) \qquad (16.14)$$

where H_{comp} is the compensated Hall output signal, H_{raw} is the uncompensated (raw) signal of the Hall plate, TCH_1 and TCH_2 are the first and second order temperature coefficients of the system, and EPC_1 and EPC_2 are the first and second order effective piezo-coefficients of the system. The *effective* piezo-coefficients comprise all effects of stress on all relevant circuit components. In practice we do not need to know which devices and to which extent they are affected by mechanical stress as long as we assure that all delicate devices depend only on $\sigma_{xx} + \sigma_{yy}$ and that the stress values on different devices at different locations are sufficiently correlated. This means that these devices must not be too close to the perimeter of the chip and they must have a layout, which avoids stress dependence different from $\sigma_{xx} + \sigma_{yy}$. The effective piezo-coefficients may again depend slightly on temperature $EPC_1 = EPC_{10} + TCEPC_1 \times T$.

The exact numbers for TCH_1, TCH_2, EPC_1, EPC_2 are conveniently found by empirical investigation, although for the purpose of circuit design one needs rough guesses according to Sects. 16.2, 16.3, and 16.4. To this end we have to subject the chip to different temperatures and different mechanical stress while recording the signals H_{raw}, T, and dS_{sum}. Note that we do not need to know the exact values of

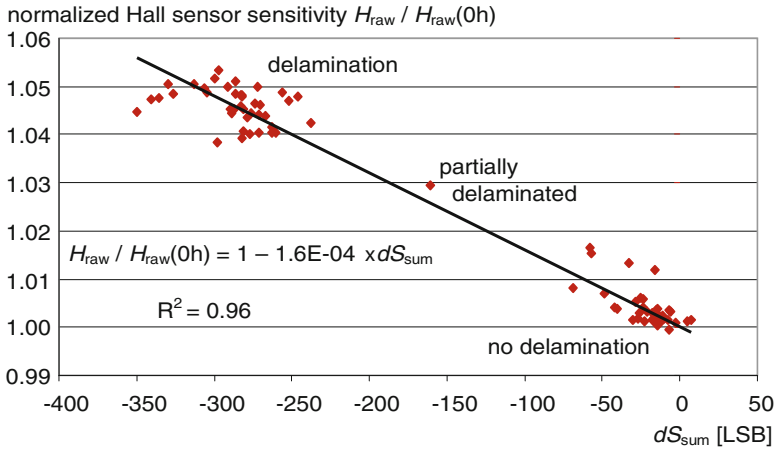normalized Hall sensor sensitivity H_{raw} / $H_{raw}(0h)$

Fig. 16.10 The measurement of normalized magnetic sensitivity of a Hall sensor and the drift of a $\sigma_{xx} + \sigma_{yy}$ stress sensor after a severe lifetime load show good correlation and detectability of delamination in plastic encapsulated packages

mechanical stress (in terms of MPa), because we only need to extract the correlation coefficients between the three signals. The application of different stress can be done by wafer bow experiments [25], by bending of stripes cut out of wafers [30], by comparing pre- and post-package assembling tests, by moisture absorption of plastic encapsulated packages [25], by applying mechanical force to packaged devices [25, 31], or by comparing different packages with different mechanical stress (e.g. with different thicknesses of leadframe and chip or with different mold compounds).

Figure 16.10 shows an example of a strong correlation between drift of normalized magnetic sensitivity of a Hall plate and the stress drift signal dS_{sum}. It was measured in the course of a temperature humidity cycling test which was continued until finally the plastic encapsulated package disintegrated. The delamination at various mechanical interfaces caused a reduction in compressive stress which means a positive stress change on the Hall-plate and this led to an increase in magnetic sensitivity of about $4 \ldots 5\%$. With the piezo-Hall coefficient of (16.12) we conclude that the delamination caused a relaxation in stress $\sigma_{xx} + \sigma_{yy}$ by 100 MPa. This is a good example how a stress sensor can detect serious mechanical flaws which might occur during lifetime. In a similar way comparison of stress sensor readouts in pre and post packaging tests can be used to monitor the quality of package assembly process. Finally, stress changes due to soldering the IC-package to a printed circuit board can also be screened.

Figure 16.11 shows the final performance of the stress compensated Hall sensor circuit. Stripes were cut out of the silicon wafer and mechanical stress was applied to them with a four-point bending bridge. The plot compares normalized magnetic sensitivity of the circuit with and without stress compensation at low and high temperature. An improvement of factor 7 can be observed.
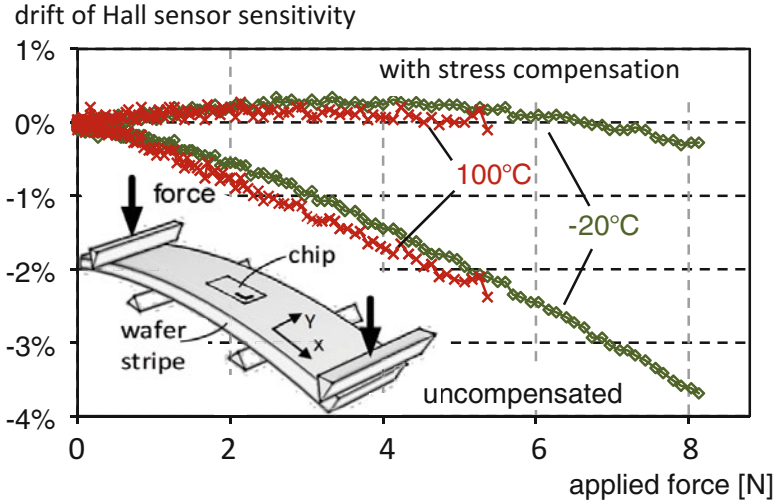
Fig. 16.11 Measured drift of magnetic sensitivity of a Hall sensor with and without stress compensation in a wafer stripe bending experiment
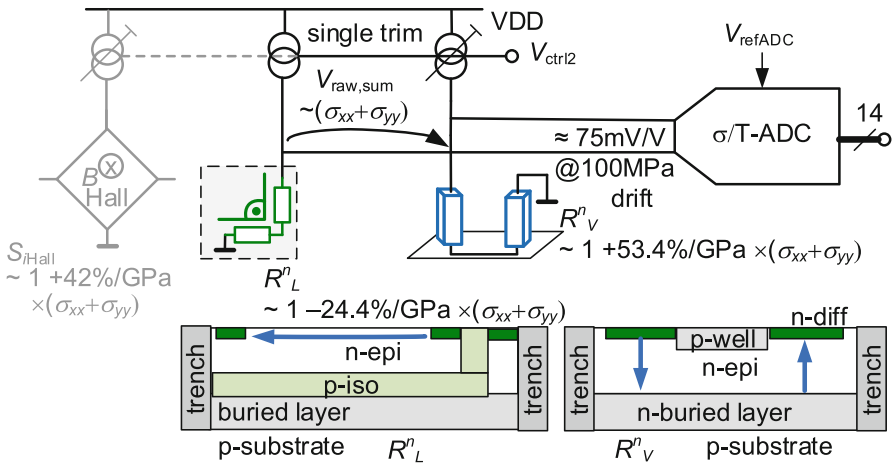

Fig. 16.12 Improved digital stress compensation of a Hall-plate with lateral/vertical n-doped stress resistors having larger stress sensitivity and smaller difference in TCR

16.5.2 Stress Compensation with Lateral and Vertical Resistors

A stress sensor with lateral/vertical n-doped stress resistors has three times higher stress sensitivity than the n/p stress resistors in L-layout (Fig. 16.12). Moreover, the TCRs of lateral/vertical n-doped stress resistors differ only in the order <0.1 %/°C, which is four times less than the TCRs of n/p resistors.

A major problem with all stress sensors for $\sigma_{xx} + \sigma_{yy}$ is the difference in TCR between the two types of stress resistors. A systematic (nominal) TCR difference can be stored as reference $S_{ref,sum}(T)$, but this requires an on-chip memory and a multi-temperature test after package assembly. For some products this is too expensive. We can reduce the errors caused by nominal TCR difference of the stress resistors by the replica circuit of Fig. 16.13. A bandgap kernel is used to generate a voltage V_{P1} of appropriate temperature dependence. If this bandgap kernel also uses devices with mere $\sigma_{xx} + \sigma_{yy}$ stress dependence the voltage shows a small dependence on $\sigma_{xx} + \sigma_{yy}$, which simply adds to the stress dependence of Hall-plate and stress sensors, and it can be compensated together with all other circuits. Besides, the stress dependence of this voltage is an order in magnitude smaller than the stress dependence of the Hall plate, especially if the bandgap kernel uses vertical PNPs and low-ohmic poly-silicon resistors. The input voltage V_{P1} is replicated to the vertical n-doped stress resistor $R^n{}_V$ in a feedback loop comprising a controlled current source and an OTA. With $V_V = V_{P1}$ the current through $R^n{}_V$ becomes stress and temperature dependent. It is mirrored to the lateral L-shaped n-well resistor $R^n{}_L$. The resulting voltage V_L can be adjusted with a trimming at a single temperature to match the voltages $V_V = V_{P1}$. Yet, even at zero stress the TCR difference between vertical resistor $R^n{}_V$ and lateral resistor $R^n{}_L$ would lead to an unwanted voltage between them. However, since $V_V = V_{P1}$ and V_{P1} is defined by the bandgap kernel, we can use the same bandgap kernel to construct a further voltage V_{P2}, which has again only tiny stress dependence and whose temperature dependence is chosen such as to guarantee $V_{P2}(T) = V_L(T)$ at zero stress for all temperatures. In other words, the temperature dependence of V_{P2} is designed to cancel out the systematic TCR differences between $R^n{}_V$ and $R^n{}_L$. Any process spread between V_{P1} and V_{P2} is minimized by the bandgap principle. This circuit technique makes use of the fact that the systematic TCR difference and the stress dependence of the resistors is much more stable than the spread of the sheet resistances (which is about $\pm 20\%$). Finally, we can superimpose the same temperature coefficient on V_{P1} and V_{P2} to set the temperature dependence of the stress sensitivity of the stress sensor to any arbitrary value. This can be used to cancel out the temperature dependence of the piezo-resistive coefficients.

16.5.3 Stress Compensation for Different Sensitivity in σ_{xx} and σ_{yy}

The lateral n-doped stress resistor in Fig. 16.13 comprises four resistor stripes connected in a Wheatstone bridge circuit. Two resistors are aligned in x-direction (i.e. [-110] crystal direction) and the other two resistors are aligned in y-direction (i.e. [-1-10]). According to (16.6a, b) the digitized output voltage $S_{raw,diff}$ of the Wheatstone bridge is proportional to $\sigma_{xx} - \sigma_{yy}$ with a sensitivity of 6.8 %/GPa. An even ten times higher stress sensitivity could be obtained if the four resistors were p-doped instead of n-doped. In both cases the output voltage vanishes for $\sigma_{xx} = \sigma_{yy}$
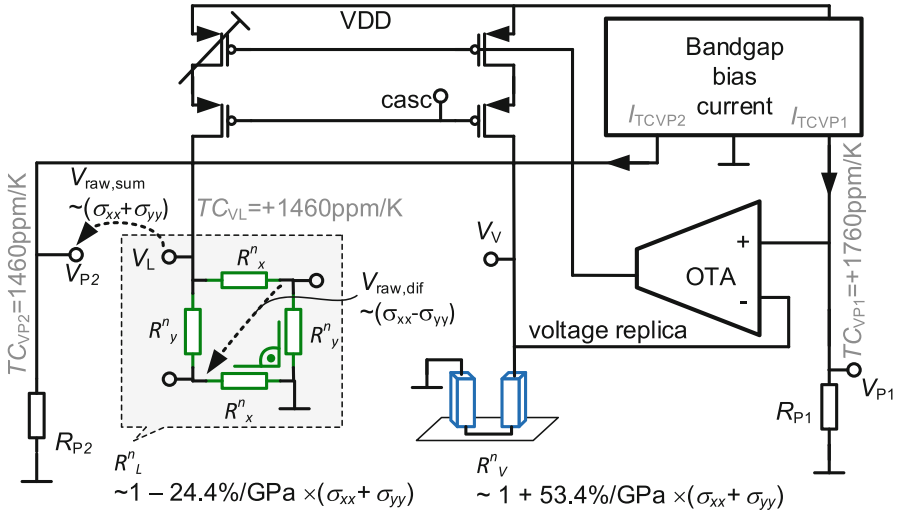
Fig. 16.13 Temperature compensation for measurement of $\sigma_{xx} + \sigma_{yy}$ and $\sigma_{xx} - \sigma_{yy}$

for all temperatures, if we disregard mismatch between the four resistors. So the signal $S_{\text{raw,diff}}$ has much less errors caused by process spread and temperature excursion than the signal $S_{\text{raw,sum}}$. Therefore it is not necessary to store reference values $S_{\text{ref,diff}}(T)$ recorded during a multi-temperature test and compute a subsequent drift $dS_{\text{diff}} = S_{\text{raw,diff}} - S_{\text{ref,diff}}(T)$ as we did in the case of $S_{\text{raw,sum}}$ (see above). Instead, we can directly use $S_{\text{raw,diff}}$ in the stress compensation algorithm. The accuracy of $S_{\text{raw,diff}}$ is quite good and comparable to MOS-stress sensors (Fig. 16.7).

So the system of Fig. 16.13 has in fact two mechanical stress sensors: one for the sum ($S_{\text{raw,sum}}$) and one for the difference of in-plane normal stress components ($S_{\text{raw,diff}}$). This can be useful if a parameter of a circuit responds differently to mechanical stress in x- or y-directions. Reasons for such an anisotropic behavior may be a device layout which lacks x-y-symmetry (because the device is too large to add a second one in L-layout) or silicon technologies, where inhomogeneities in the bulk material (such as deep trenches or the edges of the die) may lead to a cross coupling of different components of the stress tensor. An example of such a case is shown in Fig. 16.14, where the output frequency of an RC-relaxation oscillator increases with 11.7 %/GPa stress in x-direction, while it decreases with −2.3 %/GPa stress in y-direction. A compensation of the drift of this oscillator frequency caused by mechanical stress can be done like this.

$$f_{\text{comp}}^{\text{osz}} = f_{\text{raw}}^{\text{osz}} C_{\text{corr}} (T, dS_{\text{sum}}, S_{\text{raw,diff}}) \tag{16.15a}$$

$$
\begin{aligned}
C_{\text{corr}} (T, dS_{\text{sum}}, S_{\text{raw,diff}}) &= \left(1 + TC_1\ T + TC_2\ T^2 + \cdots\right) \\
&\times \left(1 + EPC_1\ dS_{\text{sum}} + EPC_2\ dS_{\text{sum}}^2 + \cdots + EPC_1'\ S_{\text{raw,diff}} + EPC_2'\ S_{\text{raw,diff}}^2 + \cdots\right)
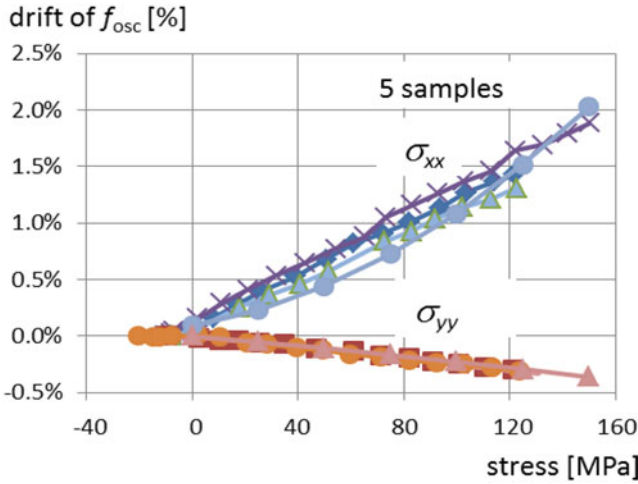\end{aligned}
\tag{16.15b}
$$

Fig. 16.14 The output frequency f_{osc} of an RC-relaxation oscillator shows different drift when stress is applied in x- and y-directions. Measurement was done in silicon-stripe bending experiments at room temperature
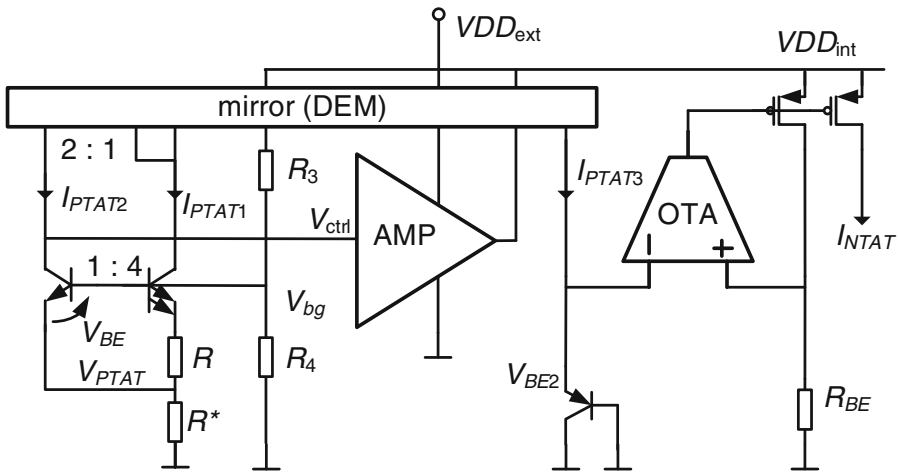

Fig. 16.15 Brokaw-bandgap with VNPNs and NTAT precision bandgap kernel

where EPC'_1, EPC'_2, ... are effective piezo-coefficients for σ_{xx}–σ_{yy} stress dependence. In (16.15a) C_{corr} is an analog or digital compensation factor that scales the oscillator frequency. In a practical circuit this can be the integration current or the fractional divider in a feedback loop of a PLL. If the oscillator frequency would also be sensitive to in-plane shear stress σ_{xy} it is straightforward to add a shear stress sensor (e.g. like in Fig. 16.7) in the same way as the σ_{xx}–σ_{yy} sensor and to add according terms in (16.15b). So the compensation principle (16.15) is versatile and can take account of all components of the stress tensor if necessary.

16.5.4 Compensation of Mechanical Stress on Precision Bandgap Circuits

Bandgap circuits in standard plastic encapsulated packages exhibit a notable drift of $1\dots4$ mV due to changes of mechanical stress on the circuit. These drifts are minimized by the use of vertical PNPs [33]. In the past a lot of effort was undertaken to improve temperature stability by chopping, dynamic element matching (DEM), and curvature-correction techniques [32]. Electrical lifetime drift is tackled by cascoding, applying symmetrical voltage stress on matched transistors, and by dynamic element matching DEM. By now the dominant residual error term seems to be mechanical stress drift [35]. The temperature stable voltage in Fig. 16.15 is

$$V_{bg} = \left(R^*/R\right) V_{PTAT} + V_T \ln\left(V_{PTAT}\right) - V_T \ln\left(RI_S\right) \tag{16.16}$$

with $V_{PTAT} = \Delta V_{BE} = V_T \ln(8)$. The voltage V_{PTAT} is proportional to absolute temperature. It depends only on the ratio of collector current densities of the bipolars, and so it does not depend on mechanical stress. Therefore, it is ideally suited for temperature sensors. The resistors R and R^* are p-doped poly—high ohmic resistors with a stress dependence of less than 5 %/GPa. With proper layout their ratio does not depend on mechanical stress. Hence, only the last term in (16.16) is affected by mechanical stress. So the mechanical stress drift of the bandgap voltage is caused by drifts of resistor R and saturation current I_S.

$$V_{bg}\left(\sigma_{ij} + \Delta\sigma_{ij}\right) - V_{bg}\left(\sigma_{ij}\right) = V_T \ln\left(\frac{R\left(\sigma_{ij}\right)}{R\left(\sigma_{ij} + \Delta\sigma_{ij}\right)}\right) + V_T \ln\left(\frac{I_S\left(\sigma_{ij}\right)}{I_S\left(\sigma_{ij} + \Delta\sigma_{ij}\right)}\right) \tag{16.17}$$

In (16.17) we wrote the complete stress tensor σ_{ij}, but for poly-silicon resistors and vertical bipolar transistors not too close to the perimeter of the die only the sum of in-plane normal stress components $\sigma_{xx} + \sigma_{yy}$ is relevant.

The compressive stress on the circuit in a plastic package at dry condition may be $\sigma_{xx} + \sigma_{yy} = -250$ MPa. During operation in the field the stress at the same temperature may relax by 90 MPa to -160 MPa due to moisture uptake. Then (16.11b) predicts a reduction of the saturation current of the VNPN by 4.7 %. With (16.17) this gives a rise of 1.1 mV in the bandgap-voltage. If the resistors R and R^* were n-doped vertical resistors with a stress dependence according to (16.6c) they would roughly compensate the drift of the VNPNs and the bandgap-voltage would decrease by 0.15 mV. In fact the stress sensitivity of pure vertical n-resistors is too strong so that it over-compensates the VNPN-drift. Thus, one can use $R^n_{V,L}$ instead of R^n_V in Fig. 16.8 to adjust its stress dependence. This approach is explained in more detail in Sect. 16.5.6 for Hall sensors, where it is better suited. For bandgap circuits it seems preferable to use resistors with smaller TCR than the low doped stress resistors R^n_V and $R^n_{V,L}$ because smaller TCR gives less troubles with curvature of bandgap voltage versus temperature. For less stringent requirements of analog
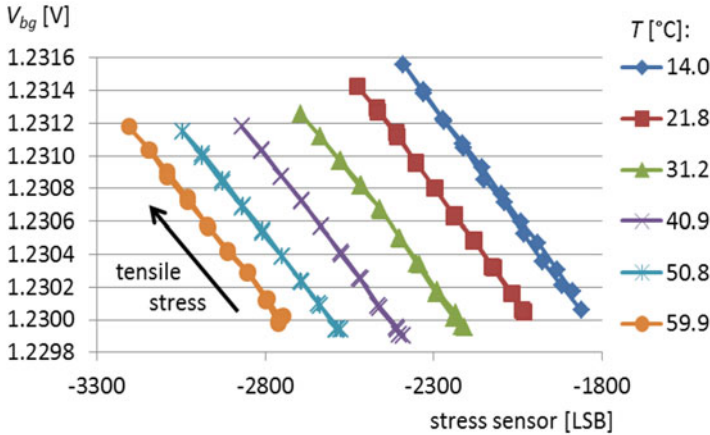
Fig. 16.16 Correlation between bandgap voltage of Fig. 16.15 and output of digital stress sensor for a typical sample. Stress was ramped up and down (0 ... 125 MPa) at various temperatures in a wafer stripe bending experiment

bias currents it is sufficient to mirror out an NTAT current generated by a VPNP, which is less stress dependent than a VNPN (see Fig. 16.15).

We implemented the circuit of Fig. 16.15 in a test chip and added a stress sensor with lateral/vertical n-doped resistors according to section 16.4(3) [34]. Then we measured a strong correlation between bandgap-voltage and stress sensor output during a wafer stripe bending experiment (Fig. 16.16). The bandgap voltage varies linearly with stress sensor output and with a constant slope at all temperatures. In practice the moisture drift in plastic encapsulated packages may reach values up to 90 MPa (for $\sigma_{xx} + \sigma_{yy}$) and in Fig. 16.16 this means a drift of about 1 mV.

A stress compensation of a reference voltage is preferably done digitally on system level instead of trimming it by analog means, which add further random errors. To this end, the system only needs a compensation factor C_{corr} as a function of temperature- and stress-signals similar to the RC-oscillator in (16.15). Figure 16.17 shows the performance of this compensation. There, stress was applied in a wafer stripe bending experiment to five devices at various temperatures. With a single value of effective piezo-coefficient for all five devices, the compensation algorithm reduces the stress drift times seven.

Figure 16.18 shows repeated thermal cycling on a packaged sample in "wet" condition. Without stress compensation, the curve 1 shows a clear hysteresis of 1.4 mV. If the compensation factor C_{corr} uses a constant value for the effective piezo-coefficient, then the hysteresis is only 0.4 mV. However, if C_{corr} uses an effective piezo-coefficient with -0.4 %/°C linear temperature coefficient, the hysteresis gets as small as 0.2 mV in the entire automotive temperature range.

Figure 16.19 shows an example how to combine stress compensation with precision analog circuit techniques like chopping, auto-zeroing, and digital assisted
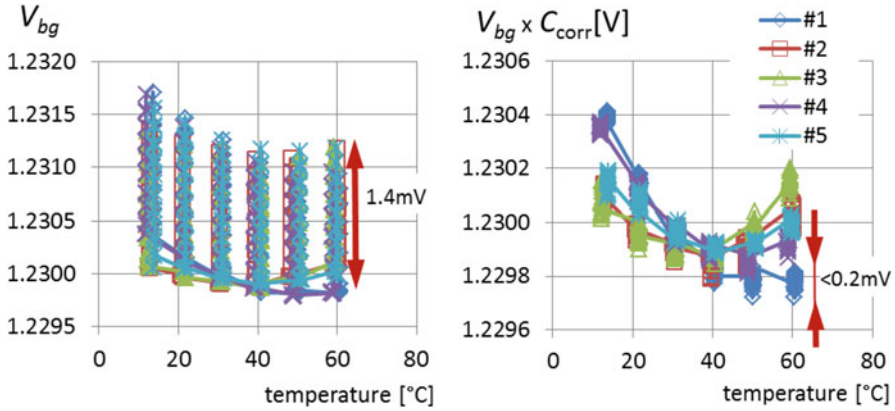
Fig. 16.17 The bandgap voltage of Fig. 16.15 without (LHS) and with (RHS) compensation of mechanical stress. Stress between 0 and 125 MPa was applied on five devices (#1 . . . #5) in a wafer stripe bending experiment
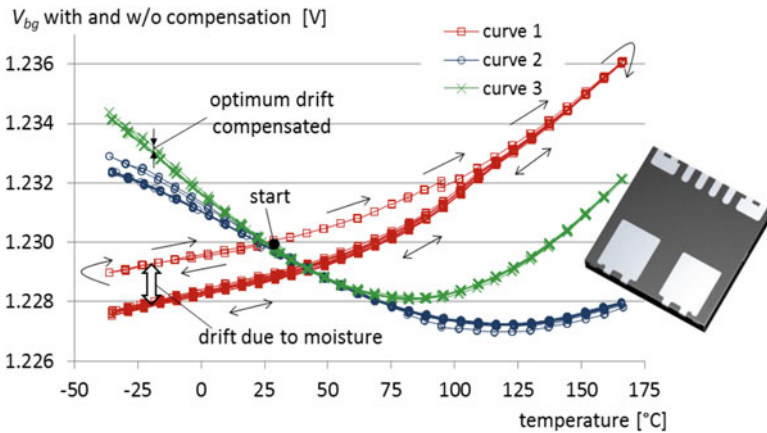

Fig. 16.18 Five thermal cycles applied to the circuit of Fig. 16.15 in PG-TISON-8-1 package measured after moisture soaking for 16 h in water at 85 °C. The effective piezo-coefficient is zero (*curve 1*), a fixed value (*curve 2*), and a temperature dependent value (*curve 3*)

signal processing in an economic and robust way [36]. Offset errors caused by mismatch and mismatch drift are equally large as mechanical stress related drifts, and therefore one has to combine mismatch cancellation techniques with stress compensation. The bandgap kernel is kept as simple as possible to make it predictable and robust against process spread: it only uses VPNPs and resistors with low TCR. Curvature correction, mechanical stress compensation, and single trim are shifted into the digital part. A control loop comprising an OTA pulls the bandgap kernel into its operating point. Offset and offset drift of the OTA (versus temperature, stress, lifetime) are cancelled out by chopping the OTA. This leads to
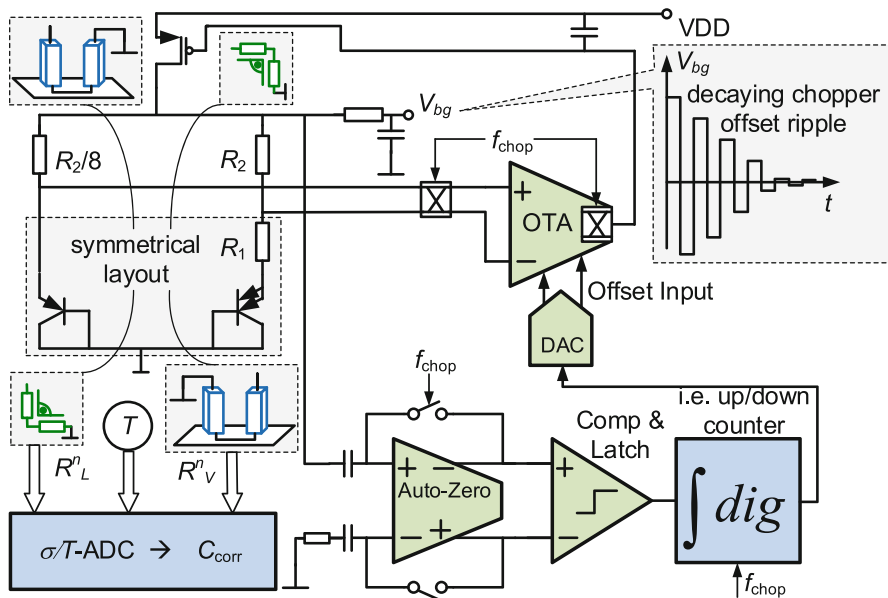
Fig. 16.19 Chopped bandgap reference in 0.13 μm technology with mechanical stress sensors for $\sigma_{xx} + \sigma_{yy}$ and digital assisted chopper ripple compensation

an offset ripple at chopper frequency at the output of the bandgap circuit. A digital assisted feedback loop compensates this offset ripple: The auto-zero comparator shifts the offset ripple from the chopper frequency into the baseband. There the offset is singe-bit quantized, which means that we throw away the amplitude information and only keep the sign. Therefore requirements for gain, speed, and linearity of the auto-zero comparator are relaxed. The sign-signal is integrated digitally by a simple up-down counter to get a multi-bit signal. This signal is fed into a DAC, which compensates the offset in the OTA. The requirements for gain accuracy and linearity of the DAC are also uncritical—it only needs to be monotonic. At transients of temperature or mechanical stress there is a decaying offset ripple at the output. Conversely, at steady state the system may freeze the DAC output, which opens the feedback loop. Then also the chopper can be switched off, to reduce residual glitches at the bandgap output and to save power. The chopper and the feedback loop can be re-activated if notable changes in temperature or stress are detected.

Drifts of mechanical stress and temperature are measured by respective sensors operated at low update rate. These drifts are cancelled out by versatile digital signal processing with a digital compensation factor C_{corr}. The idea is to use the uncompensated bandgap voltage V_{bg} as on-chip reference for ADCs in a system on chip and multiply the ADC output signal by C_{corr}. This digital multiplication is simpler than analog methods and it avoids additional errors.

The bandgap voltage and its residual temperature coefficient can be trimmed simultaneously at a single temperature, because the only errors left after chopping are PTAT errors [37]. At the same instant, the stress sensor output is trimmed to zero. All these trimming values define the digital compensation factor C_{corr}. The temperature dependence of the stress sensor can be designed to be nominally zero (Fig. 16.13) and the piezo-coefficients show little process spread.

16.5.5 Mechanical Stress on an LC-Oscillator

Figure 16.20 shows the drift of an LC-oscillator which was calibrated in a dry plastic package at several temperatures with an accuracy of ± 25 ppm [38]. After 48 h storage in wet condition, the oscillator frequency was re-measured versus temperature starting at $-40\,^\circ$C and a larger error of $+70/-125$ ppm was observed. It was also verified that a water droplet on the top of a naked silicon die does not change the oscillator frequency, which rules out purely dielectric effects. A plausible explanation for the observed drift is that the moisture uptake expands the mold compound, which reduces the compressive stress on the die. Thus, the size of the coil changes and this leads to a drift in the inductance and in the oscillator frequency. Yet, electronic compensation of this drift is more involved, because strain and not stress is at the origin of the drift. In a laminated package, strain and stress are not simply related via Young's modulus of silicon, but parameters of other package constituents also have an influence. The question is, if the correlation between strain and stress is stable enough for a given package so that one may still use a stress sensor. Further investigations are ongoing to examine the possibility for compensation of strain related drift. The target is to replace crystal and MEMs oscillators with on-chip LC-oscillators in certain applications in the future.
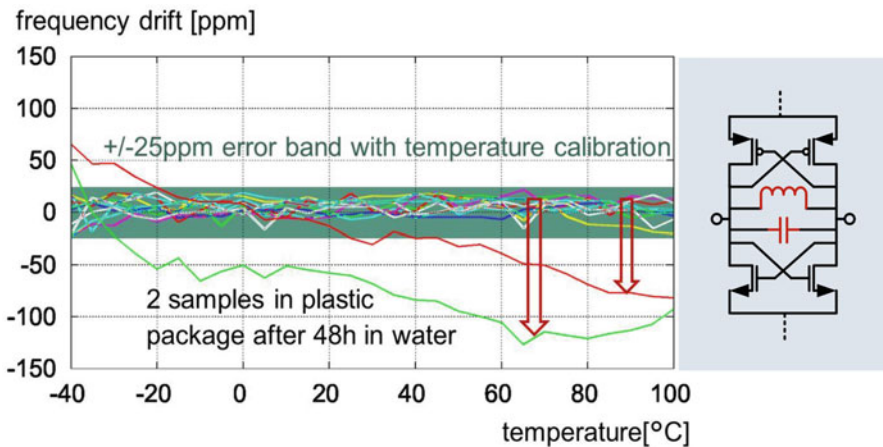

Fig. 16.20 Frequency drift of an LC-oscillator in plastic package: first calibrated vs. temperature in dry condition—then moisture uptake and re-measurement
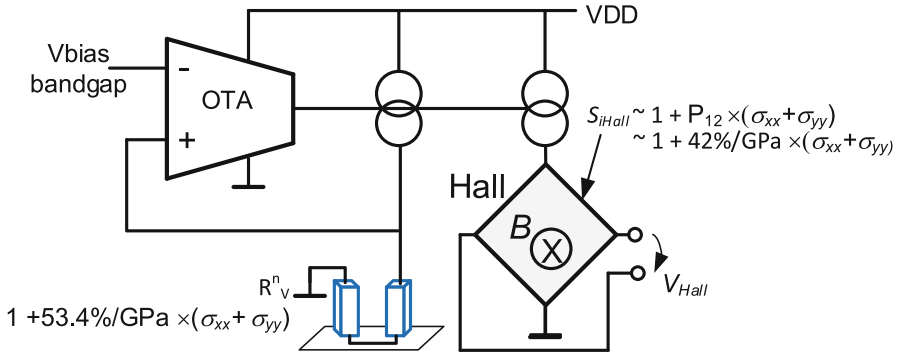
Fig. 16.21 Analog pre-compensation of Hall-plate without explicit stress sensor

16.5.6 Analog Pre-Compensation

In (100)-silicon vertical n-type resistors (incidentally) have only 20 % stronger stress dependence than n-doped Hall-plates (see (16.6c) and (16.12)). This can be used to pre-compensate the magnetic sensitivity against mechanical stress: A voltage of appropriate temperature dependence is generated by a bandgap kernel and copied onto a vertical n-type resistor. The resulting current is used as supply current for the Hall plate (Fig. 16.21). Thus, an increase in mechanical stress by 100 MPa increases the resistance of the vertical n-type resistor by 5.34 % while the bandgap referred voltage remains nearly constant versus stress. Consequently the current through the Hall plate decreases by the same percentage, yet the current related magnetic sensitivity increases by 4.5 %. The total magnetic sensitivity is proportional to the multiplication of Hall input current times current related magnetic sensitivity and therefore it decreases by 5.34–4.5 % = 0.84 %. So the stress dependence of the magnetic sensitivity of the Hall plate is reduced by a factor of 4.5/0.84 = 5.3. In practice the doping of Hall plates is larger than in (16.12), which reduces the piezo-Hall coefficient.

Yet, in practice, vertical n-type resistors always have some small lateral current flow contributions (see the bending of the current streamlines at the contacts of $R^n_{V,L}$ in Fig. 16.8). For a better pre-compensation over a large temperature range one can add two currents derived from lateral (R^n_L) and vertical (R^n_V) resistors via replica circuits from voltages with dedicated and adjustable temperature dependence like in Fig. 16.13 and adjust their ratio. The same principle can be used to reduce the mechanical stress sensitivity of Vertical Hall-effect devices (Fig. 16.22) [39]. Their current related magnetic sensitivity exhibits a roughly ten times smaller stress dependence than Hall-plates and it is also anisotropic (i.e. they respond differently to normal stress in x- and y-directions). One can adjust the size of the contacts in vertical resistors ($R^n_{V,L}$) or the spacing of the contacts in lateral resistors ($R^n_{L,V}$) in order to trim the piezo-resistive coefficients of the n-type resistors to perfectly match the piezo-Hall coefficients of the n-type Vertical Hall-effect device.
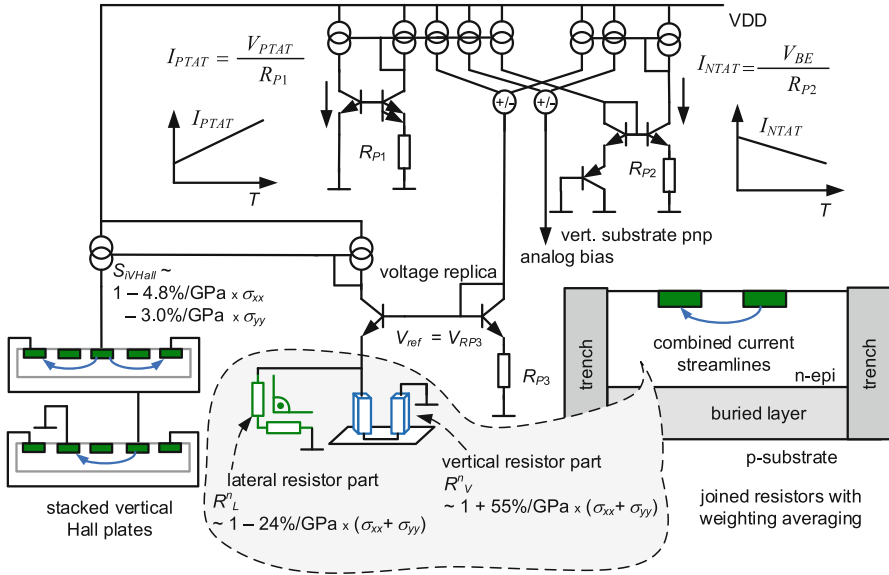
Fig. 16.22 Analog pre-compensation of vertical Hall-effect device

It should be mentioned that for magnetic field sensors it is also possible to use closed loop systems to make the magnetic sensitivity more stable against mechanical stress and temperature (and other) drifts [13]. They use on-chip coils placed near the magnetic sensor element to apply a magnetic reference field. However, the stability of the system is limited by the stability of the coil current. If the current is defined by an off-chip component (resistor), it suffers from tolerance, residual temperature coefficient, parasitics at the additional package terminal and/or EMC hazard and costs. If the current is defined by an on-chip resistor, one still needs a stable one, e.g. p-doped resistors in L-layout or on-chip metal resistors (which have even lower piezo-resistance) and one has to cope with its temperature dependence. Even more problematic is the fact that the system needs significant current (several milli-amps) to produce sufficiently strong field on sensors with moderate magnetic sensitivity like Hall effect devices. Conversely, the stress sensor needs only minute power (some 10 μA), space and extra system resources and it offers the additional advantage to monitor the package quality and detect its end of life.

Figure 16.23 shows layout suggestions how to arrange stress and temperature sensors around circuits which are compensated. These common centroids cancel out errors caused by linear stress gradients and temperature gradients.
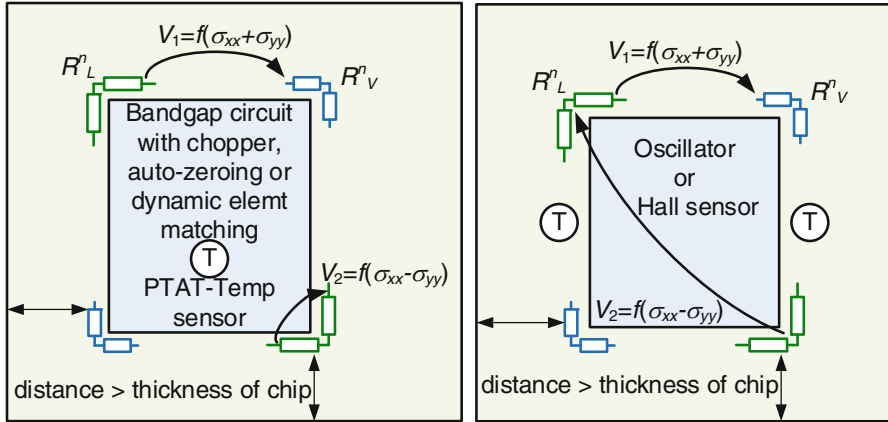
Fig. 16.23 Layouts of stress sensors and temperature sensors for thermal and stress symmetry and linear gradient rejection

16.6 Conclusions

In this paper we proposed electronic compensation circuits, which reduce the drift of integrated precision analog circuits caused by mechanical stress. This method reduces mechanical stress related drifts by a factor of 3 ... 10, thereby significantly improving overall accuracy and lifetime stability. This helps to meet the requirements for power efficient Li-ion battery management systems. Practical examples of Hall-plates, vertical Hall effect devices, bandgap voltages, system references, RC- and LC-oscillators were discussed. It was elaborated, that a crucial element for stress compensation circuits is a stress sensor that detects the sum of in-plane normal stress components. A more general mechanical stress compensation method was proposed, which uses additional sensors for other components of the mechanical stress tensor. Significant drifts of mechanical stress in common plastic encapsulated packages were found. They are provoked by moisture absorption, soldering, chemical cure shrink, and package disintegration. Mechanical stress sensors can detect these effects with negligible extra costs in terms of space and power consumption, thereby increasing the reliability of packaged ICs.

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