

Chapter 15

Heterogeneous Integration of High-Switching Frequency Inductive DC/DC Converters

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15.1 Introduction

Many electronic products are designed for compactness as shown in Fig. 15.1. Each sub-block is designed accordingly. The camera example in Fig. 15.1 features a tiny board crowded with a lens, a connector and a dedicated power supply (bottom right zone). This power supply occupies a significant part of the board and passive components are the major contributors.

It is a common knowledge that an industrial trend is to improve dramatically the power density of the power supply. Innovations cover the following fields: converter architectures, passive devices, control, design and packaging [1]. Recent literature covers many demonstrations of switched-capacitor converters either on-chip or in-package. Beyond the impressive results [2], switched-capacitor converters face a limitation due to the available capacitance density. This translates into a limitation in power density [3] where inductive converters offer a better trade-off at similar level of efficiency. This article will now on focus on high power density inductive buck converters for embedded products: this is called Power-System-on-Chip [1, 4]. Reviews of high switching frequency buck converters are available in [5, 6]. Following statements may be derived:

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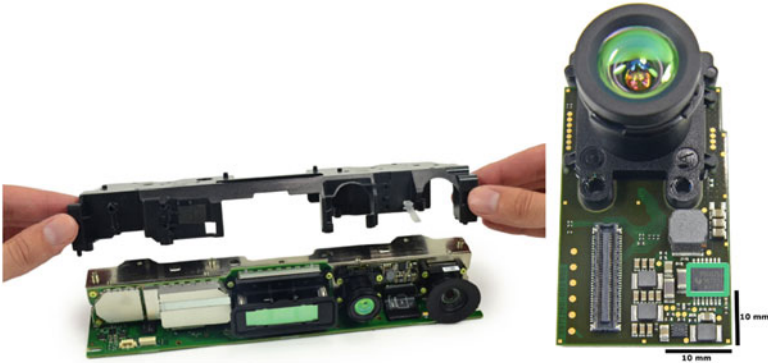


Fig. 15.1 Teardown of a commercial electronic product (*left*), zoom on the embedded camera (*right*) [on-line: www.ifixit.com/Teardown/Xbox+One+Kinect+Teardown/19725]

- The natural corner frequency of the output filter of the converter correlates with the switching frequency: the high switching frequency is used to enhance the converter transient performances but this is not a driving design indicator so far. Higher switching frequency is intended to reduce the values of passive components.
- The efficiency drops with increasing frequency. The efficiency figure must also be related to the output-to-input voltage conversion ratio. Selecting the literature results for given ratios, the different peak efficiency values drop in a similar manner. One result seems to be above the general trend (ratio of 0.5, [7, 8]).
- Efficiency profits from thin silicon technologies whatever the switching frequency.
- A penalizing effect of thin technologies is the limitation in input voltage range.

There is then a real challenge to handle a standard input voltage range (3.3 V) with a thin technology (CMOS 40 nm, 1.2 V). Efficiency in the vicinity of 90 % is reported in literature but for a high ratio of output-to-input voltage (larger than 0.85) [9]. A challenge is evidently to achieve similar efficiency but for a ratio below 0.5.

Various strategies are reported in literature to fight power losses inside a non-isolated DC/DC converter, namely a buck converter as considered here.

- Soft switching, either zero-voltage or zero-current schemes, has been applied to integrated buck converters [10]. Variability and parasitic devices are limitations to the optimization of the architecture. Moreover a shift in the actual switching frequency complicates the filtering of generated noise.
- Multi-phase architecture: the current is shared upon several phases and the Joule losses are reduced [10]. Independent inductors are considered generally. A phase shedding scheme enables to adjust the number of operating phase according to the actual output current, i.e. operates the exact amount of silicon necessary at one moment with respect to the output current.

- Multiple inductors may be coupled [11]. One magnetic device will then be affected by a current waveform at twice the switching frequency. At similar inductance values, the ripple is reduced. At similar ripple and inductance values, the switching frequency can be lowered, i.e. the switching losses in the active devices are reduced.
- Resonant gate drivers have been experimented [12]. The gain on losses is rather limited and does not compensate the penalty on silicon area to accommodate the air-core inductance needed for each single driver.
- Transistor width segmentation is an ultimate solution to adapt on the fly the silicon area to the actual output current [12]. This necessitates an evaluation of the output current. The scheme superimposes a modulation to the pulse-width modulation generally considered at high switching frequency. A risk exists for the stability of the converter.
- High-voltage MOSFETs create more switching and conduction losses than low voltage counterparts. Cascode association of low-voltage MOSFETs has been experimented to recreate a high-voltage MOSFET but with lower losses [13]. If a thin CMOS technology is to be considered, a cascode power stage is a solid candidate to stand high input voltage [7, 14].

With respect to the challenges considered here-above, it is reasonable to select hard switching operation at +100 MHz switching frequency. A cascode power stage fits the objective to rely on standard MOSFETs of the thin CMOS technology. Using coupled inductors inside a multi-phase architecture enables to reduce the values of passive components for a targeted output current ripple. The targeted system is pictured in Fig. 15.2 (left). Other specifications are listed in Table 15.1. Transient performances will not be considered here. In [15] is detailed a large-bandwidth voltage converter. The analogue voltage-mode control loop accounts for only 1.5 point of efficiency. In [15] is reported 78 % peak efficiency at the output power considered here with similar voltage conditions at input and output. The article details a proposal of a power stage that will limit power losses at similar switching frequency value. The power stage is detailed in Sect. 15.2.

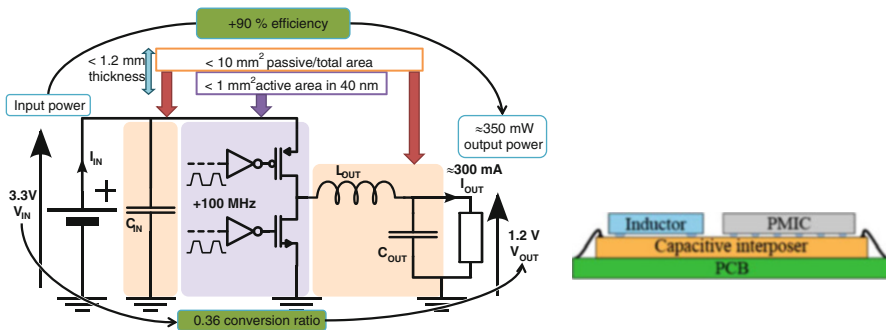
As explained later, interconnections are crucial for high-switching frequency operation. Moreover the converter should benefit from a high-quality decoupling at the input. A 2.5D approach is introduced with a capacitive interposer intended to receive the active part of the converter and the passive devices (Fig. 15.2, right). A high quality decoupling is obtained as detailed in Sect. 15.3. Measurements are given in Sect. 15.4.

15.2 Power Stage

The choice for a cascode configuration power stage stands as an alternative to the standard power stage, either with complementary transistors or with dual N-transistors, when the input voltage is of higher value than the transistor nominal

Table 15.1 Specifications of the target converter

Name	Min	Typ.	Max	Unit
V_{IN}	3.0	3.3	3.6	V
V_{OUT}	–	1.2	–	V
I_{LOAD}	50	280	500	mA
I_{SLEEP}	–	15	–	mA
$I_{STANDBY}$	–	150	–	uA
Static voltage accuracy	–2.5	–	+2.5	%
Dynamic voltage accuracy	–6	–	+6	%
Efficiency at $I_{LOAD, TYP}$	90	–	–	%
Efficiency at $I_{LOAD, MIN}$	80	–	–	%
Efficiency at I_{SLEEP}	70	–	–	%
F_{SW}	100	–	–	MHz
Ambient temperature	–40	55	125	Celsius
Package height	–	1.2	4	mm
Total area	–	–	10	mm ²
Technology platform	40 nm bulk CMOS by Infineon			

**Fig. 15.2** Schematic of the targeted power stage (*left*) and interconnection proposal (*right*)

drain-to-source voltage. Figure 15.3 shows three options. Details on the limitations of the standard power stage at high switching frequency have been reported in [15]. The 2-transistor cascode configuration has been reported in [7, 14]. Good results have been experimentally demonstrated and the conclusion is favorable to the cascode behavior. The configuration is generic and can theoretically be extended to a large number of transistors, due to the systematic arrangements [16]. The 3-transistor cascode power stage is pictured in Fig. 15.3 (right): physical implementation was first reported in literature by B. Serneels in [19, 20] in the context of high-voltage driver. Recently it was demonstrated in the context of a class-D amplifier [21]. Besides the capability of the 3-transistor cascode power stage was not demonstrated at high switching frequency.

The selected technology for silicon implementation (Table 15.1) must be considered here as a case where the nominal technology voltage (1.2 V) is not in range

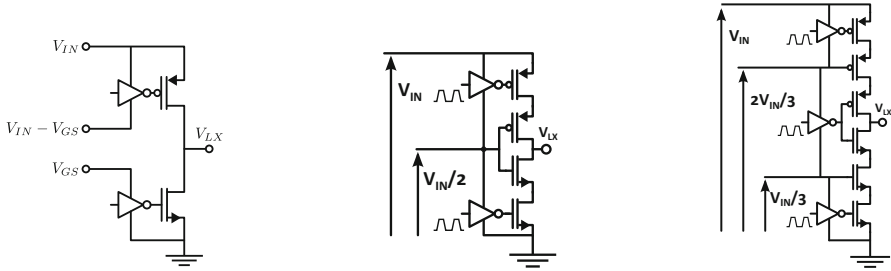
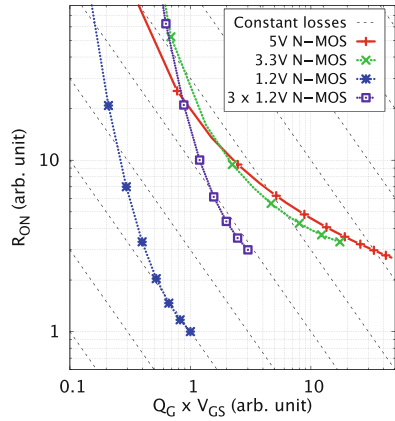


Fig. 15.3 Typical power stage configurations: standard (left), 2-stage cascode (center), 3-stage cascode (right)

Fig. 15.4 Figure-of-merit for transistor options in a standard CMOS 40 nm node



with input voltage (3.3 V). High-voltage transistors may be designed as Lateral-Drain (LDMOS) or Extended-Drain (EDMOS) structures. Transistors impact the power stage configuration in terms of losses and silicon area. Second-order issues are safe-operating-area, sensitivity to temperature or electro-magnetic-interference. Losses are related to the static on-state resistance and parasitic capacitances for given operating conditions (voltage, current, frequency, temperature). Depending on the channel width of a transistor, it is possible to evaluate the losses for given operating conditions. In nominal operating conditions for the targeted power stage, it is then easy to compare the impact of various transistor options depending on channel width or silicon area. Figure 15.4 pictures iso-value curves of losses in the $(R_{on}, Q_G \cdot V_{GS})$ plane as dashed lines. Lower losses are toward the bottom left corner. The figure-of-merit of several transistor options are then plotted. As expected the standard transistor is better in terms of losses and silicon area but can not stand the targeted input voltage. The 5 and 3.3 V transistor options are readily available to stand the input voltage but will not help reach the efficiency target. Fortunately stacking 3 standard transistors offers a better trade-off, hence the interest for the cascode power stage.

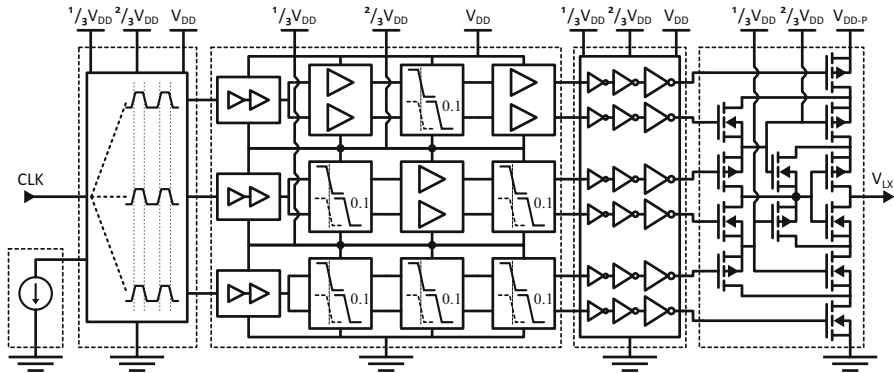


Fig. 15.5 Schematic of the power stage

As no transistors in the power stage is to stand more than 1.2 V, a systematic arrangement in the design leads to the schematic in Fig. 15.5. To take care of the Safe Operating Area of each power MOSFETs inside the cascode power stage, polarization MOSFETs have been added to the power stage.

The 3-floating drivers in Fig. 15.3 (right) are distributed on two-rows of local drivers, shared between the 3 transistors in the stack. This design is scalable to any odd number of transistors in the stack. Local intermediate voltage levels are required as $1/n$ of the transistor number in the stack. The generation of these local voltage levels as well as the associated efficiency are discussed at the end of the article. The power stage requires 3 driving signals with perfect synchronization. Skew within these latter signals is the key figure for robustness of the power stage. At 100 MHz (10 ns period), an accuracy of less than 100 ps has to be considered. Otherwise a transistor in the arrangement may have to stand a voltage higher than the nominal rating, hence inducing stress and aging. The layout of the power stage must comply to this objective: propagate synchronous signals from the global control input to the drivers' inputs through dedicated level-shifters to take care of the local change in voltage swings.

The power stage has been designed in a first step for continuous conduction mode (CCM) as the objective is to demonstrate the capability of a cascode configuration and the benefit of the 2.5D assembly. In Fig. 15.6, a color code represents the voltage levels from input voltage to ground respectively in red, blue, green and gray. In CCM operation Fig. 15.6 gives the mapping of voltages when the output voltage is respectively high (left) or low (right).

Active-well transistor is mandatory to cancel polarization of parasitic junctions in the cascode stage (Fig. 15.7, left and center). The final layout is pictured in Fig. 15.7 (right) where the power stage has been optimized for 150 mA output current and 100 MHz operation. A standard power stage with 3.3 V transistors was also designed for similar specifications and with similar care for purpose of comparison.

The full power stage requires 4 decoupling capacitors for the various input voltages. These capacitors, as well as the output filter capacitor, are removed off-chip to the passive interposer where the active die and the inductor will also take

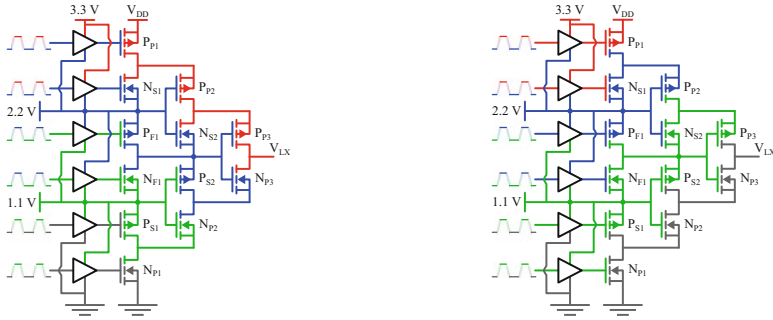


Fig. 15.6 Operation of the 2-stage cascode in CCM: high voltage on output (*left*), low voltage on output (*right*)

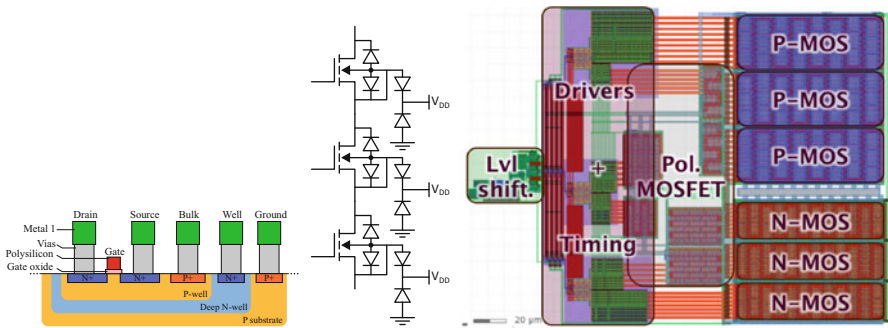


Fig. 15.7 Cross-section of the active-well transistor (*left*), 3-transistor cascode parasitic junctions (*center*), Layout of the power stage (*right*)

place. Decoupling capacitors’ values and the inductance value have been optimized with respect to output current ripple and output voltage accuracy constraints. Decoupling of main input voltage requires 33 nF with ESR accounted for 100 mΩ. Other decoupling capacitors are set to 11 nF with an accounted ESR of 150 mΩ. Finally the output filter capacitor is set to 16 nF (150 mΩ maximum ESR value and accompanied by an inductor of 60 nH (reference PFL1005-60NMRU).

15.3 High Quality Decoupling

In [12] is demonstrated a single stage of a buck converter for 200 MHz operation. Passive components are placed off-chip. Results show that dumping resistors had to be implemented on-chip to kill oscillations introduced by parasitic devices (L and C) between the off-chip devices and the on-chip power stage. Authors report a penalty of at least 2 points of efficiency. It is of utmost importance to reduce the length of interconnection between the decoupling capacitors and the power stage. The active

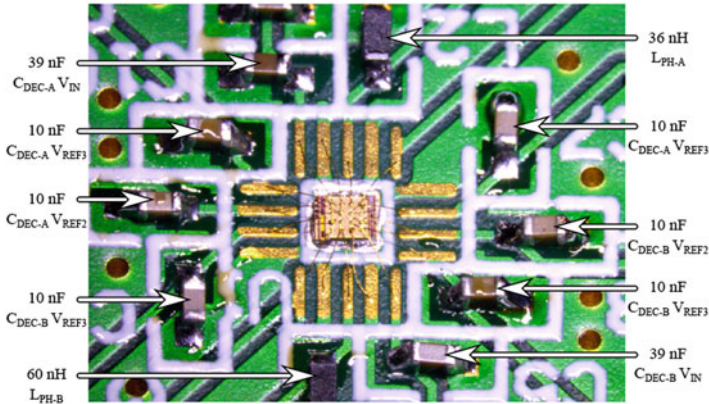


Fig. 15.8 Active die with off-chip passive devices on a board

Fig. 15.9 Capacitive interposer manufactured by IPDiA [17]

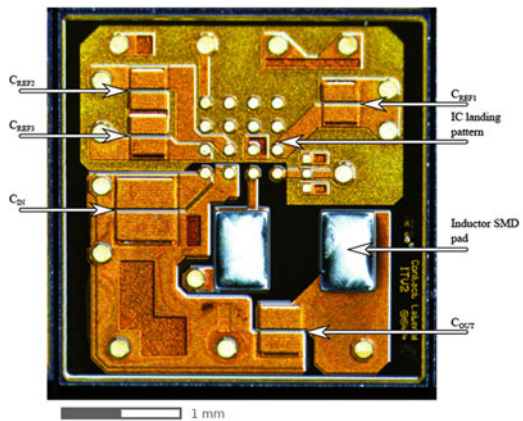


Table 15.2 Measured parameters of designed capacitor structures

	C_{MEAS} (nF)	ESR (mΩ)	SRF (MHz)
C_{IN}	33	70	330
C_{OUT}	16	110	490
$C_{REF1,2,3}$	11	150	630

die has been tested in a chip-on-board configuration with on-board passive devices. Figure 15.8 pictures the lengthy connections accounting for large parasitic devices.

In the present case, an interposer was manufactured by IPDiA to accommodate all decoupling capacitors, the output filter capacitor and all landing pads necessary to the flip-chipping connection of the active die and the inductor [17], Fig. 15.9. Table 15.2 lists the experimental performances of the embedded capacitors.

The various steps of converter manufacturing are summarized in Fig. 15.10. The obtained converter is pictured in Fig. 15.11 (left). It is ready to be connected to a system. For test purpose, samples are connected to a board through wire bonding

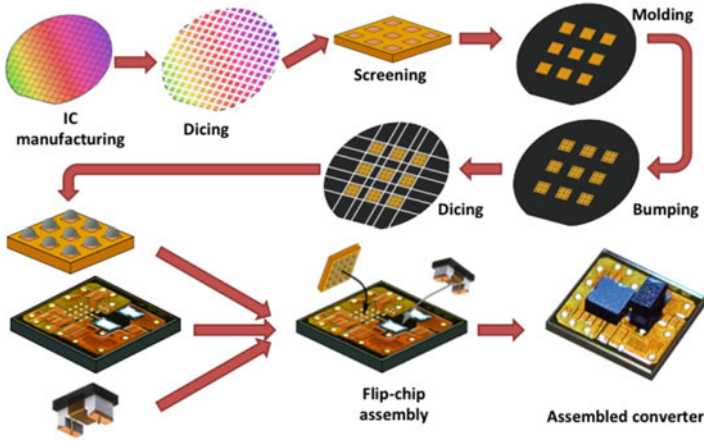


Fig. 15.10 Main steps of the 2.5D converter manufacturing

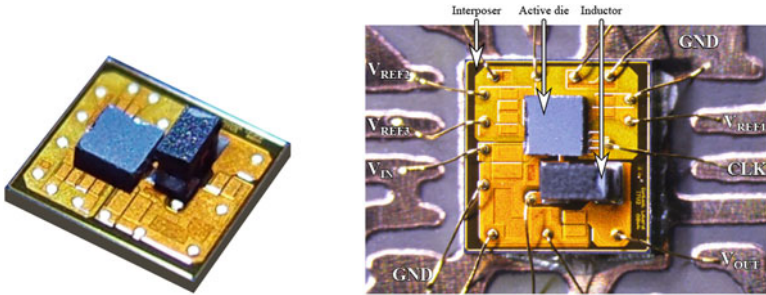


Fig. 15.11 Converter sample (left) and assembly on board (right)

(Fig. 15.11, right). No extra passive devices are added. Standard power stage and cascode power stage have been experimentally compared to interpret the benefit of interposer on the one hand, and the benefit of a cascode stage on the other hand. Measurements are presented in Sect. 15.4.

Measurements are not easy due to the compactness of the assembly. For the sake of internal signal sensing, the interposer in Fig. 15.9 is not optimal in geometry. Figure 15.12 gives the main parasitic devices awaited in the assembly when probing the power stage output voltage (V_{LX}) and the converter output voltage (V_{OUT}). Unfortunately this system of parasitic devices creates ringings and interferences in several configurations. Not all signals could be measured. As an example, Fig. 15.13 pictures the V_{OUT} node voltage when a probe is connected or not to the V_{LX} node.

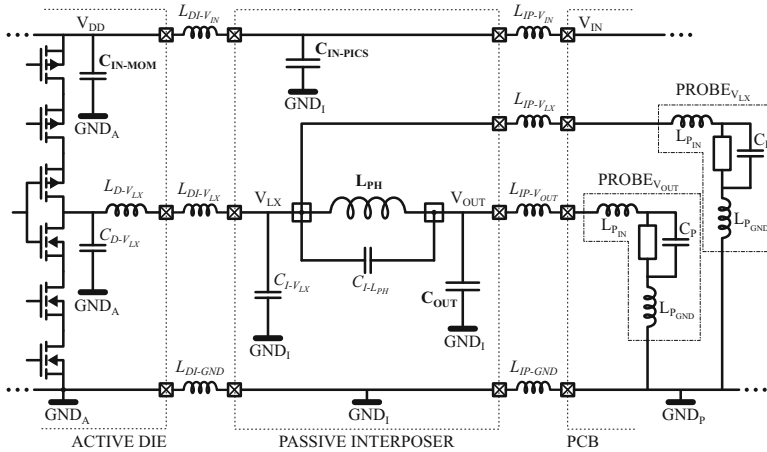
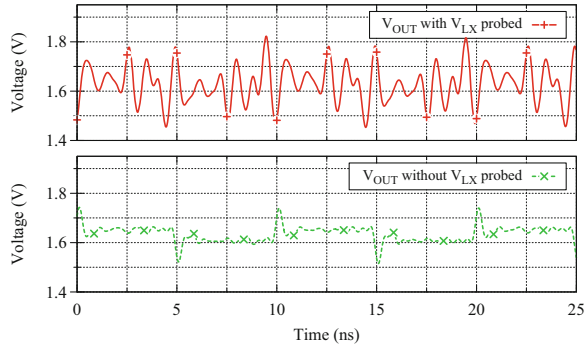


Fig. 15.12 Equivalent circuit to the 2.5 D converter from parasitic device point of view

Fig. 15.13 Measurements of output voltage in two sensing configurations



15.4 Measurements

One important thing is to assess the behavior of the cascode power stage. Synchronicity or skew are key parameters for the power stage robustness. So far experimental observation is carried out on observable signals. As said previously not all of them may be sensed without detrimental interference. The voltage at V_{OUT} node has been monitored in various operating conditions for both the standard and cascode power stage on the interposer with the same inductor value (60 nH) and same switching frequency (100 MHz). As shown in Fig. 15.14, it is impossible to detect a difference between the switching waveforms.

Efficiency is measured from total input and output power. The standard power stage has also an input voltage (3.3 V) and separate input voltages for the drivers. A mechanism of charge recycling between the drivers of the cascode power stage has not been explained but the consequence is that the currents drawn from the intermediate input voltages are very low. Figure 15.15 details some major results.

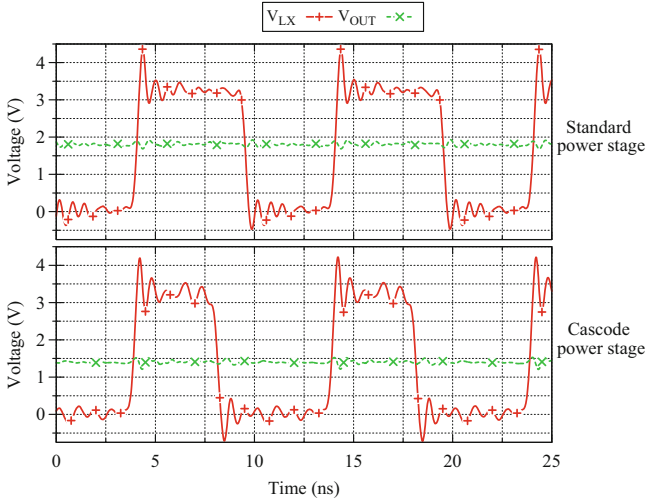


Fig. 15.14 Standard and cascode power stage behavior on interposer ($V_{IN} = 3.3\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 150\text{ mA}$, $f_{sw} = 100\text{ MHz}$)

First column compares the performance of the standard power stage on board and on interposer. It is obvious that in similar operating conditions, the interposer offers a benefit on efficiency of at least 4 points. This is mainly due to the reduction in interconnection parasitics. Voltage ringing is indeed very low and no particular precautions is to be taken inside the active part. Otherwise a technique is to insert resistance to dump ringings at the cost of additional losses. The first row in Fig. 15.15 shows that the cascode power stage offers superior performances than the standard counterpart. Somewhere 10 points of efficiency have been gained. They are repaid by some complexity in the design but the silicon penalty is affordable ($+0.006\text{ mm}^2$, i.e. $+14\%$). This efficiency budget can be used to operate the cascode power stage at 200 MHz with performances still comparable to that of the standard power stage at half the switching frequency. The converter footprint would be smaller if smaller passive component values are selected to keep the output current and voltage ripples equal.

Results in Fig. 15.15 are given in terms of losses in Fig. 15.16. Losses in the drivers and total losses from input voltages are separated for both power stages. Post-layout simulation (PLS) results are added as well. Distribution of losses over the standard and cascode power stages reflect the trend as given globally by efficiency figures. PLS results are in good agreement with measurements for drivers but not for other losses. In this case PLS results do not take into account the interconnection parasitics.

Finally it is interesting to look at the cascode power stage sensitivity to operating conditions around values considered for optimization (nominal current, nominal output reference voltage, nominal frequency). Figure 15.17 (left) indicates that the switching frequency does not significantly affect the efficiency in contrary to the

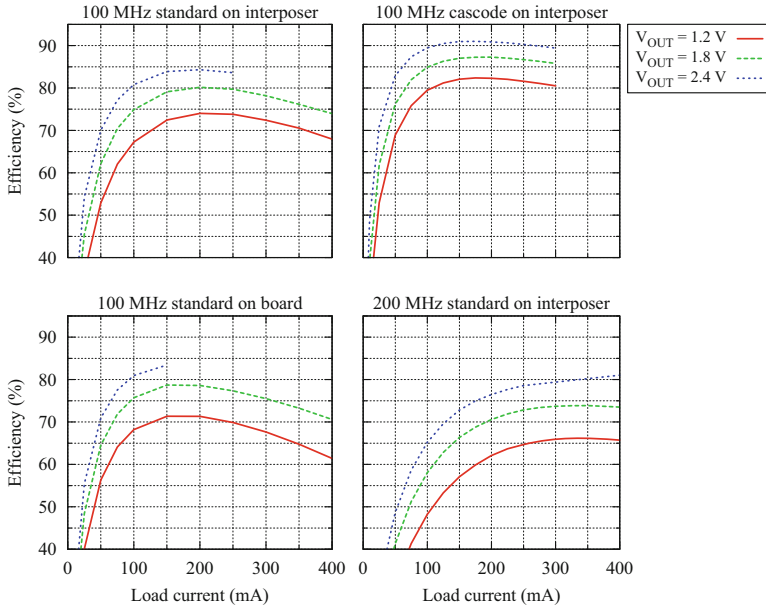


Fig. 15.15 Efficiency of standard and cascode power stages, on board or on interposer

input-to-output voltage ratio. Figure 15.17 (right) indicates that power transistor silicon area optimization is very sensitive. Drivers' losses remain insensitive to the output current and efficiency drops heavily apart from the optimization point. This corroborates the interest for multiphase architectures where the maximum output current is handled over the full number of phases. Lower output current values open the possibility of phase shedding.

15.5 Perspectives

The 3-transistor cascode power stage has been demonstrated in CCM and open-loop operation. One improvement will be to integrate the generation of the intermediate voltage level from the main input voltage through a switched-capacitor DC/DC. A redesign of the power stage is necessary to introduce two global input signals so as to be able to turn-off both the top and bottom side of the output stage. Voltage-mode control has already been demonstrated at 200 MHz for a standard power stage. This control option can be applied without any changes for the cascode power stage. More interestingly sliding-mode control could benefit from the rather insensitivity of efficiency to the switching frequency if the frequency range is limited. The fabricated interposer possesses landing pads for one inductor. A new version of the interposer must be fabricated to accommodate coupled inductors. Such a magnetic

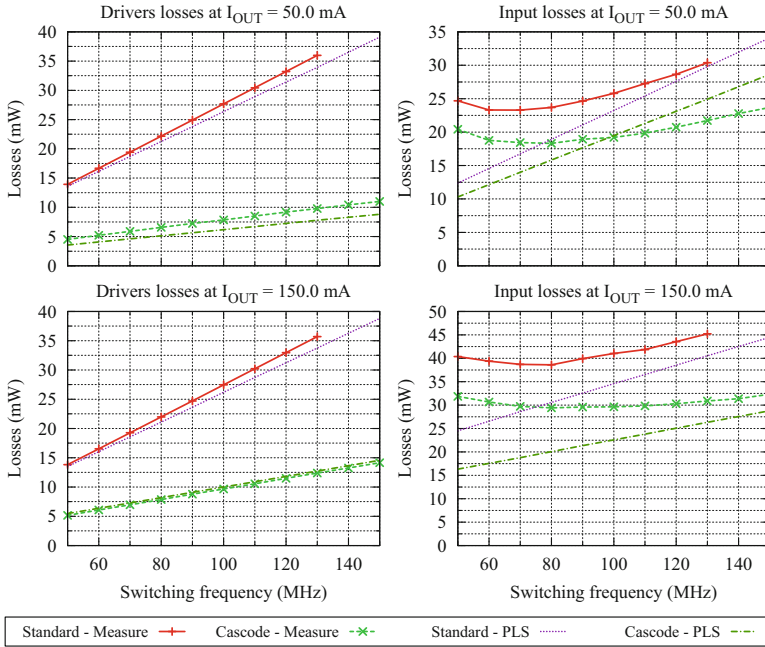
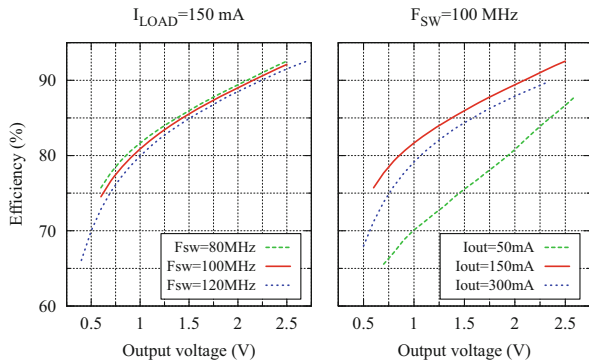


Fig. 15.16 Simulated and measured losses for standard and cascode power stage

Fig. 15.17 Efficiency of cascode power stage: sensitivity to operating conditions



device has been manufactured by Tyndall Institute upon specifications as pictured in Fig. 15.18 [18]. A rather discrete test board as pictured in Fig. 15.19 is unfortunately not sufficient as the magnetic device no more benefits from the proximity of the capacitive interposer.

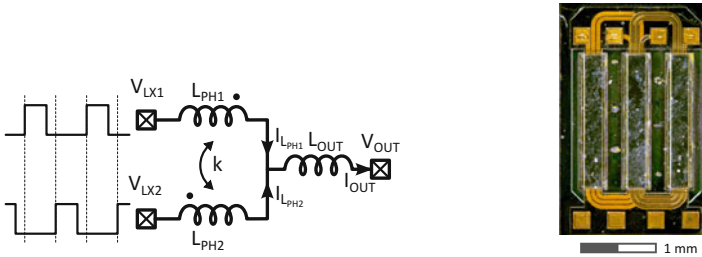
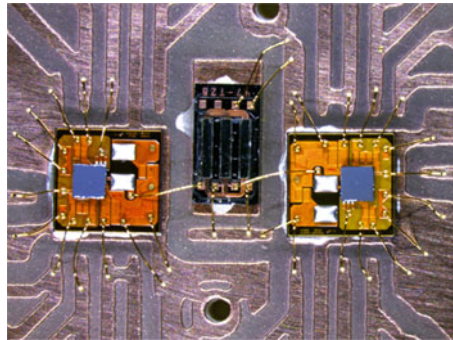


Fig. 15.18 Magnetic device suitable for a 2-phase buck converter (*left*) and integrated sample (*right*)

Fig. 15.19 Test board ready for functional verification of the two-phase buck converter



15.6 Conclusion

Low footprint DC/DC converters and/or low form factor DC/DC converters require further integration. When considered for System-on-Chip, the switched-capacitor architectures are preferable but high efficiency is related to the quality of embedded capacitors and on-chip deep trench capacitors are quite expensive. When the targeted power density leads to select an inductive architecture, the switching frequency is the degree of freedom to push the converter in the era of air-core inductors, compatible with on-chip manufacturing. However output power capability is limited. An intermediate solution to accommodate magnetic-core inductors is a 2.5 D assembly using a capacitive interposer. Each part of the system is to be manufactured with the cost-optimal industrial process compatible with the awaited performances. The article has shown the benefit of an interposer as interconnections between devices are shortened, hence lower parasitic effects at high switching frequency. On the other hand this article has reported the performances of a 3-transistor cascode power stage as a better trade-off between high input voltage and high efficiency in advanced CMOS technology nodes.

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