Chapter 14
Resonant and Multimode Switched Capacitor Converters for High-Density Power Delivery

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14.1 Introduction

Modern power electronics are driven by a constant need to improve efficiency in the effort to extend battery life of portable electronics, relax thermal constraints in power intensive applications, and help mitigate CO_2 emissions by reducing wasted energy. However, in a variety of applications, *size, form-factor, and ultimately the power-density of the energy-management subcomponents are becoming critical* as these constrain both cost and size of the packaged system [1–3]. By far, the most common power delivery architectures are based on inductive energy storage. For example, buck, boost, and transformer-coupled DC-DC converters currently dominate the market for typical low-moderate voltage and power applications. This places substantial pressure on inductive components to achieve both high volumetric energy- and power-density and also low loss at increasing switching frequencies [2].

To illustrate this, consider the well-known relationships for current and voltage ripple (Δi_L and Δv_C) in a conventional buck converter:

$$\Delta i_L \propto \frac{V_{IN}}{f_{SW} L}, \tag{14.1}$$

and

$$\Delta v_C \propto \frac{\Delta i_L}{f_{SW} C}. \tag{14.2}$$

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In Eqs. (14.1) and (14.2), V_{IN} is the supply voltage, f_{SW} is the switching frequency, L and C are the inductance and capacitance respectively. Also note that the units of (1) are [V-s/H] and units of (2) are [A-s/F]. Here, the tradeoffs among voltage, switching frequency, and size of passive components are readily apparent. For a fixed input voltage, the only way to improve the [V-s/H] FOM is by utilizing higher frequency or larger inductance. To improve the [A-s/F] FOM for a fixed Δi_L requires utilizing higher frequency or larger capacitance. To ultimately achieve higher power-density, these trends drive up switching frequencies, but demand also that active and passive components remain efficient [2–4].

Fortunately, trends in active devices are generally in support of higher switching frequencies. Scaled CMOS technologies are approaching f_{max} levels in the near-THz regime [5], providing increasingly efficient operation at switching frequencies appropriate for even the fastest power converters, although notably also trending towards lower breakdown voltages. At higher voltages, wide-bandgap technologies are gaining higher levels of integration while relaxing tradeoffs among breakdown voltage, frequency, and efficiency [6]. Capacitor technologies are also improving, one example being deep-trench technologies with densities approaching many 100 s of nF/mm^2—orders of magnitude higher than traditional MIM and MOS capacitors [7–9]. However, inductor components remain a key limitation in traditional buck and boost topologies, especially given the need for higher inductance-density while maintaining low-loss at high frequency. Available magnetic materials scale poorly to frequencies above 10 MHz, and air-core topologies remain practically constrained to (at most) 10's of nH for mm-scale geometries [2].

In the past decade, switched-capacitor DC-DC converters have gained academic and commercial interest due to a number of favorable architectural advantages and scaling properties [9–11]. In [12], it was shown that SC converters can outperform conventional magnetic-based topologies (buck and/or boost) purely in terms of conduction loss across a wide range of power and voltage levels. This is related to the active device figure of merit, the V-A product, which relates the breakdown voltage and peak current rating needed for all active devices in the circuit. More generally, the SC approach eliminates bulky and expensive magnetic components which often dominate size and cost, and limit operating frequencies due to core and winding loss. Another advantage that has emerged in favor of SC topologies is the ability to segment designs into *large numbers of interleaved phases* [9, 10, 13]. This capability enables two main advantages: in principle, interleaving can reduce input and output voltage ripple to near-negligible levels, permitting elimination of bypass capacitance and therefore full utilization of the available capacitance density for energy transfer. Interleaving also opens up the possibility of soft-charging the parasitic bottom-plate component, significantly reducing its impact on efficiency [8, 14].

However, the switched capacitor approach also has several limitations. First, it relies heavily on the capacitance density available in a given technology. While capacitive energy storage is often touted as superior to inductive energy storage

due to the relatively higher energy density of capacitors as compared to inductors, [3, 15], *to fully realize this advantage, a given converter must be able to access and utilize the available energy-density*. In the case of SC converters, accessing the available energy density comes with a penalty of higher charge-sharing losses. To mitigate charge sharing losses, SC converters remain constrained by a fundamental relationship similar to (2) and necessitate either high frequency or high capacitance to minimize conduction loss in the circuit. Therefore, an argument can be made that some of the recent performance gains in the SC area are derived largely from nascent component technologies (e.g. deep-trench capacitors) or advanced process options (e.g. deep submicron silicon-on-insulator technologies). Finally, while variable regulation can be achieved with SC designs through linear modulation of the output impedance, architectural reconfiguration [8–10], and recursive topologies [16], these approaches tend to result in lower efficiency and/or power-density. This is caused by the additional stray junction capacitance of reconfigurable architectures and higher series resistance in recursive approaches. It can also be appreciated that techniques which vary switching frequency to modulate output impedance trade off power loss for regulation capability and also cannot boost the output voltage above the nominal level.

Hybrid, soft-charging, and resonant operation of SC converters is increasingly promising to address some of the above-mentioned limitations [17–22]. In the resonant switched capacitor (ReSC) approach, the efficiency and power density of SC architectures are improved through the use of small magnetic components that resonate with flying capacitors and tune out their reactive impedance [23]. This approach also enables soft- or zero-current-switching (ZCS) which reduces power loss and stresses in the semiconductor components. Other developments in the ReSC area include the use of multi-mode operation to achieve variable conversion ratios and voltage regulation, and also to increase efficiency across the output power range [19–22]. Importantly, the ReSC concept extends and merges with a variety of SC architectures spanning Dickson, series-parallel, and flying-capacitor multilevel (FCML) topologies [19, 24]. While an inductive impedance is still needed, compared to traditional buck and boost topologies, the hybrid approach can operate with much smaller inductance as the switched-capacitor (SC) front end can reduce the energy storage requirements (volt-second product) in the inductor by a significant margin (potentially 10–100×).

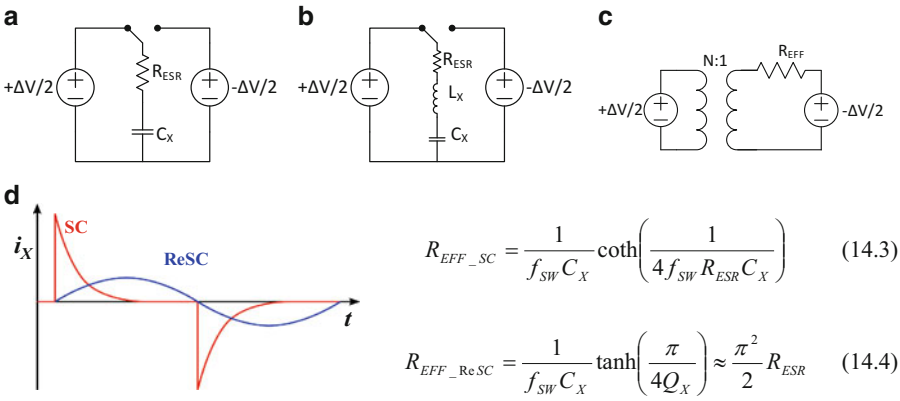
This paper will provide an overview or resonant and soft charging switched-capacitor DC-DC converters. Section 14.2 will discuss nominal resonant operation and a generalized comparison of SC and ReSC topologies. Section 14.3 will present candidate circuit architectures and their advantages and disadvantages. Section 14.4 will discuss an expanded suite of operating modes for hybrid and resonant SC converters. Section 14.5 will present implementation examples and future work in the space.

14.2 Resonant Switched Capacitor Converters

Consider Fig. 14.1a, b which shows simplified switching cells for nominally 1:1 SC and resonant switched capacitor (ReSC) converters. Here a flying impedance is switched between two voltage sources with a net voltage difference of ΔV. From the perspective of the flying impedance, this process presents a square wave of voltage, which in turn drives a respective current waveform. In the switched capacitor case, the current waveform is impulsive and is governed by the $R_{ESR} \cdot C_X$ time constant, where R_{ESR} represents the total resistance in the flying impedance loop and C_X is the flying capacitance. In the ReSC case, assuming the frequency of the voltage waveform is at the fundamental resonant frequency, f_0, of the impedance, the current waveform is sinusoidal with amplitude $\frac{2}{\pi}\frac{\Delta V}{R}$. These representative waveforms are shown in Fig. 14.1d. By integrating to get the charge transferred between voltage ports per cycle, it can be shown that in both cases, the process can be modelled as using an ideal transformer model with output resistance, R_{EFF} (Fig. 14.1c) [12, 18].

The equations that describe the parameter, R_{EFF}, for the 1:1 switching cells in Fig. 14.1a, b are shown as Eqs. (14.3) and (14.4). Here it should be noted that while the SC case is accurate for any switching frequency (f_{SW}), the ReSC case assumes operation at the fundamental resonant frequency ($f_{SW} \approx f_O$). Another distinction here can be made for the SC converter class: the 'coth' relationship in (3) governs the transition of the converter between the 'slow-switching limit' (SSL) and 'fast switching limit' (FSL). For example at low switching frequencies, (3) will approximate to $R_{EFF\_SC} \approx (f_{SW} C_X)^{-1}$, while at high frequencies to $R_{EFF\_SC} \approx 4R_{ESR}$. The boundary between the FSL and SSL is therefore defined here as $f_{FSL-SSL} \equiv (4R_{ESR}C_X)^{-1}$.

The ReSC relationship can be appreciated by examining the argument of the tanh in (4), which depends on the quality factor, Q_X, of the resonant network.



$$R_{EFF\_SC} = \frac{1}{f_{SW} C_X} \coth\left(\frac{1}{4 f_{SW} R_{ESR} C_X}\right) \tag{14.3}$$

$$R_{EFF\_ReSC} = \frac{1}{f_{SW} C_X} \tanh\left(\frac{\pi}{4Q_X}\right) \approx \frac{\pi^2}{2} R_{ESR} \tag{14.4}$$

Fig. 14.1 Ideal switching cells and behavioral transformer model. (**a**) SC cell; (**b**) ReSC cell; (**c**) behavioral; (**d**) respective current waveforms

For example, at high-Q, the relationship simplifies to $R_{EFF\_ReSC} \approx \frac{\pi^2}{2} R_{ESR}$. Then consider the ratio of R_{EFF_SC}/R_{EFF_ReSC}, while maintaining the assumption that $f_{SW} = f_0 << f_{FSL-SSL}$, and that C_X is the same for both. The result follows as:

$$\frac{R_{EFF\_SC}}{R_{EFF\_ReSC}} \approx \frac{4}{\pi} \frac{1}{2\pi f_0 C_X R_{ESR}} = \frac{4}{\pi} Q_X \tag{14.5}$$

Essentially, this indicates that at a given frequency, assumed resonant for the ReSC, and where $f_0 \ll f_{FSL\text{-}SSL}$ (operation below the FSL boundary), the effective resistance of the ReSC topology is $\sim Q_X$ times lower than the equivalent SC topology. The following conclusions can therefore be made:

1. For SC and ReSC topologies with the same C_X and R_{ESR}, at the same frequency, the ReSC topology can operate with Q times lower R_{EFF} (or conduction loss).
2. Given the same C_X and R_{ESR}, but now assuming the converters operate with the same R_{EFF}, the ReSC topology can operate at ~Q times lower frequency (or switching loss)

On the one hand, this seems like a compelling argument for the resonant topology as it provides a degree of freedom beyond what is available in the SC topology to minimize total power loss (or maximize efficiency). However, a limitation to the above analysis is that it neglects the additional losses associated with the inductor, which ultimately limits the achievable performance benefit. Another way to phrase this is that for the ReSC topology, it is *essential to consider the ESR of the additional inductor component* and its effect on power loss and efficiency.

In order to provide a more accurate assessment of the ReSC topology as compared to a comparable SC converter, a realistic model for available magnetic components must be included. Figure 14.2 provides one such comparison. Here, the power loss of a representative SC converter and ReSC converter is shown versus switching frequency. For the comparison, a fixed flying capacitance of

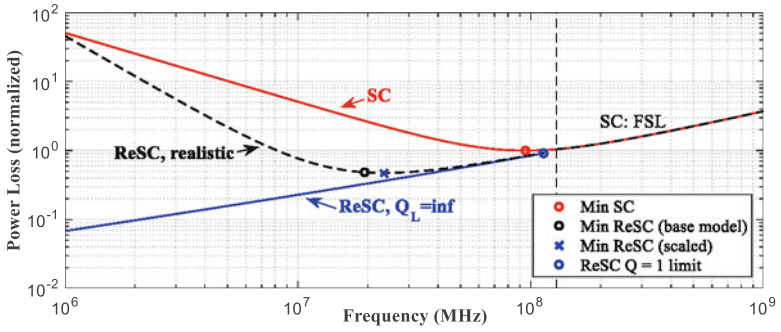


Fig. 14.2 Comparison of optimized SC and ReSC designs (nominally 2:1) given ideal and realistic assumptions about inductor ESR

10 nF with 1 % bottom plate ratio and load current of 1A was used. Also, all designs are assumed to be implemented in the same, representative CMOS process technology. It is also the case that all points on the curves are optimized at the given switching frequency (e.g. CMOS switches are sized to minimize total switching and conduction loss).

In-line with the analysis in [10], it can be appreciated that the SC converter optimization requires both a consideration of device sizes and switching frequency. In Fig. 14.2, the curve for the SC converter shows a minimum power loss at a switching frequency ~100 MHz. This happens to occur near the SSL-FSL boundary, as is found to be common in high power-density designs [18]. All power loss levels in Fig. 14.2 are normalized to the minimum SC power loss.

The curves for the ReSC case consider two scenarios: one where the inductor is assumed to add no parasitic resistance ($Q_L = \infty$, such that the effective quality factor, Q_X, is dominated by switch resistance only), and another case where a realistic mm-scale air-core inductor is used. For the $Q_L = \infty$ case, the conclusion is simply that the ReSC converter power loss scales in proportion to $\sqrt{f_{SW}}$. However, it can be appreciated that this is oversimplified because at fixed capacitance, lower switching frequency implies a larger inductor. Assuming the volume of the inductor is fixed, the ESR will scale in approximate proportion with inductance [2]. To second order, however, we assume that AC resistance in the inductor scales with $R_{AC} \approx k\sqrt{f_{SW}}$. Therefore, for a given base inductor model, ESR scaling depends both on inductance and frequency.

A representative curve for realistic ReSC performance is also shown in Fig. 14.2. Here it can be seen that, similar to SC designs, there is a minimum power loss associated with a particular operating frequency range. The predicted performance for the exact inductor base model, in this case coilcraft 0806SQ 6.9 nH with added 40 mΩ DC contact resistance, is able to achieve a factor of two reduction in loss compared to the best case SC design. This also occurs at ~5× lower frequency. The design could be very slightly improved by scaling the base inductance to an incrementally smaller level as indicated by the 'scaled' Min ReSC point. In all cases, the curves converge in the SC FSL. This is to be expected, as in the FSL, switch resistance dominates any reactive impedance in the circuit. Also note that an expanded set of 'realistic' ReSC curves can be generated by considering a range of inductor base models and physical size or volume [18].

14.2.1 ReSC Topologies

The simplified circuit schematics for two representative, nominally 2:1, ReSC topologies are shown in Fig. 14.3. Figure 14.3a shows the schematic of what we will term the 'indirect' ReSC. Here, four transistors, $M_{1\text{-}4}$ (assumed n-channel for simplicity), are controlled by switching signals $S_{1\text{-}4}$. In resonant operation, S_1 and S_3 are operated in phase, with S_3 shifted to the common mode of M_3. Switch signals S_2 and S_4 are operated complementary to S_1 and S_3. Assuming a nominal load current,

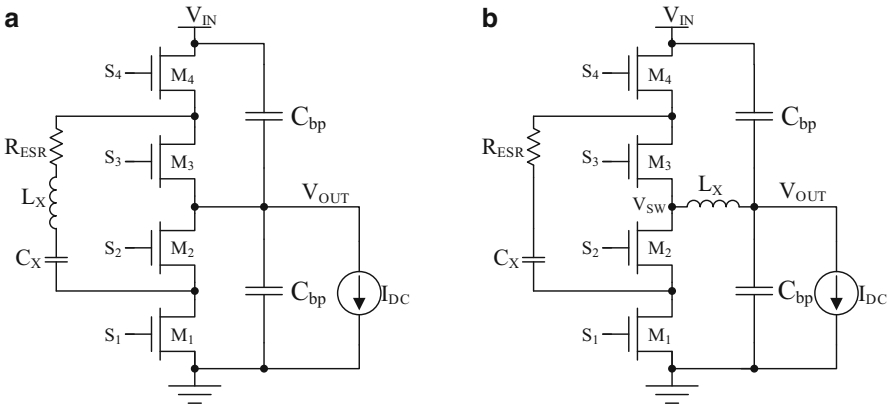


Fig. 14.3 ReSC topologies. (**a**) Indirect ReSC topology; (**b**) direct ReSC topology (3-level)

I_{DC}, V_{OUT} will be slightly lower than $V_{IN}/2$, driving a resonant current excitation in the flying impedance, assuming operation at the resonant frequency. Similar to the discussion of Fig. 14.1, the current in the inductor, L_X, will be sinusoidal with mean value of zero (C_X blocks DC current).

Figure 14.3b shows the schematic of what we will term the 'direct' ReSC. In this topology, the inductor directly connected to the output terminal. The switching process now modulates only the flying capacitance, C_X, similar to a nominal 2:1 SC converter. Also, R_{ESR} is shown as lumped with C_X, but in principle it should capture all resistance in the full resonant loop which includes switches, C_X, L_X, and one of C_{bp}. It should be apparent that the schematic in Fig. 14.3b is equivalent to the more well known 3-level buck converter, [25–27], which is a version of the general class of flying-capacitor multilevel DC-DC converters [28]. However, when we discuss this as the 'direct ReSC converter,' we are supposing operation at a resonant frequency. Also, the 'direct' vs 'indirect' distinction is similar to the distinction made in buck-boost DC-DC converters where in the 'direct' conversion case, the inductor current is unidirectional and couples directly to the output terminal in all phases.

Figure 14.4 shows representative current waveforms for the indirect and direct ReSC converters. In the indirect topology, it can be appreciated that all of the power in the inductor current waveform is concentrated at the fundamental resonant frequency. However, because the current waveform in the indirect topology appears as full-wave rectified, it has an appreciable DC component. It has been shown that approximately 80 % of the power in the indirect waveform is concentrated at DC [18]. The remaining spectral content appears at even harmonics of the fundamental resonant frequency.

Figure 14.5 overlays the power spectral densities of these waveforms (normalized to the total power) with the quality factor and ESR of a representative mm-scale air-core inductor versus frequency. In the modestly simplified inductor profile, the ESR

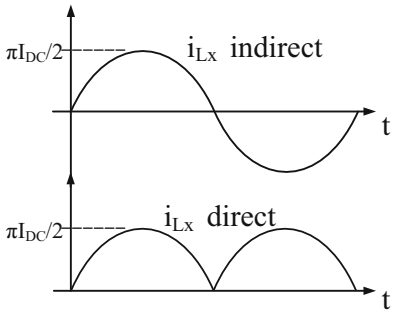


Fig. 14.4 Current waveforms

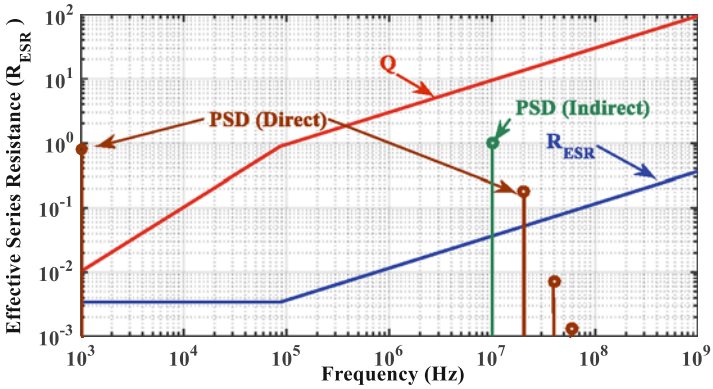


Fig. 14.5 PSD comparison: direct vs indirect

follow the DC resistance up until a frequency where the skin depth is approximately equal to the conductor radius. At higher frequencies ESR is dominated by AC resistance: $R_{AC} \approx k\sqrt{f_{SW}}$. Here, the advantages of the 'direct' approach are more apparent. Because of the large DC term in the PSD of inductor current, the direct topology has the advantage of lower effective resistance in the inductor component. As AC resistance may be much higher than DC resistance, this can provide a substantial reduction in power loss in the direct ReSC topology. A similar argument can be made for core loss, if cored inductors are considered, [19].

However, there are tradeoffs and cases where it may be more favorable to use the indirect approach. One disadvantage of the 'direct' topology is more complicated gate drive circuits and potentially higher voltage stresses on the CMOS switches. For example, the switches are exposed to the full voltage swing on the flying capacitor, C_X. The peak-peak voltage swing on the flying capacitor for the 2:1 converter in Fig. 14.2b. can be written as:

$$\Delta V_{Cs} = \pi Q_X I_{DC} R_{ESR} \approx \frac{8}{\pi} Q_X \Delta V, \tag{14.6}$$

where ΔV is again the net voltage difference between V_{OUT} in its nominal and loaded states (Fig. 14.1). Therefore, switches may be exposed to a voltage much greater than just $V_{IN}/2$ plus the loaded voltage difference, ΔV. Also, it is seen in (14.6) that this is a function of both the load and quality factor of the converter. However, in the indirect topology, switches are only exposed to ΔV itself because they are always coupled to common voltages constrained by bypass capacitors. Therefore the indirect topology may be able to achieve higher power or power-density levels for a given peak voltage stress on switching components, although with potentially lower efficiency.

14.3 Hybrid and Multimode Operation

Another opportunity in the hybrid SC converter area is the potential to leverage an expanded set of operating modes to affect variable regulation and higher efficiency across the output power range. For example, consider the direct (three-level) converter in Fig. 14.3b. In addition to nominally resonant operation, this converter can use additional switching states to couple the inductor to either ground or V_{IN}. The converter can also use high impedance (deadtime) states to provide discontinuous conduction mode (DCM-like) behavior. Similar operating modes have also been used for the indirect topology [21, 22].

Figure 14.6 shows an expanded set of operating states for the converter in Fig. 14.3b. As is well known in the 3-level buck converter literature, in scenarios with output voltages higher than $V_{DD}/2$, the converter can configure the inductor to V_{DD} for a portion of the switching cycle to increase the average voltage at the switching node, V_{SW}. Similarly, for scenarios with output voltages lower than $V_{DD}/2$, the converter can configure the inductor to *ground* for a portion of the switching cycle to decrease the average voltage at the switching node. This process results in equivalent 3-level operation because the voltage on C_X should attain a nominal level of $V_{DD}/2$.

The benefits and challenges of 3-level operation are well known. A primary benefit is the ability to reduce the inductance by a factor of four. A first factor of two reduction is achieved due to the additional mid-rail voltage level (reduces V in the [V-s/H] FOM). A second factor of 2 is achieved because the switching frequency is effectively double as there are now 4 switching states per cycle (reduces s in the [V-s/H] FOM). This advantage scales with higher conversion ratio (N-level) FCML topologies: in general, inductance scales inversely with N^2 for a constant [V-s/H] FOM or equivalently, constant current ripple.

However a central challenge of the 3-level (or N-level FCML) converter is maintenance of voltage balance on the flying capacitor(s) [28]. Without some mechanism to measure and correct for variation in the nominal voltage on C_X, this voltage can drift due to minor asymmetries in switch timing and load transients. Variation in the voltage on C_X can result in a reduction of efficiency or at worst, higher switching stresses and potentially breakdown failures of the power devices.

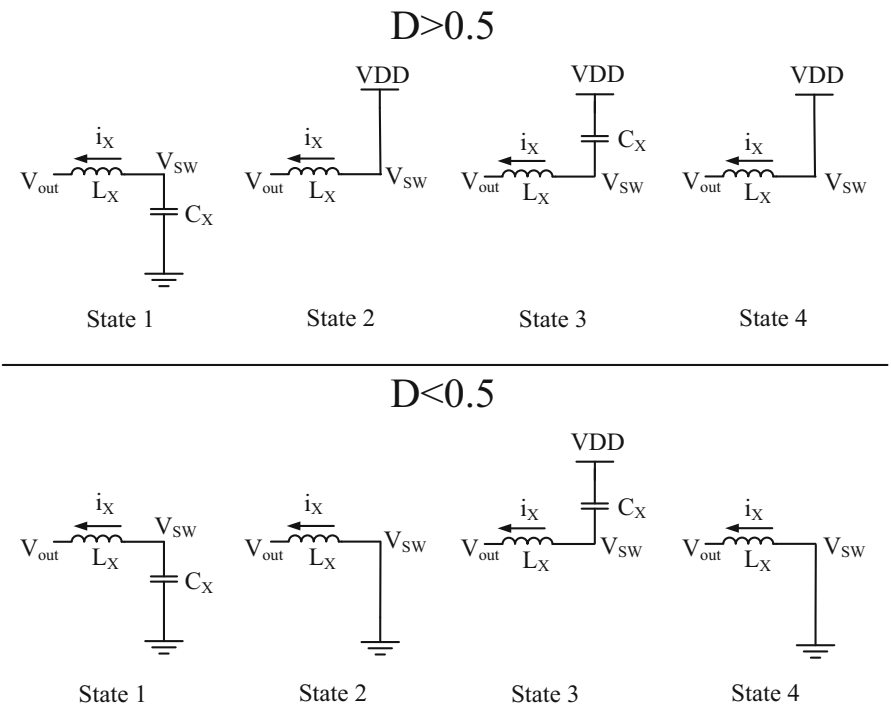


Fig. 14.6 Operating states for variable regulation modes

Here it should be noted, that while this problem is known in the 3-level and FCML converter classes, in [19], it was shown that the same problem affects all hybrid inductive SC converters.

While the 3-level converter is most well known as an augmented form of the buck converter, it merges into the ReSC circuit class. For example, depending on the switching frequency and voltage conversion ratio, the inductor current may take on a variety of forms spanning resonant, quasi-resonant, continuous, and discontinuous conduction. Figure 14.7 shows these possible operating modes segmented by voltage ratio and conduction angle. For the 2:1 3-level converter, the factor, *k*, is ½, but it can be appreciated that similar operating modes are possible in a wide range of converter topologies with different nominal conversion ratios.

Here, the inductive mode is identical to the 3-level buck converter. Also, similar to the standard treatment of the buck converter, the switching frequency is well beyond the LC corner and the inductor current approximates a triangle wave. The duty cycle can be used to affect variable output regulation both above and below the nominal conversion ratio 1:k (note that only step-down modes are shown in Fig. 14.7). Also, depending on the load current level, the converter may operate

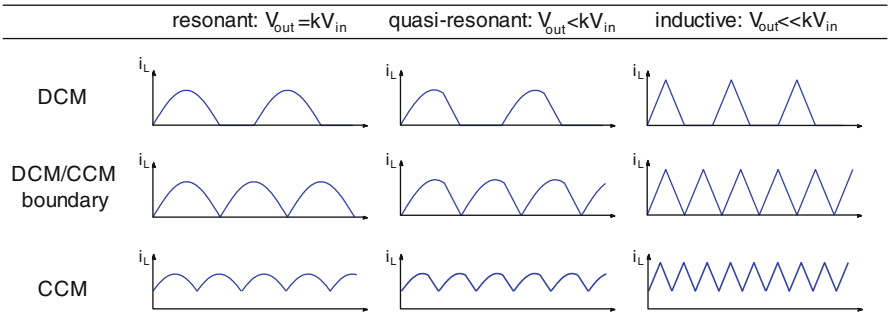


Fig. 14.7 Multimode operating scenarios: inductor current

more efficiently in continuous conduction mode, CCM (at high load current), or DCM (at low current). Pulse frequency modulation (PFM) control is also possible, and is treated here as a form of DCM.

As switching frequencies are reduced, however, the hybrid inductive-SC topology enters a quasi-resonant mode of operation. For example, in the switch states that couple L_X and C_X directly, resonant operation happens when $f_{SW} \approx f_0$. The quasi-resonant mode is therefore used when both lower frequency operation is most efficient and when variable regulation is needed. In quasi-resonance and when the output voltage is less than the nominal conversion ratio, the inductor current follows a partial resonant cycle (during *State-1* and *State-3* in Fig. 14.6) and then is linear during a hard switched state (*State-2* and *State-4* in Fig. 14.6). For the case where output voltage is greater than the nominal conversion ratio, the linear and resonant states are switched to affect a higher average voltage at the switching node, V_{SW}, but the same principle applies.

In pure resonant mode, the inductor current waveform can take several trajectories depending only on the switching frequency. For example, when $f_{SW} = f_0$, the converter operates in resonance with zero-current switching transitions. If a long dead-time is inserted between these transitions, the converter can operate in a DCM mode. This mode is the same as the dynamic off-time modulation (DOTM) mode discussed in [22]. DCM is useful to affect variable output regulation by tuning the loadline of the converter, much like in the SC case. It is also useful to provide higher efficiency in light load as it can be shown that both conduction and switching loss scale linearly with switching frequency. At higher switching frequencies, the converter enters CCM where zero-current-switching no longer occurs. CCM is useful at high load currents as this can be used (much like in conventional buck converters) to reduce the ratio of RMS/DC current in the inductor, providing higher efficiency [19].

Figure 14.2 is a plot of output impedance, R_{EFF}, normalized to the total (parasitic) series resistance, R_{ESR}. The x-axis is switching frequency, normalized to the SSL-FSL boundary frequency for an equivalent SC converter. The plots include the cases for pure (direct) ReSC converter, SC converter, and the hybrid approach

discussed above. Each of the circuits operate with the same total flying capacitance, C_X, and assume the same parasitic resistance, R_{ESR}. While the resonant and hybrid cases must accommodate the additional ESR of the inductor component, for simplicity this is neglected here.

Across the operating frequency range, it can be seen that the SC output impedance (curve 1) follows an expected relationship, i.e. (3). The pure ReSC converter (which assumes the 'direct' topology) also follows the expected behavior, quantitatively detailed in [18, 19]. However, the hybrid multimode approach traces out a more favorable curve than both previous topologies. For example, below the resonant frequency, the hybrid approach maintains the advantage of Q times lower R_{EFF} than the SC topology, while still permitting a linear tradeoff between switching and conduction loss. Above the resonant frequency, the hybrid approach enters CCM and the effective resistance approaches R_{ESR}, but at approximately Q times lower frequency than the equivalent SC converter. While derivation of the equation for R_{EFF} versus frequency for the hybrid topology is complicated, it can be captured by a behavioral model somewhat similar to the 'root-sum-squared' model [12], often used for the SC approach:

$$R_{EFF\_hybrid} = \sqrt[\alpha]{1 + \left(\frac{\pi^2 f_0}{8 f_{SW}}\right)^{\alpha}} * R_{ESR}. \tag{14.7}$$

In Eq. (14.7), f_0 is the resonant frequency, f_{SW} is the switching frequency, and α is a behavioral term that can be fit in a regression model for the given converter. It can be shown that a value of $\alpha \approx 9.2$ provides a behavioral fit to the actual model with a worst case error of approximately 2 %.

Importantly, what is shown in Fig. 14.8 and Eq. (14.7) is that the behavior of the hybrid inductive-SC DC-DC converter family is quite similar to the behavior of the underlying SC circuit family. The advantage can be quantified by the quality factor, Q_X, of the converter and the resonant frequency. While the control, gate driving, and design procedure is somewhat more complicated than a pure SC design, the

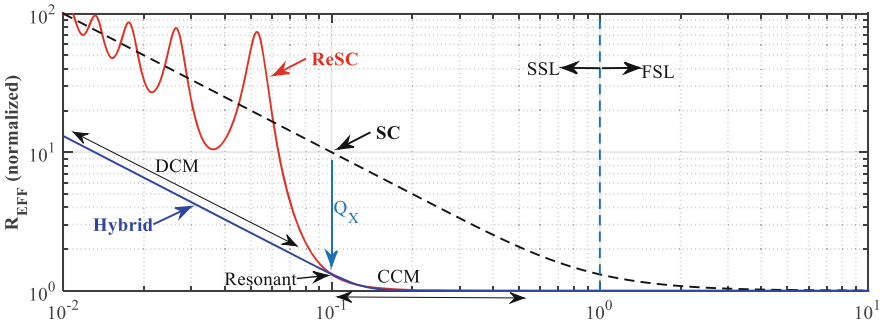


Fig. 14.8 Normalized output impedance: R_{EFF} vs switching frequency

macro-behavior is similar and can be generalized into a unified relationship, (14.7). However, while the variety of operating modes permit loss minimization across the output power spectrum, the hybrid converter class has the advantage that it can also provide variable voltage regulation without reconfiguring the native converter architecture.

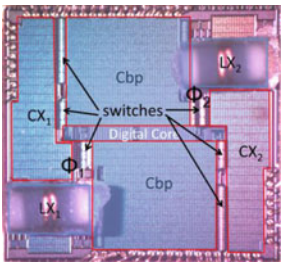
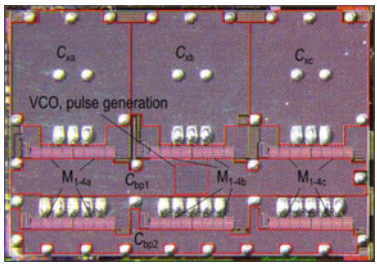
14.4 Implementation Examples

To justify some of the above discussion, here we present several recent implementations of hybrid-multimode, nominally resonant switched capacitor designs. In 2014 [22], presented a nominally 2:1 ReSC that utilized DOTM or the DCM concept highlighted in Fig. 14.7 to regulate the output voltage below the nominal level. This design used die-attached mm-scale air-core inductors and on-chip flying and bypass capacitors to achieve 85 % efficiency at 0.64 W/mm^2 in 180 nm bulk CMOS. In 2015 [21], presented a nominally 2:1 ReSC with 3-phase interleaving and an all N-channel power train to further improve efficiency and power-density to 89 % at 0.75 W/mm^2. The three-phase design used mm-scale printed circuit board (PCB) trace inductors with inductance values of 1.1 and 4.5 nH. Regulation was achieved using quasi-resonant modes similar to those in Fig. 14.7 to boost the output voltage above the nominal 2:1 level, and reduce it below this level as well. An overview of these designs and specifications is shown in Table 14.1.

More recently, several discrete implementations were built to explore further aspects of multimode operation of nominally resonant SC converters. The work in [19] explored hybrid multimode operation of 3-level and 4-level flying capacitor multilevel (FCML) DC-DC converters. The 3-level prototype operated exclusively at nominally 2:1 conversion ratios. By varying the frequency, as shown in Fig. 14.7, the converter was able to seamlessly transition from CCM operation (high frequency), to resonant operation, and finally to DCM by inserting a variable deadtime in between resonant transitions. Figure 14.9 shows measured efficiency for the 24 to 12 V step-down converter for load currents ranging between 100 mA and 10 A ($\sim$1.2 W to 120 W output power). While peak efficiency in the resonant mode was over 99 %, the converter was able to seamlessly transition to CCM at higher current and DCM at low current to maintain high efficiency (over 98 %) for most of the load range.

In another implementation, operation across the full suite of possible operating modes was explored. Figure 14.10 shows the printed circuit board design that can be operated as a 3-level or 4-level FCML. Ceramic flying capacitors (4.7 μF, X7R) and an inductance of 600 nH were used with a resulting resonant frequency of approximately 100 kHz. All different operating regimes described in Sect. 14.3 were tested in 3-level operation and measured inductor current waveforms are shown in Fig. 14.11. These can be compared to the theoretical waveforms in Fig. 14.7. It can be seen that based on the required conversion ratio and resulting duty cycle

Table 14.1 Highlights of previous designs using resonant-multimode operation

Source	Kesarwani et al. [22]	Schaef et al. [21]
Die photo		
Converter	2-Phase nominally 2:1 ReSC	3-Phase nominally 2:1 ReSC
Regulation	Dynamic off-time modulation (DOTM or DCM)	Variable quasi-resonant buck and boost modes
Power train	Complementary	N-channel with bootstrapped gate drive
Inductor(s)	Die attached mm-scale air-core (1.9–5.5 nH)	Printed circuit board trace inductors (1.1–4.5 nH)
Capacitor(s)	Flying ∼18 nF MIMBypass ∼22 nF MIM	Flying ∼25 nF MIMBypass ∼12 nF MIM
Process	180 nm Bulk CMOS	180 nm Bulk CMOS
Size	∼3 × 3 mm	∼3.8 × 2.6 mm
Frequency	∼20–30 MHz	∼20–50 MHz
Efficiency @ power density	∼85 % @ 0.64 W/mm^2	∼85 % @ 0.91 W/mm^2 (1.1 nH)∼89 % @ 0.75 W/mm^2 (4.5 nH)

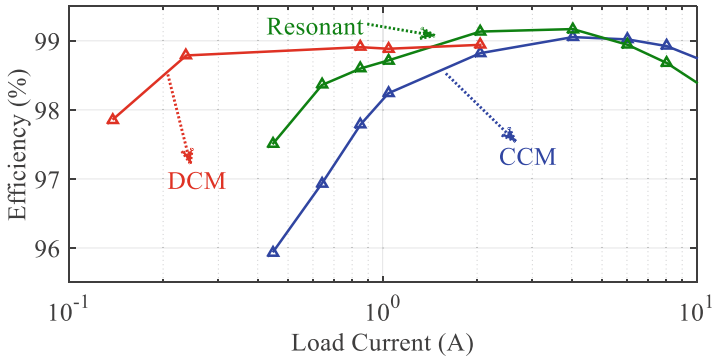


Fig. 14.9 Measured efficiency vs load current: discrete, nominally 2:1 (24 V:12 V) ReSC converter using multimode operation [19]

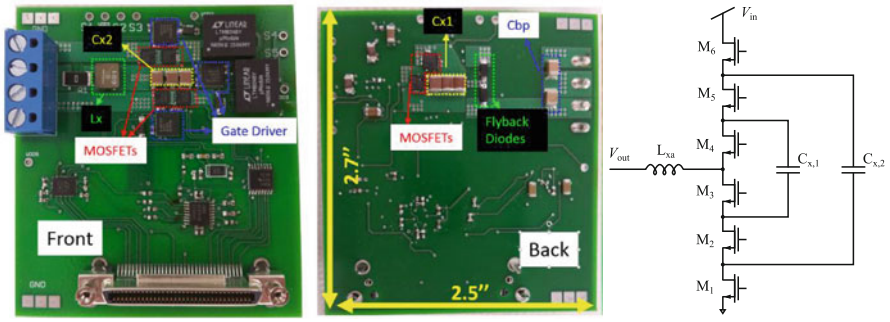


Fig. 14.10 Printed circuit board prototype: 3-level and 4-level FCML DC-DC converter

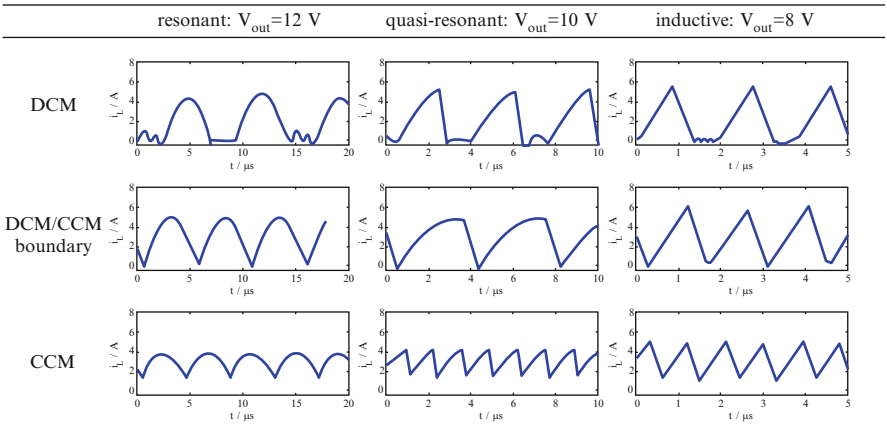


Fig. 14.11 Measured operating waveforms for discrete converter prototype shown in Fig. 14.10. These can be compared to the theoretical curves in Fig. 14.7

that the converter shows resonant, quasi-resonant or inductive behavior. Moreover, the frequency can be modulated to achieve DCM or CCM behavior to maximize efficiency for various load currents.

These operating modes can be demonstrated for 4-level operation and generally apply to all resonant or hybrid switched capacitor converters. However, the resonant frequency in different phases of operation can vary and careful tuning of the individual periods is required to achieve efficient operation as shown in Fig. 14.12 for the 4-level converter. As different flying capacitor configurations are connected in series with the inductor, the pulse widths in resonant operation need to be tuned to the resulting resonant periods in each phase to maintain the required voltage balance on the flying capacitors. Moreover, the pulse-widths need to be adjusted across the different operating regimes, e.g. in CCM operation the pulse-widths need to be of equal length to maintain charge-balance. Efficient multi-mode operation is therefore not only a design challenge but also requires careful consideration of the control strategy.

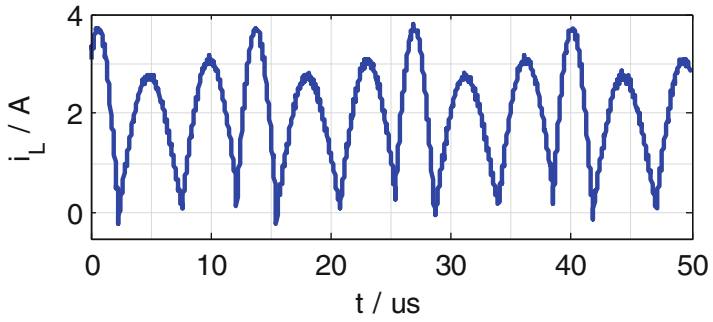


Fig. 14.12 Measured operation of the 4-level FCML in resonant mode: note that resonant frequencies in different phases is variable and requires careful tuning

14.5 Conclusions

In order to meet the challenges of future high-density power management applications, there is a need to explore architectures that break from the fundamental constraints that limit conventional DC-DC architectures. While the switched capacitor approach is favorable for many of these applications, it also has limitations that will continue to constrain efficiency, power-density, and the capability for efficient voltage regulation. Hybrid and resonant SC converters show tremendous promise to address some of these challenges. While the limitations of current inductor technologies must be factored in, the hybrid approach has many of the same scaling features and promising attributes of the SC circuit class. In this paper, we have shown also that hybrid-inductive SC converters have many of the same capabilities as more conventional DC-DC converters: the ability to regulate output voltage efficiently, and the capability for multi-mode operation to maintain high efficiency across the output power range. However these topologies benefit greatly from merging the advantages of both SC and inductive converters: the volume and inductance of magnetic components are greatly reduced while the utilization of the capacitor energy density is increased.

Going forward, there is a great opportunity for future work on hybrid, soft-switching, and resonant switched capacitor converters as these topologies will undoubtedly find a strong niche in a range of future applications.

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