

Chapter 13

Switched-Capacitor Power-Converter Topology Overview and Performance Comparison

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13.1 Introduction

In our modern society, the use of data-centric electronic devices has become ubiquitous. Due to the consumer demand of being able to use these devices anywhere, a multitude of battery-powered devices exists, including laptops, smart phones, smart watches and other so-called wearable electronic devices. Depending on the usage demands, energy storage in these devices can be implemented with a variety of different battery chemistries, where either primary (non-rechargeable) or secondary (rechargeable) batteries are used. In many cases, Li-ion batteries are used due to their superior energy density. Depending on the used battery chemistry for energy storage, the input voltage to the electronic device spans a relatively large range. At the same time, a large number of different load voltages for internal supply and for accommodating external interfaces need to be derived from the input voltage in the electronic device [1]. Bridging the gap between the input voltage range and the necessary load voltages in the electronic device can be accommodated by the power management block in Fig. 13.1 [2]. As can be seen in the figure, both voltage up and down conversion may be needed to bridge the voltage gap.

Voltage conversion in the power management block in Fig. 13.1 can be implemented in three different ways, i.e. with a continuous-time voltage regulator, an inductive or a switched-capacitor power converter (SCPC) [3]. In a continuous-time voltage regulator a dissipative pass device only allows implementing voltage down conversion from input voltage V_{in} to a lower output voltage V_{out} at a maximum efficiency of V_{out}/V_{in} . Despite their favorable Electro-Magnetic-Interference (EMI) behavior, in cases where V_{out} is much lower than V_{in} , the low efficiency may become a problem, especially at high power levels. Switched-mode circuits using

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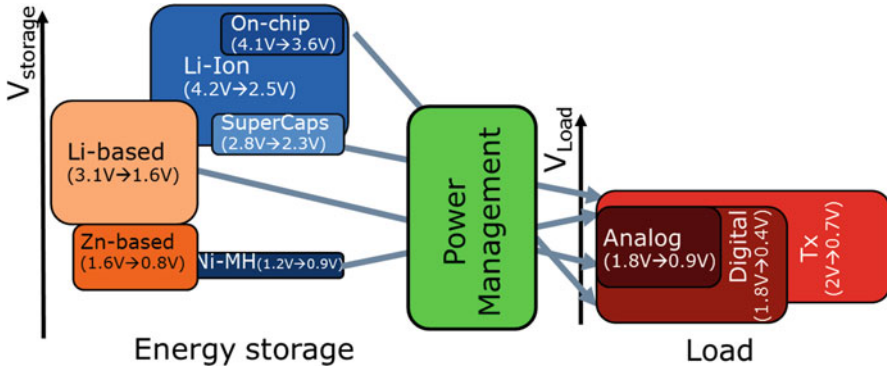


Fig. 13.1 Mismatch between energy storage voltage and load voltage [2]

reactive component(s) for temporal energy storage can implement both up and down DC/DC conversion at higher efficiency. If the primary reactive energy-storage component is an inductor, an inductive DC/DC converter can be implemented with two power switches and an inductor. Depending on how the switches and inductor are connected, either a down, an up, or an inverting up-down DC/DC converter can be constructed [4]. The ratio between input and output voltage is controlled by the duty cycle at which the power switches are operated. If the primary reactive energy-storage component is a capacitor, an SCPC can be implemented with a set of power switches and one or more so-called floating capacitors. As this paper will discuss in detail, the topology in which these switches and capacitor(s) are connected determines the ratio between input and output voltage. The output impedance of the converter is controlled to maintain a fixed output voltage when output current and/or input voltage vary.

Besides maximizing the run time of the battery-powered electronic devices by increasing the energy density of batteries and increasing the efficiency of voltage conversion, reducing the power consumption of the load is also important. For digital loads, increasing the power efficiency while maintaining the performance has led to the introduction of fine-grained power-management schemes, such as scaling the digital supply voltage with the activity of the connected block [5]. This need for local supply-voltage generation has sparked the development of DC/DC converters that are integrated with the load [1, 3].

Various methods exist to integrate the inductor with an inductive DC/DC converter [1, 3]. First, the inductor can be integrated on the same die as the converter power switches, converter control block and load, either as an air-core inductor [6, 7], or as post-processed thin-film inductor with magnetic core, e.g. based on CoZrTa alloys [8]. Alternatively, the inductor can be integrated elsewhere in the package, e.g. using bondwires [9] or package-trace air-core inductors [10], or realizing the inductor on a separate passive-integration die co-packaged with the active CMOS die [11]. In all cases, integrated inductive converters are used for relatively high output powers above 100 mW [3], because the efficiency performance of

integrated inductive DC/DC converters decreases when realized for lower output power in smaller areas, in contrast to that of their integrated capacitive counterparts [12]. This makes SCPCs an attractive candidate for monolithic integration in the power range below 100 mW, but even when external SMD capacitors are used to realize higher output powers, competitive power densities compared to inductive DC/DC converters with external inductor can be shown [13].

Several monolithic capacitor integration possibilities exist for SCPCs, such as using the gate capacitance of MOSTs (MOSCAPs), using inter-metal capacitance in fringe capacitors (usually placed on top of MOSCAPs), or, when available, using Metal-Insulator-Metal (MIM) capacitors [1, 3]. Higher power densities can be obtained when non-standard capacitor realizations such as trench capacitors are used [14]. Besides purely inductive or switched-capacitor DC/DC converters, intermediate solutions are also appearing. On the one hand, floating capacitors are added to integrated inductive converters to create multiple voltage levels at the switching node [15, 16]. This reduces the ripple current in the inductor and the blocking voltage in the switches and therefore increases efficiency. On the other hand, inductors are added to integrated capacitive converters to reduce losses associated with (dis)charging the capacitors [17].

This paper deals with the fundamental aspect in SCPCs of how to realize the needed voltage conversion ratios in different ways, and how the resulting different topologies compare in performance. Section 13.2 gives a basic theoretical background on switched-capacitor power conversion. Sections 13.3 and 13.4 describe two-clock-phase and multi-clock-phase topology examples and how to synthesize these. A performance comparison of the various topologies in Sects. 13.3 and 13.4 is made in Sect. 13.5. Finally, conclusions are drawn in Sect. 13.6.

13.2 Theoretical Considerations for Switched-Capacitor Power Converters

The basic model of an SCPC is shown in Fig. 13.2a [3]. An ideal DC transformer multiplies the input voltage V_{in} with voltage conversion ratio M . As will be described in more detail in Sects. 13.3 and 13.4, this ratio M depends on the used circuit topology, i.e. how the capacitors are connected during the different clock phases of the converter. The average equivalent output impedance of the converter is modelled by R_{out} . As shown in Fig. 13.2b, R_{out} shows asymptotic behavior for both low and high values of switching frequency, f_s [18]. For low values of f_s , the asymptote is the Slow-Switching Limit (SSL), whereas for high f_s values the Fast-Switching Limit (FSL) defines the asymptote. In the SSL, the currents flowing into capacitors are impulsive and reach zero at the end of each clock phase, and R_{out} depends on f_s and the used floating capacitance. In the FSL, the voltage across the capacitors does not change during the conductance phase and R_{out} depends on the resistance in the charge and discharge path of the floating capacitors, i.e. mostly the on-resistance of

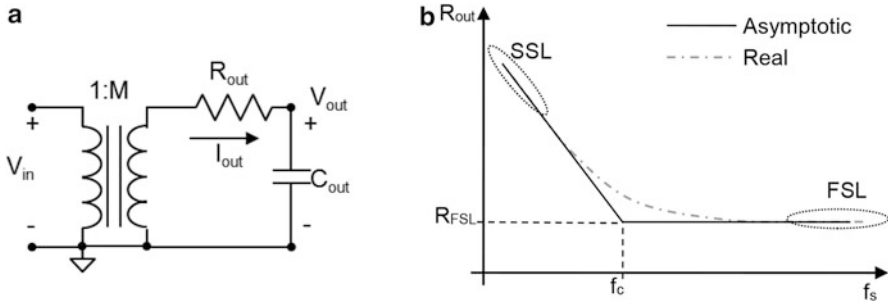


Fig. 13.2 (a) Averaged model of an SCPC, (b) equivalent output impedance R_{out} as function of switching frequency f_s

the power switches. The asymptotes cross at corner frequency, f_c . The overall curve for R_{out} can now be approximated by:

$$R_{out} = \sqrt{R_{FSL}^2 + R_{SSL}^2} \quad (13.1)$$

As can be seen from Fig. 13.2a, the maximum possible efficiency of an SCPC equals V_{out}/MV_{in} . However, since the averaged model does not consider the switching nature of the converter, in reality the achieved efficiency will be lower due to the occurrence of switching losses. These losses are caused by charging and discharging the parasitic capacitances associated with the plates of each floating capacitor in the converter, also known as bottom-plate losses, and by driver losses from turning the power switches on and off. Besides switching losses, conduction losses occur with a value of $(MV_{in} - V_{out})I_{out}$, as can be inferred from Fig. 13.2a.

In order to maintain a relatively high efficiency in cases where either V_{in} or V_{out} or both, have a large range, multiple values of M need to be used. In a multi-ratio SCPC, these multiple values of M can be generated using a single circuit [3]. A recent example of using eight values of M to maintain an efficiency above 90% across the full range of a Li-ion battery as input source is given in [13]. Another important aspect in the design of any switched-mode power converter is the output voltage ripple. As with inductive DC/DC converters, interleaving can be applied in SCPCs as well to reduce output voltage ripple [3, 19]. This can be achieved by splitting up a large converter that delivers charge packets Q to the output at time instants $T_s = 1/f_s$ apart, in N identical parallel converters or modules, each delivering a charge packet Q/N to the output consecutively at time instants T_s/N apart. For integrated converters, splitting up a converter in parallel modules is not an issue. Scaling a converter for higher or lower output power then entails placing more or fewer of these modules in parallel. Finally, the control of output voltage V_{out} involves selecting the correct value of M (in case a multi-ratio converter is used), which usually is implemented open-loop using a look-up table, and modulating the value of R_{out} in a closed control loop [3]. Modulation of R_{out} is mostly done by

Table 13.1 All possible values of M in relation to number of floating capacitors

| # floating capacitors | Possible conversion ratios M |
|-----------------------|--|
| 1 | $\frac{1}{2}; 1; 2$ |
| 2 | $\frac{1}{3}, \frac{1}{2}, \frac{2}{3}; 1; \frac{3}{2}; 2; 3$ |
| 3 | $\frac{1}{5}, \frac{1}{4}, \frac{1}{3}, \frac{2}{5}, \frac{1}{2}, \frac{3}{5}, \frac{2}{3}, \frac{3}{4}, \frac{4}{5}; 1; \frac{5}{4}, \frac{4}{3}, \frac{3}{2}, \frac{5}{3}; 2; \frac{5}{2}; 3; 4; 5$ |
| 4 | $\frac{1}{8}, \frac{1}{7}, \frac{1}{6}, \frac{1}{5}, \frac{1}{4}, \frac{2}{7}, \frac{1}{3}, \frac{3}{8}, \frac{2}{5}, \frac{3}{7}, \frac{1}{2}, \frac{4}{7}, \frac{3}{5}, \frac{5}{8}, \frac{2}{3}, \frac{5}{7}, \frac{3}{4}, \frac{5}{6}, \frac{6}{7}, \frac{7}{8}, 1$ $\frac{8}{7}, \frac{7}{6}, \frac{6}{5}, \frac{5}{4}, \frac{4}{3}, \frac{7}{5}, \frac{3}{2}, \frac{8}{5}, \frac{5}{3}, \frac{7}{4}, 2; \frac{7}{3}, \frac{5}{2}, \frac{8}{3}; 3; \frac{7}{2}; 4; 5; 6; 7; 8$ |

varying f_s (in the SSL), but can also be achieved by varying the floating capacitance (in the SSL) or modulating the on-resistance or the duty cycle of the power switches (in the FSL).

For a given number of floating capacitors, all possible values of M that can be realized using these capacitors can be calculated based on the Fibonacci number series [3, 20]. This is illustrated in Table 13.1 [3].

Though Table 13.1 shows which values of M can be realized, the systematic synthesis of each of these values has not been addressed so far. In many cases, the ratios given in Table 13.1 can be realized in multiple ways, leading to different performance tradeoffs. This paper describes the different ways that exist to realize a desired value of M , using either two clock phases (Sect. 13.3) or more than two clock phases (Sect. 13.4), and their performances are compared in Sect. 13.5.

13.3 Two-Clock-Phase Topologies

In two-clock-phase SCPCs, the floating capacitors are charged and discharged in two consecutive clock phases, both clock phases fitting within one switching period, T_s . In steady state, the charging and discharging in the two clock phases are balanced. Section 13.3.1 gives an overview of the historically used two-clock-phase topologies, while Sect. 13.3.2 describes a synthesis method for two-clock-phase SCPC topologies.

13.3.1 Overview of Known Topologies

As described in Sect. 13.1, SCPCs can accommodate both voltage up and down conversion. In fact, a converter designed for a voltage conversion ratio M can also be used for the voltage conversion ratio $1/M$ by swapping input and output connections. As Table 13.1 shows, for each M that is realizable with a given number of floating capacitors, there is a corresponding $1/M$ value. Therefore, only voltage

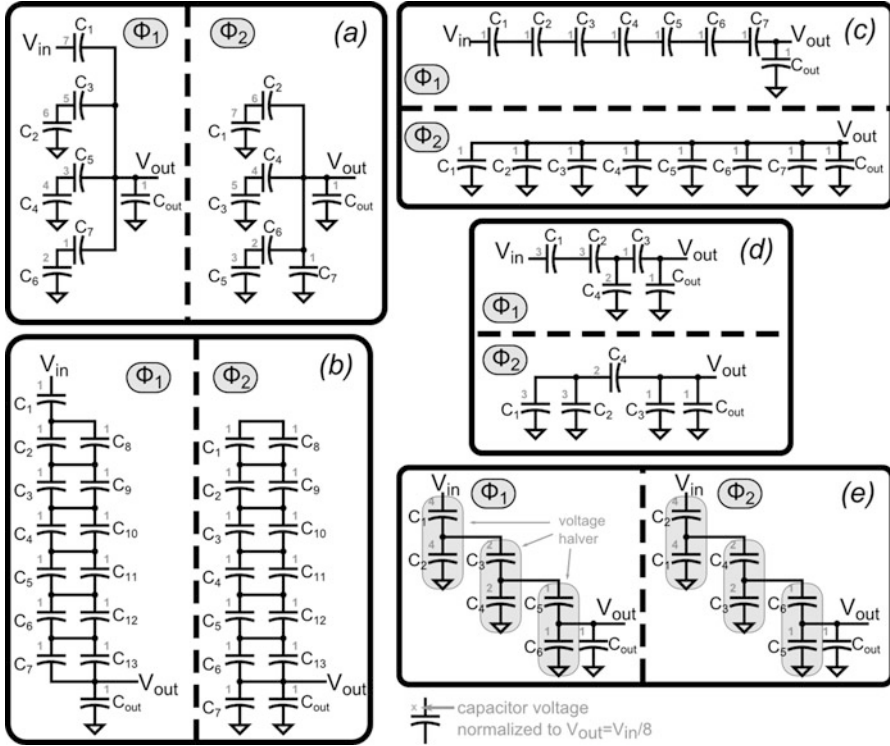


Fig. 13.3 Most well-known SCPC topologies for $M = 1/8$: (a) Dickson, (b) ladder, (c) series-parallel, (d) fractional-1, (e) recursive [24]

down conversion is considered in this section, but the five basic topologies shown also hold for up conversion [21, 22]. The five most well-known switched-capacitor power conversion topologies for $M = 1/8$ are shown in Fig. 13.3. For each topology, the circuit constellations in the two clock phases ϕ_1 and ϕ_2 are depicted, without showing the switch topology necessary to achieve these two states in a single circuit. The floating capacitors necessary to achieve these two states in a single circuit. The floating capacitors are denoted by C_i and the DC voltage across them is indicated as normalized to V_{out} , whereas the output buffer capacitor is C_{out} with voltage $V_{out} = V_{in}/8$ across it.

The Dickson topology is shown in Fig. 13.3a. This topology was inspired by the Greinacher or Cockroft-Walton topology, which effectively implements an AC/DC voltage conversion and therefore is not considered here. The Dickson topology is primarily applied in voltage up converters, since one of the switches in the charging path of each floating capacitor can be replaced with a diode, which simplifies converter control. To accommodate a voltage conversion ratio of M or $1/M$, $M - 1$ floating capacitors are needed, leading to seven floating capacitors in Fig. 13.3a. The ladder topology consists of two chains of series-connected floating capacitors that slide up and down along each other, which sets it apart from the other four

topologies, since within each string the floating capacitors remain connected in the same order in both clock phases. To accommodate a voltage conversion ratio of M or $1/M$, $2M - 3$ floating capacitors are needed, corresponding to thirteen floating capacitors in Fig. 13.3b. This inefficient use of the available capacitance makes the ladder topology less practical, but since all intermediate voltages are available at the ladder taps, it can be used as auxiliary converter to realize the needed drive voltages in a main SCPC [23].

The series-parallel topology shown in Fig. 13.3c uses $M - 1$ floating capacitors to achieve a voltage ratio of M or $1/M$. In contrast to the Dickson topology, each floating capacitor has the same DC voltage across it in steady state. Figure 13.3d shows one example of a fractional topology using the minimum possible number of capacitors to realize $M = 1/8$ according to Table 13.1, i.e., four floating capacitors. Due to this most efficient use of capacitance compared to the other four topologies, many examples of fractional SCPCs can be found in the literature. However, though Table 13.1 shows what ratios are possible, in practice a fractional topology to realize a desired value of M is usually derived by trial and error.

A larger number of capacitors compared to the fractional topology of Fig. 13.3d can be used to achieve equally spaced voltage conversion ratios using a modular approach [24], as shown in Fig. 13.3e. With the smart reconfiguration of multiple replicas of the same 2:1 unit cell ($M = 1/2$) consisting of two floating capacitors, $2^N - 1$ voltage ratios can be achieved using N unit cells, so $2N$ floating capacitors. Though less voltage ratios are possible for a given number of floating capacitors compared to Table 13.1, the recursive approach of placing the same unit cell in series or parallel makes this topology easily reconfigurable. This can be an advantage compared to the fractional topology, especially when a multi-ratio converter is needed to maintain efficiency over a wider input or output voltage range.

13.3.2 Topology Synthesis

To break away from the trial and error aspect for the topology synthesis in Fig. 13.3d, a generic iterative algorithm for synthesizing SCPC topologies was developed [25]. A short summary of the method is given in this section. Figure 13.4 shows a conceptual block diagram of a two-clock-phase SCPC consisting of n_c floating capacitors with three external terminals.

Fig. 13.4 Conceptual SCPC with n_c floating capacitors

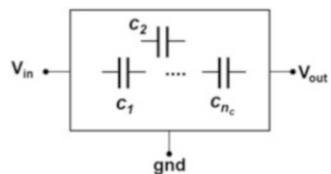


Table 13.2 Valid configuration pairs for $n_c = 2, 3$ and 4 (redundant pairs omitted)

| Description | Config. identifier | Configuration pairs | $q_{\phi 1}, q_{\phi 2}$ | q_{sum} |
|-------------|--------------------|---|--------------------------|-----------|
| $n_c = 2$ | 2 | $[\mathbf{c}_1 \oplus \mathbf{c}_2] \& [\mathbf{c}_1 \mathbf{c}_2]$ | 1,2 | 3 |
| $n_c = 3$ | 3.1 | $[(\mathbf{c}_1 \oplus \mathbf{c}_2) \oplus \mathbf{c}_3] \& [(\mathbf{c}_1 \mathbf{c}_2) \mathbf{c}_3]$ | 1,2+1 | 4 |
| | 3.2 | $[(\mathbf{c}_1 \oplus \mathbf{c}_2) \mathbf{c}_3] \& [(\mathbf{c}_1 \mathbf{c}_2) \oplus \mathbf{c}_3]$ | 1+2,2 | 5 |
| | 3.3 | $[(\mathbf{c}_1 \oplus \mathbf{c}_2) \mathbf{c}_3] \& [\mathbf{c}_1 (\mathbf{c}_2 \oplus \mathbf{c}_3)]$ | 1+1,1+1 | 4 |
| $n_c = 4$ | 4.1 | $[\mathbf{c}_1 \oplus \mathbf{c}_2 \oplus \mathbf{c}_3 \oplus \mathbf{c}_4] \& [\mathbf{c}_1 \mathbf{c}_2 \mathbf{c}_3 \mathbf{c}_4]$ | 1,3+1 | 5 |
| | 4.2 | $[(\mathbf{c}_1 \oplus \mathbf{c}_2 \oplus \mathbf{c}_3) \mathbf{c}_4] \& [(\mathbf{c}_1 \mathbf{c}_2 \mathbf{c}_3) \oplus \mathbf{c}_4]$ | 1+3,3 | 7 |
| | 4.3 | $[(\mathbf{c}_1 \oplus \mathbf{c}_2 \oplus \mathbf{c}_3) \mathbf{c}_4] \& [\mathbf{c}_1 \mathbf{c}_2 (\mathbf{c}_3 \oplus \mathbf{c}_4)]$ | 1+1,2+1 | 5 |
| | 4.4 | $[((\mathbf{c}_1 \oplus \mathbf{c}_2) \mathbf{c}_3) \oplus \mathbf{c}_4] \& [((\mathbf{c}_1 \mathbf{c}_2) \oplus \mathbf{c}_3) \mathbf{c}_4]$ | 3,2+3 | 8 |
| | 4.5 | $[(\mathbf{c}_1 \oplus \mathbf{c}_2) (\mathbf{c}_3 \oplus \mathbf{c}_4)] \& [((\mathbf{c}_1 \mathbf{c}_2) \oplus \mathbf{c}_3) \mathbf{c}_4]$ | 2,2+1 | 5 |
| | 4.6 | $[(\mathbf{c}_1 \oplus \mathbf{c}_2 \oplus \mathbf{c}_4) \mathbf{c}_3] \& [((\mathbf{c}_1 \mathbf{c}_2) \oplus \mathbf{c}_3) \mathbf{c}_4]$ | 3,2+1 | 6 |
| | 4.7 | $[(\mathbf{c}_1 \oplus \mathbf{c}_2) \mathbf{c}_3 \mathbf{c}_4] \& [(\mathbf{c}_1 \mathbf{c}_2) \oplus \mathbf{c}_3 \oplus \mathbf{c}_4]$ | 3+2,2 | 7 |
| | 4.8 | $[((\mathbf{c}_1 \oplus \mathbf{c}_2) \mathbf{c}_3) \oplus \mathbf{c}_4] \& [\mathbf{c}_1 (\mathbf{c}_2 \oplus \mathbf{c}_3) \mathbf{c}_4]$ | 2,2+2 | 6 |
| | 4.9 | $[(\mathbf{c}_1, \mathbf{c}_2) (\mathbf{c}_3, \mathbf{c}_4)] \& [\mathbf{c}_1 (\mathbf{c}_2, \mathbf{c}_3) \mathbf{c}_4]$ | 2,2+1 | 5 |
| | 4.10 | $[((\mathbf{c}_1, \mathbf{c}_2) \mathbf{c}_3) \mathbf{c}_4] \& [\mathbf{c}_1 (\mathbf{c}_2, \mathbf{c}_3, \mathbf{c}_4)]$ | 1+1,2+1 | 5 |
| | 4.11 | $[((\mathbf{c}_1, \mathbf{c}_2) \mathbf{c}_3) \mathbf{c}_4] \& [(\mathbf{c}_1, \mathbf{c}_4) (\mathbf{c}_2, \mathbf{c}_3)]$ | 2+2,2 | 6 |

$c_i \oplus c_j$ implies the same charge flows through c_i and c_j , $c_i | c_j$ implies charge is shared between c_i and c_j

The Fibonacci limit for the achievable conversion gains of SCPCs was introduced in Table 13.1. According to this limit, with n_c floating capacitors all conversion ratios given by Eq. (13.2) can be realized:

$$M(n_c) = \frac{V_{out}}{V_{in}} = \frac{1 \leq P \leq F_{n_c+1}}{1 \leq Q \leq F_{n_c+1}} \quad (13.2)$$

where P and Q are integers and F_n is the n_c th Fibonacci number. The synthesis algorithm for a target conversion ratio, $M = P/Q$, is divided into two steps:

- I) *Iterative generation of configuration pairs*: In this step, all valid configuration pairs (without considering connections to the external terminals) with the required number of floating capacitors, as given by the Fibonacci limit of Eq. (13.2), are generated through iteration. For each configuration pair, n_c floating capacitor voltages and the output voltage V_{out} need to be resolved, so valid configuration pairs are the ones that yield $n_c + 1$ valid KVL (Kirchoff Voltage Law) equations while maintaining charge balance for each floating capacitor. These valid configuration pairs are depicted in Table 13.2, where c_i denote the floating capacitors, and $q_{\phi 1}$ and $q_{\phi 2}$ are the effective charge coefficients during the two clock phases, and $q_{sum} = q_{\phi 1} + q_{\phi 2}$. A configuration pair describes charge flow through the floating capacitors and corresponds to the set of KVL equations for each clock phase.
- II) *Terminal assignment*: A converter with a desired voltage conversion ratio, $M = V_{out}/V_{in} = P/Q$ has charge conversion ratio $q_{out}/q_{in} = 1/M = Q/P$. After normalization, $q_{out} = Q$ and $q_{in} = P$. With terminal assignment, the three exter-

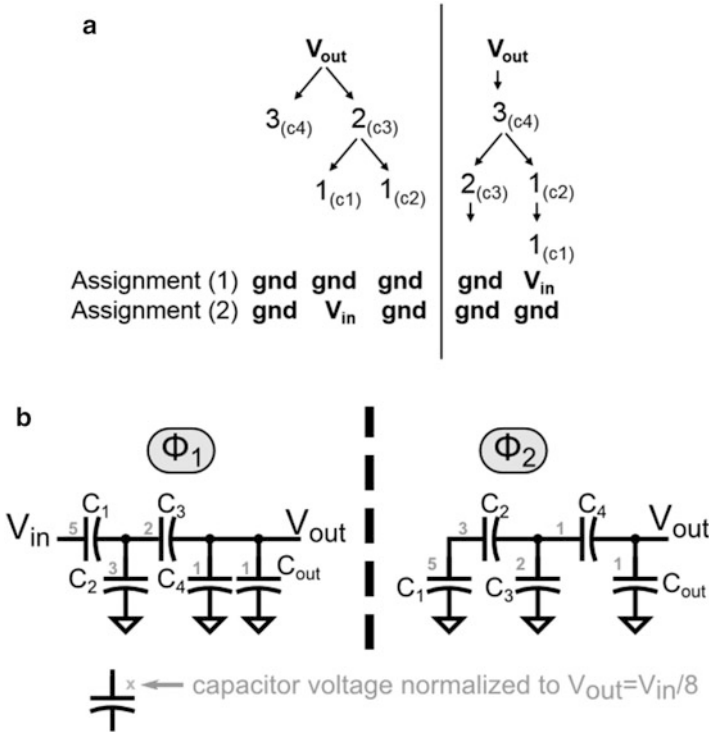


Fig. 13.5 (a) Charge flow diagram for configuration pair (4.4) in Table 13.2, (b) synthesized alternative fractional-2 SCPC topology to realize $M = 1/8$

nal terminals are connected to the configuration pairs with $q_{sum} \geq \max(P, Q)$ such that the charge conversion ratio is satisfied over the two phases Φ_1 and Φ_2 .

A more detailed example of applying the two synthesis steps is given in [25]. To further illustrate the application of this algorithm, consider $M = 1/8$, which implies $P = 1$, and $Q = 8$. Following the steps of the algorithm:

- 1) $n_c = 4$ from the Fibonacci limit on the possible conversion ratios, see Table 13.1.
- 2) Table 13.2 gives all possible configuration pairs for $n_c = 4$. The exact explanation of this table can be found in [25].
- 3) Out of 11 possible configuration pairs, only the configuration pair (4.4) satisfies $q_{sum} \geq \max(P, Q)$, since it has a value $q_{sum} = 8$. Its charge flow diagram is shown in Fig. 13.5a. The terminal assignment with $P = 1$ and $Q = 8$ can be done in two different ways resulting in two different topologies with the same M . Figure 13.3d shows the results of polarity assignment to the capacitors corresponding to assignment (1) and Fig. 13.5b shows it for assignment (2).

It should be noted that the floating capacitors of the two topologies with $M = 1/8$ have identical charge coefficients as defined in [18], hence the same SSL and FSL

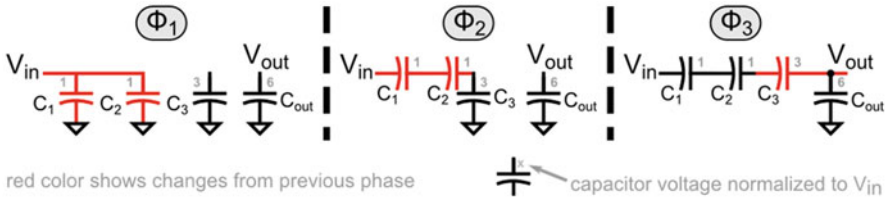


Fig. 13.6 SCPC topology using three clock phases for $M = 6$ [26]

impedances. However, they differ in the capacitor and switch blocking voltages, hence one topology can be better suited over the other in a given application. This point will be developed further in Sect. 13.5.

13.4 Multi-Clock-Phase Topologies

The Fibonacci constraint on the minimum required number of floating capacitors can be extended by employing additional clock phases within each switching period T_s . In these multi-clock-phase topologies, the charge balance of the capacitors can occur over more than two clock phases. Two recent examples of multi-clock-phase SCPCs are given in Sect. 13.4.1, while Sect. 13.4.2 shows examples of alternative synthesized multi-clock-phase topologies.

13.4.1 Overview of Known Topologies

An example of a topology using three clock phases achieving a voltage up-conversion ratio $M = 6$ using three floating capacitors is shown in Fig. 13.6 [26]. By exploiting an additional clock phases, this topology uses one less floating capacitor to realize $M = 6$. The operation of the converter is as follows:

- Φ_1 : C_1 and C_2 are charged to V_{in} while C_3 is unconnected: normalized charge coefficients $q_{c1} = 2$, $q_{c2} = 2$, $q_{c3} = 0$.
- Φ_2 : C_1 and C_2 are placed in series with V_{in} and C_3 is charged to $3V_{in}$: charge coefficients $q_{c1} = -1$, $q_{c2} = -1$, $q_{c3} = 1$.
- Φ_3 : C_1 , C_2 and C_3 are in series with V_{in} to charge C_{out} to $6V_{in}$: charge coefficients $q_{c1} = -1$, $q_{c2} = -1$, $q_{c3} = -1$.

The charge coefficients in the three clock phases reveal an important difference between multi-clock-phase and two-clock-phase topologies: in multi-clock-phase topologies, the amount of (dis)charge supplied to a floating capacitor does not need to be the same during each clock phase unlike the two-clock-phase topologies. The charge balancing of the floating capacitors occurs over more than two clock

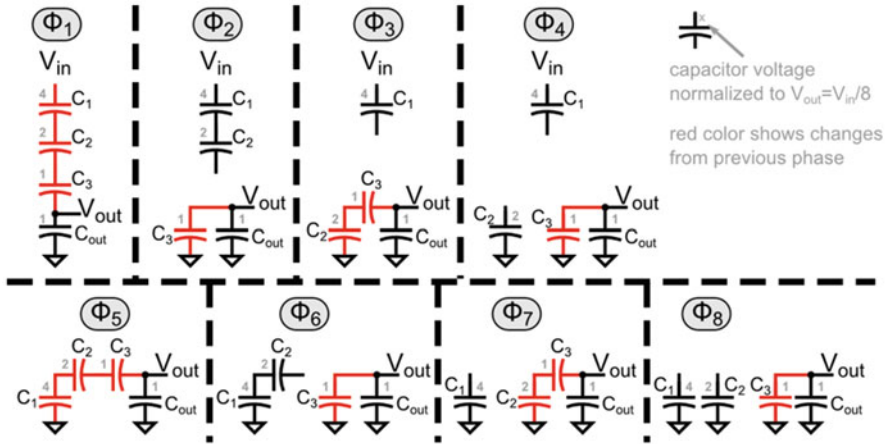


Fig. 13.7 Binary eight-clock-phase topology providing $M = 1/8$ [27]

phases, with some capacitors potentially being inactive during certain phase(s). This feature will result in different output impedance characteristics for a multi-clock-phase topology compared to a two-clock-phase topology. In the realization of the switched-capacitor up converter using this topology, the capacitance values of C_2 and C_3 were increased to enable the reduction of the capacitance of C_1 and hence its full integration, leaving only two SMD floating capacitors. Therefore, the potential of this multi-clock-phase topology to realize the desired M with a lower number of capacitors than prescribed by Table 13.1 was fully exploited to yield a high-efficiency, low-volume DC/DC converter.

Another approach to realizing multi-clock-phase converters is based on binary topologies [27]. The binary topologies employ 2^{n_c} clock phases with n_c floating capacitors to provide the binary conversion ratios given by:

$$M = \frac{1 \leq P \leq 2^{n_c} - 1}{2^{n_c}} \tag{13.3}$$

Figure 13.7 shows an example with $M = 1/2^3 = 1/8$ that uses three floating capacitors with eight clock phases. A unit charge is supplied to V_{out} during each clock phase, resulting in a total of eight units of charge over a complete switching period. Therefore, the charge coefficient of each floating capacitor, when it is used, is always $1/8$, the minimum possible. This minimum charge coefficient will result in the lowest SSL impedance as will be discussed in Sect. 13.5 (given the same total amount of floating capacitance and the same switching frequency). In [27], this topology has been implemented using a cascade of N 2:1 unit cells ($M = 1/2$) operating in successively doubling frequencies, which is the same as having a single switching frequency with 2^N clock phases. This approach has the advantage of modularity, similar to the two-clock-phase variant in Fig. 13.3e.

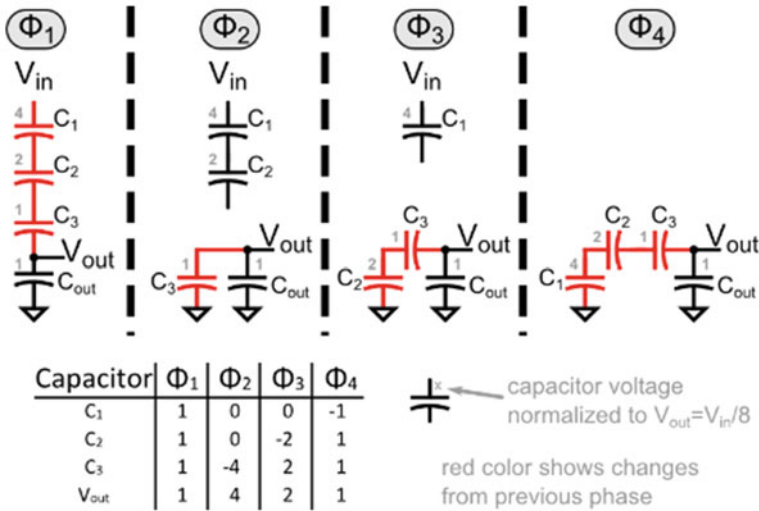


Fig. 13.8 Alternative $M = 1/8$ topology with four clock phases, including charging behaviour

Two observations can be made about this topology: (1) from the charge-flow point of view, the configurations in the phases Φ_2 , Φ_4 , Φ_6 , and Φ_8 are identical to each other, just as the configurations in phases Φ_3 , and Φ_7 are identical to each other, (2) each configuration has only one KVL loop. This means that there are actually only four unique configurations in this topology. This is consistent with the requirement of four linearly independent loops to uniquely resolve the voltages across the capacitors and the output voltage V_{out} [25].

13.4.2 Topology Synthesis

By combining the configurations with identical charge flow in Fig. 13.7 in a single phase, a multi-clock-phase fractional topology using four clock phases instead of eight clock phases can be made as shown in Fig. 13.8. The (dis)charging behavior of this topology is depicted in the table shown in the inset, normalized to $q_{in} = q_{out}/8$.

By manipulating the table in Fig. 13.8, other multi-clock-phase topologies can be generated. As an example, consider a target conversion ratio of $M = 1/7$. This converter delivers a normalized total charge of $7q_{in}$ to V_{out} over one switching period. To achieve this, the last two rows of the table in Fig. 13.8 can be adapted, resulting in the (dis)charging behavior of the table in Fig. 13.9. The (dis)charging of the floating capacitors has also been changed to maintain charge balance. The resulting topology is shown in Fig. 13.9 resulting in a four-clock-phase topology with $M = 1/7$. In general, with n_c floating capacitors, topologies with a conversion

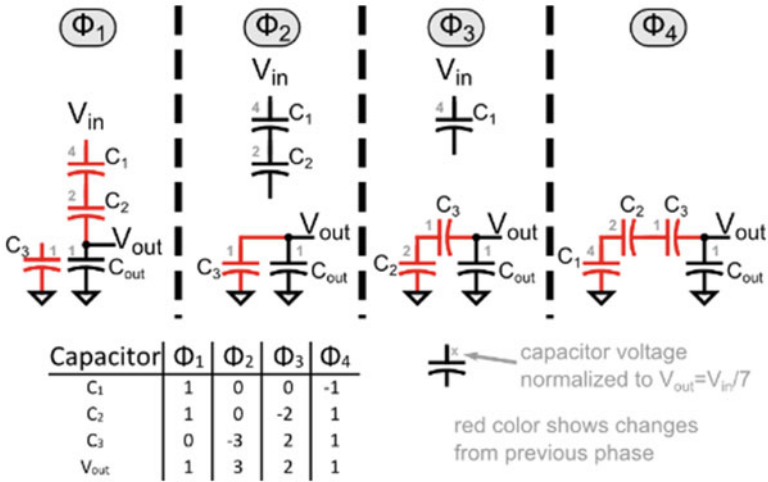


Fig. 13.9 Four-clock-phase topology to generate $M = 1/7$ including charging behavior

ratio given by:

$$M = \frac{1 \leq P \leq 2^{n_c}}{1 \leq Q \leq 2^{n_c}} \tag{13.4}$$

can be realized using a maximum of $n_c + 1$ clock phases (discounting repetition of configurations with identical charge flow, as in the case of binary multi-clock-phase topologies).

13.5 Topology Performance Comparison

13.5.1 Comparison Between Alternative Two-Clock-Phase Topologies

As described in previous sections, there are many different topologies that can provide the same conversion ratio M . However, they might present different advantages or disadvantages that makes them more or less suitable for different applications. From the functionality point of view of an SCPC, the most important parameter besides M , is the amount of output impedance R_{out} (see Fig. 13.2). In the SSL region, the output impedance R_{SSL} can be computed as follows:

$$R_{SSL} = \frac{m}{f_s C_T} \tag{13.5}$$

where f_s is the switching frequency, C_T is the total amount of floating capacitance and m is a topology-dependent parameter that is determined by circuit analysis [18].

In the FSL region, the output impedance R_{FSL} only depends on the on-resistance of the switches (neglecting the interconnect parasitic resistances) and the topology, and can be expressed as follows:

$$R_{FSL} = p \frac{k_{sw}}{A_{swT}} \quad (13.6)$$

where p is a topology-dependent parameter obtained by circuit analysis [18], A_{swT} is the total area of the switches in [mm²], and k_{sw} is a technology-related parameter that states the on-resistance of the switches per unit of silicon area (assuming the same voltage rating for all the devices), in [$\Omega \cdot \text{mm}^2$]. Therefore, the inverse ratio A_{swT}/k_{sw} describes the amount of conductance that is used by the design.

Table 13.3 shows the values of the p and m parameters for a number of different topologies that provide the same conversion ratio ($M = 1/8$) with a different number of floating capacitors n_c . As shown, all the different two-clock-phase topologies (A–E) have the same m and p values, which means that actually all the considered topologies will present the same output impedance provided that they operate at the same switching frequency, use the same amount of total floating capacitance and the same total amount of area for the switches.

Topologies F and G in Table 13.3 represent the two different multi-clock-phase topologies that were introduced in Sect. 13.4, also providing $M = 1/8$. However, because of their multi-clock-phase nature, conclusions from the comparison with the two-clock-phase topologies cannot be derived directly. This will be commented in Sect. 13.5.2, along with the content of the last two columns.

In more detail, the parameters shown in Table 13.3 can be described as follows:

- $n_c \rightarrow$ the number of required floating capacitors.
- $n_{sw} \rightarrow$ the number of power switches.
- $m \rightarrow$ product of R_{SSL} , the switching frequency and the total amount of floating capacitance (given the optimum relative sizing of all the floating capacitors), see Eq. (13.5).
- $p \rightarrow$ ratio between R_{FSL} and the amount of conductance, given the optimum relative sizing of all the power switches, see Eq. (13.6).
- $l \rightarrow$ this parameter can be used as an indication of the bottom-plate power losses that a topology suffers from. If all the energy spent to charge and discharge the parasitic bottom-plate capacitors is considered lost (pessimistic approach), the l parameter is calculated as:

$$l = \sum_{i=1}^{n_c} C_{Ri} V_{Ri}^2 \quad (13.7)$$

Table 13.3 Performance parameter comparison of various $M = 1/8$ topologies

| Topology ($M = 1/8$) | n_c | n_{sv} | m | p | l | $\sum_{i=1}^{n_c} g_i V_{off}^2$ | $\sum_{i=1}^{n_c} V_{Ci} q_{Ci}$ | V_{Ci} (norm. to V_{out}) | | | | | | | q_{Ci} (norm. to $q_{out}/8$) | | | | | | | mI | $\sum_{i=1}^{sw_events} g_i V_{off}^2$ | | | | | | | | |
|------------------------|-------|----------|-------|-------|-------|----------------------------------|----------------------------------|--------------------------------|-------|-------|-------|-------|-------|-------|----------------------------------|----------------|----------------|-------|-------|-------|-------|-------|---|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | | | | | | C_1 | C_2 | C_3 | C_4 | C_5 | C_6 | C_7 | C_1 | C_2 | C_3 | C_4 | C_5 | C_6 | C_7 | C_1 | C_2 | C_3 | C_4 | C_5 | C_6 | C_7 | | | |
| A: Fig. 13.3a | 7 | 22 | 0.766 | 15.13 | 0.031 | 0.028 | 28 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.024 | 0.021 |
| B: Fig. 13.3c | 7 | 22 | 0.766 | 15.13 | 0.625 | 0.239 | 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.479 | 0.183 |
| C: Fig. 13.3e | 6 | 20 | 0.766 | 15.13 | 0.125 | 0.08 | 12 | 4 | 4 | 2 | 2 | 1 | 1 | 1 | 1/2 | 1/2 | 1 | 1 | 1 | 2 | 2 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 0.096 | 0.061 | 0.061 |
| D: Fig. 13.3d | 4 | 13 | 0.766 | 15.13 | 0.152 | 0.092 | 13 | 3 | 3 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 3 | 2 | 1 | 1 | 1 | 1 | 3 | 2 | 2 | 2 | 2 | 2 | 0.116 | 0.070 | 0.070 |
| E: Fig. 13.5b | 4 | 13 | 0.766 | 15.13 | 0.067 | 0.058 | 15 | 5 | 3 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 3 | 1 | 1 | 1 | 1 | 2 | 3 | 3 | 3 | 3 | 3 | 0.051 | 0.044 | 0.044 |
| F: Fig. 13.7 | 3 | 10 | 0.328 | 27.5 | 0.292 | 0.163 | 7 | 4 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.096 | 0.067 | 0.067 |
| G: Fig. 13.8 | 3 | 10 | 0.571 | 24.66 | 0.135 | 0.099 | 16 | 4 | 2 | 1 | 1 | 1 | 1 | 1 | 1 ^a | 2 ^a | 4 ^a | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.077 | 0.062 | 0.062 |

Topologies: A: Two-clock-phase Dickson, B: Two-clock-phase series-parallel, C: Two-clock-phase recursive [24], D: Two-clock-phase fractional-1, E: Two-clock-phase fractional-2, F: Eight-clock-phase binary [27], G: Four-clock-phase alternative

^aThere is difference in charge flow per phase. The shown value is the maximum one

where C_{Ri} is the value of each floating capacitor normalized to the total amount of floating capacitance C_T , and V_{Ri} is the voltage across each floating capacitor, normalized to the input voltage V_{in} . From the l parameter definition in Eq. (13.7), it becomes straightforward to compute the total amount of bottom-plate losses:

$$P_{bot} = V_{in}^2 f_s \alpha C_T l \quad (13.8)$$

where α is a technology-dependent ratio representing the average of both top-plate and bottom-plate parasitics of the floating capacitors relative to their capacitance.

- The summation of the $g \cdot V_{off}^2$ (conductance g and blocking voltage V_{off}) values of all the power switches. The blocking voltage is squared because conceptually, the on-resistance of a power switch increases with the square of its blocking voltage. This parameter provides an intuitive indication about the size of the switches, and as a result, also about the energy that needs to be spent to drive their gates.
- The summation of $V_{ci} \cdot q_{ci}$ for all the floating capacitors. This parameter becomes especially relevant in fully integrated solutions, since the relative sizes of the floating capacitors is proportional to the amount of charge flowing through them and the operating voltage across them.
- $V_{Ci} \rightarrow$ The voltage across each of the floating capacitors C_i (normalized to the output voltage $V_{out} = V_{in}/8$), as shown in Sects. 13.3 and 13.4.
- $q_{Ci} \rightarrow$ The amount of charge flowing through each of the floating capacitors C_i (normalized to the amount of input charge per switching period $q_{in} = q_{out}/8 = I_{out} \cdot T_s/8$).

Based on comparing only the p and m parameters of two-clock-phase topologies A–E, it could be concluded that all the different topologies would provide the same performance. However, looking at the rest of the table content, substantial advantages could be obtained by making a proper topology choice for a particular application-technology combination. Below, different possible scenarios will be discussed.

13.5.1.1 Scenario 1: Floating Capacitors Realized with External SMD Capacitors

For this scenario, the most interesting options would be the fractional topologies (D and E), because they require the smallest number of capacitors and pins. Since the amount of bottom-plate parasitics of SMD capacitors is normally negligible, in case of a high-voltage application, the fractional-1 topology (D) would represent a better fit since the operating voltage across the floating capacitors is smaller. On the other hand, if this becomes irrelevant, e.g. because of the relatively low voltage of the application, then the fractional-2 topology (E) would be preferred because of the lower combination of conductance and blocking voltage of the power switches, which would likely result in lower switching losses.

13.5.1.2 Scenario 2: Fully Integrated Switched-Capacitor Power Converter

In the fully-integrated scenario, the relative importance of the different parameters changes quite significantly. In the integrated domain, the number of floating capacitors is not a problem by itself, but their total size is. If the application is sufficiently low-voltage enough, so that the voltage across the capacitors does not impact their implementation towards a lower capacitance density, then a Dickson topology (A) would clearly be the best choice due to its extremely low bottom-plate losses, and low area required for the switches. On the other hand, when a particular application runs at a relatively high voltage, a series-parallel topology (B) could become interesting due to the minimization of the voltage across all the floating capacitors, despite the significantly larger amount of bottom-plate and switching losses. The fractional-2 topology (E) shows a good trade-off between blocking voltage and conductance of the required switches, as well as very low bottom-plate power losses and applied voltage across the floating capacitors. Despite not standing out in any of the main converter parameters, the recursive topology (C) provides a very interesting modular approach to implement a multi-ratio SCPC by means of smart interconnection of unit cells that implement $M = 1/2$. This implies that a single cell could be designed, replicated and smartly used to easily create a large range of conversion ratios (though not all the possible ones). Unfortunately, in cases where extremely high or low ratios are needed, the number of needed unit cells and therefore floating capacitors would make a design based on external components (scenario 1) unpractical.

It is important to take into account that all parameter values shown in Table 13.3 are merely indicative of a trend, and would only apply to cases where the voltage rating of devices (both floating capacitors and power switches) could be gradually adjusted in a continuous way. Unfortunately, most technology processes provide devices with very specific voltage ratings that change in discrete steps. This clearly precludes the existence of an absolute optimum choice for every different application-technology combination.

13.5.2 Comparison Between Two-Clock-Phase and Multi-Clock-Phase Topologies

In this section, the more conventional two-clock-phase topologies will be compared to multi-clock-phase topologies, in terms of the achievable gains and performance considering similar parameters to the ones used in Sect. 13.5.1.

Although parameters related to output impedance (p and m) and the possible conversion ratios are common to all the two-clock-phase topologies (besides the ladder topology of Fig. 13.3b), this is not the case with topologies operating with multiple clock phases. As a result, the two-clock-phase topologies will be compared to the approach presented in [27] (as illustrated by the binary multi-clock-phase

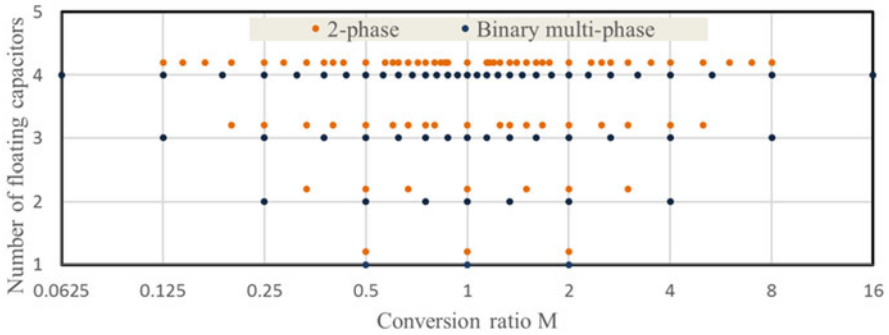


Fig. 13.10 Comparison between achievable voltage conversion ratios M for fractional two-clock-phase and binary multi-clock-phase topologies

topology F, Fig. 13.7), since this is the finest example of a multi-ratio multi-clock-phase topology that the authors are aware of. This particular approach allows for a systematic way to synthesize a different number of binary-scaled conversion ratios that operate in multi-clock-phase, with a small number of floating capacitors. As introduced in Sect. 13.4.1, a smart connection of voltage-halver stages is used that each operate at twice the frequency of its precedent, resulting in a particular case of multi-clock-phase design (with 2^{n_c} clock phases for n_c floating capacitors).

Figure 13.10 shows the achievable number of conversion ratios M (up/down) that can be obtained from a fractional two-clock-phase (see Table 13.1) and a binary multi-clock-phase topology, as a function of the number of floating capacitors. As expected from Sect. 13.4, multi-clock-phase topologies are able to achieve a higher maximum ratio for a given number of floating capacitors than fractional two-clock-phase ones. However, it is the density of available ratios in a particular gain range that allows multi-ratio designs to keep a high power efficiency over a certain range of input or output voltage.

As observed from Fig. 13.10, a fractional two-clock-phase design could provide more conversion ratios in a particular gain range than the binary multi-phase approach, eventually resulting in a higher average power efficiency. As an example of that, Fig. 13.11 compares the theoretical maximum power efficiency (V_{out}/MV_{in}) available from multi-ratio designs using four floating capacitors based on either a two-clock-phase or a binary multi-clock-phase topology. In this example an output voltage of 5 V has been considered for an input voltage range corresponding to Li-ion batteries (2.6–4.2 V), as in [13]. In this example, the two-clock-phase fractional topology delivers an average efficiency across the input voltage range of 96.4 %, compared to 95.4 % for the binary multi-clock-phase topology. However, the more evenly distributed ratios from the binary multi-clock-phase topology makes the ratio control easier by increasing the linearity.

Besides the conversion ratios that can be generated from a particular approach (either using two or multiple clock phases), the performance of an SCPC is also strongly determined by its output impedance and switching losses. Figure 13.12a

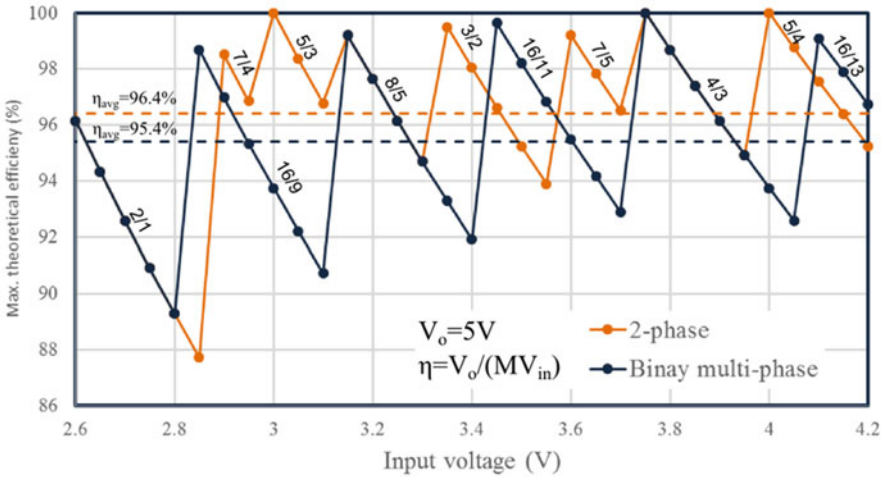


Fig. 13.11 Impact of achievable voltage conversion ratios with fractional two-clock-phase and binary multi-clock-phase topologies in practical multi-ratio converters

shows, as a function of the step-down conversion ratio M , the ratio between the switching frequency of a multi-clock-phase design (f_{mph}) and a two-clock-phase (f_{2ph}) design. Both designs provide the same R_{SSL} with the same total amount of floating capacitance C_T . It is clearly noticeable that multi-clock-phase topologies require a lower f_s to provide the same amount of impedance, although they have a higher number of switching events due to their higher number of clock phases within each switching period T_s . From Eq. (13.5), for a given value of R_{SSL} , the value of m varies with that of f_s . Therefore, the ratio of switching frequency coincides with the ratio of m values of each family of topologies.

Both binary multi-clock-phase and two-clock-phase topologies can also be compared based on their R_{FSL} value. Figure 13.12b shows the ratio of the total amount of area spent on implementing the power switches for the multi-clock-phase case (A_{mph}) and for the two-clock-phase designs (A_{2ph}), as a function of the implemented conversion ratio M . From this graph it becomes clear that the two-clock-phase topologies will require less area spent in the switches, thus making them more appealing when implementing an SCPC with external floating capacitors, especially when high output power is needed and a lower switch area leads to a lower cost [13]. Similar to the m ratio corresponding to the f_s ratio in Fig. 13.12a, the switch-area ratio in Fig. 13.12b coincides with the ratio of p values according to Eq. (13.6).

Considering that multi-clock-phase topologies require larger power switches (for the same R_{FSL}) but require lower f_s (for the same R_{SSL} and C_T) albeit with having more switching events per cycle, it is relevant to compare their expected amount of switching losses. An indication of the amount of switching losses that can be expected from either design approach could be computed as the product of the

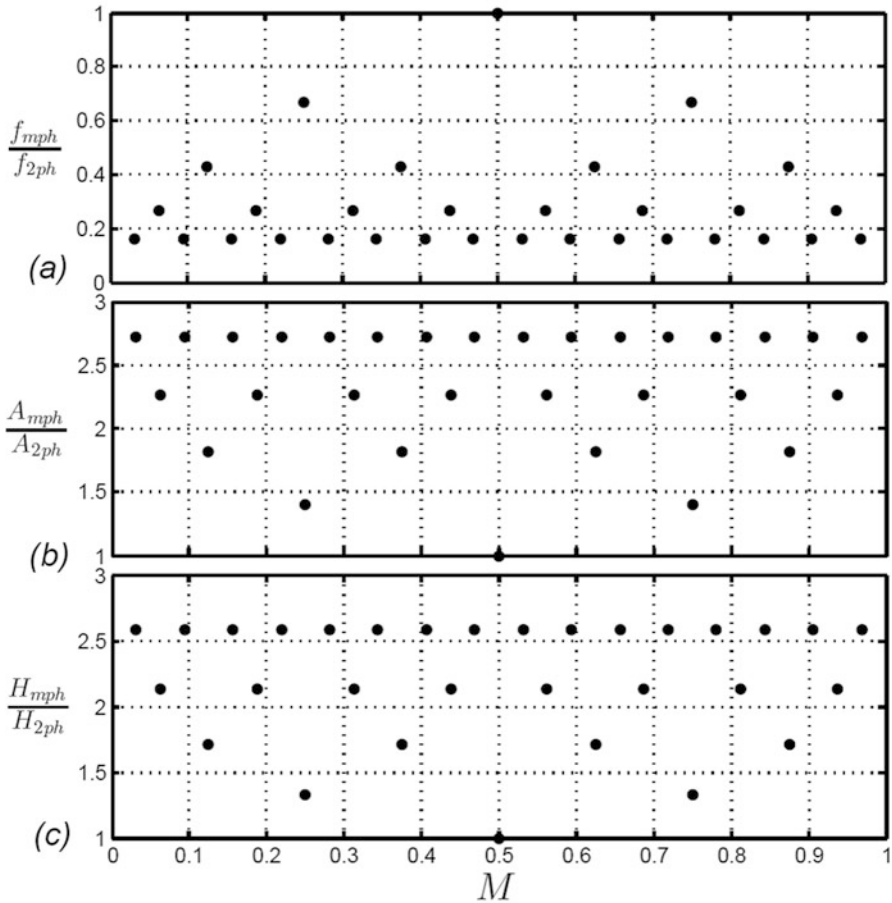


Fig. 13.12 Comparison of two-clock-phase vs. binary multi-clock-phase topologies in terms of (a) switching frequency, (b) switch area and (c) switching losses indication, as a function of the step-down conversion ratio M

switching frequency and the amount of area that is switched per cycle. In case of two-clock-phase topologies, the amount of area that switches per cycle is the same as the total amount of area spent in switches (A_{swT}). However, in multi-clock-phase designs, some switches might be turned-on/off more than once per switching period T_s , meaning that the amount of area that switches is bigger than A_{swT} by a factor $switching_events/n_{sw}$ (if all the switches are equally sized, as in the binary multi-clock-phase topology). To address this issue, the following parameter is defined as an indicative parameter of the amount of switching losses:

$$H = f_s A_{swT} \frac{switching_events}{n_{sw}} \begin{cases} 2 \text{ phases} \rightarrow switching_events = n_{sw} \\ mult.ph \rightarrow switching_events > n_{sw} \end{cases} \quad (13.9)$$

Figure 13.12c shows the ratio of this parameter for both the multi-clock-phase and two-clock-phase topology (H_{mph}/H_{2ph}), as a function of the conversion ratio M . It is observed that in general higher switching losses should be expected from multi-clock-phase designs providing the same conversion ratio and output impedance, despite the lower switching frequency. As in previous results, both approaches coincide for $M = 1/2$, for which a single floating capacitor is used and only two clock phases are possible.

Unfortunately, the amount of bottom-plate losses and the blocking voltage of the different devices could not be included in the results of Fig. 13.12b, c without loss of generality, due the wide variety of two-clock-phase topologies that could be implemented, providing the same conversion ratio. In case that not all the devices of a particular design could have the same voltage rating, this should also be taken into account when considering the different design strategies.

For completeness, the multi-clock-phase designs of Figs. 13.7 and 13.8, providing $M = 1/8$, have also been included in Table 13.3 (topologies F and G, respectively). For the particular case of $M = 1/8$, the different two-clock-phase topologies A–E can be compared to multi-clock-phase designs F and G, including the blocking voltages of the devices as well as bottom-plate losses. The relative amount of bottom-plate losses is obtained from the ml product which takes into account the difference in switching frequency. To compute the relative amount of switching losses taking into account the blocking voltage of the power switches (last column of the table), which switch is used more than once needs to be carefully considered for the multi-clock-phase topologies, as well as their relatively lower f_s (represented by the m value). From the Table 13.3, the following is observed:

- Multi-clock-phase topologies are clearly an interesting solution for designs with discrete floating capacitors, where reducing the number of components and pins is important.
- Multi-clock-phase topologies operate at lower f_s , although their bottom-plate losses are not necessarily smaller. However, when using discrete floating capacitors, this may be irrelevant.
- Multi-clock-phase designs require a larger amount of area for the switches, which is relevant for high-power designs [13, 27].
- Despite operating at lower f_s , no lower switching losses result from multi-clock-phase designs since they have more switching events per cycle.

13.6 Conclusions

Various SCPC topologies are possible to realize a desired voltage conversion ratio M . A major distinction between possible topologies is the number of clock phases that is used within a switching cycle. Within the group of two-clock-phase SCPCs, different topologies are possible that use different numbers of floating capacitors to realize a desired value of M . The fractional topology uses the minimum number of

floating capacitors to realize a given M value according to the Fibonacci limit, but the synthesis of such a fractional topology is usually performed by trial and error. Instead, this paper gives an example of systematic derivation of two-clock-phase topologies. Comparing the performance of various two-clock-phase topologies to each other, the output impedance is the same given the same switching frequency, total floating capacitance and total switch area. However, this paper has shown that depending on the application, performance differences e.g. in the amount of bottom-plate losses, the voltages appearing across the floating capacitors or the blocking voltages of power switches, different topologies come out favorably for different applications.

Using more than two clock phases allows the extension of the achievable range of M values of two-clock-phase converters. This allows realizing a target M with a lower number of floating capacitors, which can be advantageous in applications using external floating capacitors. A comparison between two-clock-phase and binary multi-clock-phase topologies shows that though the range of M values is smaller, the density of available M values in a certain needed range is higher in two-clock-phase topologies. This increases the achievable average efficiency across e.g. the desired input voltage range compared to binary multi-clock-phase topologies. Moreover, two-clock-phase topologies use less area to implement the power switches, which may be favorable for high-power applications. However, the modular approach to generate different conversion ratios with the binary multi-clock-phase reduces complexity in generating a larger number of conversion ratios.

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