VHDL Design and FPGA Implementation of the PWM Space Vector of an AC Machine Powered by a Voltage Inverter

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Abstract This paper presents a VHDL design and FPGA implementation of the space-vector pulse-width modulation (SVPWM) strategy. This design is made in a way that each block of the architecture is described on a separate entity. The global block is represented using the above entities as components. The proposed architecture for SVPWM is composed of four blocks. After the implantation of each block, we note that the resources consumed by the global entity, knowing that the same circuit is used for the different blocks namely the Stratix II device EP2S15F484C3, are 1185 ALUTs. The execution time of our architecture is two clock cycles.

Keywords SVPWM · FPGA · Vector control · VHDL · Asynchronous machine

1 Introduction

The control of AC machines with a voltage inverter frequently uses pulse width modulation techniques to control power switches. The pulse width modulation techniques are multiple. The choice of one of them depends on the type of control that is applied to the machine [1], on the inverter modulation frequency and on the harmonic constraints set by the user [2]. The modulation can be made in various approaches, particularly by comparing the reference to a triangular function [3] or applying the currently used space vector pulse width modulation (SVPWM). The principle of this technique is based on the selection of the sequence and the

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calculation of the conduction or the extinction time. In this work, we present the design of the various blocks of the vector modulation [2]. The proposed architecture is implemented on a FPGA circuit. We have used the VHDL language to describe our architecture and Quartus II tool for logic synthesis.

2 Principle of Vector PWM

A three-phase inverter with two voltage levels, has six switching cells, giving eight possible switching configurations. These eight switching configurations (denoted V_0–V_7) can be expressed in the reference (αβ) by 8 tensions vectors, among which two are null and others are equi-distributed every 60° [4].

3 Conception of SVPWM Blocks

3.1 Determination of the Reference Voltages V_α, V_β

This block is used to project the three-phase-voltages in the reference (αβ) by performing the transformation of Concordia [2, 5].

3.2 Determination of the Sectors

The determination of the sector is by comparing V_α and V_β tensions as shown in Table 1.

Once the sector number is determined, it is necessary to apply adjacent vectors to the sector concerned respectively during the period T_1 and T_2 [6].

Table 1 Identifying sector

Sectors	$V_\alpha > 0$	$V_\alpha > \sqrt{3}V_\beta$	$V_\alpha > -\sqrt{3}V_\beta$
I	1	0	1
II	0	0	1
III	0	0	0
IV	0	1	0
V	0	0	0
VI	1	1	0

Table 2 Calculation of the duration T_1 and T_2 for each sector

N° sector	i = 1	i = 2	i = 3	i = 4	i = 5	i = 6
The duration of vectors	$T_1 = X$ $T_2 = Z$	$T_1 = Y$ $T_2 = -X$	$T_1 = Z$ $T_2 = -Y$	$T_1 = -X$ $T_2 = -Z$	$T_1 = -Y$ $T_2 = X$	$T_1 = -Z$ $T_2 = Y$

3.3 Calculation of the Variables

We define intermediate variables X, Y, Z

$$X = \sqrt{(2/3)}\, V_\alpha . \mathrm{Tmod}/E \quad Y = \left(\frac{V_\alpha}{\sqrt{6}} + \frac{V_\beta}{\sqrt{2}}\right)\frac{\mathrm{Tmod}}{E}$$
$$Z = \left(\frac{-V_\alpha}{\sqrt{6}} + \frac{V_\beta}{\sqrt{2}}\right)\frac{\mathrm{Tmod}}{E} \tag{1}$$

3.4 Calculation of the Duration T_1 and T_2 for Each Sector

See Table 2.

3.5 Generation of the Series of Pulses Ta, Tb and Tc

For each inverter arm, it is necessary to define the timing that defines the time during which the middle point of one arm is E/2 or −E/2 within a switching period of the inverter. There are different PWM implementation strategies ensuring the achievement of the desired tension. To reduce the harmonics it is preferable to generate voltages centered on the modulation period of the inverter.

4 Design and Implementation of Our Architecture of the Space Vector Modulation

The proposed architecture for SVPWM is composed of four main parts. The first is the Concordia matrix. The second is the scan_sector block. The third block calculates the duration T_1_T_2 adjacent to each sector of vectors and the last block is generation_ pulse which generates the pulses to be applied to the various arms of the inverter.

Several studies on SVPWM command have already been carried out both at the university or industrial sectors [2]. The FPGA used for implantation is the Altera's Stratix 2 EP2S15F484C3.

4.1 Determination of the Reference Voltages V_α, V_β

This block is used to project the three-phase voltages in the reference (αβ) by performing the transformation of Concordia (Fig. 1).

4.2 Determination of Sectors

The determination of the sector is by comparing two voltages V_α and V_β (Fig. 2).

4.3 Calculation of T_1 and T_2 for Each Sector

The inputs of this block are the values of V_α, V_β, Tmod and sector number provided by the previous block. This block calculates the times T_1 and T_2 during which the two vectors adjacent to the sector are applied respectively (Fig. 3).

4.4 Pulse-Generation

See Fig. 4.

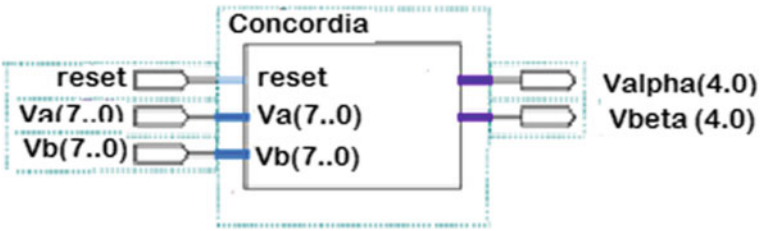

Fig. 1 RTL schematic of the Concordia matrix

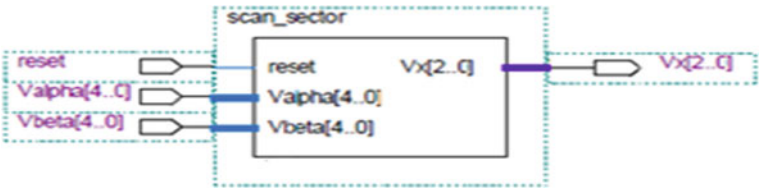

Fig. 2 RTL block diagram of scan_sector

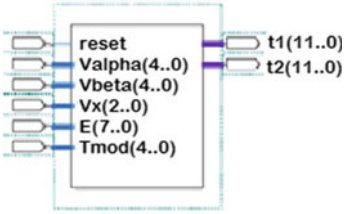

Fig. 3 RTL schematic of T_1-T_2 Duration

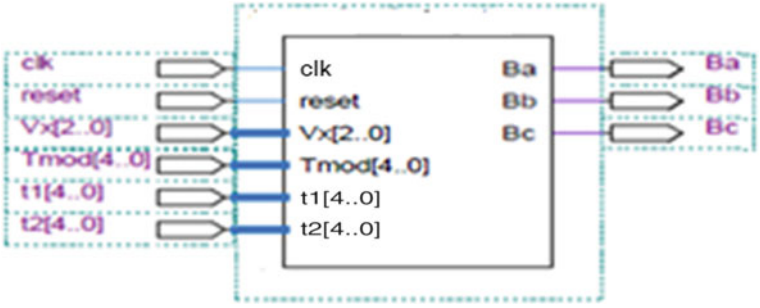

Fig. 4 RTL schematic of the pulse-generation unit

4.5 Validation of the Proposed Architecture

The proposed architecture for SVPWM is presented by Fig. 5. It is based on the selection of the sequence and the calculation of the conduction or the extinction time. The global block is represented using the above entities as components.

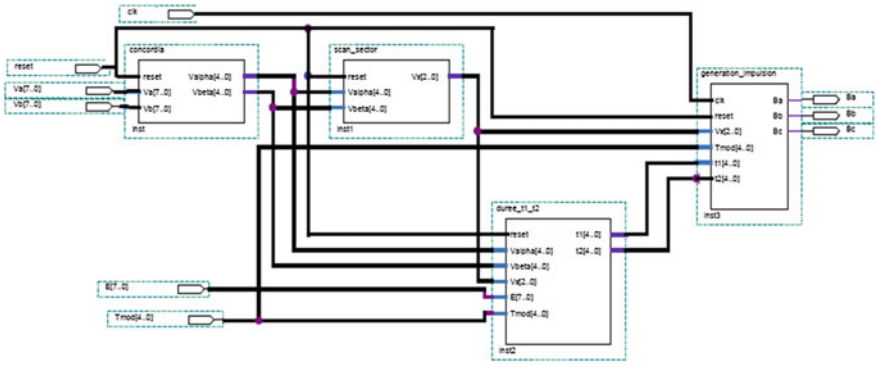

Fig. 5 RTL schematic of the global entity unit

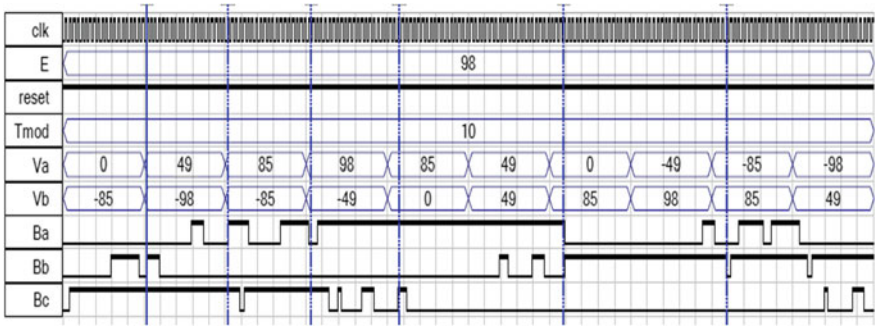

Fig. 6 Simulation result

This block generates the pulses applied to the arm of the inverter according to T_1 and T_2 values by having a PWM centered. It is clear that the sector 2 for example the timing of the pulses B_a, B_b and B_c match the desired results: $B_a = 1$ during T_1, $B_b = 0$ during T_2 and B_c is always equal to 1, i.e. We apply vector $V_2 = (010)$ during T_1 and vector $V_3 = (110)$ for T_2. The vectors V_2 and V_3 are adjacent vectors in sector 2 (Fig. 6).

Our proposed architecture responds after two clock cycles with a complexity of 1185 LUTs.

5 Conclusion

The approach of the VHDL design and FPGA implementation of the algorithm modeling the SVPWM proposed in this paper has permitted to achieve high performance when reducing complexity. Indeed, the proposed architecture responds after two clock cycles with a complexity of 1185 LUTs.

The vector control of an AC machine of this architecture allows exploitation of the results proposed in this work.

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