Chapter 27
Conclusions

As the power delivery system transforms from a lumped network with a few off-chip converters into a heterogeneous, distributed, dynamically controlled system with many thousands of on-chip power components, the design, synthesis, and control objectives of the power delivery process need to be rethought at the system level. To cope with the complexity of system-wide power optimization, efficient techniques to model, analyze, and optimize a power delivery system are required.

The generation and distribution of high quality power to the load circuitry are two primary issues in the power delivery process. The interconnect network distributing power within a modern microprocessor typically contains many millions (to several billions) of nodes. The design of power distribution networks is typically performed at several design stages, iteratively increasing the accuracy of the current flow estimate while reducing the granularity of the power distribution network. Furthermore, the power distribution network is allocated over a large area with the entire network interacting, requiring near full scale simulation. Efficient and accurate analysis is therefore a key factor in the design of high performance power delivery systems. A number of synthesis and analysis algorithms are available to enhance the power delivery design process. Accuracy and computational efficiency is the primary tradeoff within these design algorithms and tools. A methodology is described based on a model of a two-port infinite mesh, providing both high accuracy and computational efficiency when analyzing large scale power networks.

While the quality of the power supply can be efficiently addressed with distributed on-chip power supplies, the stability of these parallel connected voltage regulators is also a primary concern. To maintain a stable power delivery system composed of multiple parallel connected regulators, a passivity-based stability criterion can be used. A distributed power delivery system is stable if the total output impedance of the parallel connected LDOs exhibits no right half plane poles and a phase between $-90°$ and $+90°$. This PBSC-based approach is evaluated on a fully integrated power delivery system with distributed on-chip low dropout regulators,

I.P. Vaisband et al., *On-Chip Power Delivery and Management*,
DOI 10.1007/978-3-319-29395-0_27

fabricated in a 28 nm CMOS process. The experimental results of a distributed power delivery system satisfy this passivity-based criterion, yielding a stable system response.

An additional objective is the development of design methodologies to efficiently utilize the available resources, such as area, metal, and power. A novel link breaking methodology is discussed to optimize a mesh structured power distribution network. The resulting power distribution network is a combination of a single power distribution network to lower the network impedance, and multiple networks to reduce noise coupling among the circuits. Since the sensitivity to supply voltage variations within a power distribution network can vary among different circuits, this methodology reduces the voltage drop at the more sensitive circuits while penalizing the less sensitive circuits. This methodology is evaluated for multiple case studies, reducing voltage drops in the sensitive circuits (the critical paths).

The parasitic impedance of the interconnects, decoupling capacitances, load circuits, and on-chip power regulators are computationally expensive to simultaneously analyze. The distinctive properties of a power network have been exploited to develop closed-form expressions for the effective resistance between circuit components. This effective resistance model is based on the physical distance between circuit components within a two layer mesh where the horizontal and vertical unit resistances may be different. This effective resistance model is utilized in the development of a power grid analysis algorithm to compute the node voltage without requiring any iterations. This algorithm drastically improves computational efficiency since the iterative procedures commonly used to determine *IR* drop and *L di/dt* noise are no longer needed. The symmetric nature of the power and ground distribution networks and the principle of spatial locality are also exploited to further enhance the computational efficiency and accuracy of the analysis process.

Exhaustive ad hoc approaches for co-designing power supplies at different levels of hierarchy within a power delivery system exhibit significant design complexity and are computationally impractical in DVS/DVFS systems with hundreds to thousands of power domains. A computationally efficient methodology to co-design switching converters and on-chip linear regulators within a heterogeneous system is described, achieving high quality power and efficiency within limited on-chip area. Dynamically clustering a heterogeneous power delivery system is demonstrated on a suite of IBM benchmark circuits, exhibiting a computationally and power efficient alternative to existing ad hoc methodologies that employ either switching or linear on-chip power supplies.