Chapter 14
Simultaneous Co-Design of Distributed On-Chip Power Supplies and Decoupling Capacitors

Multiple power supplies are widely used in high performance integrated circuits to provide current close to the load circuitry in high performance integrated circuits [289]. The number of on-chip power supplies is increasing, requiring innovative design methodologies to satisfy the stringent noise and power constraints of these high complexity integrated circuits [299–302]. Placing the power supply on-chip eliminates losses due to the package parasitic impedances, improving the quality of the delivered power [289].

To provide multiple on-chip power supplies, linear voltage regulators are typically used which require small area with fast load regulation to realize point-of-load voltage delivery [303]. These power supplies alone, however, do not satisfy stringent power and noise constraints. Decoupling capacitors are therefore widely used as a local reservoir of charge which are self-activated and supply current when the power supply level deteriorates [304], as previously discussed in Chap. 14. Inserting decoupling capacitors into the power distribution network is a natural way to lower the power grid impedance at high frequencies [136]. A representative power delivery network with on-chip power supplies, decoupling capacitors, and load circuits is illustrated in Fig. 14.1. Tens of on-chip power supplies, hundreds-to-thousands of on-chip decoupling capacitors, and millions-to-billions of active transistors are anticipated in the design of next generation high performance integrated circuits.

Power supplies and decoupling capacitors exhibit similar characteristics with some important differences such as the response time, decay rate of the capacitor, on-chip area, and power efficiency. On-chip power supplies require greater area, provide limited power efficiency, and exhibit slower response time as compared to decoupling capacitors. Decoupling capacitors, however, should be placed close to a power supply to recharge before the next switching event [304]. Additionally, the placement of the decoupling capacitors should consider the resonance formed by the decoupling capacitor and the power grid inductance which degrades the effectiveness of the decoupling capacitor [305]. Existing design methodologies for

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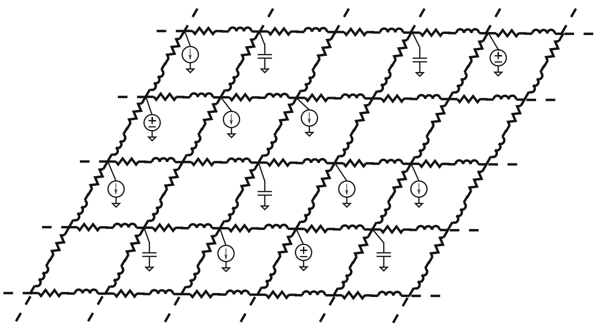

Fig. 14.1 A uniform power distribution network with multiple on-chip power supplies, decoupling capacitors, and current loads. Current loads are used to model the active circuits

placing decoupling capacitors assume one or two on-chip power supplies [304] or one decoupling capacitor interacting with multiple power supplies [306]. These assumptions are inappropriate when voltage is regulated at the point-of-load with multiple on-chip power supplies and decoupling capacitors. Design methodologies are therefore required to simultaneously place multiple on-chip power supplies and decoupling capacitors.

The effective radii of the decoupling capacitors have been developed for a single current path between a current load and a single decoupling capacitor, as described in Chap. 12, and for a mesh structure considering a single decoupling capacitor in [306]. In this chapter, not only the interactions among the power supplies, decoupling capacitors, and load circuitry but also the interactions among the power supplies and between the decoupling capacitors are considered. Those interactions considered in this chapter are schematically illustrated in Fig. 14.2.

These interactions among the circuit components are complicated by the increasing number of components in the power delivery network. In this chapter, interactions among the power supplies, decoupling capacitors, and current loads are evaluated. A methodology is described to simultaneously determine the optimum location of the distributed power supplies and decoupling capacitors within the overall power distribution network, providing an integrated approach to delivering power.

The rest of this chapter is organized as follows. The problem is formulated in Sect. 14.1. Interactions among the on-chip power supplies, decoupling capacitors, and load circuits are analyzed and a methodology for simultaneous power supply and decoupling capacitor placement is presented in Sect. 14.2. Case studies examining the interactions among the power supplies, current loads, and decoupling capacitors are provided in Sect. 14.3. Some specific conclusions are summarized in Sect. 14.4.

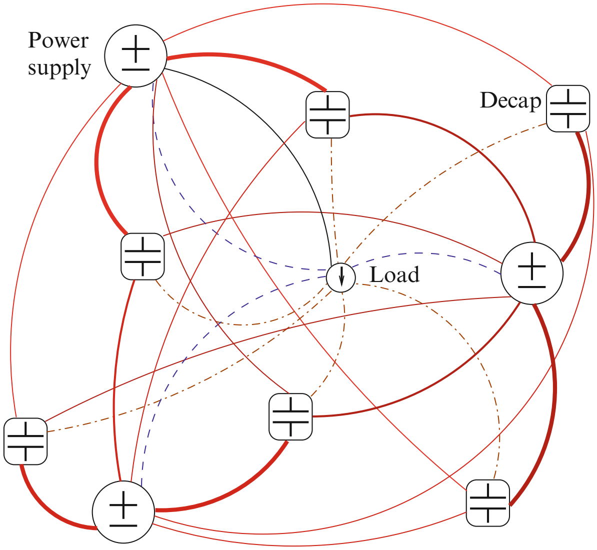

Fig. 14.2 Interactions among the on-chip power supplies, decoupling capacitors, and load circuits. *Thicker lines* represent greater interaction. Note that the effect of a power supply or a decoupling capacitance on the load circuits depends strongly on the physical distance

14.1 Problem Formulation

Power distribution networks are typically modeled as a uniformly distributed *RL* mesh structure. By exploiting the uniform nature of the power grid, the *Euclidean distance* between the circuit components can be used to determine the effective impedance between arbitrary nodes. A closed-form expression for the effective impedance in an infinite resistive mesh is provided by Venezian in [307]. This expression is modified both to produce more accurate results and to include the inductance of the power grid as the power grid impedance depends strongly on the inductance at high frequencies. A closed-form expression to determine the effective impedance between two nodes, N_{x_1,y_1} and N_{x_2,y_2}, is

$$Z_{m,n} = z * \frac{1}{2\pi} * ln(n^2 + m^2) + 0.51469, \tag{14.1}$$

where

$$m = |x_1 - x_2| \text{ and } n = |y_1 - y_2|. \tag{14.2}$$

z is the impedance of one segment of the grid. Applying this effective impedance concept, multiple current paths are considered without increasing the computational complexity of the power grid analysis process.

The complicated power distribution network schematically illustrated in Fig. 14.2 is simplified to a network consisting of only equivalent impedances among the power supplies, decoupling capacitors, and load circuitry. Multiple current paths are efficiently considered using the simplified model in (14.1).

14.2 Simultaneous Power Supply and Decoupling Capacitor Placement

Interactions among a single power supply, decoupling capacitor, and current load are illustrated in Fig. 14.3. The equivalent parasitic resistance and inductance between the power supply and decoupling capacitor, power supply and load circuit, and decoupling capacitor and load circuit are represented, respectively, as R_{vd} and L_{vd}, R_{pl} and L_{pl}, and R_{dl} and L_{dl}. The load current I_l is

$$I_l = i_{dl} + i_{pl}. \tag{14.3}$$

The current supplied from the decoupling capacitor and power supply is represented, respectively, as i_{dl} and i_{pl}. The ratio of the current supplied to the active circuits from the power supplies and decoupling capacitors depends upon the physical distances, the parasitic impedance among these components, and the size of the decoupling capacitors. i_{dl}/i_l increases for greater R_{pl} and L_{pl}, enhancing the effect on the load circuit of the decoupling capacitors as compared to the effect of the power supplies.

The effective region of a decoupling capacitor depends upon the location of those power supplies, decoupling capacitors, and load circuits in close proximity as well as the power grid impedance, and rise and fall times of the load currents. A uniform

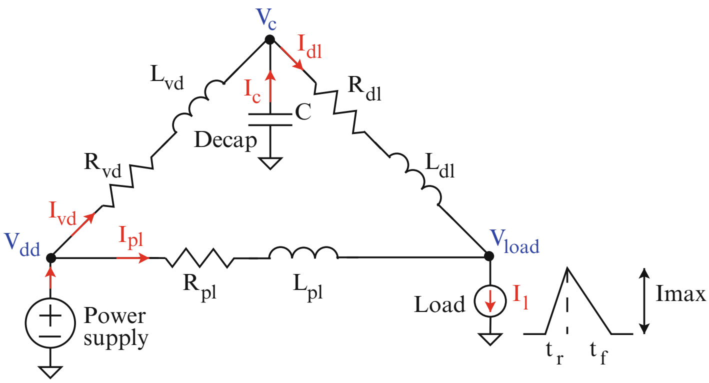

Fig. 14.3 Simplified interactions among a power supply, decoupling capacitor, and load circuit. The components are connected with the corresponding equivalent impedance in the power grid modeled by (14.1). The load current is modeled as a *triangular* current load with a rise time t_r and fall time t_f

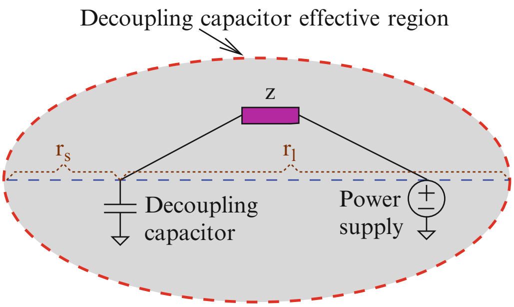

Fig. 14.4 Elliptic structure to illustrate the effective region of a decoupling capacitors with a single power supply. The short radius (r_s) and long radius (r_l) depend upon the size of the capacitor and the effective impedance between the capacitor and power supply

current distribution is assumed in this chapter to simplify this analysis. The analysis can however be generalized to a non-uniform load current distribution. The effective region for a single decoupling capacitor with a single power supply is illustrated in Fig. 14.4. The effective region exhibits an elliptic shape due to the non-uniform location of the power supplies. This elliptic shape can be explained intuitively by examining Fig. 14.4. The current supplied to the load circuit in this elliptic region is provided by the decoupling capacitor and the local power supply. When the load circuit is moved out of this elliptic region, most of the load current is provided either by the local power supply or decoupling capacitor due to the increased parasitic impedance. When the load current is supplied both by the local power supply and the decoupling capacitor, the response is faster and more effectively suppresses the switching noise.

The elliptic shape also depends upon the technology parameters and the noise constraints. The area of the elliptical region is small when the noise constraints of the power distribution network are high. For example, when the maximum target noise of the power distribution system is 5 % of the supply voltage, a smaller ellipse is formed as the effective region around the decoupling capacitor. Alternatively, the area of the elliptic region increases when the noise constraint is increased to 10 % of the supply voltage. Consequently, elliptic equipotential shapes are formed around the decoupling capacitors and power supplies, denoting identical power supply voltage levels.

An elliptic region is described by a long and short radius represented as r_l and r_s, respectively, as shown in Fig. 14.4. r_l can be determined as

$$r_{l_{(n,m)}} = \frac{K * C}{R_{(x_1,y_1)} + k * L_{(x_1,y_1)}}, \tag{14.4}$$

where C is the decoupling capacitance and the effective resistance and inductance between the decoupling capacitor and the power supply are represented, respectively, as $R_{(x_1,y_1)}$ and $L_{(x_1,y_1)}$. The horizontal and vertical distance from the decoupling capacitor to the power supply is represented, respectively, as x_1 and y_1. The effect of the transition time of the load current is embedded into the equation using k. K models the noise constraints, i.e., a smaller K is used for more stringent noise constrained circuits.

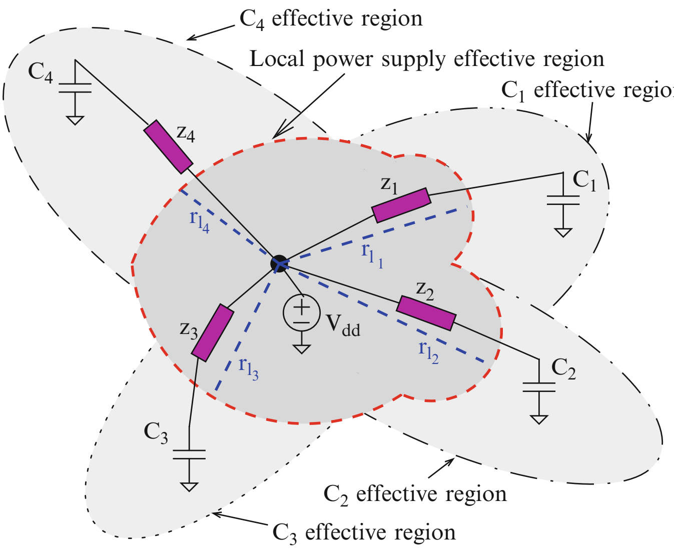

Fig. 14.5 Modified elliptic structure to illustrate the effective regions for a local power supply and decoupling capacitors. Note that the effective region for a local power supply is the overlap of the effective regions for the surrounding decoupling capacitors

The effective region for a local power supply with four decoupling capacitors is illustrated with a dark shaded modified elliptic shape in Fig. 14.5. Since the power supply interacts with four different decoupling capacitors, the effective region is the overlap of the four different elliptic shapes. Since the effect of a decoupling capacitor on r_s is limited, the effective region of the power supply can be described with four different r_l, denoted as r_{l1}, r_{l2}, r_{l3}, and r_{l4}, to represent the effect of, respectively, C_1, C_2, C_3, and C_4. A similar analysis can be performed when the system includes multiple decoupling capacitors and multiple power supplies. Each decoupling capacitor is affected by the remaining decoupling capacitors and power supplies. The effective region of a decoupling capacitor or power supply is therefore described as the overlap of the elliptic equipotential surfaces caused by each power supply and decoupling capacitor, as illustrated in Fig. 14.5.

14.3 Case Study

The method of overlapping elliptic equipotential surfaces to determine the effective region has been verified with SPICE simulations. A uniform *RL* grid structure with 20 horizontal and vertical lines (20 × 20 mesh) is assumed in the analysis. The supply voltage is 1 V and the uniformly distributed current loads switch at a 1 GHz frequency with rise and fall times of, respectively, 100 and 300 ps. A

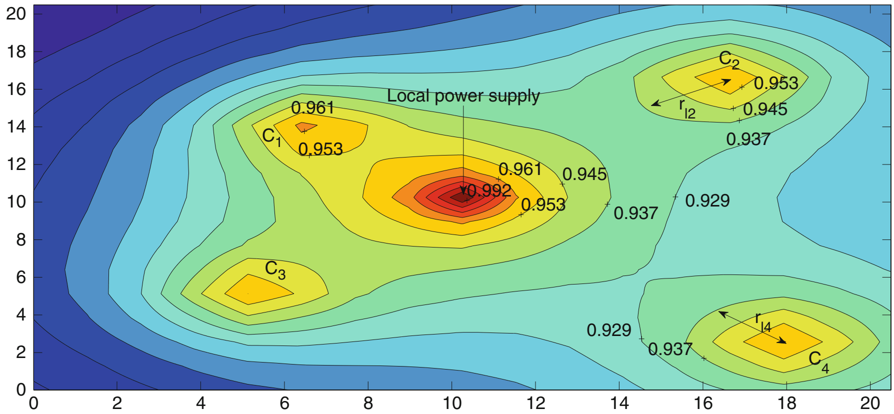

Fig. 14.6 Effective region for a local power supply at $N_{(10,10)}$ with four decoupling capacitors at $N_{(17,17)}$, $N_{(18,2)}$, $N_{(5,5)}$, and $N_{(6,14)}$ in the power distribution network. Note the elliptic shapes around the decoupling capacitors and modified elliptic shape around the local power supply

power distribution system with a local power supply and four decoupling capacitors is initially evaluated. The power supply is placed at $N_{(10,10)}$ and the decoupling capacitors C_1, C_2, C_3, and C_4 are placed, respectively, at nodes $N_{(6,14)}$, $N_{(17,17)}$, $N_{(5,5)}$, and $N_{(18,2)}$. A simulation of the power distribution network is illustrated in Fig. 14.6.

Since the closest decoupling capacitor to the local power supply is C_1, the effective region of the power supply extends towards C_1. Alternatively, the effective region of the local power supply is limited towards C_4 since C_4 is farther from the local power supply. The long radius of the effective regions for C_2 and C_4 is shown in Fig. 14.6 as, respectively, r_{l_2} and r_{l_4}. The ratio r_{l_2}/r_{l_4} is 1.2 as compared to 1.15 from (14.4), exhibiting an error of less than 5 %.

The effect of the transition time of the load current on the effectiveness of the decoupling capacitors and power supplies has also been evaluated. A 20×20 power grid with five decoupling capacitors placed at $N_{(3,3)}$, $N_{(3,17)}$, $N_{(10,10)}$, $N_{(17,3)}$, and $N_{(17,17)}$ and four on-chip power supplies located at $N_{(3,10)}$, $N_{(10,3)}$, $N_{(10,17)}$, and $N_{(16,10)}$ is evaluated. For rise and fall times of the load current of 50 and 150 ps, respectively, the effective region for the decoupling capacitors and power supplies is illustrated in Fig. 14.7a. Note that the effective region of the power supplies and decoupling capacitors exhibits similar behavior as the area of the surrounding equipotential surfaces are approximately the same. No resonance occurs and the decoupling capacitors are sufficiently close to the power supplies to be recharged before the next switching event.

The effective region of the power supplies and decoupling capacitors is depicted in Fig. 14.7b when the rise and fall transition times of the load current are increased to, respectively, 200 and 600 ps. Note that the area of the effective region of the decoupling capacitors becomes smaller. The cause of the reduced effective

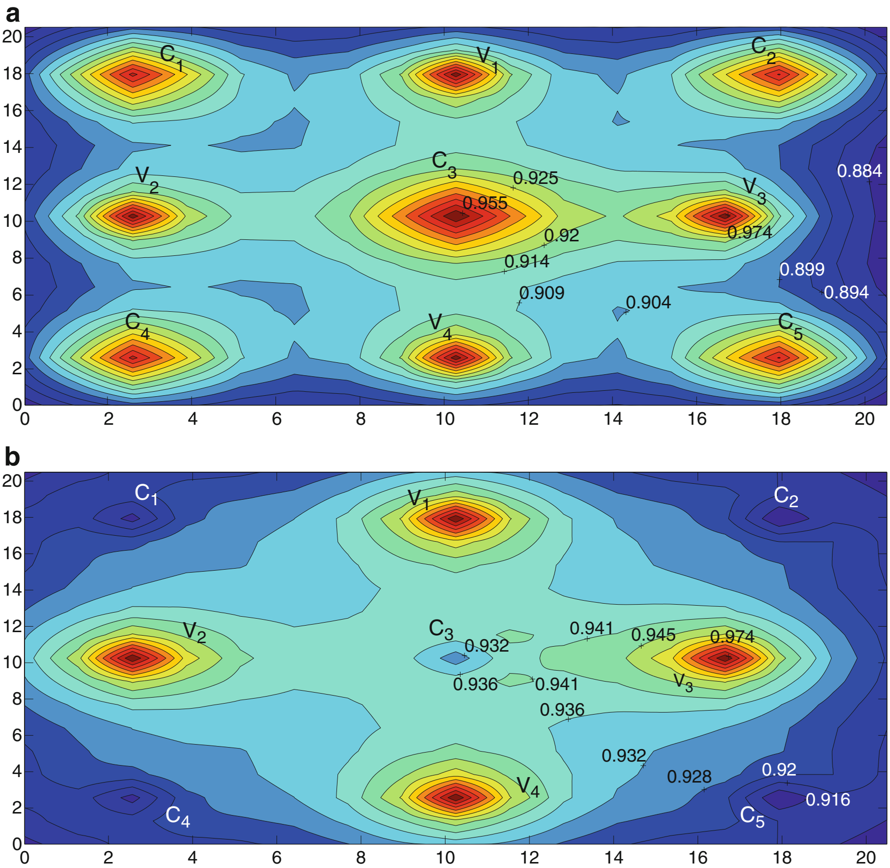

Fig. 14.7 Effective region for multiple decoupling capacitors and power supplies. Four decoupling capacitors, C_1, C_2, C_4, and C_5, are located at the corners and one decoupling capacitor C_3 is located in the middle of the power distribution network. The four power supplies are placed between the decoupling capacitors; (**a**) rise and fall transition times are, respectively, 50 and 150 ps, (**b**) rise and fall transition times are, respectively, 200 and 600 ps

region around the decoupling capacitors is that the equivalent transition times produce a resonance [305] formed by the decoupling capacitor and the power grid inductance. Also, the capacitors cannot fully recover before the next switching event. The resonance phenomenon is considered in (14.4) with k. The effective region around the on-chip power supplies is not significantly affected by the change in transition time. Considering all of these distinct properties (such as the resonance and decay rate of the capacitor) of the decoupling capacitors and power supplies can significantly improve the quality of the power distribution network.

14.4 Summary

The simultaneous co-design of distributed on-chip power supplies and decoupling capacitors is described in this chapter. The primary results are summarized as follows.

- A fundamental change in the design process of on-chip power distribution networks is necessary with the increase in the number of on-chip power supplies
- A closed-form expression to determine the effective impedance between two nodes in a uniform *RL* network is provided
- The effect of the rise and fall transition times on the effective region of the decoupling capacitors is discussed
- A closed-form expression to determine the effective elliptic region of multiple decoupling capacitors is provided
- Highly complex interactions among the power supplies, decoupling capacitors, and load circuitry are evaluated
- The analysis and simultaneous co-placement of on-chip local power supplies and decoupling capacitors are required to provide a more efficient power delivery system