Design, Simulation and Analysis of 4 × 1 Mux at 90 nm CMOS Technology

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Abstract Power and delay are regarded as the most fundamental design constraints that form the basis of comparative analysis of logic style implementation of any arbitrary circuit. Previously published research works and investigations have proposed various low power logic style implementations of 2:1 multiplexer circuits. This paper focuses on the design, simulation and analysis of 4:1 multiplexer circuit using CMOS, CVSL, PTL and dynamic logic styles at 90 nm technology followed by a comparison of the circuit performance w.r.t. power, delay and power-delay product. Further, based on this evaluation of circuit families; it has been shown that transmission gate (CMOS+) is the logic style of choice which is most optimized and efficient both in terms of power and speed within 1.6–2.4 V supply voltage range. The circuits have been designed and simulated using BSIM 3V3 90 nm technologies on Tanner EDA tool.

1 Introduction

Multiplexer is a universal logic element that is most commonly used in communication systems including TDM and optical communication systems. Hence, it needs to be optimized in terms of both power and speed in order to obtain high

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performance digital systems. The increasing demand for low-power VLSI can be addressed at different design levels, such as the architectural, circuit, layout and the process technology level. At the circuit and layout level, the power dissipation can be minimized by effectively reducing the sub-threshold conduction as well as reverse biased leakage currents. Short circuit currents, although assumed to be negligible, have been found to constitute 10–30 % of overall power consumption [1]. Minimizing delay is also an important design objective that needs to be addressed. The delay of a logic gate usually depends upon the width of transistors in the logic gate, its output current, output load capacitance and the output voltage swing [1, 2]. Faster circuit families, therefore attempt to reduce one of these parameters. Sections 2 and 3 includes a brief theoretical description of some of the basic concepts related to power, delay and power-delay product as well as the various static and dynamic logic styles. Simulation waveforms and results in the form of graphical and tabular representations have been shown in Sect. 4. Finally, some conclusions have been drawn in Sect. 5.

2 Parameters Analyzed

2.1 Power Analysis

Power is considered to be one the most important factors in designing today's VLSI circuits. Total power losses constitute both static and dynamic losses.

$$P_{(total)} = P_{(static)} + P_{(dynamic)} \tag{1}$$

Unlike a few years back, when the dynamic power losses dominated any other type of power losses [3]; with the recent shift towards UDSM level designing, nowadays static power losses too have become a key concern. Subthreshold conduction, gate oxide tunneling current, leakage through reverse biased diodes, and contention current in ratioed circuits are the main reasons for static losses [4]. These losses occur primarily because of ultra-thin channel length and carrier power overcoming barrier voltages. High doping levels of about 1×10^{18} cm^{-3} leads to decreased barrier potential and more carrier concentration; thus helping more charge movement even at very low voltages. Frequent charging-discharging of the load capacitances and short circuit currents make the major portion of dynamic power losses.

$$P_{dyn} = V_{DD}^2 \cdot f_{clk} \cdot \sum_n \alpha_n \cdot c_n + V_{DD} \cdot \sum_n I_{scn} \tag{2}$$

With the modern day technology, though decreased supply voltages should lead to low losses, however the need of fast switching activity, high clock frequency

(f_{clk}), high short circuit currents (i_{sc}) and highly complex circuits leads to more transitions and thus more dynamic power losses [3].

2.2 Delay Analysis

Delay present in any circuit increases with the increase in the number of inversion levels in series. Inter-wire capacitance, intra-wire capacitance, junction capacitance, interconnect capacitance all account for the increased delays.

$$t_{pd} = (C/I)\Delta V \tag{3}$$

Logical effort(C/I) accounts for all these factors quantitatively. Dynamic circuits were developed with the idea to use the internal capacitances to hold some valuable information which in case of static circuits is cause of only delays [5]. These circuits prove to be beneficial when fast operation speeds are required. pMOS transistors have higher internal and node capacitances and also the hole carrier speed is less as compared to the electrons; it is for these reasons nMOS are chosen over pMOS to implement circuits [6, 3].

2.3 Power Delay Product Analysis

The power delay product is a fundamental parameter which is used for measuring the quality and performance of a CMOS process and gate design. As a physical quantity, the power delay product can be interpreted as the average energy required for a gate to switch its output voltage from low to high and vice versa.

To reduce power delay product,

- Reduce load capacitance
- Reduce supply voltage
- PDP does not capture the fact that reducing supply voltage lowers power con-sumption but increases delay.

3 Logic Styles

3.1 Cmos/Cmos+

CMOS has been the logic style of choice of many VLSI circuit designers for any arbitrary circuit because of the lucrative features of CMOS like full swing, theoretically no steady state losses and robustness against transistor downsizing

(ratioless) and voltage scaling. However it must be noted that optimum logic style for any circuit is technology independent. However a new class of CMOS circuits i.e. CMOS+ also called Transmission Gate has proved to be better than CMOS in terms of effective circuit orientation and providing near constant resistance throughout its operative lifecycle. It is a non-restoring circuit providing very less isolation between input and output. It can pass both 1s and 0s in an acceptable fashion.

3.2 Cascode Voltage Switch Logic

CVSL is dual rail logic. It uses almost the same number of transistors as CMOS does to implement the logic function but also generates non-inverted output. The two additional pMOS act as load driver circuits which have gates connected to the complementary output. CVSL has no steady state losses but is ratioed circuit. *Modified CVSL* or *MCVSL* is similar to CVSL implementation of function with the only modification that is to improve the driving capabilities of pMOS load by adding nMOS in parallel to it or in other words we can say we have a transmission gate as the load driver circuit. This improves the swing restoration at the output as well.

3.3 Cascode Voltage Switch Logic

PTL logic family has inputs connected not only to the gate of MOSFET but to either drain or source as well. This reduces the transistor count significantly w.r.t. CMOS or CVSL and size of transistor can be kept minimal as well. These features seem to fascinate IC designers; but higher delays in chaining and multi-threshold voltage drop when cascaded pose a serious problem to circuit efficiency. These problems including sneak path problem need to be taken care of by adding extra circuitry in the form of buffers and pull up transistors. All these factors annihilate the advantage of less MOSFET count, small area and small input load. Short circuit currents are also large due to competing signals in swing restoration circuitry.

3.3.1 *Complementary PTL* has both inverting buffers to restore the output levels and weak pull up PMOS to restore the inputs of those inverting buffers. These have low input loads and higher output driving capabilities.

3.3.2 *Swing restored PTL* forms a latch like structure by cross coupling the output buffers. Weak PMOS pull up networks are removed and the pMOS of the output inverting buffers acts as the level restoration transistor for the input of complementary output inverter. These circuits have slow switching, poor output driving capabilities and unreliable operation.

3.3.3 *Energy economized PTL* has the sources of pMOS transistor of CPL gate connected to complementary output signal instead of Vdd. It has low power losses, full swing and shorter delays. This circuit has the capabilities to make efficient circuits.

3.3.4 *Push Pull PTL* is a CPL without output buffers. Besides low transistor count, its output driving capabilities are worse than SRPL.

3.4 Dynamic Circuits

Dynamic circuits provide the advantages of CMOS (no steady state losses, full swing, low dynamic losses) and Pseudo nMOS (faster operation and less transistor count). In addition to this, the node capacitances which accounts for only delays in static circuits can be used to store some useful information in dynamic circuits. *Domino-circuits* are fast, synchronize the output and are ratioless circuits. They have an nMOS network in series with a pMOS transistor supplied with a clock signal. During the high clock, the output node precharges and evaluates only when clock is low. Output can only make a single high to low transition giving it monotonicity. Thus multiple stages are cascaded by having invertors at the output of each stage. Additionally nMOS footer transistor can be placed to guard against output discharging during precharge phase. Dynamic losses can be reduced by reducing the duty cycle of the clock to less than 50 %.

4 Simulation and Analysis

4.1 Simulation Environment

All the circuits have been simulated using BSIM 3V3 90 nm technologies on Tanner EDA tool. All the circuits have been simulated on exactly same input patterns to make sure of impartial testing environment. Every simulation has been performed on range of voltage varying from 1.6 to 2.4 V W/L ratio for NMOS transistors were kept 1.8/1.2 and [(W/L) p/(W/L) n] = 2.

4.2 Schematics

We present schematics of 4:1 multiplexer circuit that were designed in S-Edit using different logic styles which have been discussed in Sect. 3 (Figs. 1, 2, 3, 4, 5, 6, 7, 8 and 9).

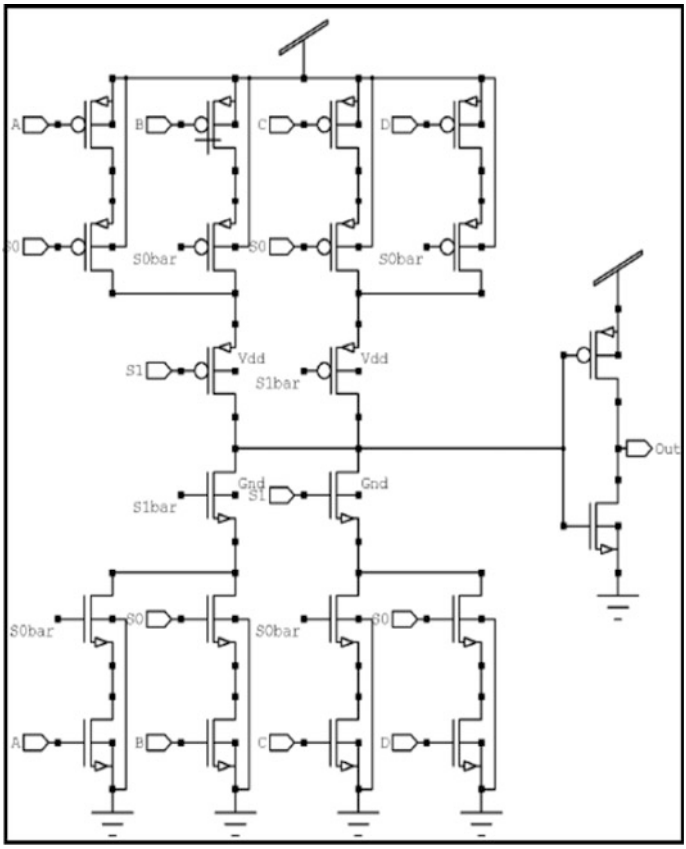

Fig. 1 Schematic of CMOS

4.3 Performance Analysis

This work includes power analysis, delay analysis and PDP analysis of the logic styles discussed above. In addition to them the same analysis was done for Pseudo-nMOS, LEAP and Dual Rail domino logic. Figure 10 depicts the power consumption versus Vdd for leap, pseudo nMOS, srpl, ppl, eepl, cpl, cmos, cmos +, cvsl, mcvsl, domino, dual-rail domino based 4:1 multiplexer circuit. CMOS + (transmission gate) circuit implementation of 4:1 multiplexer shows the least power consumption. Figure 11 shows maximum power consumption versus Vdd and Fig. 12 shows minimum power consumption versus Vdd for all 12 logic styles implemented for 4:1 multiplexer circuit. It shows that transmission gate absorbs least power in both the maximum power consumption state at Vhigh and also in the minimum power consumption state at Vlow. Here EEPL circuit shows least delay among all other design techniques (Figs. 13 and 14).

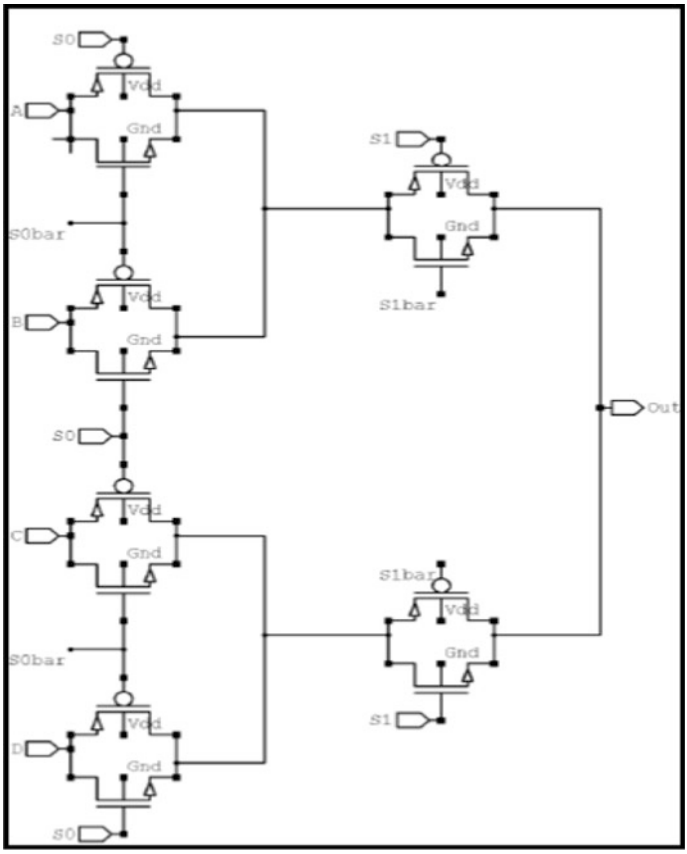

Fig. 2 Schematic of CMOS+

4.4 Results and Discussion

Waveform analysis of the different logic styles during realizing 4:1 multiplexer circuit using W-edit has been done. While performing waveform analysis of the designed circuits, we applied all the possible input values individually using bit pattern interface and also provided random values using pulse interface as voltage source. Finally using the given two figures below we show two categories of signal used in circuits. Figure 15 shows simulation of 4:1 multiplexer circuit using static circuits and Fig. 16 shows simulation of 4:1 multiplexer circuit using dynamic circuits.

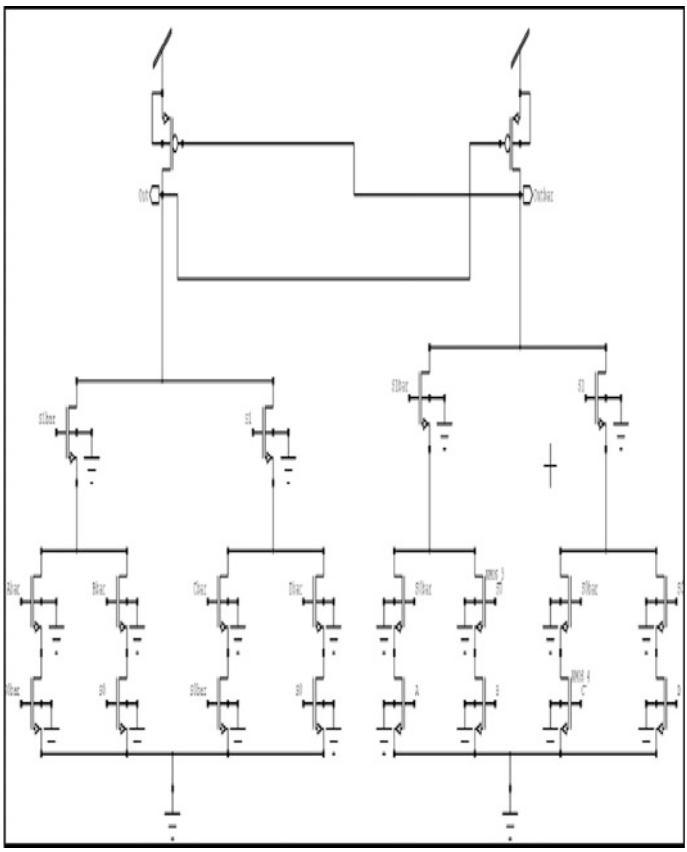

Fig. 3 Schematic of CVSL

Table 1 depicts the power delay product over a range of power supply voltages and it is shown in the table that transmission gate (CMOS+) circuit for 4:1 multiplexer shows minimum power delay product for a range of voltage values taken in consideration for low power circuits.

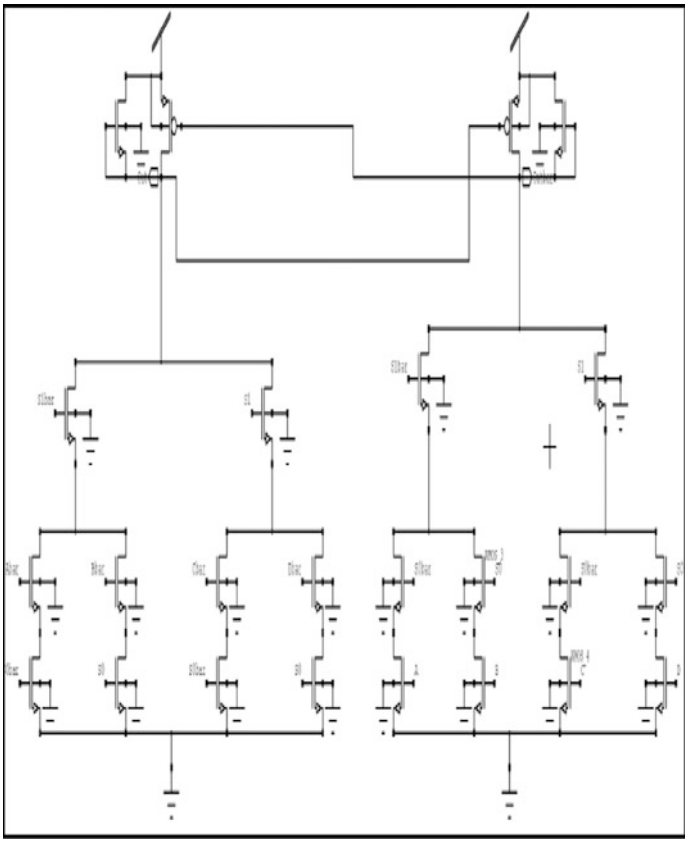

Fig. 4 Schematic of MCVSL

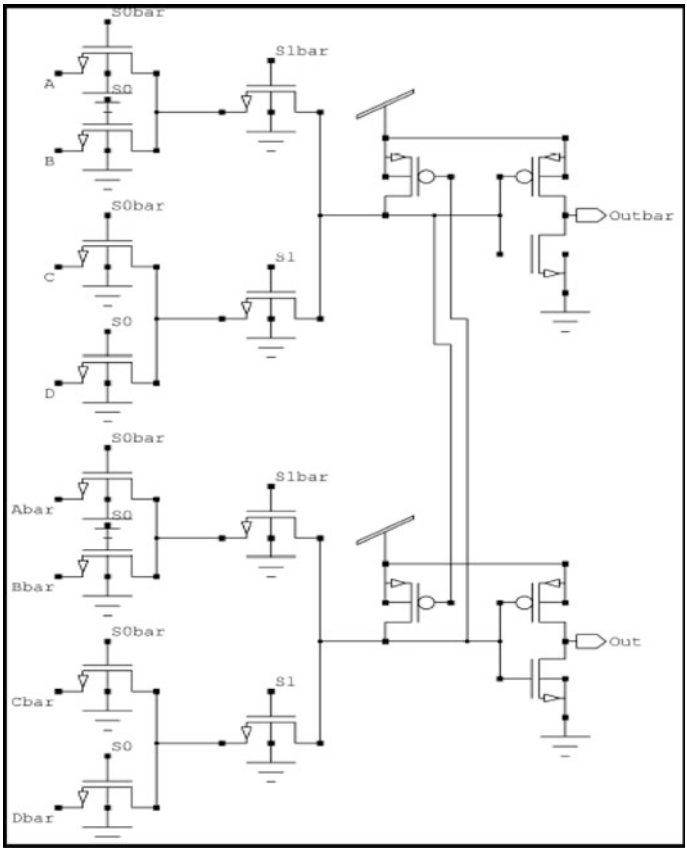

Fig. 5 Schematic of CPL

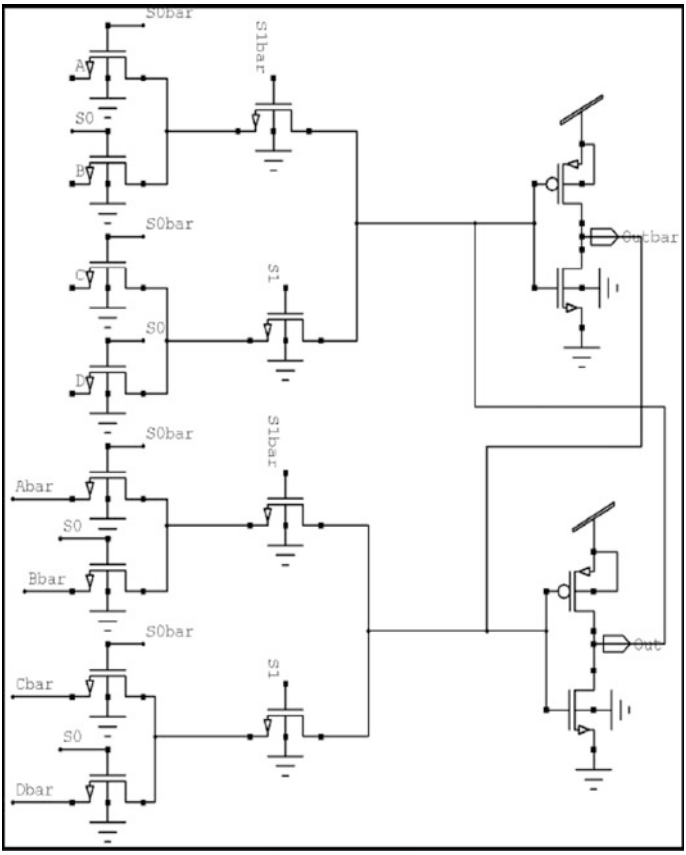

Fig. 6 Schematic of SRPL

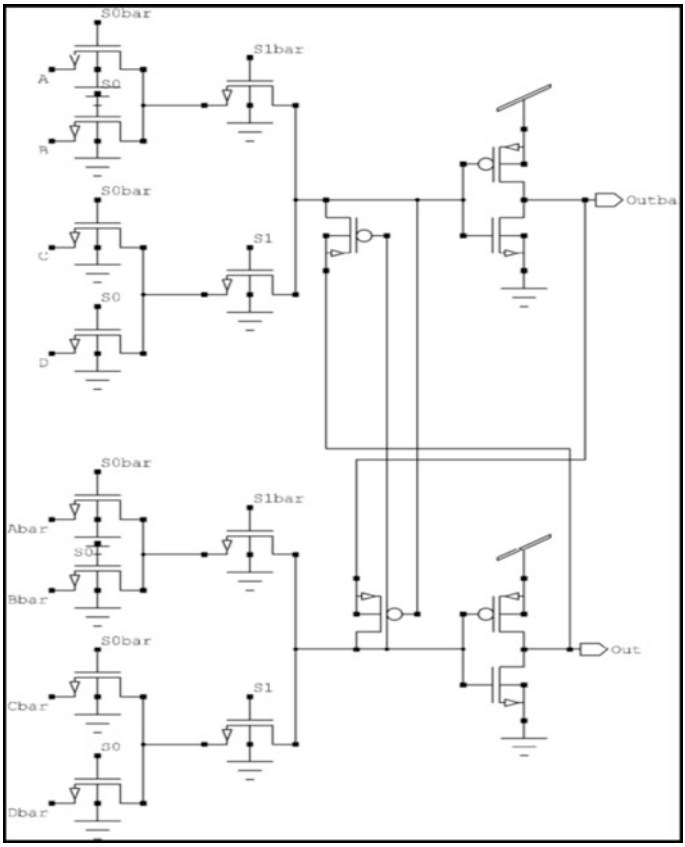

Fig. 7 Schematic of EEPL

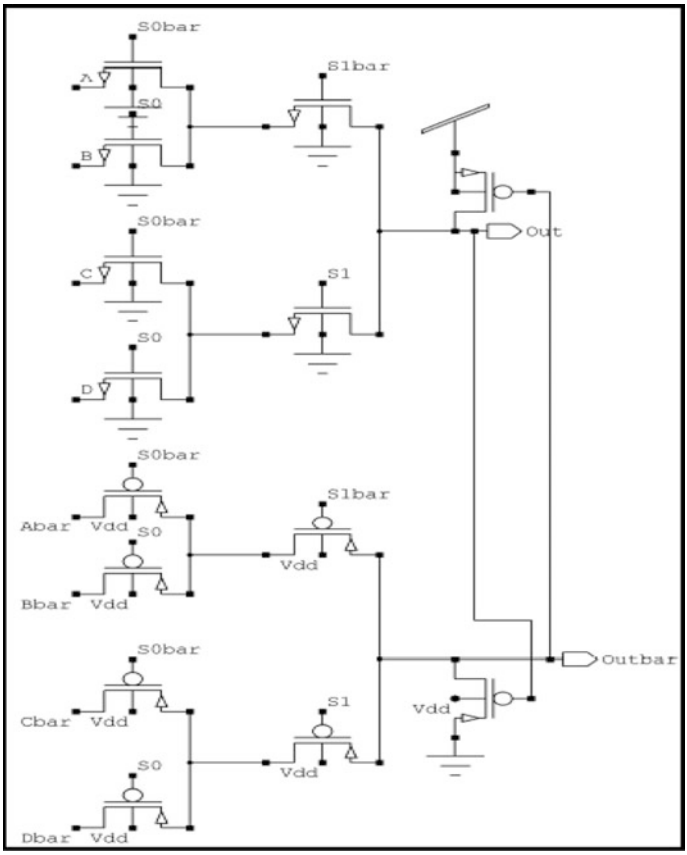

Fig. 8 Schematic of PPL

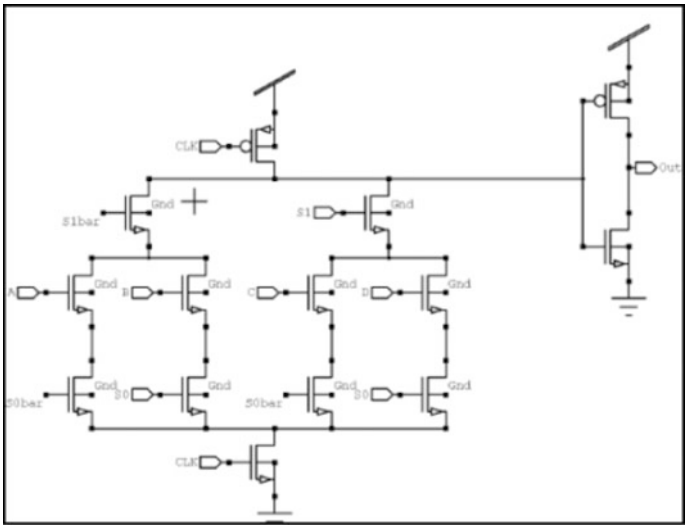

Fig. 9 Schematic of Domino

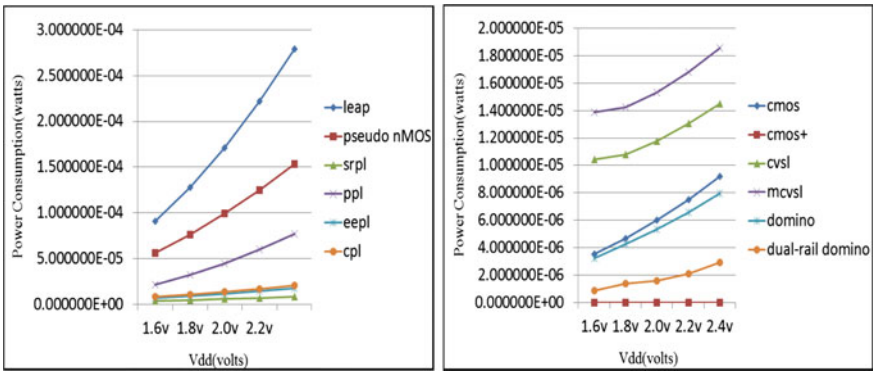

Fig. 10 Power consumption versus Vdd for leap, pseudo NMOS, srpl, ppl, eepl, cpl, cmos, cmos+, cvsl, mcvsl, domino, dual-rail domino based multiplexer circuits

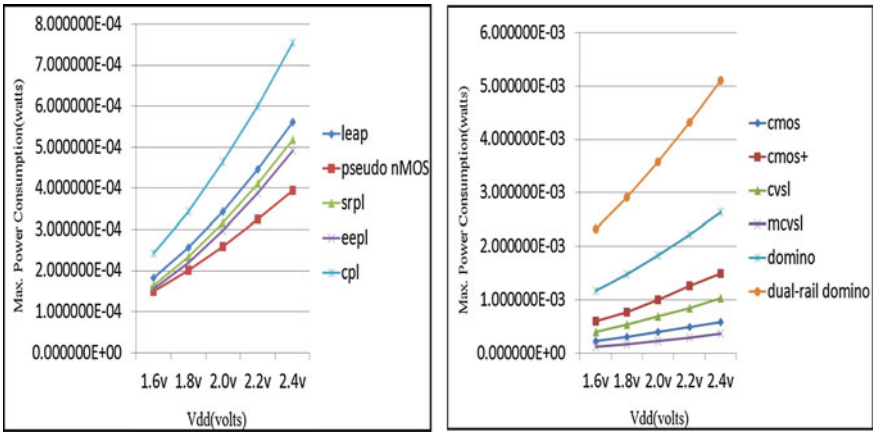

Fig. 11 Maximum power consumption versus Vdd for leap, pseudo NMOS, srpl, eepl, cpl, cmos, cmos+, cvsl, mcvsl, domino, dual-rail domino based multiplexer circuits

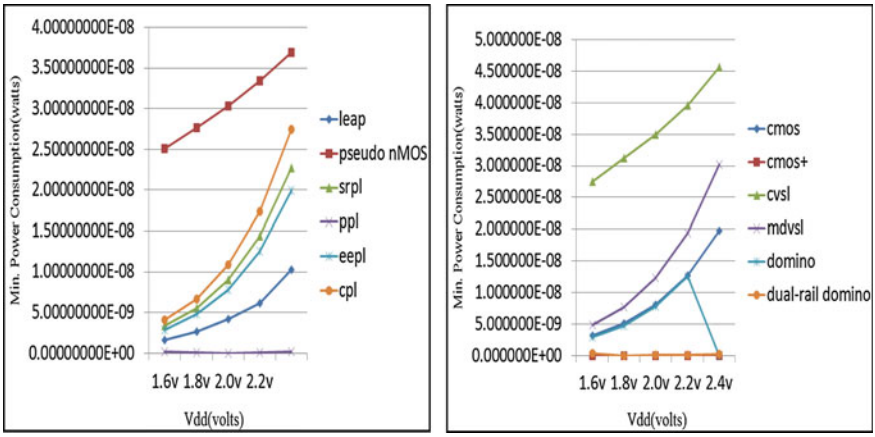

Fig. 12 Minimum power consumption versus Vdd for leap, pseudo NMOS, srpl, ppl, eepl, cpl, cmos, cmos+, cvsl, mcvsl, domino, dual-rail domino based multiplexer circuits

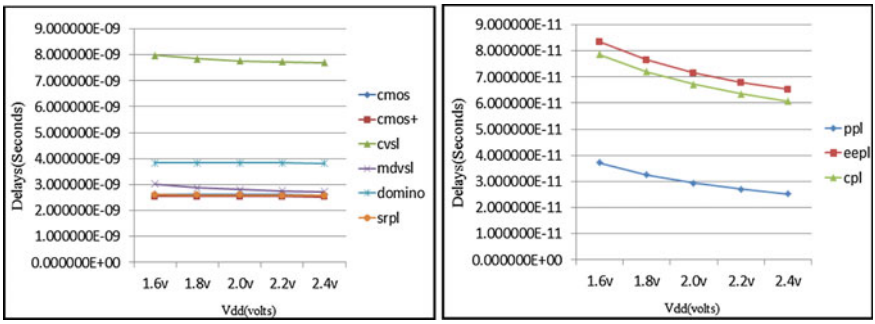

Fig. 13 Delay versus Vdd for cmos, cmos+, cvsl, mcvsl, domino, srpl, ppl, eepl, cpl based multiplexer circuits

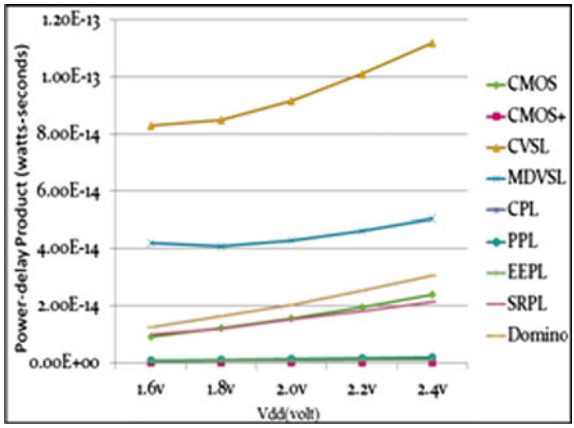

Fig. 14 Power-delay product versus Vdd for cmos, cmos+, cvsl, mcvsl, cpl, ppl, eepl, srpl, domino based multiplexer circuits

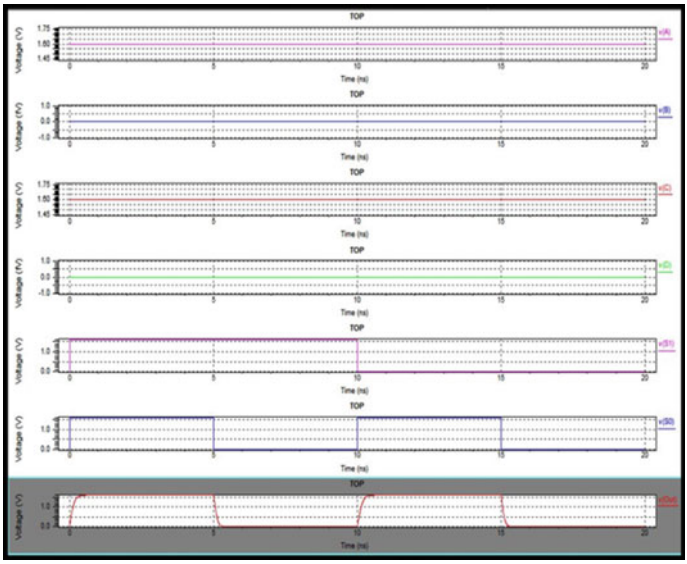

Fig. 15 Simulation result for input signal v(A), v(B), v(C), v(D), v(S1), v(S0) and output signal v(Out) for 4:1 multiplexer based circuits using static signals

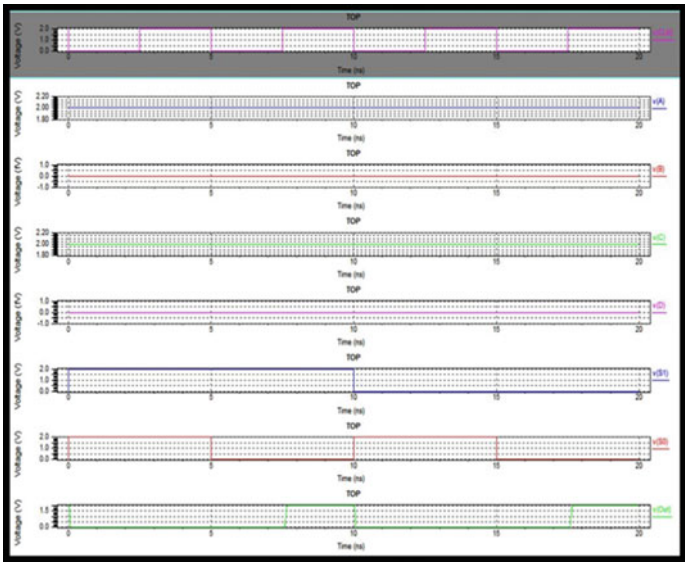

Fig. 16 Simulation result for input signal v(CLK), v(A), v(B), v(C), v(D), v(S1), v(S0) and output signal v(Out) for 4:1 multiplexer based circuits using dynamic signals

Table 1 Power delay product (Watt-Sec) comparison of different 4:1 multiplexer circuits

Voltage applied (V)	Power delay product (W-s)								
	CMOS	CMOS+	CVSL	MCVSL	CPL	PPL	EEPL	SRPL	Domino
1.6	9.25062E−15	6.95442E−18	8.30278E−14	4.18711E−14	6.41908E−16	7.88522E−16	5.88807E−16	9.93263E−15	1.24159E−14
1.8	1.22167E−14	7.55963E−18	8.47726E−14	4.10079E−14	7.70903E−16	1.04411E−15	7.04684E−16	1.2516E−14	1.64033E−14
2.0	1.56345E−14	6.62833E−18	9.1537E−14	4.29699E−14	9.15227E−16	1.32424E−15	8.36842E−16	1.52801E−14	2.0443E−14
2.2	1.95271E−14	7.14547E−18	1.00817E−13	4.62746E−14	1.07565E−15	1.62442E−15	9.85979E−16	1.82457E−14	2.51653E−14
2.4	2.39206E−14	1.0393E−17	1.11641E−13	5.04432E−14	1.25332E−15	1.94936E−15	1.15208E−15	2.14337E−14	3.05314E−14

5 Conclusion

In this paper, design, simulation and analysis of 4:1 multiplexer circuit using CMOS, CVSL, PTL and dynamic logic styles has been done on BSIM 3V3 90 nm PTM technology on Tanner EDA tool. On the basis of comparison of the circuit performance w.r.t. power, delay and power-delay product, Transmission gate (CMOS+) implementation of 4:1 multiplexer was found to be the most efficient logic style at 90 nm CMOS technology within the supply voltage range of 1.6–2.4 V. Pass transistor logic styles, particularly CPL, PPL and EEPL give better performance as compared to CMOS as far as the speed of operation is concerned. Other logic styles such as SRPL and Domino logic perform nearly as good as CMOS in terms of power, delay and power-delay product. But, due to weak output driving capability and less isolation, both SRPL and PPL are less suited while designing circuits with cascaded stages. Modified CVSL shows a slight improvement over existing CVSL w.r.t. delay. However, in case of CMOS, correct gate functionality is independent of transistor sizing and voltage scaling (ratioless logic). Its robustness and ease of use makes it a suitable candidate for the implementation of any arbitrary circuit.

References

1. R. Zimmermann, W. Fichtner, Low-power logic styles: Cmos versus pass-transistor logic. IEEE J. Solid-State Circ. **32**(7), 1079–1090 (1997)
2. S.-M. Kang, Y. Leblebici, in *CMOS Digital Integrated Circuits, Analysis and Design*
3. H.E. Weste Neil, D.M. Harris, *CMOS VLSI Design, A circuits and Systems perspective*, 4th edn.
4. Prof. A. Pal, in *Dynamic Power Dissipation* (2012), https://www.youtube.com/watch?v=I99B5bMWVr0&index=20&list=PLB3F0FC99B5D89571. Accessed 23 Nov 2015
5. A. Chaudhry, *Fundamentals of Nanoscaled Field Effect Transistors* (Springer Science, Business Media, New York, 2013). doi:10.1007/978-1-4614-6822-6_2
6. Prof. A. Pal, in *Dynamic Power Dissipation* (2012), https://www.youtube.com/watch?v=Eu9MLCekmwU&list=PLB3F0FC99B5D89571&index=12. Accessed 23 Nov 2015