Chapter 9
Direct Sequence Spread Spectrum (DSSS) Baseband Transmitter

9.1 Introduction

As today's mixed signal chips often require both digital and analog system components on the same substrate, an interesting area of application for silicon nanowire technology is to build a Direct Sequence Spread Spectrum (DSSS) baseband transmitter. A basic baseband transmitter contains an 8-Phase Shift Keying (8-PSK) modulator, a fourth order PN generator, a binary bit mapper, and two bit multipliers. This chapter uses the BSIMSOI models of NMOS and PMOS SNTs developed in Chapter 3 to simulate all transmitter circuits and shows the design and analysis of a typical DSSS baseband transmitter. All electrical data and the transmitter layout are included in this chapter.

9.2 Brief Description of Transistor Design and Modeling

Both NMOS and PMOS transistors are enhancement type with uniform, undoped silicon bodies and metal gates constructed perpendicular to the SOI substrate as discussed earlier in Chapter 1. Device simulations are performed with Silvaco's 3-dimensional ATLAS device simulator with a 1 V power supply voltage.

The optimal SNT body dimensions of 2 nm radius and 10 nm channel length are determined according to the minimum intrinsic transient times and minimum static and dynamic power dissipations for each NMOS and PMOS transistor discussed in Chapter 3. The BSIMSOI device models also generated in Chapter 3 are used for all the circuit simulations in this chapter.

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DOI 10.1007/978-3-319-27177-4_9

9.3 DSSS Baseband Transmitter

The Direct Sequence Spread Spectrum (DSSS) transmitter is implemented according to the schematic in Fig. 9.1. In this figure, the baseband portion of the transmitter is composed of four blocks: an 8-Phase Shift Keying (8-PSK) modulator, a PN generator, a binary mapper and two bit multipliers.

9.3.1 Overall Operation of the Transmitter

Figure 9.2 illustrates how the symbol (010) is processed through DSSS baseband transmitter using CommSim communications simulator. The modulator and PN generator clocks are also included in the simulation results to show the data processing sequence that ends with an analog output.

When a valid 3-bit serial input, (010), is fed to the input of the 8-PSK modulator, the modulator generates +0.707 In-phase (I) and −0.707 Quadrature (Q) components of the symbol (010) according to the unitary constellation map in Fig. 9.1. Once generated, the component values are held constant for three modulator clock periods while the next symbol is fed to the modulator. The PN generator produces a repeating 15-bit (000100110101111) chip sequence at the Cpn node with a frequency five times faster than the modulator clock frequency and each chip in the sequence is multiplied by the I and Q components of the symbol to produce the frequency spread of MI and MQ values as shown in Fig. 9.2.

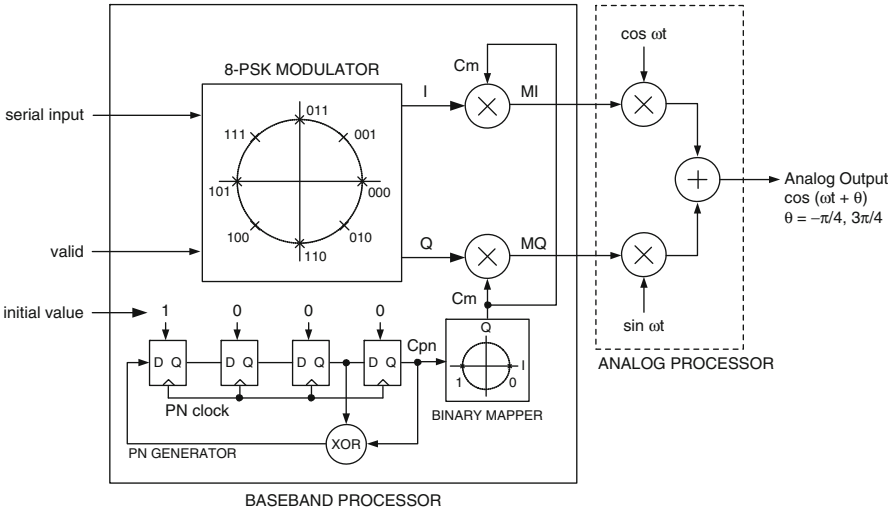

Fig. 9.1 DSSS baseband transmitter top level architecture

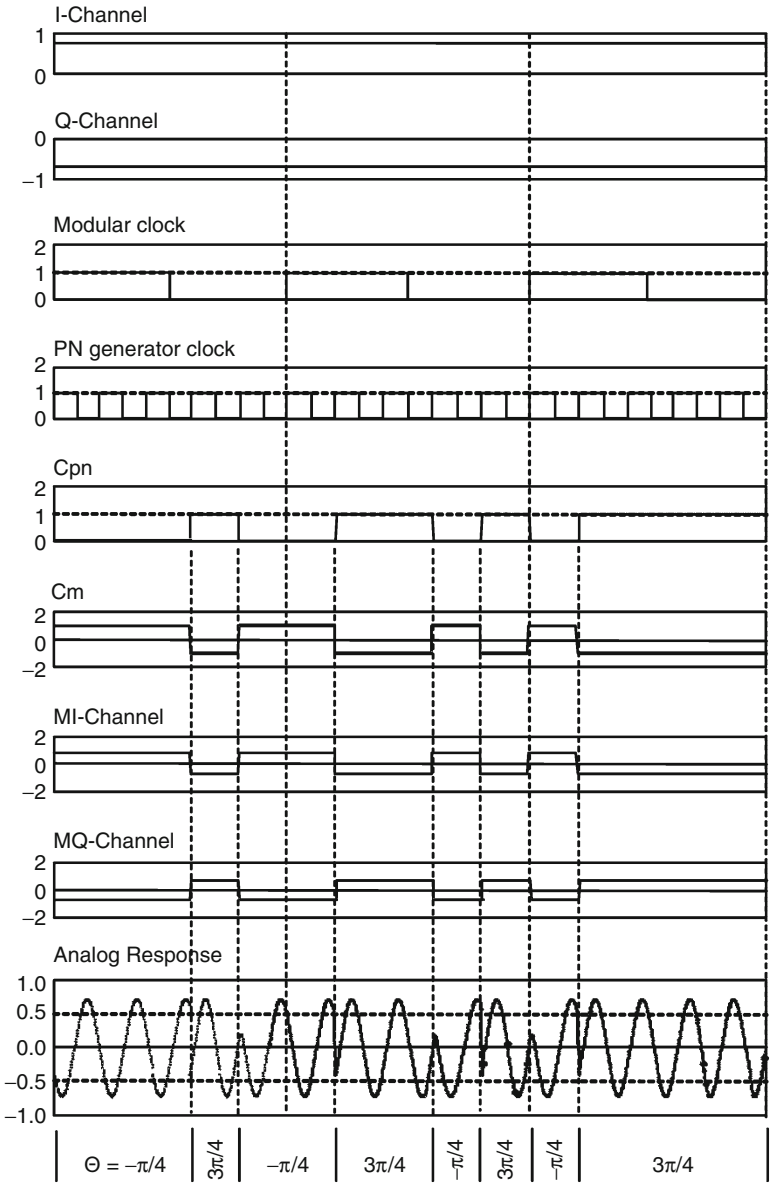

Fig. 9.2 CommSim symbol processing in the DSSS transmitter

The initial values of MI = +0.707 and MQ = −0.707 in this figure correspond to a phase shift of $-\pi/4$ according to the constellation circle. Therefore, a sine wave with a phase shift of $-\pi/4$ is generated during the first three chip periods. Then in the fourth chip, MI and MQ values change to −0.707 and +0.707, which causes the phase of the analog response to shift to $3\pi/4$ and results in a discontinuity as shown

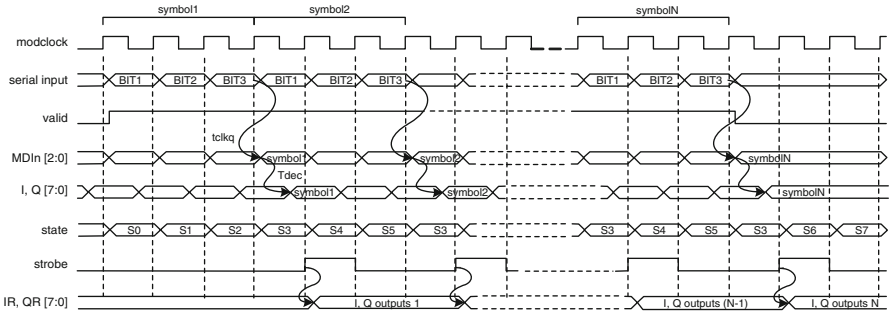

Fig. 9.3 Modulator timing diagram

in Fig. 9.2. The rest of the chip sequence reveals phase shifts between $-\pi/4$ and $3\pi/4$ and causes discontinuities in the analog output due to different MI and MQ values during each chip period.

9.3.2 8-PSK Modulator

The 8-PSK modulator generates I and Q components of a symbol as a function of serial input bit stream as shown in Fig. 9.3. The three valid input bits defining the first symbol is fed to the shift register of the modulator in Fig. 9.4. Within the forth clock period, the modulator decoder determines I and Q values of the symbol according to the constellation circle after a decoder delay, Tdec. In order to keep the symbol value constant for the next 3 clock cycles, a strobe clock is generated by the state machine in Fig. 9.5, which produces a high strobe signal during the state S4 as long as serial inputs are valid. When the last set of valid input bits is fed to the modulator, a final strobe signal is generated by the state S6 in order to latch and output the last symbol. While the registered I and Q symbol components, IR [7:0] and IQ [7:0], are held constant for three modulator clock periods for processing, the modulator continues to work in a pipeline fashion and simultaneously receives valid input bits to form the next symbol. In this design, I and Q components are 8-bit signed numbers; negative values are calculated using 2s complement addition.

9.3.3 PN Generator

The frequency-spreading element of the DSSS transmitter is the PN generator which subdivides a symbol into a 15-bit chip sequence according to its order [1]. In this system, a PN generator of the fourth order with four serial flip-flops and an XOR gate in Fig. 9.1 and also in Fig. 9.4 produces a repeating sequence of $2^4 - 1 = 15$ chips at Cpn. This sequence is dependent on the initial value loaded into

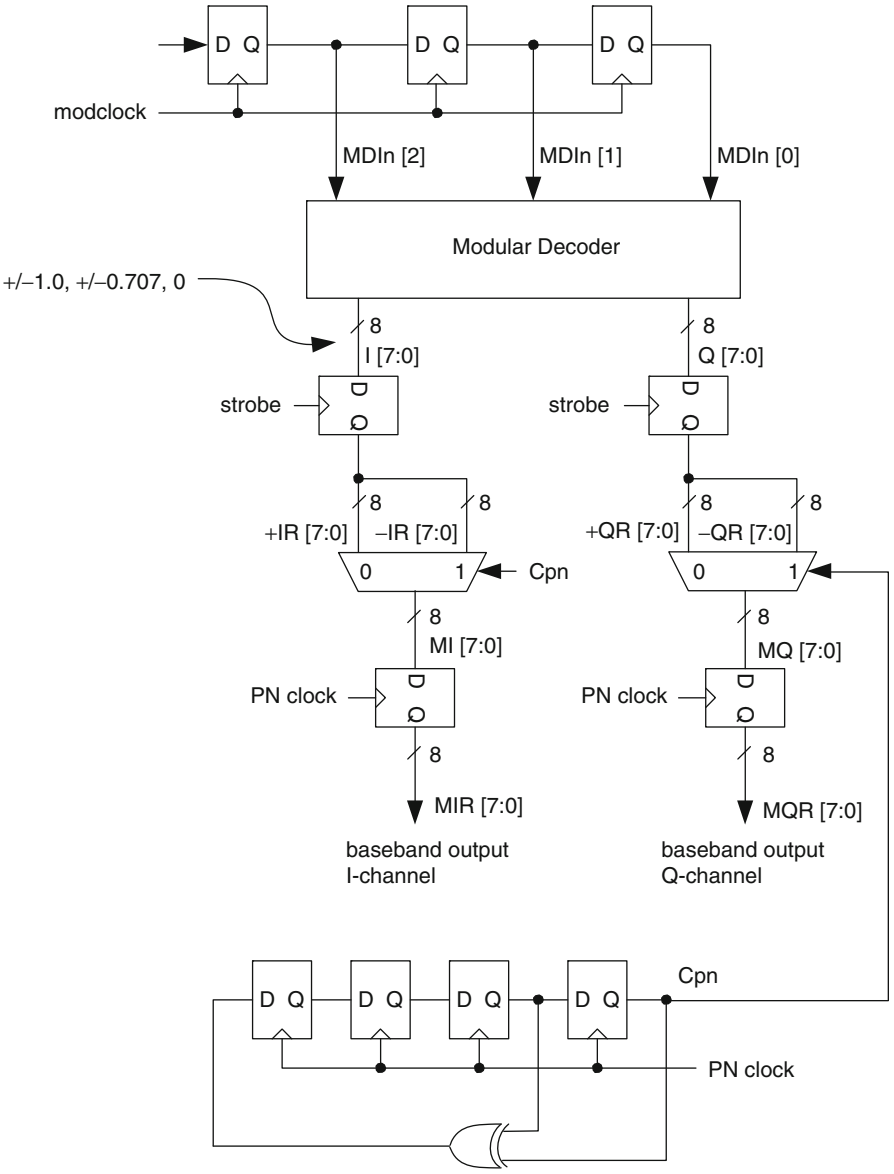

Fig. 9.4 DSSS transmitter functional block diagram

the PN generator where logic 1 is stored at the most significant flip-flop position and logic 0 is stored at the least significant flip-flop position of the PN generator.

The PN clock used in the PN generator is also used to generate the modulator clock as shown in Fig. 9.6. The PN clock frequency is selected to be five times as high as the modulator clock frequency to contain all 15 chips within three modulator clock periods.

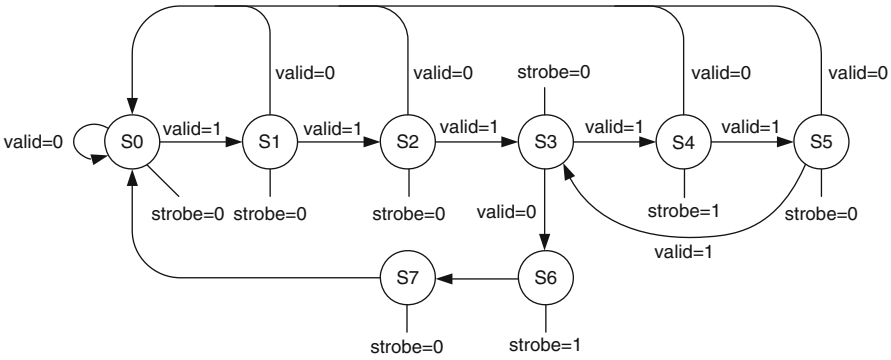

Fig. 9.5 The state machine generating the strobe clock from the modulator clock

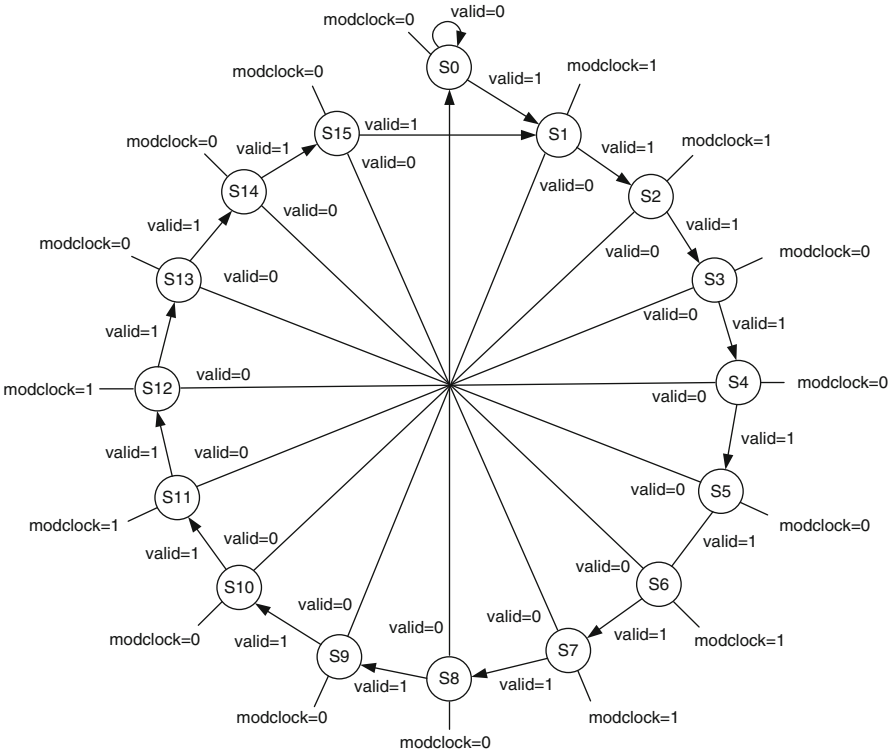

Fig. 9.6 The state machine generating the modulator clock from the PN clock

9.3.4 Binary Mapper and Bit Multipliers

The binary mapper in Fig. 9.1 produces +1 or −1 at the Cm node every time it receives logic 0 or logic 1 from the PN generator, respectively. I and Q channel values from the modulator are then multiplied by each chip at the Cpn node, and 8-bit wide, frequency-spread MI and MQ outputs are produced at MI [7:0] and MQ [7:0] nodes as shown in Fig. 9.4. Registered MI and MQ outputs, MIR [7:0] and MQR [7:0], are subsequently sent to the analog processor.

9.4 Circuit Simulations

9.4.1 Clock Generation Circuits

The Moore-type state machines in Figs. 9.6 and 9.7a are interconnected to show how each clock is generated from a single clock. The modulator clock generator is composed of FB-PN and FF-PN paths and operates with a high frequency clock, pnclockgen, to produce a secondary clock, modclockgen. Similarly, the strobe clock generator is composed of FB-mod and FF-mod paths and operates with modclockgen to produce strobe clock. The delay circuits between pnclockgen and PN clock, and between modclockgen and modclock, simply align all 3 clocks with respect to the original clock, pnclockgen, and eliminate the possibility of any hold time violation in the transmitter. Figure 9.7b shows the alignment of all system clocks within 1 ps.

9.4.2 Maximum Critical Paths

During the circuit analysis, four critical paths have emerged in the baseband transmitter. One of these paths, designated as path A around the feedback loop of the modulator clock generator (FB-PN) in Fig. 9.7a, dominates all the other critical paths B, C, and D shown in Figs. 9.7a, 9.8 and Table 9.1, and ultimately determines the PN clock frequency. Path A consists of two inverters, one 3-input and four 2-input NAND gates all connected in series as shown in Fig. 9.9a. It produces 10.2 ps pnclockgen-Q delay due to a large capacitive load at the PS [0] node and 17.3 ps total gate delay between the PS [0] and NS [3] nodes as shown in Fig. 9.9b. Since the setup time of the flip-flop is 3.5 ps, the total delay between two pnclockgen boundaries becomes $10.2 + 17.3 + 3.5 = 31$ ps as shown in Table 9.1. Adding 10 % RC parasitic delay overhead to this value brings up the PN clock period to be approximately 35 ps. Therefore, the modulator clock period containing

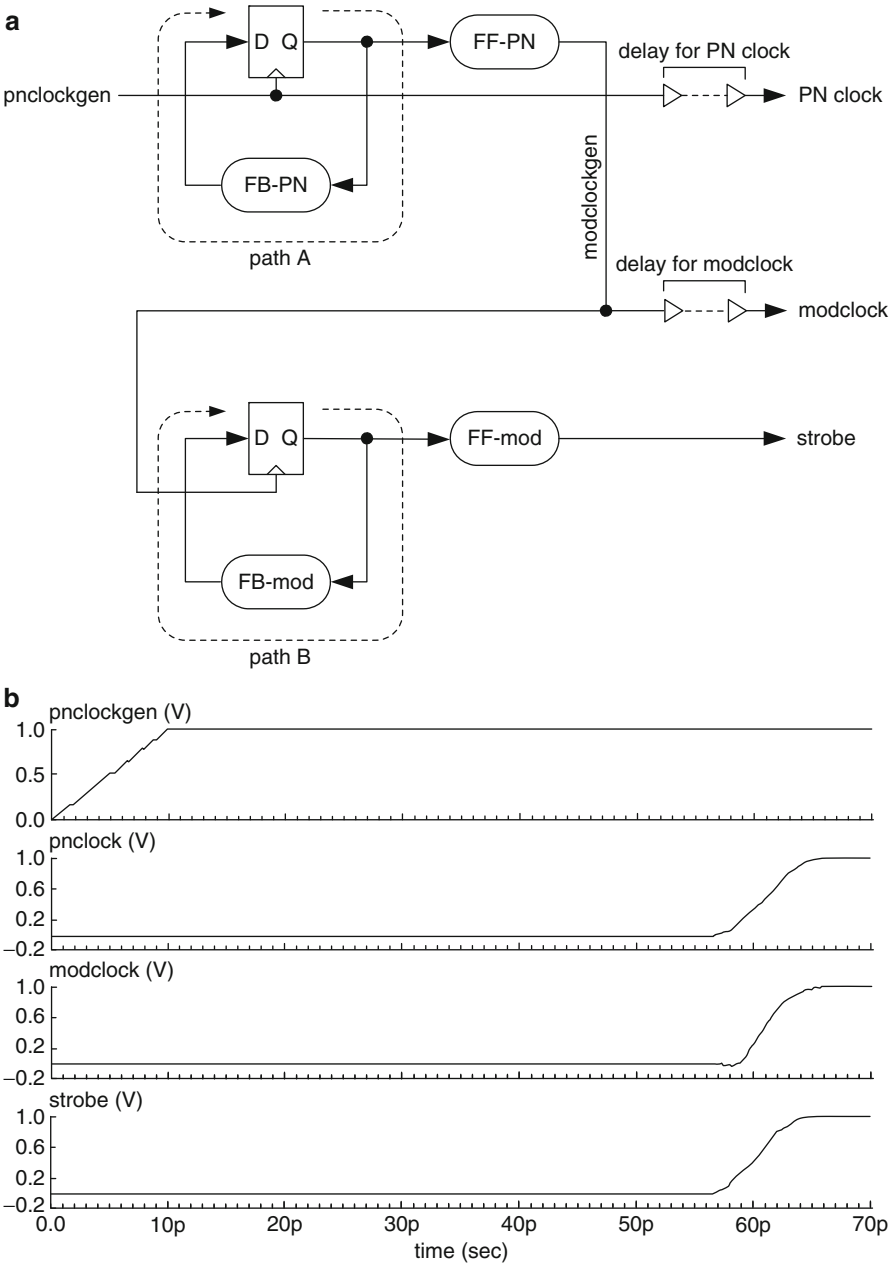

Fig. 9.7 (**a**) Critical paths in the clock generation circuits. (**b**) Generation of PN clock, modclock, and strobe

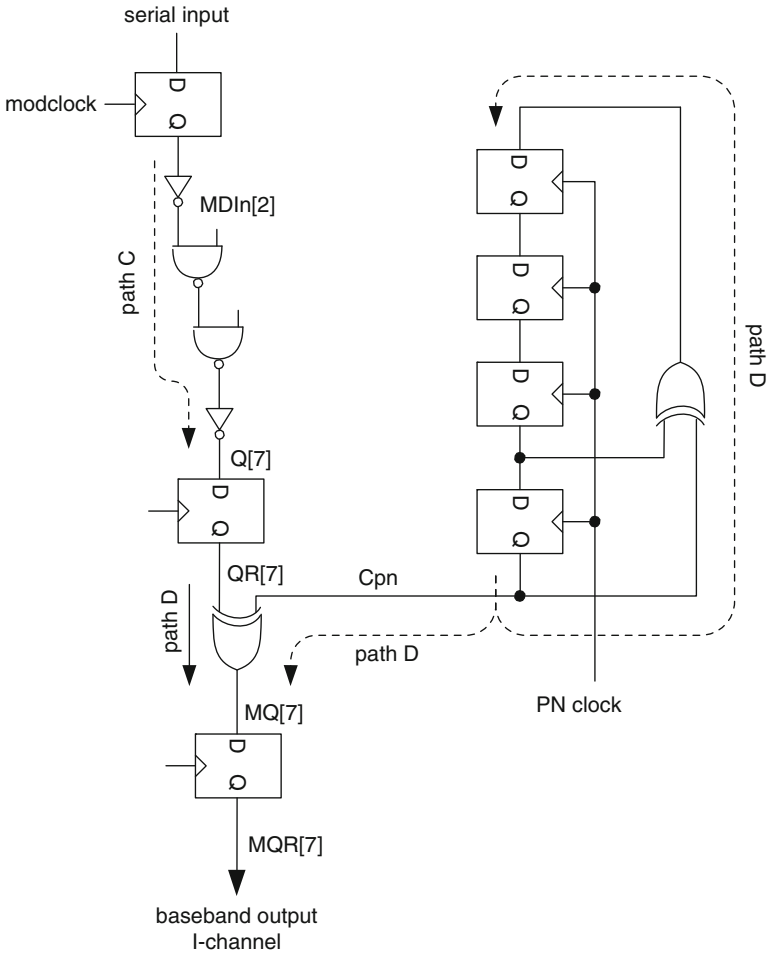

Fig. 9.8 Critical data paths in the modulator, bit mapper, and PN generator

Table 9.1 Critical path properties in DSSS transmitter

Critical	Clk-Q delay	Logic delay (ps)	Setup time (ps)	Total delay (ps)
Path A	10.2	17.3	3.5	31.0
Path B	9.1	14.2	3.5	26.8
Path C	5.8	7.9	3.5	17.2
Path D	5.8	2.2	3.5	11.5

5 chips becomes 175 ps and the strobe period containing all 15 chips or a single symbol becomes 525 ps. This translates approximately 28.6 GChips/s chip rate at the output of the baseband transmitter and makes this design suitable for any high-speed wireless application.

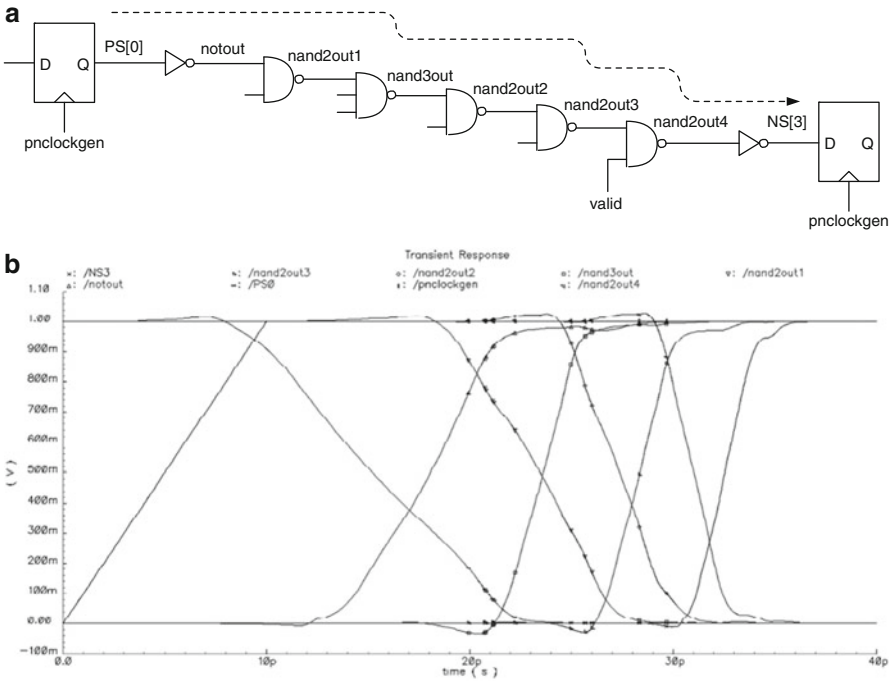

Fig. 9.9 (**a**) Logic string defining the critical path though FB-PN. (**b**) Circuit simulation results at various nodes of the feedback path, FB-PN

9.4.3 Minimum Critical Paths

Minimum critical paths are important in order to prevent hold violations in case of a clock shift. Both the PN generator and the shift register in the modulator have zero-delay paths between two flip-flop boundaries. Since the minimum clock-Q delay of a flip-flop is 4.6 ps for a fan-out of one and its hold time is 0.8 ps, the PN clock can be permitted to shift less than 3.8 ps to avoid hold time violation.

9.4.4 Parasitic RC Extraction

Two critical implementation issues of this design are to determine the layout design rules and the dielectric thickness between two metal layers to reduce the effects of parasitic resistance and capacitance on gate propagation delays. NMOS and PMOS transistors are deliberately built on circular silicon islands of SOI substrate as discussed in Chapter 1 to prevent latch-up and eliminate N-well and P-well junction capacitances.

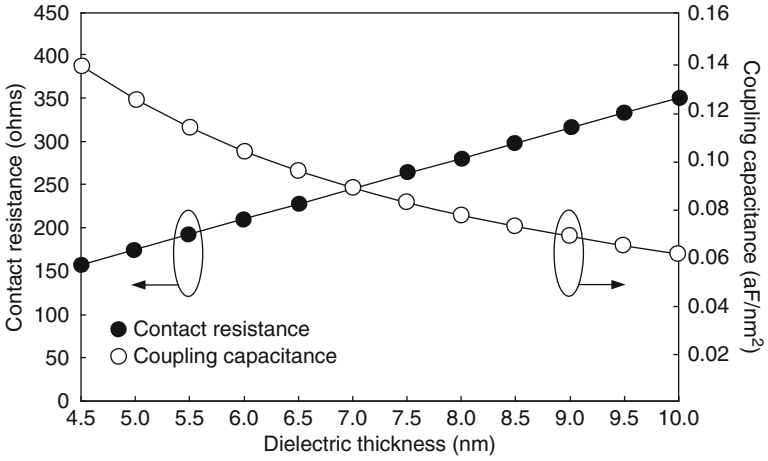

Fig. 9.10 Contact resistance of via openings and inter-metal layer coupling capacitance

Metal wire width for interconnects is kept at 4 nm for all metal layers. Since earlier experimental studies [2, 3] suggest that 10 nm metal thickness is necessary to avoid grain boundary formation and maintain a continuous metallic film, this thickness value is used for transistor gates as well as all metal interconnects. Wire interconnect spacing is assumed to be 4 nm to limit the value of coupling capacitance to 8.6×10^{-2} aF/nm^2 between two adjacent wires (height = 10 nm, width = 4 nm). The variations in contact resistance and coupling capacitance as a function of dielectric thickness are shown in Fig. 9.10.

Determining the value of the dielectric thickness between two metal layers is a trade-off between the coupling capacitance of overlapping interconnects and the contact resistance resulted from a 2×2 nm contact opening. As the dielectric thickness increases, the coupling capacitance between two metal interconnects reduces at the expense of increasing contact resistance. In Fig. 9.10, a compromise is made to select the dielectric layer thickness to be 7 nm such that minimal values of coupling capacitance (0.09 aF/nm^2) and a contact resistance (250 Ω) can be obtained. However, this dielectric thickness resulted in less than 3 fs parasitic delay on maximum critical paths; therefore, its effect is ignored from circuit simulations.

Inter-metal and intra-metal coupling capacitances are computed using Ansoft's capacitance calculator which reveals coupling, fringing, and area components of a single interconnect with respect to neighboring wires. The interconnect wire resistivity is determined by extrapolating the results of an earlier theoretical study [4] for the wire dimensions used in this study.

9.4.5 Power Consumption

The average power consumption of the DSSS baseband transmitter is found to be 198.5 μW at 5.7 GHz modulator clock frequency. Modulator and strobe clock generation circuits consume 93.8 μW while the remaining transmitter datapath including the modulator decoder, the PN generator, the bit mapper, and the two multipliers consumes an average of 104.7 μW. The total transmitter power dissipation changes between 188.1 μW for the symbol (111) and 213.4 μW for the symbol (010) according to the symbol being processed in Fig. 9.11. Each power consumption value in Fig. 9.11 is determined by averaging the time-integrated dynamic current drainage during a symbol period.

While processing symbols, high current spikes have occurred at the positive edge of each modulator clock. One such example is shown in Fig. 9.12 for the highest power dissipating symbol (010). Here, high dynamic power consumption levels tapered off rapidly as the rest of the chips in the modulator clock period are processed. Therefore, one can conclude that high current drainage results from the state change in the modulator shift register and the subsequent switching activity in the modulator decoder. Clock generator circuits are independent of processed symbol and produce constant power consumption.

Figure 9.13 shows chip power consumption for the symbol (010). Power consumption values in this figure are time averages and calculated by integrating dynamic power supply current as a function of time and dividing the result by the chip period. The power dissipation spikes in Fig. 9.12 also manifest themselves in Fig. 9.13 by reaching 300 μW when chips 1, 6, and 11 are processed and the modulator decoder experiences full activity. The rest of the chips consume relatively lower power below 100 μW due to the local activity in the bit multipliers and binary mapper. Figure 9.13 also shows the power consumption in the clock generator circuits as a function of chip number. The power dissipation changes between 43.9 and 133.7 μW depending on the active feedback and feed-forward paths in the modclock and strobe state machines.

Table 9.2 compares the chip rate, power dissipation, and the technology figures of this study with recent baseband transceivers designs [5–8]. Silicon nanowire transistors

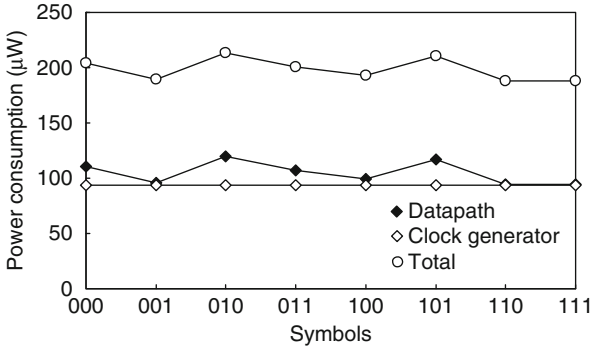

Fig. 9.11 Power consumption in the DSSS baseband transmitter for different symbols

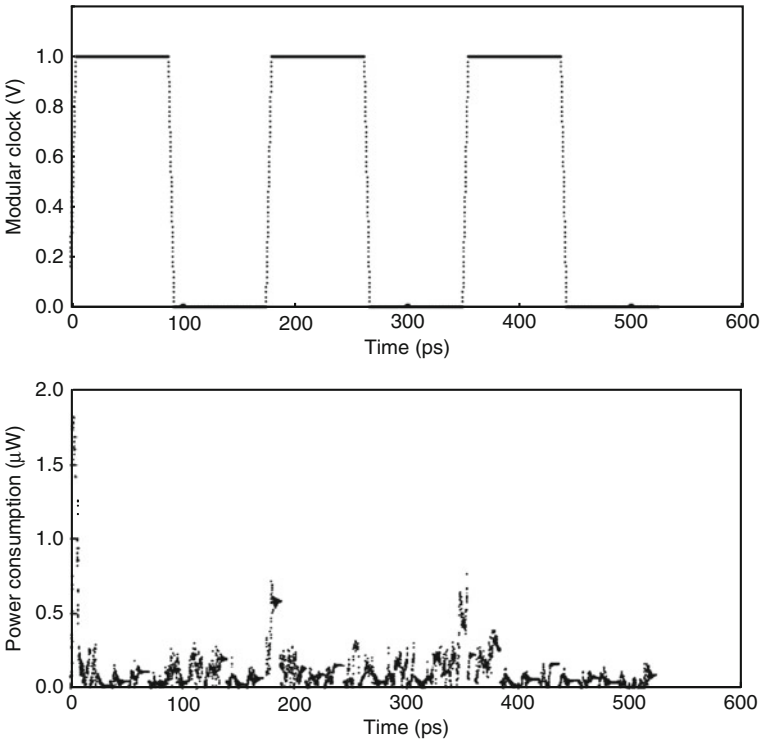

Fig. 9.12 Dynamic power consumption while processing symbol (010)

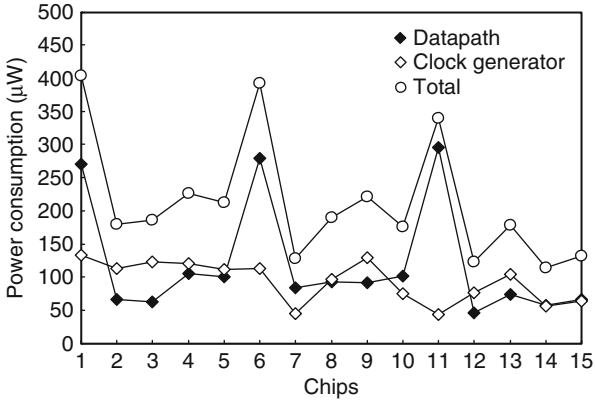

Fig. 9.13 Power consumption during chip processing for symbol (010)

with 10 nm channel length and 2 nm radius deliver almost 30 times faster chip rate compared to the study in [8] even though the device properties of nanowire transistors were optimized for minimal power consumption. It is also interesting to note that Koyama et al. [8] report almost 50 times faster chip rate compared to the study in [7] even though the transceiver power dissipations in each study stay the same.

Table 9.2 Comparative study of this work with earlier designs

References	Chip rate	Power consumption	Technology
[5]	22 MChips/sec	390 mW[a]/850 mW[a]	0.8 µm/5 V supply
[6]	22 MChips/sec	1.2 W[b]	0.6 µm/3.3 V supply
[7]	22 MChips/sec	70 mW[a]/184 mW[a]	0.18 µm/1.8 V supply
[8]	1 GChips/sec	181 mW[b]	0.13 µm/1.2 V supply
This study	28.6 GChips/sec	198.5 mW[a]	10 nm/1 V supply

[a]Power dissipation in the transmitter
[b]Power dissipation in the transceiver

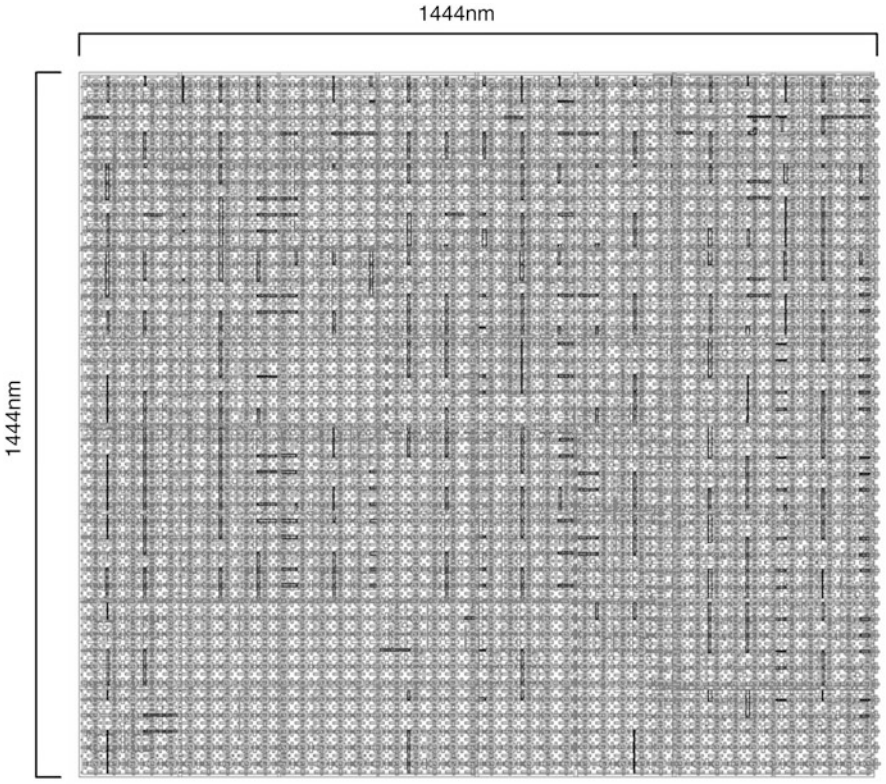

Fig. 9.14 DSSS baseband transmitter layout

9.4.6 Layout

Layout methodology used in this design is fabric-like, in the form of a crossbar configuration, as discussed in earlier chapters. In a crossbar structure, NMOS and PMOS transistors are placed in an alternate pattern that forces every NMOS transistor to have 4 neighboring PMOS transistors and vice versa.

With this fabric matrix configuration, a place-route CAD tool can be used to convert the entire circuit schematic into layout without any human interface. No custom design or ASIC approach is needed to create or characterize primitive or mega cells. Continuous lines are achieved by connecting pre-laid out metal interconnects with short metal strips. Figure 9.14 illustrates the result of fabric layout methodology for implementing the DSSS baseband transmitter. Over 90 % transistor utilization factor was achieved out of 1600 transistors used in this layout. The layout dimensions are 1444 nm by 1444 nm.

9.5 Summary

This chapter studies the possibility of using the SNT technology in a simple DSSS baseband transmitter and examines the results of the transmitter performance and power consumption. The transmitter contains four functional units: an 8-PSK modulator, a fourth order PN generator, a binary bit mapper and two bit multipliers. It generates In-phase and Quadrature outputs. The circuit simulations use the BSIMSOI nanowire transistor models developed in Chapter 3 and reveal a 31 ps worst-case delay between the two flip-flop boundaries with 28.6 GHz PN clock. Parasitic RC extractions add a maximum 3 fs delay on the designated critical paths, causing no setup time violations, and therefore ignored in the generation of the chip and modulator clocks. The resultant chip rate of 28.6 Gbits/s and the average power of 198.5 μW at a 1.9 GHz symbol frequency make this transmitter suitable for any handheld application. The layout was organized in a fabric-like fashion where NMOS and PMOS transistors are placed alternatively on a SOI substrate. The entire baseband transmitter layout occupies approximately 2.1 μm^2 of chip area.

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