Chapter 4
High-Speed Analog Applications

4.1 Introduction

In Chapter 3, we obtained accurate BSIMSOI SPICE models for NMOS and PMOS silicon nanowire transistors to replicate the simulated device I–V characteristics. We also calculated voltage-dependent intrinsic gate oxide capacitance, parasitic device resistors and capacitors, including the high frequency effective gate resistance in order to generate accurate extrinsic circuit models for SNTs. From these extrinsic models, we reproduced the realistic input and output I–V characteristics, transconductance, and output resistance curves as a function of biasing conditions, S-parameters, power gains, f_{max}, and f_T. This chapter presents the first application of silicon nanowire technology on analog circuits. Various small and large-signal analog circuits such as a single-stage CMOS amplifier, a differential pair amplifier, and a two-stage operational amplifier were designed and simulated using the BSIMSOI SPICE models of SNTs.

4.2 Brief Description of Transistor Design and Modeling

The optimal SNT body dimensions of 2 nm radius and 10 nm channel length are determined according to the minimum intrinsic transient times and minimum static and dynamic power dissipations for each NMOS and PMOS transistor discussed in Chapter 3. The BSIMSOI device models are based on these particular device dimensions and they are used for all the circuit simulations in this chapter.

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4.3 Single-Stage CMOS SNT Amplifier

4.3.1 The CMOS Amplifier Design

The layout of an SNT CMOS amplifier which can be used as a large-signal inverter or a small-signal amplifier is shown in Fig. 4.1a. The biasing point of transistors is decided by the voltage level of the input signal. For 1 V supply voltage, both transistors operate in active region when the input voltage changes between 0.4 V and 0.6 V. Two PMOS transistors, Qp1 and Qp2, are used in parallel to ensure their overall ON current is almost equal to that of a single NMOS transistor, Qn. The area of the SNT amplifier is 70×144 nm. The gate and source contacts for each transistor in this layout are doubled to reduce ohmic losses at these terminals which, otherwise, act as a degenerative factor to decrease the voltage gain of the amplifier.

The low frequency small-signal model of the amplifier, when both transistors operate in active region, is shown in Fig. 4.1b. In this figure, R_d represents the cumulative drain resistance and R_s is the cumulative source resistance given by

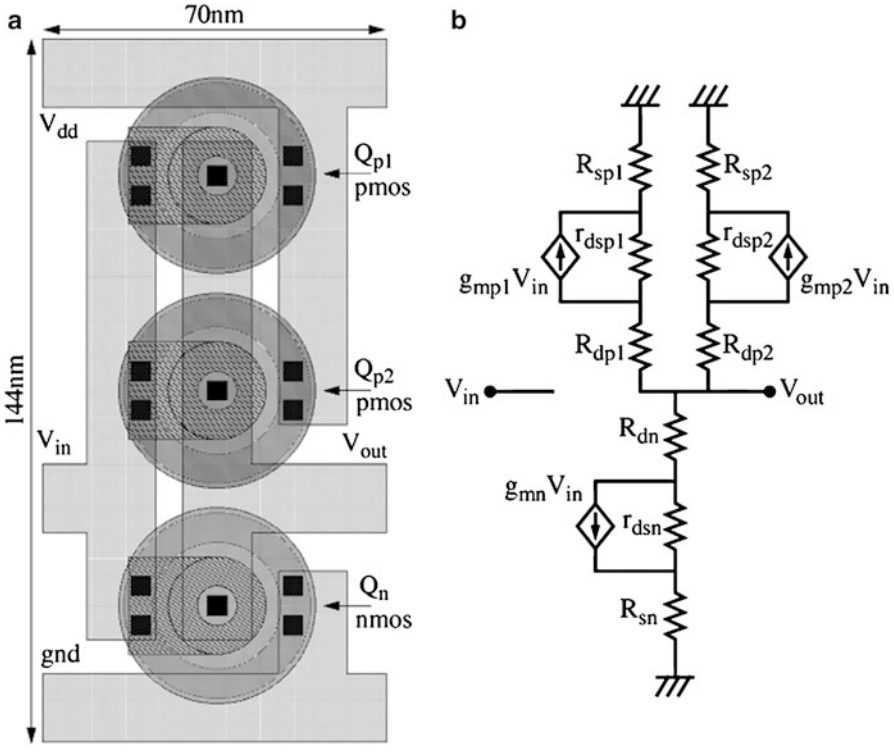

Fig. 4.1 The SNT CMOS amplifier (**a**) layout and (**b**) low frequency small-signal model

$R_{sn} = R_{sx} + R_{sy} + R_{nw}$ for the NMOS SNT and $R_{sp} = R_{sx} + R_{sy} + R_{pw}$ for the PMOS SNT. The actual values are given in Chapter 3.

According to Fig. 4.1b, the low frequency small-signal gain of the CMOS amplifier is given by Eq. 4.1.

$$A_{v0} = -\left[\frac{g_{mn}r_{dsn}}{R_n} + \frac{g_{mp1}r_{dsp1}}{R_{p1}} + \frac{g_{mp2}r_{dsp2}}{R_{p2}}\right]\left(R_n /\!/ R_{p1} /\!/ R_{p2}\right) \tag{4.1}$$

where

$$R_n = r_{dsn} + R_{sn} + R_{dn} \approx r_{dsn} \tag{4.2}$$

and

$$R_{p1} = r_{dsp1} + R_{sp1} + R_{dp1} \approx r_{dsp1} \tag{4.3}$$

and

$$R_{p2} = r_{dsp2} + R_{sp2} + R_{dp2} \approx r_{dsp2} \tag{4.4}$$

Therefore, Eq. 4.1 can be rewritten as

$$A_{v0} \approx -\left[g_{mn} + g_{mp1} + g_{mp2}\right]\left(r_{dsn} /\!/ r_{dsp1} /\!/ r_{dsp2}\right) \tag{4.5}$$

Here, A_{V0} is approximately equal to -6.9 with $g_{mn} = 14$ μA/V and $g_{mp1} = g_{mp2} = 8$ μA/V, $r_{dsn} = 400$ kΩ and $r_{dsp1} = r_{dsp2} = 1.1$ MΩ at $V_{ds} = 0.5$ V and $V_{gs} = 0.5$ V. The simplified low frequency voltage gain of the SNT CMOS amplifier becomes similar to the MOSFET amplifier gain when $R_s \ll 1/g_m \ll r_{ds}$ is satisfied.

4.3.2 The Characteristics of the CMOS Amplifier

The frequency bandwidth and linearity are the two important figures of merit for an amplifier. When biased at $V_{gs} = 0.5$ V, the maximum gain of the CMOS amplifier becomes $20 \times \log(6.5) = 17$ dB and the phase becomes 180° with a unity voltage gain cutoff frequency of 20 THz at a phase angle of 60° as shown in Fig. 4.2. The 3 dB frequency bandwidth of the amplifier is approximately 500 GHz and the power dissipation becomes 1.64 μW. The output spectrum of the amplifier in response to a two-tone test with 10 GHz spacing is shown in Fig. 4.3. The 2nd and 3rd harmonic distortions, HD2 and HD3 tones, of the amplifier are 10 dB and 20 dB below the

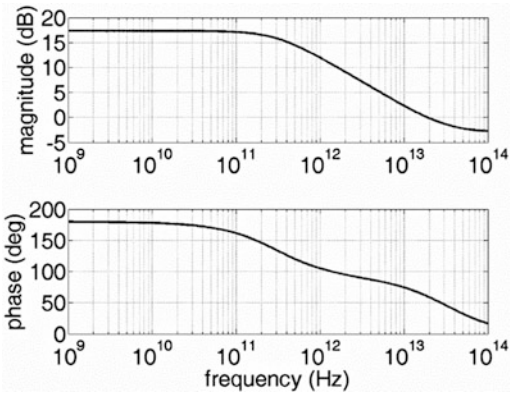

Fig. 4.2 The amplifier small-signal frequency response

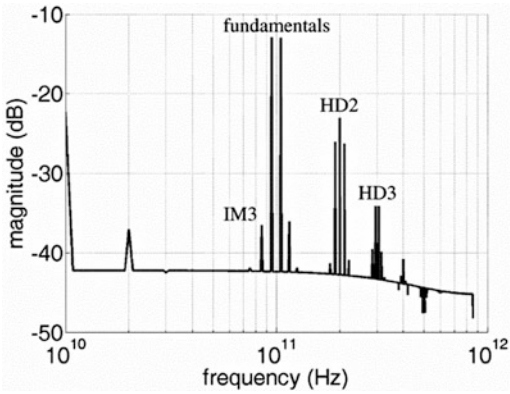

Fig. 4.3 The amplifier two-tone output spectrum

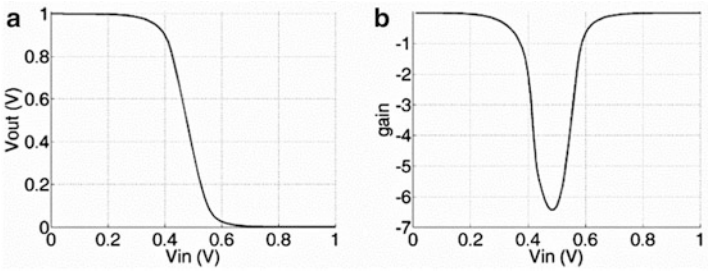

Fig. 4.4 The amplifier large-signal (**a**) transfer characteristic and (**b**) DC gain

fundamental tones, respectively. The third order intermodulation distortions, IM3 tones, are 24 dB below the fundamentals for 10 mV input signal levels.

The transfer function of the SNT CMOS amplifier including all parasitic resistors is given in Fig. 4.4a. Similarly, the slope of the transfer characteristics representing the DC voltage gain is shown in Fig. 4.4b. The large-signal transient

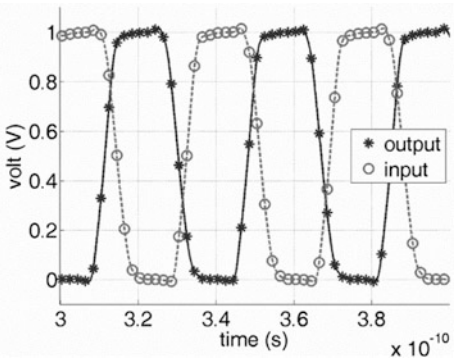

Fig. 4.5 The amplifier large-signal transient response

Table 4.1 Characteristics of SNTs with BSIMSOI modeling

Parameters	NMOS	PMOS
I_{off} ($V_{GS} = 0$ V and $V_{DS} = 1$ V)	540 pA	80 pA
I_{ds} ($V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V)	2 μA	0.7 μA
g_m ($V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V)	14 μA/V	8 μA/V
r_{ds} ($V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V)	400 kΩ	1.1 MΩ
f_τ	36 THz	25 THz
F_{max}	120 THz	100 THz
CMOS amplifier area	70×14 nm	
Amplifier power dissipations	1.64 μW	
3 dB bandwidth	500 GHz	
Third order intermodulation distortions	−24 dBm for $f_2 - f_1 = 10$ GHz	
Small-signal DC gain	−6.5	
Large-signal delay	2.2 ps	
Large-single rise time	5.4 ps	
Large-single fall time	4.7 ps	
Rail-to-swing	1 V	

response of this amplifier acting as an inverter is shown in Fig. 4.5. Seven inverters are cascaded in a closed loop feedback configuration to be able to obtain the input and the output waveforms of a single-stage amplifier in this figure. The initial condition of the circuit ensures self-oscillation with an oscillation frequency of 30 GHz. The gate delay of each SNT inverter is 2.2 ps; the rise and fall times are 5.4 ps and 4.7 ps, respectively. These values are obtained by considering all parasitic values of the layout.

The summary of the SNT amplifier characteristics is listed in Table 4.1.

4.4 Differential SNT Amplifier

4.4.1 A Single-Stage Differential Amplifier Design

Operational amplifiers are one of the most useful building blocks in analog integrated circuits. Since differential amplifiers occupy the input stage of any operational amplifier, their circuit characteristics and performance become crucial in an operational amplifier design. A typical differential amplifier with a current mirror circuit and its layout is shown in Fig. 4.6. The low frequency small-signal model of the amplifier is shown in Fig. 4.7.

In Fig. 4.7, the resistor R_3 is given by

$$R_3 = R_{s3} + \left(r_{ds3} /\!/ \frac{1}{g_{m3}} \right) \tag{4.6}$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximated by

$$\frac{V_{out}}{V_{in}} \approx g_{m2} r_{ds2} \tag{4.7}$$

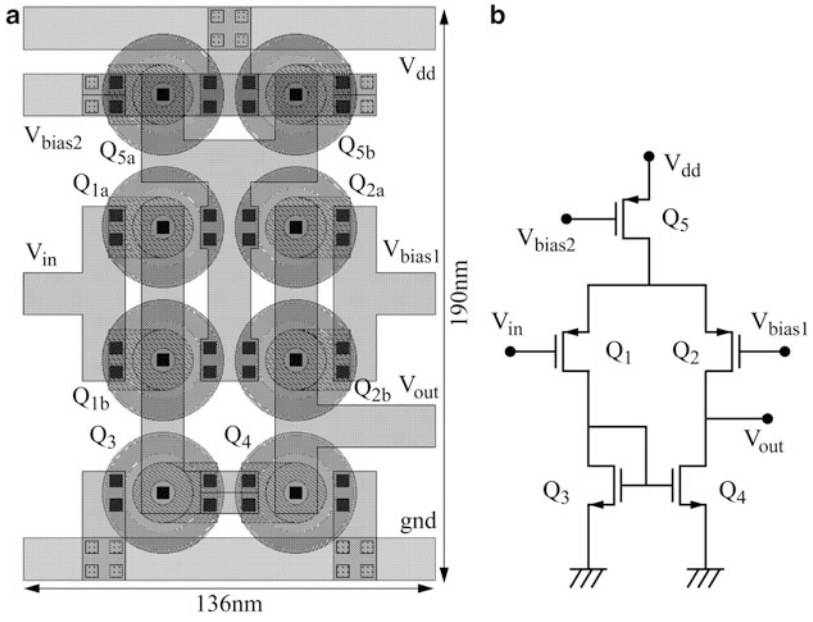

Fig. 4.6 Differential SNT amplifier (**a**) layout and (**b**) schematic

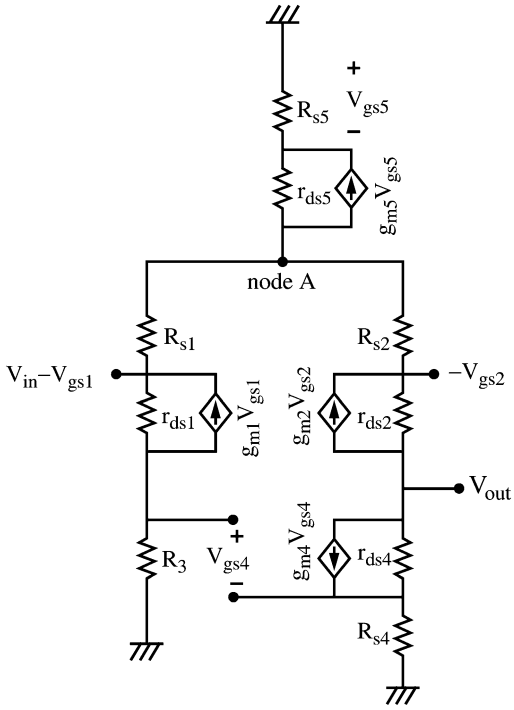

Fig. 4.7 Low frequency small-signal model

For $G_s \gg g_m \gg g_{ds}$, the output resistance is approximately given by

$$R_{out} \approx \left[r_{ds2} \left(1 + \frac{g_{m2}}{g_{m1}} \right) \right] // r_{ds4} \tag{4.8}$$

The layout of the differential pair amplifier in Fig. 4.6a is implemented by three metallization layers serving as local interconnects. All interconnect parasitic components are extracted and added to amplifier netlist for post-layout circuit simulations. The PMOS transistors at the inputs of the differential amplifier are implemented by a parallel combination of two PMOS SNTs to ensure a large transconductance. The width of the metal interconnects is selected to be 14 nm to reduce their resistivity and four vias are used to connect metal 2 and metal 3 layers to minimize the ohmic loss. Each 4 nm by 4 nm via offers 400 Ω resistance. A 14 nm by 14 nm overlap capacitance between metal 1 and metal 2 layers is 0.2 aF. The layout area of the differential amplifier occupies an area of 136 nm by 190 nm.

4.4.2 The Characteristics of the Differential Amplifier

The frequency response of the SNT differential pair amplifier is shown in Fig. 4.8. The amplifier provides a gain of 16 with the first pole located at 100 GHz and the second pole located at 100 THz. To attain high accuracy in the transfer functions of

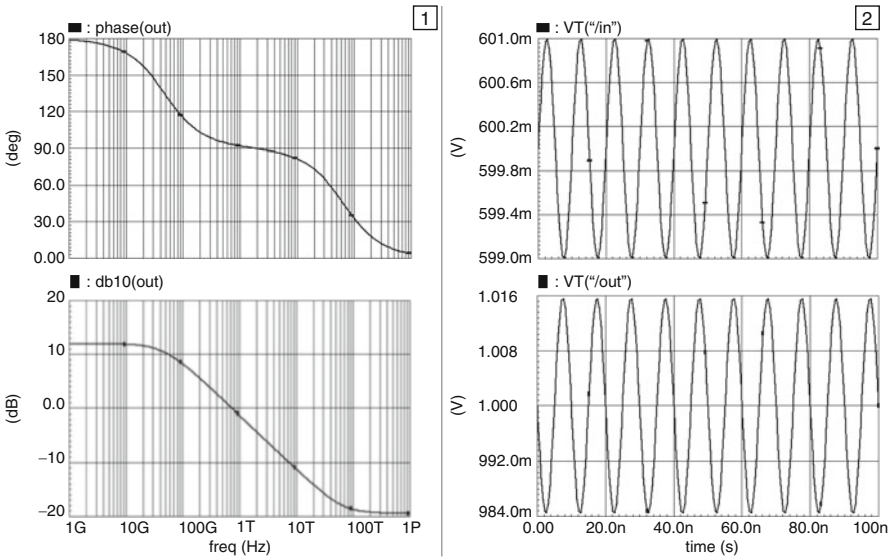

Fig. 4.8 Amplifier small-signal frequency response

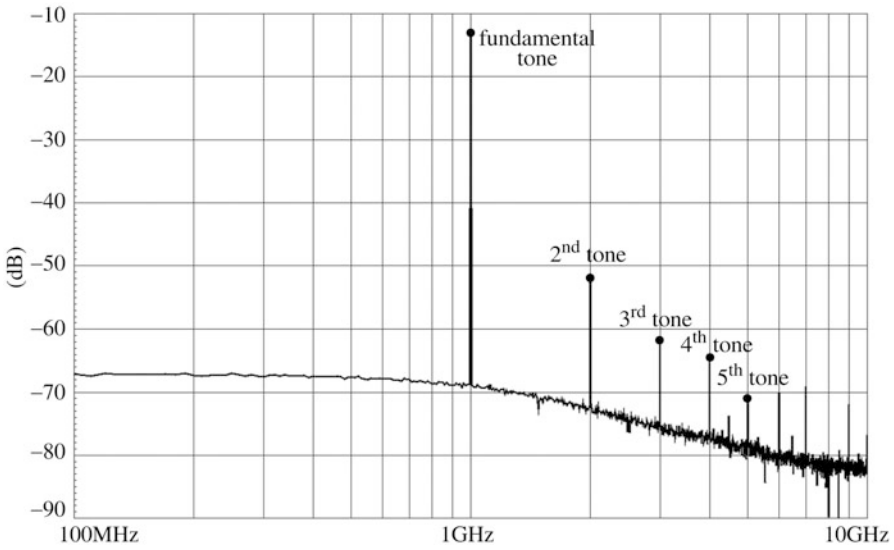

Fig. 4.9 Amplifier output spectrum

various analog circuits such as switch capacitor filters and amplifiers, it may be necessary to cascade multiple such amplifier stages in nested Miller architectures to be able to achieve a voltage gain higher than 1000.

The spectrum of the output waveform of the amplifier is shown in Fig. 4.9. The amplifier produces good linearity with a total harmonic distortion of about 3 % for

Table 4.2 Characteristics of the SNT differential pair amplifier

Parameters	NMOS	PMOS
I_{off} ($V_{GS} = 0$ V and $V_{DS} = 1$ V)	540 pA	80 pA
I_{ds} ($V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V)	2 μA	0.7 μA
g_m ($V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V)	14 μA/V	8 μA/V
R_{ds} ($V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V)	400 kΩ	1.1 MΩ
f_τ	36 THz	25 THz
F_{max}	120 THz	100 THz
Supply voltage	1.8 V	
Maximum output linear signal swing	0.5 V	
Input DC voltage level	0.6 V	
Voltage gain (at 1 GHz)	16	
Phase margin	>90°	
Unity voltage gain cutoff frequency	5.1 THz	
Third order intermodulation distortion (10 mV two-tone signals with 1 GHz spacing)	−24 dBm	
Second order harmonic distortion	−40 dBm	
Third order harmonic distortion	−52 dBm	
Total harmonic distortion	3 %	
Load capacitor	20 aF	
Power dissipation	5 μW	
Area	136 × 190 nm	

±233 mV output swing. Such a high linearity is due to the source resistance, R_s, acting as the degeneration resistance and thereby minimizing the harmonic distortion of the differential PMOS SNTs at the input.

The summary of the single-stage SNT amplifier is listed in Table 4.2.

4.5 Multi-stage SNT Operational Amplifier

4.5.1 A Two-Stage Operational Amplifier Design

Intrinsic BSIMSOI transistor models are obtained after matching the input and output I–V characteristics of NMOS and PMOS SNTs with the I–V characteristics obtained from the three-dimensional device simulations as mentioned earlier. Parasitic RC components are subsequently added to the intrinsic models to create realistic extrinsic SPICE models used for circuit simulations. Chapter 3 shows the dominant RC parasitics of an SNT superimposed on its three-dimensional structure. In this figure, the parasitic capacitance between the source contact and the metal gate is denoted as C_{gs2}. The parasitic capacitance between the metal gate and the concentric source contact, C_{gs1}, is considered the largest dominant capacitor for the SNT. The gate-drain capacitors, C_{gd1} and C_{gd2}, and the drain-source capacitors,

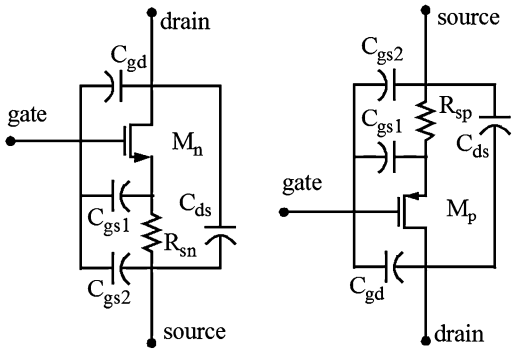

Fig. 4.10 Simplified parasitic components of (**a**) NMOS and (**b**) PMOS SNTs

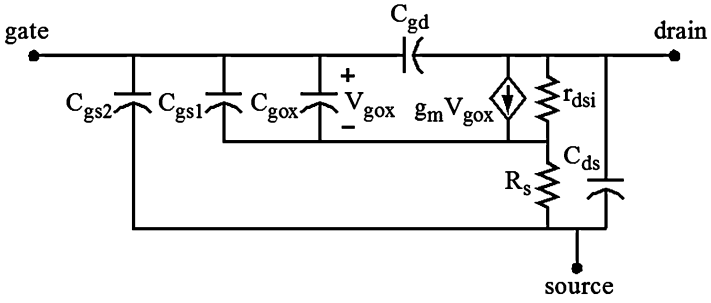

Fig. 4.11 Linearized small-signal model of SNT

C_{ds1} and C_{ds2}, can be lumped together to form C_{gd} and C_{ds}, respectively. Compared to planar bulk transistors, C_{gd} produces a very small value. In addition, there is no junction to bulk capacitance; therefore, C_{ds} becomes quite linear [1–3]. The well resistance, R_s, can be large and is a major drawback in vertical SNTs compared to planar transistors. The magnitude of this resistance can be reduced drastically by placing a concentric (ring shape) source contact in parallel with the well as discussed in Chapter 3. If the transistor is properly designed to ensure $G_s \gg g_m \gg g_{ds}$ (g_m is the intrinsic transconductance and g_{ds} is the intrinsic output conductance), the performance of the vertical SNTs surpasses those of the planar transistors for analog circuits.

The simplified parasitic RC components of the NMOS and PMOS SNTs are shown in Fig. 4.10 with lumped capacitors of C_{gd} and C_{ds}.

For simplified hand calculations and the amplifier AC parameters, the small-signal model in Fig. 4.11 can be used. This model is also helpful to compute the DC voltage gain and the output resistance of various amplifier stages at low frequencies.

Operational amplifiers offer differential amplifiers at the input stage followed by common-source amplifiers, cascode amplifiers and common-drain amplifiers in the later stages. The operation and the characteristics of an SNT differential amplifier

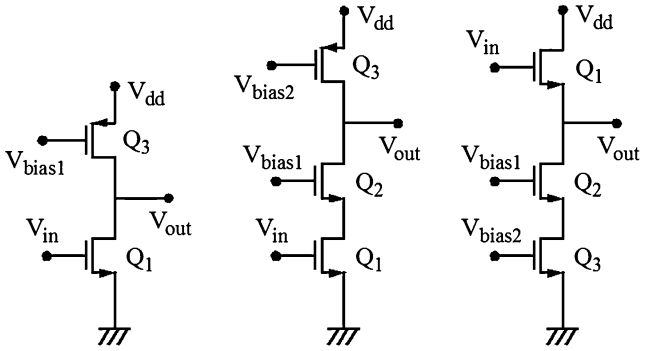

Fig. 4.12 Common-source, cascode, and common-drain amplifiers

were studied in the previous section. According to this study, the differential amplifier produced a gain of 16 at the first pole located at 100 GHz. However, to achieve high accuracy in the transfer functions of switch capacitor filters and amplifiers, it is important that operational amplifiers provide a voltage gain higher than 1000. Therefore, using only one differential pair at the input stage is not sufficient to implement a high-gain voltage amplifier; additional amplifying stages are most likely required. The second amplifying stage can also be used to improve the phase margin of the operational amplifier and ensure stability when using the amplifier in a closed loop configuration.

Common-source amplifiers, cascode amplifiers or common-drain amplifiers are the types of the amplifiers that follow the differential amplifier as shown in Fig. 4.12. Before designing a multi-stage SNT operational amplifier, the characteristics and the performance figures of each type need to be investigated.

Common-source amplifiers are used in the second stage of an operational amplifier and function as the Miller compensating stage. The low frequency small-signal model of the common-source amplifier is shown in Fig. 4.13.

The Kirchoff's current law at output branch results in

$$G_{s2}V_{gox2} = G_{s1}\left(V_{in} - V_{gox1}\right) \tag{4.9}$$

The output voltage V_{out} can be expressed by

$$V_{out} = (1 + r_{ds1}G_{s1})V_{in} - [1 + r_{ds1}(G_{s1} + g_{m1})]V_{gox1} \tag{4.10}$$

and

$$V_{out} = -[1 + r_{ds2}(G_{s2} + g_{m2})]V_{gox2} \tag{4.11}$$

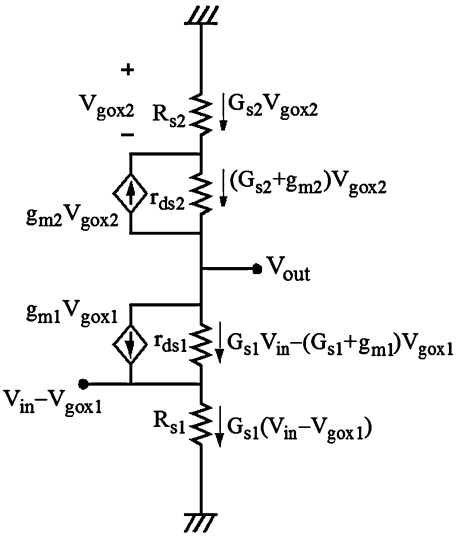

Fig. 4.13 Low frequency small-signal model of the common-source amplifier

Then the voltage gain of the common-source amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}r_{ds1}[1 + r_{ds2}(G_{s2} + g_{m2})]}{\left[1 + r_{ds2}(G_{s2} + g_{m2})\right] + \frac{G_{s2}}{G_{s1}}\left[1 + r_{ds1}(G_{s1} + g_{m1})\right]} \tag{4.12}$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximately given by

$$\frac{V_{out}}{V_{in}} = -g_{m1}(r_{ds1}//r_{ds2}) \tag{4.13}$$

The intrinsic gain, $g_m.r_{ds}$, can be as high as 15 for a common-source amplifier and it is not enough to use it for the Miller stage. SNTs have very high unity-gain cutoff frequency and very low current handling capability. Therefore, using a large Miller capacitance is not feasible to achieve frequency compensation. Therefore, other amplifier structures which can provide much larger gain need to be investigated to implement the Miller stage.

A cascode amplifier, as the second alternative, inverts the input signal as a common-source amplifier but with a much larger gain. The low frequency small-signal model of the cascode amplifier is shown in Fig. 4.14.

The Kirchoff's current law at output branch results in

$$G_{s3}V_{gox3} = G_{s1}\left(V_{in} - V_{gox1}\right) \tag{4.14}$$

The output voltage V_{out} can be expressed by

$$V_{out} = -[1 + r_{ds3}(G_{s3} + g_{m3})]V_{gox3} \tag{4.15}$$

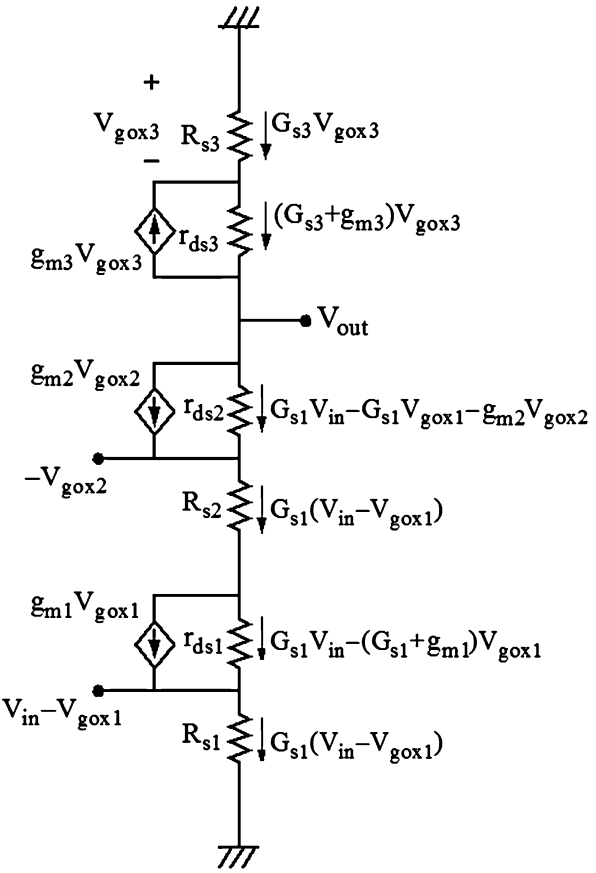

Fig. 4.14 Low frequency small-signal model of the cascode amplifier

and

$$V_{out} = r_{ds2}G_{s1}V_{in} - r_{ds2}G_{s1}V_{gox1} - (1 + r_{ds2}g_{m2})V_{gox2} \tag{4.16}$$

where

$$V_{gox2} = -[1 + G_{s1}(r_{ds1} + R_{s2})]V_{in} + [1 + G_{s1}(r_{ds1} + R_{s2}) + g_{m1}r_{ds1}]V_{gox1} \tag{4.17}$$

The voltage gain of the cascode amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{-G_{s1}[1 + r_{ds3}(G_{s3} + g_{m3})][(1 + g_{m2}r_{ds2})(2R_{s1} + 2R_{s2} + r_{ds1}(2 + g_{m1}R_{s1}))]}{G_{s3}[(1 + g_{m2}r_{ds2})(R_{s1} + R_{s2} + r_{ds1}(1 + g_{m1}R_{s1})) - r_{ds2}] - [1 + r_{ds3}(G_{s3} + g_{m3})]} \tag{4.18}$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximated as

$$\frac{V_{out}}{V_{in}} = \frac{-2g_{m2}r_{ds1}r_{ds2}r_{ds3}G_{s1}}{g_{m1}g_{m2}r_{ds1}r_{ds2}R_{s1} - r_{ds3}} \tag{4.19}$$

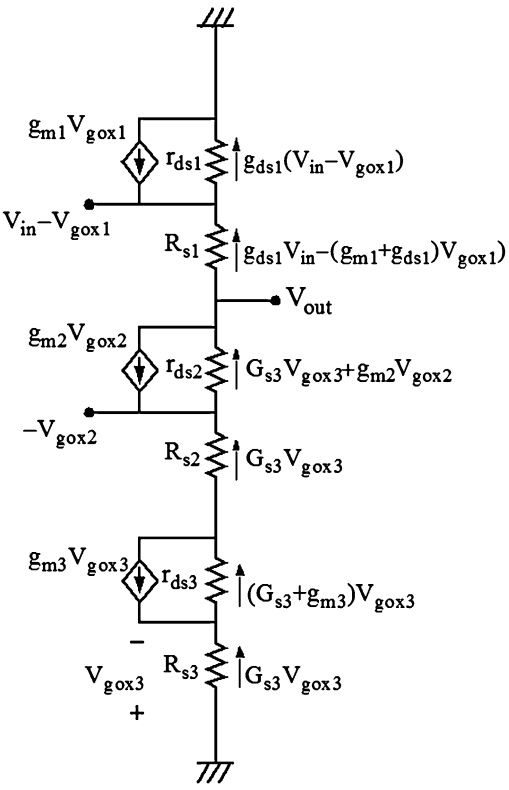

Fig. 4.15 Low frequency small-signal model of the buffer amplifier

The voltage gain can be very high due to a small value in the denominator.

The output resistance of the cascode amplifier is given by

$$R_{out} = [R_{s2} + g_{m2}r_{ds1}r_{ds2}(1 + g_{m1}R_{s1})]//[r_{ds3}(1 + g_{m3}R_{s3})] \tag{4.20}$$

For $G_s \gg g_m \gg g_{ds}$, the output resistance can be approximated as

$$R_{out} \approx r_{ds3}(1 + g_{m3}R_{s3}) \tag{4.21}$$

The SNT operational amplifier may have to drive high capacitive loads that belong to other analog stages. Therefore, it is very important to isolate the Miller stage from the load by using a buffer stage. A common-drain amplifier can be used for this purpose. The low frequency small-signal model of a common-drain buffer amplifier is shown in Fig. 4.15.

The Kirchoff's current law at output branch results in

$$G_{s3}V_{gox3} = -g_{ds1}V_{in} + (g_{ds1} + g_{m1})V_{gox1} \tag{4.22}$$

The output voltage V_{out} can be expressed by

$$V_{out} = (1 + R_{s1}g_{ds1})V_{in} - [1 + R_{s1}(g_{m1} + g_{ds1})]V_{gox1} \tag{4.23}$$

and

$$V_{out} = -(1 + r_{ds2}g_{m2})V_{gox2} - G_{s3}r_{ds2}V_{gox3} \tag{4.24}$$

where

$$V_{gox2} = -[1 + G_{s3}(r_{ds3} + R_{s2}) + g_{m3}r_{ds3}]V_{gox3} \tag{4.25}$$

The voltage gain of the amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}[-r_{ds2} + (1 + g_{m2}r_{ds2})(r_{ds3} + R_{s2} + R_{s3} + g_{m3}r_{ds3}R_{s3})]}{1 + (g_{m1} + g_{ds1})[R_{s1} - r_{ds2} + (1 + g_{m2}r_{ds2})(r_{ds3} + R_{s2} + R_{s3} + g_{m3}r_{ds3}R_{s3})]} \tag{4.26}$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximated as

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{m1}}{g_{m1} + g_{ds1}} \tag{4.27}$$

and this value is very close to unity.

The output resistance of the amplifier is given by

$$R_{out} = \left[R_{s1} + \left(r_{ds1} /\!/ \frac{1}{g_{m1}}\right)\right] /\!/ (g_{m2}r_{ds2}r_{ds3}) \tag{4.28}$$

For $G_s \gg g_m \gg g_{ds}$, the output resistance is approximated as

$$R_{out} \approx \frac{1}{g_{m1}} \tag{4.29}$$

and this value becomes very small.

Therefore, a high performance SNT operational amplifier can be implemented by a differential amplifier at the input stage, a cascode amplifier in the second stage and a common-drain amplifier in the final buffer stage as shown in Fig. 4.16.

The biasing control resistance, R_0, is adjusted to create a reference current of 670 μA for I_{ds13}, I_{ds23}, I_{ds43}, and I_{ds51}, and 1.4 mA for I_{ds33} in the current mirror circuit.

The overall low frequency voltage gain of the operational amplifier is given by

$$\frac{V_{out}}{V_{in}} \approx g_{m34}r_{ds34}\frac{-2g_{m42}r_{ds41}r_{ds42}r_{ds43}G_{s41}}{(g_{m41}g_{m42}r_{ds41}r_{ds42}R_{s41} - r_{ds43})}\frac{g_{m53}}{(g_{m53} + g_{ds53})} \tag{4.30}$$

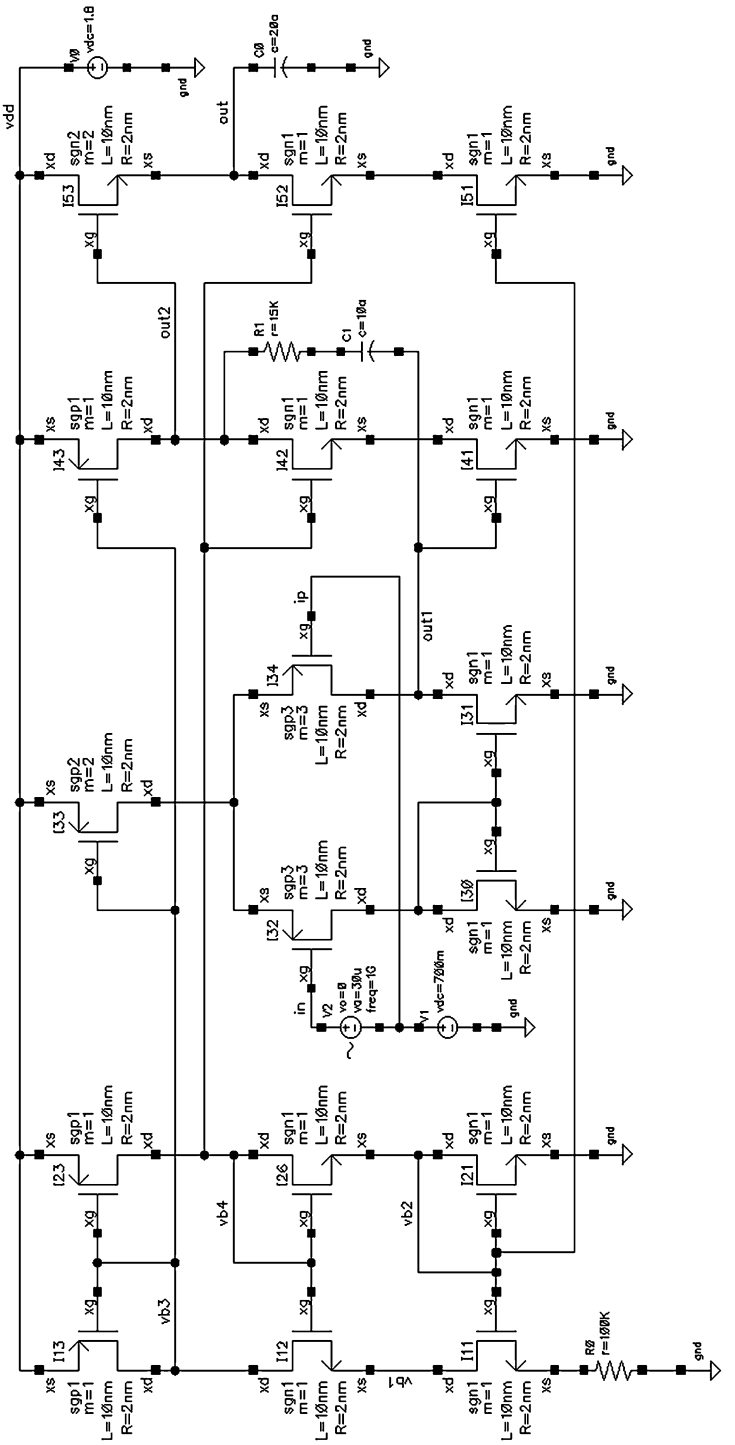

Fig. 4.16 The schematic of the two-stage operational amplifier

The location of the first pole is given by

$$f_L \approx \frac{1}{2\pi C_1 \frac{2g_{m42}r_{ds41}r_{ds42}r_{ds43}G_{s41}}{(g_{m41}g_{m42}r_{ds41}r_{ds42}R_{s41}-r_{ds43})}\left[r_{ds34}\left(1+\frac{g_{m34}}{g_{m32}}\right)//r_{ds31}\right]} \tag{4.31}$$

and the location of the second pole determined by the load capacitor is given by

$$f_H \approx \frac{g_{m53}}{2\pi C_0} \tag{4.32}$$

The slew rate (SR) is computed as

$$SR \approx \frac{I_{ds33}}{C_1} \tag{4.33}$$

4.5.2 Characteristics of the Operational Amplifier

The impact of the Miller capacitance on the location of the poles and its effect on the frequency response of the compensated and uncompensated operational amplifiers are shown in Fig. 4.17. The lead compensation produced by a series combination of a resistor, R_1, and a capacitor, C_1, helps to improve the unity voltage gain cutoff frequency of the operational amplifier without dissipating any power.

The layout of the SNT operational amplifier is shown in Fig. 4.18. The input transistors in the differential amplifier are implemented by a parallel combination of three PMOS SNTs to produce large transconductance and to be able to construct the Miller stage with NMOS SNTs. The biasing control resistor, R_0, is realized by an 8 nm wide and 320 nm long N-well. The frequency compensation is achieved by using a resistor, R_1, and a capacitor, C_1. In the compensation circuit, C_1 is implemented by 150 nm wide and 63 nm long metal 1 and metal 2 interconnect sandwich with 36 nm spacing. The resistor R_1 is implemented by 8 nm wide and 48 nm long N-well. The width of the metal interconnects is selected to be 14 nm to

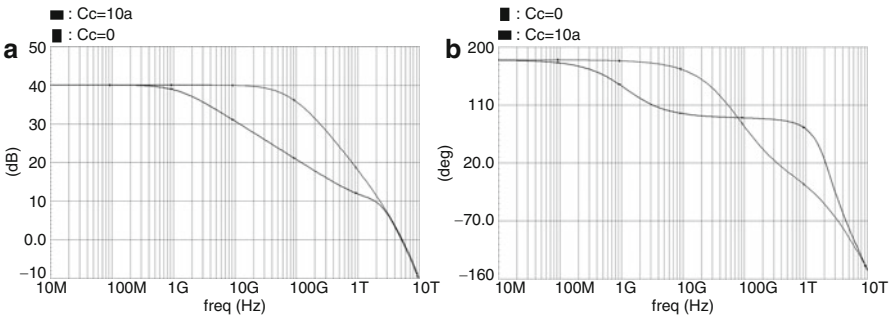

Fig. 4.17 Compensated and uncompensated (**a**) gain magnitude and (**b**) phase response of the SNT opamp

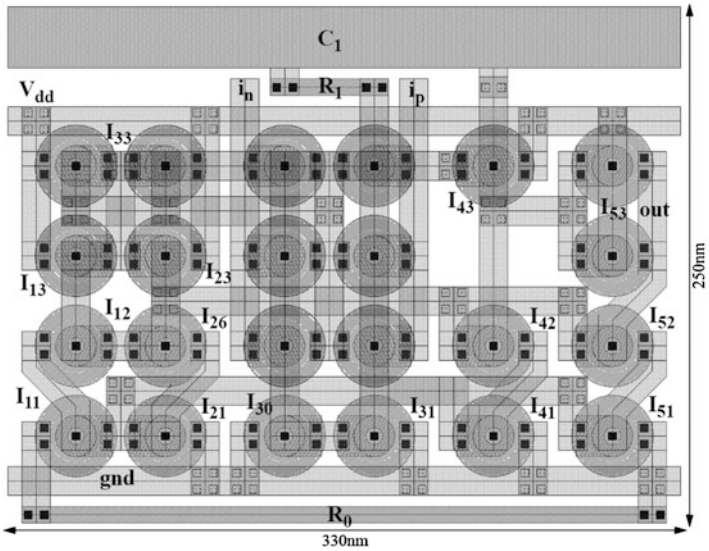

Fig. 4.18 The layout of the SNT operational amplifier

reduce the overall resistance, and four parallel vias are used to connect metal 1 layer to metal 2 layer to minimize the ohmic loss. Each 4 nm by 4 nm via produces 400 Ω. Each 14 nm by 14 nm overlap capacitance formed between metal 1 and metal 2 layers is 0.2 aF. The layout area of the operational amplifier including the biasing circuit and all compensation components occupies an area of 330 nm by 250 nm.

The post-layout frequency response of the SNT operational amplifier is shown in Fig. 4.19. This amplifier reveals a high unity voltage gain cutoff frequency at 5.1 THz but only dissipates 7.2 μW. The operational amplifier has a phase margin better than 90° for frequencies less than 1 THz and achieves a very stable operation.

The open loop transient response of the operational amplifier is shown in Fig. 4.20. The low frequency voltage gain of the amplifier is approximately 7760. For an input swing with 30 μV peak amplitude, the output of the amplifier produces 233 mV. The operational amplifier has good linearity characteristics and exhibits a total harmonic distortion of 3 % for ±233 mV output swing. This high linearity can be attributed to the source resistance, R_s, acting as the degeneration resistance, minimizing the harmonic distortions of each amplifier stage.

The Common-Mode Rejection Ratio (CMRR) and the Power Supply Rejection Ratio (PSRR) of the operational amplifier are shown in Fig. 4.21. The CMRR has a corner frequency at 100 GHz and the PSRR has a corner frequency at 1 GHz. The CMRR achieves 40 dB and the PSRR achieves 54 dB signal rejection.

The post-layout characteristics of the operational amplifier are listed in Table 4.3.

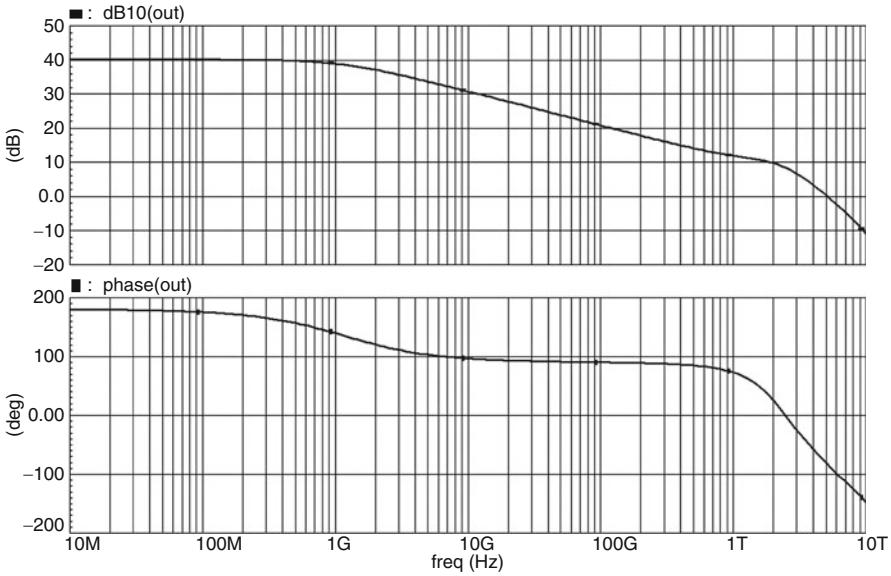

Fig. 4.19 Frequency response of the SNT operational amplifier

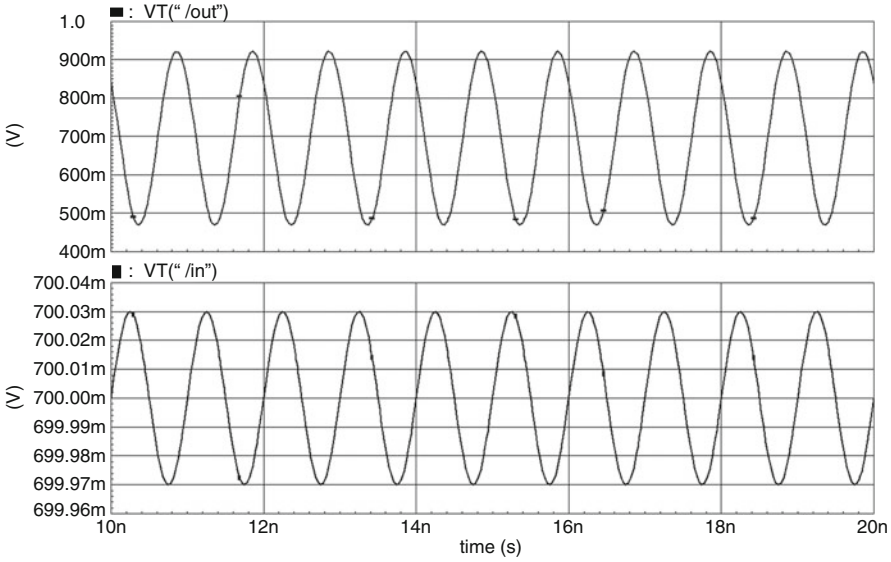

Fig. 4.20 Transient input and output waveforms of the operational amplifier

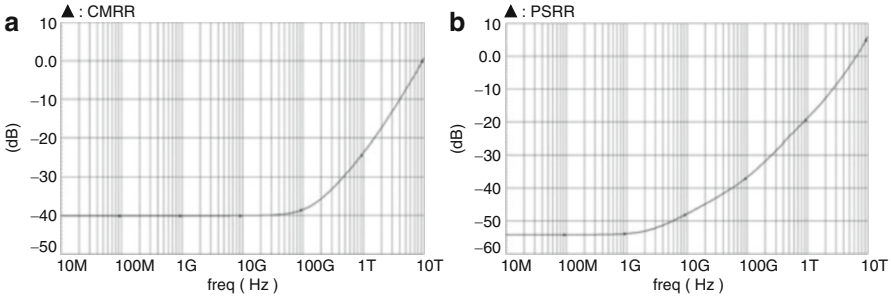

Fig. 4.21 (**a**) CMRR and (**b**) PSRR of the operational amplifier

Table 4.3 Post-layout characteristics of the two-stage SNT operational amplifier

Operational amplifier characteristics	
Supply voltage	1.8 V
Biasing circuit power dissipation	2.4 μW
Total power dissipation	4.8 μW
Maximum output linear signal swing	0.5 V
Input DC voltage level	0.7 V
Open loop voltage gain (at 1 GHz)	7760 or 38.9 dB
Open loop phase margin (at 1 GHz)	42°
Open loop unity voltage gain cutoff frequency	5.1 THz
Load capacitor	20 aF
Common-mode rejection ratio	40 dB
Power supply rejection ratio	54 dB
Total harmonic distortion	3 %
Slew rate (high to low)	2 V/ns
Slew rate (low to high)	2 V/ns
Area	0.0825 μm^2

4.6 Summary

The single-stage CMOS amplifier is a simple but a good circuit platform to show the capabilities of SNTs in large-signal and small-signal AC domains. In large-signal domain when the amplifier is used as an inverter, the circuit reveals 2.2 ps delay, 5.4 ps rise time and 4.7 ps fall time while oscillating at 30 GHz. In small-signal domain, the amplifier acts as a common-source amplifier if a proper DC level is introduced and a small AC source is applied to the input. When used as a single-stage common-source amplifier, the circuit dissipates 1.64 μW total power and produces a 500 GHz bandwidth with a −6.5 gain. The third order intermodulation distortion tones for a two-tone input signal become −24 dBm with 10 mV amplitude and 10 GHz frequency spacing.

Differential pair amplifiers provide unique circuit characteristics compared to all the other amplifier structures. Because there are two different AC signal paths from input to output, the gain of an amplifier in differential mode is much higher compared to the gain of an amplifier in common mode. This type also eliminates the amplification of noise and cross-talk because of the differential inputs. Besides high gain and low power, differential SNT amplifiers can achieve a very high common-mode rejection ratio which makes them good candidates for implementing operational amplifiers. The differential amplifier studied in this chapter dissipates 5 μW power and produces a 5 THz bandwidth with a voltage gain of 16. It produces a linear output voltage swing of 0.5 V and a total harmonic distortion better than 3 % from a 1.8 V power supply and a 20 aF capacitive load. The second and third order harmonic distortions of the amplifier are −40 and −52 dBm, respectively, and the third order intermodulation is −24 dBm for a two-tone input signal with 10 mV amplitude and 10 GHz frequency spacing.

The SNT operational amplifier consists of a differential amplifier at the input stage followed by a cascode amplifier. A common-drain amplifier can be used as a third stage in an operational amplifier to isolate the Miller stage from the load. This buffer stage also decreases the output impedance to be able to drive low resistive loads. The amplifier is frequency compensated for oscillation-free, stable operation with a 1.8 V power supply. It has a voltage gain of 40 dB and a phase margin of 42°. The current gain cutoff frequency is 5.1 THz and the amplifier produces 40 dB common-mode rejection ratio and 54 dB power supply rejection ratio with a slew rate of 2 V/ns. The layout area of a typical SNT operational amplifier is 320 nm by 250 nm.

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