Chapter 2
Single Work Function Silicon Nanowire MOS Transistors

2.1 Device Design

2.1.1 Purpose

In the first chapter of this book, SNTs with dual work function gates were designed and their device characteristics were examined. Later in the same chapter, basic digital CMOS gates were built; their circuit performance, power dissipation, and layout characteristics were analyzed; basic SNT processing steps were shown. A dual work function CMOS technology requires the use of different metals in NMOS and PMOS transistor gates. Finding the appropriate metals that match exactly to the work function values found in this study may often be a difficult enterprise as it may require alloys for gate material or incompatible metals with the SNT processing.

One way to reduce the set of problems associated with dual metals is to use a single metal gate. Therefore, this chapter is dedicated to design NMOS and PMOS transistors with a single work function metal gate, and furthermore use these transistors in designing CMOS circuits.

As in Chapter 1, this chapter will also introduce the design criteria for SNTs that use a single metal gate, show the design flow to select optimum device dimensions for both NMOS and PMOS transistors, and analyze speed, power dissipation and layout area characteristics of various CMOS logic gates and mega cells that use these devices.

The design criteria for the single work function NMOS and PMOS SNTs are very similar to what has been applied to the dual work function SNTs.

1. NMOS and PMOS transistors need to have at least 300 mV threshold voltage for 1 V CMOS circuit operation
2. The static OFF current has to be under 1 pA in either NMOS or PMOS transistor

A. Bindal, S. Hamedi-Hagh, *Silicon Nanowire Transistors*,
DOI 10.1007/978-3-319-27177-4_2

2.1.2 The Criteria for Low Static Power Dissipation

There are three major components that produce low static power dissipation in MOS transistors.

1. Junction leakage
2. Subthreshold leakage
3. Gate-Induced-Drain-Leakage (GIDL) current

The elements that reduce the OFF current are decreasing DIBL, tox, body doping concentration, and E_S as mentioned earlier in Chapter 1. In this study, tox is set to a minimum value to maintain negligible gate leakage compared to I_{OFF}. The body doping concentration is at the intrinsic level to minimize C_D. E_S is also kept at minimum because gate-drain region does not have any overlap.

2.1.3 Device Structure

As with the dual work function SNTs, this study also considers both NMOS and PMOS transistors enhancement type with undoped silicon bodies constructed perpendicular to the substrate. Both transistors have the same body radius and effective channel length. Source/drain (S/D) contacts are assumed highly doped to obtain ohmic contacts. Both NMOS and PMOS transistors have metal gates and 1.5 nm thick gate oxide.

Device simulations are performed using Silvaco's 3-D ATLAS device simulation environment with a 1 V power supply voltage. The device radius is changed from 1 nm to 25 nm while its effective channel length is varied between 5 nm and 250 nm.

2.1.4 Physical Models Used in Device Simulations

Nano-scale devices require quantum equations to obtain accurate estimations of carrier transport in the channel region. However, ATLAS simulator has limitations of using Schrodinger's equation in full capacity to calculate effective mass and mobility values, and therefore, it follows a semiclassical approach in which the semiconductor surface potential and density of states are corrected using the density gradient method. The parameters of this method are first calibrated according to the results of self-consistent Poisson–Schrodinger equation at a negligible current flow, and then used in drift–diffusion and hydrodynamic equations to compute current densities with Fermi–Dirac carrier statistics.

For low electric field effects, Lombardi's vertical and horizontal electric field dependent mobility model is used; for high electric fields, velocity saturation and

other high electric field effects are estimated by Caughey's drift velocity model. Arora's model is used for mobility degradation due to lattice temperature. To estimate the recombination rates in the bulk and at the silicon/oxide interface, concentration-dependent Shockley–Read–Hall recombination and surface recombination models are used, respectively.

Serberherr's impact ionization model constitutes the only generation model [1]. The semiconductor band-to-band tunneling mechanism producing GIDL current is not included in the simulations because of three factors. The first factor is the absence of a gate–drain (gate–source) overlap region in the cylindrical device structure: only the fringing component of the transverse electric field emanating from the edge of the gate may induce GIDL. The second factor is the decrease in transverse electric field (perpendicular to the current transport axis) compared to a bulk device with a single gate: surface band bending in bulk or a partially depleted SOI device is appreciable to promote GIDL current generation [2]. The third factor is the magnitude of the power supply voltage: the drain-to-gate potential being less than the silicon band gap is not an effective method to create enough band bending at the semiconductor surface to allow valence band electrons to tunnel into the conduction band. The gate oxide tunneling mechanisms and hot carrier injection are also ignored because these mechanisms largely depend on oxide growth and composition. Kim et al. [3] also pointed out that gate current constituted only a small percentage of the total OFF current for double-gated SOI devices with 1.5 nm gate oxide thickness.

2.1.5 Determining a Single Metal Gate Work Function

The first task of the design process is to determine a common metal gate work function that works for both NMOS and PMOS transistors as shown in Fig. 2.1. In this figure, threshold voltage, V_T, was measured as a function of metal gate work function for body radius values ranging between 1 nm and 25 nm at the minimum effective channel length of 5 nm. The intersection of NMOS and PMOS threshold voltages is projected to the *x*-axis to produce a common metal gate work function for each wire radius which results in a single threshold voltage for both transistors.

2.1.6 The OFF Current Requirement for the Design

The OFF current is an important factor towards lowering the standby power consumption in the entire chip. In this study, both NMOS and PMOS transistors are designed to have I_{OFF} in the proximity of 1 pA as mentioned previously. This value is significantly smaller than the OFF currents found in double-gated SOI

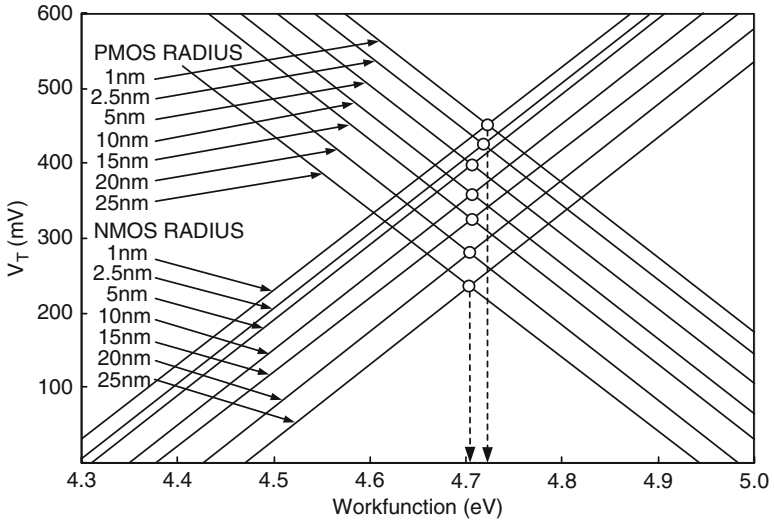

Fig. 2.1 Threshold voltages of NMOS and PMOS nanowire transistors as a function of metal work function at a minimum channel effective length of 5 nm. Both transistor radii are changed between 1 and 25 nm to produce single work function values approximately between 4.7 and 4.72 eV

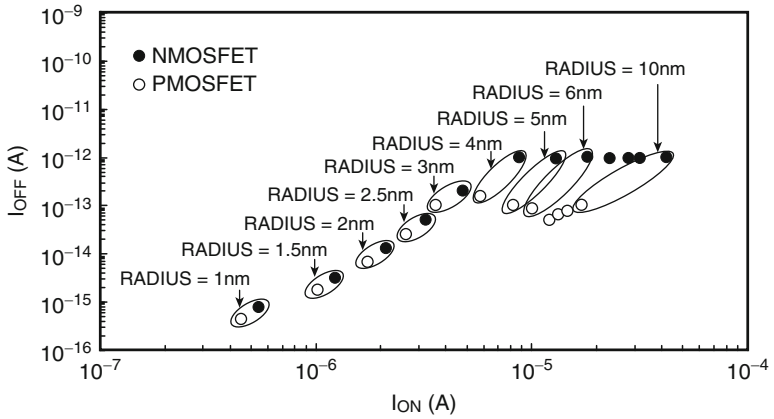

Fig. 2.2 ON versus OFF currents of NMOS and PMOS nanowire transistors. The radius of both transistors was changed between 1 and 10 nm while the effective lengths were varied between 5 and 37 nm

transistors in earlier modeling studies [3–5] and several orders of magnitude smaller than the value predicted by Sery [6]. Figure 2.2 shows I_{OFF} as a function of I_{ON} for wire radius between 1 nm and 10 nm and effective channel lengths between 5 nm and 37 nm for transistors producing 1 pA or smaller OFF currents. Table 2.1 lists the dimensions of the "selected" NMOS and PMOS transistors in Fig. 2.2.

2.1.7 *Transistor Transient Characteristics: Intrinsic Transient Time*

Following the device selection process for low static power dissipation, the intrinsic transient time, τ, of each transistor in Table 2.1 was measured. As described earlier in Chapter 1, the intrinsic transient time determines the time interval for a transistor to charge/discharge the gate capacitance of an identical transistor and it is plotted as a function of maximum DC transconductance, gmsat, in Fig. 2.3. The objective of this figure is to determine a common body dimension that produces maximum gmsat and minimum τ for both NMOS and PMOS transistors. In this figure, the only NMOS and PMOS device pair that exhibits the highest gmsat and the lowest intrinsic gate delay is the one with at 4 nm radius and 7 nm effective channel length, which is considered the optimum body geometry. The corresponding intrinsic transient time values of 0.5 ps for the NMOS and 0.7 ps for the PMOS transistor are also in close proximity to the results of Yu et al. [7] and Sery et al. [6].

Table 2.1 The dimensions of NMOS and PMOS nanowire transistors that satisfy IOFF < 1 pA

Body radius (nm)	Leff (nm)	Body radius (nm)	Left (nm)
1.0	5.0	5.0	12.0
1.5	5.0	6.0	16.0
2.0	5.0	7.0	22.0
2.5	5.0	8.0	27.0
3.0	5.0	9.0	32.0
4.0	7.0	10.0	37.0

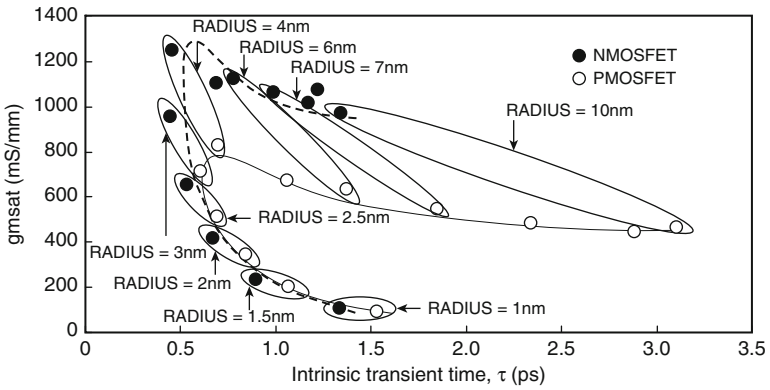

Fig. 2.3 Maximum DC transconductance versus intrinsic gate delay of the "qualified" NMOS and PMOS nanowire transistors whose leakage currents are below 1 pA

2.1.8 DC Characteristics of the Selected NMOS and PMOS Transistors

The threshold voltage roll-off of the 4 nm radius transistors with effective channel lengths ranging between 7 nm and 150 nm is measured to be 18 mV for the NMOS and 36 mV for the PMOS transistor. These values are an order of magnitude smaller than ΔV_T values of the 20 nm gate length bulk silicon transistors reported by Boeuf [8] and others [9–12].

The amount of DIBL is 114 mV/V for the NMOS and 69 mV/V for the PMOS transistors with 4 nm radius and 7 nm effective channel length. Figure 2.4 shows these values along with previously published data for comparison purposes [3, 7, 9, 11, 13, 14].

The subthreshold slope is found to be 65 mV/dec and 70 mV/dec for both NMOS and PMOS transistors at the drain voltages of 50 mV and 1 V, respectively. These results are plotted in Fig. 2.5 and show close-to-ideal characteristics in comparison with the modeling results of double-gated SOI transistors published in [3] and in the previous experimental data [7, 11–18].

Figure 2.6 shows the inverter transfer function produced by the 4 nm radius and 7 nm effective channel length NMOS and PMOS SNTs. The inverter threshold voltage (the projection of the output voltage at 0.5 V to the *x*-axis) is skewed towards 0 V due to the higher NMOS drive current; but, the inverter still produces sufficient low and high noise margins at 405 mV and 520 mV, respectively, for safe circuit operation.

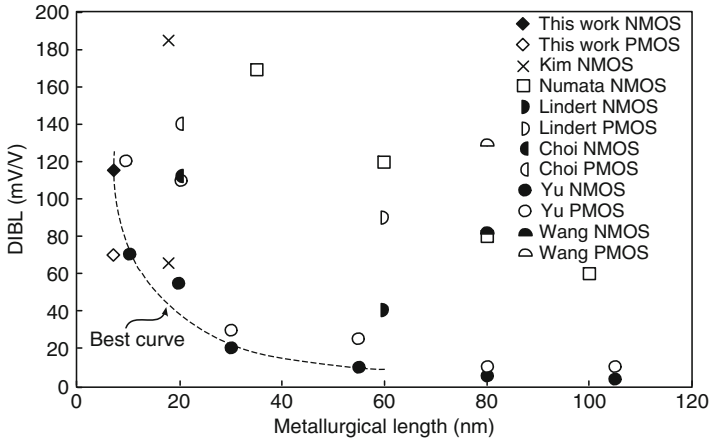

Fig. 2.4 Drain Induced Barrier Lowering (DIBL) of undoped, single work function NMOS and PMOS nanowire transistors with 4 nm body radius and 7 nm effective channel length. Prior work is included for comparison

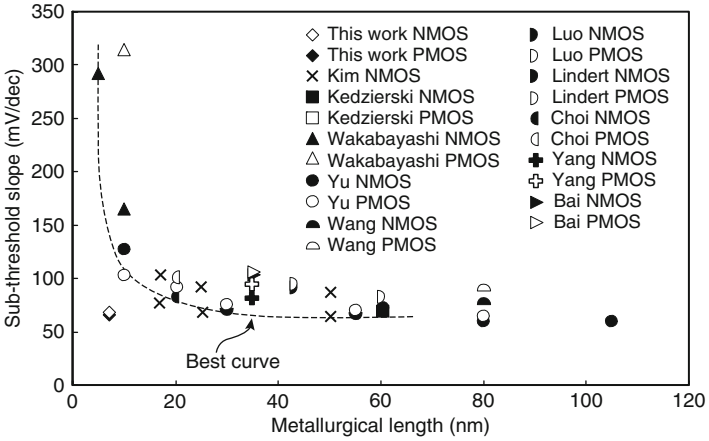

Fig. 2.5 Subthreshold slope of undoped, single work function NMOS and PMOS nanowire transistors with 4 nm body radius and 7 nm effective channel length. Prior work is included for comparison

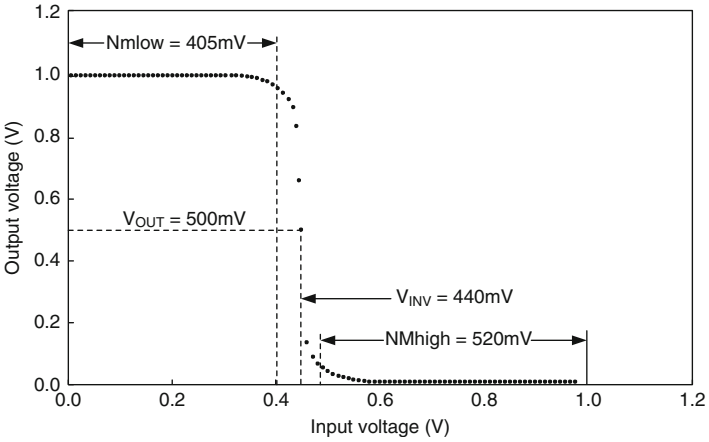

Fig. 2.6 Transfer function of an inverter built with 7 nm effective channel length and 4 nm radius NMOS and PMOS nanowire transistors. The inverter threshold voltage, V_{INV}, corresponds to the projection of Vout = 0.5 V to the *x*-axis

2.2 Circuit Performance

2.2.1 Parasitic Extraction and Post-layout Issues

As in the dual work function SNT study, primitive gates including an inverter, 2-input and 3-input NAND, NOR and XOR gates, and a full adder were built to measure the transient characteristics, power dissipation, and layout area of each

gate. All measurements were conducted before and after parasitic layout extraction and compared with each other to understand the effects of parasitic wire resistance, capacitance, and contact resistance on circuit performance. Since these transistors are constructed perpendicular to the substrate, the minimum exposed transistor feature on the layout is 4 nm wire radius to make contacts. Copper wires with 6.4 nm width and 1.4 aspect ratio (wire height to width) are used for interconnects and 2.4 nm by 2.4 nm vias are used for contacts. Since sub-10 nm range copper wire electrical characteristics do not exist in the literature, copper resistivity value was again determined from Srivastava's model [19] as shown in Fig. 1.14 in Chapter 1. Subsequently, 20 μΩ-cm resistivity was used to calculate the sheet resistance of 6.4 nm wide metal interconnects. Similarly, contact resistance was extrapolated from the experimental data on 100 nm and larger via diameters and resulted in 18.5 Ω for metal contacts as shown in Fig. 1.15 in Chapter 1.

A simple RC calculation on inverter rise and fall times reveals approximately 25 kΩ PMOS SNT channel resistance and 11.8 kΩ NMOS SNT channel resistance. If one limits the total contact and wire resistance values to be 10 % of the equivalent n-channel resistance (or 1180 Ω) to avoid interconnect-related delays, then the discharge path can accommodate a 349 nm long copper wire between two contacts. The maximum wire length in the inverter layout is only 54 nm long. Because the equivalent PMOS channel resistance is 25 kΩ instead of 11.8 kΩ, the charge path in the inverter can even support more wire resistance. More complex circuits containing multiple transistors in series can tolerate higher numbers of contacts and longer wire lengths in charge and discharge paths. However, long wire lengths interconnecting different cells may exhibit high resistance values and produce slow nodes and larger overall circuit delays. Fortunately, in the upper-metal routing, design rules are more relaxed, allowing wider and thicker wires.

Area, fringe, and coupling capacitances of metal 1 and metal 2 wires per unit length are calculated using Ansoft's two-dimensional electrostatic solver. These capacitance values are used to extract metal-to-metal and metal-to-substrate parasitic capacitances from layouts for circuit simulations.

2.2.2 Transient Performance

The worst-case transient time and delay are shown in Figs. 2.7 and 2.8 as a function of load capacitance after layout parasitic extraction for different CMOS gates. In each figure, a capacitance value of 40 aF corresponds to a fan-out of ten SNTs, considering the gate capacitance of a single transistor is approximately 4 aF.

The worst-case transient times shown in Fig. 2.7 are essentially the worst-case rise times since a PMOS transistor has higher equivalent channel resistance compared to an NMOS transistor. The worst-case transient times of the inverter, 2-input and 3-input NAND gates overlap with each other primarily due to the single PMOS transistor charging the output capacitance. The worst-case transient times of the 2-input NOR and XOR circuits cluster together because two PMOS transistors in

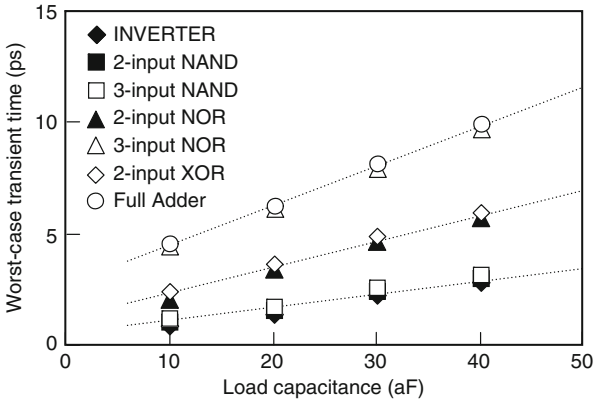

Fig. 2.7 Post-layout worst-case transient time characteristics of various primitive gates built with 7 nm effective channel length and 4 nm body radius NMOS and PMOS nanowire transistors

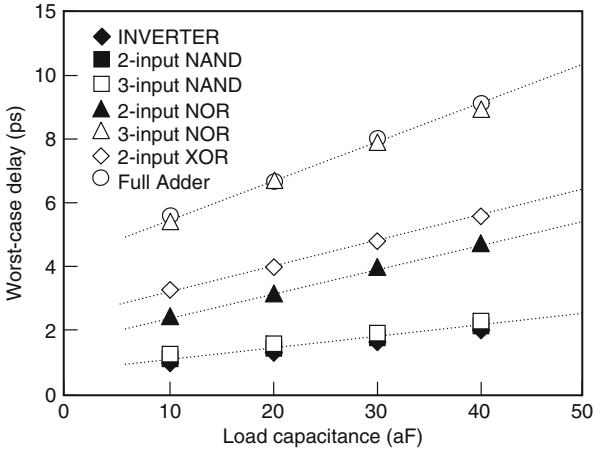

Fig. 2.8 Post-layout worst-case propagation delay characteristics of various primitive gates built with 7 nm effective channel length and 4 nm body radius NMOS and PMOS nanowire transistors

series charge the output load. The full adder and 3-input NOR circuits are in close proximity and reveal the highest worst-case transient times because the number of PMOS transistors in series increases from two to three in the critical charging path. For example, the worst-case transient times of the 2-input NAND gate and full adder in Fig. 2.7 are expressed as $T = 0.378 + 0.052C_L$ and $T = 3.21 + 0.179C_L$ in picoseconds, respectively, where C_L is the output capacitance in aF.

As in the dual work function SNTs, Fig. 2.8 shows similar characteristics compared to the worst-case transient times in Fig. 2.7 because each CMOS logic gate in this figure uses the same critical charging and discharging paths to compute worst-case delays. For example, the worst-case delays of the 2-input NAND gate and the full adder circuits are expressed as $T_D = 0.667 + 0.033C_L$ and $T_D = 4.45 + 0.124C_L$ in picoseconds, respectively, where C_L is the output capacitance in aF. Worst-case gate delay values obtained from CMOS circuits that use SNTs are significantly smaller in comparison with the CMOS circuits that use bulk silicon or SOI technologies. Inverter gate delays of 4 ns and 5 ns from a chain of

double-gated SOI and bulk silicon inverters [3] are substantially larger compared to the 1 ps inverter gate delay obtained in this study.

The effect of gate layout parasitics on transient performance is substantial when there is no capacitive load and decreases proportionally as the output capacitance increases. Worst-case post-layout gate delays at no capacitive load increase between 17 % and 36 % after layout extraction. This change primarily stems from the layout complexity, transistor count and number of series transistors on the critical path. For example, the worst-case delay of the full adder increases by 36 % after parasitic extraction when there is no output load and decreases to 14.7 % for a fan-out of six transistors.

2.2.3 *Dynamic Power Dissipation*

The worst-case dynamic power dissipation of various CMOS gates is shown in Fig. 2.9 as a function of frequency, f, when a 10 aF capacitive load is connected to each logic gate's output. Worst-case power dissipation is obtained by considering all the possible input combinations to a logic gate, measuring the average value of the power supply current within one clock period (activity factor = 1 %) for each combination, and finally selecting the combination that yields the maximum average current. Each current waveform is averaged within one clock period during charging and discharging cycle of the output capacitance. In general, worst-case power dissipation increases with increasing transistor count, layout complexity, and the number of "parallel" charging or discharging paths to a capacitive load. For example, the worst-case power dissipations of the 2-input NAND gate and full adder circuits are expressed as $P = 0.33 + 32.97f$ and $P = 0.66 + 59.93f$ in nanowatts, respectively, in Fig. 2.9.

Figure 2.10 shows the worst-case power dissipation figures of each CMOS gate as a function of load capacitance at 1 GHz. For example, the worst-case

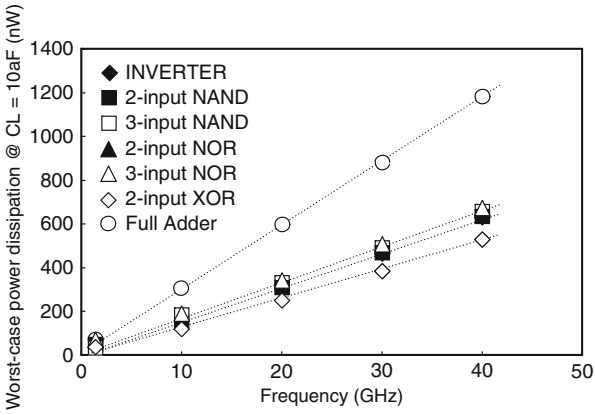

Fig. 2.9 Post-layout worst-case power dissipation of various primitive gates built with 7 nm effective channel length and 4 nm body radius NMOS and PMOS nanowire transistors at a capacitive load of 10 aF

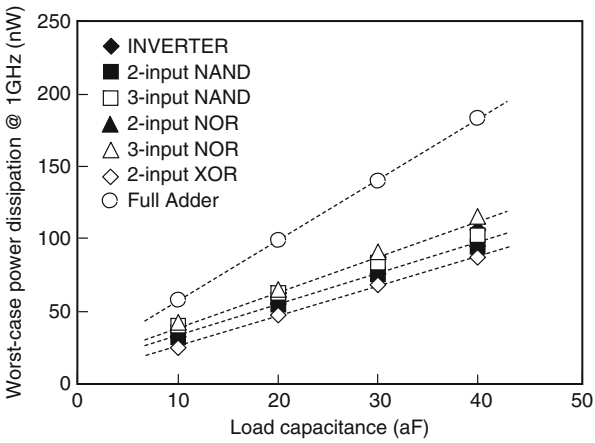

Fig. 2.10 Post-layout worst-case power dissipation of various primitive gates built with 7 nm effective channel length and 4 nm body radius NMOS and PMOS nanowire transistors at 1 GHz

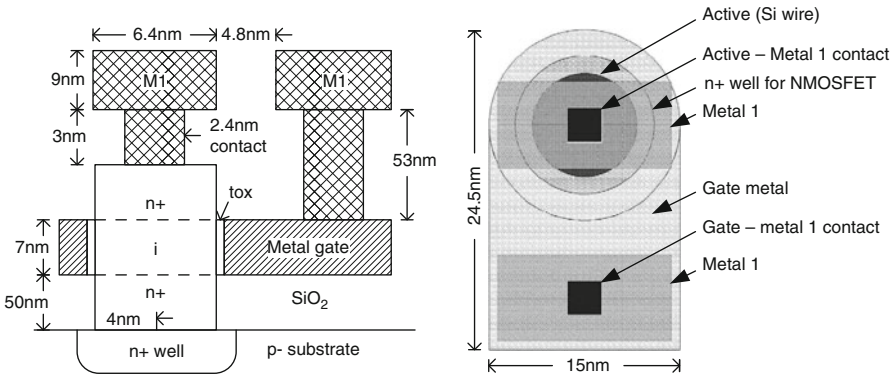

Fig. 2.11 Cross section and layout of a single, 7 nm effective channel length and 4 nm body radius NMOS transistor. Note that an N-well (shown by dashed lines in the cross-sectional view) surrounds only the p^+ well of PMOS transistors

power dissipations of the 2-input NAND gate and full adder circuits produce $P = 12.67 + 2.06C_L$ and $P = 19.44 + 4.11C_L$ in nanowatts, respectively.

2.2.4 Cell Layout Area Estimations

An inverter, 2-input and 3-input NAND, NOR and XOR circuits, and a full adder were laid out using the 4 nm radius nanowire transistors. Figure 2.11 shows the cross section and the corresponding layout of a single SNT. The active region defines the circular body of the device which is surrounded by an N-well if the transistor is an n-channel device or a P-well if it is a p-channel. The outmost circle represents the metal gate and is connected with a rectangular gate extension. All

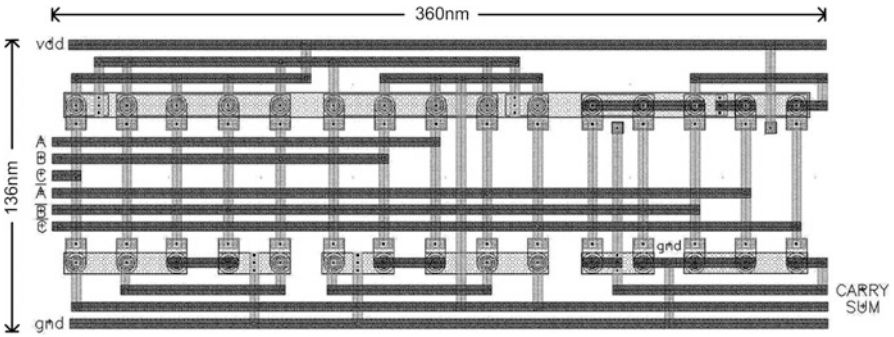

Fig. 2.12 Full adder layout using 7 nm effective channel length and 4 nm body radius NMOS and PMOS nanowire transistors. A, B, and C are the two inputs of the full adder and the carry-in, respectively. $\overline{A}$, $\overline{B}$, and $\overline{C}$ correspond to the two complemented inputs of the full adder and the carry-in, respectively

Table 2.2 Layout area of various primitive gates built with 7 nm effective channel length and 4 nm body radius NMOS and PMOS nanowire transistors

Gates	Area (nm^2)
Inverter	5712
2-input NAND	6624
3-input NAND	8736
2-input NOR	6624
3-input NOR	8736
2-input XOR	10,752
Full Adder	48,960

contacts are indicated by 2.4 nm by 2.4 nm black squares touching the drain (source) and the gate of the transistor.

Figure 2.12 shows the layout of a full adder. The vertical dimension is fixed at 136 nm in all cell layouts. Each circular structure corresponds to a vertical NMOS or PMOS transistor. Interconnections are established by 6.4 nm wide metal 1 and metal 2 wires. Power and ground connections are made to the P- and N-wells with multiple contacts, a metal 1 layer, a via and a metal 2 layer. The P-well is completely surrounded by an N-well to prevent latch-up. Layout areas of the primitive gates used in this study are listed in Table 2.2, which are considerably smaller than the state-of-the-art counterparts. The 28-transistor full adder in this study has a cell area of approximately 0.049 μm^2. Extrapolation of a 28-transistor CMOS full adder layout area in 350 nm [20], 180 nm [21], and 45 nm technology nodes towards the 7 nm technology node still produces a layout area of approximately 40 μm^2, which is more than 800 times larger than the full adder area shown in Fig. 2.12.

Table 2.3 Circuit performance, power dissipation, and layout area of 28-transistor full adder in this study and earlier work

Lg (nm)	V_{DD}(V)	f_{op} (MHz)	P_T (nW)	Delay (ps)	Area (μm^2)	References
350	3.3	[a]	164,000	227	[a]	[54]
350	1.2	50	2490	2037	387	[54]
350	1.8	50	6090	827	387	[54]
350	2.5	50	12,820	528	387	[54]
350	3.3	50	24,120	406	387	[54]
350	3.3	[a]	65,000	400	[a]	[54]
250	3.3	[a]	58,000	300	[a]	[54]
180	3.3	[a]	30,000	100	[a]	[54]
180	1.0	100	2500	650	[a]	[54]
180	1.8	100	6230	292	100	[54]
180	1.0	100	1450	756	100	[54]
180	1.8	300	345	195	[a]	[54]
180	1.8	50	11	327	[a]	[54]
7	1.0	1000	118[b]	7.5	0.05	[54]

[a]Cases not reported
[b]An output load of 24 aF (6 transistor gates)

2.2.5 Full Adder Comparison

In order to acknowledge the significance of this technology with respect to the earlier and emerging technologies, a 28-transistor CMOS full adder circuit is examined in terms of transient performance, power dissipation, and layout area in various technology nodes. The results of this study are tabulated in Table 2.3, which shows the full adder in this study excels in all three categories [20–26].

2.3 Summary

Three-dimensional undoped NMOS and PMOS SNTs with a single-work-function metal gate were designed to minimize the leakage current under 1 pA and maximize the DC transconductance as a function of device radius and effective channel length. Device simulations were performed in Silvaco's Atlas device design environment to produce transistor DC characteristics such as ON and OFF currents, ΔV_T, DIBL, and S. Transient performance, power dissipation, and layout area of an inverter, multi-input NAND, NOR and XOR gates, and full adder circuits were measured and analyzed. As a specific case, simulation results showed that the worst-case transient time and the worst-case delay for the 2-input NAND gate are 1.63 ps and 1.46 ps, respectively, and for the full adder 7.51 ps and 7.43 ps, respectively. The worst-case power dissipation is 62.1 nW for the two-input

NAND gate and 118.1 nW for a full adder operating at 1 GHz for the same output capacitance. The layout areas are 0.0066 μm^2 for the 2-input NAND gate and 0.049 μm^2 for the full adder circuits. Compared to the results previously reported on silicon bulk and double-gated SOI transistors, these data indicate the silicon wire technology is a potential choice for the future of VLSI circuits because of overall low gate delay and transient times, compact layout area, and low static and dynamic power dissipation.

References

1. Serberherr S (1984) Process and device modeling for VLSI. Microelectron Reliab 24:225–257
2. Choi Y, Ha D, King T, Bokor J (2003) Investigation of gate induced drain leakage (GIDL) current in thin body devices: single-gate ultra-thin body, symmetrical double gate, and asymmetrical double gate MOSFETs. Japan J Appl Phys 42:2073–2076
3. Kim K, Das K, Joshi R, Chuang C (2005) Leakage power analysis of 25-nm double gate CMOS devices and circuits. IEEE Trans Electron Devices 52:980–986
4. Zhang R, Roy K, Janes D (2001) Double-gate fully-depleted SOI transistors for low-power high performance nano-scale circuit design. ISLPED. pp 213–218
5. Yang J, Fossum J (2005) On the feasibility of nanoscale triple-gate CMOS transistors. IEEE Trans Electron Devices 52:1159–1164
6. Sery G, Borkar S, De V (2002) Life is CMOS: why chase the life after? DAC. pp 78–83
7. Yu B (2002) FinFET scaling to 10 nm length. IEDM. pp 251–254
8. Boeuf F (2004) A conventional 45 nm CMOS node low-cost platform for general purpose and low power applications. IEDM. pp 425–428
9. Numata T (2004) Performance enhancement of partially and fully-depleted strained-SOI MOSFETs and characterization of strained-Si device parameters. IEDM. pp 177–180
10. Shima A, Ashihara H, Hiraiwa A, Mine T, Goto Y (2005) Ultrashallow junction formation by self-limiting LTP and its application to sub-65 nm node MOSFETs. IEEE Trans Electron Devices 52:1165–1171
11. Wang H (2004) Low power device technology with SiGe channel, HfSiON, and poly-Si gate. IEDM. pp 161–164
12. Luo Z (2004) High performance and low power transistors integrated in 65 nm bulk CMOS technology. IEDM. pp 661–664
13. Lindert N, Choi Y, Chang L, Anderson E, Lee W (2001) Quasi-planar NMOS FinFETs with sub-100 nm gate lengths. Device Research Conf. pp 26–27
14. Choi Y, Lindert N, Xuan P, Tang S, Ha D, Anderson E (2001) Sub-20 nm CMOS FinFET technologies. IEDM. pp 421–424
15. Wakabayashi H (2004) Transport properties of sub-10 nm planar-bulk-CMOS devices. IEDM. pp 429–432
16. Bai P (2004) A 65 nm logic technology featuring 35 nm gate lengths, enhanced strain, 8 Cu interconnect layers, low-k ILD and 0.57 μm2 SRAM cell. IEDM. pp 657–660
17. Kedzierski J, Dried D, Nowak E, Kanarsky T, Rankin J (2001) High performance symmetric-gate and CMOS compatible Vt asymmetric-gate FinFET devices. IEDM. pp 437–440
18. Yang F, Chen H, Chen F, Chan Y (2001) 35nm CMOS FinFETs. Symp. VLSI Technol. pp 104–105
19. Srivastava N, Banerjee K (2004) A comparative scaling analysis of metallic and carbon nanotube interconnections for nanometer scale VLSI technologies. Proc. 21st Int. Multilevel Interconnect Conf. pp 393–398

20. Alioto M, Palumbo G (2002) Analysis and comparison on full adder block in submicron technology. IEEE Trans VLSI Syst 10:806–823
21. Chang C, Gu J, Zhang M (2005) A review of 0.18 μm full adder performances for tree structured arithmetic circuits. IEEE Trans VLSI Syst 13:686–695
22. Chang C, Zhang M, Gu J (2003) A novel low power low voltage full adder cell. Proc. 3rd Int. Symp. Image Signal Proc. Analysis. pp 454–458
23. Shams A, Darwish T, Bayoumi M (2002) Performance analysis of low-power 1-bit CMOS full adder cells. IEEE Trans VLSI Syst 10:20–29
24. Sayed M, Badawy W (2002) Performance analysis of single-bit full adder cells using 0.18, 0.25 and 0.35 μm CMOS technologies. IEEE Int. Symp. Circuits Syst. pp 559–562
25. Khatibzade A, Raahemifar K (2004) A study and comparison of full adder cells based on the standard static CMOS logic. Canadian Conf. Electron. and Comput. Eng. pp 2139–2142
26. Goel S, Gollamudi S, Kumar A, Bayoumi M (2004) On the design of low-energy hybrid CMOS 1-bit full adder cells. 47th Midwest Symp. Circuits and Syst. pp 209–211