Chapter 82
Development of Silicon Pad and Strip Detectors in High Energy Physics

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Abstract The unique properties of semiconductors makes them suitable for precise measurement of particle's tracks and if placed in a magnetic field, high accuracy momentum measurements are possible. Silicon, with low band gap (1.12 eV) and electron-hole pair creation energy (3.62 eV) are very efficient to create a large number of charge carriers due to ionizing particle. High density (2.33 g/cm^3) leads to large energy loss in detector bulk by ionizing particles, which gives access to production of thin detector with fairly large signal. With high electron mobility ($\mu_e = 1450\,\text{cm}^2/\text{Vs}$) and hole mobility ($\mu_h = 450\,\text{cm}^2/\text{Vs}$) silicon detector provides very fast signal. The Planner technology is widely used for fabrication of semiconductor detectors. The main steps of fabrication of semiconductor detectors are passivation, patterning, doping to form P^+ and N^+ regions, contacts. In this paper, the fabrication of Silicon Pad Detector at IIT Bombay has been described.

82.1 Introduction

Silicon strip detectors are widely used tracking sensors in high energy physics experiments. The strip sensor improves the spacial resolution of tracks of ionizing particles. When passing silicon bulk, particle produces a measurable signal proportional to energy deposited.

This section contain details of fabrication process of silicon detector using planar process. Figure 82.1 shows cross sectional view and of working of semiconductor detector [1]. The fabrication of silicon pad detector with active area of 5 mm × 5 mm from n-type silicon wafer is described. The pad detectors fabricated on 2 in n-type silicon wafer with thickness of 250 ± 15 μm and (111) orientation. The resistivity of silicon wafer is 3000−5000 Ω cm. To filter small DC current noise through contacts, a thin layer of oxide (≈100−200 nm) is deposited between p

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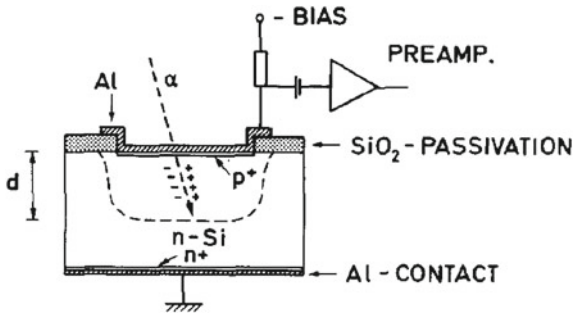

Fig. 82.1 Working principle of Si detector

implant and Al contacts. Semiconductor sensors operates in fully depleted voltage region, to ensure breakdown protection, an additional rings surrounds the sensor pad. These rings are called as *guard rings* and kept floating while measurement. This rings ensures definite drop of voltage along a larger distance and potential drop from one ring to another is adjusted via punch through biasing.

82.2 Silicon Pad Detector

The quartz sand (SiO_2) is abundant form of silicon in nature. For detector fabrication silicon wafer should have very high purity of 99.999999999 % or better than 1/100 ppb [2]. Electronic Grade Silicon (**EGS**) wafers are used for detector manufacturing. Two famous single crystal growth techniques are *Czochraiski (CZ) Silicon* and *Float Zone (FZ) Silicon* [3]. The n- or p-type silicon wafers with different resistivity are produced by adding amount of dopants to the crystal during the production (arsenic or phosphorus for n-type and boron for p-type). FZ prime quality silicon wafer is used for fabrication of silicon pad detector.

Although the manufacturing of silicon detector uses a traditional processes in semiconductor technology, the great care has to be taken for low contamination with impurities during production. Any contamination of oxide or sensor bulk and uniformity over the wafer would increase leakage current through sensor and change the operating voltage. The following subsections describes production of silicon detector at IIT Bombay.

82.2.1 Thermal Oxidation

Silicon dioxide (SiO_2) or silica with dielectric constant of 3.9 is natural oxide of silicon and easily produced on silicon in very thin and uniform layers. Thin layers of SiO_2 are deposited by heating the silicon wafer in an oxygen environment. Oxidation can be preformed at temperature 800–1200 °C using either molecular oxygen

(Dry Oxidation) or water vapour (Wet Oxidation).

$$Si + O_2 \longrightarrow SiO_2 \text{ (dry oxidation)} \tag{82.1}$$

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2 \text{ (wet oxidation)} \tag{82.2}$$

The silicon wafer is cleaned using RCA cleaning process, which is a standard cleaning process for silicon to avoid contamination during oxidation. Thermal oxidation is performed using Pyrogenic wet oxidation furnace at temperature 1050 °C in presence of H_2 and O_2 gasses. Thickness of SiO_2 layer formed on silicon wafer is 630 ± 10 nm.

82.2.2 Photolithography

Photolithography is used to transfer the layout that are designed to silicon wafer. The designed device structure is transferred to iron oxide film on glass substrate to prepare photomask (Fig. 82.3). Figure 82.2a shows a photomask design for silicon pad detector.

Patterning of SiO_2 is done using double sided mask aligner. Silicon wafer is coated with uniform layer of UV light sensitive positive photoresist of thickness 2 μm. It is then soft baked at temperature of 90 °C for 5 min. The photoresist is then exposed to UV light through photomask using double sided mask aligner. After exposure, wafer is developed to remove exposed photoresist and transfer the structure from mask to wafer. There is possibility of under etching or over etching in this process and it has to taken in to account while designing photomask. Figure 82.4a shows silicon wafer with pattern of photoresist and SiO_2. Figure 82.4b shows microscopic image of SiO_2 pattern of one device.

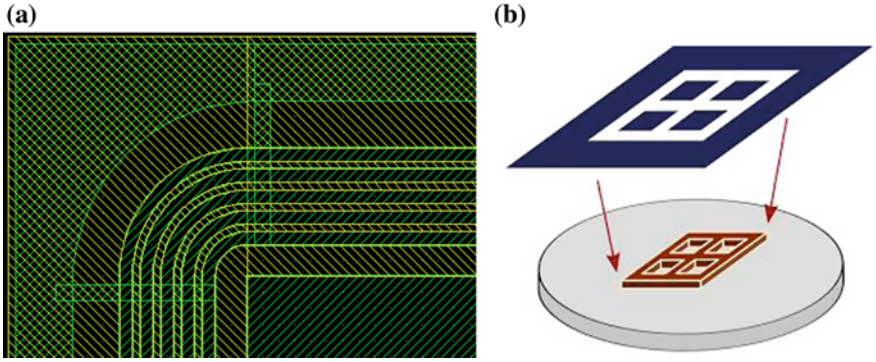

Fig. 82.2 Photolithography exposure and mask design. **a** Digital design of photomask. **b** Positive mask exposure

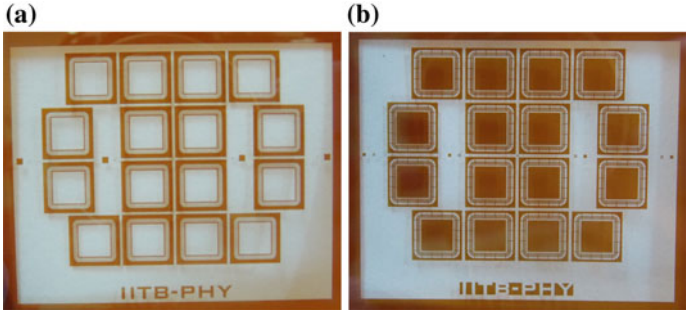

Fig. 82.3 Photomask using iron oxide plates. **a** Layer 1: pattering of pad for doping. **b** Layer 2: pattering of pad after metallization

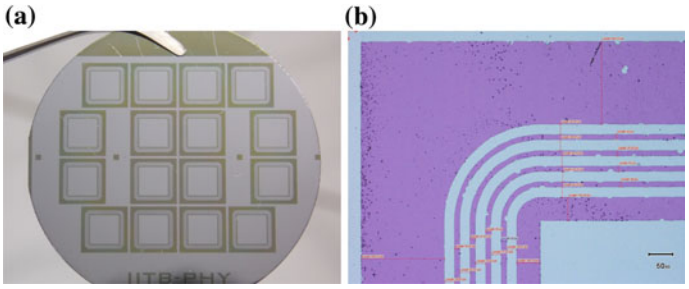

Fig. 82.4 Photomask on iron oxide using laser writer. **a** Patterning of PPR after development. **b** Pattering of SiO_2 at one device

82.2.3 Doping

To create the p-n junction, n-type silicon wafer can be doped using two methods either by ion implantation or by diffusion. Ion implantation is advantageous because, it can be performed at low temperature which prevents material deterioration and implantation profiles can be attuned precisely by proper energy and dosage of ion beam. To avoid channeling of ions, crystal axis is tilted by an angle of about 7° to beam direction. For p-side i.e. top side doping, boron beam with an energy of 2 keV and a dosage of 5×10^{15} ions/cm^2. For n^+ i.e. bottom side doping, arsenic or phosphorus beam of energy 2 keV and a dosage of 5×10^{15} ions/cm^2 is used. Once doping is done, high temperature treatment is necessary to activate the dopants. The sample is cleaned and annealed at 900 °C under dry Nitrogen. Figure 82.5 shows doping profiles for optimised parameters of the process [4].

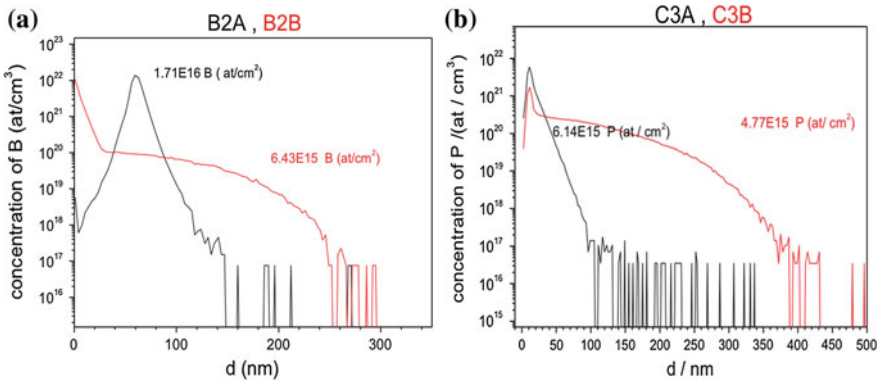

Fig. 82.5 Doping profiles for optimised parameters. **a** Boron doping profile. **b** Phosphorus doping profile

82.2.4 Metallization

Metallization is done to create contacts which are required for connection to readout systems. Al is widely used material to make contacts for Si detectors. Al can be deposited using Thermal evaporator and patterned by photolithography after ion implantation. Al must be very thin (<500 Å) to avoid absorption and deterioration of energy resolution due to energy straggling. Aluminium spikes are much less likely observed in crystal with orientation (111) than on (100) surfaces. From this wire bonding can be done using Al wires.

82.3 Silicon Strip Detector

We have also started fabrication of single sided silicon strip detector using n-type silicon wafer of thickness 250 ± 15 μm. The prototype is of 2 cm × 2 cm size with 50 μm of pitch. Total active area is 1.92 cm × 1.92 cm with total 384 strips. The dimension of pitch define the resolution of strip detector. The Guard rings surrounds the active area to protect it from breakdown. The bias to the strip can be done by two methods, *polysilicon biasing* and *punch through biasing.*

82.4 Next Steps

The immediate next step will be to characterize the silicon pad detector and test it with radiation source. Then we will proceed for fabrication and testing of prototype of single sided silicon strip detector.

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