Chapter 5
Neural Stimulation and Charge Balancing Approaches

Abstract The stimulating electrodes are generally configured in monopolar and bipolar configurations. Common simulation modes are the current mode and voltage mode. The usual stimulation waveforms are either monophasic or biphasic. Charge imbalance occurs by semiconductor failure. Such imbalance may also arise from leakage currents. The main cause is cross talk between adjacent stimulating channels (sites) as well as cable failure. Positive charge balance is provided by a blocking capacitor connected in series with each electrode. This protective mechanism is used for electrical safety against fault conditions. The large capacitance value required for the blocking capacitors (sometimes a few microfarads) is realized through off-chip surface-mount components. In applications, e.g., retinal implants, the large-size blocking capacitors cannot be used. This inability is due to physical size limitations. Then, other methods for active charge balancing are resorted to. A stimulator circuit that is foolproof without off-chip blocking capacitors produces an active stimulation phase by high-frequency current switching. This phase is followed by a succeeding passive discharge phase.

Keywords Monopolar electrode • Bipolar electrode • DAC • ADC • VIC • Voltage multiplier • CCS • VCS • ChCS • Charge balancing • Blocking capacitor

5.1 Introduction

In electrostimulation, different types of stimulating electrodes, modes, and pulse waveforms are used.

5.2 Monopolar and Bipolar Electrodes

A monopolar electrode has a single pole. Hence, it is a single electrode starting from the stimulator. It consists of an insulated wire whose tip is uncovered to deliver the current to the site to be stimulated (Fig. 5.1). The return path followed by the current

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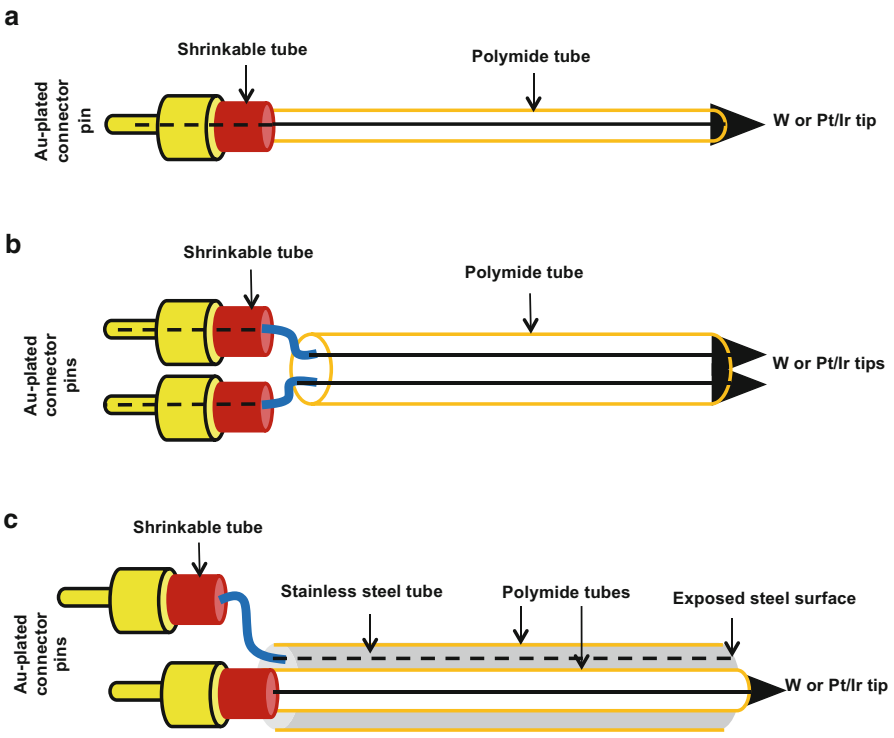

Fig. 5.1 Stimulation electrodes: (**a**) monopolar, (**b**, **c**) bipolar, (**d**) concentric bipolar electrode

is through the body of the patient to the earth. A bipolar electrode has two poles. Hence, it comprises two electrodes. One electrode is for entry of current from the stimulator into the patient tissue. Another electrode is for its exit from the tissue back to the stimulator.

In monopolar mode, the current begins its journey from the first terminal of the stimulator and traverses all through the stimulated site. Then, the current flows through the body of the patient to the ground to complete the circuit. In bipolar mode, the current only passes through the tissue between the two electrodes of the stimulator. The active and return functions take place at the targeted site. Thus, in the monopolar mode, the region of confinement of current in the body is larger. In the bipolar mode, it is smaller; in effect, the current is localized around the site. Concentric bipolar electrode and twisted wire bipolar electrode are the two popular types of bipolar electrodes. Table 5.1 explains the manner in which stimulations are carried out using the two types of electrodes and their resulting effects.

Table 5.1 Monopolar and bipolar stimulation

Sl. No.	Monopolar stimulation	Bipolar stimulation
1.	Current flow path: Starting from the pulse generator, it passes though the tissue, moves through the subject's body, and then goes back to the ground	Current flows between the regions separating the tips of the two electrodes: active and return electrodes that are incorporated into a single device
2.	Current flows across a larger chunk of the body of the patient receiving the implant	Current flow is confined to a limited region of the body of the implant receiver
3.	Stimulation effect is spread over a larger region	Stimulation effect is restricted to a smaller area

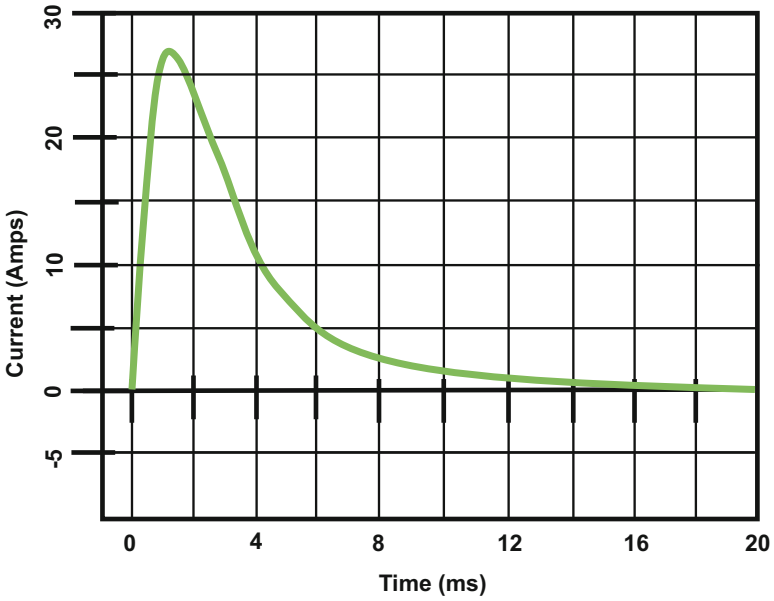

Fig. 5.2 Monophasic waveform

5.3 Monophasic and Biphasic Waveforms

Considering square-shaped stimulating pulses, a monophasic wave is a unidirectional wave. It consists of only one type of pulses, either positive pulses or negative pulses (Fig. 5.2).

A biphasic wave is a bidirectional wave. It comprises a positive pulse (anodic pulse) immediately followed by a negative pulse (cathodic pulse) or vice versa (Fig. 5.3). A train of pulses is a sequence of pulses of the intended type at repeated definite intervals of time.

To visualize the relative impact and effectiveness of these waveforms, defibrillators using the two waveforms are considered in Table 5.2.

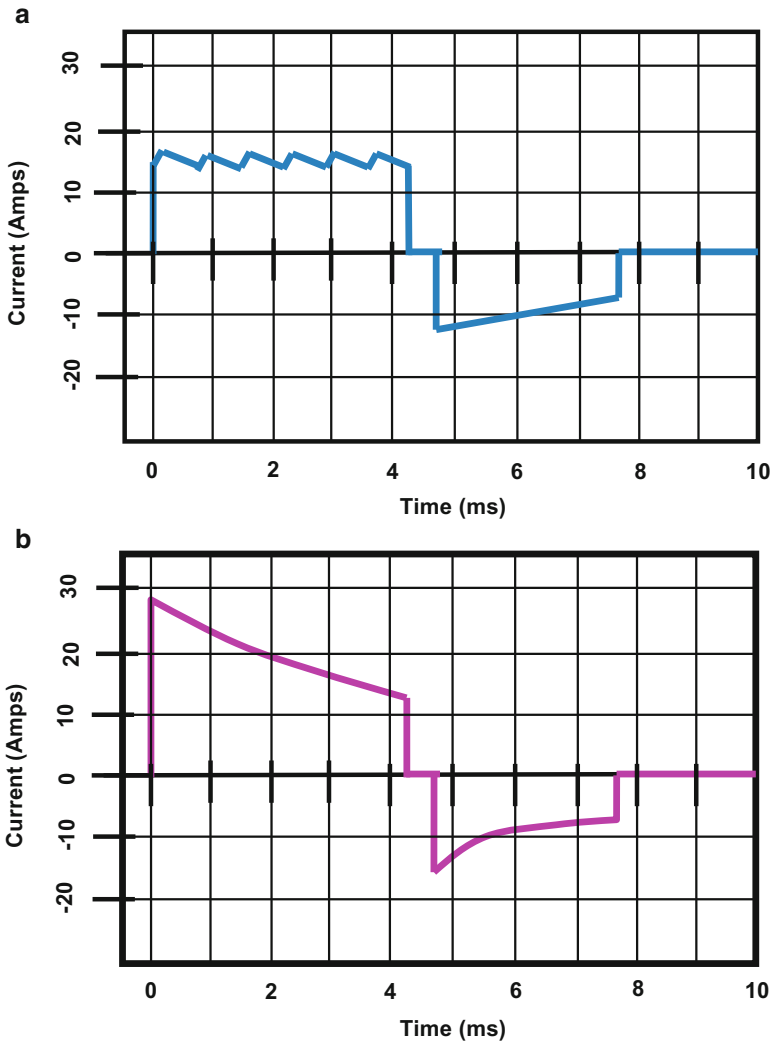

Fig. 5.3 Biphasic waveforms: (**a**) rectilinear biphasic and (**b**) biphasic truncated exponential

Table 5.2 Monophasic and biphasic defibrillators [1]

Sl. No.	Monophasic defibrillator	Biphasic defibrillator
1.	The shock is given in one direction only from a given electrode to another electrode	The direction is reversed in the latter part of the shock, and magnitude of voltage in this latter part is generally lower than in the initial part. Biphasic truncated exponential and rectilinear biphasic waveforms are commonly used
2.	Less effective	More effective
3.	Need more energy ~360 J	Require less energy ~200 J. A biphasic protocol using 120–200 J has the same efficacy as a monophasic protocol having 200–360 J
4.	Chances of more potential damage to the heart by the energy shock	Less likely damage to the heart by the lower energy shock

5.4 Functional Circuit Blocks

Many elementary circuits occur repeatedly in discussions on stimulators. It is worthwhile to recapitulate some of these circuits to facilitate understanding.

5.4.1 CMOS Switch

A CMOS switch (Fig. 5.4) is an electronic switch. It consists of two MOS transistors that are always in opposite operational conditions. When $V_G = 0$ V, the P-channel transistor Q_1 is on. At this time, the N-channel transistor Q_2 is off. An output approximating V_{ss} is obtained. This is the open switch state. When $V_G = V_{ss}$, the output ~0. In this condition, the P-channel transistor Q_1 is off. The N-channel transistor Q_2 is on. This is the closed switch state. Thus, the transistor combination is driven back and forth between V_{ss} and 0.

5.4.2 Digital-to-Analog Converter

This circuit lies on the borderline between the notional digital world and the realistic analog life. It is a circuit which converts a signal having a few, usually two (binary) defined levels/states into a signal (current, voltage, or charges) having theoretically infinite number of levels/states.

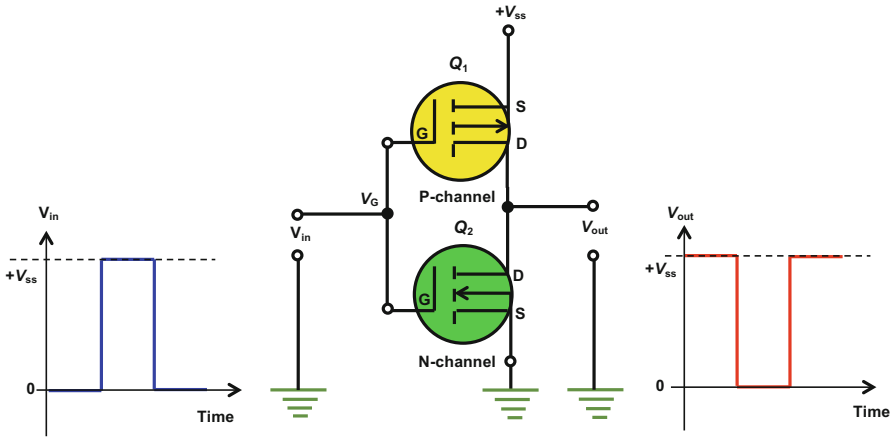

Fig. 5.4 The CMOS switch

The main kinds of digital-to-analog converters (DACs) are:

1. *The Pulse-Width Modulator*: It is an ingenious DAC of preliminary nature. It involves the switching of a steady current or voltage into an analog filter of low-pass type (Fig. 5.5). The digital input code determines the duration of switching. By analog filtering, the high-frequency components of the signal are removed. Only the DC component is left behind. The bandwidth of the DAC depends on that of the low-pass filter used.
2. *The Binary Weighted DAC*: It contains n switches. In this arrangement of switches, one switch is reserved for every single bit fed to the input. The DAC also has a weighted resistor ladder network. In this network, the values of resistances are selected in such a manner that they bear inverse proportionality relationship with binary weights of the input bits. Besides, the circuit has a reference voltage V_{Ref}. A summing amplifier performs addition of all the currents flowing in the resistor ladder network. By summing, it produces a signal proportional to the digital input (Fig. 5.6). In voltage scaling, the digital inputs are decoded. The corresponding switches are turned on to produce the analog output. This output is generated by dividing the reference voltage V_{Ref} by the series resistor network. The discrete voltages appearing on the nodes are smoothened by interpolation circuit.
   It is a fast conversion method. However, it suffers from poor accuracy. The reason for inability to provide adequate accuracy is that the circuit requires very exact values of every individual voltage or current. To meet this demand, high-precision resistors or current sources are necessary. These are expensive, so often one has to manage with components of average precision. Hence, application of this type of converter is seldom done beyond 8-bit resolution. For an 8-bit converter, the eight resistor values are distributed in the range between R and $128R$ in binary weighted steps. Large-scale manufacturing of this type of DAC is problematical. This difficulty arises due to the range of resistor values needed with desired tolerances. The tolerance required is <0.5 % to accurately convert the input. Further, it is very difficult to match the temperature coefficients of all the resistors.
3. *The R/2R Ladder DAC*: This DAC employs repeating resistors of only two different values, namely, R and $2R$ (Fig. 5.7). Hence, $2N$ resistors are required to assemble an N-bit DAC. These resistors are quite easily laser trimmed to obtain correct values because only few resistors have to be trimmed. In comparison, for high-accuracy conversion, a weighted resistor DAC necessitated a much expansive range of resistance values and switches for its different bit positions. An $R/2R$ ladder DAC eradicates the snags of weighted resistor DAC at the outlay of an extra resistor for each bit. DAC precision is thereby increased considerably. The chief cause is the comparative ready availability of equal matched values of resistors or current sources. But conversion speed is lowered owing to parasitic capacitance.

There are two possible modes of operation of an $R/2R$ ladder network. These are the voltage mode and the current mode. The voltage-mode $R/2R$ ladder DAC is implemented by switching the arms of the ladder between V_{Ref} and ground. The output signal is obtained from the end of the ladder.

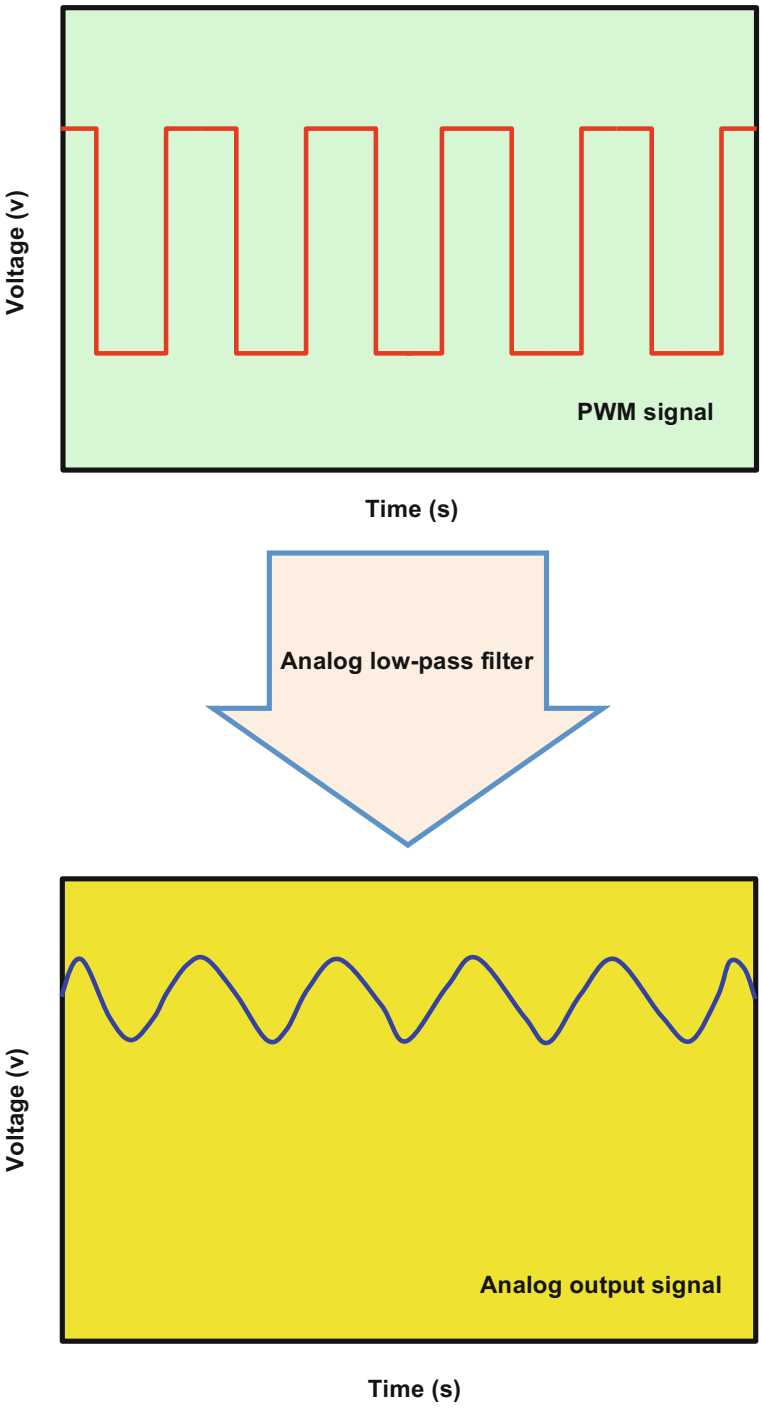

Fig. 5.5 Digital-to-analog conversion by analog low-pass filtering

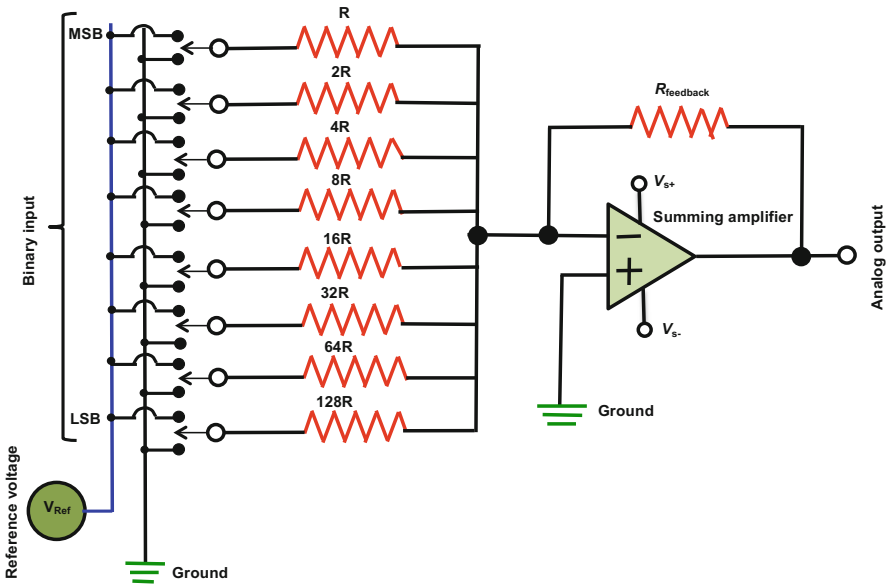

Fig. 5.6 An 8-bit binary weighted DAC constructed from weighted resistors and a summing amplifier

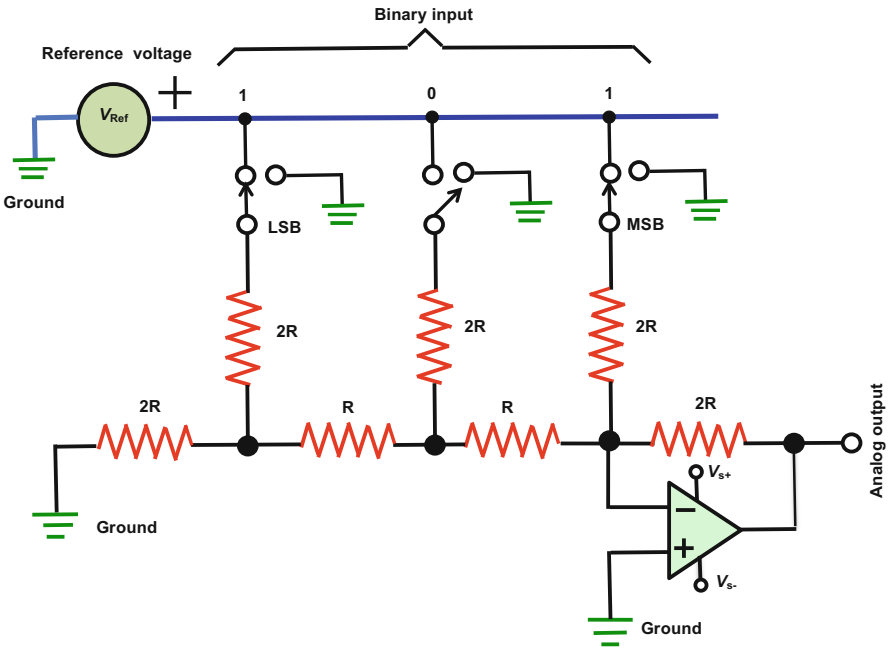

Fig. 5.7 R/2R ladder DAC

The function of current-mode $R/2R$ ladder DAC is based on the adjustment of the gain of the DAC. This adjustment is made by connecting a series resistor at the V_{Ref} terminal. The output is connected to an OP-AMP. This OP-AMP is configured as a current-to-voltage (I/V) converter.

DACs are prone to switching glitches. A glitch means a sudden, temporary malfunction. Current-mode operation is more liable to the hazard of switching glitch than voltage mode. The glitch encountered with current-mode switching arises from the manner of connection of switches. In this mode, the switches are directly connected to the output line(s). But the design of switches of a current-mode ladder network is less tricky. This is because they are always at ground potential. On the whole, their voltage specification does not impinge on the V_{Ref} rating.

5.4.3 Analog-to-Digital Converter

It is a circuit which converts a continuously variable signal having theoretically infinite number of levels/states into a signal having a few, usually two (binary) defined levels/states. An A/D converter translates analog electrical signals portraying actual world events, e.g., mechanical, optical, acoustic, or thermal signals, into digital form for handling and manipulating data. The analog-to-digital converters (ADCs) are at the front end of any digital circuit used to process signals from the exterior world.

ADCs are of the following types: flash, successive approximation register (SAR), pipelined, integrating or dual slope, and sigma delta ($\Sigma\Delta$). All the ADCs work on the same principle. They produce a signal consisting of a certain number of bits N. The sequence of bits represents the signal. Beginning from the most significant bit (MSB) and moving to the least significant bit (LSB), each bit has doubled the weight of the next. The different ADCs to be discussed have their own strengths and weaknesses. The choice of the ADC for a given application is defined by the priority in requirements of speed, precision, compactness, power consumption, etc.

Also called the parallel A/D converter, a flash converter uses a resistive ladder. This ladder divides the reference voltage linearly into 2^N equal parts (Fig. 5.8). OP-AMP comparators at different rungs of the ladder compare the input signal to successive unique reference voltages supplied by the corresponding part of the resistive ladder. One comparator is provided for each reference level. Starting with $V_{\text{Ref}} = 1/2_{\text{LSB}}$, each comparator compares V_{in} to a different reference voltage. If $V_{\text{in}} > V_{\text{Ref}}$, the output signal is high logic level. If $V_{\text{in}} < V_{\text{Ref}}$, the output signal is low logic level. The output signals from these comparators are fed into a priority encoder circuit. The output signal from the priority encoder is a binary number. This binary number is based on the highest-order active input signal, paying no heed to any other active input signal. The flash converter is a very fast ADC. Hence, it is aptly named flash converter. But it needs many parts (255 comparators for 8-bit ADC), doubling in size for each bit added to the representation. Resolution is low and power consumption is high. The ADC is expensive.

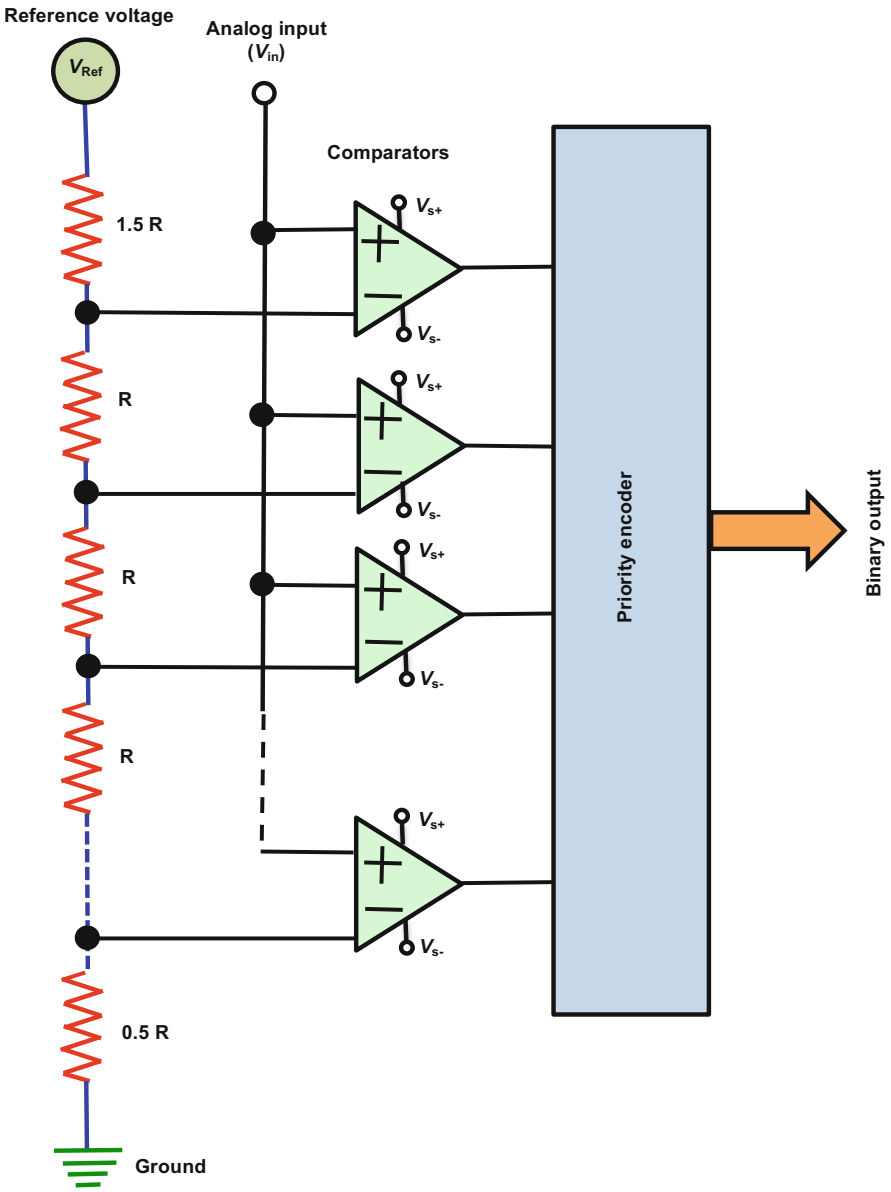

Fig. 5.8 Flash ADC based on direct conversion architecture including comparator banks and reference resistor divider networks

Successive-approximation-register (SAR) ADC is the preferred structural design for achieving average-to-large resolution and applications demanding accuracy. It provides low power consumption. Besides, it has a small form factor. It offers a worthy compromising solution between speed and cost. Its speed is limited to

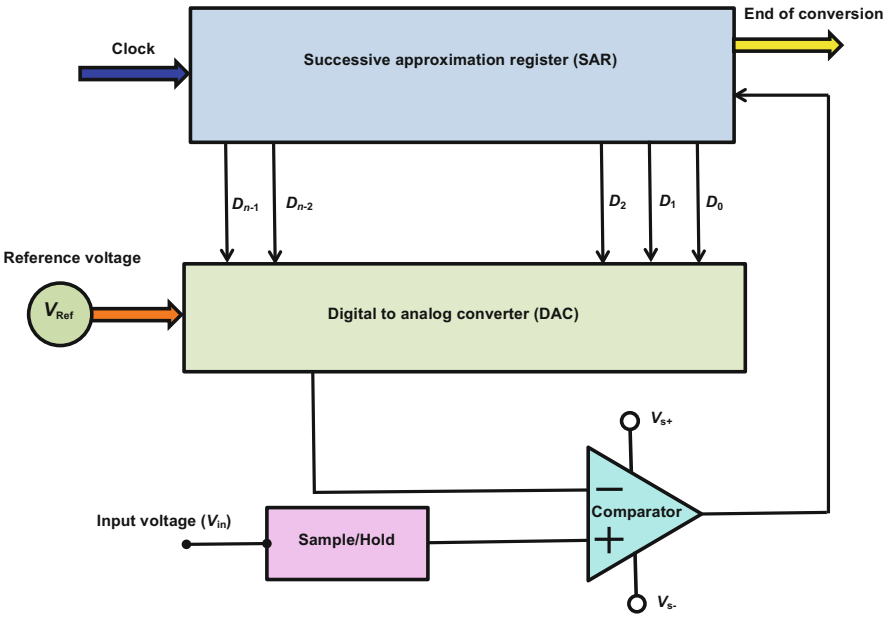

Fig. 5.9 Successive-approximation-register ADC

~5Msps. The SAR ADC (Fig. 5.9) consists of a successive-approximation-register subcircuit. Along with it a comparator, a DAC, and digital control logic are included. As obvious from its very name, the SAR ADC implements a fundamental algorithm in computer science called the binary search algorithm to look for the position of a targeted value in an organized collection. In this algorithm, the *N*-bit register is initialized and placed at midscale. This register is a counter circuit. It counts by attempting all values of bits. During counting, it begins with the MSB and terminates at the LSB. The ADC assumes the MSB to be 1 and the remaining bits to be 0. So, the DAC produces an output value of 0.5 V_{Ref} where V_{Ref} is the reference voltage furnished to the ADC. Then, a comparison is made to find whether V_{in} is $<V_{\text{DAC}}$ or V_{in} is $>V_{\text{DAC}}$. If V_{in} is $>V_{\text{DAC}}$, the output signal of the comparator is a high logic level. In this situation, the MSB of the *N*-bit register remains at 1. In opposition, if V_{in} is $<V_{\text{DAC}}$, the output signal of the comparator is a low logic level. The MSB of the register is reset to logic 0.

The SAR control logic budges to the succeeding bit downwards by following a similar procedure. It compels that bit to ascend to high logic level and performs one more comparative assessment. The above sequence of steps carries on, treading along the path towards the LSB. When the sequence reaches LSB, the conversion has been completed. The register shows the *N*-bit digital word.

5.4.4 Voltage and Current Sources

A voltage source is a device having two terminals, which maintains a fixed output voltage across it, independent of load resistance variations. The internal resistance of an ideal voltage source is zero. So, load resistance changes do not affect the voltage.

A current source is a circuit that supplies or receives fixed electric current in it, independent of the voltage across it. The internal resistance of an ideal current source is infinite. So, the current is not affected by changes in the load resistance. The current source is the dual of a voltage source. Ideal voltage and current sources are depicted in Fig. 5.10.

In a circuit diagram, a real voltage source is shown as an ideal voltage source in series with a resistance *r*. For the ideal voltage source, resistance = 0. The circuit diagram representation of a real current source is in the form of an ideal current source in parallel with a resistance *r*. For the ideal current source, resistance = ∞.

5.4.5 Current Source vs. Current Sink

The term "current source" is used when current flows from the invisible region such as the battery to the visible region, making the electric circuit to do some work. This is analogous to water current ejected from a mountain spring (invisible underground) to the surrounding areas. In a current source, the current flows towards the output, i.e., the load.

The term "current sink" is used when the current flows from the visible region such as a circuit to the invisible region inside the battery for charging the same. This flow is similar to the flow of water current from the tap to the drain where it cannot be seen. In the case of a current sink, the current flow occurs towards the input, i.e., away from the load. Figure 5.11 shows ideas of current source and current sink.

Sources and sinks are analysis formalisms. They are applied for distinguishing between directions in which current enters or exits a system.

5.4.6 Current Mirror

It is also called current-controlled current source (CCCS). The current mirror circuit reads a current entering a read node. It copies the current to an output node(s). It does so with a suitable gain. In other words, it is a replicating circuit. It copies the current flowing through one active device in the circuit. It does so by controlling the current passing through another active device of the circuit. The current is maintained constant irrespective of any loading effect. Hence, a high output resistance is shown. The current mirror also has a low input resistance. This low value seeks to

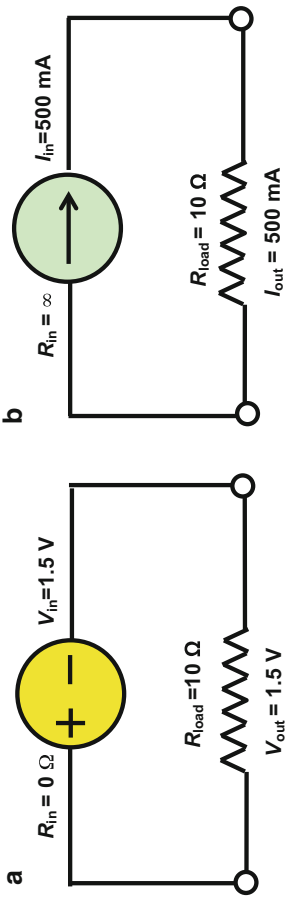

Fig. 5.10 Ideal sources: (**a**) voltage source and (**b**) current source

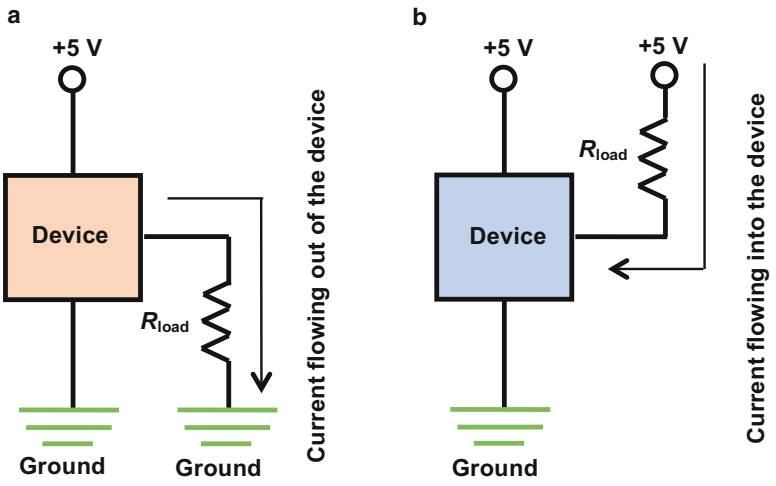

Fig. 5.11 Source and sink: (**a**) current source and (**b**) current sink

keep the input current constant notwithstanding the drive conditions. Current mirrors form the fundamental building blocks of analog circuit design.

Figure 5.12 shows the implementation of a current mirror using MOS transistors. The current mirror consists of two parallel branches. These branches carry approximately equal currents; hence, the name "mirror." The circuit has a compliance voltage. The compliance voltage is the minimum output voltage required for correct circuit operation. For this circuit, the MOSFET Q_2 on the output side (right) should be in the saturation region. For the left MOSFET Q_1, the gate being shorted to drain, $V_{DG}=0$ and $I_{in}=I_{DS1}$. Since the circuit in the diagram forces the same gate-to-source voltage to be applied to transistor Q_2, $V_{GS1}=V_{GS2}$. Hence, the current flowing in the right MOSFET must be the same, i.e., $I_{DS2}=I_{DS1}$, so that $I_{out}=I_{in}$, provided Q_2 is operating in saturation mode, and transistors Q_1 and Q_2 match well in their properties, such as channel length, width, threshold voltage, etc. Temperature should also be same for both Q_1 and Q_2.

5.4.7 Voltage-to-Current Converter

Voltage-to-current converter (VIC) is also called a voltage-controlled current source (VCCS) or transconductance amplifier. Transconductance (transfer conductance) or mutual conductance (g_m) is the ratio of a change in current (ΔI) to change in voltage (ΔV) which produced the current change; hence, $g_m=\Delta I/\Delta V$. The unit of transconductance is siemens or ohm^{-1}.

The VIC circuit (Fig. 5.13) is actually an amplifying arrangement. It generates an output current signal proportional to the input voltage signal. The constant in this

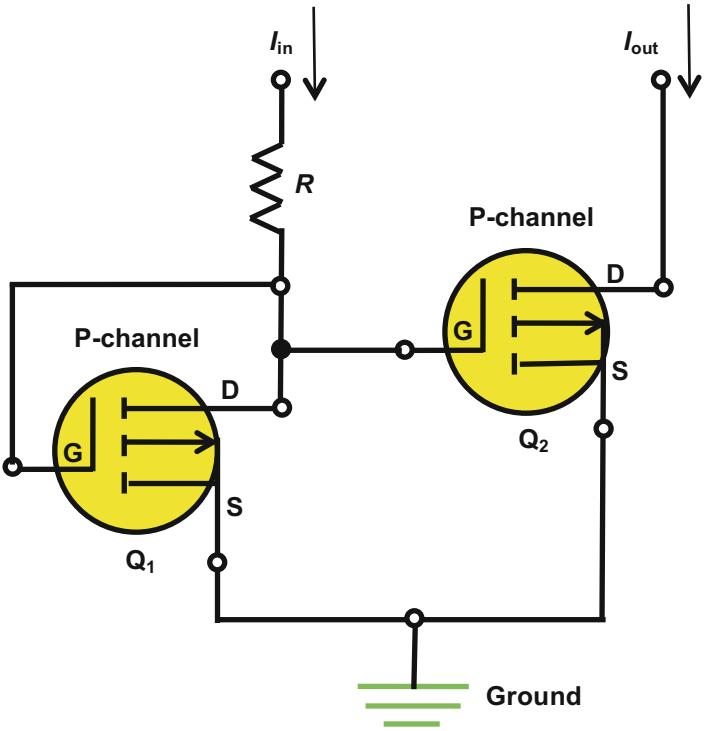

Fig. 5.12 MOS current mirror

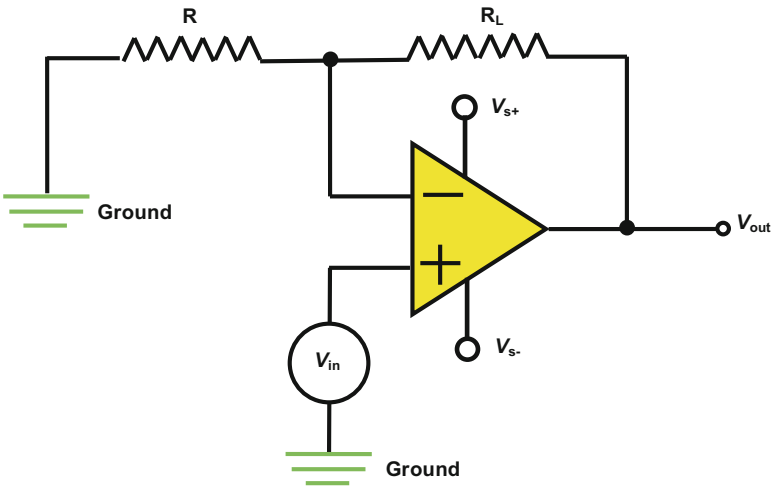

Fig. 5.13 Voltage-to-current converter (transconductance amplifier)

proportionality relation is referred to as transconductance. The circuit employs an OP-AMP configuration furnished with negative feedback. The load resistor R_L is left floating without any connection to ground. The input voltage V_{in} is applied to the non-inverting input terminal of the OP-AMP. The inverting input terminal of OP-AMP is driven by the feedback voltage across the load resistor R_L. Then, the output current flowing through the load resistor R_L is proportional to the input voltage V_{in}. This statement is valid on the presupposition that the OP-AMP has infinite input impedance. The circuit keeps the current fixed at a prescribed value by applying the required voltage of sufficient magnitude to the load resistor to maintain the current constant. Any perturbation of the circuit from its normal functioning, as induced by outside influences, is very small because the operational amplifier has very high impedance.

5.4.8 Voltage Multiplier

It is a specialized rectifier circuit. It is made of combinations of diodes and capacitors. It serves to produce an output DC voltage (V_{dc}) having magnitude equal to either an odd or even multiple of the peak or crest value of alternating input voltage (V_{in}), e.g., 2, 3, 4 … times the peak AC input voltage (V_{in}). A voltage multiplier employs charge pumps. The charge pumps are DC-to-DC converters using capacitors as storage devices to create voltage sources supplying higher voltages without using a transformer. On theoretical grounds, the voltage produced by a voltage multiplier circuit can be indefinitely large. But practically, this is hardly feasible. A major cause is the resulting low current capability. Another factor is the poor voltage regulation achieved. Due to such types of performance degradations accompanying the voltage multiplication, the design of voltage multipliers is not encouraged up to multiplication factors beyond 10 [2].

The full-wave voltage doubler is a symmetrical voltage multiplier circuit (Fig. 5.14). It is assembled from two half-wave rectifier circuits. Its operation can be described with reference to the successive time durations in which the sinusoidal input voltage acquires positive and negative values.

During the period of time in which the input voltage has a positive value, capacitor C_1 charges through diode D_1. This charging proceeds to the peak value of the input voltage (V_p).

Afterwards, during the time interval in which the input voltage acquires a negative value, capacitor C_2 charges through diode D_2 to V_p.

Thus, the total output voltage developed across the capacitors C_1 and C_2 connected in series = voltage across capacitor C_1 (V_p) + voltage across capacitor C_2 (V_p) – the sum of voltage drops across the diodes = $2V_p$, neglecting the forward voltage drops of the diodes.

Referring to the negative and positive half cycles of the sinusoidal input voltage, the half-wave voltage doubler circuit works as follows: For the period in which the input voltage is negative, the diode D_1 operates in a forward-biased mode. It conducts current. Consequently, the pump capacitor C_1 is charged to the maximum

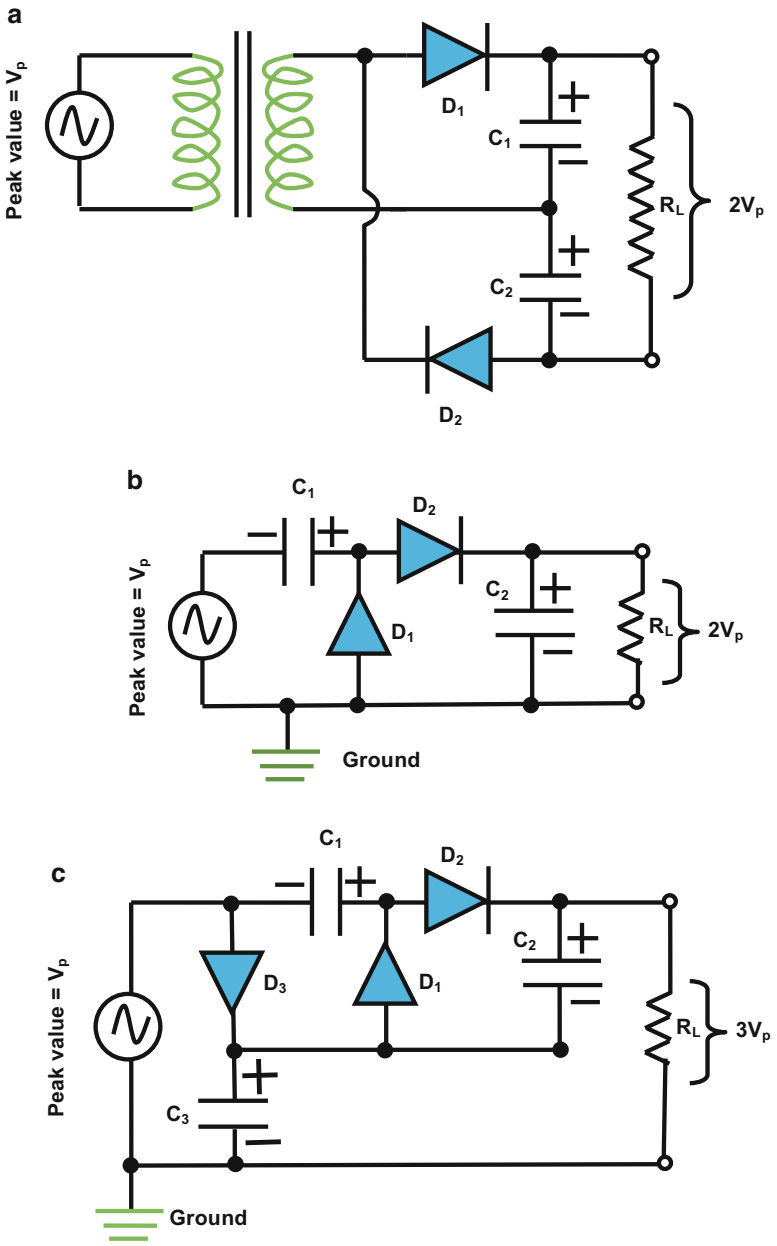

Fig. 5.14 Voltage multipliers: (**a**, **b**) full-wave and half-wave doubler circuits, (**c**) voltage tripler circuit

voltage = peak voltage V_p. With no path left for capacitor C_1 to lose its charge, it has no other option but to retain its charge. It remains in this fully charged condition. Therefore, it acts as a charge storage device in series with the voltage supply. At the same time, diode D_2 conducts via D_1. The resulting current charges the capacitor C_2. During the time interval in which the input voltage is positive, diode D_1 is reverse biased and nonconducting. It blocks the discharging of capacitor C_1. However, the forward-biased diode D_2 allows current to flow. This current charges the capacitor C_2. But a previous voltage = V_p persists across the capacitor C_1. So capacitor C_2 charges to the voltage $2V_p$, twice the peak voltage of input signal.

A voltage tripler circuit contains an ancillary single diode–capacitor stage. This stage is connected to the half-wave voltage doubler circuit explained above. A voltage quadrupler circuit is assembled by connecting together two full-wave voltage doubler circuits in succession. Thus, it is a cascade of two such voltage doubler circuits.

5.4.9 *Boost Converter*

It is also called a step-up converter. It is basically a DC–DC converter circuit providing an output voltage > the input voltage, albeit it supplies a higher voltage at a reduced current because power = voltage × current. So, an increase in voltage irrefutably goes hand in hand with a decrease in available current. Essentially, it is a type of switch-mode power supply (SMPS) used with battery-powered implant circuits. It is used when the battery cannot supply the required high voltage for circuit operation. Moreover, the use of extra batteries is disallowed from weight and volume restrictions [3]. It also takes care of the dropping battery voltage with time. It does so by increasing the battery voltage, thereby extending its service life.

Referring to Fig. 5.15, the circuit operation is explained by examining the incidents that take place during the positive and negative logic levels of the square wave. When the square wave acquires high logic level, the switching power MOSFET turns on. Hence, current starts to flow from the positive terminal of the supply. On the way, it passes through the inductance L_1. It then moves back to the negative terminal of the supply. During the current flow through the inductance, energy is accumulated in the

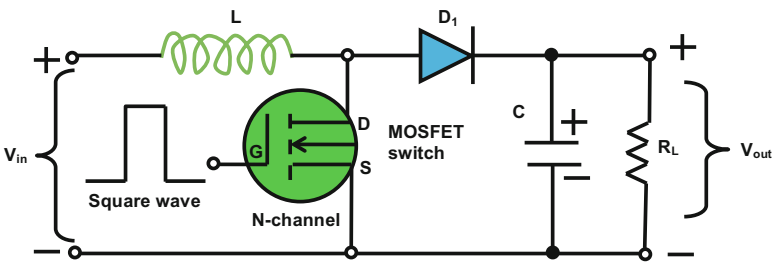

Fig. 5.15 Boost converter circuit

magnetic field surrounding the inductance. Practically, no current flows through the high-impedance path formed by diode D_1, capacitor C_1, and the load.

When the square wave attains the low logic level, the MOSFET is turned off. As a result, current flow in the inductance stops. Its magnetic field begins to collapse. A back electromotive force (EMF) is generated in the opposite direction to the voltage across L_1 in the on-state to maintain the flow of current. This back EMF (V_L) is in series with the supply voltage (V_{in}). Therefore, the higher voltage $= V_{in} + V_L$ forward biases the diode D_1, as the MOSFET is not conducting. This higher voltage minus the voltage dropped across the diode charges the capacitor C_1. It also feeds the load.

The scenario during the next high logic level of the square wave is as follows: By virtue of the charge on C_1, the cathode of D_1 is more positive than its anode. The diode is reverse biased. However, current is still supplied to the load by the charged capacitor C_1. The capacitor C_1 being discharged, it is recharged when the MOSFET again turns off. Thus, a constant voltage is produced across the load. In terms of the input voltage V_{in} and the duty cycle D of the switching square waveform, the DC output voltage is expressed as

$$V_{out} = V_{in} \Big/ (1 - D) \tag{5.1}$$

In an IC boost converter, a suitable fraction of V_{out}, dependent on the resistance ratio R_2/R_3 is compared with a reference voltage within the IC. The aim is to produce an error voltage. This error voltage is the key controlling variable. It is used to vary the duty cycle of the switching oscillator. Therefore, a series of boost voltages can be obtained. Also, these voltages are automatically regulated. The IC contains an internal oscillator and an FET switching transistor. To minimize conduction losses and achieve higher switching speeds, a Schottky diode is used in place of D_1. In order to save power, the IC also has a shutdown (SHDN) facility. This facility disables the boost converter when not required.

5.4.10 Timer Circuit

It is a circuit made from resistors, capacitors, and transistors/timer ICs. It is used for introducing a time delay to switch a circuit on or off. Usually, the user has the freedom to adjust the time delay to trigger the load as desired in the application. This delay is determined by the values of resistive and capacitive components.

5.4.11 Driver Circuit

It is a circuit used to control another circuit or component, e.g., the output driver circuit of an implant serves to source/sink a current at programmed level through the resistive load offered by the body tissue.

5.5 Current-, Voltage-, and Charge-Mode Stimulation

The front-end circuit selects the active electrodes. It either sends and controls current between them or applies and controls voltage across them. The power consumption in any arrangement consists of two parts. The first part is the power utilized by the electronic circuit inside the stimulator for its operation. The second part is the power utilized by the stimulator in delivering the required current or voltage pulse to the tissue for treatment of the malady. By lowering the operating voltage, the internal power consumption by the circuit is decreased. This is possible through careful circuit design. For bipolar electrodes, the instantaneous power consumption is found by multiplication of the voltage V applied between the two electrodes and the resulting current I flowing between the electrodes. In the case of monopolar electrodes, the voltage of interest is that between the active monopolar electrode and the distant ground electrode.

5.5.1 Current-Mode Stimulation

Figure 5.16 shows the basic idea of a current-mode stimulation circuit. In current-mode stimulation, or current-controlled stimulation (CCS), the voltage signal from the microprocessor is fed to a DAC [4]. The output signal from the DAC flows to the VIC. Thus, the stimulator output is a current pulse. The amplitude of this current pulse is controlled by the DAC. The current pulse is applied to the tissue.

In another version [5, 6], the voltage signal from the microprocessor is transformed into a current signal. A VIC is used for this transformation. The obtained current signal is changed into an analog form by the DAC. The analog signal is fed to a current mirror. The output signal obtained from the current mirror is applied to the tissue.

In a current source with high output impedance, any changes in load impedance, i.e., the tissue–electrode impedance, cannot affect the amplitude of current. So, the amount of charge supplied per stimulus is easily maneuvered. If current pulse has magnitude I and it lasts for a duration T, the charge injected into the tissue is $Q = I \times T$. Knowledge of the charge injected and its controllability makes this mode safe in implementation.

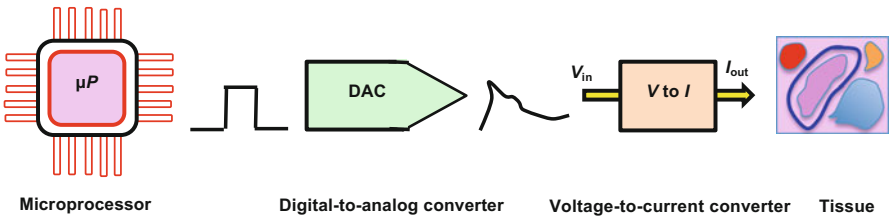

Fig. 5.16 Steps in current-mode stimulation

In reality, the medic programs the current *I*. In an automatic fashion, the front-end circuit adjusts the voltage *V* between the electrodes. So, the current of programmed value *I* flows athwart the electrodes. The current flows all the way through the tissue having impedance *Z*. The value of *Z* is composed of resistive and capacitive components. It is a nonlinear parameter. The parameter varies with time and frequency. It also changes according to any reactions that take place in the tissue with passage of current. However, despite all these complications, the stimulator circuit maintains a constant current flow *I*. The only exceptional case occurs when the maximum voltage available from the stimulator is not able to keep the current constant. In that situation, the current value cannot be kept constant.

5.5.2 *Voltage-Mode Stimulation*

Figure 5.17 illustrates the principle of voltage-mode stimulation. In voltage-mode stimulation, or voltage-controlled stimulation (VCS), the stimulator is an adjustable-gain amplifier. The input voltage of this amplifier is set by the DAC [4]. The load resistance is the sum of the resistances of the conducting lead and the tissue.

In another version of voltage-mode stimulation [7, 8], a rectifier chip is used to charge several capacitors to certain voltages. In this chip, the capacitive voltage repositories are derived from a solo AC voltage on a secondary coil. The capacitors discharge and deliver the charge to the relevant tissue. Controlled synchronous rectification is used in the above system. In synchronous or active rectification, active devices such as power MOSFETs are used in place of junction diodes to increase the efficiency.

The magnitude of current supplied to the tissue varies with interelectrode impedance. Hence, the load impedance variations do not allow easy controllability of the charge supplied to the load. Within safety limits, the voltage can be set by the clinician to obtain the desired result. The clinician has limited options to vary the current *I*. The current must be always restricted within safe limits. Irreversible or damaging effects to the tissue must be always avoided. Naturally, therefore, VCS is less safe than CCS. It must be used with precaution. Safety limits must be clearly mentioned by the manufacturing companies. Nevertheless, its design simplicity and power efficiency make it more appealing than CCS. The power consumption is decreased

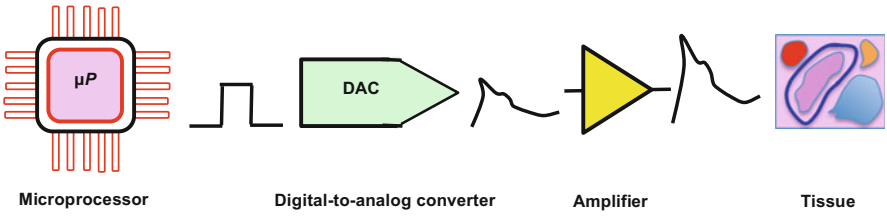

Fig. 5.17 Steps in voltage-mode stimulation

at lower supply voltages. For this reason, cardiac pacemakers and deep brain stimulators use this mode [9].

In actual practice, the clinician chooses a particular voltage V between two electrodes. Then, the current drawn by the tissue is governed by the impedance Z of the tissue. Application of this approach is therefore restricted to limited cases. These are the cases where the temporal Z variations across different electrode pairs are small. These variations must be invariably already known. The efficiency is maximum when the applied voltage V equals the battery voltage. But efficiency falls above or below this value.

5.5.3 *Charge-Mode Stimulation*

In charge-mode stimulation or switched-capacitor-based stimulation, the stimulator consists of a bank of capacitors (Fig. 5.18). This bank of capacitors is charged sequentially from a DC–DC converter. The supply voltage of DC–DC converter is adjustable. So, the total charge on a capacitor is alterable [4]. The capacitors are discharged into the tissue. This discharging action is carried out through several electrodes by digitally controlled switches. Every capacitor can be discharged into the load consecutively. In this way, quantized amounts of charge are impelled into the tissue. The charge injected over each stimulation pulse is measured. For this measurement, the current is integrated over the period of the pulse. But the main issue is that the circuit requires large capacitors. The large capacitors can only be provided in off-chip form. Difficulty in provision of large-value on-chip capacitors is the main disadvantage of this technique. Otherwise, it serves as a unification of

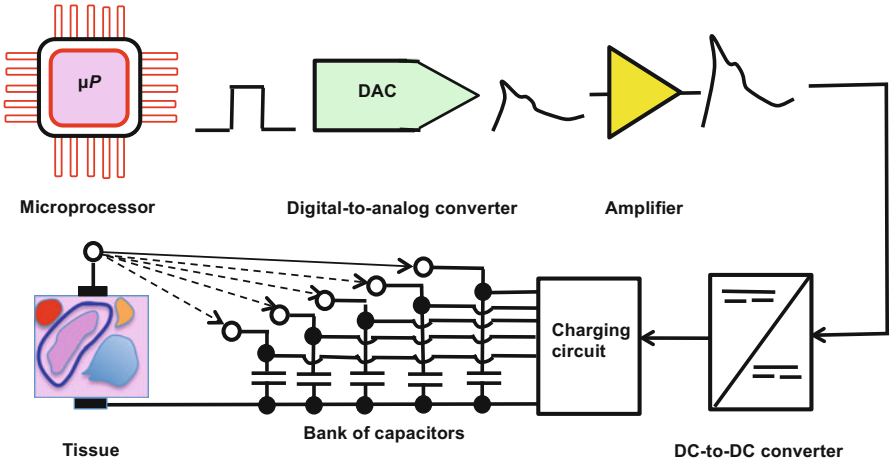

Fig. 5.18 Steps in charge-mode stimulation

Table 5.3 Current-controlled stimulation (CCS), voltage-controlled stimulation (VCS), and charge-controlled stimulation (ChCS) [4]

Sl. No.	Property	CCS	VCS	ChCS
1.	Design	Complex	Simplest	Simple
2.	Safety	High	Poor	Good
3.	Power efficiency	Poor	Highest	Between CCS and VCS

advantages of VCS and CCS methods. It combines the improved power efficiency and safety of VCS with the superior charge-controlling ability of CCS method.

Table 5.3 gives an overall view of CCS, VCS, and ChCS.

5.6 Charge Balancing

In electrical stimulation, charge is transferred from the electrode to the tissue. If a large potential is applied for a long period of time, enormous charge exchange occurs between the electrode and the tissue. The enormous charge exchange leads to flow of a strong faradaic current. The outcome is the inception of irreversible electrochemical processes. These processes are electrolysis, pH changes, electrode dissolution, and tissue destruction. To avoid the onset of these untoward incidents, net charge in each stimulation cycle must be zero. This requires that appearance of any direct currents during stimulation be prevented. From here arises the notion of charge balancing. On first thought, it seems that use of biphasic pulses can straightaway stop the charge unbalance. In biphasic pulses, the first phase is the stimulating phase for evoking the physiological response. The second phase is the reversal phase to quash any electrochemical reactions that are initiated during the first phase. So each stimulation phase is free of DC currents. But the nonuniformities and variations in IC fabrication processes are unavoidable. These result in mismatches between current pulses. The mismatches upset the charge balance. Adoption of preventive means for charge upsetting is therefore essential. Table 5.4 outlines the key features of active and passive charge balancing techniques.

5.6.1 Passive Charge Balancing

5.6.1.1 Blocking Capacitor

A large off-chip DC capacitor in μF range is connected in series with the electrode. By connecting this capacitor, DC currents are stopped from reaching the tissue. Protection against any accidental semiconductor chip failure is also assured. This is because any resulting excessively harmful current cannot flow in the body. It must

Table 5.4 Passive and active charge balancing

Sl. No.	Active charge balancing	Passive charge balancing
1.	A monitoring system is engaged to perceive the remnant voltage on electrode–tissue interface when no current is flowing through the tissue. It also equalizes the charges of the two phases: cathodic and anodic	No monitoring system is used. Balancing is done by charge storing and discharging phases. The connection of capacitors between the output circuits of the pulse generator and the electrodes aids in charge balancing. The capacitors block errant continuous direct current. They are discharged typically after delivery of an individual pulse
2.	No requirement of large off-chip components	Due to restriction in the voltage tolerance, the blocking capacitor must be sufficiently large. Its value is generally approximately several μF. Several off-chip blocking capacitors may be necessary. The area consumption by these capacitors may cause a space crisis in very small implants like those for multichannel retinal stimulation
3.	Usable for different stimulation parameters	Anodic duration is uncontrollable for different stimulation parameters. The large blocking capacitor value lengthens the time constant of discharge. Therefore, it is possible that the discharging phase may terminate prematurely. It may reach the stimulation phase

be remembered that DC current integration will cause voltage buildup on the capacitor. Hence, the capacitor must be regularly discharged.

Among the disadvantages of this technique, it must be mentioned that the value of blocking capacitor has to be the electrode–electrolyte capacitance. Generally, this large capacitor cannot be integrated. It is externally connected with the chip. In multichannel implants, several such capacitors are required. One capacitor is needed for each electrode. A large amount of space is therefore wasted. Lastly, the discharging step for charge balancing is an uncontrolled process.

5.6.1.2 Short-Circuiting of Electrodes

The method is commonly used for a biphasic pulse. It removes any leftover charges present due to mismatching effects. Following each stimulation cycle, short-circuiting of the electrodes helps to discharge them. However, a perplexing situation often arises. It appears because the discharging time is not exactly known. The reason for the inability to know discharging time accurately is the wide variation in current matching and electrode impedances. Further, changes take place in their behavior over a period of time. Nonetheless, the blocking capacitor issues are steered clear off.

5.6.2 Active Charge Balancing

5.6.2.1 Charge Surveillance

This scheme is based on calculation or measurement of charge in the stimulation phase. This knowledge is used in the discharge phase to control its intensity and duration. Thus, the charges in cathodic and anodic phases are compensated.

5.6.2.2 Pulse Insertion

Suppose, after each stimulation phase, the remnant charge on the electrode exceeds a defined safety limit. Then, a corrective short-duration discharging pulse is inserted to remove this charge. This routine is repeated until the electrode charge falls sufficiently to lie within safe bounds.

5.7 Discussion and Conclusions

The criteria for choosing among the three types of stimulation, CCS, VCS, and ChCS, depend on their relative merits and demerits. VCS has the highest power efficiency but less safety. CCS is poor in power efficiency but relatively safe. ChCS has power efficiency between CCS and VCS but is safe like CCS. In charge balancing, human safety is the prime consideration. The main aim of charge balancing is to keep the electrode voltage below the safe limit. It also safeguards against failures.

Review Questions

5.1 What are monopolar and bipolar electrodes? Describe the paths of flow of current in the two types of electrodes. In which type of electrode does the current flow over a greater region of the body?

5.2 What are monophasic and biphasic waveforms? Which kind of waveform is less effective? Which one requires more energy? Which one can be more damaging to the heart?

5.3 Draw the circuit diagram and explain the operation of a CMOS switch. What is meant by "open switch" and "closed switch" positions in this circuit?

5.4 Name three types of DACs. Describe the working of a binary weighted DAC. What is the reason of its poor accuracy?

5.5 How many resistors are required to build an N-bit $R/2R$ ladder DAC? Discuss the relative requirements of binary weighted DAC and N-bit $R/2R$ ladder DAC for high-achieving accuracy.

5.6 What are the two principal modes in which an R/2R ladder network may be operated as a DAC? In what respects do these modes differ?

(continued)

(continued)

5.7 What is an analog-to-digital (ADC) converter? Name two types of ADC circuits.
5.8 What does a flash converter circuit do? Why is it called by this name?
5.9 What is the full form of SAR ADC circuit? Draw its diagram and explain its operation.
5.10 What is a voltage source? Name the dual circuit of the voltage source.
5.11 What are the requirements of the following circuits: (1) a perfect voltage source and (2) a perfect current source?
5.12 How does a current source differ from a current sink?
5.13 What is a current mirror? By what other name is this circuit called?
5.14 Draw the circuit diagram of a MOSFET-based current mirror circuit and explain its working.
5.15 Write two alternative names of a current-to-voltage converter circuit. Explain the working of a VIC circuit using OP-AMP.
5.16 What is the task performed by a voltage multiplier circuit? Is it theoretically possible to increase the voltage indefinitely? What is its practical limitation? Up to what limiting factor is voltage multiplication generally done?
5.17 How is a full-wave voltage doubler circuit constructed from two half-wave rectifier circuits? Explain the working of a half-wave voltage doubler circuit.
5.18 A boost converter provides a higher voltage than the input voltage. What about the output current?
5.19 Draw the circuit diagram of a boost converter circuit and describe its operation. How does an IC boost converter work?
5.20 Describe two approaches used for making a current-mode stimulation circuit. What is the reason for safety in implementation of a current-mode stimulation circuit?
5.21 Describe two schemes for making a voltage-mode stimulation circuit. Why is this mode said to be less safe as compared to the current-mode circuit?
5.22 How does charge-mode stimulation combine the beneficial features of current-controlled and voltage-controlled stimulation circuits? What is the main shortcoming preventing its extensive utilization?
5.23 Why should any charge unbalance be stopped during electrical stimulation? How does the use of a biphasic pulse help in this regard?
5.24 Explain the concept of charge balancing in electrical stimulation. Discuss the main features of active and passive charge balancing. Point out any similarities and dissimilarities between the two methods.
5.25 How is a blocking capacitor used for charge balancing? What protection does it provide against semiconductor chip failure? What is the main limitation of this method?
5.26 How is charge balancing done by short-circuiting electrodes? What is the main difficulty of using this method?
5.27 Describe the charge surveillance and pulse insertion methods of charge balancing.

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