

# Performance Analysis of Scaler SoC for 4K Video Signal

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**Abstract.** This paper considers some issues to implement the scaler SoC. Because the size and power of SoC are constrained, the bit number to represent the coefficients of scaler kernel and LPF should be limited. In addition, the interpolation position should be located at the quantized phases. We analyze the effects of the various constraints in the performance of scaling system. The simulation results provide the guidance to implement the scaler SoC.

**Keywords:** Cubic convolution scaler · Interpolation · System on chip

## 1 Introduction

Scaler is one of the most important modules in image and video broadcasting systems to get a better overview, where the supported resolutions are from QCIF to Ultra High Definition (UHD). In these systems, the original image data is resampled by interpolation schemes according to the resolution supported by the display module.

During last decades, several researchers have proposed various scaling algorithms to increase the quality of the resized images. Among them, the bilinear [1], cubic B-spline [2, 3], and bi-cubic (Cubic Convolution Scaler) [4] are practically used, because they provide the resized image having high quality with simple operations.

When the scaling module is implemented in a System on Chip (SoC), there are several constraints for the size of the internal memory, the number of data bus, the quantized data format and so on. In this paper, we analyze the performances of scaling systems for a variety of constraints about the quantized coefficients of the interpolation filter and the quantized interpolation positions.

This paper is organized as follows. Section 2 explains the scaling algorithm of cubic convolution scaler [4]. The problem to be solved is formulated in Sect. 3, where the constraints about the bit number to represent the coefficients of scaler and LPF are considered to increase the efficiency of implementation of SoC. In addition to the constraints related to the coefficients, the number of phase which is related to the interpolation position is considered to implement the scaler SoC. In Sect. 4, various

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simulation results show that the parameters optimized to implement the scaler SoC provide the reasonable performances. We conclude this paper briefly in Sect. 5.

## 2 Scaling Algorithm

Figure 1 shows the scaling process for the original pixel  $f(x_k)$  and scaled pixel value  $g(y_k)$ , where  $f(x_k)$ 's are the given digital sample values. In this process, the interpolated signal  $\hat{f}(x)$  is represented as follows.

$$\hat{f}(x) = \sum f(x_k)\beta(x - x_k) \tag{1}$$

where  $\beta(x)$  is the interpolation kernel  $x$  and  $x_k$  represent continuous and discrete values, respectively. The scaled pixels  $g(y_k)$  are obtained by sampling the continuous interpolation function, i.e.,  $g(y_k) = \hat{f}(x = y_k)$ . In the scaling process using bi-cubic [4], the kernel is

$$\beta(x, \alpha) = \begin{cases} (\alpha + 2)|x|^3 - (\alpha + 3)|x|^2 + 1, & 0 \leq |x| \leq 1 \\ \alpha|x|^3 - 5\alpha|x|^2 + 8\alpha|x| - 4\alpha, & 1 \leq |x| \leq 2 \end{cases} \tag{2}$$

The scaler module calculates the interpolated pixel values by using a set of its nearest neighboring pixels. If  $f(x_{k-1}), f(x_k), f(x_{k+1}),$  and  $f(x_{k+2})$  are the neighbor pixels, the interpolated function can be calculated as follows.

$$\hat{f}(x) = f(x_{k-1})A_0(s) + f(x_k)A_1(s) + f(x_{k+1})A_2(s) + f(x_{k+2})A_3(s) \tag{3}$$

where

$$\begin{aligned} A_0(s) &= \alpha s^3 - 2\alpha s^2 + \alpha s \\ A_1(s) &= (\alpha + 2)s^3 - (3 + \alpha)s^2 + 1 \\ A_2(s) &= -(\alpha + 2)s^3 + (3 + 2\alpha)s^2 - \alpha s \\ A_3(s) &= -\alpha s^3 + \alpha s^2 \end{aligned} \tag{4}$$

In (3) and (4), the spacing of the sampling grid is assumed as '1'.  $x_k < x < x_{k+1}, s = x - x_k, 0 < s < 1$ . The bi-cubic is known as one of the most efficient schemes, because the complexity of the bi-cubic is low while the performance is comparable to that of cubic B-spline [5].

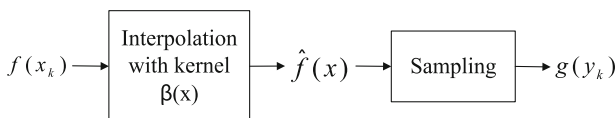


Fig. 1. Scaling process.

### 3 Optimization of Scaler SoC

#### 3.1 Constrained Coefficients of Scaler in SoC

Because the size of SoC chip is limited, it is important to choose the optimal bit number to represent the coefficients of scaler filter. As the bit number increases, the quality of the resized image is more enhanced, because the accuracy of the interpolation increases. If the coefficients are represented with the constrained bit number, those are altered as follows.

$$I_i(s) = (\text{int})A_i(s), \quad i = 0, 1, 2, 3 \quad (5)$$

$$F_{i,N}(s) = (A_i(s) - (\text{int})A_i(s))_N, \quad i = 0, 1, 2, 3 \quad (6)$$

where  $I_i(s)$  is the integer part of  $A_i(s)$ .  $F_{i,N}(s)$  is the number below the decimal point, where  $F_{i,N}(s)$  is represented with  $N$  bits. Based on the altered coefficients, the interpolated function is represented as follows.

$$\begin{aligned} \tilde{f}(x) = & f(x_{k-1})(I_0(s) + F_{0,N}(s)) + f(x_k)(I_1(s) + F_{1,N}(s)) \\ & + f(x_{k+1})(I_2(s) + F_{2,N}(s)) + f(x_{k+2})(I_3(s) + F_{3,N}(s)) \end{aligned} \quad (7)$$

#### 3.2 Quantized Phase of Scaler in SoC

The interpolation position depends on  $s$  in (3)-(7), where  $0 < s < 1$  when no constrained is assigned. However, although it is  $0 < s < 1$ , arbitrary  $s$  value is not permitted in implementation of SoC, because of the limitation about the complexity and the size of chip area. Thus, the phase  $s$  is permitted on the finite  $M$  positions. In this paper, we decide the finite optimal positions to interpolate the new pixel values. It implies that the quantized values of  $s$ ,  $0 < s < 1$ , are used in SoC. When  $M$  positions are permitted for interpolation, the quantized phase is represented as follows.

$$\tilde{s} = (\text{int})(s \times M)/M \quad (8)$$

#### 3.3 Constrained Coefficients of LPF in SoC

When the resolution of the original image is reduced to be displayed on the specific devices, the Low Pass Filter (LPF) should be used to cutoff the components of high-frequency of the original data, before applying the scaling algorithm. In this procedure, the problem related to the bit number to represent the filter coefficients should be considered also. Because the bit number  $L$  to represent the coefficients of LPF affects the quality of the low passed image, the optimal bit number should be used in the implementation of Soc.

## 4 Simulation Results

### 4.1 Performance for Constrained Coefficients of Scaler

Figures 2 and 3 show the performances of the scalers when the bit number to represent the coefficients of scaler is constrained from 2 to 6 bits.

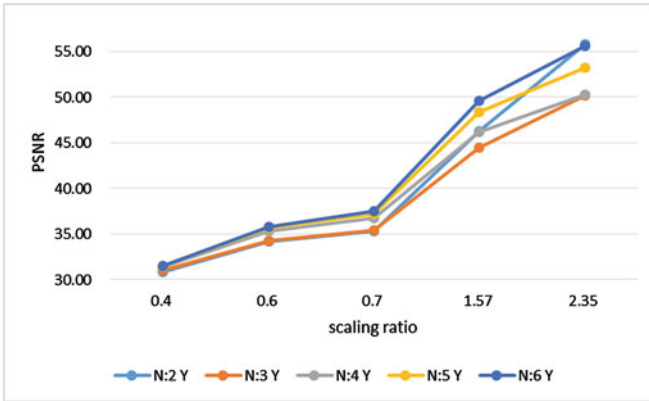


Fig. 2. Image qualities according to the bit number to represent the coefficients of scaler.



Fig. 3. When scaling ratio is 1.57, (a) original image (above), (b) the resized image by bi-cubic without any constraints about the coefficients of scaler (left), (c) the resized image by bi-cubic with  $N = 5$  (right).

### 4.2 Performance for Quantized Phase of Scaler

Figures 4 and 5 show the performances of the scalers when the number of the permitted phases is from 2 to 32.

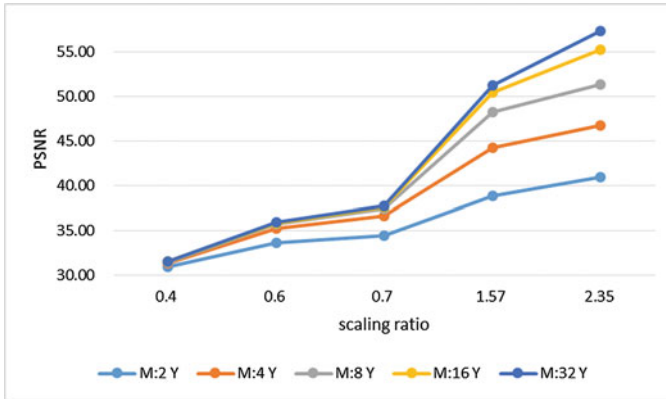


Fig. 4. Image qualities according to the number of the quantized phase in scaling procedure.



Fig. 5. When scaling ratio is 1.57, (a) original image (above), (b) the resized image by bi-cubic without any constraints about the phase (left), (c) the resized image by bi-cubic with  $M = 32$  (right).

### 4.3 Performance for Constrained Coefficients of LPF

Figures 6 and 7 show the performances of the scalers when the bit number to represent the coefficients of LPF is constrained from 2 to 6 bits.

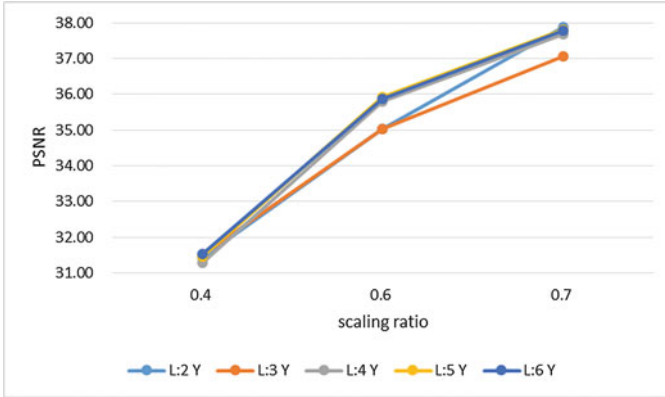


Fig. 6. Image qualities according to the bit number to represent the coefficients of LPF.



Fig. 7. When scaling ratio is 0.7, (a) original image (above), (b) the resized image by bi-cubic without any constraints about the coefficients of LPF (left), (c) the resized image by bi-cubic with  $L = 6$  (right).

## 5 Conclusions

In this paper, we have considered the problems related to implement the scaler SoC. Due to the constraints about the size and power of SoC, the bit number to represent the coefficients of scaler kernel and LPF, and the phase number have been limited. We have analyzed the effects of the various constraints. Based on the computer simulation results, we are guided to implement the SoC efficiently.

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